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HIGHLY INTEGRATED SINGLE-CHIP BASEBAND PROCESSOR FOR GSM HANDSETS

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Abstract

A highly-integrated single-chip baseband processor for next-generation GSM personal communications handsets was designed and implemented. The chip's architecture is suited for new and emerging GSM standards for enhanced full-rate speech, high-rate multislot, and packet-radio service. The chip's architecture and key system design and implementation issues are described.

I. INTRODUCTION

Current-generation GSM handset chip sets utilize at least three main chips: (1) RF/IF transceiver, (2) baseband digital processor, and (3) baseband mixed-signal processor. The mixed signal processor contains the numerous analog-to-digital converters (ADC) and digital-to-analog converters (DAC) required in a GSM handset. This paper describes the architecture of a highly integrated baseband chip which includes both baseband digital processing and mixed signal processing functions. All drivers and interfaces for external devices such as LCD controller, microphone, speaker, and data terminal equipment were also integrated into the baseband chip in order to reduce handset parts count. The design objective was to reduce GSM handset electronics to two main processing chips, (1) the highly integrated baseband chip, and (2) an RF chip, with a minimum of additional components required.

A design requirement imposed on the single-chip baseband processor was support for certain new and emerging GSM standards: (1) enhanced full-rate speech (EFRS) service [1] for higher speech quality than the standard full-rate speech (FRS) service, (2) general packet radio service (GPRS) [2] which is suited for the bursty communications of Internet services, (3) GSM Class 12 multislot operation which achieves up to four-fold increase in data rate, and (4) GSM/DCS1800 multiband operation. Another requirement for the baseband processor was achievement of very low power consumption for very long talk and standby times on a standard handset battery.

II. ARCHITECTURE

A block diagram of the architecture for the highly integrated baseband processing chip is illustrated in Figure 1. Software processing is partitioned between (1) the Mobil Station Processor (MSP) which runs on a RISC core, and (2) the Radio Interface Processor (RIP) which runs on a DSP core. The RIP performs or supervises GSM physical layer processing which includes speech transcoding, channel block and convolutional coding, interleaving, GMSK modulation, and equalization/demodulation. The equalizer is a Viterbi maximum-likelihood sequence estimator modified to improve joint equalizer and convolutional decoder performance in fading GSM channels. Computationally intensive functions were implemented in hardware as RIP coprocessors to minimize power consumption. The onboard ROM contains RIP program and data memory including speech transcoding algorithms for both FRS and EFRS service. The RIP supervises transceiver control functions such as power amplifier ramping, synthesizer frequency selection, and automatic gain control via respective DAC's. The RIP also supervises operation of the mixed-signal processing of the voice band codec and baseband codec hardware.

The MSP performs man-machine interface (MMI) and GSM protocol stack functions for the handset. The network layer protocol functions include connection management, mobility management and radio resource management. In the application layer the MSP manages applications such as Short Message Service (SMS), Supplementary Services and Data/FAX services. SMS allows the sending and receiving of short text messages. Supplementary Services modify or supplement the basic telecommunication services such as call forwarding, call waiting, call hold, calling line identification presentation, etc. The Data/FAX services allow the handset to be connected to a PC or personal digital assistant via the UART interface without the need for an external PC card/modem..

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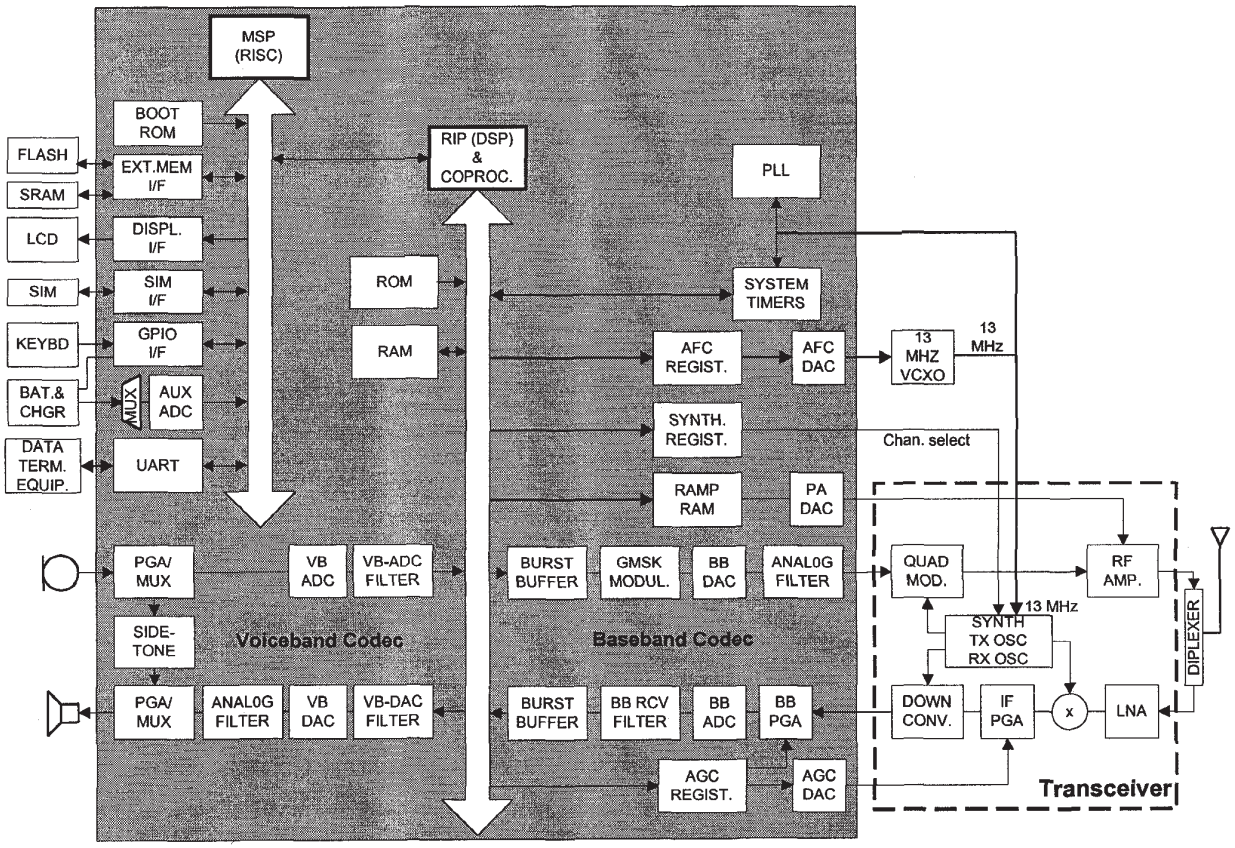

Figure 1. Block Diagram of the Single-Chip Baseband GSM Processor

The program and data memory for the MSP reside in external FLASH resulting in flexibility for addition or modifications for new GSM services and MMI features. The MSP and RIP communicate through shared memory.

III. KEY SYSTEM DESIGN ISSUES

The RIP coprocessors generally minimized power consumption for computationally intensive operations, and the higher data rates of Class 12 multislot operation are supported with minimal increase in power consumption. RIP processing capacity is sufficient to support computationally intensive EFRS speech transcoding so that addition of a second DSP as in the case of some current-generation handset architectures is unnecessary. A flexible transceiver control interface is highly desirable to support a wide selection of transceivers, and to support multiband operation. The desired flexibility is provided by progammable transceiver control interfaces. Special design measures such as shielding for critical analog circuits were required to achieve the necessary isolation of digital and analog sections for this highly integrated chip. Scheduled power down for all idle processing sections is performed to achieve very long talk and standby times for GSM handsets.

IV. CONCLUSIONS

The architecture of a GSM single-chip baseband processor implementation was described. The chip is designed to support new GSM standards while maintaining very low power consumption.

Acknowledgements

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References

[1] ETSI, "GSM 06.60 Enhanced Full Rate Speech Transcoding", March 1997

[2] ETSI, "GSM 03.64 Overall Description of the GPRS Radio Interface, Stage 2", v. 5.0.0, July 1997.