

## **LOW NOISE AMPLIFIERS FOR CARRIER AGGREGATION**

### **I. Claim of Priority under 35 U.S.C. §119**

[0001] The present Application for Patent claims priority to Provisional U.S. Application Serial No. 61/652,064, entitled “LOW NOISE AMPLIFIERS FOR CARRIER AGGREGATION,” filed May 25, 2012, assigned to the assignee hereof, and expressly incorporated herein by reference.

## **BACKGROUND**

### **I. Field**

[0002] The present disclosure relates generally to electronics, and more specifically to low noise amplifiers (LNAs).

### **II. Background**

[0003] A wireless device (e.g., a cellular phone or a smartphone) in a wireless communication system may transmit and receive data for two-way communication. The wireless device may include a transmitter for data transmission and a receiver for data reception. For data transmission, the transmitter may modulate a radio frequency (RF) carrier signal with data to obtain a modulated RF signal, amplify the modulated RF signal to obtain an amplified RF signal having the proper output power level, and transmit the amplified RF signal via an antenna to a base station. For data reception, the receiver may obtain a received RF signal via the antenna and may amplify and process the received RF signal to recover data sent by the base station.

[0004] A wireless device may support carrier aggregation, which is simultaneous operation on multiple carriers. A carrier may refer to a range of frequencies used for communication and may be associated with certain characteristics. For example, a carrier may be associated with system information describing operation on the carrier. A carrier may also be referred to as a component carrier (CC), a frequency channel, a cell, etc. It is desirable to efficiently support carrier aggregation by the wireless device.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

- [0005] FIG. 1 shows a wireless device communicating with a wireless system.
- [0006] FIGS. 2A to 2D show four examples of carrier aggregation (CA).
- [0007] FIG. 3 shows a block diagram of the wireless device in FIG. 1.
- [0008] FIGS. 4A and 4B show a receiver supporting intra-band CA.
- [0009] FIGS. 5A and 5B show a receiver supporting intra-band CA and inter-band CA.
- [0010] FIGS. 6A to 6C show an LNA with inductive degeneration and cascode shutoff.
- [0011] FIG. 7 shows an LNA with inductive degeneration, cascode shutoff, and resistive feedback.
- [0012] FIG. 8A shows an LNA with a separate input attenuation circuit for each amplifier stage.
- [0013] FIG. 8B shows an LNA with a shared input attenuation circuit for two amplifier stages.
- [0014] FIG. 9 shows an LNA with a tunable input matching circuit.
- [0015] FIGS. 10 to 11C show several exemplary designs of a multiple-input multiple-output (MIMO) LNA.
- [0016] FIGS. 12A to 12F show six exemplary designs of a tunable input matching circuit.
- [0017] FIG. 13 shows a process for receiving signals in a wireless system.

### **DETAILED DESCRIPTION**

- [0018] The detailed description set forth below is intended as a description of exemplary designs of the present disclosure and is not intended to represent the only designs in which the present disclosure can be practiced. The term “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any design described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other designs. The detailed description includes specific details for the purpose of providing a thorough understanding of the exemplary designs of the present disclosure. It will be apparent to those skilled in the art that the exemplary designs described herein may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form in order to avoid obscuring the novelty of the exemplary designs presented herein.

- [0019] LNAs supporting carrier aggregation are disclosed herein. These LNAs may have better performance and may be used for various types of electronic devices such as wireless communication devices.
- [0020] **FIG. 1** shows a wireless device 110 communicating with a wireless communication system 120. Wireless system 120 may be a Long Term Evolution (LTE) system, a Code Division Multiple Access (CDMA) system, a Global System for Mobile Communications (GSM) system, a wireless local area network (WLAN) system, or some other wireless system. A CDMA system may implement Wideband CDMA (WCDMA), cdma2000, or some other version of CDMA. For simplicity, FIG. 1 shows wireless system 120 including two base stations 130 and 132 and one system controller 140. In general, a wireless system may include any number of base stations and any set of network entities.
- [0021] Wireless device 110 may also be referred to as a user equipment (UE), a mobile station, a terminal, an access terminal, a subscriber unit, a station, etc. Wireless device 110 may be a cellular phone, a smartphone, a tablet, a wireless modem, a personal digital assistant (PDA), a handheld device, a laptop computer, a smartbook, a netbook, a cordless phone, a wireless local loop (WLL) station, a Bluetooth device, etc. Wireless device 110 may be capable of communicating with wireless system 120. Wireless device 110 may also be capable of receiving signals from broadcast stations (e.g., a broadcast station 134), signals from satellites (e.g., a satellite 150) in one or more global navigation satellite systems (GNSS), etc. Wireless device 110 may support one or more radio technologies for wireless communication such as LTE, cdma2000, WCDMA, GSM, 802.11, etc.
- [0022] Wireless device 110 may support carrier aggregation, which is operation on multiple carriers. Carrier aggregation may also be referred to as multi-carrier operation. Wireless device 110 may be able to operate in low-band from 698 to 960 megahertz (MHz), mid-band from 1475 to 2170 MHz, and/or high-band from 2300 to 2690 and 3400 to 3800 MHz. Low-band, mid-band, and high-band refer to three groups of bands (or band groups), with each band group including a number of frequency bands (or simply, “bands”). Each band may cover up to 200 MHz and may include one or more carriers. Each carrier may cover up to 20 MHz in LTE. LTE Release 11 supports 35 bands, which are referred to as LTE/UMTS bands and are listed in 3GPP TS 36.101.

Wireless device 110 may be configured with up to 5 carriers in one or two bands in LTE Release 11.

[0023] In general, carrier aggregation (CA) may be categorized into two types - intra-band CA and inter-band CA. Intra-band CA refers to operation on multiple carriers within the same band. Inter-band CA refers to operation on multiple carriers in different bands.

[0024] **FIG. 2A** shows an example of contiguous intra-band CA. In the example shown in FIG. 2A, wireless device 110 is configured with four contiguous carriers in the same band, which is a band in low-band. Wireless device 110 may receive transmissions on multiple contiguous carriers within the same band.

[0025] **FIG. 2B** shows an example of non-contiguous intra-band CA. In the example shown in FIG. 2B, wireless device 110 is configured with four non-contiguous carriers in the same band, which is a band in low-band. The carriers may be separated by 5 MHz, 10 MHz, or some other amount. Wireless device 110 may receive transmissions on multiple non-contiguous carriers within the same band.

[0026] **FIG. 2C** shows an example of inter-band CA in the same band group. In the example shown in FIG. 2C, wireless device 110 is configured with four carriers in two bands in the same band group, which is low-band. Wireless device 110 may receive transmissions on multiple carriers in different bands in the same band group (e.g., low-band in FIG. 2C).

[0027] **FIG. 2D** shows an example of inter-band CA in different band groups. In the example shown in FIG. 2D, wireless device 110 is configured with four carriers in two bands in different band groups, which include two carriers in one band in low-band and two additional carriers in another band in mid-band. Wireless device 110 may receive transmissions on multiple carriers in different bands in different band groups (e.g., low-band and mid-band in FIG. 2D).

[0028] FIGS. 2A to 2D show four examples of carrier aggregation. Carrier aggregation may also be supported for other combinations of bands and band groups. For example, carrier aggregation may be supported for low-band and high-band, mid-band and high-band, high-band and high-band, etc.

[0029] **FIG. 3** shows a block diagram of an exemplary design of wireless device 110 in FIG. 1. In this exemplary design, wireless device 110 includes a transceiver 320 coupled to a primary antenna 310, receivers 322 coupled to a secondary antenna 312,

and a data processor/controller 380. Transceiver 320 includes multiple (K) receivers 330aa to 330ak and multiple (K) transmitters 360a to 360k to support multiple bands, carrier aggregation, multiple radio technologies, etc. Receivers 322 include multiple (M) receivers 330ba to 330bm to support multiple bands, carrier aggregation, multiple radio technologies, receive diversity, MIMO transmission, etc.

**[0030]** In the exemplary design shown in FIG. 3, each receiver 330 includes input circuits 332, an LNA 340, and receive circuits 342. For data reception, antenna 310 receives signals from base stations and/or other transmitter stations and provides a received RF signal, which is routed through switches/duplexers 324 and provided to a selected receiver. The description below assumes that receiver 330aa is the selected receiver. Within receiver 330aa, the received RF signal is passed through input circuits 332aa, which provides an input RF signal to an LNA 340aa. Input circuits 332aa may include a matching circuit, a receive filter, etc. LNA 340aa amplifies the input RF signal and provides an output RF signal. Receive circuits 342aa amplify, filter, and downconvert the output RF signal from RF to baseband and provide an analog input signal to data processor 380. Receive circuits 332aa may include mixers, a filter, an amplifier, a matching circuit, an oscillator, a local oscillator (LO) generator, a phase locked loop (PLL), etc. Each remaining receiver 330 in transceiver 320 and each receiver 330 in receivers 322 may operate in similar manner as receiver 330aa in transceiver 320.

**[0031]** In the exemplary design shown in FIG. 3, each transmitter 360 includes transmit circuits 362, a power amplifier (PA) 364, and output circuits 366. For data transmission, data processor 380 processes (e.g., encodes and modulates) data to be transmitted and provides an analog output signal to a selected transmitter. The description below assumes that transmitter 360a is the selected transmitter. Within transmitter 360a, transmit circuits 362a amplify, filter, and upconvert the analog output signal from baseband to RF and provide a modulated RF signal. Transmit circuits 362a may include mixers, an amplifier, a filter, a matching circuit, an oscillator, an LO generator, a PLL, etc. A PA 364a receives and amplifies the modulated RF signal and provides an amplified RF signal having the proper output power level. The amplified RF signal is passed through output circuits 366a, routed through switches/duplexers 324, and transmitted via antenna 310. Output circuits 366a may include a matching circuit, a transmit filter, a directional coupler, etc.

- [0032] FIG. 3 shows an exemplary design of receivers 330 and transmitters 360. A receiver and a transmitter may also include other circuits not shown in FIG. 3, such as filters, matching circuits, etc. All or a portion of transceiver 320 and receivers 322 may be implemented on one or more analog integrated circuits (ICs), RF ICs (RFICs), mixed-signal ICs, etc. For example, LNAs 340, receive circuits 342, and transmit circuits 362 may be implemented on one module, which may be an RFIC, etc. Switches/duplexers 324, switches/filters 326, input circuits 332, output circuits 366, and PAs 364 may be implemented on another module, which may be a hybrid module, etc. The circuits in receivers 330 and transmitters 360 may also be implemented in other manners.
- [0033] Data processor/controller 380 may perform various functions for wireless device 110. For example, data processor 380 may perform processing for data being received via receivers 330 and data being transmitted via transmitters 360. Controller 380 may control the operation of switches/duplexers 324, switches/filters 326, input circuits 332, LNAs 340, receive circuits 342, transmit circuits 362, PAs 364, output circuits 366, or a combination thereof. A memory 382 may store program codes and data for data processor/controller 380. Data processor/controller 380 may be implemented on one or more application specific integrated circuits (ASICs) and/or other ICs.
- [0034] Wireless device 110 may receive multiple transmissions from one or more cells/base stations on multiple carriers at different frequencies for carrier aggregation. For intra-band CA, the multiple transmissions are sent on multiple carriers in the same band. For inter-band CA, the multiple transmissions are sent on multiple carriers in different bands.
- [0035] FIG. 4A shows a block diagram of an exemplary design of a receiver 400 that includes a CA LNA 440 supporting no CA and intra-band CA. CA LNA 440 may be used for one or more LNAs 340 within wireless device 110 in FIG. 3.
- [0036] At receiver 400, an antenna 410 receives transmissions on multiple carriers in the same band and provides a received RF signal. The received RF signal is routed through switches/duplexers 424 and provided as a receiver input signal, RXin, to an input matching circuit 432. Matching circuit 432 performs power and/or impedance matching between CA LNA 440 and either switches/duplexers 424 or antenna 410 for one or more bands of interest. Matching circuit 432, which may be part of one of input circuits 332 in FIG. 3, provides an input RF signal, RFin, to CA LNA 440.

- [0037] CA LNA 440 receives the input RF signal from matching circuit 432, amplifies the input RF signal, and provides up to M output RF signals, RFout1 to RFoutM, via up to M LNA outputs, where  $M > 1$ . M load circuits 490a to 490m are coupled to the M LNA outputs. Each load circuit 490 may include one or more inductors, capacitors, transistors, mixers, etc. Each load circuit 490 may be part of one of receive circuits 342 in FIG. 3. Each output RF signal may be provided to one or more mixers within one load circuit 490 and may be downconverted by the associated mixer(s) such that transmissions on one or more carriers of interest are downconverted from RF to baseband.
- [0038] A CA LNA, such as CA LNA 440 in FIG. 4A, may operate in a non-CA mode or a CA mode at any given moment. In the non-CA mode, the CA LNA operates in a 1-input 1-output ( $1 \times 1$ ) configuration, receives one input RF signal comprising one or more transmissions on one set of carriers, and provides one output RF signal to one load circuit. In the CA mode, the CA LNA operates in a  $1 \times M$  configuration, receives one input RF signal comprising multiple transmissions on M sets of carriers, and provides M output RF signals to M load circuits, one output RF signal for each set of carriers, where  $M > 1$ . Each set of carriers may include one or more carriers in one band.
- [0039] FIG. 4B shows a schematic diagram of an exemplary design of a CA LNA 440x supporting no CA and intra-band CA on two sets of carriers in the same band. CA LNA 440x is one exemplary design of CA LNA 440 in FIG. 4A. In the exemplary design shown in FIG. 4B, CA LNA 440x receives an input RF signal from input matching circuit 432 and provides up to two output RF signals, RFout1 and RFout2, for up to two sets of carriers. The first output RF signal is provided to a load circuit 490x, and the second output RF signal is provided to a load circuit 490y.
- [0040] In the exemplary design shown in FIG. 4B, load circuit 490x includes two mixers 492a and 492b coupled to two baseband filters 494a and 494b, respectively. Mixers 492a and 492b implement a quadrature downconverter for a first set of carriers. Mixer 492a receives the first output RF signal from CA LNA 440x and an inphase LO signal, ILO1, at a first mixing frequency for the first set of carriers. Mixer 492a downconverts the first output RF signal with the ILO1 signal and provides an inphase (I) downconverted signal. Mixer 492b receives the first output RF signal from CA LNA 440x and a quadrature LO signal, QLO1, at the first mixing frequency for the first set of carriers. Mixer 492b downconverts the first output RF signal with the QLO1 signal and

provides a quadrature (Q) downconverted signal. Filters 494a and 494b receive and filter the I and Q downconverted signals from mixers 492a and 492b, respectively, and provide I and Q baseband signals, Vout1, for the first set of carriers.

[0041] Mixers 492c and 492d and filters 494c and 494d within load circuit 490y similarly process the second output RF signal from CA LNA 440x and provide I and Q baseband signals for a second set of carriers. Mixers 492c and 492d receive the second RF signal and I and Q LO signals, respectively, at a second mixing frequency for the second set of carriers. Mixers 492c and 492d downconvert the second output RF signal with the I and Q LO signals and provide the I and Q downconverted signals, respectively. Filters 494c and 494d receive and filter the I and Q downconverted signals from mixers 492c and 492d, respectively, and provide I and Q baseband signals, Vout2, for the second set of carriers.

[0042] FIG. 4B shows an exemplary design of load circuits 490x and 490y. A load circuit may also comprise different and/or additional circuits. For example, a load circuit may include an amplifier coupled before the mixers, or between the mixers and the filters, or after the filters.

[0043] FIG. 5A shows a block diagram of an exemplary design of a receiver 500 that includes a MIMO LNA 540 supporting no CA, intra-band CA, and inter-band CA. MIMO LNA 540 may be used for one or more LNAs 340 within wireless device 110 in FIG. 3.

[0044] At receiver 500, an antenna 510 receives transmissions on one or more carriers in the same band or different bands and provides a received RF signal to switches/duplexers 524. Switches/duplexers 524 provide up to N receiver input signals, RXin1 to RXinN, to up to N input matching circuits 532a to 532n, respectively, where  $N > 1$ . Matching circuits 532a to 532n may be part of one or more input circuits 332 in FIG. 3. Each matching circuit 532 performs power and/or impedance matching between MIMO LNA 540 and either switches/duplexers 524 or antenna 510 for one or more bands of interest. The N matching circuits 532a to 532n may be designed for different bands and may provide up to N input RF signals, RFin1 to RFinN.

[0045] MIMO LNA 540 receives up to N input RF signals and amplifies (i) one input RF signal for no CA or intra-band CA or (ii) multiple input RF signals for inter-band CA. MIMO LNA 540 provides up to M output RF signals, RFout1 to RFoutM, via up to M LNA outputs. M load circuits 590a to 590m are coupled to the M LNA outputs.



Each load circuit 590 may include one or more inductors, capacitors, transistors, mixers, etc. Each output RF signal may be provided to one or more mixers within one load circuit 590 and may be downconverted by the associated mixer(s) such that one or more transmissions on one or more carriers of interest are downconverted from RF to baseband.

[0046] A MIMO LNA, such as MIMO LNA 540 in FIG. 5A, may operate in a non-CA mode, an intra-band CA mode, or an inter-band CA mode at any given moment. In the non-CA mode, the MIMO LNA operates in a  $1 \times 1$  configuration, receives one input RF signal comprising one or more transmissions on one set of carriers, and provides one output RF signal to one load circuit. In the intra-band CA mode, the MIMO LNA operates in a  $1 \times M$  configuration, receives one input RF signal comprising multiple transmissions on  $M$  sets of carriers in the same band, and provides  $M$  output RF signals to  $M$  load circuits, one output RF signal for each set of carriers, where  $M > 1$ . In the inter-band CA mode, the MIMO LNA operates in an  $N \times M$  configuration, receives  $N$  input RF signals comprising multiple transmissions on  $M$  sets of carriers in up to  $N$  different bands, and provides  $M$  output RF signals to  $M$  load circuits, where  $M > 1$  and  $N > 1$ . The  $N$  input RF signals may correspond to up to  $N$  different bands.

[0047] A MIMO LNA, such as MIMO LNA 540 in FIG. 5A, may be used to receive transmissions on multiple carriers at different frequencies. A MIMO LNA may include multiple outputs providing multiple output RF signals for different carriers or different sets of carriers of interest. A MIMO LNA is different from LNAs used to receive a MIMO transmission sent from multiple transmit antennas to multiple receive antennas. An LNA for a MIMO transmission typically has (i) one input receiving one input RF signal from one receive antenna and (ii) one output providing one output RF signal. The multiple outputs of a MIMO LNA thus cover frequency dimension whereas the outputs of LNAs used for a MIMO transmission cover spatial dimension.

[0048] **FIG. 5B** shows a schematic diagram of an exemplary design of a MIMO LNA 540x supporting no CA, intra-band CA, and inter-band CA on two sets of carriers in different bands. Each set of carriers may include one or more carriers in one band. MIMO LNA 540x is one exemplary design of MIMO LNA 540 in FIG. 5A. Matching circuits 532a and 532b may receive (i) the same receiver input signal from one antenna or (ii) different receiver input signals from one or more antennas. Hence, the RXin2

signal may or may not be equal to the RXin1 signal in FIG. 5B. Each matching circuit 532 performs power and/or impedance matching for one or more bands of interest.

[0049] In the exemplary design shown in FIG. 5B, MIMO LNA 540x includes two amplifier stages 550a and 550b for two sets of carriers. Amplifier stage 550a receives and amplifies the first input RF signal from matching circuit 532a and provides a first output RF signal, RFout1, for a first set of carriers. Amplifier stage 550b receives and amplifies the second input RF signal from matching circuit 532b and provides a second output RF signal, RFout2, for a second set of carriers. Although not shown in FIG. 5B for simplicity, MIMO LNA 540x may include circuitry to route an output RF signal from each amplifier stage 550 to any one of load circuits 590x and 590y.

[0050] In the exemplary design shown in FIG. 5B, load circuit 590x includes two mixers 592a and 592b coupled to two baseband filters 594a and 594b, respectively. Mixer 592a receives the first output RF signal from amplifier stage 550a and an inphase LO signal, ILO1, at a first mixing frequency for the first set of carriers. Mixer 592a downconverts the first output RF signal with the ILO1 signal and provides an I downconverted signal. Mixer 592b receives the first output RF signal from amplifier stage 550b and a quadrature LO signal, QLO1, at the first mixing frequency for the first set of carriers. Mixer 592b downconverts the first output RF signal with the QLO1 signal and provides a Q downconverted signal. Filters 594a and 594b receive and filter the I and Q downconverted signals from mixers 592a and 592b, respectively, and provide I and Q baseband signals, Vout1, for the first set of carriers.

[0051] Mixers 592c and 592d and filters 594c and 594d within load circuit 590y similarly process the second output RF signal from amplifier stage 550b and provide I and Q baseband signals, Vout2, for a second set of carriers.

[0052] CA LNA 440 in FIG. 4A may be implemented in various manners. Some exemplary designs of CA LNA 440 are described below. CA LNA 440 may also be implemented with transistors of various types. Some exemplary designs of CA LNA 440 using N-channel metal oxide semiconductor (NMOS) transistors are described below.

[0053] **FIG. 6A** shows a schematic diagram of an exemplary design of a CA LNA 640a with inductive degeneration and cascode shutoff. CA LNA 640a is one exemplary design of CA LNA 440 in FIG. 4A. CA LNA 640a includes two amplifier stages 650a and 650b coupled to a common input matching circuit 632 and to two load circuits 690a

and 690b. Matching circuit 632 receives a receiver input signal, RXin, performs input matching for CA LNA 640a, and provides an input RF signal, RFin. Matching circuit 632 may correspond to matching circuit 432 in FIG. 4A. Load circuits 690a and 690b may correspond to load circuits 490a and 490m in FIG. 4A. CA LNA 640a receives the input RF signal, which may include transmissions on two sets of carriers, with each set including one or more carriers.

**[0054]** In the exemplary design shown in FIG. 6A, amplifier stage 650a includes a source degeneration inductor 652a, a gain transistor 654a, and a cascode transistor 656a. Gain transistor 654a and cascode transistor 656a may be implemented with NMOS transistors (as shown in FIG. 6A) or with transistors of other types. Gain transistor 654a has its gate coupled to matching circuit 632 and its source coupled to one end of inductor 652a. The other end of inductor 652a is coupled to circuit ground. Cascode transistor 656a has its source coupled to the drain of gain transistor 654a and its drain coupled to load circuit 690a. A switch 658a has its input port coupled to the gate of cascode transistor 656a, its first output port coupled to a bias voltage, Vcasc, and its second output port coupled to circuit ground. Amplifier stage 650b includes a source degeneration inductor 652b, a gain transistor 654b, a cascode transistor 656b, and a switch 658b, which are coupled in similar manner as inductor 652a, gain transistor 654a, cascode transistor 656a, and switch 658a in amplifier stage 650a.

**[0055]** For simplicity, FIG. 6A shows CA LNA 640a including two amplifier stages 650a and 650b for two sets of carriers. Amplifier stages 650a and 650b may be independently enabled or disabled via switches 658a and 658b, respectively. CA LNA 640a may include more than two amplifier stages 650 for more than two sets of carriers.

**[0056]** An input RF signal may include transmissions on multiple sets of carriers in the same band and may be referred to as a carrier-aggregated RF signal. The carrier-aggregated RF signal may be downconverted using LO signals at different frequencies corresponding to the center frequencies of the multiple sets of carriers on which the transmissions are sent. The carrier-aggregated RF signal may be split at the LNA input in order to achieve good LO-LO isolation between the LO signals for the multiple sets of carriers. CA LNA 640a includes two amplifier stages 650a and 650b to amplify the carrier-aggregated RF signal and provide two output RF signals to two separate downconverters in the two load circuits 690a and 690b.

- [0057] CA LNA 640a may operate in a non-CA mode or a CA mode at any given moment. In the non-CA mode, CA LNA 640a receives transmissions on one set of carriers and provides one output RF signal to one load circuit. In the CA mode, CA LNA 640a receives transmissions on two sets of carriers and provides two output RF signals to two load circuits, one output RF signal for each set of carriers.
- [0058] **FIG. 6B** shows operation of CA LNA 640a in the CA mode. In the CA mode, both amplifier stages 650a and 650b are enabled by connecting the gate of cascode transistor 656a to the  $V_{casc}$  voltage via switch 658a and coupling the gate of cascode transistor 656b to the  $V_{casc}$  voltage via switch 658b. Amplifier stage 650a amplifies the input RF signal and provides the first output RF signal to load circuit 690a. Amplifier stage 650b amplifies the input RF signal and provides the second output RF signal to load circuit 690b.
- [0059] **FIG. 6C** shows operation of CA LNA 640a in the non-CA mode. In the non-CA mode, only one amplifier stage is enabled, and the other amplifier stage is disabled. In the example shown in FIG. 6C, amplifier stage 650a is enabled by connecting the gate of cascode transistor 656a to the  $V_{casc}$  voltage via switch 658a, and amplifier stage 650b is disabled by shorting the gate of cascode transistor 656b to circuit ground via switch 658b. Amplifier stage 650a amplifies the input RF signal and provides an output RF signal to load circuit 690a.
- [0060] In another configuration of the non-CA mode, amplifier stage 650b is enabled, and amplifier stage 650a is disabled (not shown in FIG. 6C). In this configuration, amplifier stage 650b amplifies the input RF signal and provides an output RF signal to load circuit 690b.
- [0061] In the exemplary design shown in FIG. 6A, separate source degeneration inductors 652a and 652b are used for amplifier stages 650a and 650b in order to reduce interaction between the two amplifier stages and to help reduce noise figure (NF) degradation. Source degeneration inductors 652a and 652b may also improve linearity of amplifier stages 650a and 650b and help input impedance matching of CA LNA 640a. Inductors 652a and 652b may have the same value or different values. The values of inductors 652a and 652b may be selected (e.g., independently) based on a trade-off between voltage gain and linearity in the CA mode and the non-CA mode.
- [0062] As shown in FIG. 6A, a variable capacitor 668a may be present across the gate and source of gain transistor 654a. Capacitor 668a may include parasitic of gain

transistor 654a. Capacitor 668a may also include a bank of switchable capacitors, which may be coupled between the gate and source of gain transistor 654a and may be used to fine-tune the input impedance of CA LNA 640a. Each switchable capacitor may be implemented with a capacitor coupled in series with a switch. Similarly, a variable capacitor 668b may be present across the gate and source of gain transistor 654b. Capacitor 668b may include a bank of switchable capacitors, which may be coupled between the gate and source of gain transistor 654b and may be used to fine-tune the input impedance.

[0063] Input matching circuit 632 is common to both amplifier stages 650a and 650b and is used in both the CA mode and the non-CA mode. In the CA mode, both amplifier stages 650a and 650b are enabled, and gain transistors 654a and 654b operate in a saturation region, as shown in FIG. 6B. In the non-CA mode, one amplifier stage (e.g., amplifier stage 650a) is enabled, and the other amplifier stage (e.g., amplifier stage 650b) is disabled. However, the gain transistor in the disabled amplifier stage (e.g., gain transistor 654b in amplifier stage 650b) is turned On by the input RF signal that is applied to both gain transistors 654a and 654b. Since the cascode transistor in the disabled amplifier stage (e.g., cascode transistor 656b) is turned Off, the gain transistor in the disabled amplifier stage operates in a linear region. Hence, a gain transistor may operate in the saturation region when an amplifier stage is enabled and may operate in the linear region when the amplifier stage is disabled. Operating the gain transistor of the disabled amplifier stage in the linear region may help to reduce changes in the input impedance of CA LNA 640a between the CA mode and the non-CA mode, without a current penalty in the disabled amplifier stage. In particular, the input capacitance,  $C_{IN}$ , of a given gain transistor (e.g., gain transistor 654b) in an enabled amplifier stage and in a disabled amplifier stage may be expressed as:

$$C_{IN} = \frac{2}{3} \cdot W \cdot L \cdot C_{OX} \quad \text{amplifier stage is enabled, and} \quad \text{Eq (1)}$$

$$C_{IN} = \frac{1}{2} \cdot W \cdot L \cdot C_{OX} \quad \text{amplifier stage is disabled,} \quad \text{Eq (2)}$$

where  $W$  is the width and  $L$  is the length of gain transistor 654b, and

$C_{OX}$  is a gate oxide capacitance of gain transistor 654b.

- [0064] As shown in equations (1) and (2), there may be a finite change in the input impedance of a gain transistor depending on whether an amplifier stage is enabled or disabled. However, the input impedance of CA LNA 640a may be maintained within tolerable limits even with the change in the input impedance of the gain transistor.
- [0065] CA LNA 640a splits the carrier-aggregated RF signal at the “gate” level by having the carrier-aggregated RF signal applied to two gain transistors 654a and 654b. The carrier-aggregated RF signal may also be split at the “cascode” level by having the carrier-aggregated RF signal applied to a single gain transistor driving two cascode transistors. Splitting the carrier-aggregated RF signal at the gate level (as shown in FIG. 6A) may provide better performance (e.g., better gain, noise figure, linearity, and isolation) than splitting the carrier-aggregated RF signal at the cascode level. For example, splitting the carrier-aggregated RF signal at the gate level may provide good LO-LO isolation of about 35 dB whereas splitting the carrier-aggregated RF signal at the cascode level may provide LO-LO isolation of only about 15 dB.
- [0066] FIG. 7 shows a schematic diagram of an exemplary design of a CA LNA 640b with inductive degeneration, cascode shutoff, and resistive feedback. CA LNA 640b is another exemplary design of CA LNA 440 in FIG. 4A. CA LNA 640b includes two amplifier stages 650a and 650b coupled to a common input matching circuit 632 and to two load circuits 690a and 690b, similar to CA LNA 640a in FIG. 6A. CA LNA 640b further includes a feedback circuit 660 coupled between the drains of cascode transistors 656a and 656b and the gates of gain transistors 654a and 654b, i.e., between the input and output of amplifier stages 650a and 650b.
- [0067] In the exemplary design shown in FIG. 7, feedback circuit 660 includes switches 662a and 662b, a resistor 664, and a capacitor 666. Resistor 664 and capacitor 666 are coupled in series, with the bottom terminal of capacitor 666 being coupled to the gates of gain transistors 654a and 654b. Switch 662a is coupled between the drain of cascode transistor 656a and the top terminal of resistor 664. Switch 662b is coupled between the drain of cascode transistor 656b and the top terminal of resistor 664. Switches 662a and 662b may each be closed to connect feedback circuit 660 to its associated cascode transistor 656 and may be opened to disconnect feedback circuit 660 from the associated cascode transistor 656. A feedback path from RFout1 to feedback circuit 660 may be formed by closing switch 662a. A feedback path from RFout2 to feedback circuit 660 may be formed by closing switch 662b. Feedback circuit 660 may also

include one or more active circuits such as a transistor. In an exemplary design, feedback circuit 660 may be used/enabled for low-band to provide input power match. For mid-band and high-band, feedback circuit 660 may be disabled, and source degeneration inductors 652a and 652b may be used with matching circuit 632 for input power match. Feedback circuit 660 may also be used in other manners.

[0068] Input matching circuit 632 is common to both amplifier stages 650a and 650b and is used in both the CA mode and the non-CA mode. In the CA mode, input matching for CA LNA 640b may be achieved with feedback circuit 660 around amplifier stages 650a and 650b as well as source degeneration inductors 652a and 652b. In the non-CA mode, input matching for CA LNA 640b may be achieved with feedback circuit 660 and source degeneration inductor 652a and 652b. Feedback circuit 660 may help with input matching for the entire LNA 640b in both the CA mode and the non-CA mode. Input matching for CA LNA 640b may be achieved (i) with feedback circuit 660 and source degeneration inductor 652a for RFout1 and (ii) with feedback circuit 660 and source degenerated inductor 652b for RFout2.

[0069] Amplifier stage 650a may be linearized by (i) both source degeneration inductor 652a and feedback circuit 660 when feedback circuit 660 is selected or (ii) only source degeneration inductor 652a when feedback circuit 660 is not selected. Feedback circuit 660 may improve the linearity of amplifier stage 650a in both the CA mode and the non-CA mode. This may allow a smaller inductor 652a to be used for amplifier stage 650a to obtain the desired linearity. Similarly, amplifier stage 650b may be linearized by (i) both source degeneration inductor 652b and feedback circuit 660 when feedback circuit 660 is selected or (ii) only source degeneration inductor 652b when feedback circuit 660 is not selected. A smaller inductor may be used for inductor 652a and/or 652b to obtain the desired linearity for amplifier stage 650b with feedback circuit 660 enabled.

[0070] **FIG. 8A** shows a schematic diagram of an exemplary design of a CA LNA 840a with a separate input attenuation circuit for each amplifier stage. CA LNA 840a is yet another exemplary design of CA LNA 440 in FIG. 4A. CA LNA 840a includes two amplifier stages 850a and 850b coupled to two input attenuation circuits 860a and 860b and to two load circuits 890a and 890b.

[0071] An input RF signal is provided to the input of CA LNA 840a, which is node X. Amplifier stage 850a is coupled to node X via an NMOS transistor 842a operating as a

switch, attenuation circuits 860a, and an AC coupling capacitor 844a. NMOS transistor 842a has its source coupled to node X, its gate receiving a first control signal,  $Enb1$ , and its drain coupled to the input of attenuation circuit 860a. Attenuation circuit 860a includes (i) a resistor 862a coupled between the input and output of attenuation circuit 860a and (ii) a variable resistor 864a coupled between the output of attenuation circuit 860a and circuit ground. AC coupling capacitor 844a is coupled between the output of attenuation circuit 860a and the input of amplifier stage 850a. Amplifier stage 850b is coupled to node X via an NMOS transistor 842b, an attenuation circuit 860b, and an AC coupling capacitor 844b, which are coupled in similar manner as NMOS transistor 842a, attenuation circuit 860a, and AC coupling capacitor 844a.

[0072] Amplifier stage 850a includes a gain transistor 854a and a cascode transistor 856a. Gain transistor 854a has its gate coupled to AC coupling capacitor 844a and its source coupled to circuit ground (as shown in FIG. 8A) or to a source degeneration inductor (not shown in FIG. 8A). Cascode transistor 856a has its gate receiving a first bias voltage,  $V_{casc1}$ , its source coupled to the drain of gain transistor 854a, and its drain coupled to load circuit 890a. Amplifier stage 850b includes a gain transistor 854b and a cascode transistor 856b, which are coupled in similar manner as gain transistor 854a and cascode transistor 856a. Amplifier stages 850a and 850b may be independently selected via NMOS transistor 842a and 842b, respectively, and independently enabled or disabled via the  $V_{casc1}$  and  $V_{casc2}$  voltages, respectively.

[0073] FIG. 8A shows an exemplary design in which a signal path from the LNA input (node X) to each amplifier stage 850 includes NMOS transistor 842, attenuation circuit 860, and AC coupling capacitor 844. A signal path may also include fewer, different, and/or additional circuits. Furthermore, the signal path for amplifier stage 850a may or may not match the signal path for amplifier stage 850b. For example, NMOS transistor 842a may be omitted whereas NMOS transistor 842b may be retained. Attenuation circuits 860a and 860b for the two signal paths may be identical, or may have the same circuit design but different values, or may have different circuit designs with different circuit topologies.

[0074] NMOS transistor 842a operates as a switch that can pass the input RF signal to amplifier stage 850a when NMOS transistor 842a is enabled by the  $Enb1$  signal. Similarly, NMOS transistor 842b operates as a switch that can pass the input RF signal to amplifier stage 850b in the CA mode when NMOS transistor 842b is enabled by the



Enb2 signal. In one design, NMOS transistors 842a may be enabled in both the CA mode and the non-CA mode, and NMOS transistors 842b may be enabled only in the CA mode. Separate NMOS transistors 842a and 842b and separate attenuation circuits 860a and 860b may be used to allow the input RF signal to encounter only one series switch prior to hitting gain transistor 854a or 854b.

[0075] In the CA mode, both NMOS transistors 842a and 842b are turned On, and the input RF signal is provided to both attenuation circuits 860a and 860b and amplifier stages 850a and 850b. Each amplifier stage 850 amplifies the input RF signal and provides a respective output RF signal to its load circuit 890. In the non-CA mode, one amplifier stage 850a or 850b may be selected. NMOS transistor 842 for the selected amplifier stage 850 is turned On, and the input RF signal is provided to attenuation circuit 860 and the selected amplifier stage 850. NMOS transistor 842 for the unselected amplifier stage 850 is turned Off, and attenuation circuit 860 and the unselected amplifier stage 850 are disconnected from node X, thereby reducing loading on the signal path for the selected amplifier stage 850. The selected amplifier stage 850 amplifies the input RF signal and provides an output RF signal to the associated load circuit 890.

[0076] CA LNA 840a may be advantageously used in a scenario in which the input RF signal includes jammers, which are undesired signals of large amplitude and close in frequency to the desired signals. Input attenuation circuits 860a and 860b may be programmable (e.g., as shown in FIG. 8A) or may be fixed (not shown in FIG. 8A) and may serve a dual purpose of attenuating the jammers in the input RF signal and providing a good input impedance match for CA LNA 840a. Attenuation circuits 860a and 860b may be designed differently and/or may have different settings/values for the CA mode and the non-CA mode in order to obtain a good input impedance match in both modes.

[0077] For simplicity, FIG. 8A shows CA LNA 840a including two amplifier stages 850a and 850b for two sets of carriers. CA LNA 840a may include more than two amplifier stages for more than two sets of carriers.

[0078] **FIG. 8B** shows a schematic diagram of an exemplary design of a CA LNA 840b with a shared input attenuation circuit for both amplifier stages 850a and 850b. CA LNA 840b is yet another exemplary design of CA LNA 440 in FIG. 4A. CA LNA 840b includes two amplifier stages 850a and 850b coupled to a shared input attenuation

circuit 860a and to two load circuits 890a and 890b. Sharing input attenuation circuit 860a between amplifier stages 850a and 850b may reduce circuit area and may also provide other advantages.

[0079] CA LNA 840b includes all of the circuit components in CA LNA 840a in FIG. 8A except for input attenuation circuit 860b and AC coupling capacitor 844b. All of the circuit components within CA LNA 840b are coupled as described above for CA LNA 840a in FIG. 8A except for NMOS transistor 842b. NMOS transistor 842b has its source coupled to the input of amplifier stage 850a, its gate receiving an Enb2 control signal, and its drain coupled to the input of amplifier stage 850b. Amplifier stages 850a and 850b may be independently selected via NMOS transistor 842a and 842b, respectively, and may be independently enabled or disabled via the Vcasc1 and Vcasc2 voltages, respectively.

[0080] In the exemplary design shown in FIG. 8B, amplifier stages 850a and 850b share a common input switch implemented with NMOS transistor 842a and a common input attenuation circuit 860a. Input attenuation circuit 860a may be programmable (e.g., as shown in FIG. 8B) or may be fixed (not shown in FIG. 8B) and may serve a dual purpose of attenuating incoming jammers in the input RF signal and providing a good input impedance match for CA LNA 840b. Attenuation circuit 860a may have different settings for the CA mode and the non-CA mode in order to obtain a good input impedance match in both modes.

[0081] In the CA mode, both NMOS transistors 842a and 842b are turned On, and the input RF signal is provided via attenuation circuit 860a to both amplifier stages 850a and 850b. The input RF signal passes through a single series switch prior to hitting gain transistor 854a. The input RF signal passes through two series switches prior to hitting gain transistor 854b, which may result in a small degradation in performance of amplifier stage 850b. In the non-CA mode, NMOS transistor 842a is turned On, and the input RF signal is provided to attenuation circuit 860a and amplifier stage 850a. NMOS transistor 842b is turned Off, and amplifier stage 850b is disconnected from node Y, thereby reducing capacitive loading on the signal path for amplifier stage 850a. The input RF signal passes through a single series switch implemented with NMOS transistor 842a prior to hitting gain transistor 854a in the non-CA mode.

[0082] FIG. 9 shows a schematic diagram of an exemplary design of a CA LNA 940 with a tunable matching circuit. CA LNA 940 is another exemplary design of CA LNA

440 in FIG. 4A. CA LNA 940 includes two amplifier stages 950a and 950b coupled to a shared tunable matching circuit 932 and to two load circuits 990a and 990b. Amplifier stage 950a includes a source degeneration inductor 952a, a gain transistor 954a, and a cascode transistor 956a, which are coupled in similar manner as inductor 652a, gain transistor 654a, and cascode transistor 656a in FIG. 6A. Amplifier stage 950b includes a source degeneration inductor 952b, a gain transistor 954b, and a cascode transistor 956b, which are also coupled in similar manner as inductor 652a, gain transistor 654a, and cascode transistor 656a in FIG. 6A. Cascode transistor 956a has its gate receiving a first control voltage,  $V_{casc1}$ . Cascode transistor 956b has its gate receiving a second control voltage,  $V_{casc2}$ . Each amplifier stage 950 may be independently enabled or disabled based on its  $V_{casc}$  control voltage. Amplifier stages 950a and 950b may be independently enabled or disabled via the  $V_{casc1}$  and  $V_{casc2}$  voltages, respectively.

[0083] Matching circuit 932 receives an input RF signal and performs input matching for CA LNA 940. An AC coupling capacitor 944a has one end coupled to the output of matching circuit 932 and the other end coupled to the gate of gain transistor 954a. An AC coupling capacitor 944b has one end coupled to the output of matching circuit 932 and the other end coupled to the gate of gain transistor 954b.

[0084] CA LNA 940 supports the CA mode and the non-CA mode. In the CA mode, both amplifier stages 950a and 950b are enabled with the  $V_{casc1}$  and  $V_{casc2}$  voltages applied to cascode transistors 956a and 956b, respectively. In the non-CA mode, only one of the two amplifier stages 950a and 950b is enabled, depending on the particular load circuit to which the input RF signal is to be routed. Matching circuit 932 may be adjusted based on the number of enabled amplifier stages and/or which amplifier stage(s) are enabled in order to obtain good noise/power match in both the CA modes and the non-CA mode.

[0085] MIMO LNA 540 in FIG. 5A may be implemented with various circuit architectures. Some exemplary designs of MIMO LNA 540 are described below. MIMO LNA 540 may also be implemented with transistors of various types. Some exemplary designs of MIMO LNA 540 using NMOS transistors are described below.

[0086] FIG. 10 shows a schematic diagram of an exemplary design of a 2×2 MIMO LNA 1040 based on a cascode shutoff architecture. MIMO LNA 1040 is an exemplary design of MIMO LNA 540 in FIG. 5A and includes (i) two LNA inputs receiving two

input RF signals, RFin1 and RFin2, and (ii) two LNA outputs providing two output RF signals, RFout1 and RFout2.

[0087] MIMO LNA 1040 includes four amplifier stages 1050a to 1050d coupled to two load circuits 1090a and 1090b. Each amplifier stage 1050a includes a source degeneration inductor 1052, a gain transistor 1054, and a cascode transistor 1056, which are coupled in similar manner as inductor 652a, gain transistor 654a, and cascode transistor 656a in FIG. 6A. Gain transistors 1054a and 1054b within amplifier stages 1050a and 1050b have their gates receiving the first input RF signal. Gain transistors 1054c and 1054d within amplifier stages 1050c and 1050d have their gates receiving the second input RF signal. Cascode transistors 1056a and 1056c within amplifier stages 1050a and 1050c have their drains coupled to load circuit 1090a and providing the first output RF signal. Cascode transistors 1056b and 1056d within amplifier stages 1050b and 1050d have their drains coupled to load circuit 1090b and providing the second output RF signal.

[0088] Amplifier stages 1050a and 1050b may be designed to provide good performance for a first set of one or more bands, e.g., as described above for CA LNA 640a in FIG. 6A. Similarly, amplifier stages 1050c and 1050d may be designed to provide good performance for a second set of one or more bands.

[0089] MIMO LNA 1040 may operate in a  $1 \times 2$  configuration for intra-band CA. In the  $1 \times 2$  configuration, an input RF signal, RFin1 or RFin2, may be provided via one LNA input to two gain transistors 1054 in two amplifier stages 1050. The input RF signal is amplified by the two gain transistors, buffered by the two cascode transistors coupled to the two gain transistors, and provided to load circuits 1090a and 1090b. MIMO LNA 1040 can support intra-band CA with the input RF signal provided to either of the two LNA inputs.

[0090] MIMO LNA 1040 may operate in a  $2 \times 2$  configuration for inter-band CA. In the  $2 \times 2$  configuration, a first input RF signal may be amplified by a first selected gain transistor 1054 in one amplifier stage 1050, buffered by cascode transistor 1056 coupled to the first selected gain transistor 1054, and provided to load circuit 1090a. A second input RF signal may be amplified by a second selected gain transistor 1054 in another amplifier stage 1050, buffered by cascode transistor 1056 coupled to the second selected gain transistor 1054, and provided to load circuit 1090b.

- [0091] **FIG. 11A** shows a schematic diagram of an exemplary design of a  $2 \times 2$  MIMO LNA 1140a based on the cascode shutoff architecture. MIMO LNA 1140a is another exemplary design of MIMO LNA 540 in FIG. 5A and includes (i) two LNA inputs receiving two input RF signals, RFin1 and RFin2, and (ii) two LNA outputs providing two output RF signals, RFout1 and RFout2.
- [0092] MIMO LNA 1140a includes two amplifier stages 1150a and 1150b coupled to two load circuits 1190a and 1190b, respectively. Amplifier stage 1150a includes a source degeneration inductor 1152a, a gain transistor 1154a, and a cascode transistor 1156a, which are coupled in similar manner as inductor 652a, gain transistor 654a, and cascode transistor 656a in FIG. 6A. Gain transistor 1154a has its gate receiving the first input RF signal. Cascode transistor 1156a has its gate receiving a Vcascl1a voltage and its drain coupled to load circuit 1190a. Amplifier stage 1150a further includes a gain transistor 1164a and a cascode transistor 1166a. Gain transistor 1164a has its source coupled to inductor 1152a and its gate receiving the second input RF signal. Cascode transistor 1166a has its gate receiving a Vcascl2a voltage and its drain coupled to load circuit 1190a.
- [0093] Amplifier stage 1150b includes a source degeneration inductor 1152b, two gain transistors 1154b and 1164b, and two cascode transistors 1156b and 1166b, which are coupled in similar manner as inductor 1152a, gain transistors 1154a and 1164a, and cascode transistors 1156a and 1166a in amplifier stage 1150a. Gain transistors 1154b and 1164b have their gates receiving the first and second input RF signals, respectively. Cascode transistors 1156b and 1166b have their gates receiving Vcascl1b and Vcascl2b voltages, respectively, and their drains coupled to load circuit 1190b.
- [0094] MIMO LNA 1140a may operate in a  $1 \times 2$  configuration for intra-band CA. In the  $1 \times 2$  configuration, an input RF signal, RFin1 or RFin2, may be provided via one LNA input to two gain transistors 1154a and 1154b (or to gain transistors 1164a and 1164b) in the two amplifier stages 1150a and 1150b. The input RF signal is amplified by the two gain transistors, buffered by the two cascode transistors coupled to the two gain transistors, and provided to load circuits 1190a and 1190b. MIMO LNA 1140a can support intra-band CA with the input RF signal applied to either of the two LNA inputs.
- [0095] MIMO LNA 1140a may operate in a  $2 \times 2$  configuration for inter-band CA. In the  $2 \times 2$  configuration, a first input RF signal (e.g., RFin1) may be received by amplifier

stage 1150a or 1150b and may be amplified by gain transistor 1154a or 1154b, buffered by cascode transistor 1156a or 1156b, and provided to load circuit 1190a or 1190b. A second input RF signal (e.g., RFin2) may be received by amplifier stage 1150a or 1150b, amplified by gain transistor 1164a or 1164b, buffered by cascode transistor 1166a or 1166b, and provided to load circuit 1190a or 1190b. Each amplifier stage 1150 would receive only one of the two input RF signals and would provide its output RF signal to load circuit 1190 coupled to that amplifier stage 1150.

[0096] **FIG. 11B** shows a schematic diagram of an exemplary design of a 4×2 MIMO LNA 1140b based on the cascode shutoff architecture. MIMO LNA 1140b is yet another exemplary design of MIMO LNA 540 in FIG. 5A and includes (i) four LNA inputs receiving four input RF signals, RFin1 to RFin4, and (ii) two LNA outputs providing two output RF signals, RFout1 and RFout2. MIMO LNA 1140b includes four amplifier stages 1150a to 1150d coupled to two load circuits 1190a and 1190b. Amplifier stages 1150a and 1150b include source degeneration inductors, gain transistors, and cascode transistors that are coupled as described above for FIG. 11A.

[0097] Amplifier stage 1150c includes a source degeneration inductor 1152c, two gain transistors 1154c and 1164c, and two cascode transistors 1156c and 1166c, which are coupled in similar manner as inductor 1152a, gain transistors 1154a and 1164a, and cascode transistors 1156a and 1166a in amplifier stage 1150a. Gain transistors 1154c and 1164c have their gates receiving the third and fourth input RF signals, respectively. Cascode transistors 1156c and 1166c have their gates receiving Vcasc3a and Vcasc4a voltages, respectively, and their drains coupled to load circuit 1190a.

[0098] Amplifier stage 1150d includes a source degeneration inductor 1152d, two gain transistors 1154d and 1164d, and two cascode transistors 1156d and 1166d, which are coupled in similar manner as inductor 1152a, gain transistors 1154a and 1164a, and cascode transistors 1156a and 1166a in amplifier stage 1150a. Gain transistors 1154d and 1164d have their gates receiving the third and fourth input RF signals, respectively. Cascode transistors 1156d and 1166d have their gates receiving Vcasc3b and Vcasc4b voltages, respectively, and their drains coupled to load circuit 1190b.

[0099] MIMO LNA 1140b may operate in a 1×2 configuration for intra-band CA. In the 1×2 configuration, an input RF signal (RFin1, RFin 2, RFin3 or RFin4) may be provided via one LNA input to two gain transistors in two amplifier stages 1150. The input RF signal is amplified by the two gain transistors, buffered by the two cascode

transistors coupled to the two gain transistors, and provided to load circuits 1190a and 1190b. MIMO LNA 1140b can support intra-band CA with the input RF signal applied to any one of the four LNA inputs.

[00100] MIMO LNA 1140b may operate in a 2-input 2-output (2×2) configuration for inter-band CA. In the 2×2 configuration, a first input RF signal (e.g., RFin1 or RFin2) may be received by amplifier stage 1150a or 1150b, amplified by a first selected gain transistor in one amplifier stage 1150a or 1150b, buffered by the cascode transistor coupled to the first selected gain transistor, and provided to load circuit 1190a or 1190b. A second input RF signal (e.g., RFin3 or RFin4) may be received by amplifier stage 1150c or 1150d, amplified by a second selected gain transistor in amplifier stage 1150c or 1150d, buffered by the cascode transistor coupled to the second selected gain transistor, and provided to load circuit 1190a or 1190b. Only two amplifier stages 1150 are enabled to amplify the two input RF signals. Each enabled amplifier stage 1150 would receive only one of the two input RF signals and would provide its output RF signal to load circuit 1190 coupled to that amplifier stage 1150.

[00101] FIG. 11C shows a schematic diagram of another view of 4×2 MIMO LNA 1140b in FIG. 11B. MIMO LNA 1140b in FIG. 11C include all of the degeneration inductors, gain transistors, and cascode transistors shown in FIG. 11B, which are arranged differently in FIG. 11C. FIG. 11C shows that MIMO LNA 1140b can receive a single input RF signal provided to any LNA input (e.g., RFin1, RFin2, RFin3, or RFin4) and can provide two output RF signals to two load circuits 1190a and 1190b for intra-band CA. FIG. 11C also shows that MIMO LNA 1140b can receive two input RF signals provided to two LNA inputs (e.g., RFin1 and RFin3, or RFin1 and RFin4, or RFin2 and RFin3, or RFin2 and RFin4) and can provide two output RF signals to two load circuits 1190a and 1190b for inter-band CA. If a separate source degeneration inductor is used for each gain transistor (for a total of eight source degeneration inductors), then two input RF signals may be applied to any two LNA inputs.

[00102] FIGS. 10 and 11A show two exemplary designs of a 2×2 MIMO LNA. FIG. 11B shows an exemplary design of a 4×2 MIMO LNA. A MIMO LNA may also be implemented in other manners. For example, a MIMO LNA may include one or more feedback circuits, with each feedback circuit being coupled between the input and output of one or more amplifier stages, e.g., as shown in FIG. 7.

- [00103] In general, a MIMO LNA with any number of inputs and any number of outputs may be implemented based on the cascode shutoff architecture. More LNA inputs for more bands may be supported with more amplifier stages and/or more gain and cascode transistors in each amplifier stage. More LNA outputs for more sets of carriers may also be supported with more amplifier stages and/or more gain and cascode transistors in each amplifier stage.
- [00104] A matching circuit and a tunable matching circuit may be implemented in various manners. Some exemplary designs of a tunable matching circuit are described below.
- [00105] **FIG. 12A** shows an exemplary design of a tunable matching circuit 1210 based on an L topology. The L topology includes a series circuit component coupled to a shunt circuit component. A series circuit component is a circuit component connected between two nodes. A shunt circuit component is a circuit component connected between a node and circuit ground. A circuit component may be an inductor, a capacitor, a resistor, etc. Matching circuit 1210 includes (i) a series inductor 1212 coupled between the input and output of matching circuit 1210 and (ii) a tunable shunt capacitor 1214 coupled between the output of matching circuit 1210 and circuit ground.
- [00106] **FIG. 12B** shows an exemplary design of a tunable matching circuit 1220 based on the L topology. Matching circuit 1220 includes (i) a tunable series capacitor 1222 coupled between the input and output of matching circuit 1220 and (ii) a shunt inductor 1224 coupled between the output of matching circuit 1220 and circuit ground.
- [00107] **FIG. 12C** shows an exemplary design of a tunable matching circuit 1230 based on an R topology. The R topology includes a shunt circuit component coupled to a series circuit component. Matching circuit 1230 includes (i) a tunable shunt capacitor 1232 coupled between the input of matching circuit 1230 and circuit ground and (ii) a series inductor 1234 coupled between the input and output of matching circuit 1230.
- [00108] **FIG. 12D** shows an exemplary design of a tunable matching circuit 1240 based on a Pi topology. The Pi topology includes a shunt circuit component coupled to a series circuit component, which is coupled to another shunt circuit component. Matching circuit 1240 includes (i) a shunt capacitor 1242 coupled between the input of matching circuit 1240 and circuit ground, (ii) a series inductor 1244 coupled between the input and output of matching circuit 1240, and (iii) a tunable shunt capacitor 1246 coupled between the output of matching circuit 1240 and circuit ground.



- [00109] **FIG. 12E** shows an exemplary design of a tunable matching circuit 1250 with two R sections. Matching circuit 1250 includes (i) a shunt inductor 1252 coupled between the input of matching circuit 1250 and a power supply, Vdd, (ii) a series capacitor 1254 coupled between the input of matching circuit 1250 and node E, (iii) a tunable shunt capacitor 1256 coupled between node E and circuit ground, and (iv) a series inductor 1258 coupled between node E and the output of matching circuit 1250.
- [00110] **FIG. 12F** shows an exemplary design of a tunable matching circuit 1260 based on the Pi topology. Matching circuit 1260 includes (i) a shunt inductor 1262 coupled between the input of matching circuit 1260 and the Vdd supply, (ii) a series capacitor 1264 coupled between the input and output of matching circuit 1260, (iii) a tunable shunt capacitor 1266 coupled between the output of matching circuit 1260 and circuit ground, and (iv) a shunt inductor 1268 coupled between the output of matching circuit 1260 and circuit ground.
- [00111] A fixed matching circuit may also be implemented based on any of the exemplary designs shown in FIGS. 12A to 12F. In this case, each adjustable circuit component (e.g., each adjustable capacitor) may be replaced with a fixed circuit component (e.g., a fixed capacitor).
- [00112] In an exemplary design, an apparatus (e.g., a wireless device, an IC, a circuit module, etc.) may include first and second amplifier stages (e.g., for a CA LNA or a MIMO LNA). The first amplifier stage (e.g., amplifier stage 650a in FIG. 6A) may receive and amplify an input RF signal and provide a first output RF signal to a first load circuit (e.g., load circuit 690a) when the first amplifier stage is enabled. The input RF signal may comprise transmissions sent on multiple carriers at different frequencies to a wireless device. The second amplifier stage (e.g., amplifier stage 650b in FIG. 6A) may receive and amplify the input RF signal and provide a second output RF signal to a second load circuit (e.g., load circuit 690b) when the second amplifier stage is enabled. Each load circuit may comprise at least one mixer (e.g., as shown in FIG. 4B or 5B) and/or other circuits. The first output RF signal may be processed (e.g., downconverted) for transmissions on a first set of at least one carrier. The second output RF signal may be processed for transmissions on a second set of at least one carrier.
- [00113] In an exemplary design, the first amplifier stage may comprise a first gain transistor (e.g., gain transistor 654a in FIG. 6A) coupled to a first cascode transistor

(e.g., cascode transistor 656a). The second amplifier stage may comprise a second gain transistor (e.g., gain transistor 654b) coupled to a second cascode transistor (e.g., cascode transistor 656b). The input RF signal may be provided to both the first and second gain transistors. In an exemplary design, the first amplifier stage may further comprise a first inductor (e.g., inductor 652a) coupled to the first gain transistor. The second amplifier stage may further comprise a second inductor (e.g., inductor 652b) coupled to the second gain transistor. In another exemplary design, the first and second gain transistors may have their sources coupled to circuit ground (e.g., as shown in FIGS. 8A and 8B).

**[00114]** In an exemplary design, the first and second amplifier stages may (i) provide the first and second output RF signals in a first/CA mode and (ii) provide the first output RF signal but not the second output RF signal in a second/non-CA mode. The first and second cascode transistors may both be enabled in the first/CA mode. Only one of the first and second cascode transistors may be enabled in the second/non-CA mode. The first and second gain transistors may be applied the input RF signal in both the first/CA mode and the second/non-CA mode. One of the first and second gain transistors may operate in a saturation region and the other one of the first and second gain transistors may operate in a linear region in the second/non-CA mode. Each amplifier stage may be enabled or disabled by providing one or more appropriate voltages to one or more cascode transistors in the amplifier stage.

**[00115]** In an exemplary design, a feedback circuit (e.g., feedback circuit 660 in FIG. 7) may be coupled between an output and an input of at least one of the first and second amplifier stages. The feedback circuit may comprise a resistor, or a capacitor, or an active circuit such as a transistor, or some other circuit, or any combination thereof.

**[00116]** In an exemplary design, separate attenuation circuits may be used for the amplifier stages, e.g., as shown in FIG. 8A. A first attenuation circuit (e.g., attenuation circuit 860a in FIG. 8A) may be coupled to the first amplifier stage and may receive the input RF signal and provide a first attenuated input RF signal to the first amplifier stage. A second attenuation circuit (e.g., attenuation circuit 860b in FIG. 8A) may be coupled to the second amplifier stage and may receive the input RF signal and provide a second attenuated input RF signal to the first amplifier stage.

**[00117]** In another exemplary design, a shared/common attenuation circuit may be used for all amplifier stages, e.g., as shown in FIG. 8B. The share attenuation circuit (e.g.,

attenuation circuit 860a in FIG. 8B) may be coupled to the first and second amplifier stages and may receive the input RF signal and provide an attenuated input RF signal to both amplifier stages.

**[00118]** In an exemplary design, an input matching circuit may be used for the amplifier stages. The input matching circuit (e.g., input matching circuit 632 in FIG. 6A) may be coupled to the first and second amplifier stages and may receive a receiver input signal and provide the input RF signal. The input matching circuit may be fixed (e.g., as shown in FIG. 6A) and may comprise one or more fixed circuit components. Alternatively, the input matching circuit may be tunable (e.g., as shown in FIG. 9) and may comprise at least one adjustable circuit component.

**[00119]** In an exemplary design, the apparatus may further component third and fourth amplifier stages (e.g., amplifier stages 1050c and 1050d in FIG. 10 for a MIMO LNA). The third amplifier stage (e.g., amplifier stage 1050c) may receive and amplify a second input RF signal and provide the first output RF signal to the first load circuit when the third amplifier stage is enabled. The fourth amplifier stage (e.g., amplifier stage 1050d) may receive and amplify the second input RF signal and provide the second output RF signal to the second load circuit when the fourth amplifier stage is enabled.

**[00120]** In another exemplary design, the first amplifier stage (e.g., amplifier stage 1150a in FIG. 11A) may receive and amplify the input RF signal or a second input RF signal and may provide the first output RF signal to the first load circuit when the first amplifier stage is enabled. The second amplifier stage (e.g., amplifier stage 1150b) may receive and amplify the input RF signal or the second input RF signal and may provide the second output RF signal to the second load circuit when the second amplifier stage is enabled. The first amplifier stage may further comprise a third gain transistor (e.g., gain transistor 1164a) coupled to a third cascode transistor (e.g., cascode transistor 1166a). The second amplifier stage may further comprise a fourth gain transistor (e.g., gain transistor 1164b) coupled to a fourth cascode transistor (e.g., cascode transistor 1166b). The second input RF signal may be provided to both the third and fourth gain transistors.

**[00121]** In another exemplary design, the apparatus may further include third and fourth amplifier stages (e.g., amplifier stages 1150c and 1150d in FIG. 11B for a MIMO LNA). The third amplifier stage (e.g., amplifier stage 1150c) may receive and amplify a third input RF signal or a fourth input RF signal and may provide the first output RF

signal to the first load circuit when the third amplifier stage is enabled. The fourth amplifier stage (e.g., amplifier stage 1150d) may receive and amplify the third input RF signal or the fourth input RF signal and may provide the second output RF signal to the second load circuit when the fourth amplifier stage is enabled.

**[00122]** FIG. 13 shows an exemplary design of a process 1300 for receiving signals in a wireless system. Process 1300 may be performed by a wireless device (as described below) or by some other entity. The wireless device may enable first and second amplifier stages in a first/CA mode (block 1312). The wireless device may enable the first amplifier stage and disable the second amplifier stage in a second/non-CA mode (block 1314). The wireless device may amplify a first input RF signal with the first amplifier stage to obtain a first output RF signal when the first amplifier stage is enabled (block 1316). The wireless device may amplify the first input RF signal or a second input RF signal with the second amplifier stage to obtain a second output RF signal when the second amplifier stage is enabled (block 1318). The first and second input RF signals may comprise transmissions sent on multiple carriers at different frequencies to the wireless device. The first and second input RF signals may be for different bands.

**[00123]** The LNAs described herein may be implemented on an IC, an analog IC, an RFIC, a mixed-signal IC, an ASIC, a printed circuit board (PCB), an electronic device, etc. The LNAs may also be fabricated with various IC process technologies such as complementary metal oxide semiconductor (CMOS), N-channel MOS (NMOS), P-channel MOS (PMOS), bipolar junction transistor (BJT), bipolar-CMOS (BiCMOS), silicon germanium (SiGe), gallium arsenide (GaAs), heterojunction bipolar transistors (HBTs), high electron mobility transistors (HEMTs), silicon-on-insulator (SOI), etc.

**[00124]** An apparatus implementing the LNAs described herein may be a stand-alone device or may be part of a larger device. A device may be (i) a stand-alone IC, (ii) a set of one or more ICs that may include memory ICs for storing data and/or instructions, (iii) an RFIC such as an RF receiver (RFR) or an RF transmitter/receiver (RTR), (iv) an ASIC such as a mobile station modem (MSM), (v) a module that may be embedded within other devices, (vi) a receiver, cellular phone, wireless device, handset, or mobile unit, (vii) etc.

**[00125]** In one or more exemplary designs, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in

software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A storage media may be any available media that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store desired program code in the form of instructions or data structures and that can be accessed by a computer. Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and blu-ray disc where *disks* usually reproduce data magnetically, while *discs* reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[00126] The previous description of the disclosure is provided to enable any person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations without departing from the scope of the disclosure. Thus, the disclosure is not intended to be limited to the examples and designs described herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

[00127] **WHAT IS CLAIMED IS:**

**CLAIMS**

1. An apparatus comprising:  
a first amplifier stage configured to receive and amplify an input radio frequency (RF) signal and provide a first output RF signal to a first load circuit when the first amplifier stage is enabled, the input RF signal comprising transmissions sent on multiple carriers at different frequencies to a wireless device; and  
a second amplifier stage configured to receive and amplify the input RF signal and provide a second output RF signal to a second load circuit when the second amplifier stage is enabled.
2. The apparatus of claim 1, the first amplifier stage comprising a first gain transistor coupled to a first cascode transistor, the second amplifier stage comprising a second gain transistor coupled to a second cascode transistor, and the input RF signal being provided to both the first and second gain transistors.
3. The apparatus of claim 2, the first amplifier stage further comprising a first inductor coupled to the first gain transistor, and the second amplifier stage further comprising a second inductor coupled to the second gain transistor.
4. The apparatus of claim 2, the first and second gain transistors having sources coupled to circuit ground.
5. The apparatus of claim 2, the first and second amplifier stages providing the first and second output RF signals in a first mode and providing the first output RF signal but not the second output RF signal in a second mode, the first and second cascode transistors being enabled in the first mode, and only one of the first and second cascode transistors being enabled in the second mode.
6. The apparatus of claim 5, the first and second gain transistors being applied the input RF signal in both the first mode and the second mode, and one of the first and second gain transistors operating in a saturation region and the other one of the first and second gain transistors operating in a linear region in the second mode.

7. The apparatus of claim 1, further comprising:  
a feedback circuit coupled between an output and an input of at least one of the first and second amplifier stages.

8. The apparatus of claim 7, the feedback circuit comprising a resistor, or a capacitor, or both a resistor and a capacitor.

9. The apparatus of claim 1, further comprising:  
a first attenuation circuit coupled to the first amplifier stage and configured to receive the input RF signal; and  
a second attenuation circuit coupled to the second amplifier stage and configured to receive the input RF signal.

10. The apparatus of claim 1, further comprising:  
an attenuation circuit coupled to the first and second amplifier stages and configured to receive the input RF signal.

11. The apparatus of claim 1, further comprising:  
an input matching circuit coupled to the first and second amplifier stages and configured to receive a receiver input signal and provide the input RF signal.

12. The apparatus of claim 11, the input matching circuit being tunable and comprising at least one adjustable circuit component.

13. The apparatus of claim 1, further comprising:  
a third amplifier stage configured to receive and amplify a second input RF signal and provide the first output RF signal to the first load circuit when the third amplifier stage is enabled; and  
a fourth amplifier stage configured to receive and amplify the second input RF signal and provide the second output RF signal to the second load circuit when the fourth amplifier stage is enabled.

14. The apparatus of claim 1,  
the first amplifier stage configured to receive and amplify the input RF signal or a second input RF signal and provide the first output RF signal to the first load circuit when the first amplifier stage is enabled, and  
the second amplifier stage configured to receive and amplify the input RF signal or the second input RF signal and provide the second output RF signal to the second load circuit when the second amplifier stage is enabled.

15. The apparatus of claim 2, the first amplifier stage further comprising a third gain transistor coupled to a third cascode transistor, the second amplifier stage further comprising a fourth gain transistor coupled to a fourth cascode transistor, and a second input RF signal being provided to both the third and fourth gain transistors.

16. The apparatus of claim 14, further comprising:  
a third amplifier stage configured to receive and amplify a third input RF signal or a fourth input RF signal and provide the first output RF signal to the first load circuit when the third amplifier stage is enabled; and  
a fourth amplifier stage configured to receive and amplify the third input RF signal or the fourth input RF signal and provide the second output RF signal to the second load circuit when the fourth amplifier stage is enabled.

17. A method comprising:  
amplifying a first input radio frequency (RF) signal with a first amplifier stage to obtain a first output RF signal when the first amplifier stage is enabled, the first input RF signal comprising transmissions sent on multiple carriers at different frequencies to a wireless device; and  
amplifying the first input RF signal or a second input RF signal with a second amplifier stage to obtain a second output RF signal when the second amplifier stage is enabled.

18. The method of claim 17, further comprising:  
enabling the first and second amplifier stages in a first mode to obtain the first and second output RF signals; and



enabling the first amplifier stage and disabling the second amplifier stage in a second mode to obtain the first output RF signal but not the second output RF signal.

19. An apparatus comprising:

first means for amplifying configured to amplify a first input radio frequency (RF) signal and provide a first output RF signal when the first means for amplifying is enabled, the first input RF signal comprising transmissions sent on multiple carriers at different frequencies to a wireless device; and

second means for amplifying configured to amplify the first input RF signal or a second input RF signal and provide a second output RF signal when the second means for amplifying is enabled.

20. The apparatus of claim 19, further comprising:

means for enabling the first and second means for amplifying in a first mode to obtain the first and second output RF signals; and

means for enabling the first means for amplifying and disabling the second means for amplifying in a second mode to obtain the first output RF signal but not the second output RF signal.

### **ABSTRACT**

Low noise amplifiers (LNAs) supporting carrier aggregation are disclosed. In an exemplary design, an apparatus includes first and second amplifier stages, e.g., for a carrier aggregation (CA) LNA or a multiple-input multiple-output (MIMO) LNA. The first amplifier stage receives and amplifies an input radio frequency (RF) signal and provides a first output RF signal to a first load circuit when the first amplifier stage is enabled. The input RF signal includes transmissions sent on multiple carriers at different frequencies to a wireless device. The second amplifier stage receives and amplifies the input RF signal and provides a second output RF signal to a second load circuit when the second amplifier stage is enabled. Each amplifier stage may include a gain transistor coupled to a cascode transistor.

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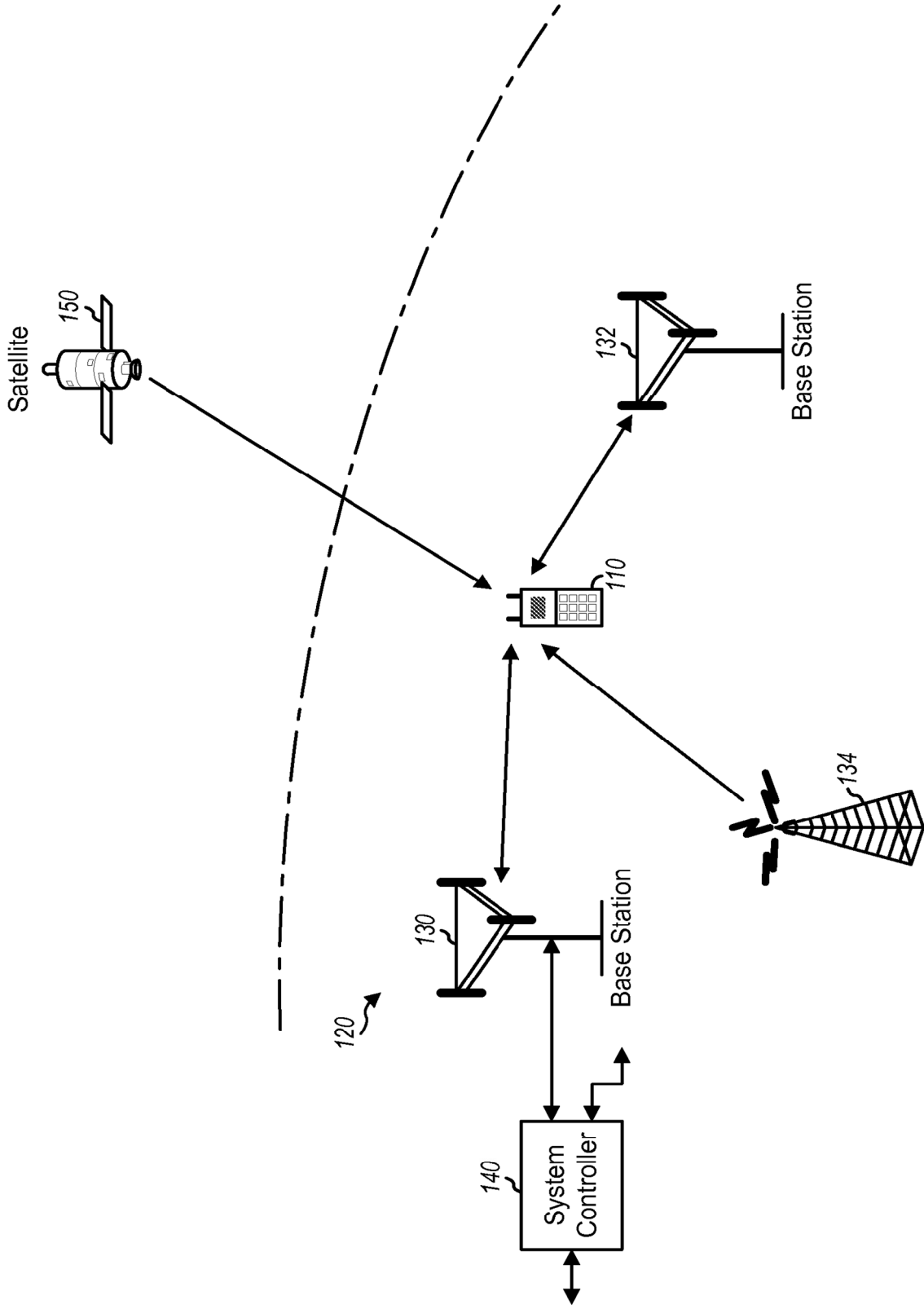
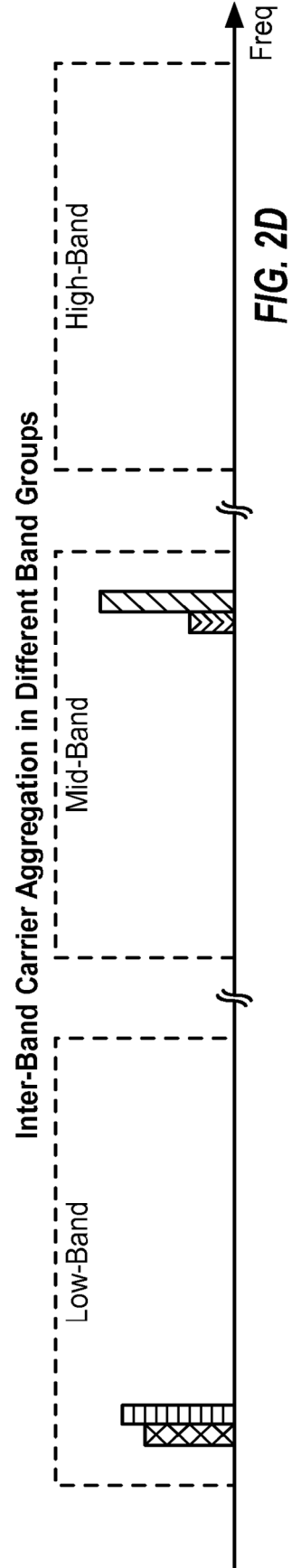
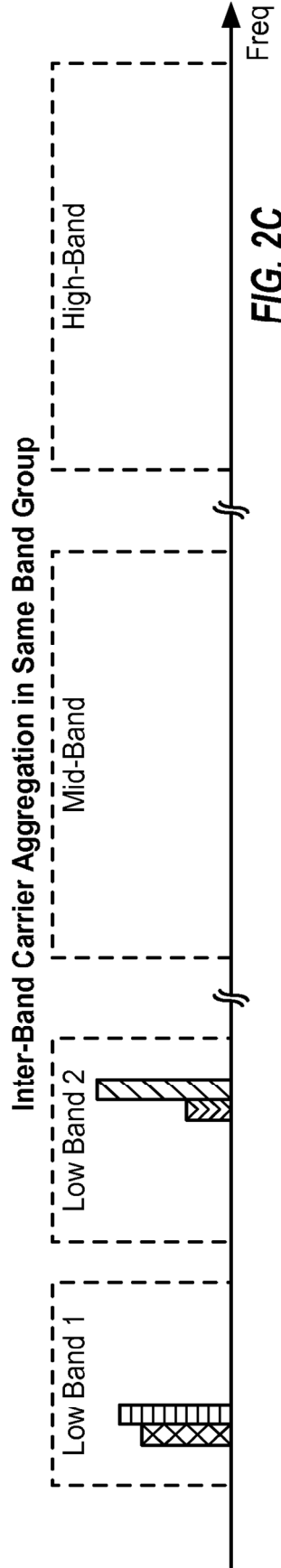
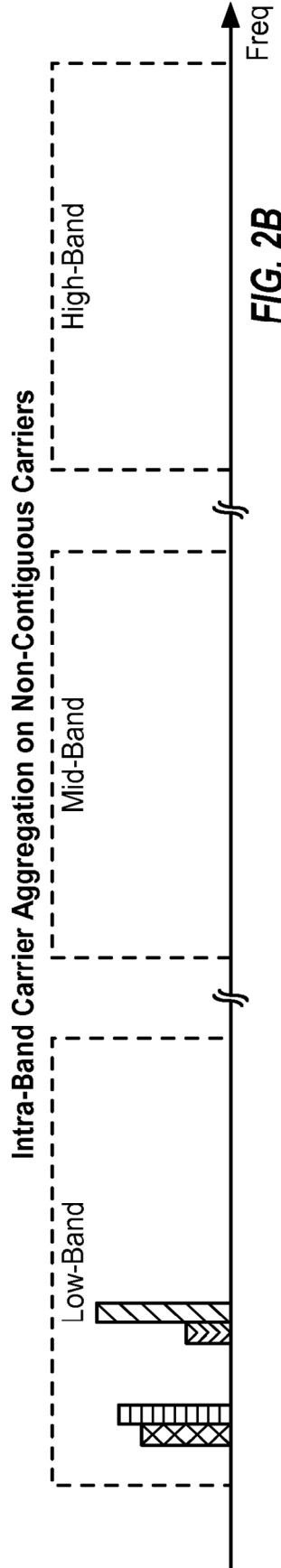
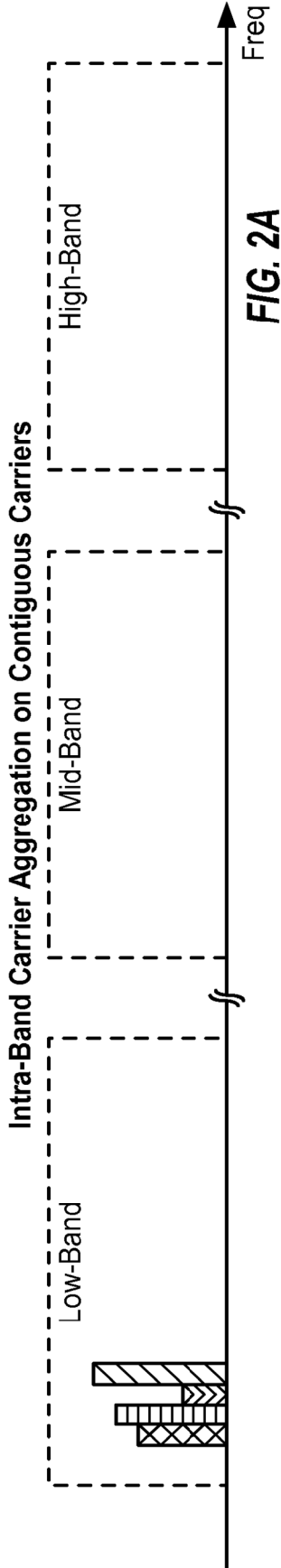


FIG. 1

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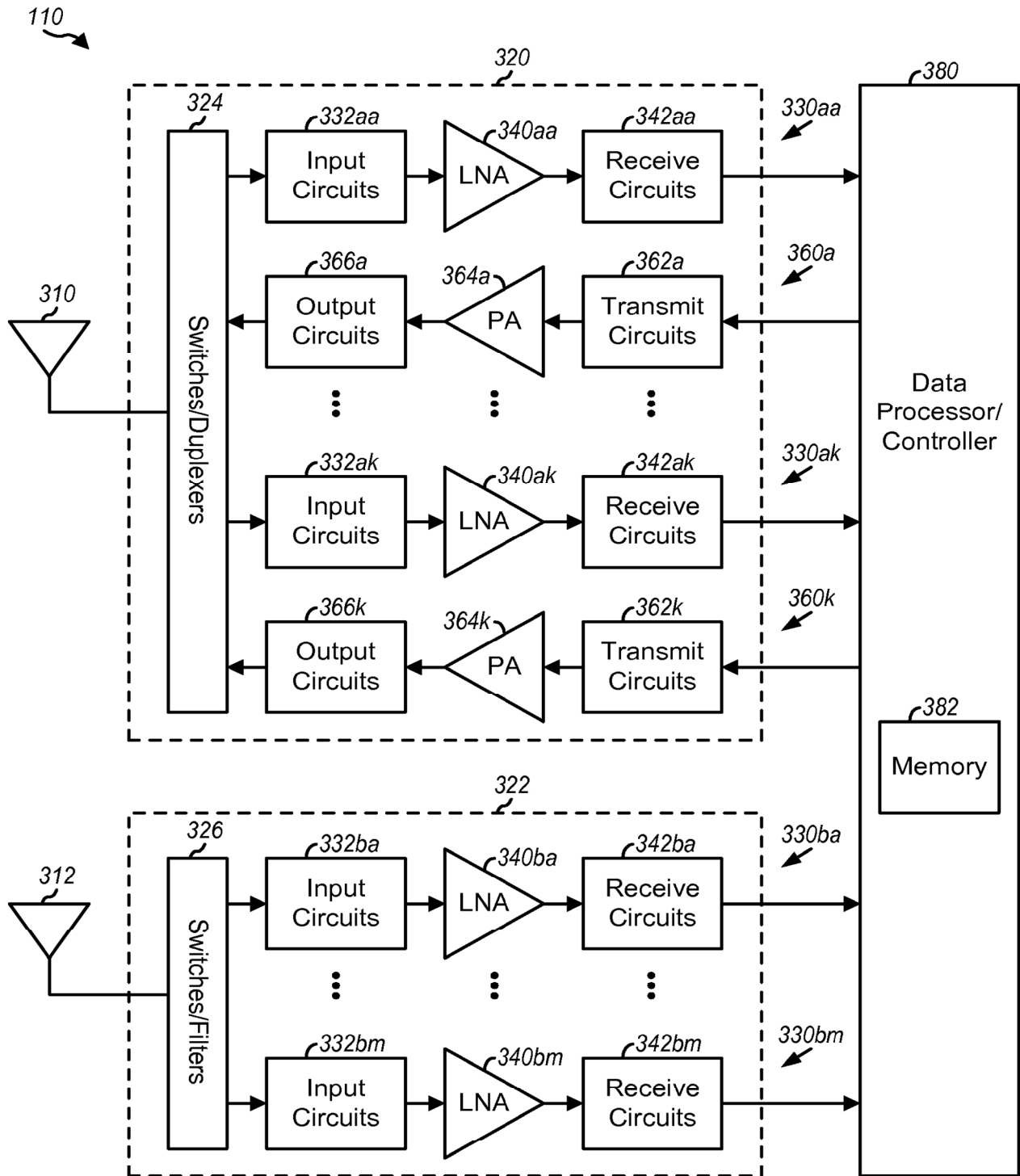


FIG. 3

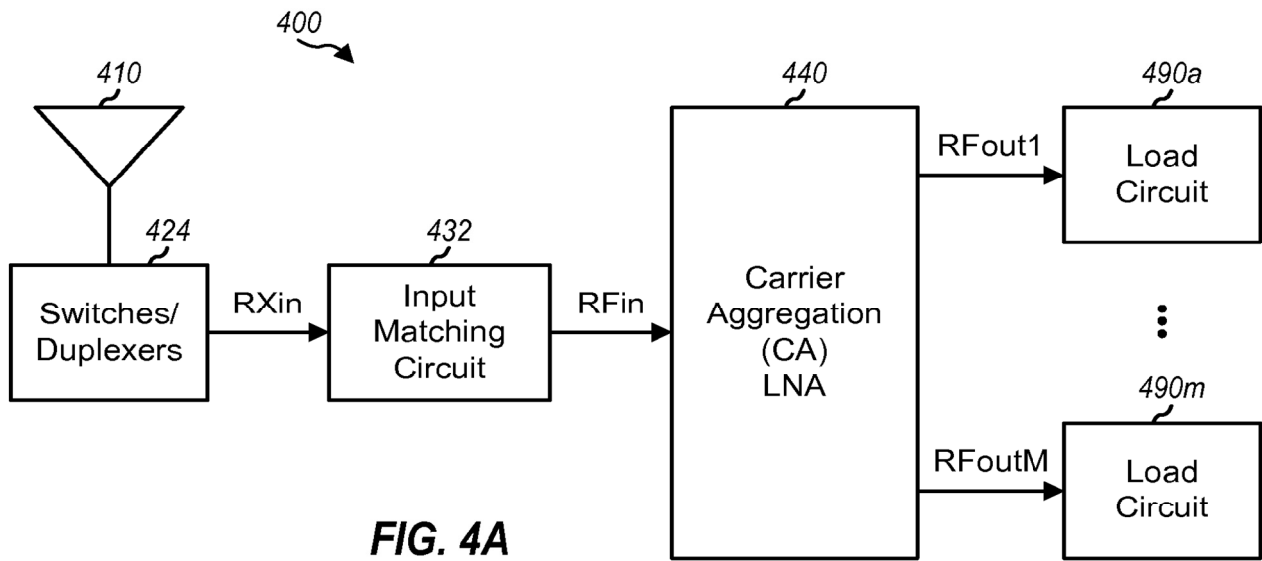


FIG. 4A

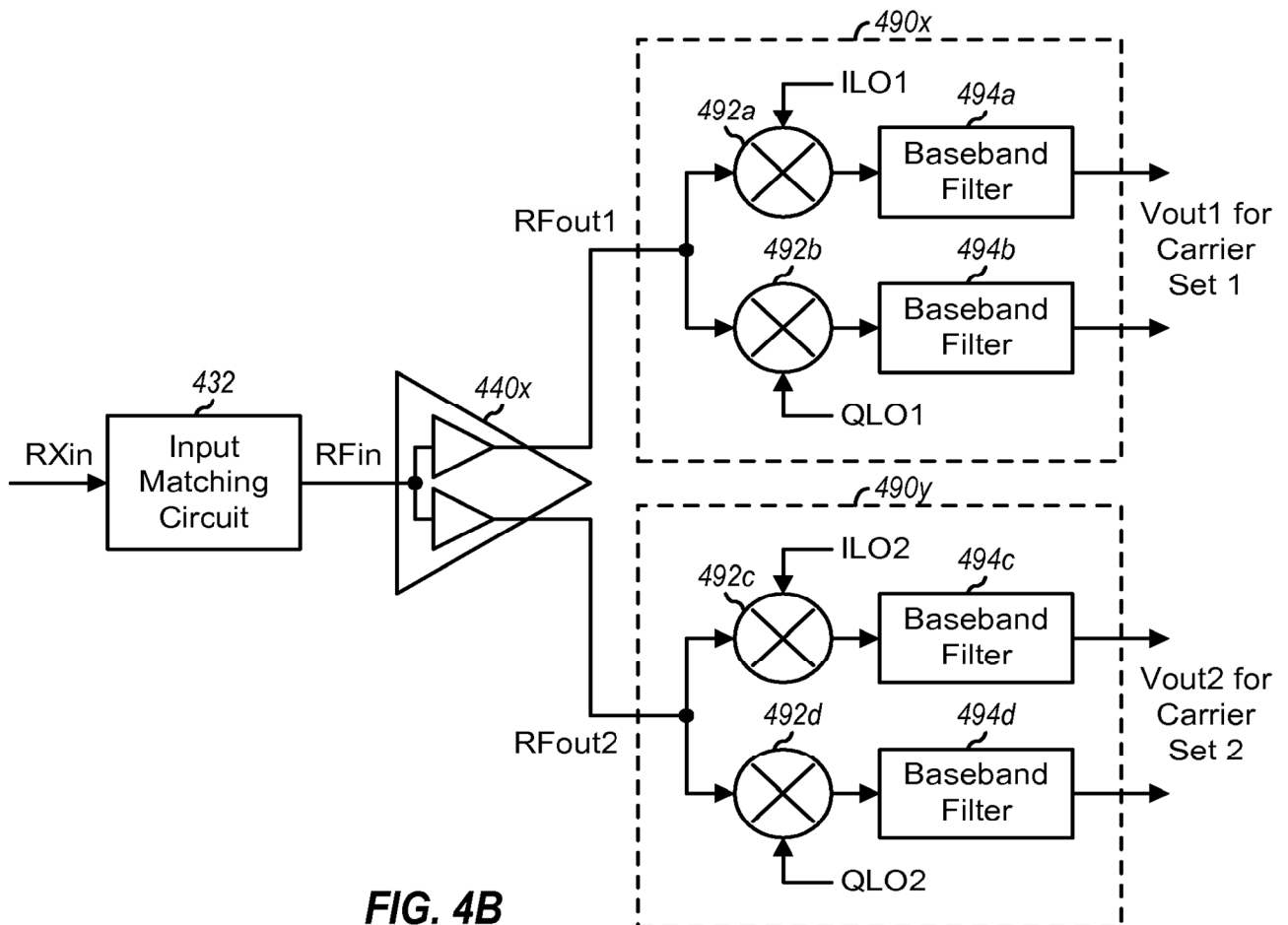


FIG. 4B

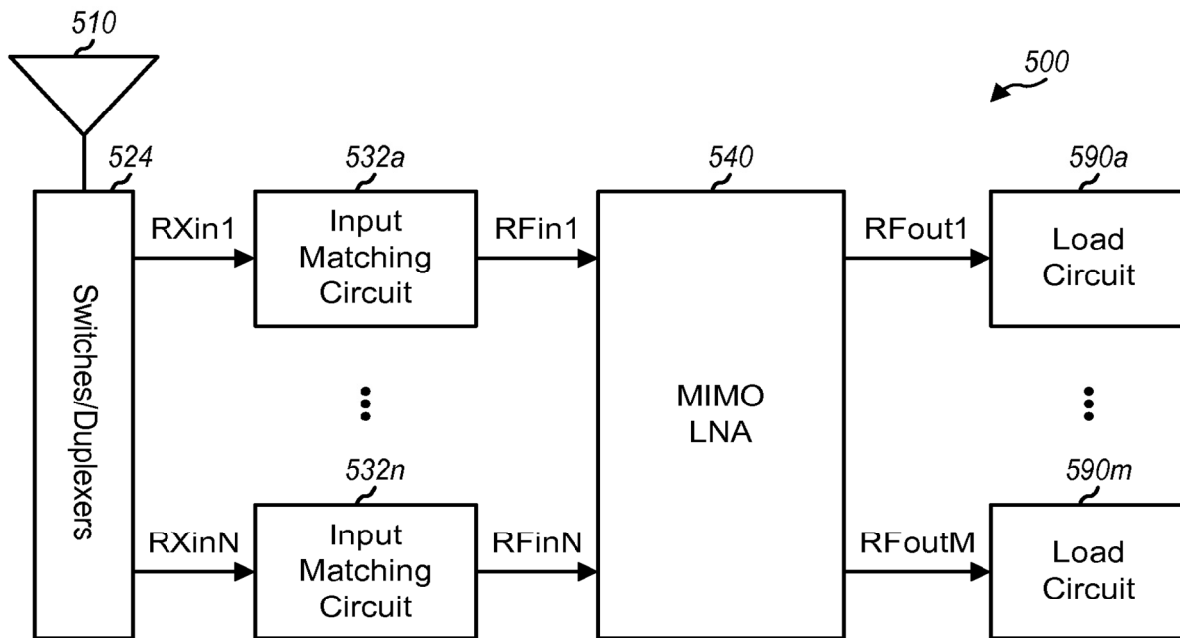


FIG. 5A

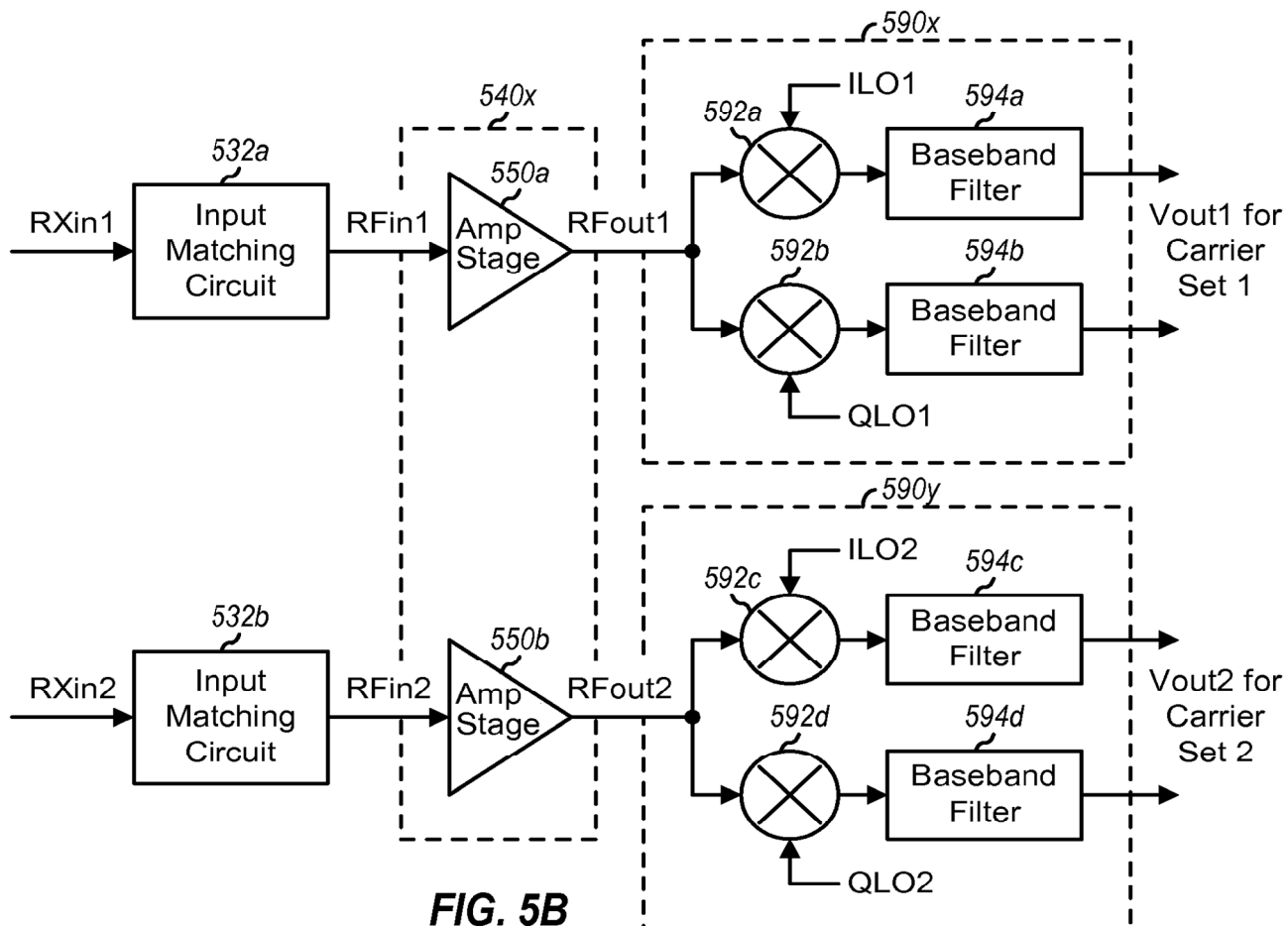


FIG. 5B

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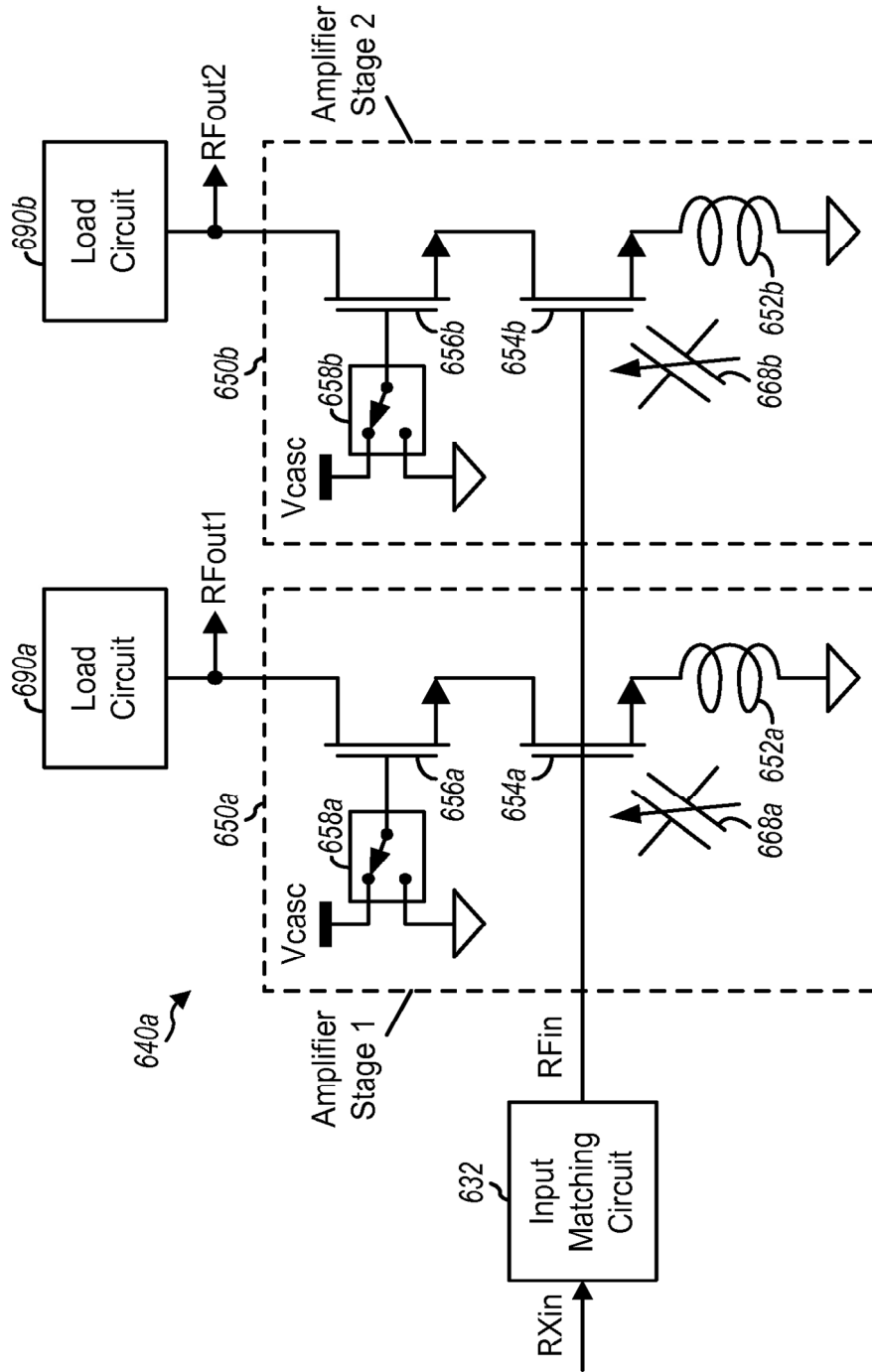
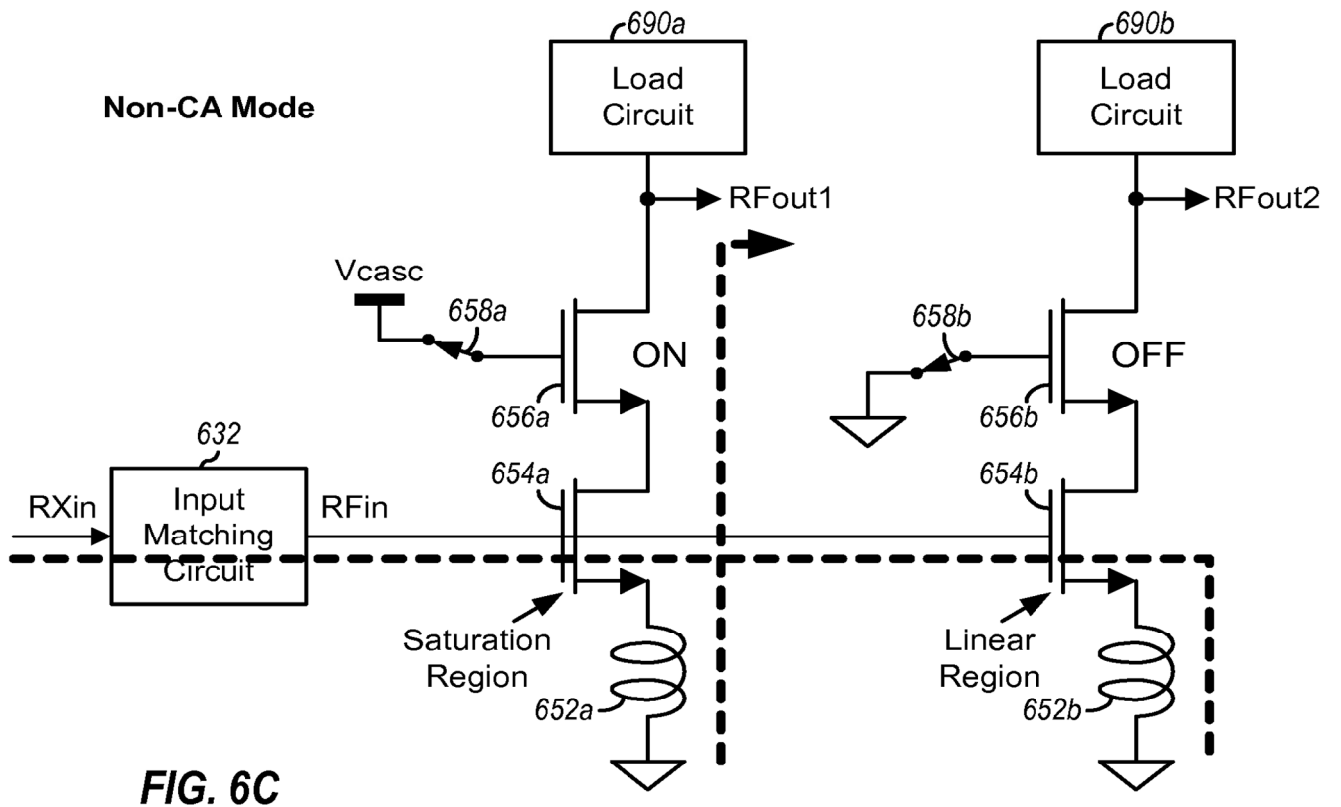
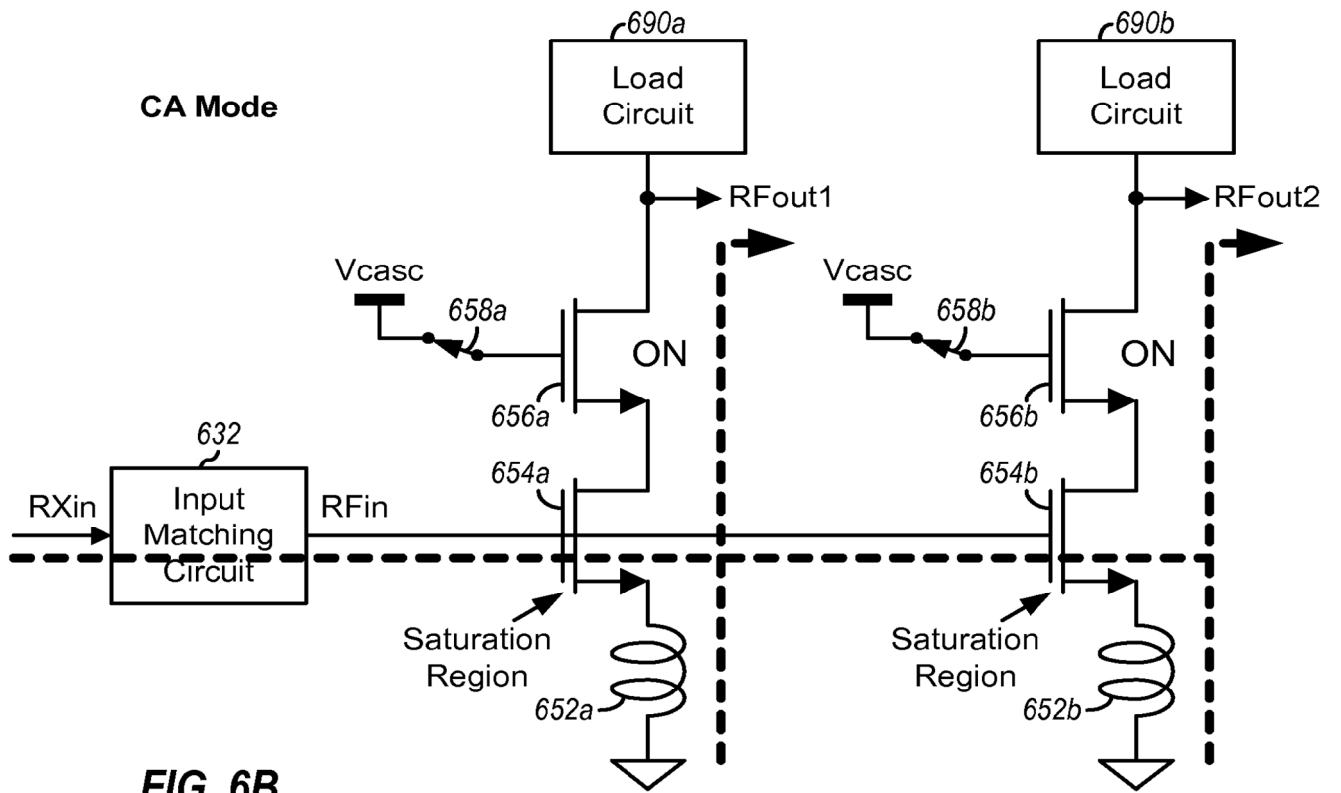


FIG. 6A



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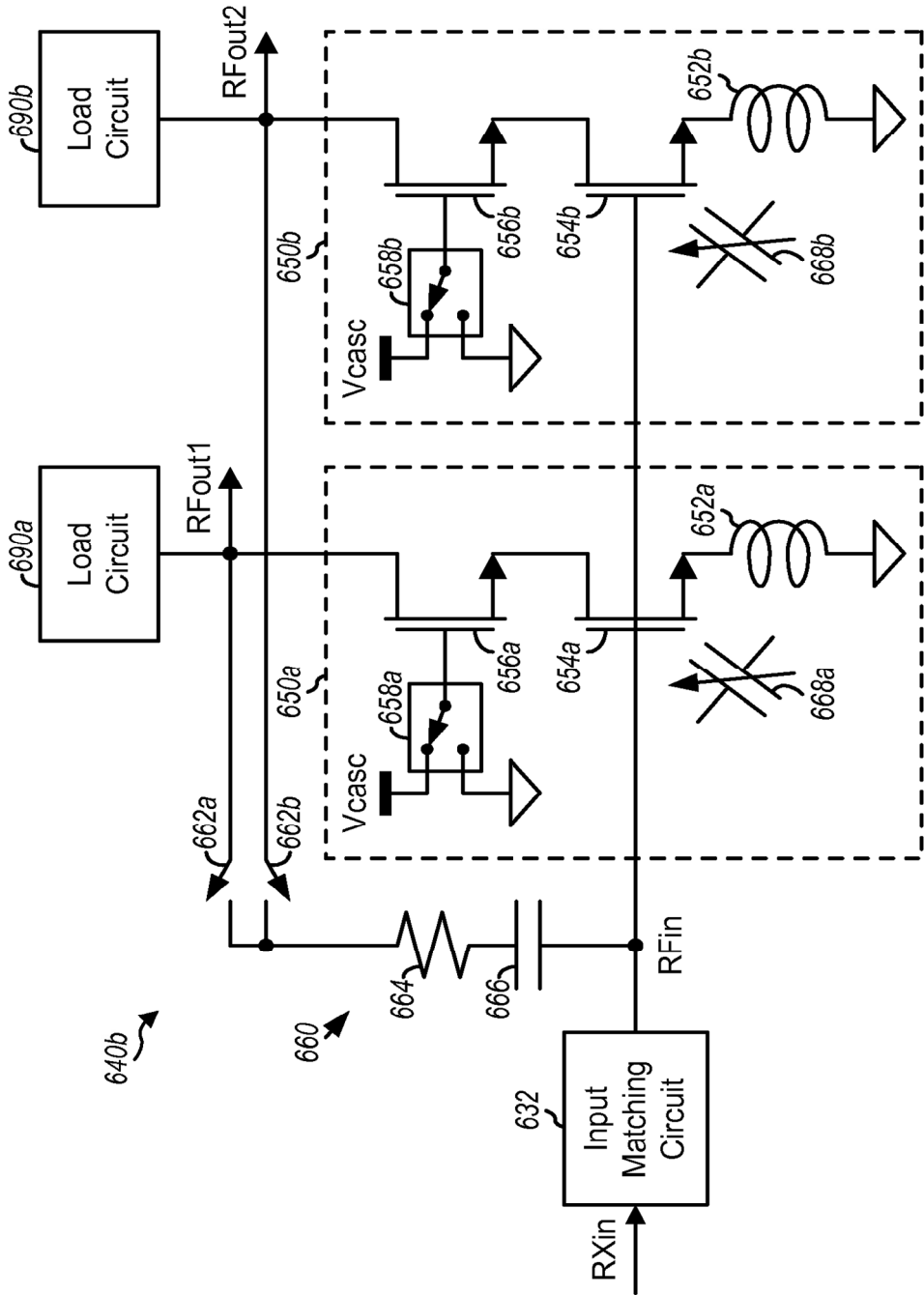


FIG. 7

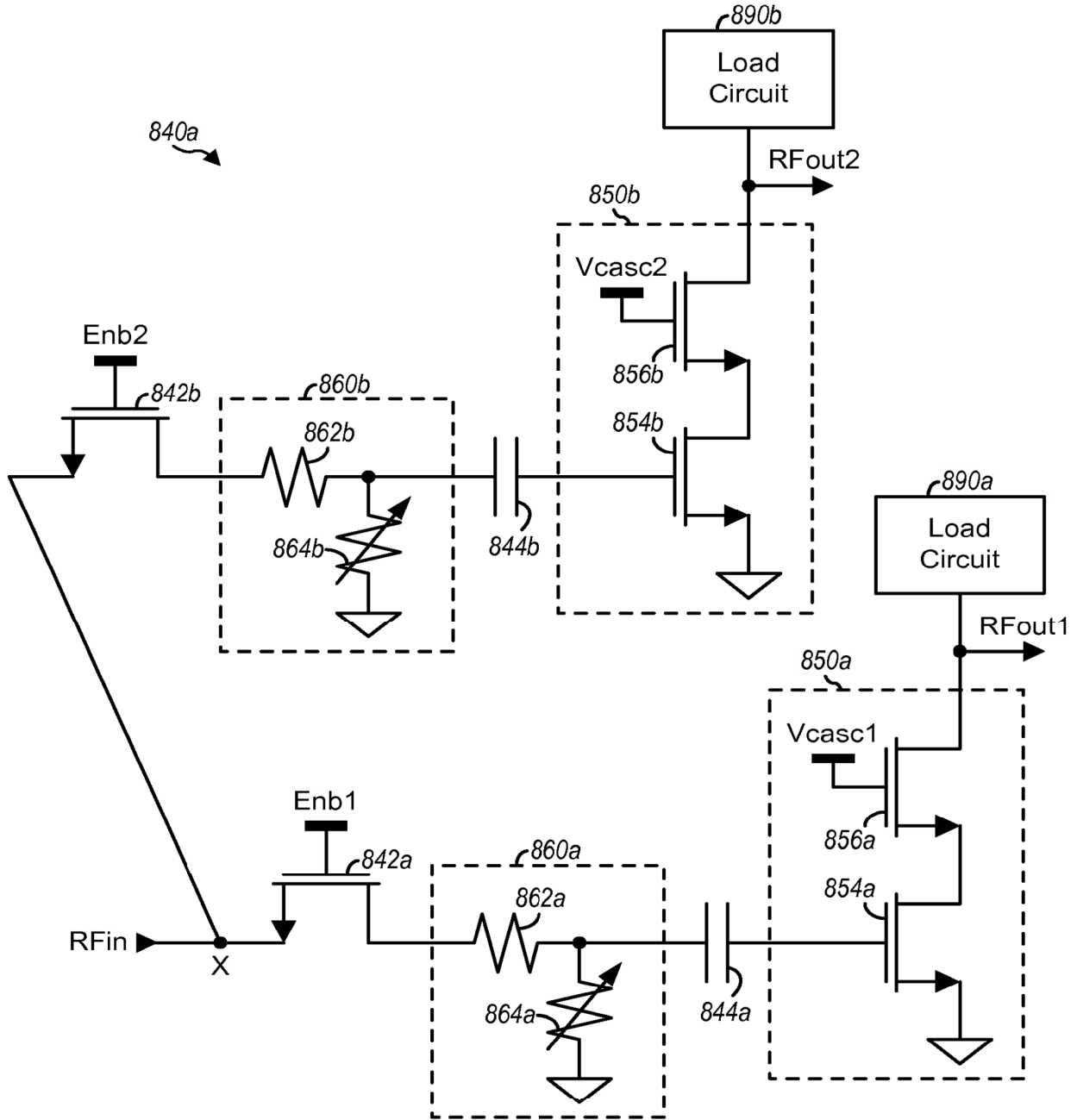


FIG. 8A

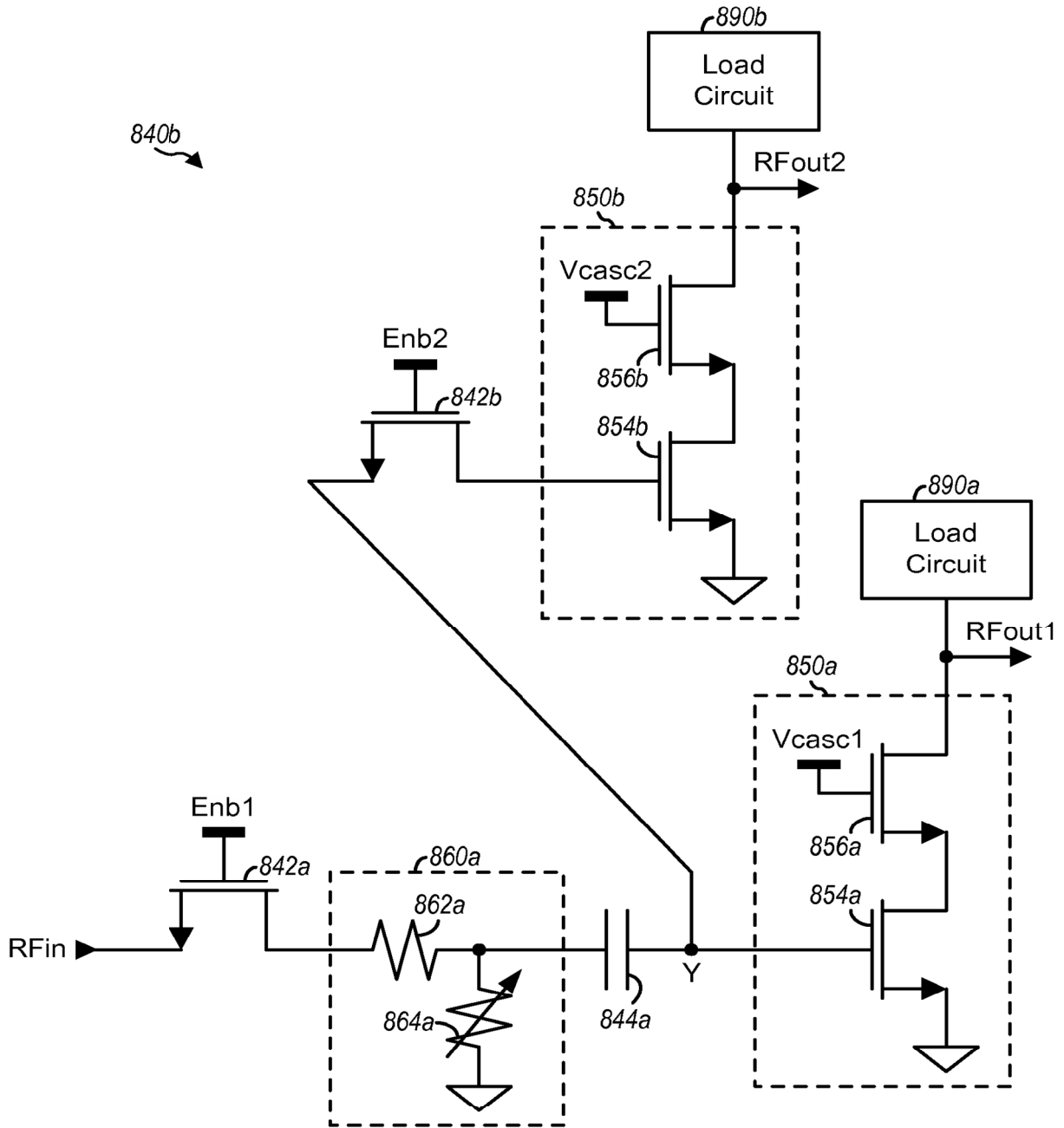


FIG. 8B

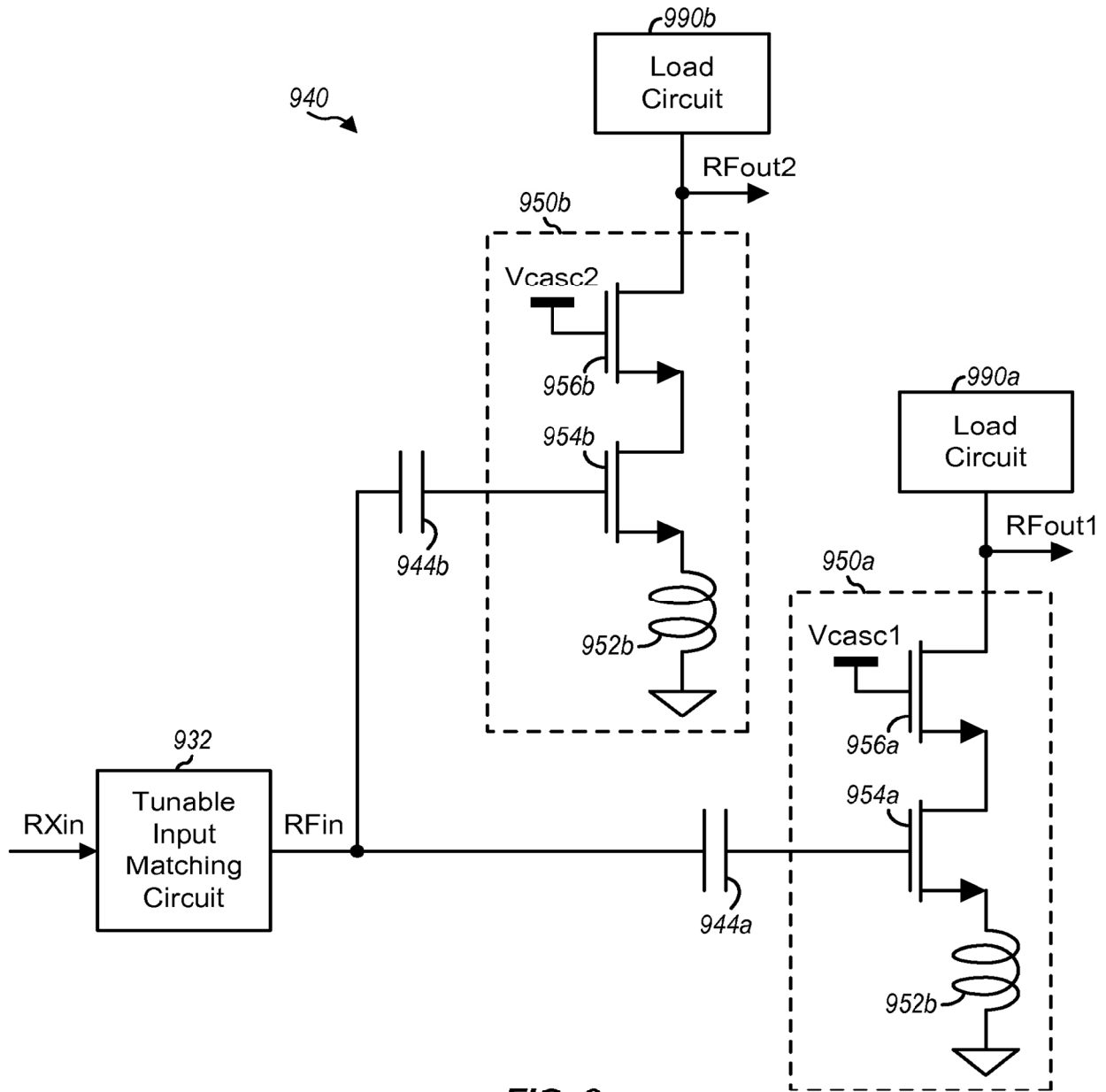


FIG. 9

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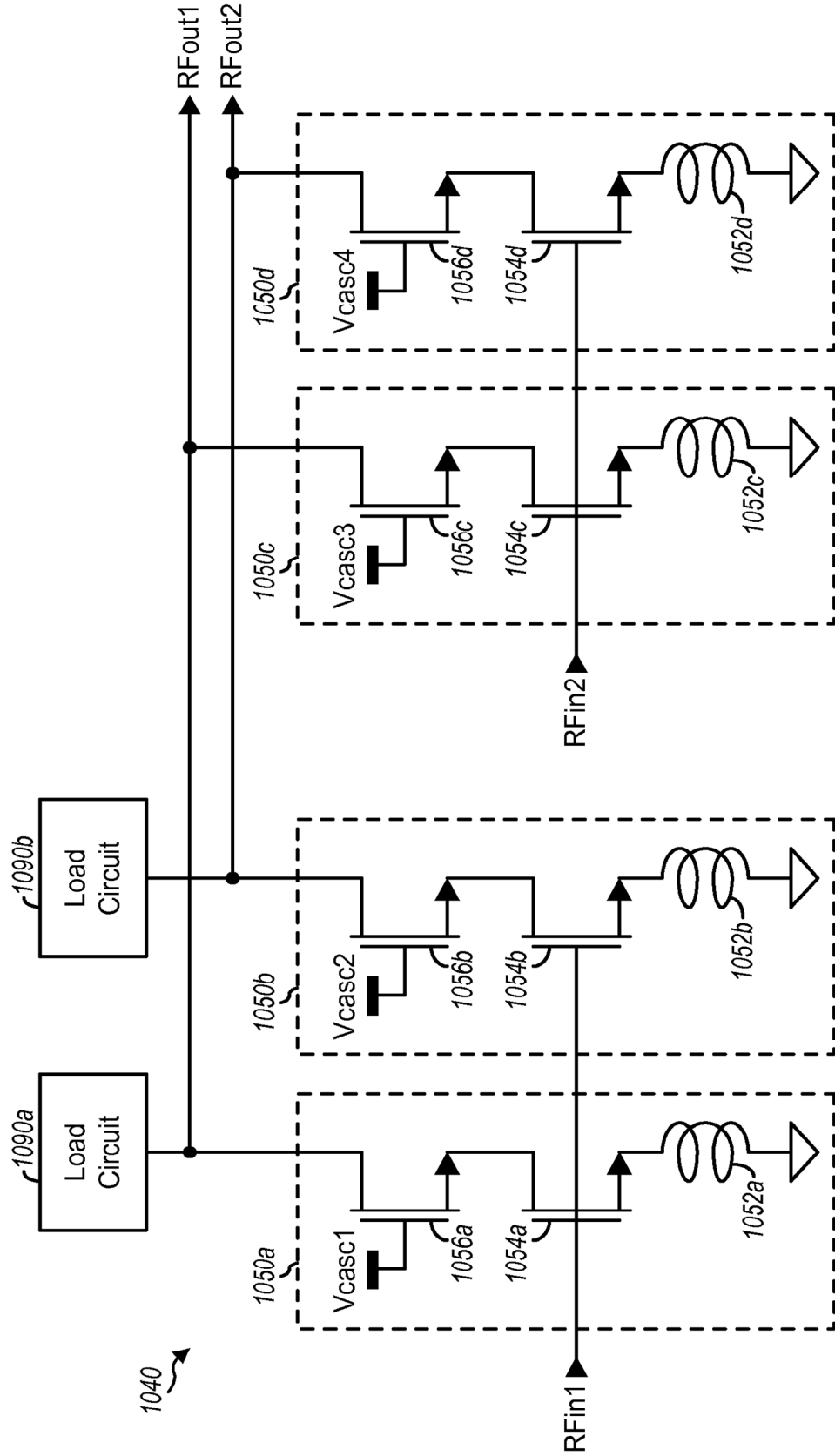


FIG. 10

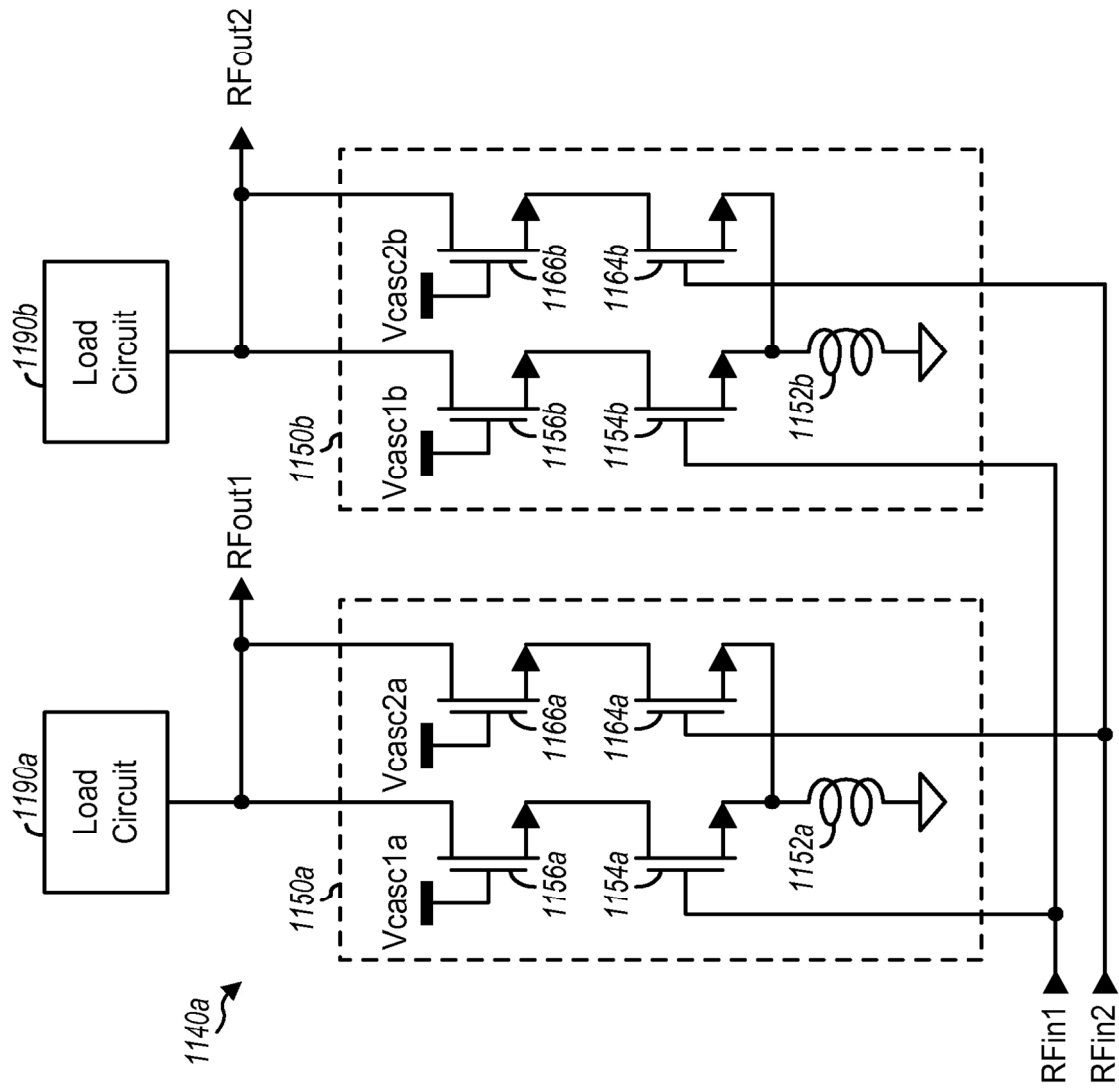


FIG. 11A

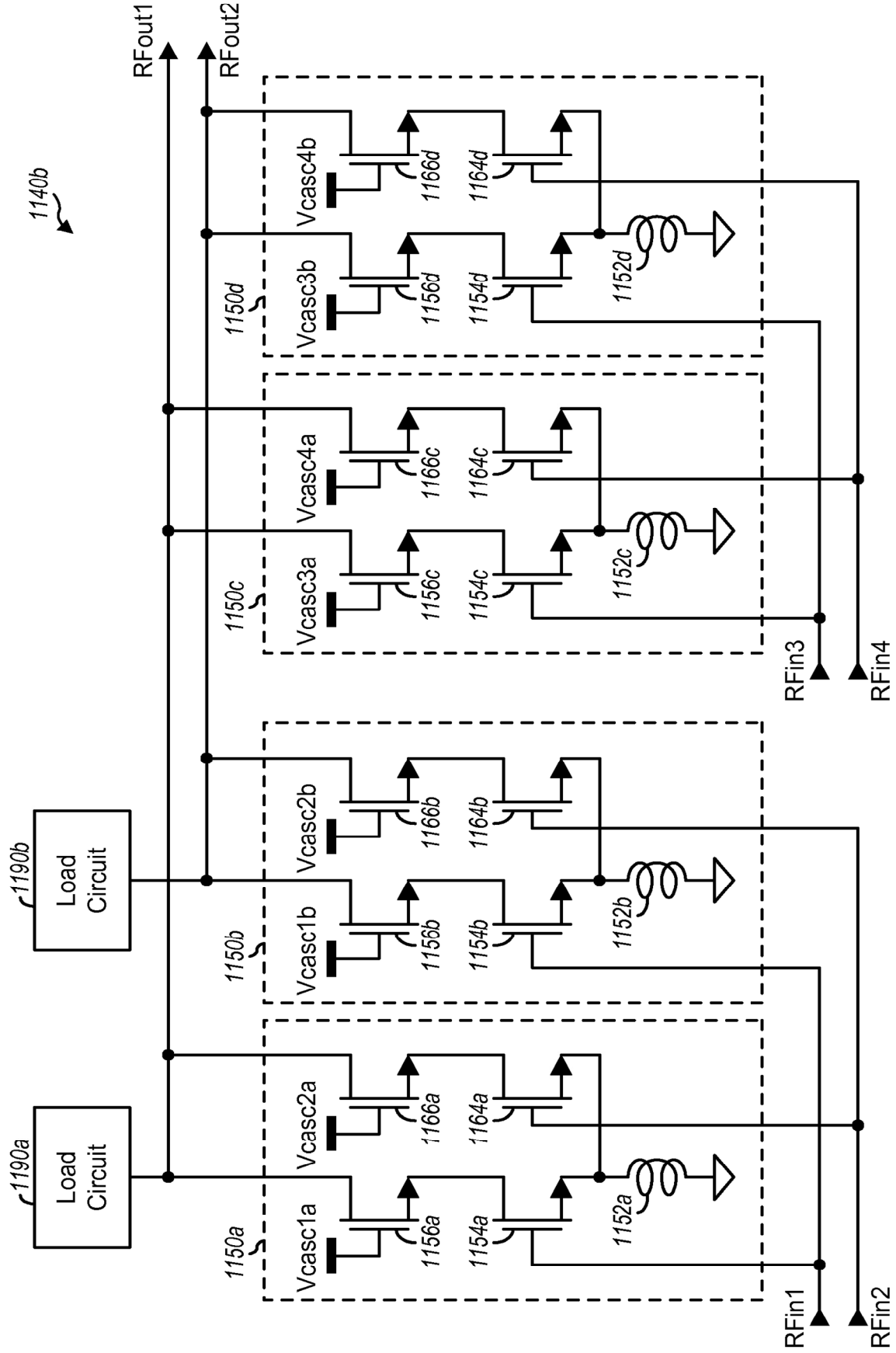


FIG. 11B



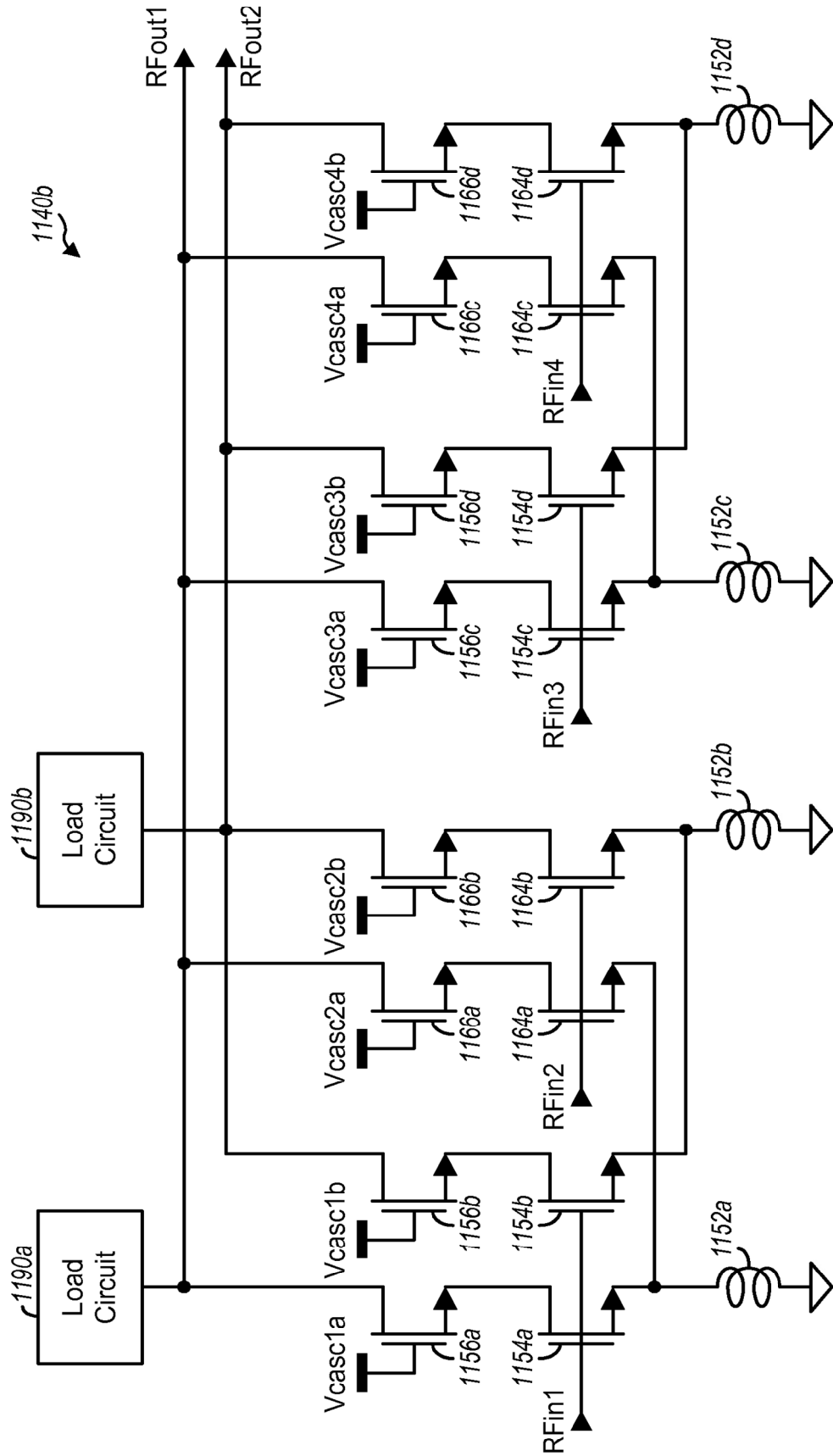
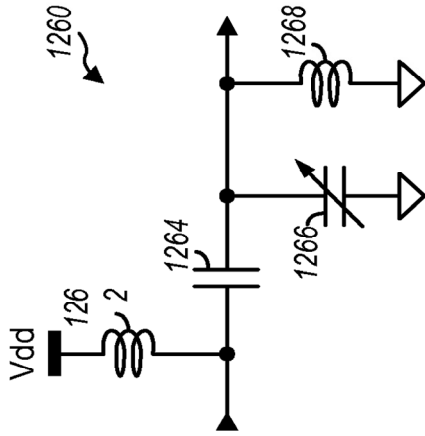
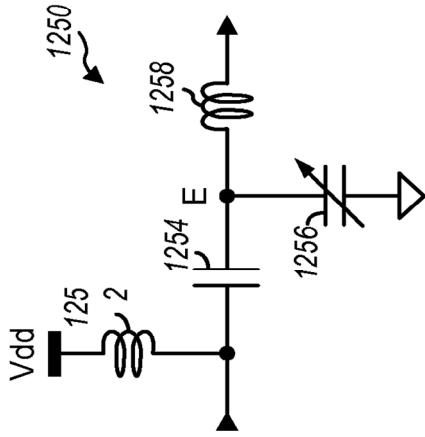
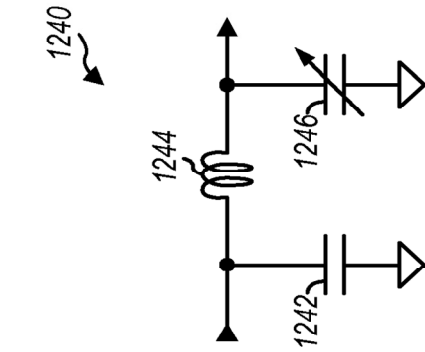
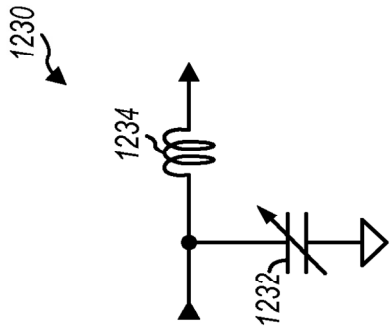
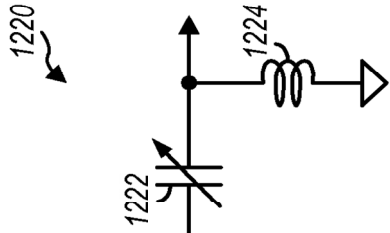
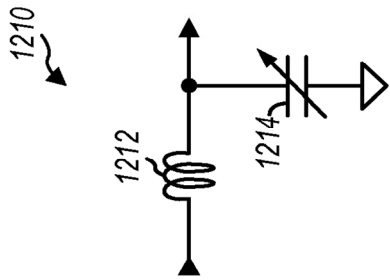


FIG. 11C



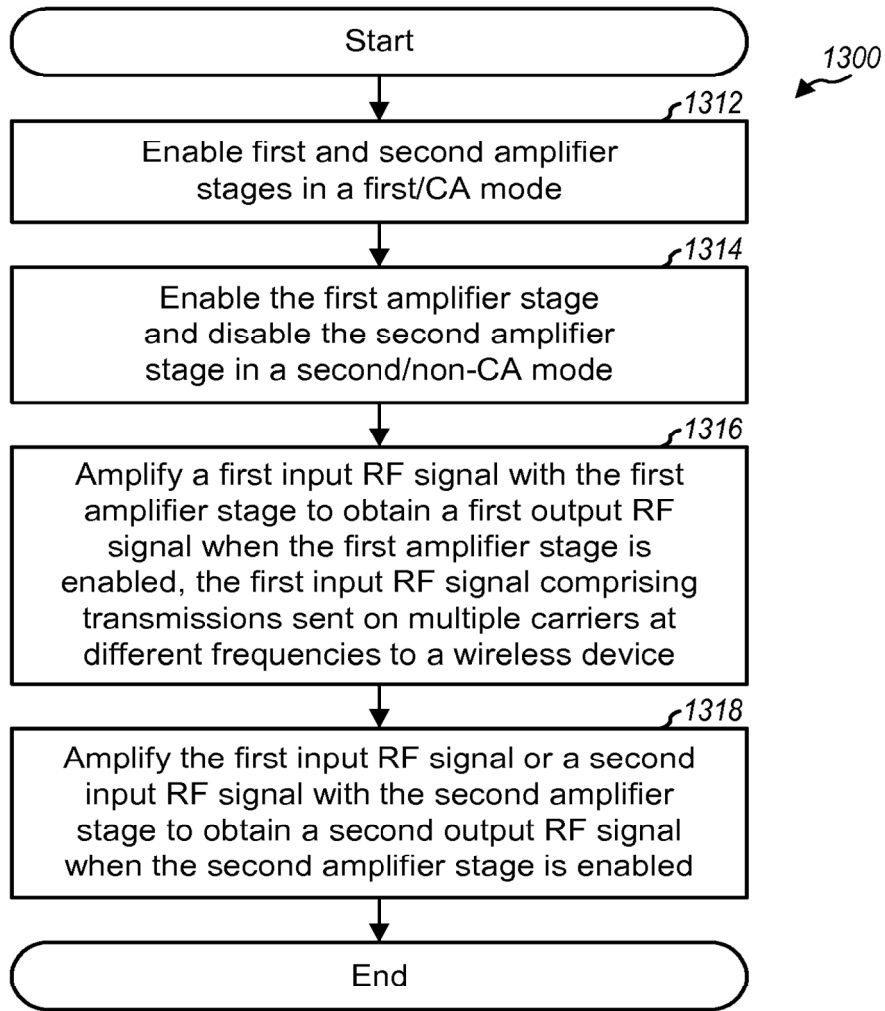


FIG. 13