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Paper No. 9
Entered: May 29, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

Case IPR2019-00128
Patent 9,154,356 B2

Before DANIEL N. FISHMAN, MICHELLE N. WORMMEESTER, and AARON W. MOORE, *Administrative Patent Judges*.

WORMMEESTER, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Intel Corporation[1] ("Petitioner") filed a Petition (Paper 3, "Pet.") requesting *inter partes* review of claims 1, 7, 8, 11, 17, and 18 of U.S. Patent No. 9,154,356 B2 (Ex. 1301, "the '356 patent"). Qualcomm Incorporated ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons that follow, we institute an *inter partes* review as to all the challenged claims of the '356 patent and all the grounds presented.

II. BACKGROUND

A. Related Proceedings

The parties identify a district court case in the Southern District of California in which Patent Owner asserted the '356 patent against Apple: *Qualcomm Incorporated v. Apple Incorporated*, No. 3:17-cv-02398 (S.D. Cal.). Pet. 1; Paper 4, 1. Petitioner indicates that the district court has dismissed this case. Paper 8, 1.

The parties also identify an International Trade Commission ("ITC") investigation in which Patent Owner has asserted the '356 patent against Apple. Pet. 1; Paper 4, 1. According to Petitioner, the parties have moved to terminate the investigation. Paper 8, 1.

[1] Intel Corporation identifies itself and Apple Inc. ("Apple") as real parties in interest. Paper 3, 1.

In addition, the parties identify four other petitions for *inter partes* review involving the '356 patent that Petitioner has filed. Pet. 1; Paper 4, 1.

B. The '356 Patent

The '356 patent describes low noise amplifiers. Ex. 1301, 1:15–16. Figure 6A, which is reproduced below, illustrates an example of a low noise amplifier according to the '356 patent. *Id.* at 1:54–55.

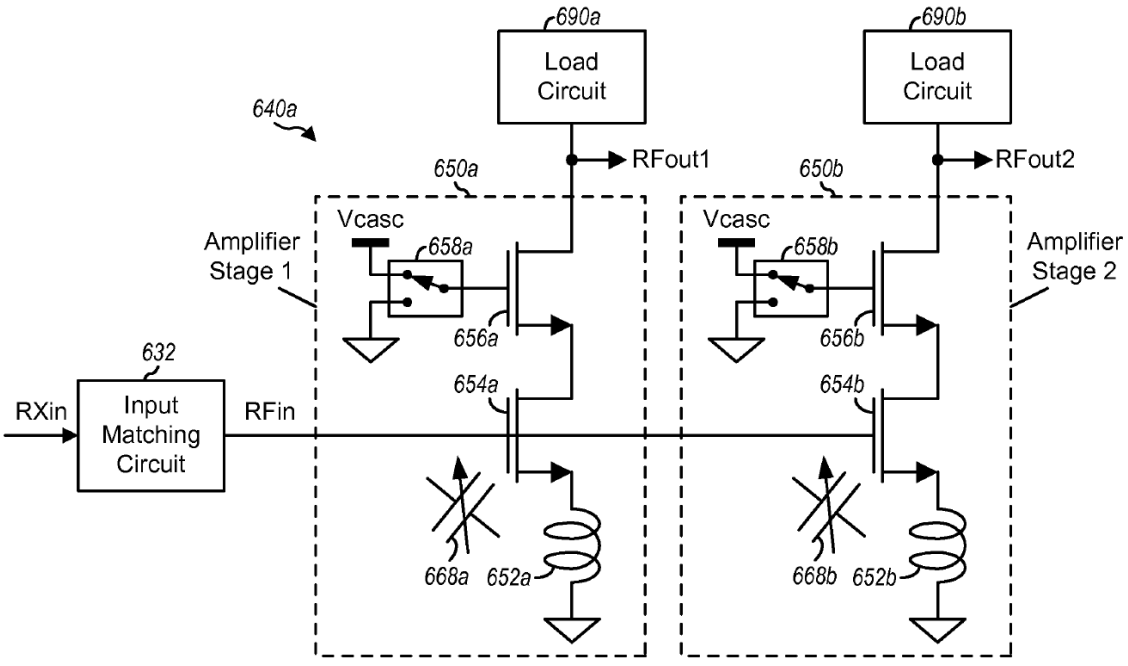

FIG. 6A

In particular, Figure 6A shows carrier aggregation low noise amplifier 640a, which has two amplifier stages 650a and 650b. *Id.* at 7:44–49. Amplifier stage 650a includes source degeneration inductor 652a, gain transistor 654a, cascode transistor 656a, and switch 658a. *Id.* at 7:58–8:4. Similarly, amplifier stage 650b includes source degeneration inductor 652b, gain transistor 654b, cascode transistor 656b, and switch 658b. *Id.* at 8:4–9. Both amplifier stages 650a and 650b are coupled to common input matching circuit 632 and to respective load circuits 690a and 690b. *Id.* at 7:47–49.

In operation, matching circuit 632 receives receiver input signal RXin, performs input matching for low noise amplifier 640a, and provides input RF signal RFin to low noise amplifier 640a. *Id.* at 7:49–52. Input RF signal RFin may include transmissions on one set of carriers or transmissions on two sets of carriers in the same band, with each set including one or more carriers. *Id.* at 7:55–57, 8:16–18, 8:30–32. An RF signal with transmissions on multiple sets of carriers is called a carrier aggregated RF signal. *Id.* at 8:16–18.

Low noise amplifier 640a operates in either a non-carrier aggregation (non-CA) mode or a carrier aggregation (CA) mode, depending on the type of input RF signal it receives. *Id.* at 8:24–32, 8:36–44. In the non-CA mode, low noise amplifier 640a receives transmissions on one set of carriers and provides one output RF signal to one load circuit. *Id.* at 8:30–32. Only one amplifier stage is enabled, while the other amplifier stage is disabled. *Id.* at 8:46–47. To illustrate, Figure 6C is reproduced below.

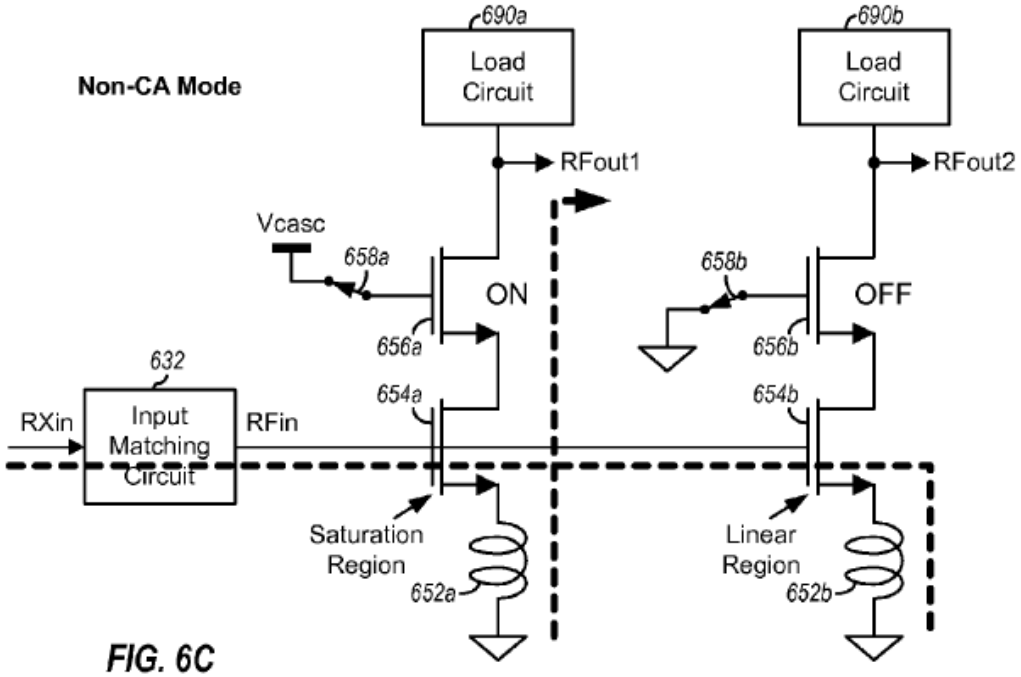

FIG. 6C

Figure 6C shows low noise amplifier 640a operating in the non-CA mode. *Id.* at 8:45–46. Amplifier stage 650a is enabled by connecting the gate of cascode transistor 656a to the Vcasc voltage via switch 658a, and amplifier stage 650b is disabled by shorting the gate of cascode transistor 656b to circuit ground via switch 658b. *Id.* at 8:47–52. Amplifier stage 650a amplifies the input RF signal and provides an output RF signal to load circuit 690a. *Id.* at 8:52–54.

In the CA mode, low noise amplifier 640a receives transmissions on two sets of carriers and provides two output RF signals to two load circuits, one output RF signal for each set of carriers. *Id.* at 8:32–35. Both amplifier stages are enabled. *Id.* at 8:37–38. To illustrate, Figure 6B is reproduced below.

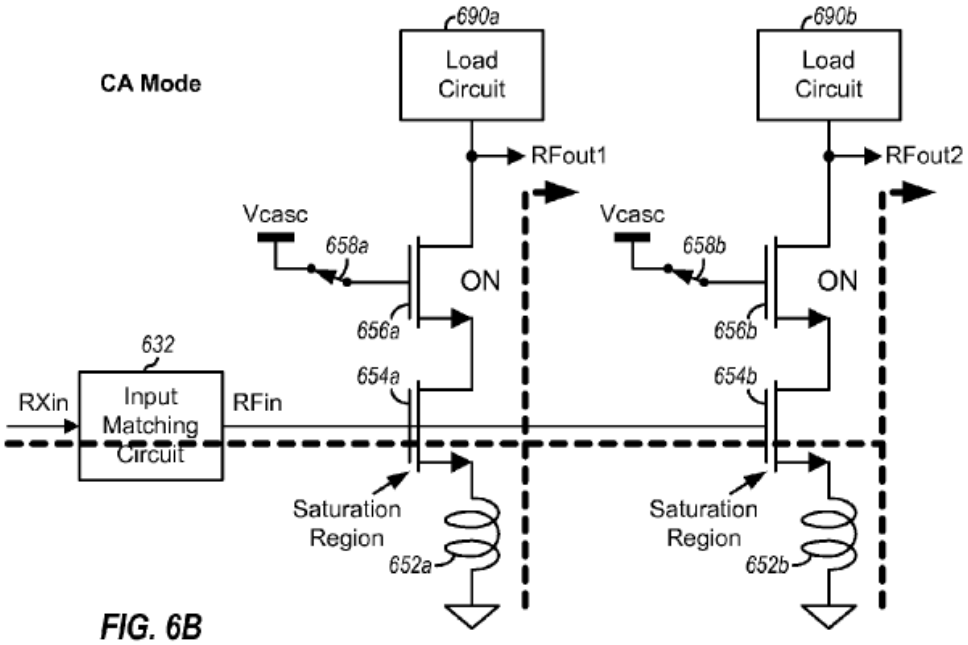

FIG. 6B

Figure 6B shows low noise amplifier 640a operating in the CA mode. *Id.* at 8:36–37. Amplifier stages 650a and 650b are enabled by connecting the gate of cascode transistor 656a to the Vcasc voltage via switch 658a and

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