IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMAZON WEB SERVICES, INC., AMAZON.COM, INC., and VADATA, INC.,

Petitioners

- vs. -

SRC LABS, LLC, and SAINT REGIS MOHAWK TRIBE,

Patent Owners

Patent No. 7,149,867
Issued: December 12, 2006
Inventors: Daniel Poznanovic, David E. Caliga, Jeffrey Hammes
Title: SYSTEM AND METHOD OF ENHANCING EFFICIENCY
AND UTLILZATION OF MEMORY BANDWITH
IN RECONFIGURABLE HARDWARE

Inter Partes Review No.

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,149,867
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.1-.80, 42.100-.123

Mail Stop Patent Board Patent Trial and Appeal Board P.O. Box 1450 Alexandria, VA 22313-1450

October 19, 2018



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		3.	Lange discloses and/or renders obvious "a data prefetch unit coupled to the memory."	7
		4.	Lange discloses and/or renders obvious that "the data prefetch unit retrieves only computational data required by the algorithm from a second memory of second characteristic	



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		memory bandwidth and/or memory utilization and places the retrieved computational data in the first memory."20
	5.	Lange discloses and/or renders obvious that "the data prefetch unit operates independent of and in parallel with logic blocks using the computional [sic] data."
	6.	Lange discloses "at least the first memory and data prefetch unit are configured to conform to needs of the algorithm."24
	7.	Lange discloses and/or renders obvious "the data prefetch unit is configured to match format and location of data in the second memory."
B.	CLA	IM 326
	1.	Lange discloses that "the data prefetch unit receives processed data from on-processor memory and writes the processed data to an external off-processor memory."26
C.	CLA	IM 4
	1.	Lange discloses "the data prefetch unit comprises at least one register from the reconfigurable processor."
D.	CLA	IM 530
	1.	Lange renders obvious that "the data prefetch unit is disassembled when another program is executed on the reconfigurable processor."
E.	CLA	IM 631
	1.	Lange discloses and/or renders obvious that "said second memory comprises a processor memory and said data prefetch unit is operative to retrieve data from a processor memory."
F.	CLA	IM 732
	1.	Lange discloses and/or renders obvious that "said processor memory is a microprocessor memory."32
G.	CLA	IM 8



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	2.	Lange discloses "a common memory."	33		
	3.	Lange discloses and/or renders obvious "one or more reconfigurable processors that can instantiate an algorithm hardware coupled to the common memory."			
	4.	Lange discloses and/or renders obvious "at least one of the reconfigurable processors includes a data prefetch unit to read and write only data required for computations by the algorithm between the data prefetch unit and the common memory."			
	5.	Lange discloses and/or renders obvious "the data prefetch unit operates independent of and in parallel with logic blocusing the computational data."	ks 35		
	6.	Lange discloses and/or renders obvious "the data prefetch unit is configured to conform to needs of the algorithm and match format and location of data in the common memory.			
I.	CLAIM 11				
	1.	Lange discloses and/or renders obvious "the at least of [sic the reconfigurable processors also includes a computational unit coupled to the data access unit."	ıl		
J.	CLAIM 12				
	1.	Lange discloses and/or renders obvious "the computational unit is supplied the data by the data access unit."			
K.	CLAIM 13				
	1.	Lange discloses and/or renders obvious "[a] method of transferring data comprising transferring data between a memory and a data prefetch unit in a reconfigurable processor."	37		



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	2.	Lange discloses and/or renders obvious "transferring the data between a computational unit and the data access unit."38		
	3.	Lange discloses and/or renders obvious "the computational unit and the data access unit, and the data prefetch unit are configured to conform to needs of an algorithm implemented on the computational unit and transfer only data necessary for computations by the computational unit."		
	4.	Lange discloses and/or renders obvious "the prefetch unit operates independent of and in parallel with the computational unit."		
L.	CLA	IM 1439		
	1.	Lange discloses "the data is written to the memory."39		
	2.	Lange discloses "transferring the data from the computational unit to the data access unit."		
	3.	Lange discloses "writing the data to the memory from the data prefetch unit."		
M.	CLA	IM 1540		
	1.	Lange discloses that "the data is read from the memory." 40		
	2.	Lange discloses and/or renders obvious "transferring only the data desired by the data prefetch unit as required by the computational unit from the memory to the data prefetch unit."		
	3.	Lange renders obvious "reading the data directly from the data prefetch unit to the computational unit through a data access unit."		
N.	CLA	CLAIM 164		
	1.	Lange discloses and/or renders obvious "all the data transferred from the memory to the data prefetch unit is processed by the computational unit."		
\circ	CI A	IM 17		



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