U.S. Patent No. 7,149,867- Declaration of Brad L. Hutchings, Ph.D.

IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMAZON WEB SERVICES, INC., AMAZON.COM, INC., and VADATA, INC.,

Petitioners

- VS. -

SRC LABS, LLC, and SAINT REGIS MOHAWK TRIBE,

Patent Owners

Patent No. 7,149,867 Issued: December 12, 2006 Inventors: Daniel Poznanovic, David E. Caliga, Jeffrey Hammes Title: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTLILZATION OF MEMORY BANDWITH IN RECONFIGURABLE HARDWARE

Inter Partes Review No.

DECLARATION OF BRAD L. HUTCHINGS, PH.D., IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,149,867

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		2. Zhong17
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	vi.	"and wherein at least the first memory and data prefetch unit are configured to conform to needs of the algorithm" 32
	vii.	"and the data prefetch unit is configured to match format and location of data in the second memory."33
2.	Lange '867 I	e Anticipates and/or Renders Obvious Claim 3 of the Patent
	i.	"The reconfigurable processor of claim 1, wherein the data prefetch unit receives processed data from on- processor memory and writes the processed data to an external off-processor memory."
3.	Lange '867 I	Anticipates and/or Renders Obvious Claim 4 of the Patent
	i.	"The reconfigurable processor of claim 1, wherein the data prefetch unit comprises at least one register from the reconfigurable processor."
4.	Lange	e Renders Obvious Claim 5 of the '867 Patent
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	iv.	"wherein at least one of the reconfigurable processors includes a data prefetch unit to read and write only data required for computations by the algorithm between the data prefetch unit and the common memory" 44
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	vi.	"and wherein the data prefetch unit is configured to conform to needs of the algorithm and match format and location of data in the common memory."
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