UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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AMAZON WEB SERVICES, INC., AMAZON.COM, INC., and
VADATA, INC.,
Petitioner,

v.

SAINT REGIS MOHAWK TRIBE,
Patent Owner.

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IPR2019-00103
Patent 7,149,867 B2

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Before KALYAN K. DESHPANDE, JUSTIN T. ARBES,
and CHRISTA P. ZADO, *Administrative Patent Judges*.

ZADO, *Administrative Patent Judge*.

DECISION
Denying Petitioner's Request on Rehearing of
Decision Denying Institution of *Inter Partes* Review
35 U.S.C. § 42.71(d)

I. INTRODUCTION

Amazon Web Services, Inc., Amazon.com, Inc., and VADATA, Inc. (collectively, "Petitioner") seek rehearing (Paper 23, "Request" or "Req. Reh'g") of our Decision Denying *Inter Pates* Review (Paper 22, "Decision" or "Dec."). According to Petitioner, the sole reason for our denial was based on the erroneous finding that the Petition (Paper 1, "Petition" or "Pet.") did not specify how the prior art references—Lange and Zhong—each teach a "data prefetch unit" as properly construed. Req. Reh'g 2.

We have considered Petitioner's Request, but for the reasons that follow, we decline to modify our Decision.

II. LEGAL STANDARD

A party requesting rehearing bears the burden of showing that the decision should be modified. 37 C.F.R. § 42.71(d). "The request must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed in a motion, an opposition, or a reply." *Id.* "When rehearing on petition, a panel will review the decision for an abuse of discretion." 37 C.F.R. § 42.71(d).

III. DISCUSSION

The Petition did not propose any construction of the claim term "data prefetch unit," as recited in challenged independent claims 1, 9, and 13. Pet. 6–7. Rather, the Petition identified the constructions proposed by the parties in district court proceedings in which Petitioner argued the term is indefinite. *Id.* The Petition asserted that because indefiniteness cannot be raised in an *inter partes* review, the Board should adopt the construction

proposed by Patent Owner in district court—i.e., "a functional unit that retrieves computational data needed to complete the algorithm instantiated on the reconfigurable processor during processing" (hereinafter, the "proposed district court construction"). *Id.* at 6. Petitioner provided no argument or evidence to support this construction, which we rejected in the Decision because it is contrary to the express definition provided in the specification of U.S. Patent No. 7,149,867 B2 (Ex. 1001, "the '867 patent"). Dec. 9–10. The '867 patent specification expressly defines "data prefetch unit" under the heading "Definitions" as follows:

> 1. Definitions: . . . Data prefetch Unit—is a functional unit that moves data between members of a memory hierarchy. The movement may be as simple as a copy, or as complex as an indirect indexed strided copy into a unit stride memory.

Ex. 1001, 5:18, 5:40–43. The '867 patent defines "memory hierarchy" as "a collection of memories." *Id.* at 5:39. In accordance with the express definition set forth in the patent specification, we construed "data prefetch unit" as "a functional unit that moves data between members of a memory hierarchy. The movement may be as simple as a copy, or as complex as an indirect indexed strided copy into a unit stride memory," wherein a "memory hierarchy" is "a collection of memories." Dec. 10.

The Petition applied only the proposed district court construction in arguing that the prior art references—Lange and Zhong—each teach a "data prefetch unit," and failed to assert that these references teach a "data prefetch unit" as the term is defined in the '867 patent. Dec. 15–19. Prior to the Decision, Petitioner sought leave to file a reply in order to address the express definition of "data prefetch unit" set forth in the '867 patent specification. Paper 21, 2–3. We denied Petitioner's request, explaining

that Petitioner had not shown that it could not have foreseen, and addressed in the Petition, a construction "taken directly from the specification of the challenged patent." *Id.* at 3.

In the Decision, we explained the Petition must specify with particularity where each element of the claim is found in the prior art. Dec. 16 (citing 37 C.F.R. §§ 42.104(b)(4), 42.22(a)(2), 42.104(b)(5); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) ("In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.")). We found that in applying the proposed district court construction of "data prefetch unit," the Petition did not "specify with particularity how [either] Lange [or Zhong] teaches a memory hierarchy, and moving data between members of a memory hierarchy, as required under our interpretation" of "data prefetch unit." *Id.* at 16, 19. We acknowledged that the Petition identified a first memory and a second memory, as recited in the claims, but found that the Petition fell short of specifying that these memories comprise a memory hierarchy or explaining why that would be the case. *Id.* at 16–20. We explained that in so doing, Petitioner improperly placed the burden on the Board to ascertain how the prior art allegedly reads on the challenged claims. *Id.* at 17, 19.

In the Request, Petitioner argues our Decision was erroneous for two reasons: 1) the Petition explicitly described both Lange and Zhong as being directed to improving the movement of data within "memory hierarchies," and 2) our construction of "data prefetch unit" did not add any requirements that were not already in the claims. Req. Reh'g 2–5.

As to the first reason, Petitioner identifies where the Petition quoted: a) Lange as "seek[ing] to improve the performance of 'memory hierarchies'

using 'techniques such as pre-fetching and streaming,'" and b) Zhong as disclosing "implementing prefetching in 'configurable memory hierarchies' to improve application memory behavior." Req. Reh'g 2–3 (citing Pet. 8–9, 11) (emphases omitted). These quotes do not persuade us to alter our Decision. These quotes did not appear in Petitioner's analysis of how the prior art reads on the claims, but instead appeared in an "Overview of the Prior Art." Pet. 8–9, 11. Moreover, the Petition did not tie these quotes to the language of the claims or specify how either Lange or Zhong teach a "data prefetch unit" that moves data between memories of a memory hierarchy. *Id.* at 8–9, 11, 17–19, 48–50. It was insufficient for Petitioner to broadly cite to and/or quote the prior art references, without specifying its assertion as to what in Lange and Zhong comprises memory hierarchies and how the alleged "data prefetch unit" in each reference moves data between members of an asserted memory hierarchy. Accordingly, we are not persuaded that we overlooked these teachings of Lange and Zhong because Petitioner did not adequately present these teachings.

The Request also cites to language in the Petition relating to claim 11, which does not recite a "data prefetch unit," but rather recites a "data access unit." Req. Reh'g 3 (citing Pet. 36). The Petition asserted Lange discloses and/or renders obvious a reconfigurable processor that includes a computational unit coupled to a "data access unit." Pet. 35. Petitioner argued that the '867 patent defines a "data access unit" as a "functional unit that accesses a component of a memory hierarchy, and delivers data directly to computational logic." *Id.* at 35–36 (citing Ex. 1001, 5:44–46). Petitioner further argued that front-end interfaces in Lange "access a component of a memory hierarchy"—i.e., streaming ports access FIFO memories and caching ports access BlockSelectRAM. *Id.* at 36. This argument in the

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