

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMAZON WEB SERVICES, INC.,
AMAZON.COM, INC., and VADATA, INC.,
Petitioners,

v.

SAINT REGIS MOHAWK TRIBE,
Patent Owner.

Case IPR2019-00103
Patent 7,149,867 B2

PETITIONERS' REQUEST FOR REHEARING UNDER 37 C.F.R. § 42.71

Pursuant to 37 C.F.R. § 42.71, Petitioners Amazon Web Services, Inc., Amazon.com, Inc., and VADATA, Inc. respectfully request rehearing of the Board’s Decision Denying Institution of *Inter Partes* Review of U.S. Patent No. 7,149,867 (Paper 22) (“Decision”) because the Board “misapprehended or overlooked” matters addressed by the Petition and thus abused its discretion in denying institution. *See* 37 C.F.R. § 42.71(c) and (d).

All claims challenged in the Petition require a “data prefetch unit.” *See* Ex. 1001. The Board construed the term as:

“a functional unit that moves data between members of a memory hierarchy. The movement may be as simple as a copy, or as complex as an indirect indexed strided copy into a unite stride memory,’ wherein a ‘memory hierarchy’ is ‘a collection of memories.’”

Decision at 10. Neither the Board, Patent Owner, nor the patent itself defines “collection of memories,” and so the plain and ordinary meaning applies; it is a pair or group of memories, *i.e.*, two or more memories. The Board denied institution solely because it found that the Petition did not specify how each prior art reference—Lange and Zhong—“taught a memory hierarchy and moving data between members of a memory hierarchy,” which under the Board’s construction is “a collection of memories.” Decision at 16-19. In light of the record, this denial is erroneous for at least two reasons.

First, the Petition explicitly describes that both Lange and Zhong are directed

to improving the movement of data within “*memory hierarchies*,” quoting the references directly:

Petition at 8-9: Lange “seeks to improve the performance of ‘*memory hierarchies*’ using ‘techniques such as pre-fetching and streaming’”;

Petition at 11: Zhong discloses implementing prefetching in “configurable *memory hierarchies*” to improve application memory behavior.

Petition at 36: “The front-end interfaces ‘access a component of a *memory hierarchy*’: the streaming ports access the FIFO memories, and the caching ports access the BlockSelectRAM.” (emphases added).

Second, the Board’s construction of “data prefetch unit” did not add any requirements that were not already in the claim, and Petitioners explained in detail how the asserted prior art references met each requirement of the challenged claims. For example, the language of claim 1 already requires that the data prefetch unit moves data between the first memory and the second memory, *i.e.*, members of a collection of memories. Ex. 1001 at claim 1 (“[T]he data prefetch unit retrieves only computational data required by the algorithm from a second memory of second characteristic memory bandwidth and/or memory utilization and places the retrieved computational data in the first memory.”) The Board’s construction of the “data prefetch unit” does not add any requirement not already present in the language of the claim itself. And the Petition explained in detail how both Lange and Zhong

disclose a functional unit that *moves* (*i.e.*, retrieves and places) data between the first memory and the second memory, *i.e.*, members of a collection of memories. *See, e.g.*, Petition at 18-22, 47-52. The Board made no contrary finding. *See* Decision. Indeed, it acknowledged in its Decision that the Petition explains how both Lange and Zhong teach at least two memories. Decision at 16-17 (“Petitioner asserts that Lange discloses a first memory (*i.e.*, either the FIFO memory in the MARC core or BlockSelectRAM in the FPGA) and a second memory (*i.e.*, SRAM and/or DRAM accessed by the MARC core back-end ports), as recited in the claim.”); *id.* at 18-19 (“Petitioner asserts that Zhong discloses a first memory (*i.e.*, prefetch buffers) and a second memory (*i.e.*, main memory or L2 cache), as recited in the claim”). Thus, the Petition explained how Lange and Zhong disclose the claimed data prefetch unit as construed by the Board. Notably, Patent Owner did not argue otherwise in its preliminary response; it did not address disclosures of Lange and Zhong at all. *See* Preliminary Response.

Petitioners explained in the Petition how Lange and Zhong disclose every aspect of the “data prefetch unit” as construed by the Board using the very language from the Board’s construction. Petitioners identified in each reference a memory hierarchy with the first and second memories of the claims and upon which the data prefetch unit acts by moving data between the memories. *See* Petition at 17-22, 47-52. There are no additional or separate requirements in the Board’s construction.

See IPR2018-01600, Paper No. 20 (this same panel of administrative patent judges properly granted institution against the same Patent Owner after construing claim terms differently than Petitioner proposed).

Petitioners respectfully request that the Board rehear the Decision and grant institution based on both grounds raised in the Petition. *See* 37 C.F.R. § 42.71(c) and (d).

Dated: June 3, 2019

Respectfully submitted,
FENWICK & WEST LLP

/s/ J. David Hadden

J. David Hadden, Reg. No. 40,629

Counsel for Petitioners
AMAZON WEB SERVICES, INC.,
AMAZON.COM, INC., and
VADATA, INC.

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