UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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AMAZON WEB SERVICES, INC., AMAZON.COM, INC., and
VADATA, INC.,
Petitioner,

v.

SAINT REGIS MOHAWK TRIBE,
Patent Owner.

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Case IPR2019-00103
Patent 7,149,867 B2

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Before KALYAN K. DESHPANDE, JUSTIN T. ARBES,
and CHRISTA P. ZADO, *Administrative Patent Judges.*

ZADO, *Administrative Patent Judge*.

DECISION
Denying *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Overview

Amazon Web Services, Inc., Amazon.com, Inc., and VADATA, Inc. (collectively, "Petitioner")[1] filed a petition requesting *inter partes* review of claims 1, 3–9, and 11–19 (the "challenged claims") of U.S. Patent No. 7,149,867 B2 (Ex. 1001, "the '867 patent"). Paper 1 ("Pet."). Saint Regis Mohawk Tribe ("Patent Owner")[2] filed a Preliminary Response. Paper 20 ("Prelim. Resp.").

35 U.S.C. § 314 provides that an *inter partes* review must not be instituted "unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Upon considering the evidence and arguments presented, we determine the Petition does not demonstrate a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims.

Accordingly, we do not institute an *inter partes* review.

B. Related Proceeding

The parties advise that the '867 patent has been subject to, or relates to, the following district court proceeding: *SRC Labs and Saint Regis Mohawk Tribe v. Amazon Web Services, Inc., Amazon.com, Inc., and VADATA, Inc.*, No. 2:18-cv-00317 (W.D. Wash.). Pet. 2; Paper 17, 1.

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[1] Petitioner identifies only itself as real parties-in-interest to the Petition. Pet. 1–2.

[2] Patent Owner identifies only itself as a real party-in-interest to this proceeding. Paper 17, 1.

C. The '867 Patent

The '867 patent, titled "System and Method of Enhancing Efficiency and Utilization of Memory Bandwidth in Reconfigurable Hardware," generally relates to "implementing explicit memory hierarchies in reconfigurable processors that make efficient use of off-board, on-board, on-chip storage and available algorithm locality." Ex. 1001, 1:18–21.

The '867 patent explains that microprocessors "enjoyed annual performance gains averaging about 50% per year," wherein most of the gains were attributable to higher clock processor speeds, more memory bandwidth, and increasing utilization of instruction level parallelism ("ILP") at execution time. *Id.* at 1:26–30. However, as microprocessor speeds increased, challenges arose to designing memory hierarchies that could keep up. *Id.* at 1:31–33. The '867 patent identifies two measures of the gap between microprocessor and memory hierarchy speeds—bandwidth efficiency and bandwidth utilization. *Id.* at 1:35–37. Because potential performance gains from using a faster microprocessor were reduced or negated by corresponding drops in bandwidth efficiency and bandwidth utilization, significant effort had been spent, according to the '867 patent, on development of memory hierarchies that could maintain high bandwidth efficiency and utilization. *Id.* at 1:45–50.

The '867 explains that one approach to bridging the gap was the utilization of cache memories. *Id.* at 1:51–53. In designing cache memories, a number of considerations had to be taken into account. *Id.* at 59–60. For example, for programs that exhibit a high degree of spatial locality (i.e., it is likely that other data within the same cache line will be needed), wide cache lines are efficient. *Id.* at 1:64–2:4. However, for programs that have low levels of spatial locality, narrow cache lines are

more efficient. *Id.* at 2:4–7. The '867 patent provides additional examples of considerations in cache design. *Id.* at 2:14–3:40. The '867 patent states that the various considerations and tradeoffs made cache design challenging for a multipurpose computer that executes a wide variety of programs. *Id.* at 3:30–32. Cache designers tried to derive the program behavior of the "average" program, and optimize the cache for the "average" program. *Id.* at 3:32–36. As a result, the cache was sub-optimal for most programs, because most programs that actually run on the microprocessor are not "average." *Id.* at 3:36–39.

Because of the above-discussed issues, there was a growing need, according to the '867 patent, to develop improved memory hierarchies that limited overhead of a memory hierarchy without also reducing bandwidth efficiency and utilization. *Id.* at 3:57–60. To address the need, the '867 patent describes a system including a memory hierarchy and a reconfigurable processor that includes a data prefetch unit. *Id.* at 4:4–10, 5:60–62, 6:9–13, 7:34–48. "Unlike conventional static hardware platforms," the memory hierarchy is reconfigurable so that computational demands and memory bandwidth can be matched. *Id.* at 7:17–22. The '867 patent explains:

> An important feature of the present invention is that many types of data prefetch units can be defined so that the prefetch hardware can be configured to conform to the needs of the algorithms currently implemented by the computational logic. The specific characteristics of the prefetch can be matched with the needs of the computational logic and the format and location of data in the memory hierarchy.

Id. at 7:49–55. The '867 patent provides an example of configuring the data prefetch unit depending on the needs of the computational logic. For

example, Figures 9A and 9B show an external memory organized into a 128 byte (16 word) block structure that is optimized for stride 1 access of a cache. *Id.* at 7:56–59. However, the data prefetch unit can be configured to extract only 8 bytes of data in the memory block, discarding the remaining 120 bytes if only the 8 bytes are needed. *Id.* at 8:3–11. In another example relating to a computational intensive matrix multiplication problem, the '867 patent explains that

> On a conventional microprocessor with static execution resources, these loops [representing matrix multiplication] would be arranged to give stride-one data access where possible and also block or tile these uses to facilitate data cache hits on the B and A matrices, which are read many times. With the configurable memory hierarchy of the present invention, matrix B may be stored in on-board BRAM memory 307 and rows of matrix A in registers.

Id. at 10:33–40.

D. Asserted Grounds of Unpatentability

Petitioner challenges claims 1, 3–9, and 11–19 of the '867 patent on the following grounds. Pet. 3.

Reference	Ground	Claims
Lange[3]	§ 103(a)	1, 3–9, 11–19
Zhong[4]	§ 103(a)	1, 4, 6, 7, 9

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[3] Holger Lange & Andreas Koch, "Memory Access Schemes for Configurable Processors," *Field-Programmable Logic and Applications: The Roadmap to Reconfigurable Computing*, 10th International Conference, FPL 2000, Villach, Austria, 615–25 (Aug. 27–30, 2000) (Ex. 1003) ("Lange").

[4] Peixin Zhong & Margaret Martonosi, "Using Reconfigurable Hardware to Customize Memory Hierarchies," *High-Speed Computing, Digital Signal Processing, and Filtering Using Reconfigurable Logic*, SPIE—The International Society for Optical Engineering, Boston, MA, 237–248 (Nov.

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