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Serial No. 10/869,200

Application of: Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes

Filed: June 16, 2004

Art Unit: 2186

Examiner: Thomas, Shane M.

Attorney Docket No. SRC028

For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE

Confirmation No.: 5929

5825

Customer No.: **25235**

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1. Amendment in response to the Office Action dated October 19, 2005.

on 5 January 2006 (Date) 9 (No. of Pages (incl. Coversheet))

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Signature

Julie Lange
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Client Reference No. 80404.0033.001 Fax No. 719-448-5922

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200 Application of: Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes Filed: June 16, 2004 Art Unit: 2186 Examiner: Thomas, Shane M. Attorney Docket No. SRC028 For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	Confirmation No.: 5929 Customer No.: **25235**

AMENDMENT

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the office communication mailed October 19, 2005, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A reconfigurable processor that instantiates an algorithm as hardware comprising:

a first memory having a first characteristic memory bandwidth and/or memory utilization; and

a data prefetch unit coupled to the first memory, wherein the data prefetch unit retrieves data from a second memory of second characteristic memory bandwidth and/or memory utilization and place the retrieved data in the first memory and wherein at least the first memory and data prefetch unit are configured by a program.

2. (Cancelled)

3. (Cancelled)

4. (Previously Presented) The reconfigurable processor of claim 1, wherein the data prefetch unit is coupled to a memory controller that controls the transfer of the data between the second memory and the data prefetch unit.

5. (Previously Presented) The reconfigurable processor of claim 1, wherein the data prefetch unit receives processed data from on-processor memory and writes the processed data to an external off-processor memory.

6. (Original) The reconfigurable processor of claim 1, wherein the data prefetch unit comprises at least one register from the reconfigurable processor.

7. (Original) The reconfigurable processor of claim 1, wherein the data prefetch unit is disassembled when another program is executed on the reconfigurable processor.

8. (Previously Presented) The reconfigurable processor of claim 1 wherein said second memory comprises a processor memory and said data prefetch unit is operative to retrieve data from the processor memory.

9. (Original) The reconfigurable processor of claim 8 wherein said processor memory is a microprocessor memory.

10. (Original) The reconfigurable processor of claim 8 wherein said processor memory is a reconfigurable processor memory.

11. (Previously Presented) A reconfigurable hardware system, comprising:

a common memory; and

one or more reconfigurable processors that can instantiate an algorithm as hardware coupled to the common memory, wherein at least one of the reconfigurable processors includes a data prefetch unit to read and write data between the data prefetch unit and the common memory, and wherein the data prefetch unit is configured by a program executed on the system.

12. (Original) The reconfigurable hardware system of claim 11, comprising a memory controller coupled to the common memory and the data prefetch unit.

13. (Cancelled)

14. (Cancelled)

15. (Previously Presented) The reconfigurable hardware system of claim 11, wherein the at least one of the reconfigurable processors also includes a computational unit coupled to a data access unit.

16. (Original) The reconfigurable hardware system of claim 15, wherein the computational unit is supplied the data by the data access unit.

17. (Previously Presented) A method of transferring data comprising:

transferring data between a memory and a data prefetch unit in a reconfigurable processor; and

transferring the data between a computational unit and a data access unit, wherein the computational unit and the data access unit, and the data prefetch unit are configured by a program.

18. (Original) The method of claim 17, wherein the data is written to the memory, said method comprising:

transferring the data from the computational unit to the data access unit; and

writing the data to the memory from the data prefetch unit.

19. (Previously Presented) The method of claim 17, wherein the data is read from the memory, said method comprising:

transferring the data from the memory to the data prefetch unit; and

reading the data directly from the data prefetch unit to the computational unit through the data access unit.

20. (Original) The method of claim 19, wherein all the data transferred from the memory to the data prefetch unit is processed by the computational unit.

21. (Original) The method of claim 19, wherein the data is selected by the data prefetch unit based on an explicit request from the computational unit.

22. (Original) The method of claim 17, wherein the data transferred between the memory and the data prefetch unit is not a complete cache line.

23. (Original) The method of claim 17, wherein a memory controller coupled to the memory and the data prefetch unit, controls the transfer of the data between the memory and the data prefetch unit.

24. (Cancelled)

REMARKS/ARGUMENTS

Claims 1, 4-12, and 15-24 were presented for examination and are pending in this application. In an Official Office Action dated October 19, 2005, claims 1, 4-12, and 15-24 were rejected. Claim 24 is canceled without prejudice and no new claims are presently added. Claims 1, 4-12, and 15-23 remain pending. The Applicants thank the Examiner for his consideration and address the Examiner's comments concerning the claims pending in this application below.

Rejection of the Claims under 35 U.S.C. §102(e)

Claims 1, 3, 4, 7-10, and 12-18 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0084244 ("Paulraj"). Applicants respectfully traverse these rejections in light of the following remarks.

MPEP §2131 provides:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of Califomia*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir.1987). "The identical invention must be shown in as complete detail as contained in the claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Paulraj fails to disclose each and every limitation recited in the claims. The Examiner reasons that Paulraj discloses a system having a program that reconfigures computational units, data access units, and pre-fetch units. The Applicants disagree.

The Examiner's logic in making the above assertion is faulty. Assume for argument sake (as does the Examiner) that the computational unit is the element of the Paulraj system that executes and collects performance data regarding an

application to determine an optimal memory configuration. The program operating on the Paulraj system depicted in Figure 5 of Paulraj "configures" the collection process so as to ascertain information about a specific application. In this sense the Examiner uses the term configure to state that the program executed by the Paulraj system modifies, directs, and/or controls the collection means (the computational unit) to properly assess the target application so that the memory can be optimally configured.

The Examiner then extends this argument to the data access units and pre-fetch units. While such an extension is perhaps conceivable today given the present invention, it is not, nonetheless, disclosed by Paulraj. Nor is it reasonable to conclude that such an extension would be apparent to one skilled in the art at the time of the Applicants' invention.

As the Examiner points out, Paulraj discloses creating a "configuration vector containing data relating to the optimal configuration to the necessary instruction for programming the programmable memory module." Paulraj [0024]. Paulraj also discloses a reconfiguration module that uses the vector to configure the programmable memory module. Once the Paulraj system collects information about the target application and creates the configuration vector for optimal memory module configuration, "the configuration vector is then retrieved (step 212), used to program the FPGA module (step 214), and the application is executed with the optimal memory configuration for that application (step 216)." Paulraj [0026].

The "program" that the Examiner considers to configure the computational unit does not, according to Paulraj, "configure" the data access unit nor the pre-fetch unit. The Examiner restates that he considers the reconfiguration unit of Paulraj to be a data pre-fetch unit. The Examiner also correctly states that Paulraj discloses that the reconfiguration unit retrieves the configuration vector and sets up a programmable memory module. It is conceivable to argue that the "program" of Figure 5 of Paulraj configures the configuration vector to configure the

programmable memory module but once the vector is configured Paulraj discloses that the vector is simply retrieved and used by the reconfiguration unit to program the FPGA module. No configuration by the "program" of the reconfiguration module is even implied let alone disclosed. The Examiner expands Paulraj beyond the four corners of the document and what is literally presented so as to craft an argument for anticipation. Such a creation is not contemplated nor allowable under 35 U.S.C. § 102(e). As the rules governing anticipation are clear, the Applicants submit that Paulraj does not disclose a pre-fetch unit and a memory unit that is configured by a program as is recited in claim 1.

For at least the same aforementioned reasons, claims 11 and 17 are not anticipated by Paulraj. As Claims 4-10, 12, 15, 16, and 18-23 depend from claims 1, 11, or 17 and carry with them the limitations recited in those independent claims, claims 4-10, 12, 15, 16, and 18-23 are also not anticipated by Paulraj. The Applicants respectfully request withdrawal of the rejections and reconsideration of the claims.

In view of all of the above, the claims are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

No fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

January 5, 2006

Respectfully submitted,

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PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10869 200

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	4 minus 3 =	* 1
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
X$ 9=		OR	X$18=	72
X43=		OR	X86=	86
+145=		OR	+290=	—
TOTAL		OR	TOTAL	928

CLAIMS AS AMENDED - PART II

4-1-05

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 24	Minus	** 24	
Independent	* 4	Minus	*** 4	*
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 20	Minus	** 24	* —
Independent	* 4	Minus	*** 4	* —
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 19	Minus	** 24	*
Independent	* 3	Minus	*** 4	*
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 10/03)

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/869,200	06/16/2004	Daniel Poznanovic	SRC028	5929

25235 7590 03/23/2006

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER	
THOMAS, SHANE M	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/869,200	POZNANOVIC ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-12 and 15-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-12 and 15-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the response filed 1/5/2006. Claims 1,4-12, and 15-23 remain pending; claims 2,3,13,14, and 24 have been canceled.

Response to Arguments

Applicant's arguments filed 1/5/2006 have been fully considered but they are not persuasive for the reasons stated herein.

Applicant does not argue the rejections of claims 1-10 and appears to be arguing the rejection of claim 17 (page 7, ¶2, of the response):

"The Examiner then extends this argument to the data access units and prefetch units"

Examiner notes that only one --data access unit-- and one --prefetch unit-- are claimed.

"While such an extension is perhaps conceivable today given the present invention, it is not, nonetheless, disclosed by Paulraj. Nor is it reasonable to conclude that such an extension would be apparent to one skilled in the art at the time of Applicant's invention,"

The Examiner respectfully traverses and states that the Applicant has mischaracterized the prior rejection made by the Examiner with regard to claim 17. The following is a more detailed explanation of the Examiner's previous interpretation of the claims that clearly shows that each limitation of Applicant's clam 17 is anticipated by Paulraj or necessarily inherent, based on the teachings of Paulraj taken by one having ordinary skill in the art.

While the Examiner does state on page 5, lines 4-8, of the prior Office action (filed 10/19/2005) that the same program that "modifies, directs, and/or controls the collection means

(i.e. the computation unit) to properly assess the target application so that the memory can be optimally configured" is extended to the data access unit and the data prefetch unit, the Examiner was merely stating that different portions of the --program-- (*entire* figure 5 that is running on the system of Paulraj in order to perform the cache optimization when a new application is started) are responsible for --configuring-- the computational unit, the data access unit, and the data prefetch unit, so as to perform their unique procedures in order to optimize the reconfigurable cache.

The Examiner is considering the entirety of figure 5 of Paulraj to be an "access program." In other words, because Applicant does not specifically claim any limitations on specifics of the "program" [that does the configuring], the Examiner is broadly interpreting the term "program" to simply be a "collection of processes working together to accomplish a common task" - which is coherent with the IEEE definition of a "program" (refer to cited *IEEE 100*, page 874). Further, as it well known in the art, for a computer system to implement a method, computer instructions (either low-level or high-level) must be executed in order to perform the execution of the steps of the method. The --program--, as related to Paulraj figure 5, is being considered by the Examiner to be the steps required to implement a cache configured exclusively for a specific application, such as will be shown below.

The first portion (which is being considered by the Examiner to be performed by the --prefetch unit--) of the program of figure 5 of Paulraj (steps START through 200) determines (1) whether the operation of the program of figure 5 should run (i.e. when a new application is to be run that requires cache optimization - an inherent step since it can be argued that only if a new application is to be executed by the system of Paulraj will the operation of the program of figure

5 be executed. Refer to ¶21 of Paulraj which states that a wide range of applications can be used" and that the "cache architecture … reconfigure itself for optimal performance"; therefore, in order to be *reconfigured*, a first configuration must be present and if a change to that configuration is to occur, it is *necessarily inherent* that a new application is to be run to trigger the reconfiguration. Secondly, the first portion (prefetch unit) of the program of figure 5 of Paulraj (steps START through 200) determines (2) whether a vector is known for a given application that is to be executed on the system of Paulraj. It can be seen and argued herein, that in order to determine whether or not a given vector is known for a specific application, the first portion must perform a lookup or access of the memory comprising the vectors; therefore, it is *necessarily inherent* that the program *configure* the data prefetch unit to *access* and *index* the vector memory in order to ascertain whether or not the program should perform the steps of collecting and analyzing application data (steps 202-210 of figure 5). Without the program's configuration, the data prefetch unit would not know which application to search for when indexing the memory for the corresponding application vector. In other words, the program portion that is to perform the lookup of the vector *must* configure the data prefetch unit accordingly by sending the unique application identification and instructing the data prefetch unit to perform the search of the vector memory.

Further, if the memory vector is known (right path of step 200) the data prefetch unit is *configured* by the program as shown in figure 5, to retrieve the vector by accessing and reading the vector memory and subsequently, relaying the vector so the program can configure the FPGA to the vector's cache specification. Yet further, it can be seen in figure 5, that the data prefetch

unit is *configured* to not read from the vector memory if a determination is made that the application does not have a corresponding vector entry (left path of step 200).

Simply put, the data prefetch unit must be configured to (1) be able to access the vector memory when a new application is to be executed and (2) to respond with either a vector or a "vector not found" indication so that the program may either program the FPGA module (step 214) or begin the process of collecting performance data (step 204), respectively.

Similarly, the --data access unit-- (the unit that takes the vector data and accesses the vector memory to store the vector in an available location within the memory) is *configured* by the program of figure 5 to receive the vector created by the computational unit (in step 208) and then store the vector (step 210). It can be seen that the data access unit requires configuration, since if a vector is not created, a store by the data access unit would not have been required. Only when a new vector is created is the data access unit configured to execute a storage/write routine.

Finally, the "program" that is being executed by the --computational unit-- of Paulraj (steps 202-208) is shown as being only a *portion* of the *program* of figure 5 (i.e. the program that performs the *configurations* based on the decision block 200). The program of Paulraj configures the prefetch unit to check the vector data for a particulat application to be executed and retrieve the vector if available. If not available, the program configures the computational unit to collect and analyze application data and configures the data access unit to store the vector in the memory.

As argued herein, the prior art of Paulraj anticipates the claims as presented by the Applicant and interpreted by the Examiner. The Examiner does not "extend Paulraj beyond the

four corners of the document" since each limitation, as argued by the Applicant in the response filed 1/5/2006, is shown as being met in relation to figure 5 of Paulraj. Each of the computational unit, data access unit, and the prefetch unit (as defined by the Examiner in relation to Paulraj) are *configured* by the program of the steps of figure 5 in order to correctly implement the cache reconfiguration system of Paulraj. Without program configuration,

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,4-12, and 15-23, are rejected under 35 U.S.C. 102(e) as being anticipated by Paulraj (U.S. Patent Application Publication No. 2003/0084244).

As per claim 1, Paulraj shows a reconfigurable processor in figure 6 and a first memory (L1) having a first characteristc memory utilization and a second memory (L2) having a second characteristic memory utilization. It is well known in the art that L1 caches have a higher utilziation rate than a lower-level cache such as L2. Paulraj teaches in ¶1 that upon a command from a processor, a search for the requested data is begines with the highest level cache (L1) and [if a miss occurs] continues next to the next level cache (L2). Thus it is inherent that the memory utilziation characteristc of the L1 cache of the reconfigurable processor 110 in figure 6 is greater

than the memory utilziation characteristic of the L2 cache (and likewise for the L3 cache) as the L2 cache would only be utilzied when a miss to the L1 cache occurred. In other words, the reconfigurable processor *always* utilizes the L1 cache for a memory access and the *only* utilzies the L2 cache for requested data when the data is not in the L1 cache. Therefore, the cache utilziation characteristics of the --first memory-- and the --second memory-- are different.

Paulraj further teaches a functional unit 102 that executes applications using the memories L1 and L2 (paragraph 9). As is known in the art, a cache memory controller is often used to access and move data between a memory hierarchy. The Examiner is considering a data prefetch unit to be the logic assocatied with the moving, and only the moving, of data between the first and second memories (L1 and L2) since Paulraj shows a connection between the levels of cache in figure 6. This logic as well as the first and second memory types (L1 and L2) are configued by a program – refer to paragraphs 23-24. The data prefetch unit as defined by the Examiner must be configued as well by the program when moving data since the cache line size and blocking factor can change, so different amounts of data can be exchanged for the same access when different programs run.

The reconfigurable processor of Paulraj has the ability to collect memory usage statistics for a particular application and based on those statistics, create a configuration vector as taught in ¶¶23-24. This vector allows the programmable memory module 104 of Paulraj to be reconfigured to the most optimal memory configuration for that specific software program (¶26). As defined by the Applicant in ¶55 of the originally filed specification, a software program or application is a collection of "algorithms"; therefore, the configuration vector for a particular software program allows the system of Paulraj to instantiate a software program as hardware

since the configuration vector represents optimal configuration of the hardware (programmable memory module 104 - element 112 of figure 6).

As per claim 4, Paulraj teaches that a load/store unit is used to access the caches (L1-L3) in order to determine if cache data is present in the cache hierarchy (paragraph 6). Since the functional unit 102 (figure 6) is responsible for accessing the programmable memory unit 104, the Examiner is therefore considering the load/store unit logic of the programmable memory unit that is responsible for for accessing the L1 and L2 caches (first and second memory types) to be a memory controller. It can be seen that the memory controller, as defined by the Examiner, controls the transfer of data between the memory (assuming second memory L2) and the data prefetch unit, since the memory controller (load/store unit logic) is responsible for retrieving the data from the cache if a hit occurs (paragraph 4).

As per claim 5, as taught in paragraph 1, an external memory (element 18, figure 1) is generaly coupled to a microprocessor and holds data to be used by the microcontroller during program execution. The Examiner is considering the process of writing data back to the external memory from the FPGA memory 104 containing the caches (on-board memory), such as during a write-back scheme as known in the art, to be performed by the data prefetch unit portion of the functional logic as defined above by the Examiner. The data prefetch logic, as defined above, is responsible for all of the transfer of data into, out of, and between the FPGA memory 104.

As per claim 6, the Examiner is regarding a --register-- in its broadest reasonable sense and it thus considering it be to be a unit of logic. Therefore, the portion of the function logic that is responsible for the movement of data (as defined above to be the data prefetch unit) is being considered by the Examiner as containing a --register-- portion of the reconfigurable processor

since, for instance, the blocking factor and line size of the programmable memory 112 can change, a --register-- or portion of the reconfigurable processor must be set in order to indicate the currnet line size and blocking factor when a given application is being run on the reconfigurable processor at a given point in time. Refer to paragraph 23.

As per claim 7, the Examiner is considering the process of --disassembling the data prefetch unit-- as modifying the data prefetch unit logic of the fucntion logic 102 every time the program being executed by the reconfigurable processor changes. It can be seen that the data prefetch unit changes during these intervals since the cache line size, blocking factor, and associativity of the FPGA changes when optimal for the next program to be executed (refer to paragraph 23). Thus it can be seen that the data prefetch unit logic is --disassembled-- when another program is executed by the reconfigurable processor of Paulraj.

As per claim 8, as can be seen that the FPGA memory 112, that comprises the first and second memories (L1 and L2) and which is accessed by the data prefetch unit of the functional unit 102 as discussed above, is a --processor memory-- (part of cpu 110). It can also be seen that the --second memory-- (L2) is also a --processor memory-- since it is contained within reconfigurable processor 110. Therefore, since the data pretech unit can access the L2 cache as discussed above in the rejection of claim 1, the data prefetch unit can retrive data from the L2 portion of --processor memory--112.

As per claim 9, as shown in figure 1 and taught in paragraph 1 of Paulraj, the system 10 is actually a microprocessor, which contains a memory controller 14. The main difference between the prior art of figure 1 and the invention of Paulraj in figure 6 is that the memroy hierarchy is configurable and accessed by a fucntional unit in lieu of a separate memory

controller logic (paragraph 9). Therefore, since the memory controller logic for accessing the cache hierarchy is still contained within cpu 110 of figure 6, it can be seen that the cpu 110 is actually a microprocessor. It follows that the --processor memory-- 112 is therefore a --microprocessor memory--.

As per claim 10, since the cpu 110 of figure 6 is a reconfigurable processer (able to reconfigure its memory heirarchy to match the needs of the application it is currently running), it can be seen that the cpu memory 112 is a reconfigurable processor memory.

As per claim 11, Paulraj depicts a reconfigurable hardware system in figure 6. Paulraj further teaches in paragraph 26 that when a particular application is to be run by the reconfigrable processor 110, a configuration vector is retrieved to program the programmable memory 112 (figure 6). As shown in figure 6, the step of accesing the configuration vector is executed outside of the reconfigurable processor 110. Therefore, the Examiner is considering the memory that contains the configuration vectors to be a--common memory-- and a data prefetch unit (reconfiguration unit 106 executing on the reconfigurable processor 110) accessing the common memory in order to determine how to program the memory 112 (paragraph 29). The data prefetch unit 106 is --configured-- by an application to be excuted on the sysem 110 since when a new application is to be executed, the data prefetch unit is called upon (or configured) to access the configuration vector for the particular application.

The reconfigurable processor of Paulraj has the ability to collect memory usage statistics for a particular application and based on those statistics, create a configuration vector as taught in ¶¶23-24. This vector allows the programmable memory module 104 of Paulraj to be reconfigured to the most optimal memory configuration for that specific software program (¶26).

As defined by the Applicant in ¶55 of the originally filed specification, a software program or application is a collection of "algorithms"; therefore, the configuration vector for a particular software program allows the system of Paulraj to instantiate a software program as hardware since the configuration vector represents optimal configuration of the hardware (programmable memory module 104 - element 112 of figure 6).

As per claim 12, the Examiner is considering a --memory controller-- to be the system portion utilized when creating a new configuration vector for an application. Such a process occurs in figure 5 and taught in paragraghs 23-25 of Paulraj. When a new configuration vector is created by analizing performance information that has been collected for the application. The Examiner is thereby considering the --memory controller-- to be the element of the reconfigurable hardware system that is associated with storing the new configuration vector into the common memory so that the vector can be accessed later when the same application is run again.

As per claim 15, the Examiner is considering the reconfiguration module 106 of the reconfigurable processsor 110, as comprising two distinct elements: a --computational unit-- and a --data access unit--. The data access unit is the element that is responsible for accessing the configuration vector as taught in paragraph 29 of Paulraj; or in other words, the Examiner is considering the --data access unit-- to be the same as the --memory controler-- defined in the rejection of claim 12. The Examiner is further considering the --computational unit-- of the rconfiguration module 106 to be the element that sets up the programmable memory module 104 using the configuration vector that was accessed by the --data access unit-- (paragraph 29).

As per claim 16, as taught by Paulraj in paragraph 29, the --data access unit-- supplies the configuration vector to the --computational unit-- in order to set up the programmable memory 104 as required by the application to be run on the reconfurable processor 110.

As per claim 17, the Examiner is considering a --data prefetch unit-- to be the reconfiguration unit 106 of reconfigurable processor 110 (figure 6). As taught in paragraph 26 and 29 of Paulraj, the --data prefetch unit-- accesses a memory in order to determine if a configuration vector is known for a given application, and if so, the vector is retrieved (from the memory). If this --data-- (configuration vector) is not known then a simulation is performed with the application in order to collect performance information. The Examiner is considering the element that executes and collects the performance data as being a --computational unit-- and the element of Paulraj that stores the configuration vector, once determined, to be a --data access unit-- since it stores the vector into the --memory-- from which it can be later retrieved (step 212 of figure 5).

All of the computational, data access, and data prefetch units are configured by a program, as immediately discussed. As defined by the Examiner, the "computational unit" of Paulraj is being considered to be the element of the system of Paulraj that executes and collects the performance data regarding how a specific application utilizes memory in order to determine an optimal memory configuration as discusses in ¶27. Figure 5 of Paulraj shows a method for creating a configuration vector by using the --computational unit-- in steps 204-206. The Examiner is considering the inherent *program* that is being executed in order to perform the steps of figure 5 to be the *program* that configures the computational unit. Therefore, it can be seen that Paulraj suggests configuring the computational unit by a program. The *program* of

figure 5 *configures* the computational unit to collect data for a specific application's memory usage statistics in order to create a configuration vector that allows the system of Paulraj to optimally reconfigure the programmable memory module 104. Thus the computational unit can be configured to collect memory usage statistics for a plurality of applications that are to be executed by the reconfigurable processor 100 of Paulraj (¶23).

The same reasoning applies to the data access and data prefetch units. The *program* that is executing the steps of figure 5 (i.e. running on the system of Paulraj that implements the method) *configures* the data access unit to retrieve/store a configuration vector (step 212) based on if a new configuration vector had to be created and further *configures* the data prefetch unit to search for a configuration vector and retrieve that vector if found (steps 200 and 212).

In order to prevent repetition, a full discussion of the rejection of claim 17 is found above in response to the Applicant's arguments filed in the response.

As per claim 18, the --data-- (configuration vector) is transferred from the --computational unit-- to the --data access unit-- when the configuration unit has created a configuration vector (step 208 of figure 5). The --data-- is written to the memory --from-- the --data prefetch unit-- since the data prefetch unit (reconfiguration unit 106) is the element that executed the beginning of the configuration vector creation process (step 200 of figure 5). Refer to paragraph 26. Thus the Examiner is considering the data as being written --from-- the data prefetch unit.

As per claim 19, as taught in paragraph 26, if the configuration vector is known, the vector is retrieved from the memory to the data prefetch unit (reconfiguration unit 106). The data is read directly from the data prefetch unit when a request to create a configuration vector is

made for a new application as shown in figure 6 since the data prefetch unit is responsible for being the vector creation process. The data is directed from the data prefetch unit (reconfigure logic) to be read from the memory by the data access unit to the computational unit where it is processed to produce a configuration vector.

As per claim 20, as stated above, the configuration vector (--data--) is created by the computational unit via acquired simulation data. The configuration vector is the resultant product that is transferred from the memory to the data prefect unit when it is determined that the configuration vector for the application is available (paragraph 26). Thus --all-- of the data that is transferred is processed by the computational unit (albeit before the transfer occurs) since the data prefetch unit required the entire configuration vector in order to set up the programmable memory 112.

As per claim 21, Paulraj shows in paragraph 26 that an explicit request for the configuration vector for the current application results in the data (if it exists) selected for the optimal configuration of the programmable memory 112 for that application.

As per claim 22, the Examiner is not considering the data (configuration vector) to be the size of a complete cache line since the data is used to create a cache hierarchy. In other words, the caches (L1-L3) of the programmable memory 112 are not programmed when the data is transferred from the memory to the data prefetch unit; therefore, the data cannot be a complete cache line.

As per claim 23, since the Examiner defined the portion of the reconfiguration unit that accesses the configuration file (data) from the memory, the Examiner is defining the logic that controls the actual transfer of that data to the data prefetch unit (portion of the reconfiguration

unit that executes the fetch of the configuration vector and then programs the programmable memory 112) to be a --memory controller--. Thus the data access unit determines whether a configuration vector exists for an application and if so, the memory controller sends that data to the data prefetch unit.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

HONG CHONG KIM
EXAMINER

Notice of References Cited	Application/Control No. 10/869,200	Applicant(s)/Patent Under Reexamination POZNANOVIC ET AL.	
	Examiner Shane M. Thomas	Art Unit 2186	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Standards Information Network, 2000, pp. 874.
	V	
	W	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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modules may operate in systems complying with other profiles if the system meets Profile A physical requirements and if modules support a compatible transaction set when sharing data. (C/BA) 896.2-1991w

Profile A system The assembly of hardware elements made up of, at a minimum, the Profile A compliant backplane and subrack, power supply, fans, etc. Modules complying with other profiles may operate compatibly with Profile A systems and modules if they meet Profile A physical requirements and if their features constitute an identity or a superset of those implemented in a Profile A system as per Tables 59 and 60. (C/BA) 896.2-1991w

Profile B module The assembled plug-in unit, containing a Futurebus+ interface and one or two nodes complying with Profile B, which is inserted into a compatible Futurebus+ slot. Profile B modules may operate compatibly in systems complying with other profiles if the system meets Profile B mechanical requirements, and if non-Profile B nodes properly subset their transaction set when addressing Profile B modules, as specified in this profile. (C/BA) 896.2-1991w

Profile B system The assembly of hardware elements made up of, at a minimum, the Profile B compliant backplane and card cage, power supply, air mover, and a bridge to the rest of the system or to another bus. Modules complying with other profiles may operate compatibly with Profile B systems and modules if they meet Profile B mechanical requirements, and if their features constitute an identity or a superset of those mandated in this profile. (C/BA) 896.2-1991w

profile dispersion (A) (fiber optics) In an optical waveguide, that dispersion attributable to the variation of refractive index contrast with wavelength, where contrast refers to the difference between the maximum refractive index in the core and the refractive index of the homogeneous cladding. Profile dispersion is usually characterized by the profile dispersion parameter, defined by the following entry. **(B) (fiber optics)** In an optical waveguide, that dispersion attributable to the variation of refractive index profile with wavelength. The profile variation has two contributors:

1) variation in refractive index contrast, and
2) variation in profile parameter.

See also: distortion; refractive index profile; dispersion. (Std100) 812-1984

profile dispersion parameter (fiber optics)

$$P(\lambda) = \frac{n_1}{N_1}\frac{\lambda}{\Delta}\frac{d\Delta}{d\lambda}$$

where n_1, N_1 are, respectively, the refractive and group indices of the core, and

$$n_1\sqrt{1-2\Delta}$$

is the refractive index of the homogeneous cladding, $N_1 = n_1 - \lambda(dn_1/d\lambda)$, and Δ is the refractive index constant. Sometimes it is defined with the factor (-2) in the numerator. *See also:* dispersion. (Std100) 812-1984w

Profile F module The assembled unit, containing a Futurebus+ interface and one or two nodes complying with Profile F, which is inserted into a compatible Futurebus+ slot. Profile F modules may operate compatibly in systems complying with other profiles if the system meets Profile F mechanical requirements, and if non-Profile F nodes properly subset their transaction set when addressing Profile F modules, as specified in this profile. (C/BA) 896.2-1991w

Profile F system The assembly of hardware elements made up of, at a minimum, the Profile F compliant backplane and card cage, power supply, and an air mover. Modules complying with other profiles may operate compatibly with Profile F systems and modules if they meet Profile F mechanical requirements, and if their features constitute an identity or a superset of those mandated in this profile. (C/BA) 896.2-1991w

profile parameter (fiber optics) The shape-defining parameter, g, for a power-law index profile. *See also:* refractive index profile; power-law index profile. (Std100) 812-1984w

Profile S module The assembled unit, containing a Futurebus+ interface and one or two nodes complying with Profile S, which is inserted into a compatible Futurebus+ slot. (C/BA) 896.10-1997

Profile S system The assembly of hardware elements made up of, at a minimum, the Profile S compliant backplane, card cage, and a power supply. Modules complying with other profiles may operate compatibly with Profile S systems and modules if they meet Profile S mechanical requirements, and if their features constitute an identity or a superset of those mandated in this profile. (C/BA) 896.10-1997

prognosis (test, measurement, and diagnostic equipment) The use of test data in the evaluation of a system or equipment for potential or impending malfunctions. (MIL) [2]

program (1) (general) A sequence of signals transmitted for entertainment or information. (SP) 151-1965w

(2) (A) (electronic computation) A plan for solving a problem. **(B) (electronic computation)** Loosely, a routine. **(C) (electronic computation)** To devise a plan for solving a problem. **(D) (electronic computation)** Loosely, to write a routine. *See also:* communication; source program; object program; target program; computer program; programmed acceleration. (ED/ED/C) 581-1978, 641-1987, 162-1963

(3) (telephone switching systems) A set of instructions arranged in a predetermined sequence to direct the performance of a planned action or actions. (COM) 312-1977w

(4) (semiconductor memory) The inputs that when true enable programming, or writing into, a programmable read only memory (PROM). (TT/C) 662-1980s

(5) (software) To write a computer program. (C) 610.12-1990

(6) A prepared sequence of instructions to the system to accomplish a defined task. The term *program* in POSIX.2 encompasses applications written in the Shell Command Language, complex utility input languages (for example, awk, lex, sed, etc.), and high-level languages. (C/PA) 9945-2-1993

(7) The process of incorporating digital data onto an integrated circuit. (C) 610.10-1994w

(8) A collection of processes working together to accomplish a common task. (C/MM) 855-1990

(9) The operation of injecting electrons onto the floating gate of the memory cell. (ED) 1005-1998

(10) A set of partitions, which can execute in parallel with one another, possibly in a separate address space and possibly on a separate computer. (C) 1003.5-1999

program amplifier *See:* line amplifier.

program architecture (software) The structure and relationships among the components of a computer program. The program architecture may also include the program's interface with its operational environment. *See also:* computer program; component. (C/SE) 729-1983s

program attention key *See:* attention key.

program block (software) In problem-oriented languages, a computer program subdivision that serves to group related statements, delimit routines, specify storage allocation, delineate the applicability of labels, or segment paths of the computer program for other purposes. *See also:* computer program; label; segment; routine. (C/SE) 729-1983s

program correctness *See:* correctness.

program counter (1) A register in the processing unit that contains the address of the next instruction to be executed. *Synonym:* instruction address register. (C) 610.10-1994w

(2) *See also:* instruction counter. (C) 610.12-1990

program data set A data set in which user programs are stored. (C) 610.5-1990w

program definition language *See:* program design language.

program design language (1) (software) A specification language with special constructs and, sometimes, verification

Index of Claims

Application No.	Applicant(s)	
10/869,200	POZNANOVIC ET AL.	
Examiner	**Art Unit**	
Shane M. Thomas	2186	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Claim		Date								
Final	Original	1/5/05	7/6/05	10/15/05	3/17/06					
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25235 7590 05/12/2006

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ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 05/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Interview Summary	Application No.	Applicant(s)	
	10/869,200	POZNANOVIC ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Shane M. Thomas*. (3)_____.

(2) *Mike C. Martensen (Reg. No. 46,901)*. (4)_____.

Date of Interview: *08 May 2006*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1,11 and 17*.

Identification of prior art discussed: *Paulraj (US Pre-Grant Pub 2003/0084244)* .

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *See Continuation Sheet*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: Representative for Applicant, Mr. Martensen, initiated the interview in order to discuss the claims' rejections and for clarification regarding how the Paulraj reference teaches the claim limitations as interpreted by the Examiner. The Examiner explained how the entirety of figure 5 of Paulraj was being considered by the Examiner to be a --program--, as defined by the IEEE definition of a --program--, and how figure 5 was being used to teach the claim limitations of claim 17. Rep. Martensen agreed that the claims could be reworded in order to more clearly convey the subject matter which Applicant considered his invention and to draft such limitations in a forth-coming amendment.

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Client Matter No. 80404.0033.001
EFS-Web

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200 Application of: Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes Filed: June 16, 2004 Attorney Docket No. SRC028 For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	Confirmation No.: 5929 Art Unit: 2186 Examiner: THOMAS, Shane M. Customer No.: **25235**

AMENDMENT AND RESPONSE PURSUANT TO FINAL OFFICE ACTION DATED MARCH 23, 2006

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the final office communication mailed March 23, 2006, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A reconfigurable processor that instantiates an algorithm as hardware comprising:

a first memory having a first characteristic memory bandwidth and/or memory utilization; and

a data prefetch unit coupled to the first memory, wherein the data prefetch unit retrieves only computational data required by the algorithm from a second memory of second characteristic memory bandwidth and/or memory utilization and places the retrieved computational data in the first memory wherein the data prefetch unit operates independent of and in parallel with logic blocks using the computational data, and wherein at least the first memory and data prefetch unit are configured ~~by a program~~ to conform to needs of the algorithm, and the data prefetch unit is configured to match format and location of data in the second memory.

2. (Cancelled)

3. (Cancelled)

4. (Currently Amended) The reconfigurable processor of claim 1, wherein the data prefetch unit is coupled to a memory controller that controls the transfer of the data between the second memory and the data prefetch unit and transmits only portions of data desired by the data prefetch unit and discards other portions of data prior to transmission of the data to the data prefetch unit.

5. (Previously Presented) The reconfigurable processor of claim 1, wherein the data prefetch unit receives processed data from on-processor memory and writes the processed data to an external off-processor memory.

6. (Original) The reconfigurable processor of claim 1, wherein the data prefetch unit comprises at least one register from the reconfigurable processor.

7. (Original) The reconfigurable processor of claim 1, wherein the data prefetch unit is disassembled when another program is executed on the reconfigurable processor.

8. (Previously Presented) The reconfigurable processor of claim 1 wherein said second memory comprises a processor memory and said data prefetch unit is operative to retrieve data from the processor memory.

9. (Original) The reconfigurable processor of claim 8 wherein said processor memory is a microprocessor memory.

10. (Original) The reconfigurable processor of claim 8 wherein said processor memory is a reconfigurable processor memory.

11. (Currently Amended) A reconfigurable hardware system, comprising:

a common memory; and

one or more reconfigurable processors that can instantiate an algorithm as hardware coupled to the common memory, wherein at least one of the reconfigurable processors includes a data prefetch unit to read and write only data required for computations by the algorithm between the data prefetch unit and the common memory wherein the data prefetch unit operates independent

of and in parallel with logic blocks using the computational data., and wherein the data prefetch unit is configured ~~by a program executed on the system~~ to conform to needs of the algorithm and match format and location of data in the common memory.

12. (Currently Amended) The reconfigurable hardware system of claim 11, comprising a memory controller coupled to the common memory and the data prefetch unit that transmits to the prefetch unit only data desired by the data prefetch unit as required by the algorithm.

13. (Cancelled)

14. (Cancelled)

15. (Previously Presented) The reconfigurable hardware system of claim 11, wherein the at least one of the reconfigurable processors also includes a computational unit coupled to a data access unit.

16. (Original) The reconfigurable hardware system of claim 15, wherein the computational unit is supplied the data by the data access unit.

17. (Currently Amended) A method of transferring data comprising:

transferring data between a memory and a data prefetch unit in a reconfigurable processor; and

transferring the data between a computational unit and a data access unit, wherein the computational unit and the data access unit, and the data prefetch unit are configured ~~by a program~~ to conform to needs of an algorithm implemented on the computational unit and transfer only data necessary for computations by the computational unit, and wherein the prefetch unit operates independent of and in parallel with the computational unit.

18. (Original) The method of claim 17, wherein the data is written to the memory, said method comprising:

transferring the data from the computational unit to the data access unit; and

writing the data to the memory from the data prefetch unit.

19. (Currently Amended) The method of claim 17, wherein the data is read from the memory, said method comprising:

transferring only the data desired by the data prefetch unit as required by the computational unit from the memory to the data prefetch unit; and

reading the data directly from the data prefetch unit to the computational unit through the data access unit.

20. (Original) The method of claim 19, wherein all the data transferred from the memory to the data prefetch unit is processed by the computational unit.

21. (Original) The method of claim 19, wherein the data is selected by the data prefetch unit based on an explicit request from the computational unit.

22. (Original) The method of claim 17, wherein the data transferred between the memory and the data prefetch unit is not a complete cache line.

23. (Original) The method of claim 17, wherein a memory controller coupled to the memory and the data prefetch unit, controls the transfer of the data between the memory and the data prefetch unit.

24. (Cancelled)

REMARKS/ARGUMENTS

Claims 1, 4-12 and 15-23 were presented for examination and are pending in this application. In an Official Final Office Action dated March 23, 2006, claims 1, 4-12 and 15-23 were rejected. The Applicants thank the Examiner for his consideration and address the Examiner's comments concerning the claims pending in this application below.

Rejection of the Claims under 35 U.S.C. §102(e)

Claims 1, 4-12 and 15-23 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0084244 ("Paulraj"). In light of the aforementioned amendments, the Applicants traverse these rejections and request reconsideration. Independent claims 1, 11 and 17 have been amended to further describe the nature of the data retrieved by the prefetch unit. Support for the amendments can be found in the specification beginning generally at paragraph [0055] and continuing to paragraph [0064]. Paulraj discloses a system for cache optimization that configures a computational unit for a particular application. The Applicants' invention claims a system having a prefetch unit that retrieves computational data needed to complete the algorithm instantiated on the reconfigurable processor during processing. The retrieval of this data is done such that only data necessary for computations by the computational unit is accomplished in a manner so that the prefetch unit operates independent of and in parallel with the computational unit.

In view of all of the above, the claims are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the

Examiner is requested to contact Applicants' attorney at the telephone number listed below.

No fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

May 16, 2006

Michael C. Martensen, No. 46,901
Hogan & Hartson LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5910 Tel
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Electronic Acknowledgement Receipt

EFS ID:	1049173
Application Number:	10869200
Confirmation Number:	5929
Title of Invention:	System and method of enhancing efficiency and utilization of memory bandwidth in reconfigurable hardware
First Named Inventor:	Daniel Poznanovic
Customer Number:	25235
Filer:	Michael Christian Martensen/Julie Lange
Filer Authorized By:	Michael Christian Martensen
Attorney Docket Number:	SRC028
Receipt Date:	16-MAY-2006
Filing Date:	16-JUN-2004
Time Stamp:	18:15:36
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1		DOC077.PDF	51635	yes	7

	Multipart Description		
	Doc Desc	**Start**	**End**
	Amendment After Final	1	1
	Amendment Copy Claims/Response to Suggested Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	7
Warnings:			
Information:			
	Total Files Size (in bytes):	51635	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

10/869200

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number 10/869200

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							
SEARCH FEE (37 CFR 1.16(k), (l), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	x =		OR	x =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	x =			x =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 19	Minus	** 19	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/869,200	06/16/2004	Daniel Poznanovic	SRC028	5929

25235 7590 05/24/2006

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 05/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/869,200	**Applicant(s)** POZNANOVIC ET AL.	
	Examiner Shane M. Thomas	**Art Unit** 2186	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 16 May 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet*. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1,4-12 and 15-25*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
    _____
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

Continuation of 3. NOTE: Independent claims 1,11, and 17, all contain new limitations that were not previously considered by the Examiner; thus, a further search and additional consideration is required..

HONG CHONG KIM
PRIMARY EXAMINER

Do Not Enter.

SMT 5/18/06.

Client Matter No. 80404.0033.001
EFS-Web

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200 Application of: Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes Filed: June 16, 2004 Attorney Docket No. SRC028 For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	Confirmation No.: 5929 Art Unit: 2186 Examiner: THOMAS, Shane M. Customer No.: **25235**

AMENDMENT AND RESPONSE PURSUANT TO FINAL OFFICE ACTION DATED MARCH 23, 2006

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the final office communication mailed March 23, 2006, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

PTO/SB/30 (04-05)
Approved for use through 07/31/2006. OMB 0651-0031
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/869,200
Filing Date	June 16, 2004
First Named Inventor	Daniel Poznanovic et al.
Group Art Unit	2186
Examiner Name	THOMAS, Shane M.
Attorney Docket Number	SRC028

This is a Request for Continued Examination (RCE) under 37 C.F.R. 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 C.F.R. 1.114. Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).
   - a. ☒ Previously submitted. If a final Office Action is outstanding, any amendments filed after the final Office Action may be considered as a submission even if this box is not checked.
     - i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - ii. ☐ Other _____
   - b. ☐ Enclosed
     - i. ☐ Amendment/Reply
     - ii. ☐ Affidavit(s)/Declaration(s)
     - iii. ☐ Information Disclosure Statement (IDS)
     - iv. ☐ Other _____
2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. 1.17(i) **required**)
   - b. ☐ Other
3. Fees. The RCE fee under 37 C.F.R. 1.17(e) is required by 37 C.F.R. 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 50-1123.
     - i. ☒ RCE fee required under 37 C.F.R 1.17(e)
     - ii. ☐ Extension of time fee (37 C.F.R 1.136 and 1.17)
     - iii. ☒ Other: Charge any additional fees or credit any overpayments **for this filing**
   - b. ☐ Check in the amount of $ enclosed
   - c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Michael C. Martensen	*Registration No. (Attorney/Agent)*	46,901
Signature	/Michael C. Martensen/	*Date*	6/14/06

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Name (Print/Type)	Julie Lange		
Signature	/Julie Lange/	*Date*	15 June 2006

Electronic Patent Application Fee Transmittal

Application Number:	10869200
Filing Date:	16-Jun-2004
Title of Invention:	System and method of enhancing efficiency and utilization of memory bandwidth in reconfigurable hardware
First Named Inventor:	Daniel Poznanovic
Filer:	Michael Christian Martensen
Attorney Docket Number:	SRC028

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	790	790
		Total in USD ($)		**790**

Electronic Acknowledgement Receipt	
EFS ID:	1079525
Application Number:	10869200
Confirmation Number:	5929
Title of Invention:	System and method of enhancing efficiency and utilization of memory bandwidth in reconfigurable hardware
First Named Inventor:	Daniel Poznanovic
Customer Number:	25235
Filer:	Michael Christian Martensen
Filer Authorized By:	
Attorney Docket Number:	SRC028
Receipt Date:	15-JUN-2006
Filing Date:	16-JUN-2004
Time Stamp:	10:54:20
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$790
RAM confirmation Number	626
Deposit Account	501123
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1	Request for Continued Examination (RCE)	DOC182.PDF	28871	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	8207	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	37078		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	2258	711/154.ccls.	US-PGPUB; USPAT	OR	ON	2006/07/24 12:14
L3	11	2 and memory and ((reconfigurable reconfigurability configurable configurability) near5 (processor microprocessor CPU controller cache)) and (pre-fetch$3 prefetch$3)	US-PGPUB; USPAT	OR	ON	2006/07/24 12:18
S165	1675	reconfigur$4 near2 processor	US-PGPUB; USPAT	OR	ON	2006/07/24 10:27
S166	138	S165 and "711".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 10:20
S167	1854	reconfigur$4 near2 (processor microprocessor micro-processor)	US-PGPUB; USPAT	OR	ON	2006/07/24 10:28
S168	144	S167 and "711".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 10:28
S169	3355	(reconfigur$4 adaptive) near2 (processor microprocessor micro-processor)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:34
S170	156	S169 and "711".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 10:40
S171	6	"869200".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 10:58
S172	4	"021492".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:20
S173	2217	711/170.ccls.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:20
S174	5	S173 and (algorithm application task instructions computation arithmetic program) near3 (reconfigur$5) and (prefetch$3 pre-fetch$3)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:22
S175	28	S173 and (algorithm application task instructions computation arithmetic program) same (reconfigur$5) and (prefetch$3 pre-fetch$3)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:30
S176	7	712/207.ccls. and prefetch$3 near5 computation$2	US-PGPUB; USPAT	OR	ON	2006/07/24 11:31
S177	100	712/207.ccls. and prefetch$3 with (configur$5 reconfig$5)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:32
S178	81	712/207.ccls. and prefetch$3 with (configur$5 reconfig$5) same (process algorithm program instructions calculation application)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:33

EAST Search History

S179	3	712/207.ccls. and prefetch$3 with (configur$5 reconfig$5) same (process algorithm program instructions calculation application) same parallel	US-PGPUB; USPAT	OR	ON	2006/07/24 11:33
S180	1118	(configurable) near2 (processor microprocessor micro-processor)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:35
S181	977	S180 not S169	US-PGPUB; USPAT	OR	ON	2006/07/24 11:35
S182	58	S181 and "711".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:35
S183	161	reconfigur$3 adj (processor micro-processor CPU processor)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S184	190	reconfigur$3 adj (processor micro-processor CPU microprocessor)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S185	8	reconfigur$3 adj (processor micro-processor CPU microprocessor) and "711".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S186	0	reconfigur$3 adj (processor micro-processor CPU microprocessor) and prefetch	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S187	13	711/170-173.ccls. and dynamic near3 logic	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S188	999	smc.as.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S189	0	smc.as. and "711".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S190	0	smc.as. and "712".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S191	0	(smc and computers) .as. and "712".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S192	0	(smc and computers) .as.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S193	0	(smc and computers).as.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S194	16	(src and computers).as.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S195	114	711/170.ccls. and dynamic$4 near3 configur$5	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S196	6	711/170.ccls. and dynamic$4 near3 configur$5 with cache	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S197	438	reconfigurable adj processor	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46

EAST Search History

S198	6	"206189".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S199	1	"5024031".pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S200	6	"869200".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S201	2217	711/170.ccls.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S202	598	711/170.ccls. and (reconfigur$5 rearrang$4 application adj specific)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S203	126	711/170.ccls. and matrix	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S204	81	711/170.ccls. and fpga	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S205	214	712/15.ccls.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S206	378	711/170.ccls. and (application near2 specific application-specific)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S207	438	reconfigurable adj processor	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S208	298	S207 and fpga	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S209	12	S208 and memory with reconfiguring	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S210	57	711/170.ccls. and ((reconfigur$5 rearrang$4) and application adj specific)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S211	81	711/170.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S212	314	711/170.ccls. and reconfig$7	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S213	1	"6779131".pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S214	1	("6779131").URPN.	USPAT	OR	ON	2006/07/24 11:46
S215	9	("5892896" | "6060339" | "6081463" | "6154851" | "6204562" | "6363502" | "6405324" | "6483755" | "6530005").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:46
S216	29	direct adj execution adj logic	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:46
S217	4	711/170.ccls. and programmable adj logic adj blocks	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:46

EAST Search History

S218	6	"869200".ap.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:46
S219	8	711/171-172.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S220	81	711/170.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S221	81	711/170.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:46
S222	8	711/171-172.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:46
S223	17	711/173.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:46
S224	106	711/170.ccls. and reprogram$5	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S225	93	711/171-172.ccls. and (reprogram$5 reconfig$6)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S226	82	S225 not S224	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S227	527	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S228	19	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and prefetch	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S229	113	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and bandwidth	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S230	7	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and vhdl	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S231	47	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and matrix	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S232	15	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and parallelism	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S233	1	"6553477".pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S234	6	711/170-173.ccls. and reconfigurable adj processor	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46

EAST Search History

S235	9	("20030046530" | "5737524" | "5872919" | "5915104" | "5953512" | "6000014" | "6104415" | "6216219" | "6339819").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:46
S236	445	reconfigurable adj processor	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46
S237	812	reconfigurable adj2 processor	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46
S238	367	S237 not S236	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46
S239	160	S237 and ("711" "713").clas.	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46
S240	11	(adaptive adj processor) and ("711" "713").clas.	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46
S241	5	S240 not S239	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46
S242	0	"008128".pa.	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46
S243	6	"008128".ap.	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46
S244	49	src adj computers	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46
S245	7	711/117.ccls. and reconfigurable near3 (memory cache RAM random adj access adj memory processor)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S246	19	711/118.ccls. and reconfigurable near3 (memory cache RAM random adj access adj memory processor)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S247	4	"859051".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S248	1	"6678790".pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S249	4	"021492".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S250	1	"6563746".pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S251	2	("6574682" "5860111").pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46

EAST Search History

S252	4	("6026402" "6633515").pn. "20030169283" "20030136846"	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S253	3	"20030208658" "20030194458"	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S254	161	reconfigur$3 adj (processor micro-processor CPU processor)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S255	0	reconfigur$3 adj (processor micro-processor CPU microprocessor) and prefetch	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S256	999	smc.as.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S257	0	smc.as. and "711".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S258	0	smc.as. and "712".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S259	0	(smc and computers) .as. and "712".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S260	0	(smc and computers) .as.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S261	0	(smc and computers).as.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S262	2217	711/170.ccls.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S263	438	reconfigurable adj processor	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S264	1	("6779131").URPN.	USPAT	OR	ON	2006/07/24 11:46
S265	8	711/171-172.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S266	81	711/170.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S267	81	711/170.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:46
S268	527	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S269	113	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and bandwidth	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S270	445	reconfigurable adj processor	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46
S271	11	(adaptive adj processor) and ("711" "713").clas.	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46

EAST Search History

S272	0	"008128".pa.	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:46
S273	1	"5024031".pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S274	1	"6779131".pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S275	1	"6553477".pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S276	1	"6678790".pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S277	1	"6563746".pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S278	8	reconfigur$3 adj (processor micro-processor CPU microprocessor) and "711".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S279	13	711/170-173.ccls. and dynamic near3 logic	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S280	16	(src and computers).as.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S281	114	711/170.ccls. and dynamic$4 near3 configur$5	US-PGPUB; USPAT	OR	ON	2006/07/24 11:46
S282	6	711/170.ccls. and dynamic$4 near3 configur$5 with cache	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S283	6	"206189".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S284	6	"869200".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S285	81	711/170.ccls. and fpga	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S286	298	S263 and fpga	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S287	12	S286 and memory with reconfiguring	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S288	57	711/170.ccls. and ((reconfigur$5 rearrang$4) and application adj specific)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S289	81	711/170.ccls. and FPGA	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S290	9	("5892896" | "6060339" | "6081463" | "6154851" | "6204562" | "6363502" | "6405324" | "6483755" | "6530005").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:47

EAST Search History

S291	29	direct adj execution adj logic	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:47
S292	4	711/170.ccls. and programmable adj logic adj blocks	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:47
S293	6	"869200".ap.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:47
S294	8	711/171-172.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:47
S295	17	711/173.ccls. and FPGA	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:47
S296	106	711/170.ccls. and reprogram$5	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S297	93	711/171-172.ccls. and (reprogram$5 reconfig$6)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S298	82	S297 not S296	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S299	19	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and prefetch	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S300	7	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and vhdl	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S301	47	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and matrix	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S302	15	711/170-172.ccls. and ((configur$5).ti. (configur$6).ab.) and parallelism	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S303	6	711/170-173.ccls. and reconfigurable adj processor	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:47
S304	9	("20030046530" | "5737524" | "5872919" | "5915104" | "5953512" | "6000014" | "6104415" | "6216219" | "6339819").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/24 11:47
S305	812	reconfigurable adj2 processor	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:47
S306	160	S305 and ("711" "713").clas.	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:47

EAST Search History

S307	5	S271 not S306	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:47
S308	6	"008128".ap.	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:47
S309	49	src adj computers	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:47
S310	7	711/117.ccls. and reconfigurable near3 (memory cache RAM random adj access adj memory processor)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S311	19	711/118.ccls. and reconfigurable near3 (memory cache RAM random adj access adj memory processor)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S312	4	"859051".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S313	4	"021492".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S314	2	("6574682" "5860111").pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S315	4	("6026402" "6633515").pn. "20030169283" "20030136846"	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S316	3	"20030208658" "20030194458"	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S317	190	reconfigur$3 adj (processor micro-processor CPU microprocessor)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S318	126	711/170.ccls. and matrix	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S319	214	712/15.ccls.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S320	298	S263 and fpga	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S321	160	S305 and ("711" "713").clas.	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:47
S322	438	reconfigurable adj processor	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S323	378	711/170.ccls. and (application near2 specific application-specific)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S324	314	711/170.ccls. and reconfig$7	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S325	367	S305 not S270	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:47

EAST Search History

S326	598	711/170.ccls. and (reconfigur$5 rearrang$4 application adj specific)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S327	812	reconfigurable adj2 processor	US-PGPUB; USPAT; JPO	OR	ON	2006/07/24 11:47
S328	2	("20030070055" "20030217244")	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S329	6	"869200".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S330	707	(configurable reconfigurable "re-configurable") adj processor	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S331	789	(configurable reconfigurable "re-configurable") adj (processor (processing adj unit) CPU microprocessor "micro-processor")	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S332	57	((configurable reconfigurable "re-configurable") adj (processor (processing adj unit) CPU microprocessor "micro-processor")).ti.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S333	393	S331 and (FPGA PLD)	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S334	359	S333 not S332	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S335	1	"6507213".pn.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S336	4	("6507213").URPN.	USPAT	OR	ON	2006/07/24 11:47
S337	957	((configurable reconfigurable "re-configurable") adj (processor (processing adj unit) CPU microprocessor "micro-processor" cache))	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S338	391	S337 and fpga	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S339	15	S338 and "711".clas.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S340	30	direct adj execut$3 adj logic	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S341	20	memory adj algorithm adj processor	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S342	6	"869200".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S343	3363	711/170-173.ccls.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47

EAST Search History

S344	35	S343 and reconfigurable near3 (processor multiprocessor cache CPU (processing adj unit))	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S345	3	"682579".ap.	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S346	1	"20030088610"	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S347	0	"2003004117"	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S348	1	"20030004117"	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S349	10	hoyle.in. and operating adj system	US-PGPUB; USPAT	OR	ON	2006/07/24 11:47
S350	1	"6507898".pn.	USPAT	OR	OFF	2006/07/24 12:06
S351	1	"6507898".pn.	USPAT	OR	OFF	2006/07/24 12:06

INTERFERENCE SEARCH

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	26	(processor and prefetch$3 and memory and algorithm).clm.	US-PGPUB; USPAT	OR	ON	2006/07/24 12:19