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NOTICE OF ALLOWANCE AND FEE(S) DUE

25235 7590 07/26/2006

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER	
THOMAS, SHANE M	
ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 07/26/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/869,200	06/16/2004	Daniel Poznanovic	SRC028	5929

TITLE OF INVENTION: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	10/26/2006

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

Petitioners Amazon
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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25235 7590 07/26/2006

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/869,200	06/16/2004	Daniel Poznanovic	SRC028	5929

TITLE OF INVENTION: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	10/26/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
THOMAS, SHANE M	2186	711-137000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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EXAMINER	
THOMAS, SHANE M	
ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 07/26/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

Notice of Allowability	Application No.	Applicant(s)	
	10/869,200	POZNANOVIC ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE / Amendment filed 6/15/2006*.

2. ☒ The allowed claim(s) is/are *1,4-12,15-23 (renumbered 1-19)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

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REASONS FOR ALLOWANCE

Claims 1,4-12, and 15-23 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance:

As per independent claims 1,11, and 17, the prior art of record does not teach or suggest, either alone or in combination, the every limitation of each claim. Specifically the prior art of record does not teach in combination a reconfigurable processor with a data prefetch unit only fetching computational data required by an algorithm in addition to a first memory and the prefetch unit being configurable to conform to the requirements (needs) of a particular algorithm where the data prefetch unit is configured to match format and location of the in the second memory (claim 1). Further regarding claims 11 and 17, the prior art of record does not teach the prefetch unit operating independent and in parallel with the logic blocks that are using computational data with the data prefetch unit only transferring data necessary for computations. Further regarding claim 17, the prior art of record does not specifically teach a computation unit, prefetch unit, and data access unit all being configurable in order to conform to the needs of an algorithm implemented on the computational unit.

Gibson et al. (U.S. Patent No. 6,507,898) teaches a reconfigurable cache controller but does not teach each limitation of the independent claims of Applicant.

Howard et al. (U.S. Patent Application Publication No. 2005/0044327) teaches a reconfigurable processor that may be reconfigured based on the algorithm being run (¶52 and ¶90).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Shane M. Thomas

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Notice of References Cited	Application/Control No. 10/869,200	Applicant(s)/Patent Under Reexamination POZNANOVIC ET AL.	
	Examiner Shane M. Thomas	Art Unit 2186	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,507,898	01-2003	Gibson et al.	711/168
*	B	US-2005/0044327	02-2005	Howard et al.	711/147
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Petitioners Amazon
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Issue Classification	Application/Control No. 10/869,200	Applicant(s)/Patent under Reexamination POZNANOVIC ET AL.
	Examiner Shane M. Thomas	Art Unit 2186

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION											
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED						
711	170	G	06	F	12	/00					/		
CROSS REFERENCES						/					/		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)												
711	154					/					/		
						/					/		
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Shane M. Thomas 7/24/06
(Assistant Examiner) (Date)

(Legal Instruments Examiner) (Date)

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
(Primary Examiner) (Date) 7/24/06

Total Claims Allowed: 19

O.G. Print Claim(s)	O.G. Print Fig.
1	4

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
2	4		34		64		94		124		154		184
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5	7		37		67		97		127		157		187
6	8		38		68		98		128		158		188
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18	22		52		82		112		142		172		202
19	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
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	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/869,200	POZNANOVIC ET AL.	
Examiner	**Art Unit**	
Shane M. Thomas	2186	

SEARCHED			
Class	Subclass	Date	Examiner
711	170	7/24/2006	SMT

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
Interference Search (see interference search printout)		7/24/2006	SMT

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Updated East Search	10/15/2005	SMT
711/170-173 (text search only - see search printout)	10/15/2005	SMT
Updated EAST Search (see attached printout)	7/24/2006	SMT
712/207 (text search only - see search printout)	7/24/2006	SMT
711/154 (text search only - see search printout)	7/24/2006	SMT

Index of Claims

Application No.	Applicant(s)	
10/869,200	POZNANOVIC ET AL.	
Examiner	**Art Unit**	
Shane M. Thomas	2186	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date									
Final	Original	1/5/05	7/6/05	10/15/05	3/17/06	7/24/06					
	1	√	√	√	√	=					
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BIBDATASHEET

Bib Data Sheet

CONFIRMATION NO. 5929

SERIAL NUMBER	FILING OR 371(c) DATE / RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/869,200	06/16/2004	711	2186	SRC028

APPLICANTS

Daniel Poznanovic, Colorado Springs, CO;
David E. Caliga, Colorado Springs, CO;
Jeffrey Hammes, Colorado Springs, CO;

**** CONTINUING DATA ***************************

This appln claims benefit of 60/479,339 06/18/2003 YES SM 7/24/06

**** FOREIGN APPLICATIONS *********************

NONE

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/04/2004

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☒ no 35 USC 119 (a-d) conditions ☐ yes ☒ no ☐ Met after Allowance met Verified and Acknowledged Examiner's Signature Initials	CO	12	24	4

ADDRESS

25235

TITLE

System and method of enhancing efficiency and utilization of memory bandwidth in reconfigurable hardware

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
928	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Petitioners Amazon
Ex. 1010, p. 302 of 399

Issue Classification	Application/Control No. 10/869,200	Applicant(s)/Patent under Reexamination POZNANOVIC ET AL.
	Examiner Shane M. Thomas	Art Unit 2186

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION											
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED						
711	170	G	06	F	12	/00				/			
CROSS REFERENCES						/				/			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)												
711	154					/				/			
						/				/			
						/				/			
						/				/			
						/				/			

Shane M. Thomas 7/24/06
(Assistant Examiner) (Date)

(Legal Instruments Examiner) (Date)

GARY PORTKA
PRIMARY EXAMINER
Gary J Portka 9/19/06
(Primary Examiner) (Date)

Total Claims Allowed: 19

O.G. Print Claim(s)	O.G. Print Fig.
1	4

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
2	4		34		64		94		124		154		184
3	5		35		65		95		125		155		185
4	6		36		66		96		126		156		186
5	7		37		67		97		127		157		187
6	8		38		68		98		128		158		188
7	9		39		69		99		129		159		189
8	10		40		70		100		130		160		190
9	11		41		71		101		131		161		191
10	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
	14		44		74		104		134		164		194
11	15		45		75		105		135		165		195
12	16		46		76		106		136		166		196
13	17		47		77		107		137		167		197
14	18		48		78		108		138		168		198
15	19		49		79		109		139		169		199
16	20		50		80		110		140		170		200
17	21		51		81		111		141		171		201
18	22		52		82		112		142		172		202
19	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

PTO/SB/08a (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	10869200
	Filing Date	2004-06-16
	First Named Inventor	Daniel Poznanovic et al.
	Art Unit	2186
	Examiner Name	Thomas, Shane M.
	Attorney Docket Number	SRC028

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6076152		2000-06-13	Huppenthal et al.	
	2	6247110		2001-06-12	Huppenthal et al.	
	3	6356963		2002-03-12	Parks	
	4	6594736		2003-06-15	Parks	
If you wish to add additional U.S. Patent citation information please click the Add button.						Add

U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS								Remove
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10869200
	Filing Date	2004-06-16
	First Named Inventor	Daniel Poznanovic et al.
	Art Unit	2186
	Examiner Name	Thomas, Shane M.
	Attorney Docket Number	SRC028

	1							☐

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10869200
	Filing Date	2004-06-16
	First Named Inventor	Daniel Poznanovic et al.
	Art Unit	2186
	Examiner Name	Thomas, Shane M.
	Attorney Docket Number	SRC028

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☑ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☑ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/william j. kubida/	Date (YYYY-MM-DD)	2006-10-05
Name/Print	William J. Kubida	Registration Number	29664

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

EFS-Web
Attorney Docket No. SRC028
Client/Matter No. 80404.0033.001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200	Art Unit: 2186
Application of: Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes	Confirmation No.: 5929
Filed: June 16, 2004	Customer No.: **25235**
Examiner: THOMAS, Shane M.	
Attorney Docket No. SRC028	
For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.97

MAIL STOP ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.97(i), please place the attached Form PTO/SB/08A of the listed patents and non-patent publications in the above-referenced file. In submitting these references, no representation is made or implied that the references are or are not material to the examination of this application.

A Notice of Allowance was mailed in this case on July 26, 2006. The Issue Fee is due October 26, 2006, but has not yet been paid.

This Information Disclosure Statement is filed with no request for consideration of these references. Accordingly, no fee is believed due. However, any fee associated herewith may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

05 Oct 2006
Date

William J. Kubida, Reg. No. 29,664
HOGAN & HARTSON LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5909 Tel
(303) 899-7333 Fax

Electronic Acknowledgement Receipt

EFS ID:	1241254
Application Number:	10869200
Confirmation Number:	5929
Title of Invention:	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
First Named Inventor:	Daniel Poznanovic
Customer Number:	25235
Filer:	William J. Kubida/Julie Lange
Filer Authorized By:	William J. Kubida
Attorney Docket Number:	SRC028
Receipt Date:	06-OCT-2006
Filing Date:	16-JUN-2004
Time Stamp:	17:50:02
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1	Information Disclosure Statement (IDS) Filed	SRC028IDSform.pdf	720846	no	4

Warnings:					
Information:					
2	Transmittal letter	DOC200.PDF	10564	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	731410		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25235 7590 07/26/2006

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

via EFS-Web

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for ~~first class mail~~ in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Julie Lange	(Depositor's name)
	(Signature)
18 October 2006	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/869,200	06/16/2004	Daniel Poznanovic	SRC028	5929

TITLE OF INVENTION: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	10/26/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
THOMAS, SHANE M	2186	711-137000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 William J. Kubida
2 Michael C. Martensen
3 Hogan & Hartson LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: SRC Computers, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Colorado Springs, Colorado

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-1123 (~~enclose an extra copy of this form~~).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 18 October 2006

Typed or printed name William J. Kubida Registration No. 29,664

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Petitioners Amazon
Ex. 1010, p. 311 of 399

Electronic Patent Application Fee Transmittal

Application Number:	10869200
Filing Date:	16-Jun-2004
Title of Invention:	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
First Named Inventor/Applicant Name:	Daniel Poznanovic
Filer:	William J. Kubida/Julie Lange
Attorney Docket Number:	SRC028
Filed as Large Entity	

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1400	1400
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	1700

Electronic Acknowledgement Receipt	
EFS ID:	1260781
Application Number:	10869200
International Application Number:	
Confirmation Number:	5929
Title of Invention:	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
First Named Inventor/Applicant Name:	Daniel Poznanovic
Customer Number:	25235
Filer:	William J. Kubida/Julie Lange
Filer Authorized By:	William J. Kubida
Attorney Docket Number:	SRC028
Receipt Date:	18-OCT-2006
Filing Date:	16-JUN-2004
Time Stamp:	17:29:10
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$1700
RAM confirmation Number	475
Deposit Account	501123
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment Recorded	DOC270.PDF	163656	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	8362	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	172018		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/869,200	06/16/2004	Daniel Poznanovic	SRC028	5929

25235 7590 10/19/2006

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER	
THOMAS, SHANE M	
ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Supplemental Notice of Allowability	Application No.	Applicant(s)	
	10/869,200	POZNANOVIC ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *IDS filed 10/6/2006, after Notice of Allowance*.

2. ☒ The allowed claim(s) is/are *1,4-12 and 15-23 (renumbered 1-19)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/06/2006
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

PIERRE BATAILLE
PRIMARY EXAMINER 10/12/06

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Ex. 1010, p. 317 of 399

PTO/SB/08a (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10869200
	Filing Date	2004-06-16
	First Named Inventor	Daniel Poznanovic et al.
	Art Unit	2186
	Examiner Name	Thomas, Shane M.
	Attorney Docket Number	SRC028

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
SM	1	6076152		2000-06-13	Huppenthal et al.	
SM	2	6247110		2001-06-12	Huppenthal et al.	
	~~3~~	~~6356963~~		~~2002-03-12~~	~~Parks~~	
SM	4	6594736		2003-06-15	Parks	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10869200
	Filing Date	2004-06-16
	First Named Inventor	Daniel Poznanovic et al.
	Art Unit	2186
	Examiner Name	Thomas, Shane M.
	Attorney Docket Number	SRC028

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
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Examiner Signature		Date Considered	10/12/06

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/869,200	12/12/2006	7149867	SRC028	5929

25235 7590 11/22/2006

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Daniel Poznanovic, Colorado Springs, CO;
David E. Caliga, Colorado Springs, CO;
Jeffrey Hammes, Colorado Springs, CO;

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO: 7,149,867

APPLICATION NO.: 10/869,200

ISSUE DATE: Dec. 12, 2006

INVENTOR(S): Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12, line 43, insert "first" after "coupled to the"

Column 12, line 57, insert "second" after "between the"

Column 13, line 6, "a" should be --the--

Column 14, line 4, the second occurrence of "the" should be --a--

Mailing Address of Sender:
William J. Kubida
Hogan & Hartson LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, CO 80202

Send to: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Electronic Acknowledgement Receipt	
EFS ID:	1601087
Application Number:	10869200
International Application Number:	
Confirmation Number:	5929
Title of Invention:	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
First Named Inventor/Applicant Name:	Daniel Poznanovic
Customer Number:	25235
Filer:	William J. Kubida/Julie Lange
Filer Authorized By:	William J. Kubida
Attorney Docket Number:	SRC028
Receipt Date:	16-MAR-2007
Filing Date:	16-JUN-2004
Time Stamp:	21:01:40
Application Type:	Utility

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1		DOC001.PDF	24153	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	2
	Request for Certificate of Correction	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	24153	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Attorney Docket No.: SRC028
Client/Matter No: 80404.0033.001
EFS-Web

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Name of Patentee:

Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes

Patent No.: 7,149,867

Issued: Dec. 12, 2006

Title: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE

ATTENTION: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR

PTO Mistake (37 C.F.R. 1.322(a))

DEAR SIR:

An error appears in this patent. The error is a formatting mistake by the PTO. The error occurred in good faith. Correction thereof does not involve such changes in the patent as would constitute new matter or would require reexamination.

Attached hereto in duplicate is form PTO-1050, with at least one copy being suitable for printing.

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Hogan & Hartson LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, CO 80202

Although no fee is believed due, any fee deficiency associated with this transmittal may be charged to Deposit Account 50-1123.

Respectfully submitted,

Date: 16 March 2007

BY: _____

William J. Kubida, Reg. No. 29,664
Hogan & Hartson LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5909 Tel
(303) 899-7333 Fax

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,149,867 B2
APPLICATION NO. : 10/869200
DATED : December 12, 2006
INVENTOR(S) : Daniel Poznanovic, David E. Caliga and Jeffrey Hammes

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12, line 43, insert --first-- after "coupled to the"

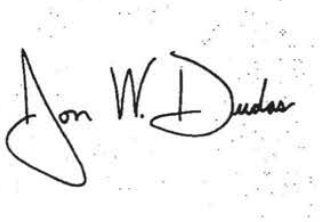
Column 12, line 57, insert --second-- after "between the"

Column 13, line 6, "a" should be --the--

Column 14, line 4, the second occurrence of "the" should be --a--.

Signed and Sealed this

Twenty-fourth Day of April, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

PATENT
EFS-Web
Attorney Docket No. SRC028
Client/Matter No. 80404.0033.001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200 Application of: Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes Filed: June 16, 2004 Attorney Docket No. SRC028 For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	Art Unit: 2186 Confirmation No.: 5929 Examiner: THOMAS, Shane M. Customer No.: **25235**

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.97

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.97(i), please place the attached Form 1449 and the enclosed copy of the listed non-patent reference in the above-referenced file. In submitting these references, no representation is made or implied that the references are or are not material.

This Information Disclosure Statement is filed with no request for consideration of this reference. Accordingly, no fee is believed due. However, any fee associated herewith may be charged to Deposit Account No. 50-1223.

Respectfully submitted,

31 AUGUST 2008
Date

William J. Kubida, Reg. No. 29,664
HOGAN & HARTSON LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5909 Tel
(303) 899-7333 Fax

Doc code :IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (08-08)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	10869200
	Filing Date	2004-06-16
	First Named Inventor	Daniel Poznanovic et al.
	Art Unit	2186
	Examiner Name	Thomas, Shane M.
	Attorney Docket Number	SRC028

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5941981		1999-08-24	Tran Thang M.	Abstract, fig. 1; col. 2, line 31 - 59; col. 3, line 6 - 18; col. 4, line 10 - 24.

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10869200
	Filing Date	2004-06-16
	First Named Inventor	Daniel Poznanovic et al.
	Art Unit	2186
	Examiner Name	Thomas, Shane M.
	Attorney Docket Number	SRC028

	1	HAUCK S. ED, Association for Computing Machinery: "Configuration Prefetch for Single Context Reconfigurable Coprocessors", ACM/SIGDA International Symposium on Field Programmable Gate Arrays, FPGA '98, Monterey, CA, New York, NY, ACM, US, vol. 6th Conf., XP000883989, ISBN: 978-0-89791-978-4, Feb. 22-24, 1998, the whole document.	☐

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Examiner Signature		Date Considered	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10869200
	Filing Date	2004-06-16
	First Named Inventor	Daniel Poznanovic et al.
	Art Unit	2186
	Examiner Name	Thomas, Shane M.
	Attorney Docket Number	SRC028

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature		Date (YYYY-MM-DD)	2008-08-13
Name/Print	WILLIAM J. KUBIDA	Registration Number	29,664

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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- 9 JUN 2008
Hanna, Moore & Curley

Date
05.06.08

Reference	Application No./Patent No.
H07-283-16	04776806.4 - 1229
Applicant/Proprietor	
SRC COMPUTERS, INC.	

Communication

The European Patent Office herewith transmits as an enclosure the supplementary European search report under Article 153(7) EPC for the above-mentioned European patent application.

If applicable, copies of the documents cited in the European search report are attached.

☑ Additional set(s) of copies of the documents cited in the European search report is (are) enclosed as well.

Refund of the search fee

If applicable under Article 9 Rules relating to fees, a separate communication from the Receiving Section on the refund of the search fee will be sent later.

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EPO Form 1507.4 12.07

European Patent Office

SUPPLEMENTARY EUROPEAN SEARCH REPORT

Application Number
EP 04 77 6806

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 5 941 981 A (TRAN THANG M [US]) 24 August 1999 (1999-08-24) * abstract; figure 1 * * column 2, line 31 - line 59 * * column 3, line 6 - line 18 * * column 4, line 10 - line 24 *	1-15	INV. G06F12/00
A	US 2003/084244 A1 (PAULRAJ DOMINIC [US]) 1 May 2003 (2003-05-01) * paragraphs [0010] - [0012], [0022] - [0024], [0026] - [0028]; figures 4-6 *	1-15	
A	HAUCK S ED - ASSOCIATION FOR COMPUTING MACHINERY: "CONFIGURATION PREFETCH FOR SINGLE CONTEXT RECONFIGURABLE COPROCESSORS" ACM/SIGDA INTERNATIONAL SYMPOSIUM ON FIELD PROGRAMMABLE GATE ARRAYS. FPGA '98. MONTEREY, CA, FEB. 22 - 24, 1998; [ACM/SIGDA INTERNATIONAL SYMPOSIUM ON FIELD PROGRAMMABLE GATE ARRAYS], NEW YORK, NY : ACM, US, vol. 6TH CONF, 22 February 1998 (1998-02-22), pages 65-74, XP000883989 ISBN: 978-0-89791-978-4 * the whole document *	1-15	

TECHNICAL FIELDS SEARCHED (IPC)
G06F

The supplementary search report has been based on the last set of claims valid and available at the start of the search.

Place of search	Date of completion of the search	Examiner
The Hague	28 May 2008	Jardon, Stéphan

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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Ex. 1010, p. 332 of 399

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 04 77 6806

This annex lists the patent family membersrelating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

28-05-2008

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5941981 A	24-08-1999	NONE	
US 2003084244 A1	01-05-2003	WO 03038626 A2	08-05-2003

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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XS CPRTENFRDE

BNSDOCID: <XS ____ 2006100103CF_I_>

XP-000883989

Configuration Prefetch for Single Context Reconfigurable Coprocessors

P.D. 22.02.98
p. 65-74 = 10
B022000

Scott Hauck
Department of Electrical and Computer Engineering
Northwestern University
Evanston, IL 60208-3118 USA
hauck@ece.nwu.edu

Abstract

Current reconfigurable systems suffer from a significant overhead due to the time it takes to reconfigure their hardware. In order to deal with this overhead, and increase the power of reconfigurable systems, it is important to develop hardware and software systems to reduce or eliminate this delay. In this paper we propose one technique for significantly reducing the reconfiguration latency: the prefetching of configurations. By loading a configuration into the reconfigurable logic in advance of when it is needed, we can overlap the reconfiguration with useful computation. We demonstrate the power of this technique, and propose an algorithm for automatically adding prefetch operations into reconfigurable applications. This results in a significant decrease in the reconfiguration overhead for these applications.

1 Introduction

When FPGAs were first introduced in the mid 1980s they were viewed as a technology for replacing standard gate arrays for some applications. In these first generation systems, a single configuration is created for the FPGA, and this configuration is the only one loaded into the FPGA. A second generation soon followed, with FPGAs that could use multiple configurations, but reconfiguration was done relatively infrequently [Hauck97a]. In such systems, the time to reconfigure the FPGA was of little concern.

Many of the most exciting applications being developed with FPGAs today involve run-time reconfiguration [Hauck97a]. In such systems the configuration of the FPGAs may change multiple times in the course of a computation, reusing the silicon resources for several different parts of a computation. Such systems have the potential to make more effective use of the chip resources than even standard ASICs, where fixed hardware may only be used in a portion of the computation. However, the advantages of run-time reconfiguration do not come without a cost. By requiring multiple reconfigurations to complete a computation, the time it takes to reconfigure the FPGA becomes a significant concern. In most systems the FPGA must sit idlewhile it is being reconfigured, wasting cycles that could otherwise be performing useful work. For example, applications on the DISC and DISC II system have spent 25% [Withlin96] to 71% [Wirthlin95] of their execution time performing reconfiguration.

It is obvious from these overhead numbers that reductions in the amount of cycles wasted to reconfiguration delays can have a significant impact on the performance of run-time reconfigured systems. For example, if an application spends 50% of its time in reconfiguration, and we were somehow able to reduce the overhead per reconfiguration by a factor of 2, we would reduce the application's runtime by at least 25%. In fact, the performance improvement could be even higher than this. Specifically, consider the case of an FPGA used in conjunction with a host processor, with only the most time-critical portions of the code mapped into reconfigurable logic. An application developed for such a system with a given reconfiguration delay may be unable to take advantage of some optimizations because the speedups of the added functionality are outweighed by the additional reconfiguration delay required to load the functionality into the FPGA. However, if we can reduce the reconfiguration delay, more of the logic might profitably be mapped into the reconfigurable logic, providing an even greater performance improvement. For example, in the UCLA ATR work the system wastes more than 75% of its cycles in reconfiguration [Villasenor96, Villasenor97]. This overhead has limited the optimizations explored with the algorithm, since performance optimizations to the computation cycles will yield only limited improvement in the overall runtimes. This has kept the researchers from using higher performance FPGA families and other optimizations which can significantly reduce the computation cycles required.

Because of the potential for improving the performance of reconfigurable systems, developing techniques for reducing the reconfiguration delay is an important research area. In this paper we consider one method for reducing this overhead: the overlapping of computation with reconfiguration via the prefetching of FPGA configurations.

2 Configuration Prefetch

Run-time reconfigured systems use multiple configurations in the FPGA(s) in the system during a single computation. In current systems the computation is allowed to run until a configuration that is not currently loaded is required to continue the computation. At that point, the computation is stalled while the

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new configuration is loaded. These stall cycles represent an overhead to the computation, increasing runtimes without performing useful work on the actual computation.

A simple method to reduce or eliminate this reconfiguration overhead is to begin loading the next configuration before it is actually required. Specifically, in systems with multiple contexts [Bolotski94], partial run-time reconfigurability [Hutchings95], or tightly coupled processors [DeHon94, Razdan94, Wittig96, Hauck97b] it is possible to load a configuration into all or part of the FPGA while other parts of the system continue computing. In this way, the reconfiguration latency is overlapped with useful computations, hiding the reconfiguration overhead. We will call the process of preloading a configuration before it is actually required *configuration prefetching*.

The challenge in configuration prefetching is determining far enough in advance which configuration will be required next. Many computations (especially those found in general-purpose computations) can have very complex control flows, with multiple execution paths branching off from any point in the computation, each potentially leading to a different next configuration. At a given point in the computation it can be difficult to decide which configuration will be required next. Even worse, the decision of which configuration to prefetch may need to be done hundreds or thousands of cycles in advance if we wish to hide the entire reconfiguration delay. In a system where it takes a thousand cycles to load a configuration, if we do not begin fetching the configuration at least a thousand cycles in advance we will be unable to hide the entire reconfiguration latency.

Not only is it necessary to decide which configuration to load far in advance of a configuration's actual use, it is also important to correctly guess which configuration will be required. In order to load a configuration, configuration data that is already in the FPGA must be overwritten. An incorrect decision on what configuration to load can not only fail to reduce the reconfiguration delay, but in fact can greatly increase the reconfiguration overhead when compared to a non-prefetching system. Specifically, the configuration that is required next may already be loaded, and an incorrect prefetch may require the system to have to reload the configuration that should have simply been retained in the FPGA, adding reconfiguration cycles where none were required in the non-prefetch case.

Note that prefetching has already been used successfully in other domains. Standard processors can use prefetching to load data into the processor's caches, or load data from disk into the processor's memory. However, the demands of configuration prefetching are quite different than those of other prefetching domains. In the case of prefetching data from disks into memory, or from memory into the processor's cache, the system can look for regular access patterns in order to predict the next required data. For configurations, the calling pattern will be extremely irregular. Because of this, new algorithms for determining how to best perform prefetching in reconfigurable systems must be developed in order to make this a viable approach to reducing the reconfiguration overhead.

In this paper, we will demonstrate the potential of prefetching for reconfigurable systems, and present a new algorithm for automatically determining how this prefetching should be performed. We first present a simple model of a reconfigurable system that can allow us to experiment with configuration prefetching. We then develop an upper bound on the improvements possible from configuration prefetching under this model via an (unachievable) optimal prefetching algorithm. Finally, we present a new algorithm for configuration prefetching which can provide significant decreases in the per-reconfiguration latency in reconfigurable systems. To the best of our knowledge, this is the first configuration prefetch algorithm developed for reconfigurable computing.

3 Reconfigurable System Model

In order to explore the potential of configuration prefetching, we will assume a reconfigurable computing architecture similar to that of the PRISC system [Razdan94]. This system will allow us to easily measure the benefits of configuration prefetch, while representing one of the most difficult systems for which to develop prefetching algorithms. In our experiments, we assume that the reconfigurable computing system consists of a standard microprocessor coupled with a reconfigurable coprocessor. This coprocessor is capable of implementing custom instructions for arbitrary computations. While the coprocessor can support multiple configurations for a given application, we assume that it is only capable of holding one computation at a time. In order to use the reconfigurable coprocessor to compute a different computation a new configuration must be loaded, which takes a fixed latency before it is ready for operation. The actual reconfiguration latency will be varied in our experiments to demonstrate the sensitivity of prefetching to reconfiguration latency, yet each individual experiment will have a fixed latency for all reconfigurations.

In normal operation, the processor executes instructions until a call to the reconfigurable coprocessor is found. These calls to the reconfigurable coprocessor (RFUOPs) contain the ID of the configuration required to compute the desired function. At this point, the coprocessor checks to see if the proper configuration is loaded. If it is not, the host processor is stalled while the configuration is loaded. Once the configuration is loaded (or immediately if the proper configuration was already present), the reconfigurable coprocessor executes the desired computation in a single clock cycle. Once a configuration is loaded it is retained for future executions, only being unloaded when some other coprocessor call or prefetch operation specifies a different configuration.

In order to avoid this latency, a program running on this reconfigurable system can insert prefetch operations into the code executed on the host processor. These prefetch instructions are executed just like any other instructions, occupying a single slot in the processor's pipeline. The prefetch instruction specifies the ID of a specific configuration that should be loaded into the coprocessor. If the desired configuration is already loaded, or is in the process of being loaded by some other prefetch instruction, this prefetch instruction becomes a NO-OP. If the specified configuration is not present, the coprocessor trashes the current configuration and begins loading the configuration specified. At this point the host processor is free to perform other computations.

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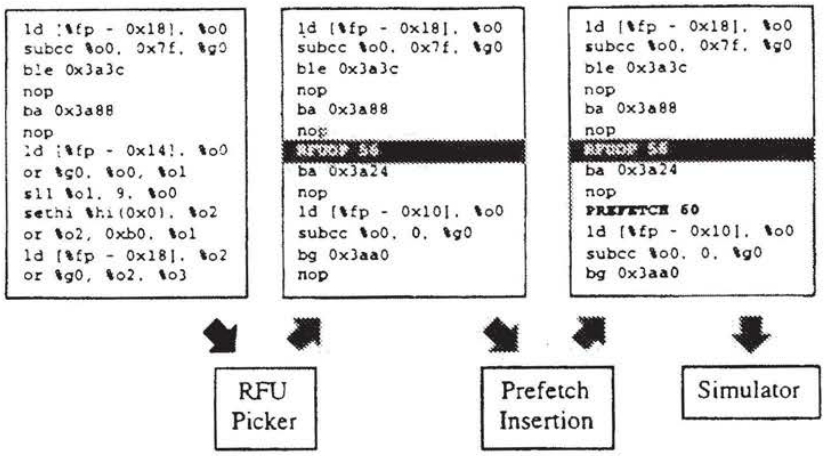

Figure 1. Experimental setup for the prefetch tests. Source code is augmented with calls to the reconfigurable coprocessor (RFUOPs) by the RFU picker. This code then has prefetch instructions inserted into it. The performance of a given set of RFUOPs and PREFETCHes is measured by the simulator.

overlapping the reconfiguration of the coprocessor with other useful work. Once the next call to the coprocessor occurs, it can take advantage of the loading performed by prefetch instruction. If this coprocessor call requires the configuration specified by the last prefetch operation, it will either have to perform no reconfiguration if the coprocessor has had enough time to load the entire configuration, or only require a shorter stall period as the remaining reconfiguration is done. Obviously, if the prefetch instruction specified a different configuration than was required by the coprocessor call, the processor will have to be stalled for the entire reconfiguration delay to load the correct configuration. Because of this, an incorrect prefetch operation can not only fail to save reconfiguration time, it can in fact increase the overhead due to the reconfigurable coprocessor. This occurs both in the wasted cycles of the useless prefetch operations, as well as the potential to overwrite the configuration that is in fact required next, causing a stall to reload a configuration that should have been retained in the reconfigurable coprocessor.

For simplicity we assume that the coprocessor can implement arbitrary code sequences, but these code sequences must not have any sequential dependencies. This is enforced by requiring that the code sequences mapped to the reconfigurable coprocessor appear sequentially in the executable, have a single entry point and a single exit point, and have no backwards edges. Note that while assuming a reconfigurable coprocessor could implement any such function is optimistic, it provides a reasonable testbed with properties similar to reconfigurable systems that have been proposed [Razdan94, Wittig96, Hauck97b].

4 Experimental Setup

In order to investigate the impact of prefetching on the reconfiguration overhead in reconfigurable systems, we have tested prefetching on some standard software benchmarks from the SPEC benchmark suite [Spec95]. Note that these applications have not been optimized for reconfigurable systems, and may not be as accurate in predicting exact performance as would real applications for reconfigurable systems. However, such real applications are not in general available for experimentation. Also, applications of reconfigurable systems are tailored to a specific system, and can be carefully optimized in reaction to a specific reconfiguration overhead. These applications may change significantly if they were mapped to a system with a much higher or lower reconfiguration delay, with different portions of the source code mapped to the reconfigurable logic. Thus, we feel that the only feasible way to investigate optimizations to the reconfiguration system is to use current, general-purpose applications, and make reasonable assumptions in order to mimic the structure of future reconfigurable system.

In order to conduct these experiments, we must perform three steps. First, some method must be developed to choose which portions of the software algorithms should be mapped to the reconfigurable coprocessor. Second, a prefetch algorithm must be developed to automatically insert prefetch operations into the source code. Third, a simulator of the reconfigurable system must be employed to measure the performance of these applications Each of these three steps will be described in paragraphs that follow.

The first step in the experiments is to choose which portions of the source code should be mapped to the reconfigurable coprocessor (these mappings will be referred to as RFUOPs here). As mentioned before, in this paper we will assume that arbitrary code sequences can be mapped to the reconfigurable logic as long as they have a single entry and a single exit point and have no backward branches or jumps. This ensures that only combinational code sequences are considered. This is a somewhat conservative assumption, since in many reconfigurable systems it is possible to implement loops and other sequential control flow operations in the reconfigurable logic.

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One complexity in deciding which portions of the source code should be mapped to the reconfigurable logic is to find that set of mappings that provide the best performance improvement in the face of a potentially substantial delay for each reconfiguration. In general this is a complex problem, and one we do not attempt to solve here. Our solution is to simply find all potential mappings to the reconfigurable logic, and then simulate the impact of including each candidate. This is done by repeatedly calling the reconfigurable system simulator, and assuming optimal prefetching (both of which are described later in this paper). Our algorithm then greedily chooses the candidate which provides the best performance improvement, and retests the remaining candidates. These retests examine the impact of including any one candidate in with the already chosen candidates. This repeats until the simulator determines that there is at most a potential 1% improvement available in the remaining candidates. In this way a reasonable set of RFUOPs can be developed which produces a significant performance improvement even when reconfiguration delay is taken into consideration. The result of this operation is to create a file that specifies which portion of the source executable should be mapped into RFUOPs, and which can be given to the simulator to compute the delays seen in the target reconfigurable system.

The simulator we have developed takes in an executable for a Sun SPARCstation, a specification of the location of RFUOPs and PREFETCH instructions in the executable, and a parameter that specifies the number of cycles it takes to reconfigure the coprocessor. This simulator is developed from the SHADE simulator [Cmelik93a]. This allows us to track the cycle-by-cycle operation of the system, and get exact cycle counts. Note that only one program can be executed at a time, and operating system calls are not instrumented, so context switch effects and the potential to overlap reconfiguration with cycles in the operating system are not considered. This simulator reports the reconfiguration time and overall performance for the application under both normal and optimal prefetching, as well as performance assuming no prefetching occurs at all. These numbers are used to measure the impact of the various prefetching techniques.

Note that for simplicity we model reconfiguration costs as a single delay constant. Issues such as latency verses bandwidth in the reconfiguration system, conflicts between configuration load and other memory accesses in systems which use a single memory port, and other concerns are ignored. Such effects can be considered to simply increase the average delay for each configuration load, and thus should not significantly impact the accuracy of the results. We consider a very wide range of reconfiguration overheads, from 10 cycles to 10,000 per reconfiguration. This delay range should cover most systems that are likely to be constructed, including the very long delays found in current systems, as well as very short delays that might be achieved by future highly cached architectures.

The remaining component of the experimental setup is the prefetch insertion program. This algorithm decides where prefetch instructions should be inserted into the executable given the set of RFUOPs determined by the RFU picker. The specific algorithm used will be described in a later section. The prefetch insertion program takes in the specification of RFUOPs from the RFU picker, as well as a control flow graph for the executable, and produces a file for the simulator that specifies the PREFETCH locations. Note that in a production system both the RFU picker and the prefetch insertion program would directly modify the executable. However, in order to allow us to use a standard processor simulator to simulate the reconfigurable system this information is maintained in a separate file.

5 Optimal Prefetch

In order to measure the potential prefetching has to reduce reconfiguration overhead in reconfigurable systems, we have developed the *Optimal Prefetch* concept. Optimal Prefetch represents the best any prefetch algorithm could hope to do, given the architectural assumptions and choice of RFUOPs presented earlier.

In Optimal Prefetching, instead of choosing specific locations for prefetch operations we assume that prefetch operations occur only when necessary, and occur as soon as possible. Specifically, whenever an RFUOP is encountered in the code, we determine what RFUOP was last called. If it was the same RFUOP it is assumed that no PREFETCH instructions occurred in between the RFUOPs since the correct RFUOP will simply remain in the coprocessor, requiring no reconfiguration. If the last RFUOP was different than the current call, it is assumed that a PREFETCH operation for the current call occurred directly after the last RFUOP. This yields the greatest possible overlap of computation with reconfiguration.

```
...
03a28 RFUOP 56
      ?? PREFETCH ??
03a2c ble 0x3a28 ! Branch to RFUOP 56
03a30 nop
03a34 ld [%fp - 0x10], %o0
03a38 subcc %o0, 0, %g0
03a3c ble 0x3a60 ! Branch beyond RFUOP 60
03a40 nop
03a44 RFUOP 60
...
```

Figure 2. Example of the optimism of the Optimal Prefetch technique. Once RFUOP 56 in line 3a28 is executed, there are multiple possible next RFUOPs which might be encountered. If the branch at 3a2c is taken, RFUOP 56 is executed again, and no intermediate prefetch cycle occurs. If neither the branch at 3a2c nor at 3a3c is taken, RFUOP 60 is the next to occur, and it is assumed that a PREFETCH 60 occurs right after the call of RFUOP 56, overlapping 6 cycles of computation with the reconfiguration. No fixed prefetching scheme could achieve both results for the code sequence shown.

It is important to realize that the Optimal Prefetch technique, while providing a bound on the potential of prefetching, potentially produces results better than what could possibly be

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Benchmark	Latency	No Prefetching	Optimal Prefetching	Ratio
Go	10	6,239,090	2,072,560	33.2%
	100	6,860,700	1,031,739	15.0%
	1,000	2,520,000	225,588	9.0%
	10,000	1,030,000	314,329	30.5%
Compress	10	344,840	63,403	18.4%
	100	127,100	46,972	37.0%
	1,000	358,000	289,216	80.8%
	10,000	520,000	12,535	2.4%
Li	10	6,455,840	958,890	14.9%
	100	4,998,800	66,463	1.3%
	1,000	55,000	21,325	38.8%
	10,000	330,000	43,092	13.1%
Perl	10	4,369,880	656,210	15.0%
	100	3,937,600	398,493	10.1%
	1,000	3,419,000	9,801	0.3%
	10,000	20,000	2	0.0%
Fpppp	10	2,626,180	1,415,924	53.9%
	100	11,707,000	6,927,877	59.2%
	1,000	19,875,000	5,674,064	28.5%
	10,000	370,000	4,485	1.2%
Swim	10	600,700	265,648	44.2%
	100	10,200	4,852	47.6%
	1,000	91,000	79,905	87.8%
	10,000	330,000	43,019	13.0%
Cumulative	10			26.2%
	100			16.6%
	1,000			16.5%
	10,000			2.3%
	All			11.4%

Table 1. The results of Optimal Prefetch on the benchmark programs. Each benchmark is tested at four different per-reconfiguration delay values. The "No Prefetch" and "Optimal Prefetch" columns report the total number of cycles spent stalling the processor while the coprocessor is reconfigured, plus the number of cycles spent on PREFETCH opcodes. The ratio column lists the ratio of Optimal Prefetching delays to No Prefetching delays. "All" is the average of all benchmarks at all reconfiguration delays considered.

done by an actual prefetching algorithm. As shown in Figure 2, Optimal Prefetching may assume that a prefetch instruction occurs at a given point in the code during some portions of the execution, while the same location does not contain a prefetch at other times. However, the bound provided by Optimal Prefetching is useful to demonstrate the limits of configuration prefetching.

As can be seen in Table 1, optimal prefetching has the potential to significantly reduce reconfiguration times. This ranges from an average factor of almost 4 for reconfigurable systems with a 10 cycle reconfiguration delay, to a factor of almost 44 for systems with a reconfiguration delay of 10,000 cycles. Averaged across the reconfiguration delays considered, this produces a reduction in reconfiguration delay of 88.6%, or a factor of almost 9.

It is important to realize that the reductions in reconfiguration delay shown in Table 1 represent only an upper bound on what is possible within the architecture described in this paper. It is unlikely that any actual prefetching algorithm will be able to achieve improvements quite as good as the Optimal Prefetch technique suggests. In the next section, we will present an algorithm for configuration prefetch. This algorithm determines

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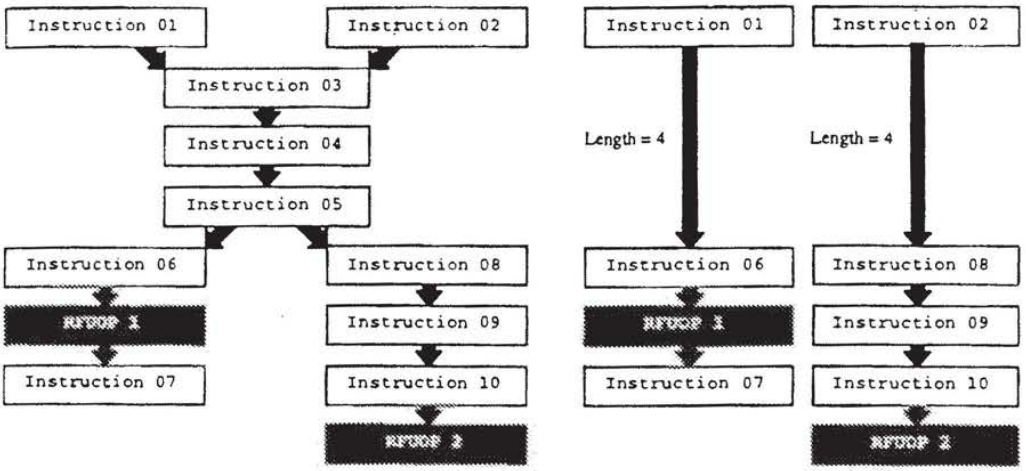

Figure 3. An example for the prefetch insertion algorithm (left), and the same example with the subroutine at instructions 3-5 removed (right).

specific locations where prefetch instructions should be inserted in order to overlap computation with reconfiguration.

6 Prefetch Insertion

In the previous sections we have proposed the concept of configuration prefetch, and have demonstrated that this technique has the potential to significantly reduce the reconfiguration overhead in reconfigurable systems, thus improving the performance of these systems. In this section we detail a specific algorithm which has the capability to realize some of these potential gains.

The challenge in developing a prefetch algorithm is to statically determine which RFUOP is the next to be needed at some point in the code. This decision must be done as far in advance of the RFUOP's execution as possible, so that most or all of the reconfiguration can be overlapped with useful computations. However, the earlier the PREFETCH operation occurs the more complicated the control flow between the PREFETCH and the RFUOP, increasing the likelihood that the wrong configuration will be loaded. In fact, from a given point in the code there may be many different RFUOPs that might occur next, since subsequent branches may lead to many different RFUOPs. Thus, at best we can hope to make an educated guess as to what configuration should be loaded, hoping that on average this prefetch will reduce the reconfiguration overhead as much as possible.

Our prefetch insertion algorithm starts with a control flow graph for the benchmark being considered. This graph contains information on the potential execution paths within the program, and thus forms the basis for determining which RFUOP will occur next. In a production system this control flow graph would be extracted from the source code. In our experimental system we construct the control flow graph from the executable via information provided by the SpixTools [Cmelik93b] code profiler, as well as some additional information from the simulator. The insertion algorithm also takes the locations of RFUOPs produced by the RFU picker.

The basis of our algorithm is a directed shortest-path algorithm on the control flow graph, starting from each RFUOP location. This is based upon the belief that the RFUOP that can be reached in the least number of clock cycles is the RFUOP configuration that should be loaded. We determine for each instructions in the executable which RFUOP can be reached in the shortest number of steps. Note that we only consider forward arcs in the control flow graph from an instruction to an RFUOP, or alternatively backward edges from RFUOP to preceding instructions, since this corresponds to the direction of control flow. This closest RFUOP is assumed to *own* the instruction, in that we will insert PREFETCH operations such that that RFUOP will either be present in the coprocessor when that instruction is executed, or will begin prefetching it at this time.

Once we determine which RFUOP owns each instruction, we have broken the code into *ownership regions*, where each region represents the portion of the executable's instructions owned by a given RFUOP. For example, in the code segment in Figure 3 left, instructions 01-06 are in RFUOP 1's ownership region, while instructions 08-10 are in RFUOP 2's ownership region. The next step in our prefetch insertion algorithm is to add PREFETCH operations before any instruction in one ownership region which has a direct predecessor in another ownership region. This PREFETCH operation will prefetch whichever RFUOP owns that instruction. Thus, in Figure 3 left we would insert a single PREFETCH operations, and that would be a prefetch for RFUOP 2 just before Instruction 08. Prefetches for RFUOP 1 would appear somewhere before Instruction 01 and Instruction 02, although their exact placement would depend on the exact control flow. In this way, we have multiple cycles in which to prefetch RFUOP 1, while we will change to prefetching RFUOP 2 once it becomes clear that that is the next RFUOP to occur, which

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Benchmark	Latency	No Prefetching	Basic Prefetch	(Bas/No)	Pruned Prefetch	(Pru/No)	(Pru/Opt)
Go	10	6,239,090	3,134,360	50.2%	2,862,128	45.9%	138.1%
	100	6,860,700	4,126,293	60.1%	2,989,912	43.6%	289.8%
	1,000	2,520,000	2,599,305	103.1%	996,300	39.5%	441.6%
	10,000	1,030,000	5,562,593	540.1%	706,611	68.6%	224.8%
Compress	10	344,840	86,284	25.0%	78,284	22.7%	123.5%
	100	127,100	78,821	62.0%	78,821	62.0%	167.8%
	1,000	358,000	311,677	87.1%	311,651	87.1%	107.8%
	10,000	520,000	1,156,939	222.5%	263,213	50.6%	2099.8%
Li	10	6,455,840	2,043,246	31.6%	1,929,195	29.9%	201.2%
	100	4,998,800	3,209,090	64.2%	2,395,041	47.9%	3603.6%
	1,000	55,000	6,898,414	12542.6%	42,082	76.5%	197.3%
	10,000	330,000	150,720	45.7%	150,720	45.7%	349.8%
Perl	10	4,369,880	1,873,472	42.9%	1,579,463	36.1%	240.7%
	100	3,937,600	2,241,365	56.9%	1,965,287	49.9%	493.2%
	1,000	3,419,000	5,616,728	164.3%	2,015,812	59.0%	20567.4%
	10,000	20,000	5,715	28.6%	5,714	28.6%	285700.0%
Fpppp	10	2,626,180	1,505,906	57.3%	1,490,467	56.8%	105.3%
	100	11,707,000	7,660,039	65.4%	7,656,892	65.4%	110.5%
	1,000	19,875,000	11,782,888	59.3%	5,805,461	29.2%	102.3%
	10,000	370,000	79,616,610	21518.0%	350,002	94.6%	7803.8%
Swim	10	600,700	325,339	54.2%	324,589	54.0%	122.2%
	100	10,200	139,174	1364.5%	5,573	54.6%	114.9%
	1,000	91,000	4,004,510	4400.6%	81,265	89.3%	101.7%
	10,000	330,000	41,995,371	12725.9%	56,126	17.0%	130.5%
Cumulative	10			41.8%		38.9%	148.3%
	100			103.3%		53.4%	321.2%
	1,000			411.1%		58.6%	355.2%
	10,000			591.8%		44.0%	1906.5%
	All			180.0%		48.1%	423.8%

Table 2. The results of the prefetching algorithm on the benchmark programs. Each benchmark is tested at four different per-reconfiguration delay values. The "Basic Prefetch" and "Pruned Prefetch" columns report the total number of cycles spent stalling the processor while the coprocessor is reconfigured, plus the number of cycles spent on PREFETCH opcodes. The ratio of prefetch to non-prefetch latency is also reported. The final column lists the ratio of Pruned Prefetch to Optimal Prefetch. "All" is the average of all benchmarks at all reconfiguration delays considered.

happens when we branch to Instruction 08. Note that an RFUOP is considered to be owned by itself, and thus if Instruction 07 is in REFUOP 1's ownership region we will not waste a PREFETCH by inserting it before Instruction 07, while if Instruction 07 is owned by some other RFUOP we would insert a PREFETCH for that RFUOP at this location.

There is one refinement to this initial prefetch insertion algorithm that can be important to creating the best prefetching. The issue is that subroutine calls may combine multiple different regions of the control flow graph, creating "false paths". Specifically, imagine that Instructions 03-05 represent a subroutine in the software, called by Instructions 01 and 02. If we use the algorithm just discussed, RFUOP 1 would be considered to own Instruction 02, even though there may be no execution path that would lead from Instruction 02 to RFUOP 1 without passing through some other RFUOP. The solution to this is simple: we replace most subroutine calls in the control flow graph with control flow edges from the instruction just before the subroutine call to the corresponding instruction just after the call, and this edge has a "length" (used in the shortest path algorithm) equal to the shortest execution path through that subroutine. Thus, if

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Instructions 03-05 in Figure 3 left were in fact a subroutine, we would remove these instructions, and replace them with a control flow arc from Instruction 01 to Instruction 06, and another arc from Instruction 02 to Instruction 08, with both of them having a length of 4 (Figure 3 right). Normal arcs have a length of 1. In this way, Instruction 01 would be owned by RFUOP 1, and Instruction 02 would be owned by RFUOP 2, giving each of them a much longer time to prefetch their configurations without sacrificing any accuracy in the prefetching decisions.

In order to do this simplification of the control flow graph we classify procedures as *pure* or *impure*. Any subroutine that does not contain an RFUOP, and does not call any impure subroutines, is considered *pure*. All others are considered *impure*. This distinction is important, because we do not want to remove any impure subroutines from the control flow graph. The reason for this is that an impure subroutine will contain RFUOPs which should block the ownership regions of RFUOPs following this subroutine call. For example, assume that Instructions 03-05 in Figure 3 left are a subroutine, and Instruction 04 is in fact an RFUOP 3 instruction. In this case, it should be clear that Instructions 01 and 02 should be owned by RFUOP 3, since that will always be the next RFUOP encountered after these instructions. However, if we remove this subroutine from the control flow graph we would not discover this fact. To deal with this, we only remove *pure* subroutines from the control flow graph, leaving all *impure* subroutines as is. Our algorithm would then properly label Instructions 01 and 02 as being owned by RFUOP3 and prefetch accordingly. The classification of subroutines as *pure* or *impure* can be made by a very simple search of the control flow graph.

As shown in Table 2, the prefetching algorithm as described so far (referred to here as the "Basic Prefetch" algorithm) does a reasonable job of prefetching in most cases, but can do a poor job in others. For example, the Basic Prefetch algorithm reduces the reconfiguration overhead by 58% on average for systems with a reconfiguration delay of 10 cycles, but can in fact increase the reconfiguration delay by a factor of almost 6 for systems with a reconfiguration delay of 10,000 cycles. The problem is that the algorithm sometimes makes poor decisions for some prefetch placements, causing the coprocessor to unload the configuration that is in fact the next one needed in the system. Obviously, something must be done to improve the consistency of the algorithm's results.

Our solution is to use a profiler-based pruning of the prefetch operations. We maintain statistics, on a per PREFETCH operation basis, of whether the outcome of that PREFETCH operation was beneficial or not. In those cases where it begins loading the configuration that is in fact the next RFUOP to be called, we credit it with the number of cycles saved. If it is the first RFUOP to overwrite the configuration that is required next, we reduce it's benefit by the number of cycles the system has to stall while reloading that configuration (note that a subsequent PREFETCH of the proper configuration can reduce this penalty). Finally, we also reduce the PREFETCH's benefit by the total number of times that prefetch operation is executed, since every time a PREFETCH operation is executed the processor must waste a cycle performing this operation. All of these statistics are easy to maintain, and could be reported by techniques similar to those found in prof, gprof, and other program profilers.

The information gathered on a per PREFETCH basis measures the effect this instruction has on the operation of the system. We go through these statistics and remove ("prune") any PREFETCH instruction that has a net loss on the operation of the system. This operation is similar to the performance optimization performed on standard software algorithms, with the added benefit that it can be easily automated, requiring no user intervention. Note that the pruning of one PREFETCH operation can cause another PREFETCH to have a negative impact on the system operation. For example, in between two calls to the same RFUOP there may be two different PREFETCH operations for other RFUOPs. During the first pruning step the first PREFETCH operation would be penalized for unloading the RFUOP, and would be removed. At this point, the second PREFETCH is responsible for overwriting the RFUOP that should have been retained. Our solution is to run the pruning process iteratively, continuing to remove PREFETCH operations that have a negative impact on the system operation. Note that this takes at most a handful of pruning cycles.

As can be seen in Table 2, when we combine our original prefetch insertion algorithm with a pruning step ("Pruned Prefetch"), we get a much more consistent result. This greatly improves the performance of the prefetching algorithm, providing an overall 52% reduction in reconfiguration overhead when compared to the base case of no prefetching. While this is not nearly as good as the 89% improvement suggested by the Optimal Prefetch technique, it is important to realize that the Optimal Prefetch numbers may not be achievable by any static configuration prefetch algorithm. With the algorithm described here, we are capable of providing a significant reduction in the reconfiguration overhead of reconfigurable systems. As shown in Table 3, this speedup has a direct impact on the runtime of the reconfigurable system, providing a 10% reduction in overall runtime over the case of no prefetching.

7 Conclusions

In this paper we have introduced the concept of configuration prefetch for reconfigurable systems. By adding instructions into the code of an application, configurations for a reconfigurable coprocessor can be loaded in advance. This allows the overlapping of computation and reconfiguration, reducing the reconfiguration overhead of reconfigurable systems. We have also developed an algorithm which can automatically determine the placement of these prefetch operations, avoiding burdening the user with the potentially difficult task of placing these operations by hand. Finally, we have developed the Optimal Prefetch technique, which provides a bound on the potential improvement realizable via configuration prefetch. The results indicate that these techniques can reduce the reconfiguration overhead of reconfigurable systems by more than a factor of two, which will have a direct impact on the performance of reconfigurable systems.

We believe that such techniques will become even more critical for more advanced reconfigurable systems. When one considers

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Benchmark	Latency	Basic Prefetch	Pruned Prefetch	Optimal Prefetch
Go	10	82.4%	80.8%	76.4%
	100	89.5%	85.1%	77.6%
	1,000	100.3%	93.8%	90.7%
	10,000	118.5%	98.7%	97.1%
Compress	10	87.4%	87.0%	86.3%
	100	97.9%	97.9%	96.5%
	1,000	98.2%	98.2%	97.3%
	10,000	119.5%	92.1%	84.5%
Li	10	79.2%	78.7%	74.1%
	100	92.6%	89.2%	79.6%
	1,000	134.3%	99.9%	99.8%
	10,000	99.1%	99.1%	98.6%
Perl	10	83.8%	81.9%	75.9%
	100	90.5%	88.9%	80.1%
	1,000	111.6%	92.6%	82.0%
	10,000	99.9%	99.9%	99.9%
Fpppp	10	79.2%	78.9%	77.6%
	100	80.0%	80.0%	76.3%
	1,000	84.0%	72.2%	72.0%
	10,000	205.9%	100.0%	99.5%
Swim	10	84.4%	84.4%	81.1%
	100	106.7%	99.8%	99.7%
	1,000	293.3%	99.5%	99.5%
	10,000	1732.8%	89.3%	88.8%
Cumulative	10	82.7%	81.9%	78.4%
	100	92.5%	89.9%	84.5%
	1,000	124.0%	92.2%	89.6%
	10,000	192.0%	96.4%	94.5%
	All	116.2%	89.9%	86.6%

Table 3. Relative performance numbers for different prefetch techniques. The numbers represent the ratio of the total runtime (execution plus reconfiguration time) under the specified prefetch technique to the delay with no prefetching. "All" is the average of all benchmarks at all reconfiguration delays considered.

techniques such as partial Run-Time Reconfiguration [Hutchings95] or multiple contexts [Bolotski94], this greatly increases the amount of computation available to overlap with the reconfiguration, since prefetching can be overlapped with other computations in the reconfigurable logic. We plan to explore the application of prefetching to such advanced systems in our future work.

Acknowledgments

This research has been sponsored in part by a grant from the Defense Advanced Research Projects Agency, and a grant from the National Science Foundation.

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Ex. 1010, p. 344 of 399

Electronic Acknowledgement Receipt	
EFS ID:	3806167
Application Number:	10869200
International Application Number:	
Confirmation Number:	5929
Title of Invention:	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
First Named Inventor/Applicant Name:	Daniel Poznanovic
Customer Number:	25235
Filer:	William J. Kubida/Julie Lange
Filer Authorized By:	William J. Kubida
Attorney Docket Number:	SRC028
Receipt Date:	19-AUG-2008
Filing Date:	16-JUN-2004
Time Stamp:	17:39:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		DOC054.PDF	60647 9ad95e65d8c889ad17b6a787bb23c023e5a2d777	yes	4

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	Information Disclosure Statement (IDS) Filed (SB/08)	2	4		
Warnings:					
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2	Foreign Reference	DOC052.PDF	52578 483c68d61cdf9d33c70d3647c09b2e80a5c1d15d	no	4
Warnings:					
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3	NPL Documents	DOC055.PDF	233575 f36a0ebb84e8d70d3ca57a5115fcbde50f58ee04	no	10
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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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PATENT
EFS-Web
Attorney Docket No. SRC028
Client/Matter No. 80404.0033.001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200 Application of: Daniel Poznanovic, David E. Caliga, and Jeffrey Hammes Filed: June 16, 2004 Attorney Docket No. SRC028 For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	Art Unit: 2186 Confirmation No.: 5929 Examiner: THOMAS, Shane M. Customer No.: **25235**

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.97

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.97(i), please place the attached Form 1449 and the enclosed copy of the listed non-patent reference in the above-referenced file. In submitting these references, no representation is made or implied that the references are or are not material.

This Information Disclosure Statement is filed with no request for consideration of this reference. Accordingly, no fee is believed due. However, any fee associated herewith may be charged to Deposit Account No. 50-1223.

Respectfully submitted,

3 September 2009
Date

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\\\CS - 080404/000033 - 117744 v1

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	10869200
	Filing Date	2004-06-16
	First Named Inventor	Daniel Poznanovic
	Art Unit	2186
	Examiner Name	Thomas, Shane M
	Attorney Docket Number	SRC028

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10869200
	Filing Date	2004-06-16
	First Named Inventor	Daniel Poznanovic
	Art Unit	2186
	Examiner Name	Thomas, Shane M
	Attorney Docket Number	SRC028

	1	Japanese Office Action for JPN application no. 517452/2006, English translation mailed June 16, 2009, pgs. 24.	☐
	2	NAKAZATO Gaku et al., "Architecture and evaluation of OCHANOMIZ-1", Special Interest Group on Information Processing Society of Japan Report, Special Interest Group on Computer Architecture Report, Information Processing Society of Japan, September 20, 1993, IPSJ SIG Notes 93(71), pp. 57-64.	☐

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

Mailed June 16, 2009

NOTICE OF GROUNDS OF REJECTION

Patent Application No.	517453/2006
Drafting Date	June 9, 2009
Patent Office Examiner	Toshio MISAKA (4178 5B00)
Attorney	Mr. Hisao Fukami (et al.)
Applied Provision	Paragraph 2 of Article 29, Article 36

The present application is recognized as rejected on the following grounds. It is required that any remarks be submitted within three months from the date on which the present NOTICE was mailed.

GROUNDS

1. It is recognized that, because the invention described in Claim(s) of SCOPE OF CLAIMS FOR PATENT of the present application could have been invented readily by a person having ordinary knowledge in the field of the art to which the present invention pertains prior to the filing of the present application based on the invention as described in the following publication(s) distributed or the invention as made available to the public through electric telecommunication lines in Japan and/or foreign countries prior to the filing of the present application, a patent cannot be granted thereto under the provision of Paragraph 2 of Article 29 of the Patent Law.

2. It is recognized that the present application does not satisfy the conditions prescribed in Paragraph 6 (ii) of Article 36 of the Patent Law because of the defectiveness of the description in SCOPE OF CLAIMS FOR PATENT on the following points.

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3. It is recognized that the present application does not satisfy the conditions prescribed in Paragraph 6 (i) of Article 36 of the Patent Law because of the defectiveness of the description in SCOPE OF CLAIMS FOR PATENT on the following points.

REMARKS

[LIST OF CITED REFERENCES]

1. NAKAZATO Gaku et al., "Architecture and evaluation of OCHANOMIZ-1", Special Interest Group on Information Processing Society of Japan Report, Special Interest Group on Computer Architecture Report, Information Processing Society of Japan, September 20, 1993, IPSJ SIG Notes 93(71), pp.57-64

[Ground 1] (Paragraph 2 of Article 29)

[Claims] 1-8

[Cited Reference] 1

[Notes]

Cited Reference 1 discloses a processor system including a plurality of scalar processors, a main memory and an external agent configured by using an FPGA and having a Global Structure Pre-Fetch mechanism, wherein said Global Structure Pre-Fetch mechanism included in said external agent is configured to receive information about structure data (base address, size, stride, and the like) from the scalar processor, obtain data from the main memory based on the provided information and store the data in a local buffer memory (see, in particular, the descriptions in 2, 3.1, Figs. 1 and 2).

The scalar processor, the main memory and the local buffer memory in the invention disclosed in Cited Reference 1 correspond to "logic block," "first memory"

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and "second memory" in the invention claimed in claim 1 of the present application.

Furthermore, the Global Structure Pre-Fetch mechanism of the external agent in the invention disclosed in Cited Reference 1 corresponds to "data prefetch unit" in the invention claimed in claim 1 of the present application because the Global Structure Pre-Fetch mechanism operates independent of and in parallel with the scalar processor to prefetch the requested structure data.

Cited Reference 1 does not disclose the format of the structure data stored in the local buffer memory by the Global Structure Pre-Fetch mechanism included in the external agent. Those skilled in the art, however, would have readily arrived at configuring the structure data format on the local buffer memory to conform to a request from the logic block.

Therefore, the invention claimed in claims 1-8 of the present application would have been readily made by those skilled in the art, based on the invention disclosed in Cited Reference 1.

[Claims] 9-12
[Cited Reference] 1
[Notes]

The scalar processor, the main memory and the local buffer memory in the invention disclosed in Cited Reference 1 correspond to "logic block," "common memory" and "second memory" in the invention claimed in claim 9 of the present application.

Therefore, the invention claimed in claims 9-12 of the present application would have been readily made by those skilled in the art, based on the invention disclosed in Cited Reference 1.

[Claims] 13-19
[Cited Reference] 1

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[Notes]

The scalar processor and the main memory in the invention disclosed in Cited Reference 1 correspond to "computational unit" and "data access unit" and "memory" in the invention claimed in claim 13 of the present application.

Therefore, the invention claimed in claims 13-19 of the present application would have been readily made by those skilled in the art, based on the invention disclosed in Cited Reference 1.

[Ground 2] (Paragraph 6 (ii) of Article 36)

(1) Claim 1 recites "a reconfigurable processor that instantiates an algorithm as hardware," "computational data required by the algorithm," "configured to conform to needs of the algorithm," and "configured to match format and location of data in the second memory." Although these recitations specifies the processor, the data and the like in terms of their functions, properties and the like, their concrete structure is not clear.

The same is applied as well to the recitations "data required for computations by the algorithm," "configured to conform to needs of the algorithm" and "match format and location of data in the second memory" of claim 9.

The same is applied as well to the recitations "configured to conform to needs of an algorithm implemented on the computational unit" and "transfer only data necessary for computations by the computational unit" of claim 13.

(2) Claim 2 recites "transmits only portions of data desired by the data prefetch unit." Although, "data desired" specifies the data in terms of its function, property and the like, and it is unclear how it is obtained concretely.

The same is applied as well to "data desired" recited in claims 10 and 15.

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(3) Claim 4 recites "the data prefetch unit comprises at least one register from the reconfigurable processor." The relationship between "processor" and "at least one register" is unclear.

(4) It is unclear how "processor memory" recited in claim 6 is configured. It is noted that "on-processor memory" is found in claim 3. If "processor memory" is the same as "on-processor memory" recited in claim 3, the same term should be used.

The same is applied as well to "processor memory" and "microprocessor memory" recited in claims 7 and 8.

(5) A method recited in claim 13 is unclear in terms of the category of the claimed invention. In other words, the method recited in claim 13 includes having a hardware configuration of a computational unit, a data access unit and a data prefetch unit, as well as transferring data between respective components. It is unclear what performs each operation.

Therefore, the invention claimed in claims 1-19 is not clear.

[Ground 3] (Paragraph 6 (i) of Article 36)

(1) Claim 1 recites "first memory" and "second memory." It is unclear which components described in the best mode for carrying out the invention in the specification of the present application "first memory" and "second memory" correspond to.

The best mode for carrying out the invention describes "external memory" and "memory bank." As described below, it is unclear how these components are related to "first memory" and "second memory."

In other words, based on the recitation of claim 1 "places the retrieved computational data in the first memory" (the recitation "retrieves data from a second

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memory" is also found in paragraph 19), it can be understood that "first memory" corresponds to "memory bank" and "second memory" corresponds to "external memory."

On the other hand, based on the recitation of claim 1 "the data prefetch unit is configured to match format and location of data in the second memory" and the recitation of claim 6 "said second memory comprises a processor memory," it can also be understood that "first memory" corresponds to "external memory" and "second memory" corresponds to "memory bank."

(2) Claim 1 recites "retrieves only computational data required by the algorithm." The best mode for carrying out the invention in the specification of the present application describes a method for reading only data having a certain size into the processor and processing the data when it is located in the memory at regular spacings.

It can be understood that the method described in the best mode for carrying out the invention can be applied if an address where the data is located is known before executing the algorithm. It is not recognized that the method can be applied in the case of any algorithms.

Therefore, it cannot be said that what the detailed description of the invention discloses can be extended and generalized to the extent of the invention claimed in claim 1.

The same is applied as well to the recitation of claim 9 "read and write only data required for computations by the algorithm" and the recitation of claim 13 "conform to needs of an algorithm implemented on the computational unit and transfer only data necessary for computations by the computational unit."

(3) The operation recited in claim 5, "the data prefetch unit is disassembled when another program is executed on the reconfigurable processor," is not described in the best mode for carrying out the invention.

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Therefore, the invention claimed in claims 1-19 is different from that described in the detailed description of the invention.

If any grounds of rejection are newly found, the grounds of rejection will be noticed.

Record of Search for Prior Art Documents

* Searched Technical Field IPC G06F 9/30 - 9/38

Prior Art Documents

U.S. Patent No. 5941981

This record of search for prior art documents does not form any grounds of rejection.

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Architecture and Evaluation of OCHANOMIZ-1

1 Introduction

Many large-scale practical applications have portions where parallelism can be easily extracted, and portions where extraction of parallelism is difficult. In the portions where parallelism can be easily extracted by the coarse grain, the processing speed can be significantly increased if the number of processors for parallel execution is large enough. As a result, the portions where coarse-grain parallel processing is difficult to become a bottleneck. The use of fine-grain parallelism is essential in order to increase the processing speed also in the portions where parallel processing is difficult. However, close cooperation of a plurality of processors results in serious overhead for data transfer and synchronization between the processors. Reducing such overhead and configuring a system having mechanisms for efficient communication and synchronization between processors are the keys to the success of the fine-grain processing method. Moreover, support of an optimization compiler is essential to extract fine-grain parallelism, and tightly coupled parallel processing is convenient for this purpose. Various computers have been conventionally produced to efficiently implement efficient tightly coupled parallel processing [1, 2, 3, 4]. However, none of the mechanisms installed in these systems are not satisfactory enough.

This time, we produced OCHANOMIZ-1 (Omnipotent Concurrency Handling Architecture with Novel OptimMIZer-1), a general-purpose fine-grain parallel computer system using conventional high performance microprocessors as element processors. OCHANOMIZ-1 is a tightly coupled parallel computer system having low overhead synchronization mechanisms and communication mechanisms, and capable of efficient fine-grain parallel processing. An Elastic Barrier, a global structure pre-fetch mechanism, a memory-based data-driven synchronization mechanism, a mechanism for switching cache protocols on a page-by-page basis, and the like are installed as fine-grain parallel processing support mechanisms. A general-purpose large-scale parallel computer system is implemented by hierarchizing OCHANOMIZ-1 as a cluster.

Moreover, support of an optimization compiler is essential to extract fine-grain

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parallelism. As its name indicates, OCHANOMIZ-1 is produced to be used with a dedicated optimization compiler [5], and operates on the assumption that codes statically scheduled by the compiler are executed.

The overall architecture of OCHANOMIZ-1 will be described in Section 2. Three primary communication/synchronization mechanisms of the fine-grain parallel processing support mechanisms implemented on OCHANOMIZ-1 will be described in Sections 3, 4, and 5, respectively.

2 Structure of OCHANOMIZ-1

In the case of performing fine-grain parallel processing by computer systems formed by coupling conventional microprocessors, overhead becomes large and improvement in performance cannot be expected unless data communication and synchronization are supported. It is important to fabricate small-scale prototypes for performing fine-grain parallel processing, and to install experimental functions thereon to examine their effectiveness. The general-purpose fine-grain parallel computer OCHANOMIZ-1 uses conventional high performance microprocessors for communication and synchronization between processors with low overhead, thereby performing fine-grain parallel processing. Fig. 1 shows the overall structure of the system. Four VR4400MC (75 MHz) made by NEC [6, 7][1] are used as element processors. The processors are connected to each other via a shared bus. The system shared bus is a synchronization bus for performing split processing. Bus arbitration is performed by a distributed method. Address buses are 36-bit buses, data buses are 64-bit buses, and control lines for supporting snoop caches are included. VR4400MC includes a secondary cache controller in a chip, and supports invalidate type and update type snoop protocols. However, all the control of the secondary cache is performed by the processors, and inquiries regarding a cache status[2] for snooping, and the like are made via the processors, and thus, the response is very slow. Therefore, OCHANOMIZ-1 performs backmap management of the secondary cache in order to reduce the response time. OCHANOMIZ-1 has the same high-speed SRAM as that of the secondary cache for backmapping.

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Circuits called "external agents" are positioned between the processors and the bus. The external agents receive requests from the respective processors to send the requests to the bus, and return responses to the respective processors.

Cache pre-fetch, which is effective to hide latency, is not implemented in VR4400MC. Thus, OCHANOMIZ-1 has additional circuits for implementing a pre-fetch mechanism, which are controlled by the external agents.

A memory controller is positioned between a main memory and the bus. The memory controller refreshes the main memory, and accesses the memory so as to satisfy requests from the processors and a host. Moreover, the memory controller manages synchronization bits implemented by an SRAM. A global synchronizer is provided to implement high-speed communication and synchronization between the processors without using the shared bus. A barrier-type synchronizer and a shared register file are implemented as the global synchronizer. A host computer (a PC-AT compatible machine) is connected via a host interface. The host is used to configure an FPGA (Field Programmable Gate Array), to write data and programs to the main memory and caches, to reset the entire system, and to collect data.

The external agents, the memory controller, the global synchronizer, and the host interface are configured by using FPGA XC4010 (corresponding to 10,000gates) made by Xilinx. The operating clock[3] of this FPGA is a frequency-divided clock of the internal clock of the processors.

3 Global Structure Pre-Fetch Mechanism

In principle, in conventional parallel computers using cache memories, performance is derived by using locality of reference. Thus, such parallel computers are not good at performing processing having essentially no locality. OCHANOMIZ-1 also uses locality of reference in principle, but has a GSPF mechanism (a Global Structure Pre-Fetch mechanism) as a solution to the challenge of efficiently performing processing essentially having no locality. This section describes the GSPF mechanism, and shows expected performance at the time of design.

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3.1 Structure

Fig. 2 is a structural diagram of this mechanism. A scalar processor is connected to the system shared bus via a system called the "external agent." An original job of the external agent is to interpret a command[4] issued by the processor to meet the request of the processor by using the system shared bus. Since implementation of the external agent is left to the users, it is possible to include various mechanisms in the external agent. This GSPF mechanism is also installed by using the external agent.

Operation of the GSPF mechanism will be described below together with limitations upon its installation, and the like.

1. The processor transmits information on required structure data to a corresponding external agent. Various types of the structure are possible, but the structure is herein limited to constant strides. Thus, a base address, a size, and a stride are enough as the information on the structure[5]. Transfer of this information from the processor to the external agent is implemented by allocating a part of an address space to a register for communication with the external agent, and exchanging information. Note that the basic data size is 1 double word (64 bits) when using the GSPF mechanism.
2. Based on the provided information, the external agent obtains data from the main memory via the system shared bus to temporarily store the data in a local buffer memory. It should be avoided to cause the state where the external agent cannot answer the data request from the processor until the external agent obtains all the requested structure data. In this installation, information on how much data has been obtained is held in a counter, on the assumption that the order in which the processor requests data is the same as that in which the GSPF mechanism obtains data. Determination of whether data requested by the processor is already present in the local buffer memory or not is made based on a comparison with this counter. If the data is

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present in the local buffer memory, the external agent immediately sends the data to the processor. Otherwise, the external agent keeps the processor waiting until the data arrives.

3. The external agent immediately sends data from the local buffer memory to the processor when it receives a data request from the processor. The local memory buffer of the external agent is directly mapped in a part of the address space of the processor, and data exchange is implemented by reading/writing to/from that address.

This GSPF mechanism has similarities to Decoupled architectures [8], but is different therefrom in that it has no command stream for access processors for accessing data. Moreover, the Decoupled architectures necessarily use dedicated processors, while the GSPF mechanism has an advantage that it can use commercially available microprocessors. On the other hand, the GSPF mechanism is also similar to pre-fetch mechanisms having fetch buffers [9], but is different therefrom in that the pre-fetch mechanisms having fetch buffers require a code for every pre-fetch, while the GSPF mechanism requires no code for pre-fetch any more once setup is completed.

In the case of using the same structure data by a plurality of processors, if the plurality of processors separately access the data, the number of times the bus is used increases, causing a problem of bus contention. There is a possibility that the number of times the bus is used can be reduced if all the relevant processors fetch data flowing on the bus during data transfer. There is also a possibility that data can be supplied to the plurality of processors by one block transfer, if respective data required by the processors is included in data to be transferred in one block transfer, or the like, even if the same data is not used by the plurality of processors.

Thus, in the case where the GSPF mechanism is somewhat expanded so that the same structure data is used by a plurality of processors, a GSPF for fetching data was prepared for other processors[6] in addition to the normal GSPF. This is similar to a pre-fetch version of an all-read protocol in the MISC [10]. However, all-read in the MISC injects data directly to a cache, while, in the GSPF mechanism, the external agent

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temporarily manages data until it receives a data request from the processor.

The system bus protocol was expanded to support all-read in the GSPF mechanism, whereby the system bus was able to behave as if requests had issued from other processors. The system shared bus will now be described briefly. The system bus has signal lines for informing who issued a request via the bus, and there are lines respectively corresponding to the processors. In a normal request, a side issuing a request activates only the line corresponding to the request-issuing side itself, and a responding side responds by activating the same line as that was activated when it received the request. This is expanded so that a side issuing an all-read request activates also lines corresponding to other processors when issuing the request, whereby it is regarded that a plurality of requests were issued by a single request. Since the responding side activates the same signal lines as those that were activated when receiving the request, other processors can merely receive the response. In this case, although the plurality of processors were trying to issue the same request, the processors other than the first processor to issue the request need to only receive a response without issuing any request. If not all of the data in the received block is used, unnecessary data can be skipped when sending the data to the processors.

3.2 Performance Estimation

This section shows estimated performance of this mechanism. This section also shows a comparison with the case of using cache memories.

First, sample programs are shown in Fig. 3. For these programs, codes were generated at the maximum optimization level by using an optimization compiler[8] for R3000. As a result, loop unrolling was performed, and codes for executing four operations and load/store instructions corresponding to the four operations during one iteration were output. Code relocation was performed by using a code relocation back end of a compiler OP.1 [5][9] developed in our laboratory, and estimated performance was calculated based on the resultant codes. Performance of a unit stride and a constant stride with a stride of 4 when using sample program 1, and performance in the case of using all-read by product-sum calculation and the case of using no all-read when

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using sample program 2 were calculated, and also compared with corresponding performance in the case of caches.

Design values and some assumption for calculating estimated performance values are listed below. Actual values of the processors VR4400 [7] used in OCHANOMIZ-1 were used as values such as the number of clocks required to execute an instruction.

- Processors operate at 75 MHz.
- It is assumed that no cache miss is caused in an instruction stream.
- Both a primary cache and a secondary cache have a line size of 4 double words (32 bytes), and it takes 2 clocks to access the primary cache, and it takes 6 clocks to access the secondary cache.
- It takes 24 clocks to transfer data of one line from the memory to the secondary cache.
- On the bus, until one piece of data (64 bit width) can be supplied to the external agent in 2 clocks, and 6 clocks are required to fill the secondary cache with data of one line held in the external agent.

Table 1 shows a comparison between the case where the GSPF mechanism was used and the case where the cache memories were used, based on the above design values (and some assumption). It may not be a fair comparison, since the same codes are used both in the case of using the caches and the case of using the GSPF mechanism and this can be disadvantageous rather to the caches. However, it is estimated that higher performance can be obtained by using the GSPF mechanism than by simply using only the caches.

4 Memory-based Data Driven Synchronization Mechanism

In fine-grain parallel processing, data communication between processors can occur frequently. Thus, it is important to reduce the overhead for data communication

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and synchronization associated therewith to a low level. Examples of synchronization mechanisms that have been conventionally used for producer/consumer synchronization include full/empty bits [11] of HEP, and an I-structure memory [12] that has been used in data driven computers and the like. However, such mechanisms have not been used in parallel computers using von Neumann processors as element processors. However, a mechanism [10] for efficiently processing producer/consumer synchronization, implemented by a combination of a snoop cache mechanism and a full/empty bit synchronization mechanism was proposed, and such performance has been increasingly expected also in von Neumann shared memory, shared bus mutiprocessors. When using such a mechanism, synchronization is performed in a data driven manner. Thus, there is an advantage that data communication and synchronization can be processed in an integrated manner, and no special means is required for synchronization, separately from data communication.

Such a data driven synchronization mechanism is introduced in OCHANOMIZ-1. A synchronization bit indicating full/empty is added to every word in the main memory, and synchronization is performed by the memory controller and the respective external agents of the processors. Moreover, in OCHANOMIZ-1, a mechanism for configuring FIFO queues is provided on the main memory. Each FIFO queue is configured by using a memory address as an identifier, and is shared by a plurality of processors by accessing the address as an identifier. Actual FIFO management is performed by the memory controller independently of the processors.

Data driven synchronization using the synchronization bits, a method for installing the mechanism for configuring the FIFO queues on the memory, and estimation of synchronization performance in OCHANOMIZ-1 will be described below.

4.1 Synchronization Bit Mechanism

The main memory of OCHANOMIZ-1 is divided into banks. A synchronization bit is added to every word in a memory of each bank. At present, each synchronization bit is 1 bit indicating the presence of data, but a high performance memory [13] can be implemented by expanding the synchronization bits. Each memory

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bank is associated with a memory controller. In addition to processing normal accesses, the memory controller controls the synchronization mechanism together with the external agents.

If the synchronization bits are added also to the caches to process the synchronization bits on the caches, efficient synchronization can be implemented by a combination with a snoop cache protocol [10]. However, for existing multiprocessors using processors having embedded caches, such as OCHANOMIZ-1, there are many difficulties in management of the synchronization bits on the caches. Thus, in OCHANOMIZ-1, the synchronization bits are added only to the main memory, and synchronization is not performed on the caches. Thus, this mechanism can be used in a region that is not cached, and synchronization and data communication are implemented by the memory controller and the external agents via the main memory.

When a read request is issued from a processor, the external agent of that processor holds an address of that request. The memory controller examines the synchronization bit of a corresponding word. If the synchronization bit is in FULL state, the memory controller responds to the request with data, but if it is in EMPTY state, the memory controller does nothing. The processor that issued the read request remains in a wait state until it receives data. The external agent of that processor detects a data response from the memory controller, or a write request to the target address from another processor. The external agent performs write detection by comparing an address of the write request on the bus with the address held in the external agent. When the response data arrives, the external agent receives the data, and sends the data to the processor. When detecting a write request, the external agent fetches write data directly from the bus during write operation to the memory, and sends the data to the processor.

When a write request is issued from a processor, the memory controller writes data into the memory, and rewrites the value of a corresponding synchronization bit with FULL state. At this time, as described above, if there is any processor that has been blocked by a read request to the same address which was issued before the write request, the external agent of the blocked processor fetches the data from the bus, and sends the

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data to the processor.

Fig. 4 shows an example of synchronization. Processor B and processor C have been blocked since they issued a read request before processor A writes data to address X. The external agents of processor B and processor C monitor the bus. If processor A writes data to address X, the external agents fetch the data from the bus, and send the data to the respective processors, whereby blocked processors B and C are restarted.

The synchronization bits are set to a value of either EMPTY or FULL, but EMPTY and FULL are not fixed to 0 or 1. A synchronization polarity bit [10] is included in a part of an address, and the correspondence between FULL/EMPTY and 0/1 is determined by the value of the synchronization polarity bit. Thus, reuse of the memory after being used for data communication can be implemented at low cost. Moreover, as access means, it is necessary to distinguish memory accesses for synchronization from normal memory accesses that does not relate to synchronization. Thus, these accesses are also distinguished by using a bit as a part of an address.

4.2 Memory FIFO Mechanism

Another function on the memory of OCHANOMIZ-1 is a function to configure FIFO queues. A total of eight FIFO queues are currently prepared. (A part of) a memory address is designated as an identifier of the FIFO queues. The processors can access the FIFO queues in the same manner as that of normal memory accesses, and an address to be accessed is an address used as an identifier. The FIFO queues are managed by the memory controller, and FIFOs are configured only in a region that is not cached. The memory controller has pointers to the respective FIFO queues, and manages the FIFOs by a ring buffer method.

When a read request to a FIFO queue is issued from a processor, the memory controller responds to the request with data if there is data in the queue, and does nothing if there is no data in the queue. At this time, the external agent of the processor that issued the read request detects if a data response has arrived or another processor has issued a write to the same address (i.e., a write to the same FIFO queue).

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If the external agent receives the data response from the memory, the external agent sends the data to the processor. However, if the external agent detects a write, the external agent issues a read request to the FIFO queue again. If there is a data write from a processor to a FIFO, the memory controller writes data to a corresponding FIFO. However, if the FIFO is filled with data, the memory controller retries the write.

4.3 Estimation of Synchronization Performance

In this section, performance of data driven synchronization using the synchronization bits in OCHANOMIZ-1 is estimated by a simple comparison with synchronization using synchronization variables by software. An example of performing one-word data communication between processor A and processor B (processor A writes data, and processor B reads the data) will be herein considered. Table 2 shows a performance comparison. The values of Table 2 were obtained on the assumption that it takes 6 clocks to access the secondary cache, and it takes 24 clocks to access the main memory as design values of OCHANOMIZ-1, and that the bus is always available.

Condition 1 is the case where processor A wrote data before processor B issued a read request. In this case, in the mechanism using the synchronization bits, only one memory access is required for data communication. However, in the case of using the synchronization variables, the main memory needs to be read for the synchronization variables, in addition to the memory access for data communication. Condition 2 is the case where processor B issued a read request first, and a write request from processor A occurred after the read request. It should be noted that, in this case, the time from the data write operation of processor A to completion of data communication was compared. In the mechanism using the synchronization bits, data being written to the memory by processor A is directly fetched from the bus. However, in the case of using the synchronization variables, it is necessary to access the memory after accessing the synchronization variables. In this case, it is assumed that the synchronization variables have been cached, and an update type snoop protocol is used. In the case of using an invalidate type protocol, an access to the main memory is required also to access the

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synchronization variables.

Note that the comparison was herein made in terms of the access to the memory. However, it is considered that the difference therebetween is further increased if waiting due to checking for establishment of synchronization, bus arbitration, and the like are considered.

5 Global Synchonizer

Shared memory, shared bus type multiprocessor systems perform data communication by using shared variables, but the overhead is generated by an increase in memory accesses, a waiting time for acquiring the bus, and the like. Although OCHANOMIZ-1 has a global structure pre-fetch mechanism, and a memory-based data driven synchronization mechanism, the performance of these mechanisms can be degraded more than expected if contention occurs in a system shared bus. Thus, OCHANOMIZ-1 is provided with hardware that enables direct data exchange with each processor, and a mechanism using this hardware was also implemented. A Global Synchronizer (GS) is a mechanism for supporting high-speed communication and synchronization between processors without using a shared bus. As shown in Fig. 5, the GS is connected to each external agent via an 8-bit data bus.[10] By efficiently using these buses, the Elastic Barrier and the shared register file was implemented with low overhead.

5.1 Elastic Barrier

A barrier type synchronization mechanism is a relatively light synchronization mechanism in which all the shreds that belong to the same process queue simultaneously, and the hardware thereof can be relatively easily configured. The Elastic Barrier [14] is capable of performing synchronization with no overhead if the order in which synchronization is generated can be statically determined in a generalized barrier type synchronization mechanism. One of objects of OCHANOMIZ-1 is to install this Elastic Barrier to examine its effectiveness for applications. Since a prototype had a small-scale structure having four processors, the processors were intensively managed

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by using the GS, instead of providing synchronization controllers for the respective processors. Since the GS and the processors cannot directly exchange data with each other, the external agent of each processor has three counters (acknowledgement, advance notice, and establishment counters) required for the Elastic Barrier to implement faster synchronization. Processes that can be processed in the external agent are processed in the external agent, and a response is returned to the corresponding processor. Thus, the GS operates to mask synchronization signal lines and synchronization mask registers which are indicated by each processor, to detect establishment of synchronization conditions, and to return Acknowledgement. There are two mask registers so as to enable simultaneous barrier synchronization of two groups. Each external agent operates to increment and decrement the three counters according to the kind of synchronization information, to request activate/negate the synchronization signal lines for SL of the GS, and to allow the corresponding processor to perform continuous execution.

Regarding the relationship between instructions issued by the processor and the Elastic Barrier, the Elastic Barrier is implemented by regarding a LOAD instruction to a specific address provided by the processor as synchronization information in the case of RREQ, and by regarding a STORE instruction to the specific address as synchronization information in the case of APRV and PRRE.

Since functions are implemented by the FPGA, the external agents and the GS are rewritten with a normal barrier, a Fuzzy Barrier [15], a FIFO queue type Elastic Barrier [16], whereby their respective effectiveness can be examined.

5.2 Multiport Shared Register File

VR4400MC supports invalidate type and update type snoop cache protocols. However, this imposes a large load on the external agents and the shared bus, and in order to efficiently operate the processors, it is convenient if there is a mechanism capable of easily performing data communication. In addition to the barrier-type synchronization mechanism, the GS is provided with a multiport shared register file that can be accessed by the processors with no delay.

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The shared register file has the following two characteristic functions.

- To always enable read operation by the four processors.
- To perform exclusive control regarding write operation.

There are a total of sixteen 32-bit shared registers[11]. In a prototype machine, since the data buses between the GS and the external agents are only 8 bits buses, data larger than 1 byte needs to be divided into a plurality of parts for transmission.

An actual (as viewed from the external agents) communication protocol is as follows since the number of data buses and the number of control buses are small.

Read $\overline{CS}$ is asserted, and read, the data size, and the register are designated by the data bus. Data is read unless $\overline{Wait}$ is asserted. $\overline{CS}$ is returned.

Write $\overline{CS}$ is asserted, and write, the data size, and the register are designated by the data bus. Write data is sent to the data bus unless $\overline{Wait}$ is asserted. $\overline{CS}$ is returned.

Not only simple read/write operations, but also indivisible instructions for the shared variables, such as "Test-and-Set," can be implemented with no overhead by using the shared register file. A processor that successfully "Tested" a certain shared variable enters a critical section, that is, can receive data on the data bus, and thus, can continue the processing. The GS "Sets" the shared variable from 0 to 1 hardware-wise, and a processor that failed to read 0 receives 1 (lock failure) on a control signal line.

5.3 Performance Estimation

Table 3 shows estimated performance when the Elastic Barrier and the multiport shared register file were implemented by the GS. It is herein assumed that the parameters have the values as shown in Section 3, and that the FPGA operates at 1/4 of the internal clock of the processors. Only 2 clocks [12] for write are required for APRV and PREQ of the Elastic Barrier. However, 12 clocks are required for RREQ since the instruction is issued from the processor to the external agent, and a response to the

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instruction is returned to the processor. In implementation by software, in the case of implementing the Elastic Barrier and the multiport shared register by shared counters, shared flags, and flags for each shred, at least 120 clocks are required since each processor increments and decrements the shared counters, and the last processor that reaches a barrier region inverts the shared flags (96 clocks), and then, each shred checks for a match with the flag.

It is assumed that the data size is 1 byte in read/write to a shared register. Provided that no read contention occurs, 16 clocks are required for read to a shared register, because the instruction is first issued from the processor to the external agent, data is then read from the GS, and the result is returned to the processor via the external agent. This value is the same even if there is a read contention to the same register. In the software, it takes four times as long as 24 clocks in the worst case, if read to the same address occurs simultaneously in the four processors. Provided that no write contention occurs, the write is completed in 2 clocks since the instruction need only be sent out of the processor. However, it takes 26 clocks in the worst case, if write to the same register occurs in the four processors. Write using the shared bus can be performed quickly (12 clocks) if a write buffer is used. However, it takes 96 clocks in the worst case, as in the case of the read.

Since "Test&Set" using the shared register file is a Load instruction, it takes only 16 clocks. In the software, the shared bus needs to be accessed two times, and thus, it takes at least 48 clocks[13] if the shared bus can be occupied during these accesses.

6 Conclusion

The structure of the general-purpose fine-grain parallel computer, OCHANOMIZ-1, was described above. OCHANOMIZ-1 is a small-scale multiprocessor system using conventional processors, and has a global structure pre-fetch mechanism, a memory-based data driven synchronization mechanism, and a global synchronizer, as mechanisms for supporting fine-grain communication and synchronization with low overhead.

At present, OCHANOMIZ-1 has been debugged, hoping to practically operate

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OCHANOMIZ-1 soon. Moreover, an optimization compiler for OCHANOMIZ-1, based on the use of the above synchronization mechanisms, is going to be completed. Henceforth, we would like to evaluate the effectiveness of OCHANOMIZ-1 architecture by executing various applications, which can be executed in parallel, on OCHANOMIZ-1, and measuring the performance.

[1] VR4000MC (50 MHz) is currently used for the reason of supply, but is not operated.

[2] The cache status includes "invalid," "clean exclusive," "dirty exclusive," "shared," and "dirty shared."

[3] In VR4400MC, the operating clock can be set to up to 1/16 of the internal clock.

[4] The commands are coded data read/write requests, and various coded processing requests for implementing snoop caches.

[5] In practice, information for designating an object for fetching data for all-read processing described below is also transferred.

[6] To be exact, "external agents" associated with those processors.

[7] To be exact, "each external agent," but description is herein given by using the processors.

[8] Since no optimization compiler for R4000 was currently on hand, we had to use an optimization compiler for R3000.

[9] OP.1 is currently capable of outputting no code using the GSPF mechanism.

[10] The data bus size could not be increased any more due to design limitations.

[11] Two of those are used for the Elastic Barrier.

[12] VR4400MC has a write buffer.

[13] It actually takes more time since this is the time required for bus transaction.

Fig. 1: Structural Diagram of OCHANOMIZ-1

Fig. 2: Structure of GSPF Mechanism

Fig. 3: Sample Programs

```
/* sample program 1 */
/* sample program 2 */
```


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Table 1: Expected Performance of GSPF Mechanism (MFLOPS)

Sample 1

GSPF mechanism

Caches

Unit stride

Stride 4

Sample 2

all-read used

No all-read used

Fig. 4: a synchronization example using synchronization bits

Table 2: Estimation of Performance of Synchronization Mechanism

Synchronization bits

Synchronization variables

Condition 1

Condition 2

Fig. 5: Global Synchronizer (GS)

Table 3: Estimated GS performance

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情報処理学会論文1999-01739-008
(1993. 8. 20)

お茶の水１号の構成と評価

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本研究室で開発中の汎用細粒度並列計算機お茶の水１号の概要を報告する。従来のバス結合型マルチプロセッサでは、低オーバーヘッドの同期・通信機構が備わっていなかったために、命令レベルの細粒度並列処理を効率よく行なうことは不可能であった。お茶の水１号では、要素プロセッサには市販の汎用高性能マイクロプロセッサを用いているが、外部の支援機構にはFPGAを用いているため、応用に適したさまざまな機構を実現することができ、細粒度並列処理の汎用テストベッドとすることができる。今回実現した機構には、1) オーバーヘッドの極めて少ない *Elastic Barrier*、2) メモリベースの同期・通信を融合したデータ駆動同期機構、3) 大規模な配列データをキャッシュ上の連続領域に効率良くフェッチする大域構造体先行フェッチ機構がある。本稿では、お茶の水１号の構造および上記の機構について述べ、細粒度並列処理における効果を考察する。

Architecture and evaluation of OCHANOMIZ-1

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We report the general-purpose fine-grain multiprocessor OCHANOMIZ-1. Conventional bus connected multiprocessors have no facilities to support light weight synchronisation nor communication. Therefore these machines cannot handle efficiently instruction level parallelism. OCHANOMIZ-1 has commercial high performance microprocessors as its processor elements and FPGA's to support fine grain parallel processing. These FPGA's enable us to implement various type of mechanisms fitting to applications. Our current implementation of fine grain supporting mechanisms are 1) *Elastic Barrier*, which provides processors' synchronisation with little overhead. 2) *Data Driven Synchronisation*, which unifies producer-consumer type data transfer and synchronisation. 3) *Global Structure Pre-Fetching Mechanism*, which efficiently transfers large array data (possibly with non-unit stride) into continuous cache lines. In this paper, the overall structure of OCHANOMIZ-1 and the implementation of these mechanisms are described. We also discuss the impact of these mechanisms on fine grain parallel processing.

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1　はじめに

多くの大規模実用アプリケーションは容易に並列度が抽出可能な部分と抽出困難な部分を含んでいる。粗粒度で容易に並列度抽出できる部分は並列実行するプロセッサの台数さえあれば、かなりのスピードアップが可能であるが、その結果として細粒度による並列化が困難な部分がボトルネックとなってしまう。この並列化の困難な部分に関しても高速化を達成するためには細粒度の並列性の活用が不可避である。しかしながら、複数のプロセッサが密に協調動作を行なえばプロセッサ間のデータ転送や同期のためのオーバヘッドが深刻になってくる。これらのオーバヘッドをいかに削減することができるか、いかに効率的なプロセッサ間通信・同期機構を備えたシステムを構築できるかが細粒度処理方式成功の鍵である。さらに細粒度の並列性の抽出には最適化コンパイラの支援が不可避であるが、そのためには密結合並列処理が都合がよい。これまでも効率的な密結合並列処理の実現のために数々な計算機が作成されてきた[1, 2, 3, 4]。しかしながら、これらのシステムに実装された機構は今一つ満足できないものであった。

今回我々は従来型の高性能マイクロプロセッサを要素プロセッサとして用いた汎用細粒度並列計算機システム お茶の水1号 (OCHANOMIZ-1: Omnipotent Concurrency Enabling Architecture with Novel OptiMIZer-1) を作成した。お茶の水1号は低オーバヘッドな同期機構や通信機構を装備し、効率の良い細粒度並列処理が可能な密結合並列計算機システムである。細粒度並列処理支援機構として、Elastic Barrier、大域順序先行フェッチ機構、メモリベースのデータ駆動同期機構、ページ単位でのキャッシュプロトコルの切替え機構などが実装されている。汎用大規模並列計算機システムはお茶の水1号をクラスタとして階層化することで実現される。

また細粒度の並列性の抽出には最適化コンパイラの支援が不可避である。お茶の水1号はその名の通り専用の最適化コンパイラ [5] を仮定しており、コンパイラで静的にスケジューリングされたコードが実行されることを前提としている。

以下では、2節でお茶の水1号全体のアーキテクチャについて述べる。3、4、5節ではお茶の水1号上に実現された細粒度並列処理支援機構のうち主な3つの通信・同期支援機構についてそれぞれ説明する。

2　お茶の水1号の構成

従来型のマイクロプロセッサを結合した計算機システムによって細粒度並列処理を行う場合、データの送信・同期に対する支援がされなければオーバヘッドが大きくなり性能向上が望めない。細粒度並列処理をする小規模のプロトタイプを作成し、その上に試験的な機構を実装し有効性を検証することが重要である。汎用細粒度並列計算機お茶の水1号は従来型の高性能マイクロプロセッサを用い、低オーバヘッドでプロセッサ間の通信・同期をおこない細粒度の並列実行する。システムの全体構成図を図1に示している。要素プロ

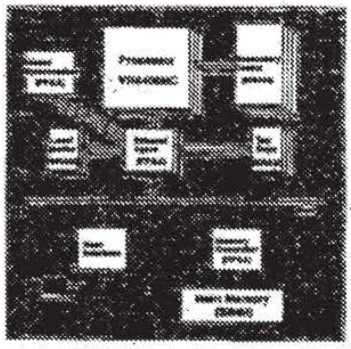

図1: お茶の水1号の構成図

セッサには NEC の VR4400MC(75MHz)[6]，7[1]を４台用いている。プロセッサは共有バスを介して互いに接続している。システム共有バスはスプリット処理を行なう同期バスであり、バスアービトレーションは分散方式で行なわれる。アドレスバスは 36bit、データバスは 64bit でスヌープキャッシュを支援する制御線を備えている。VR4400MC はチップ内部に２次キャッシュコントローラを内蔵しており、インバリデイト系及びアップデイト系のスヌーププロトコルをサポートしている。しかしながら、２次キャッシュの制御は全てプロセッサに委ねられており、スヌープのためのキャッシュの状態[2]の問い合わせ等はプロセッサを疲弊したものになるためにレスポンスが非常に遅い。そこでお茶の水１号ではレスポンスを高速化するために３次キャッシュのバックマップ管理を行なっている。バックマップ用として２次キャッシュと同じ高速 SRAM を装備している。

プロセッサとバスの間に外部エージェントと呼ばれる回路が位置しており、プロセッサからの要求を受けとりバスに要求を出したり、プロセッサにレスポンスを返したりする。

VR4400MC ではレイテンシ隠蔽に有効なキャッシュプリフェッチが実現されていない。そこでお茶の水１号ではプリフェッチ機構を実現するための付加回路が装備されており外部エージェントにより制御されている。

主メモリとバスの間にメモリコントローラがあり、主メモリのリフレッシュをしプロセッサやホストからの要求を満たすようにメモリアクセスをする。さらに SRAM により実現された同期ビットを管理している。プロセッサどうしが共有バスを使わずに高速に通信したり、同期を行うために大域同期機構がある。大域同期機構としてバリア型同期機構、共有レジスタファイルを実現している。ホストインタフェースを介してホストコンピュータ (PC-AT互換機) が接続されてい

[1]現在のところ実験の都合で VR4000MC(50MHz) を使っているが差がついていない。

[2]invalid, clean exclusive, dirty exclusive, shared, dirty shared がある。

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5。ホストはFPGA(Field Programmable Gate Array)のコンフィギュレーション、主記憶やキャッシュに対するデータやプログラムの書き込み、システム全体のリセット、データの収集のために使用される。

外部エージェント、メモリコントローラ、大域同期機構、ホストインタフェースはXilinx社のFPGA XC4010(10,000gates相当)を用いて構成されている。このFPGAはプロセッサ内部のクロックを分周したクロック[5]で動いている。

3　大域構造体先行フェッチ機構

従来のキャッシュメモリを用いた並列計算機では参照の局所性を利用して性能を引き出すことを原則としている。それゆえに本質的に局所性のない処理を苦手としている。本来の水1号も原則として参照の局所性を利用するが、本質的に局所性のない処理を効率良く処理するという問題に対する解答として大域構造体先行フェッチ機構(GSPF機構：Global Structure Pre-Fetch機構)を備えている。この節ではGSPF機構について説明を行なうと共に設計時の予定仕様を示す。

3.1　構成

図2は本機構の構成図である。スカラプロセッサが外部エージェントと呼ばれるシステムを介してシステム共有バスに接続されている。外部エージェントの本来の仕事はプロセッサが発行するコマンド[6]を解釈してシステム共有バスを使用してプロセッサの要求を満たすことである。外部エージェントの実現はユーザに任されているのでここに様々な機構を盛り込むことが可能となっている。本GSPF機構もこの外部エージェントを利用して実現される。

GSPF機構の動作を実現の際の制限などと併せて説明すると次のようになる。

1. プロセッサは用意してもらいたい構造体データに関する情報を外部エージェントに伝える。構造体としてはいろいろなものが考えられるが今回はロンスタントストライドに対応を絞ることにした。よって構造体に関する情報としてはベースアドレス、サイズ、ストライドの3つが分かれば十分である。[7]。プロセッサから外部エージェントへいかにしてこの情報を転送するかに関してはアドレス空間の一部を外部エージェントとの通信用レジスタに割当て情報のやり取りを行なうことで実現する。なおGSPF機構使用時のデータの基本サイズは1ダブルワード(64ビット)である。

2. 提供された情報をもとに外部エージェントはシステム共有バスを通じて、主メモリからデータを持ってきて一時的にローカルバッファメモリに格納しておく。要求されている構造体データを全て持ってくるまでプロセッサのデータ要求に答えられないという状況を避けなければならない。本実装ではプロセッサがデータを要求する順はGSPF機構がデータを獲得し先送りであるという仮定をおき、現在何処までデータを獲得できた

[5]VR4400MCでは16分周までが設定可能。
[6]データのread/write要求やスヌープキャッシュ実現のための様々な処理要求がコード化されたもの。
[7]実際には後で述べるall-read処理のためにデータを取り込ませる順序を指定するための情報も設定される。

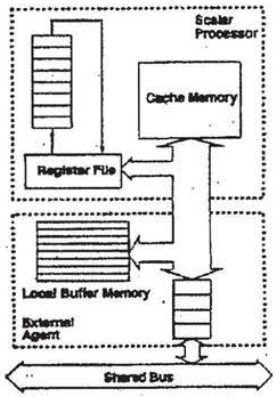

図2: GSPF機構の構成

かという情報をカウンタで保持することにした。プロセッサが要求したデータが既にローカルバッファメモリ内に存在するかどうかの判断はこのカウンタとの比較で行ない、もしデータがローカルバッファメモリ内に存在すれば即座にデータをプロセッサに受け渡し、存在しなければデータがやってくるまでプロセッサを待たせる。

3. プロセッサからデータの要求が来たら即座にローカルバッファメモリからデータをプロセッサに渡す。外部エージェントのローカルメモリバッファはプロセッサのアドレス空間の一部に直接マップされており データの受渡しはそのアドレスへのread/writeで実現されている。

とのGSPF機構はDecoupledアーキテクチャ[8]と似ている点も存在するが、データアクセスを行なうアクセスプロセッサのための命令流がない点で異なる。さらにDecoupledアーキテクチャではプロセッサは必然的に専用プロセッサを使用することになるが、GSPF機構の場合は市販のマイクロプロセッサを使用することができるという利点を備えている。また一方でフェッチバッファ付きのプリフェッチ機構[9]とも類似しているが、フェッチバッファ付きのプリフェッチ機構は毎回プリフェッチのためのロードを必要とするのに対して、GSPF機構は一度セットアップが済めば以後プリフェッチのためのコードは必要ない点で異なる。

同じ構造体データを複数のプロセッサで利用するという場合これらを別々にデータを取りにいったのではバスの使用回数が増えてバス競合が問題となる。これはデータ転送を行なっている最中に関係するプロセッサ全てがバス上に流れているデータを取り込めばバスの使用回数を激減できる可能性がある。また同じデータを使用しなくても1回のブロック転

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送分のデータ中にそれぞれのプロセッサが必要とするデータが含まれる場合などは１回のブロック転送で複数のプロセッサにデータを供給できる可能性がある。

そこでGSPP機構に多少の拡張を加えて同じ構造体データを複数のプロセッサで利用する場合は通常のGSPPとは別に他のプロセッサ[3]にもデータを取り込ませるGSPPを用意した。これはMISC[10]におけるall-readプロトコルのプリフェッチ版に類似しているが、MISCにおけるall-readが直接キャッシュにデータを注入するのに対し、GSPP機構ではプロセッサからのデータの要求が来るまで外部エージェントが一時的に管理する点が異なる。

GSPP機構でall-readサポートするためにシステムバスのプロトコルに拡張がなされ、あたかも他のプロセッサから要求を出したかのように振舞うことができるようになった。ここでシステム共有バスについて簡単に触れる。システムバスには調停バスを通じて要求を出したかを知らせる信号線があり、各プロセッサ[4]に対応した線が存在している。通常のリクエストでは要求を出す側は自分に対応した線のみをアクティブにして要求を出し、通事をする側は要求を受け取ったときにアクティブになっていた線と同じ線をアクティブにすることで通事をする。これを拡張して、all-readの要求を出す側が要求を出す際に他のプロセッサの分までアクティブにすることで一度のリクエストで複数個のリクエストを出したことにする。通事を返す側はリクエストを受け取った時と同じ信号線をアクティブにするので他のプロセッサ仕様に通事を受け取る だけでよい。この際、複数のプロセッサが同じリクエストを出そうとしていたわけであるが一番最初にリクエストを出せたプロセッサ以外はリクエストを出さずに通事だけを受け取るようにしなければならない。もしも受け取ったブロック中の全データを使用しない場合は、プロセッサに受け渡す時に不必要なデータをスキップすればよい。

3.2　性能見積り

本小節では本機構の予定性能を示す。同時にキャッシュメモリを使用した場合との比較も行なう。

先ず、図3にサンプルプログラムを示す。これらのプログラムに対してR3000用の最適化コンパイラ[5]を用いて最適化レベルを最大にしてコード生成を行なった結果、ループのアンロールが行なわれ１回のイテレーション中に４つの演算と４回分の演算に相当するロードストア命令が実行されるコードが出力された。これを基研究室で開発したコンパイラOP.1[6]のコード再配置バックエンドを用いてコードの再配置を行なったコードをもとに予定性能を算出した。サンプルプログラム１を用いてユニットストライド、ストライドが４のコンスタントストライドの性能、サンプルプログラム２を用いて積和演算でall readを使用した場合と使用しない場合の性能をそれに対応するキャッシュの場合との比較と併せて算出した。

以下に予定性能算出の際の設計値及び若干の仮定を列挙する。命令の実行にかかるクロック数などの数値はお茶の

[4]正確にはそれに相当している外部エージェントである。

[3]正確には外部エージェントであるがここではプロセッサとして扱う。

[5]調査時点でR4000用の最適化コンパイラが完成にほったのでやむを得ずR3000用の最適化コンパイラを使用した。

[6]OP.1は現在、GSPP機構を利用するコードを出力できない。

```
double a[N], b[N], c[N];
double s;
int i;

/* サンプルプログラム 1 */
for (i = 0; i < N; i++)
  a[i] = b[i] + c[i];

/* サンプルプログラム 2 */
s = 0.0;
for (i = 0; i < N; i++)
  s += a[i] * b[i];
```

図 3: サンプルプログラム

	サンプル1	
	ユニットストライド	ストライド4
GSPP機構	12.5	12.5
キャッシュ	7.1	1.8
	サンプル2	
	all-read 使用	all-read 使用しない
GSPP機構	45.3	37.5
キャッシュ	21.4	21.4

表 1: GSPP 機構予定性能 (MFLOPS)

水1号に採用されたプロセッサVR4400[7]の実際の値を使用した。

- プロセッサは75MHzで動作。
- 命令ストリームによるキャッシュミスは起こらないとする。
- 1次キャッシュ、2次キャッシュのラインサイズはどちらも4ダブルワード(32バイト)であり、1次キャッシュへのアクセスには2クロック、2次キャッシュへのアクセスには6クロックを要する。
- メモリから2次キャッシュへの1ライン分のデータ転送に36クロック。
- バス上では2クロックに1データ(64ビット幅)を外部エージェントに供給でき、外部エージェントが保持する1ライン分のデータを2次キャッシュにフィルするのに6クロックを必要とする。

表1は上記設計値（及び若干の仮定）をもとにして、GSPP機構を使用した場合とキャッシュメモリを使用した場合との比較を行なったものである。キャッシュを使用した場合もGSPP機構を使用した場合も同じコードを使用しているのでどちらかと言えばキャッシュに不利に働いている可能性もありフェアな比較とは言えないかもしれないが、GSPP機構の方が単純にキャッシュのみを使用した場合よりも性能が出せる予定である。

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4　メモリベースのデータ駆動的同期機構

細粒度並列処理ではプロセッサ間のデータ通信が頻繁に起こりうるため、データ通信とそれに伴う同期のオーバヘッドを小さく抑えることが重要である。従来、生産者消費者型の同期のために利用されてきた同期機構としては HEP の full/empty ビット [11] やデータ駆動計算機等で用いられてきた I-structure メモリ [12] があげられる。しかし、フォンノイマン型のプロセッサを要素プロセッサとする並列計算機ではこれまでこのような機構は用いられてこなかった。しかし、スヌープキャッシュ機構と full/empty ビットによる同期機構を組み合わせた生産者消費者型の同期を効率良く処理する機構 [10] が提案されるに至り、フォンノイマン型の共有メモリ共有バスマルチプロセッサにおいてもその性能が期待されるようになってきた。このような機構を用いると同期がデータ駆動的に行なわれるため、データ通信と同期を統合的に処理でき、データ通信と仕別の同期のための特別な手段を必要としないという利点がある。

お茶の水１号にはこのようなデータ駆動的同期機構が導入されている。メインメモリにはワード毎にデータの full/empty を示す同期ビットが付加されており、同期はメモリコントローラおよび各プロセッサの外部エージェントによって行なわれる。また、お茶の水１号にはメインメモリ上に FIFO キューを構成する機構が搭載されている。この FIFO キューはメモリアドレスを識別子として構成されるものであり、複数のプロセッサが識別子であるアドレスにアクセスすることによりその FIFO キューが共用されるものである。実際の FIFO の管理はメモリコントローラによってプロセッサとは独立に行なわれる。

以下ではお茶の水１号における同期ビットによるデータ駆動同期およびメモリ上に FIFO キューを構成する機構の実装方式および同期性能の見積もりを行なう。

4.1　同期ビット機構

お茶の水１号のメインメモリは各バンクにわかれている。各バンクのメモリにはワード毎に同期ビットが付加されている。現状では同期ビットはデータの存在を示す１ビットであるが、同期ビットの拡張により高機能メモリ [13] を実現することも可能になる。各メモリバンクにはメモリコントローラが付随されている。メモリコントローラは通常のアクセスの処理を行なうほか、同期機構の制御を外部エージェントと共に行なう。

同期ビットをキャッシュ上にも付加し、同期ビットの処理をキャッシュ上で行なうようにすれば、スヌープキャッシュプロトコルとの組合せで効率の良い同期が実現できる [10]が、お茶の水１号のように既存の内蔵キャッシュをもつプロセッサを利用したマルチプロセッサではキャッシュ上での同期ビットの管理には困難な点が多い。そこで、お茶の水１号ではメインメモリのみに同期ビットが付加されており、キャッシュ上で同期を行なうような機構にはなっていない。このため本機構はキャッシュされない領域で利用可能であり、メモリコントロークと外部エージェントによりメインメモリを介した形で同期、データ通信が実現されるようになっている。

リードリクエストがプロセッサから発行されるとそのプロセッサの外部エージェントはそのリクエストのアドレスを保持する。メモリコントローラは該当するワードの同期ビットを調べ、FULL 状態であればデータのレスポンスを行なうが、EMPTY 状態であれば何もしない。リードリクエストを発行したプロセッサはデータを受け取るまで待ち状態にはいる。そのプロセッサの外部エージェントはメモリコントローラからのデータのレスポンスか、あるいはターゲットアドレスへの別のプロセッサからのライトリクエストの検出を行なう。ライトの検出は外部エージェントがバス上のライトリクエストのアドレスと保持しているアドレスとの比較によっておこなう。外部エージェントはレスポンスデータが到着したときはデータを受け取りプロセッサに送り、ライトを検出したときはメモリへのライト中にメモリに書き込むデータをそのままバスから取り込んでプロセッサに送る。

プロセッサからライトリクエストが発行されるとメモリコントローラはデータのメモリへのライトとともに対応する同期ビットの値を FULL 状態に書き換える。このとき上記のとおりに、先に同じアドレスへのリードリクエストによりブロックしているプロセッサがあれば、そのプロセッサの外部エージェントはデータをバスから取り込みプロセッサにデータを送る。

同期の一例を図4に示す。プロセッサ B とプロセッサ C はプロセッサ A がアドレス X にデータを書く前にリード要求をし、ブロックされている。プロセッサ B とプロセッサ C の外部エージェントはバスを見張っており、プロセッサ A がアドレス X にデータの書き込みをすると、外部エージェントはそのデータをバスから取り込んでプロセッサに渡すことで、ブロックしていたプロセッサ B とプロセッサ C は再起動される。

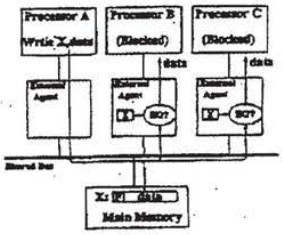

図 4: 同期ビットを使用した同期の例

同期ビットは EMPTY あるいは FULL のどちらかの値をとることになるが、それぞれ 0 か 1 のどちらかに固定してはいない。アドレスの一部に同期極性ビット [10] をもたせ、極性ビットの値によって FULL/EMPTY と 0/1 の対応を決めている。これにより、データ通信に使い終った後のメモリの再使用が低コストに実現できる。また、アクセス手段として通常の同期とは無関係のメモリアクセスと区別する必要があるため、これもアドレスの一部のビットを使って区別している。

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4.2 メモリFIFO機構

お茶の水1号のメモリ上のもう一つの機能としてFIFOキューを構成する機能がある。FIFOキューは現在は全部で8本用意してある。このFIFOキューはメモリアドレス（の一部）を識別子として指定される。プロセッサからのアクセスは通常のメモリアクセスと同様でよく、アクセスするアドレスは識別子であるアドレスであればよい。FIFOキューの管理はメモリコントローラによって行なわれ、FIFOはキャッシュされない領域においてのみ構成される。メモリコントローラは各FIFOキューに対するポインタを持っており、FIFOの管理をリングバッファによる方式で行なっている。

プロセッサからのFIFOキューへのリードリクエストが起こると、メモリコントローラはキューにデータがあればデータのレスポンスを行ない、データがなければ何もしない。このときリードリクエストを発行したプロセッサの外部エージェントはデータのレスポンスがきたか、他のプロセッサから同じアドレスに対するライト（すなわち同じFIFOキューへのライト）が発行されたかの検出を行なう。外部エージェントはメモリからデータが返送されたときはそのデータをプロセッサに渡すが、ライトの検出をしたときは再度FIFOキューへのリード要求を発行する。プロセッサからFIFOへのデータの書き込みがあると、メモリコントローラはデータを該当するFIFOに書き込むが、もしFIFOがデータで満たされていた時はそのライトをリトライさせるようにしている。

4.3 同期性能の見積もり

ここではお茶の水1号の同期ビットを使用したデータ駆動同期の性能の見積もりをソフトウェアによる同期変数を用いた同期との結果を比較によっておこなう。例としてプロセッサAとプロセッサBの間で1ワード分のデータ通信を行なう場合（プロセッサAがデータを書き、プロセッサBがそのデータを読む）を考える。性能の比較を表2に載せる。表2の値を求めるにあたっては、お茶の水1号の設計値として2次キャッシュアクセスに6クロック、メインメモリアクセスに34クロックかかるものとし、仮定としてバスは常に空いているものとした。

状況1はプロセッサAが、プロセッサBがリードリクエストを発行する前にデータの書き込みを行なった場合である。この場合、同期ビットを用いる機構ではデータ通信のための一回のメモリアクセスのみでよいが、同期変数を用いる場合ではデータ通信以外に同期変数のためにもメインメモリを読みにいかなければならない。状況2はプロセッサBが先にリードリクエストを発行し、プロセッサAからのライトリクエストが後から起こった場合である。ただし、この場合はプロセッサAがデータのライトを行なった時点を基準にし、それからのデータ通信完了までの時間の比較を行なったものである。同期ビットを用いる機構ではプロセッサAがメモリに書き込んでいるデータをバスから直接取り込むのに対し、同期変数を用いる場合では最初に同期変数をアクセスし、その後でメモリにアクセスしにいかなければならない。このとき同期変数はキャッシュされているものとし、スヌーププロトコルとしてファンデイト型を用いたものとしている。インバリデイト型のプロトコルを用いた場合は同期変数のアクセスのためにもメインメモリへのアクセスが必要になる。

	同期ビット	同期変数
状況1	34クロック	46クロック
状況2	4クロック	30クロック

表2: 同期機構の性能の見積もり

なお、ここでの比較はメモリへのアクセスのみに注目したものであったが、同期成立のチェックやバスのアービトレーションによる待ちなどを考慮すればさらに両者の差は広がるものと考えられる。

5 大域同期機構

共有メモリ共有バス型のマルチプロセッサシステムでは共有変数を用いてデータ通信を行うがメモリアクセスの増大やバス獲得の待ち時間などによりオーバヘッドが生じてしまう。お茶の水1号も大域縮退先行フェッチ機構、メモリベースのデータ駆動的同期機構を装備しているが、いずれもシステム共有バスに競合が発生した時には性能が予想以上に悪くなることが考えられる。そこでお茶の水1号では各プロセッサと直接データのやりとりができるようなハードウェアをもうけて、それを利用した機構も実現した。大域同期機構(GS: Global Synchroniser)は共有バスを介さないでプロセッサ間の高速な通信・同期を支援するための機構である。図5のように1つの外部エージェントとは8bitのデータバスでつながっている。[10]これらのバスを効率的に利用して低オーバヘッドでElastic Barrier、共有レジスタファイルを実現した。

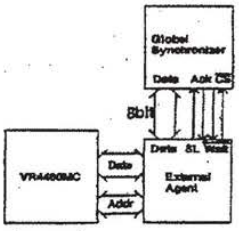

図5: 大域同期機構(GS)

5.1 Elastic Barrier

バリア型同期機構は同じプロセスに属するすべてのシュレッドが同時に待ち合わせる比較的軽い同期機構でかつハードウェアとしては比較的簡単に構成できる。Elastic

[10]データバスは設計時の制約によりこれ以上増やすことはできなかった。

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Barrier[14]は一般化されたバリア型同期機構で同期の発生順序が静的に決定できればオーバヘッドなしに同期をとることができるものである。お茶の水1号の目的の1つとしてこのElastic Barrierを実装してアプリケーションに対する有効性を検証することにある。プロトタイプはプロセッサ4台と小規模構成なので同期コントローラをプロセッサ毎にもつのではなく、GSを用いて集中的な管理をすることにした。GSとプロセッサは直接データを受け渡しできないので、より高速な同期を実現するためにElastic Barrierに必要な3つのカウンタ(承認、予告、成立カウンタ)はGSプロセッサの外部エージェントがもっている。外部エージェント内で処理できるものは処理してプロセッサにレスポンスを返すことにした。したがってGSの動作としては各プロセッサが出した同期信号線と同期マスクレジスタとのマスクをとり同期条件の成立を検出してAcknowledgmentを返すことになる。マスクレジスタは2個あり、2組のグループが同時にバリア同期を張れるようにした。外部エージェントの働きとしては、同期情報の複製による3つのカウンタの増減、GSのSLICに対する同期信号線のactivate/negateの要求、プロセッサに対する割込実行の許可になる。

プロセッサの出す命令とElastic Barrierの関係は、RREQはプロセッサの出した特定のアドレスに対するLOAD命令、APRV, PREQは特定のアドレスへのSTORE命令を同期情報とみなすことにより Elastic Barrierを実現している。

FPGAによって機能を実現しているために外部エージェントとGSの中身を通常のバリア、Fuzzy Barrier[15]、FIFOキュー方式のElastic Barrier[16]に容易に変えてそれぞれの有効性を調べることができる。

5.2 マルチポート共有レジスタファイル

VR4400MCはインバリデイト系とアップデイト系のスヌープキャッシュプロトコルをサポートしているが、外部エージェントと共有バスに対する負担は大きくプロセッサをさらに効率良く動かすためには簡単にデータの通信が行える機構があると便利である。バリア型同期機構の他にプロセッサが逐次なしにアクセスできるマルチポート共有レジスタファイルをGSに持たせることにした。

共有レジスタファイルの機能の特徴としては以下の2点ある。

- 4台のプロセッサによる読み出しを常に可能にする。
- 書き込みに対しては排他制御する。

共有レジスタは32bitで全部で16本ある[11]。試作機ではGSと外部エージェント間のデータパスが8bitしかないので1バイトより大きなデータに対しては複数回に分けて転送する必要がある。

実際の(外部エージェントから見た)通信プロトコルはデータ、コントロールパスとも本数が少ないので以下のようになっている。

read $\overline{CS}$をアサートし、データパスでread、データサイズ、レジスタ指定をする。$\overline{Wait}$がアサートされてなければデータを読み出す。$\overline{CS}$を戻す。

write $\overline{CS}$をアサートし、データパスでwrite、データサイズ、レジスタ指定をする。$\overline{Wait}$がアサートされてなければ書き込むデータをデータパスに送る。$\overline{CS}$を戻す。

単純なread/writeの操作だけではなくTest-and-Setなどの共有変数に対する不可分命令も共有レジスタファイルを利用してオーバヘッドなしで実現できる。ある共有変数をTestできたプロセッサはクリティカル・セクションに入り、つまりデータパスにデータを受けとることができるのでその書き込みを続けることができる。GSがハード的に共有変数を0から1にSetし、0を読み出すのに失敗したプロセッサはコントロール信号線に1(ロック失敗)を受けとることになる。

5.3 性能見積り

GSによってElastic Barrierとマルチポート共有レジスタファイルを実現した時の予測性能が表3である。パラメータは2節の値に従っているとし、FPGAはプロセッサ内部のクロックを4分周したクロックで動いているとする。Elastic BarrierのAPRVとPREQについてはwriteの2クロック[12]で済むが、RREQについてはプロセッサから外部エージェントに出てたのレスポンスがプロセッサに戻るので12クロックかかる。ソフトウェアによる実現は共有カウンタ、共有フラグ、各シュレッド毎のフラグで実現する場合、各プロセッサが共有カウンタを増加し最後にバリア領域に脱退したプロセッサが共有フラグを反転した後[96クロック]、各シュレッドがフラグとの一致を確認するので120クロックはかかってしまう。

共有レジスタに対するread/writeはデータのサイズが1バイトであるとした。共有レジスタに対するreadは競合が起こらない仮定では、プロセッサから外部エージェントに出た後GSからデータを読み出しその結果が外部エージェントを経てプロセッサに戻るので16クロックかかる。この値は同一レジスタに対する読み出しが競合しても同じである。ソフトウェアでは同一アドレスに対するreadが4台で同時に起こると最悪の場合で24クロックの4倍の時間がかかる。writeは競合が起こらない仮定ではプロセッサの外に命令が出ればよいので2クロックで済む。しかし同一レジスタに対する書き込みが4台で起こった場合は最悪で26クロックかかる。共有バスを利用してのwriteはライトバッファーを利用すれば速い(12クロック)が、最悪の場合はreadの場合と同様96クロックかかる。

共有レジスタファイルを使用したTest&Setは Load命令なので16クロックで済む。ソフトウェアでは共有バスを2回アクセスしなければならないのでこの間占有できるとすれば48クロック[13]はかかる。

6 まとめ

汎用細粒度並列計算機お茶の水1号の構成について説明した。お茶の水1号は従来型のプロセッサを使用した小規模のマルチプロセッサシステムであり、低オーバヘッドで細粒度

[11] その内2つはElastic Barrierのために使用される。

[12] VR4400MCはライトバッファを持っている。

[13] これはバストランザクションにかかる時間なのでCPU内部ではもっとかかる。

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操作	ソフトウェア	GS
Elastic Barrier	120(96)	2-12
read	24-96	16
write	12-96	2-26
TestSet	48	16

表 3: GS の予定性能

の通信・同期を支援する機構として大域精密体先行フェッチ機構、メモリベースのデータ駆動的同期機構、および大域同期機構を搭載している。

現在のところお茶の水１号はデバッグ中であり、近々始動を目指している。また、お茶の水１号のための上記同期機構の使用を前提とした最適化コンパイラが完成される予定である。今後の課題として、並列実行可能なさまざまなプログラムをお茶の水１号上で実行し、性能を測定することにより、お茶の水１号のアーキテクチャの有効性を評価していきたい。

謝辞

お茶の水１号の作成にあたりチップを供給していただいた日本電気株式会社と FPGA に関する環境を支援していただいた日本ダイリンクス社に感謝いたします。

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This is not an USPTO supplied IDS fillable form					
2	Foreign Reference	DOC021.PDF	801918 5e89790c17d3b3e38524e471f92e0f7f9ccec5b0	no	24
Warnings:					
Information:					
3	NPL Documents	DOC022.PDF	355915 078d6c5f1e50cbec5b6df5a5130a80a6b56e2848	no	8
Warnings:					
Information:					
			Total Files Size (in bytes):	1253856	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/869,200 Filed: June 16, 2004 Attorney Docket No. SRC028 For: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE	Confirmation No.: 5929 Art Unit: 2186 Examiner: Thomas, Shane M. Customer No.: **25235**

TRANSMITTAL OF NOTIFICATION OF ENTITLEMENT TO SMALL ENTITY STATUS PURSUANT TO 37 C.F.R. § 1.27(c)(2)

MAIL STOP - OFFICE OF PETITIONS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

By this communication, Applicant hereby notifies the Commissioner of Patents that large entity status is no longer appropriate for the above-identified application, and we assert that Applicant is entitled to small entity status.

A **Certification of Small Entity Status,** signed by Applicant, is attached.

Respectfully submitted,

December 17, 2014

Peter J. Meza, No. 32,920
Hogan Lovells US LLP
2 North Cascade Avenue, Suite 1300
Colorado Springs, Colorado 80903
(719) 448-5906 Tel
(719) 448-5922 Fax

SMALL ENTITY STATUS

The Patent Office allows "Small Entities" to pay lower Patent Office fees. However, improperly claiming small entity status can invalidate your patent. Section A below will help you determine if you or your business qualify as a small entity. Section B includes a certification for small entity status. If after reviewing the following materials you determine that you qualify for small entity status, please complete the certification and return it to us. If we do not receive the signed certification from you, we will not claim small entity status for the application identified below, and you will not qualify for the lower Patent Office fees. If you do complete the certification, we may ask you to confirm your small entity status at various points during the prosecution of the application and the life of the issued patent.

A. Definition of Small Entity

A small entity means any "person," "small business concern," "nonprofit organization," or a combination of these, that holds the rights in the invention and (a) has not assigned or licensed the rights to another who is not a small entity, and (b) is not obligated to assign or license the rights to another who is not a small entity.

(1) *Person.* An inventor or other individuals who hold the rights in an invention.

(2) *Nonprofit organization.* A nonprofit organization is either:

(i) A university or institution of higher education in any country;

(ii) An organization described in section 501(c)(3), and exempt from taxation under section 501(a) of the Internal Revenue Code;

(iii) Any nonprofit scientific or educational organization qualified under a state's nonprofit organization statute; or

(iv) Any nonprofit organization located in a foreign country, that would otherwise qualify as a "nonprofit organization" if it were located in the U.S.A.

(3) *Small business concern.* Any business concern whose number of employees, (part-time and full-time), including affiliates, does not exceed 500 persons.

B. Certification

Applicant or Patentee: SRC Computers, LLC

Assignee: SRC Computers, LLC

Application No(s). SEE EXHIBIT A

Petitioners Amazon
Ex. 1010, p. 385 of 399

SRC Computers, LLC

STATEMENT CONCERNING SMALL ENTITY STATUS

I hereby certify that the owner of the application/patent identified above qualifies for small entity status because the owner has not assigned or licensed the rights in the invention to another who is not a small entity, and is not obligated to assign or license the rights in the invention to another who is not a small entity, and because:

The owner is a small business concern:

Business Name SRC Computers, LLC

Signor's Name Jon Huppenthal Signature

Title President and CEO Date 10/10/14

Business Address 4240 N. Nevada Avenue, Colorado Springs, C0 80907

SRC Computers, LLC
EXHIBIT A

Docket Number	Application Date	Application Number	Grant Date	Patent Number	Title
SRC001	12/17/1997	08/992,763	06/13/2000	6,076,152	MULTIPROCESSOR COMPUTER ARCHITECTURE
SRC001 CON	01/12/2000	09/481,902	06/12/2001	6,247,110	MULTIPROCESSOR COMPUTER ARCHITECTURE
SRC001 CON/DIV	01/05/2001	09/755,744			MULTIPROCESSOR COMPUTER ARCHITECTURE
SRC001 CON2	01/08/2003	10/339,133	11/01/2005	6,961,841	MULTIPROCESSOR COMPUTER ARCHITECTURE
SRC001 CON3	10/20/2004	10/969,635	06/26/2007	7,237,091	MULTIPROCESSOR COMPUTER ARCHITECTURE
SRC002	01/20/1998	09/008,871			SCALABLE SINGLE SYSTEM IMAGE OPERATING
SRC003	02/03/1998	09/018,032	02/15/2000	6,026,459	SYSTEM AND METHOD FOR DYNAMIC PRIORITY
SRC004	06/30/1998	09/108,088	09/25/2001	6,295,598	SPLIT DIRECTORY-BASED CACHE COHERENCY
SRC006	07/25/2000	09/624,788	03/12/2002	6,356,983	SYSTEM AND METHOD PROVIDING CACHE
SRC007	08/15/2000	09/638,365	07/15/2003	6,594,736	SYSTEM AND METHOD FOR SEMAPHORE AND
SRC008	05/03/2000	09/563,561	01/15/2002	6,339,819	MULTIPROCESSOR WITH EACH PROCESSOR
SRC009	11/05/2001	10/008,128	12/28/2004	6,836,823	BANDWIDTH ENHANCEMENT FOR UNCACHED
SRC010	06/22/2001	09/888,276	08/13/2002	6,434,687	SYSTEM AND METHOD FOR ACCELERATING WEB
SRC011	12/05/2001	10/011,835	12/26/2006	7,155,602	INTERFACE FOR INTEGRATING
SRC011 CON	05/31/2005	11/140,718	01/23/2007	7,167,976	AN INTERFACE FOR INTEGRATING
SRC011 PRO	04/30/2001	60/286,979			DELIVERING ACCELERATION: THE POTENTIAL
SRC012	08/17/2001	09/932,330	05/13/2008	7,373,440	SWITCH/NETWORK ADAPTER PORT FOR
SRC012 CIP	01/10/2003	10/340,390	03/27/2007	7,197,575	SWITCH/NETWORK ADAPTER PORT COUPLING A
SRC012 CIP2	08/15/2005	11/203,983	07/21/2009	7,565,461	SWITCH/NETWORK ADAPTER PORT COUPLING A
SRC012 DIV	11/23/2004	10/996,016	09/02/2008	7,421,524	SWITCH/NETWORK ADAPTER PORT FOR
SRC013	10/23/2002	10/278,345	10/17/2006	7,124,211	SYSTEM AND METHOD FOR EXPLICIT
SRC014	05/09/2002	10/142,045			ADAPTIVE PROCESSOR ARCHITECTURE
SRC014 DIV	05/02/2005	11/119,598			ADAPTIVE PROCESSOR ARCHITECTURE
SRC014 DIV/CIP	09/08/2005	11/222,417	07/29/2008	7,406,573	RECONFIGURABLE PROCESSOR ELEMENT
SRC015	10/31/2002	10/285,318	05/29/2007	7,225,324	MULTI-ADAPTIVE PROCESSING SYSTEMS AND
SRC015 CON	04/09/2007	11/733,064	11/17/2009	7,620,800	MULTI-ADAPTIVE PROCESSING SYSTEMS AND
SRC016	10/29/2002	10/282,986	02/21/2006	7,003,593	COMPUTER SYSTEM ARCHITECTURE AND
SRC017	10/31/2002	10/284,994	02/07/2006	6,996,656	SYSTEM AND METHOD FOR PROVIDING AN
SRC017 CON	07/22/2005	11/187,534			SYSTEM AND METHOD FOR PROVIDING AN
SRC018	10/31/2002	10/285,401	09/06/2005	6,941,539	EFFICIENCY OF RECONFIGURABLE HARDWARE
SRC019	10/31/2002	10/285,299	01/03/2006	6,983,456	PROCESS FOR CONVERTING PROGRAMS IN
SRC019 CON	10/04/2005	11/243,498	04/20/2010	7,703,085	PROCESS FOR CONVERTING PROGRAMS IN
SRC020 PRO	10/31/2002	60/422,722			GENERAL PURPOSE RECONFIGURABLE
SRC021	10/31/2002	10/285,399	11/20/2007	7,299,458	SYSTEM AND METHOD FOR CONVERTING
SRC022	10/31/2002	10/285,298	11/08/2005	6,964,029	SYSTEM AND METHOD FOR PARTITIONING
SRC023	10/31/2002	10/285,389	12/26/2006	7,155,708	DEBUGGING AND PERFORMANCE PROFILING
SRC024	01/10/2003	10/340,400			SYSTEM AND METHOD FOR SCALABLE
SRC025	01/14/2003	10/345,082	11/07/2006	7,134,120	MAP COMPILER PIPELINED LOOP STRUCTURE
SRC026					HANDLING OF NON-NUMERIC VARIABLES
SRC027	07/11/2003	10/618,041	09/09/2008	7,424,552	SWITCH/NETWORK ADAPTER PORT
SRC027 CIP	06/16/2004	10/869,199			SWITCH/NETWORK ADAPTER PORT
SRC027 CIP/DIV	08/06/2007	11/834,439	03/16/2010	7,680,968	SWITCH/NETWORK ADAPTER PORT
→ SRC028	06/16/2004	10/869,200	12/12/2006	7,149,867	SYSTEM AND METHOD OF ENHANCING
SRC028 PRO	06/18/2003	60/479,339			BANDWIDTH EFFICIENCY AND UTILIZATION
SRC029	10/17/2005	11/252,341	02/15/2011	7,890,686	DYNAMIC PRIORITY CONFLICT RESOLUTION IN A
SRC030	07/10/2006	11/456,466	11/19/2013	8,589,666	ELIMINATION OF STREAM CONSUMER LOOP

Petitioners Amazon
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SRC Computers, LLC
EXHIBIT A

SRC031 PRO	11/05/2010	61/410,676			SNAP INTERFACE USING MEMORY BUFFERS
SRC032 PRO	11/10/2010	61/412,124			COMPUTATIONAL UNIFICATION
SRC033 PRO	12/16/2011	61/576,846			MOBILE DEVICE UTLITIZING RECONFIGURABLE
SRC031	11/01/2011	13/286,996			HETEROGENEOUS COMPUTING SYSTEM
SRC032	11/02/2011	13/287,322	04/29/2014	8,713,518	SYSTEM AND METHOD FOR COMPUTATIONAL
SRC033	02/02/2012	13/365,090			MOBILE ELECTRONIC DEVICES UTILIZING
SRC036	05/27/2014	14/288,094			SYSTEM AND METHOD FOR RETAINING DRAM
SRC037	05/22/2014	14/284,616			SYSTEM AND METHOD FOR THERMALLY
SRC035	05/28/2013	13/903,720			MULTI-PROCESSOR COMPUTER ARCHITECTURE
SRC032 CON	03/10/2014	14/203,035			SYSTEM AND METHOD FOR COMPUTATIONAL

Petitioners Amazon
Ex. 1010, p. 388 of 399

Electronic Acknowledgement Receipt	
EFS ID:	21130575
Application Number:	10869200
International Application Number:	
Confirmation Number:	5929
Title of Invention:	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
First Named Inventor/Applicant Name:	Daniel Poznanovic
Customer Number:	25235
Filer:	Peter John Meza/Joyce Medrano-Paywa
Filer Authorized By:	Peter John Meza
Attorney Docket Number:	SRC028
Receipt Date:	06-JAN-2015
Filing Date:	16-JUN-2004
Time Stamp:	14:20:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assertion of entitlement to small entity status	DOC037.pdf	218665 a1abf77f811eb797c152ff6bcb1c067efa822f22	no	5

Warnings:
Information:

Total Files Size (in bytes):	218665

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/81A (02-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Patent Number	7,149,867
Issue Date	12-12-2006
First Named Inventor	Daniel Poznanovic
Title	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
Attorney Docket No.	

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: 23452

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/AIA/96) submitted herewith or filed on _____.

SIGNATURE of Applicant or Patent Owner

Signature	/Todd Rooke/	Date	March 3, 2016
Name	Todd Rooke	Telephone	
Title and Company	CEO, SRC Labs, LLC		

NOTE: Signatures of all the applicants or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☑ A total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: SRC Labs, LLC

Application No./Patent No.: 7,149,867 Filed/Issue Date: 12-12-2006

Titled: SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE

SRC Labs, LLC, a Limited Liability Company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 037820, Frame 0147, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Todd R. Fronek/	March 3, 2016
Signature	Date
Todd R. Fronek	48516
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	25097226
Application Number:	10869200
International Application Number:	
Confirmation Number:	5929
Title of Invention:	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
First Named Inventor/Applicant Name:	Daniel Poznanovic
Customer Number:	25235
Filer:	Todd Ryan Fronek/Kathryn Becker
Filer Authorized By:	Todd Ryan Fronek
Attorney Docket Number:	SRC028
Receipt Date:	03-MAR-2016
Filing Date:	16-JUN-2004
Time Stamp:	17:37:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	867.pdf	135744 e5e01686913fc660c171a378ebf41bbf7f8e450a	no	2

Warnings:
Information:

2	Assignee showing of ownership per 37 CFR 3.73	867_373c.pdf	106717 743ecb081c478faf31aff1b41b4f571874ece84c	no	3

Warnings:	
Information:	
Total Files Size (in bytes):	242461

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/869,200	06/16/2004	Daniel Poznanovic	

CONFIRMATION NO. 5929

POA ACCEPTANCE LETTER

23452
LARKIN HOFFMAN DALY & LINDGREN, LTD.
8300 Norman Center Drive
Suite 1000
Minneapolis, MN 55437

OC000000081240232

Date Mailed: 03/08/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/03/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rmturner myles/

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/869,200	06/16/2004	Daniel Poznanovic	

CONFIRMATION NO. 5929

POWER OF ATTORNEY NOTICE

25235
HOGAN LOVELLS US LLP - Colorado Springs
TWO NORTH CASCADE AVENUE
SUITE 1300
COLORADO SPRINGS, CO 80903

OC000000081240199

Date Mailed: 03/08/2016

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/03/2016.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/rmturner myles/