A Scalable 6-to-18 GHz Concurrent Dual-Band Quad-Beam Phased-Array Receiver in CMOS

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***Abstract*—This paper reports a 6-to-18 GHz integrated phased-array receiver implemented in 130-nm CMOS. The receiver is easily scalable to build a very large-scale phased-array system. It concurrently forms four independent beams at two different frequencies from 6 to 18 GHz. The nominal conversion gain of the receiver ranges from 16 to 24 dB over the entire band while the worst-case cross-band and cross-polarization rejections are achieved 48 dB and 63 dB, respectively. Phase shifting is performed in the LO path by a digital phase rotator with the worst-case RMS phase error and amplitude variation of 0.5° and 0.4 dB, respectively, over the entire band. A four-element phased-array receiver system is implemented based on four receiver chips. The measured array patterns agree well with the theoretical ones with a peak-to-null ratio of over 21.5 dB.**

***Index Terms*—CMOS, concurrent, large-scale phased arrays, multi-band, multi-beam, phased arrays, scalable, tritave.**

I. Introduction

PHASED arrays steer the beam direction electronically, bringing many benefits such as high directivity, interference rejection, signal-to-noise ratio improvement, and fast scanning response [1]–[4]. For this reason, phased arrays have been extensively employed in radar and communication systems in the area of military, space, and radio astronomy since their advent in the 1950s [5], [6]. Recently, substantial attention is also drawn in civil applications including high-speed point-to-point communications and car radars [4], [7].

Benefits of phased arrays increase with the number of elements combined in the array. This gives rise to the desire to make very large-scale phased arrays (up to 10^6 elements) for high-precision radars, long-range sensors, or high-directivity communication systems. One of the major obstacles in implementing large-scale phased arrays lies in the high complexity and cost to assemble the whole array system. Traditionally, phased-array systems have been built using a module-based approach. Most transmitter/receiver components, such as low-noise amplifiers (LNAs), power amplifiers, phase shifters, attenuators, filters, mixers, and LO sources, are implemented in separate modules and then interconnected to each other externally [3], [6]. This approach not only increases the assembly size and cost, but also degrades the system reliability due to the complicated configuration. Furthermore, several transmit/receive module components have been implemented using expensive compound semiconductors such as GaAs, which takes a substantial portion of the overall system cost [6], [8]. Thus, the size of phased arrays has been limited to a certain number of elements (10^4 or 10^5 at most), making it difficult to take full advantage of very large-scale array systems.

Integrated CMOS solutions offer an opportunity for dramatic reduction in cost and size of such systems. The high yield and repeatability of silicon ICs allows the entire transmitter and/or receiver to be integrated on a single chip. For example, there have been reported a CMOS RF front-end [9], a fully integrated Si-based phased-array receiver [10] and a CMOS phased-array transmitter [11], all at 24 GHz and a fully integrated Si-based phased-array transceiver at 77 GHz [12]. This single-chip approach in silicon reduces the overall system cost substantially, compared to the conventional module-based counterpart in compound semiconductors.

There is a trend in radar and communication systems that the transceiver operates concurrently in multiple modes and multiple bands [13]. Furthermore, many applications require the transceiver to operate in a wide range of RF frequencies [14]. These trends also apply to phased arrays when multiple targets must be tracked at the same time in radars and electronic countermeasure systems or when multi-point communications are desired at multiple frequencies in a wide bandwidth. The high integration capability of CMOS offers a promising solution to achieve the wideband phased arrays with multiple functionalities. Several wideband phased (or timed) array receivers [15], [16] and transceiver [17] have been reported in silicon. However, none of the previous work has implemented a concurrent multi-band multi-beam phased-array receiver operating in a wide range of RF frequencies.

In this work, we integrated RF front-end components of a concurrent dual-band quad-beam phased-array receiver element on a single CMOS chip. The receiver is programmable to concurrently receive two RF frequencies between 6 and 18 GHz (a tritave) while forming four independently-controlled beams with separate phase shifting operation. The receiver is also easily scalable toward very large-scale phased arrays because additional receiver chips can be added to increase the number

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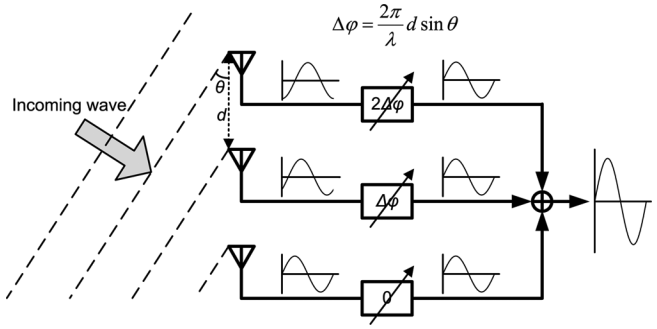

Fig. 1. Basic phased-array receiver configuration.

of array elements with relatively lower cost and complexity. To the authors' best knowledge, this is the first reported concurrent tritave phased-array receiver implemented in CMOS.

The paper is organized as follows. Section II briefly reviews phased arrays and a conventional approach to implement large-scale phased arrays. Section III presents a proposed concurrent array system architecture as well as the associated advantages. In Section IV, the architecture and frequency plan of the CMOS phased-array receiver chip is described. Section V presents the detailed circuit block design. Section VI provides the experimental results of the receiver chip and a four-element array system that combines four receiver chips.

II. Phased Arrays

A. Overview

Phased-array receivers consist of multiple antenna elements spaced with a certain distance (d) and a following separate phase shifter per each element for the electronic beamforming at a given incident angle (θ) in space (Fig. 1). When a RF wave arrives at the antenna elements, the arrival time of wavefront is different between two adjacent elements by

$$\Delta t = \frac{d \sin\theta}{c} \tag{1}$$

where c is the speed of light. In the narrowband circumstances, the arrival time difference results in a phase delay of the received signal between two adjacent elements, given by

$$\Delta\varphi = \frac{2\pi d \sin\theta}{\lambda} \tag{2}$$

where λ is the wavelength of the incoming wave. Thus, the following phase shifter adjusts the phase delay in such a way that output signals from each element are all in-phase with one another. By summing the signals from each element, a coherent output signal can be obtained with a large array gain. On the other hand, other incoming waves at different incident angles will not be summed coherently and thus will be significantly attenuated at the array output.

B. Benefits of Phased Array

gain than a single element receiver. When the signals are combined in the amplitude domain (current or voltage) with a same output load, the array gain is given by

$$G_{\text{Array}} = G_{\text{Single}} + 20\log_{10} N \ (\text{dB}) \tag{3}$$

where G_{Single} is the gain of each single element and N is the number of array elements. Again, undesired signals such as the interference or jammers arriving at other incident angles are inherently rejected according to the established array pattern.

Furthermore, the signal integrity is enhanced at the array output through an effective improvement of the output signal-to-noise ratio (SNR) by a factor of $10\log_{10} N$ (dB). This is because noise generated from each element is uncorrelated with one another while the desired signal is combined coherently [10].

Finally, since phase arrays steer the beam direction electronically, it is able to receive multiple beams arriving at different incident angles simultaneously. Also, the beam can be steered in a faster and more reliable way than that of a mechanically steered antenna system.

C. Large-Scale Phased-Array System

The benefits of phased arrays given in Section II-B are more noticeable as we increase the number of array elements. For instance, if we combine the signals from one million (10^6) elements without any loss and phase distortion, then the array gain given in (3) and the output SNR will be improved by a factor of 120 dB and 60 dB, respectively. Although the improvement factor will be degraded in a practical array system due to the non-ideal signal distribution and combining, it will enhance the sensitivity of the receiver to a substantial degree. The capability of rejecting undesired signals will also be reinforced with a larger number of elements because the main beam narrows and a more number of null positions are presented in the array pattern.

In spite of the apparent advantages of large-scale phased arrays, their applications have been limited due to several difficulties, mainly, the prohibitive complexity and cost. Fig. 2 shows one of the conventional ways of building a large-scale phased-array receiver system. In order to combine a very large number of elements efficiently, several elements are grouped together into a sub-array, and then several sub-arrays are combined by a RF distribution network to present a single output for down-conversion. It is noteworthy that for active phased arrays [1], every single element contains an independent receiver module which includes a filter, a LNA, a phase shifter, and an attenuator. Usually, these receiver components are implemented in separate chips or packages, interconnected to each other, and then assembled into a sub-array system by external transmission lines such as microstrips, cables, or waveguides. Therefore, as the number of array elements increases, the cost and complexity will also rise dramatically to assemble these components into a system. Furthermore, the design of the low-loss RF distribution network will be challenging with a large number of elements for two reasons. The first reason is that the number of sub-ar-

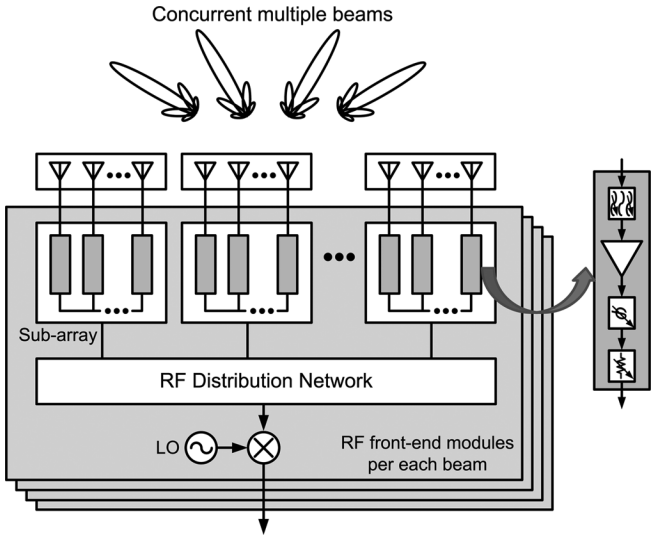

Fig. 2. A conventional way of building a large-scale phased-array receiver system (in the active array configuration) that supports multiple beams.

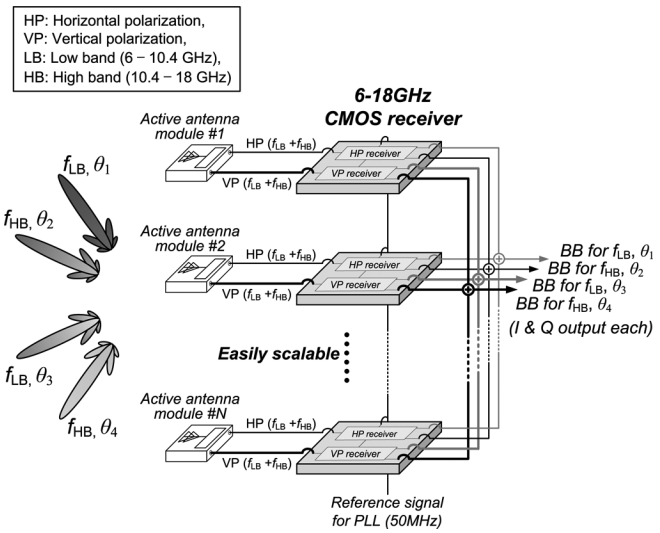

Fig. 3. A proposed 6–18 GHz phased-array receiver system that receives four beams at two frequencies concurrently and is easily scalable toward a very large-scale array.

that the signal is distributed (or combined) in the RF domain before down-conversion, which gives rise to higher loss than if the distribution (or combining) were to be performed in the IF or baseband domain.

Another challenge in large-scale phased arrays is the high cost of active circuit components, most of which are fabricated usually in expensive compound semiconductors such GaAs. Although the cost of monolithic microwave integrated circuits (MMICs) in GaAs decreased recently due to the process maturity, it still takes a large portion of the total array system cost [6], [8], making a very large-scale array practically difficult to implement.

Even more challenge arises when the array must receive multiple beams at the same time. Since each beam requires a separate receiver module and a distribution network for the independent beamforming capability, the associated complexity and cost will be further exacerbated.

III. Proposed Large-Scale Phased-Array System Architecture

To deal with the challenges discussed in Section II-C, we propose an efficient way of building large-scale phased-array receiver systems, as shown in Fig. 3. With a single CMOS chip (a shaded block in Fig. 3), we integrate all receiver module components on the same die except for the antenna and front-end LNA. The CMOS receiver includes the tunable concurrent amplifiers (TCAs), down-conversion mixers, phase shifters, frequency synthesizers, and baseband buffers [18]. This integrated solution avoids the costly large number of separate component modules and their complicated interconnection for large-scale arrays, which results in a dramatic cost reduction. More importantly, the chip is implemented in CMOS, which will bring another substantial cost reduction compared with its compound-semiconductor counterpart.

The CMOS receiver has two input ports to receive two different frequencies concurrently, one in the low band (LB) from 6 to 10.4 GHz and the other in the high band (HB) from 10.4 to 18 GHz. The dual-band signal is then split into two separate signals on-chip, one for each band. Subsequently, each signal is down-converted with the independent phase-shifting operation to provide separate beamforming. Therefore, the proposed array system can receive and steer four different beams at two different frequencies concurrently.

The baseband outputs from each array element are combined off-chip in the current domain, providing the back-end processors with one combined baseband signal per beam. Since the signal combining is performed at the baseband rather than the RF frequency, it alleviates the difficulty in designing a low-loss combining network for large-scale arrays.

It is also noteworthy that the only feed signal which needs to be distributed among the elements other than DC supplies is a 50 MHz reference signal for on-chip frequency synthesizers. Due to its low frequency, the reference can be simply distributed without adding extra complexity. It also makes the proposed array architecture easily scalable.

The LO signals generated by the on-chip frequency synthesizers may have relatively higher phase noise than those provided by off-chip low-noise sources. However, when combining N elements (or N chips) in the array, the phase noise originating from the on-chip components of each element is uncorrelated with one another and thus adds up in power. On the other hand, the carrier signal is combined in amplitude in the current domain. Therefore, the phase-noise performance at the array output improves by a factor of $10\log_{10}N$ (dB) as long as the phase noise is dominated by on-chip sources, not by an off-chip reference signal. This improvement also makes the integrated solution including on-chip frequency synthesizers suit-

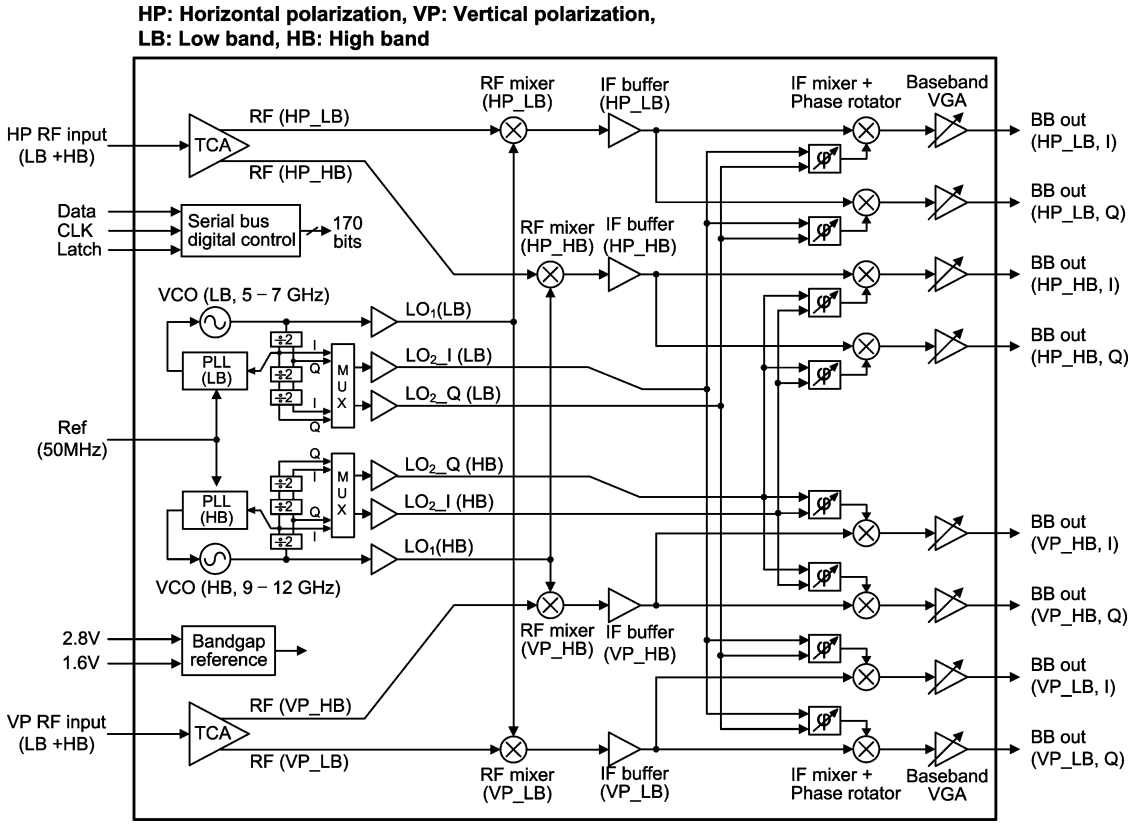

Fig. 4. Architecture of the tunable concurrent dual-band quad-beam phased-array receiver in CMOS.

In the complete array system, a separate active antenna module, consisting of a broadband antenna and a GaN LNA, will be employed in front of the CMOS receiver.

IV. CMOS Phased-Array Receiver Element

In this section, the architecture and frequency plan of the CMOS concurrent phased-array receiver element is discussed in detail. It should be noted that a single receiver chip operates as one receiver element in the array system, as shown in Fig. 3.

A. Receiver Architecture

A block diagram of the receiver architecture is presented in Fig. 4. Since it is a concurrent dual-band receiver, the incoming RF signal contains two frequencies at LB and HB respectively, and feeds a front-end tunable concurrent amplifier (TCA). The TCA amplifies, filters, and finally splits the RF signal into two separate outputs; one at LB and the other at HB. Each of the two signals goes through separate double down-conversion by subsequent RF and IF mixers. The IF mixers generate the I and Q components of the baseband signal for digital demodulation capability. The baseband VGAs adjust the baseband amplitude and drive the output load differentially.

There are two sets of RF input (HP RF input and VP RF input in Fig. 4) which are down-converted by two same sets of the RF signal-path circuitry, respectively. Therefore, the receiver presents a total of eight differential baseband outputs, one for

The receiver includes two on-chip programmable frequency synthesizers in order to support the separate down-conversion of the LB and HB signals, respectively. The frequency synthesizers generate the first LO (LO_1) signal between 5–7 GHz for LB and between 9–12 GHz for HB with a frequency step of 200 MHz. The LO_1 signal drives the RF mixers for two polarizations. The second LO (LO_2) signal, driving the phase rotators and IF mixers, is generated by three static divide-by-2 dividers and a 2:1 multiplexer. According to the receiver frequency scheme discussed in Section IV-B, the LO_2 frequency is selected as either one half or one eighth of the LO_1 frequency by the multiplexer. The LO_2 signal carries the I and Q components separately to feed the phase rotators in quadrature. A 50 MHz reference signal for the phase-locked loops (PLLs) is generated by an off-chip crystal oscillator.

The LO phase-shifting architecture is adopted in this phased-array receiver in order to circumvent the challenge of designing high-resolution wideband phase shifters in the RF signal path [19]. The phase shifting is performed in the LO_2 signal by a 10-bit digital phase rotator. Each IF mixer is driven by a separate phase rotator to maximize the flexibility of the receiver. This not only provides the independent beamforming capability to the signals of different bands and polarizations, but also helps to minimize the I and Q mismatch of the quadrature baseband outputs.

The receiver includes an on-chip digital serial-bus control

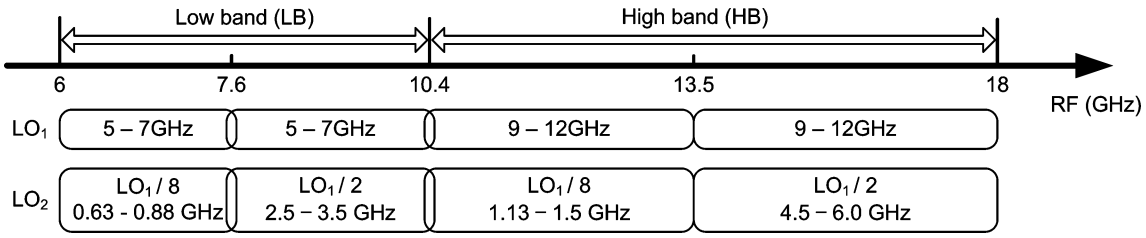

Fig. 5. Frequency scheme.

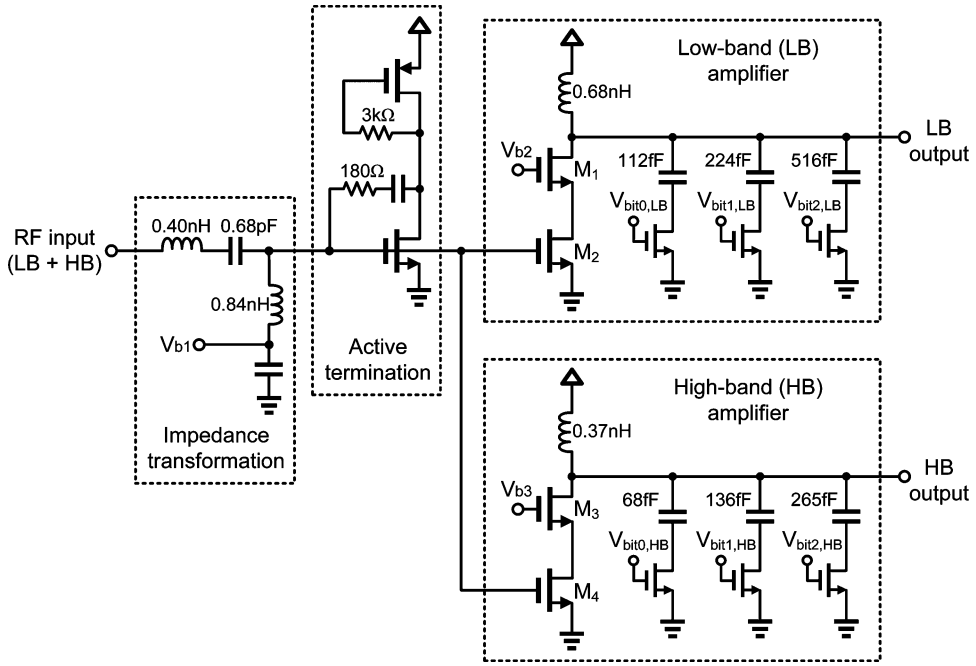

Fig. 6. Schematic of the TCA with a single input and a dual output.

other functionalities of the receiver. Bias voltages are generated by on-chip bandgap reference circuitry.

B. Receiver Frequency Scheme

The receiver supports a concurrent dual-band RF signal, such that two receive frequencies are tunable simultaneously and independently, one from 6 to 10.4 GHz (LB) and the other from 10.4 to 18 GHz (HB). As shown in Fig. 5, each band is further divided into two sub-bands depending on the corresponding IF frequency. Accordingly, the LO_2 frequency switches between 1/2 and 1/8 of the LO_1 frequency. For instance, a RF signal between 5.625–7.875 GHz is down-converted to the IF between 0.625–0.875 GHz by the LO_1 between 5–7 GHz. The LO_2 is then selected as 1/8 of LO_1 to down-convert the IF to the baseband. On the other hand, for a RF signal between 7.5–10.5 GHz, the LO_2 is selected as 1/2 of LO_1 to down-convert the IF between 2.5–3.5 GHz to the baseband. In this way, the entire RF frequencies for LB (6–10.4 GHz) are covered without discontinuity and so are those for HB as well.

With the dual-IF frequency scheme, the required VCO tuning range is reduced from 54% to 33% and 29% for LB and HB, respectively. This relaxed tuning range enables us to further optimize the RF channel spacing depends on which LO_2 frequency scheme is selected at the given LO_1 frequency step (200 MHz). The channel spacing is 225 MHz when operating in the 1/8 LO_1 scheme and 300 MHz in the 1/2 LO_1 scheme.

V. Circuit Implementation

The detailed circuit design of the CMOS receiver is presented in this section. Most circuit blocks including the mixers, baseband VGAs, VCOs, LO distribution buffers, and phase rotators use differential signaling while the TCA amplifies a single-ended signal.

A. Tunable Concurrent Amplifier (TCA)

Since the incoming concurrent dual-band signal is split on-chip before the down-conversion, the front-end TCA must provide a single input and a dual output. Important design parameters in the TCA are the wideband input matching, noise figure, frequency tunability, and isolation between two different outputs. The single input port should provide a good input matching performance over the entire tritave, from 6 to 18 GHz. The two output ports present two separate signals well filtered at the desired frequencies that should be tunable over

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