A Scalable 6-to-18 GHz Concurrent Dual-Band Quad-Beam Phased-Array Receiver in CMOS

Sanggeun Jeon, *Member, IEEE*, Yu-Jiu Wang, *Student Member, IEEE*, Hua Wang, Florian Bohn, *Student Member, IEEE*, Arun Natarajan, Aydin Babakhani, *Member, IEEE*, and Ali Hajimiri, *Member, IEEE*

***Abstract*—This paper reports a 6-to-18 GHz integrated phased-array receiver implemented in 130-nm CMOS. The receiver is easily scalable to build a very large-scale phased-array system. It concurrently forms four independent beams at two different frequencies from 6 to 18 GHz. The nominal conversion gain of the receiver ranges from 16 to 24 dB over the entire band while the worst-case cross-band and cross-polarization rejections are achieved 48 dB and 63 dB, respectively. Phase shifting is performed in the LO path by a digital phase rotator with the worst-case RMS phase error and amplitude variation of 0.5° and 0.4 dB, respectively, over the entire band. A four-element phased-array receiver system is implemented based on four receiver chips. The measured array patterns agree well with the theoretical ones with a peak-to-null ratio of over 21.5 dB.**

***Index Terms*—CMOS, concurrent, large-scale phased arrays, multi-band, multi-beam, phased arrays, scalable, tritave.**

I. Introduction

PHASED arrays steer the beam direction electronically, bringing many benefits such as high directivity, interference rejection, signal-to-noise ratio improvement, and fast scanning response [1]–[4]. For this reason, phased arrays have been extensively employed in radar and communication systems in the area of military, space, and radio astronomy since their advent in the 1950s [5], [6]. Recently, substantial attention is also drawn in civil applications including high-speed point-to-point communications and car radars [4], [7].

Benefits of phased arrays increase with the number of elements combined in the array. This gives rise to the desire to make very large-scale phased arrays (up to 10^6 elements) for high-precision radars, long-range sensors, or high-directivity communication systems. One of the major obstacles in implementing large-scale phased arrays lies in the high complexity and cost to assemble the whole array system. Traditionally, phased-array systems have been built using a module-based approach. Most transmitter/receiver components, such as low-noise amplifiers (LNAs), power amplifiers, phase shifters, attenuators, filters, mixers, and LO sources, are implemented in separate modules and then interconnected to each other externally [3], [6]. This approach not only increases the assembly size and cost, but also degrades the system reliability due to the complicated configuration. Furthermore, several transmit/receive module components have been implemented using expensive compound semiconductors such as GaAs, which takes a substantial portion of the overall system cost [6], [8]. Thus, the size of phased arrays has been limited to a certain number of elements (10^4 or 10^5 at most), making it difficult to take full advantage of very large-scale array systems.

Integrated CMOS solutions offer an opportunity for dramatic reduction in cost and size of such systems. The high yield and repeatability of silicon ICs allows the entire transmitter and/or receiver to be integrated on a single chip. For example, there have been reported a CMOS RF front-end [9], a fully integrated Si-based phased-array receiver [10] and a CMOS phased-array transmitter [11], all at 24 GHz and a fully integrated Si-based phased-array transceiver at 77 GHz [12]. This single-chip approach in silicon reduces the overall system cost substantially, compared to the conventional module-based counterpart in compound semiconductors.

There is a trend in radar and communication systems that the transceiver operates concurrently in multiple modes and multiple bands [13]. Furthermore, many applications require the transceiver to operate in a wide range of RF frequencies [14]. These trends also apply to phased arrays when multiple targets must be tracked at the same time in radars and electronic countermeasure systems or when multi-point communications are desired at multiple frequencies in a wide bandwidth. The high integration capability of CMOS offers a promising solution to achieve the wideband phased arrays with multiple functionalities. Several wideband phased (or timed) array receivers [15], [16] and transceiver [17] have been reported in silicon. However, none of the previous work has implemented a concurrent multi-band multi-beam phased-array receiver operating in a wide range of RF frequencies.

In this work, we integrated RF front-end components of a concurrent dual-band quad-beam phased-array receiver element on a single CMOS chip. The receiver is programmable to concurrently receive two RF frequencies between 6 and 18 GHz (a tritave) while forming four independently-controlled beams with separate phase shifting operation. The receiver is also easily scalable toward very large-scale phased arrays because additional receiver chips can be added to increase the number

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S. Jeon is with the School of Electrical Engineering, Korea University, Seongbuk-gu, Seoul, Korea (e-mail: sgjeon@korea.ac.kr).

Y.-J. Wang, H. Wang, F. Bohn, A. Babakhani, and A. Hajimiri are with the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA 91125 USA.

A. Natarajan is with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA.

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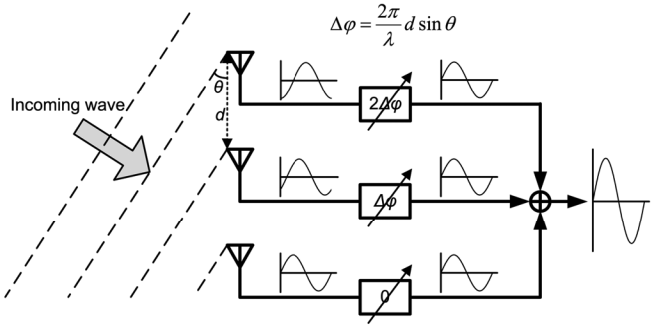

Fig. 1. Basic phased-array receiver configuration.

of array elements with relatively lower cost and complexity. To the authors' best knowledge, this is the first reported concurrent tritave phased-array receiver implemented in CMOS.

The paper is organized as follows. Section II briefly reviews phased arrays and a conventional approach to implement large-scale phased arrays. Section III presents a proposed concurrent array system architecture as well as the associated advantages. In Section IV, the architecture and frequency plan of the CMOS phased-array receiver chip is described. Section V presents the detailed circuit block design. Section VI provides the experimental results of the receiver chip and a four-element array system that combines four receiver chips.

II. Phased Arrays

A. Overview

Phased-array receivers consist of multiple antenna elements spaced with a certain distance (d) and a following separate phase shifter per each element for the electronic beamforming at a given incident angle (θ) in space (Fig. 1). When a RF wave arrives at the antenna elements, the arrival time of wavefront is different between two adjacent elements by

$$\Delta t = \frac{d \sin\theta}{c} \tag{1}$$

where c is the speed of light. In the narrowband circumstances, the arrival time difference results in a phase delay of the received signal between two adjacent elements, given by

$$\Delta\varphi = \frac{2\pi d \sin\theta}{\lambda} \tag{2}$$

where λ is the wavelength of the incoming wave. Thus, the following phase shifter adjusts the phase delay in such a way that output signals from each element are all in-phase with one another. By summing the signals from each element, a coherent output signal can be obtained with a large array gain. On the other hand, other incoming waves at different incident angles will not be summed coherently and thus will be significantly attenuated at the array output.

B. Benefits of Phased Array

Since a phased array combines several in-phase signals coherently at the array output, it can achieve an effectively higher gain than a single element receiver. When the signals are combined in the amplitude domain (current or voltage) with a same output load, the array gain is given by

$$G_{\text{Array}} = G_{\text{Single}} + 20\log_{10} N \ (\text{dB}) \tag{3}$$

where G_{Single} is the gain of each single element and N is the number of array elements. Again, undesired signals such as the interference or jammers arriving at other incident angles are inherently rejected according to the established array pattern.

Furthermore, the signal integrity is enhanced at the array output through an effective improvement of the output signal-to-noise ratio (SNR) by a factor of $10\log_{10} N$ (dB). This is because noise generated from each element is uncorrelated with one another while the desired signal is combined coherently [10].

Finally, since phase arrays steer the beam direction electronically, it is able to receive multiple beams arriving at different incident angles simultaneously. Also, the beam can be steered in a faster and more reliable way than that of a mechanically steered antenna system.

C. Large-Scale Phased-Array System

The benefits of phased arrays given in Section II-B are more noticeable as we increase the number of array elements. For instance, if we combine the signals from one million (10^6) elements without any loss and phase distortion, then the array gain given in (3) and the output SNR will be improved by a factor of 120 dB and 60 dB, respectively. Although the improvement factor will be degraded in a practical array system due to the non-ideal signal distribution and combining, it will enhance the sensitivity of the receiver to a substantial degree. The capability of rejecting undesired signals will also be reinforced with a larger number of elements because the main beam narrows and a more number of null positions are presented in the array pattern.

In spite of the apparent advantages of large-scale phased arrays, their applications have been limited due to several difficulties, mainly, the prohibitive complexity and cost. Fig. 2 shows one of the conventional ways of building a large-scale phased-array receiver system. In order to combine a very large number of elements efficiently, several elements are grouped together into a sub-array, and then several sub-arrays are combined by a RF distribution network to present a single output for down-conversion. It is noteworthy that for active phased arrays [1], every single element contains an independent receiver module which includes a filter, a LNA, a phase shifter, and an attenuator. Usually, these receiver components are implemented in separate chips or packages, interconnected to each other, and then assembled into a sub-array system by external transmission lines such as microstrips, cables, or waveguides. Therefore, as the number of array elements increases, the cost and complexity will also rise dramatically to assemble these components into a system. Furthermore, the design of the low-loss RF distribution network will be challenging with a large number of elements for two reasons. The first reason is that the number of sub-arrays is also increased accordingly, which requires more depth of the signal distribution (or combining) network. The other is

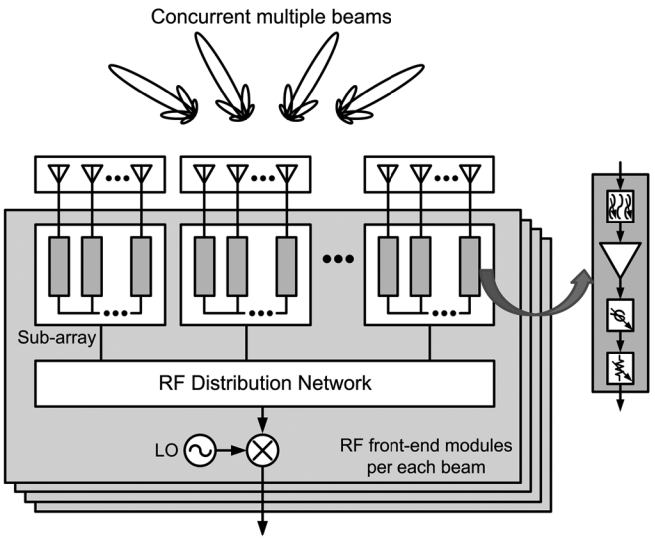

Fig. 2. A conventional way of building a large-scale phased-array receiver system (in the active array configuration) that supports multiple beams.

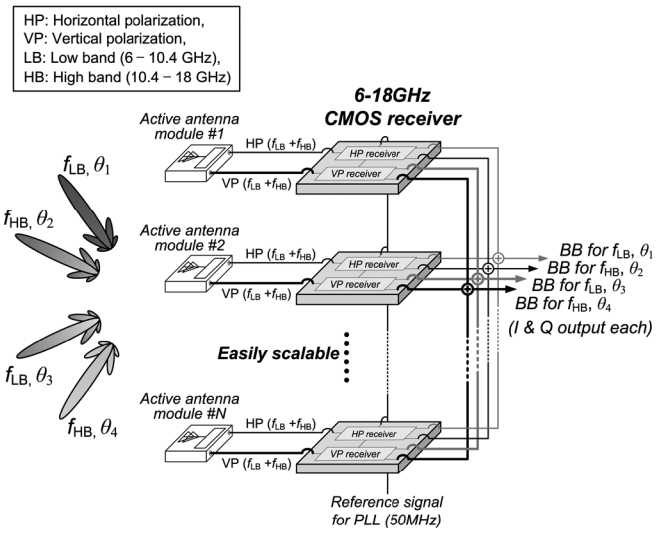

Fig. 3. A proposed 6–18 GHz phased-array receiver system that receives four beams at two frequencies concurrently and is easily scalable toward a very large-scale array.

that the signal is distributed (or combined) in the RF domain before down-conversion, which gives rise to higher loss than if the distribution (or combining) were to be performed in the IF or baseband domain.

Another challenge in large-scale phased arrays is the high cost of active circuit components, most of which are fabricated usually in expensive compound semiconductors such GaAs. Although the cost of monolithic microwave integrated circuits (MMICs) in GaAs decreased recently due to the process maturity, it still takes a large portion of the total array system cost [6], [8], making a very large-scale array practically difficult to implement.

Even more challenge arises when the array must receive multiple beams at the same time. Since each beam requires a separate receiver module and a distribution network for the independent beamforming capability, the associated complexity and cost will be further exacerbated.

III. Proposed Large-Scale Phased-Array System Architecture

To deal with the challenges discussed in Section II-C, we propose an efficient way of building large-scale phased-array receiver systems, as shown in Fig. 3. With a single CMOS chip (a shaded block in Fig. 3), we integrate all receiver module components on the same die except for the antenna and front-end LNA. The CMOS receiver includes the tunable concurrent amplifiers (TCAs), down-conversion mixers, phase shifters, frequency synthesizers, and baseband buffers [18]. This integrated solution avoids the costly large number of separate component modules and their complicated interconnection for large-scale arrays, which results in a dramatic cost reduction. More importantly, the chip is implemented in CMOS, which will bring another substantial cost reduction compared with its compound-semiconductor counterpart.

The CMOS receiver has two input ports to receive two different polarization signals fed from an active antenna module, i.e., horizontal polarization (HP) and vertical polarization (VP), respectively. On the other hand, each input port is able to receive a dual-band signal containing two different frequencies concurrently, one in the low band (LB) from 6 to 10.4 GHz and the other in the high band (HB) from 10.4 to 18 GHz. The dual-band signal is then split into two separate signals on-chip, one for each band. Subsequently, each signal is down-converted with the independent phase-shifting operation to provide separate beamforming. Therefore, the proposed array system can receive and steer four different beams at two different frequencies concurrently.

The baseband outputs from each array element are combined off-chip in the current domain, providing the back-end processors with one combined baseband signal per beam. Since the signal combining is performed at the baseband rather than the RF frequency, it alleviates the difficulty in designing a low-loss combining network for large-scale arrays.

It is also noteworthy that the only feed signal which needs to be distributed among the elements other than DC supplies is a 50 MHz reference signal for on-chip frequency synthesizers. Due to its low frequency, the reference can be simply distributed without adding extra complexity. It also makes the proposed array architecture easily scalable.

The LO signals generated by the on-chip frequency synthesizers may have relatively higher phase noise than those provided by off-chip low-noise sources. However, when combining N elements (or N chips) in the array, the phase noise originating from the on-chip components of each element is uncorrelated with one another and thus adds up in power. On the other hand, the carrier signal is combined in amplitude in the current domain. Therefore, the phase-noise performance at the array output improves by a factor of $10\log_{10} N$ (dB) as long as the phase noise is dominated by on-chip sources, not by an off-chip reference signal. This improvement also makes the integrated solution including on-chip frequency synthesizers suitable for large-scale phased arrays without degrading the array performance.

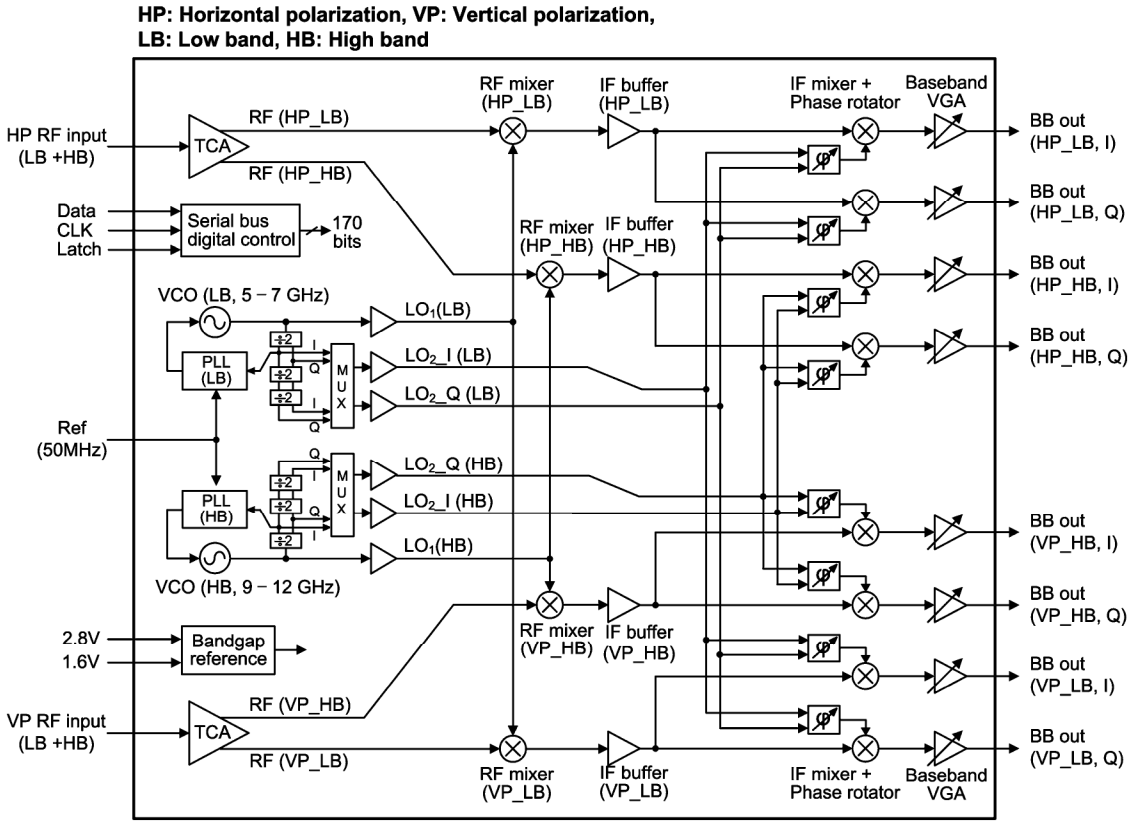

Fig. 4. Architecture of the tunable concurrent dual-band quad-beam phased-array receiver in CMOS.

In the complete array system, a separate active antenna module, consisting of a broadband antenna and a GaN LNA, will be employed in front of the CMOS receiver.

IV. CMOS Phased-Array Receiver Element

In this section, the architecture and frequency plan of the CMOS concurrent phased-array receiver element is discussed in detail. It should be noted that a single receiver chip operates as one receiver element in the array system, as shown in Fig. 3.

A. Receiver Architecture

A block diagram of the receiver architecture is presented in Fig. 4. Since it is a concurrent dual-band receiver, the incoming RF signal contains two frequencies at LB and HB respectively, and feeds a front-end tunable concurrent amplifier (TCA). The TCA amplifies, filters, and finally splits the RF signal into two separate outputs; one at LB and the other at HB. Each of the two signals goes through separate double down-conversion by subsequent RF and IF mixers. The IF mixers generate the I and Q components of the baseband signal for digital demodulation capability. The baseband VGAs adjust the baseband amplitude and drive the output load differentially.

There are two sets of RF input (HP RF input and VP RF input in Fig. 4) which are down-converted by two same sets of the RF signal-path circuitry, respectively. Therefore, the receiver presents a total of eight differential baseband outputs, one for each combination of two different polarizations (HP and VP), two different frequency bands (LB and HB), and I and Q.

The receiver includes two on-chip programmable frequency synthesizers in order to support the separate down-conversion of the LB and HB signals, respectively. The frequency synthesizers generate the first LO (LO_1) signal between 5–7 GHz for LB and between 9–12 GHz for HB with a frequency step of 200 MHz. The LO_1 signal drives the RF mixers for two polarizations. The second LO (LO_2) signal, driving the phase rotators and IF mixers, is generated by three static divide-by-2 dividers and a 2:1 multiplexer. According to the receiver frequency scheme discussed in Section IV-B, the LO_2 frequency is selected as either one half or one eighth of the LO_1 frequency by the multiplexer. The LO_2 signal carries the I and Q components separately to feed the phase rotators in quadrature. A 50 MHz reference signal for the phase-locked loops (PLLs) is generated by an off-chip crystal oscillator.

The LO phase-shifting architecture is adopted in this phased-array receiver in order to circumvent the challenge of designing high-resolution wideband phase shifters in the RF signal path [19]. The phase shifting is performed in the LO_2 signal by a 10-bit digital phase rotator. Each IF mixer is driven by a separate phase rotator to maximize the flexibility of the receiver. This not only provides the independent beamforming capability to the signals of different bands and polarizations, but also helps to minimize the I and Q mismatch of the quadrature baseband outputs.

The receiver includes an on-chip digital serial-bus control unit that programs 170 bits to configure the dual RF frequencies, LO frequencies, phase-shifting angles, baseband gains, and

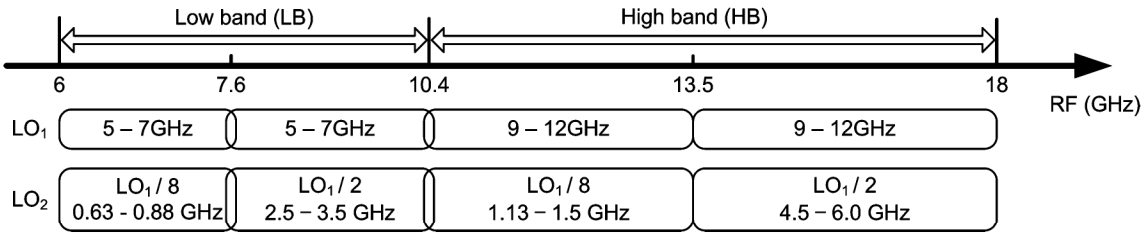

Fig. 5. Frequency scheme.

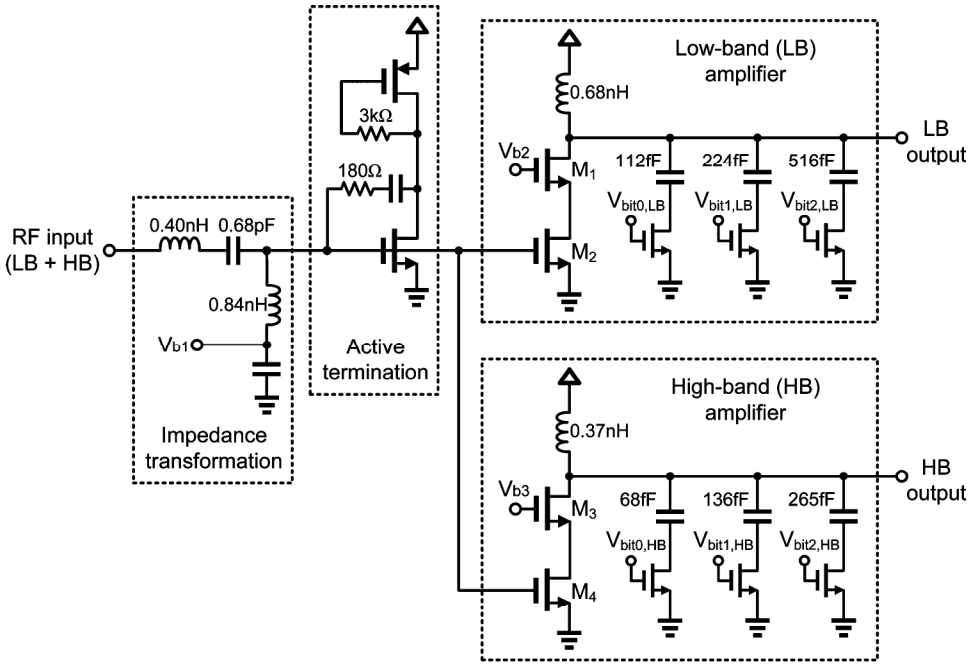

Fig. 6. Schematic of the TCA with a single input and a dual output.

other functionalities of the receiver. Bias voltages are generated by on-chip bandgap reference circuitry.

B. Receiver Frequency Scheme

The receiver supports a concurrent dual-band RF signal, such that two receive frequencies are tunable simultaneously and independently, one from 6 to 10.4 GHz (LB) and the other from 10.4 to 18 GHz (HB). As shown in Fig. 5, each band is further divided into two sub-bands depending on the corresponding IF frequency. Accordingly, the LO_2 frequency switches between 1/2 and 1/8 of the LO_1 frequency. For instance, a RF signal between 5.625–7.875 GHz is down-converted to the IF between 0.625–0.875 GHz by the LO_1 between 5–7 GHz. The LO_2 is then selected as 1/8 of LO_1 to down-convert the IF to the baseband. On the other hand, for a RF signal between 7.5–10.5 GHz, the LO_2 is selected as 1/2 of LO_1 to down-convert the IF between 2.5–3.5 GHz to the baseband. In this way, the entire RF frequencies for LB (6–10.4 GHz) are covered without discontinuity and so are those for HB as well.

With the dual-IF frequency scheme, the required VCO tuning range is reduced from 54% to 33% and 29% for LB and HB, respectively. This relaxed tuning range enables us to further optimize the other VCO performance such as phase noise and power consumption [20].

The RF channel spacing depends on which LO_2 frequency scheme is selected at the given LO_1 frequency step (200 MHz). The channel spacing is 225 MHz when operating in the 1/8 LO_1 scheme and 300 MHz in the 1/2 LO_1 scheme.

V. Circuit Implementation

The detailed circuit design of the CMOS receiver is presented in this section. Most circuit blocks including the mixers, baseband VGAs, VCOs, LO distribution buffers, and phase rotators use differential signaling while the TCA amplifies a single-ended signal.

A. Tunable Concurrent Amplifier (TCA)

Since the incoming concurrent dual-band signal is split on-chip before the down-conversion, the front-end TCA must provide a single input and a dual output. Important design parameters in the TCA are the wideband input matching, noise figure, frequency tunability, and isolation between two different outputs. The single input port should provide a good input matching performance over the entire tritave, from 6 to 18 GHz. The two output ports present two separate signals well filtered at the desired frequencies that should be tunable over the entire LB and HB frequencies, respectively. Also, good isolation is needed between the two output ports in terms of

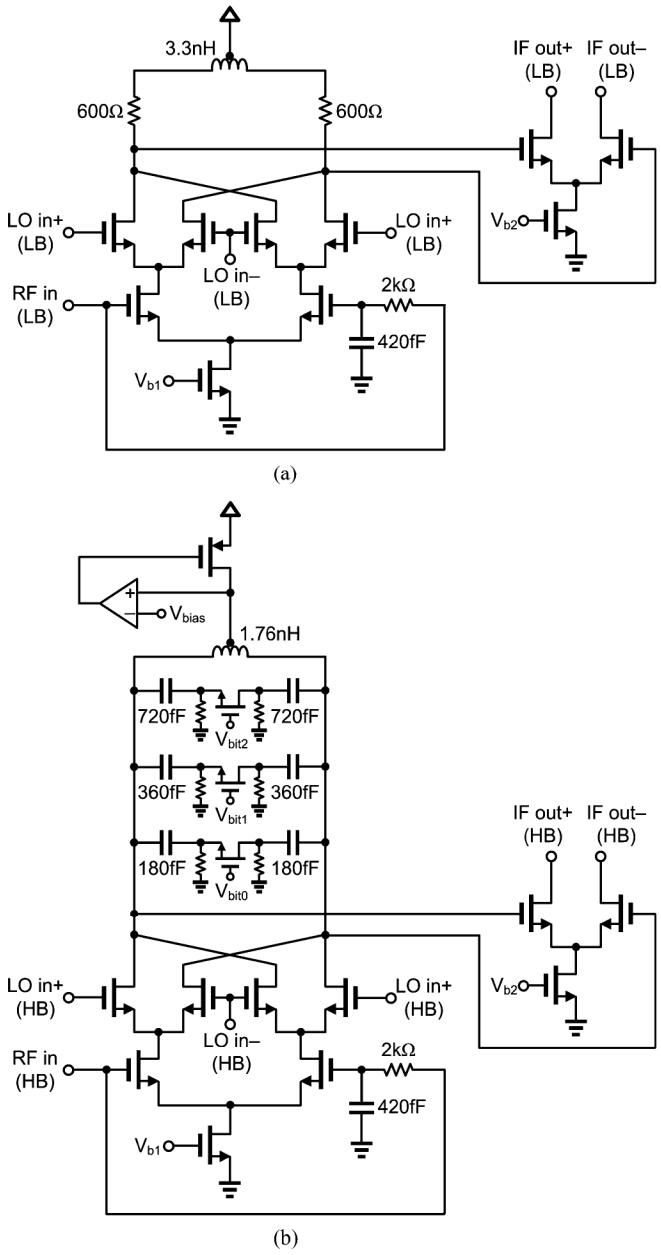

Fig. 7. Schematic of the RF mixer and IF buffer for (a) LB and (b) HB.

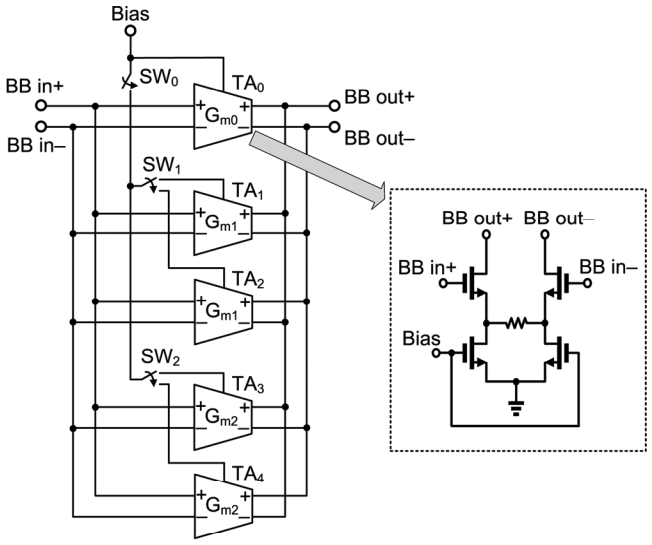

Fig. 8. Baseband VGA.

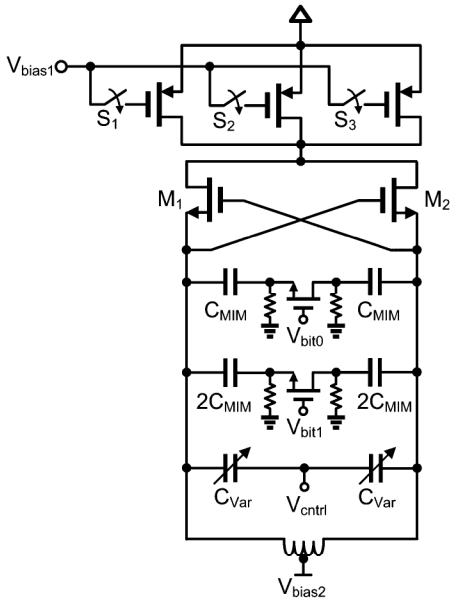

Fig. 9. Schematic of the wideband VCO.

signal and noise. Note that the noise figure requirement of the TCA is relaxed to a significant degree due to the low-noise active antenna module that will be deployed in front of the CMOS receiver in the array system (Fig. 3).

Through an in-depth investigation of several potential topologies, the TCA is implemented in a parallel cascode configuration with an active termination [21], as shown in Fig. 6. The cascode amplifiers not only enhance the isolation between the two output signals, but also minimize the crosstalk of noise produced by the active blocks.

The wideband input matching to 50 Ω is achieved by an active termination with shunt resistive feedback and an impedance transformation network. The active termination contributes less noise to the subsequent blocks than a simple shunt resistive termination [22].

The RF signals at two frequencies are then selectively amplified by two separate cascode amplifiers (M_1–M_2, M_3–M_4) that have tunable LC output loads. A 3-bit switched capacitor bank at each output load is tuned to cover the entire LB and HB frequencies. This allows for the digital tuning of the amplifier so that it can provide the maximum gain at the desired frequency while attenuating out-of-band signals prior to the first down-conversion.

B. Mixers

Four different mixer designs are presented in the receiver; RF and IF mixers, each for LB and HB, respectively. The current-commutating double-balanced topology is adopted for all the mixers in order to minimize the LO-to-IF feedthrough. Fig. 7(a) shows the schematic of the RF mixer and IF buffer for LB. A shunt-peaking inductor (3.3 nH) is used to extend the IF 3-dB

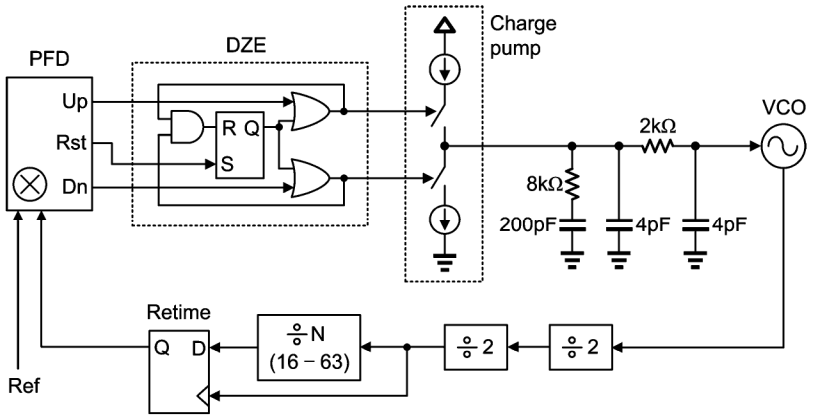

Fig. 10. Block diagram of the programmable PLL.

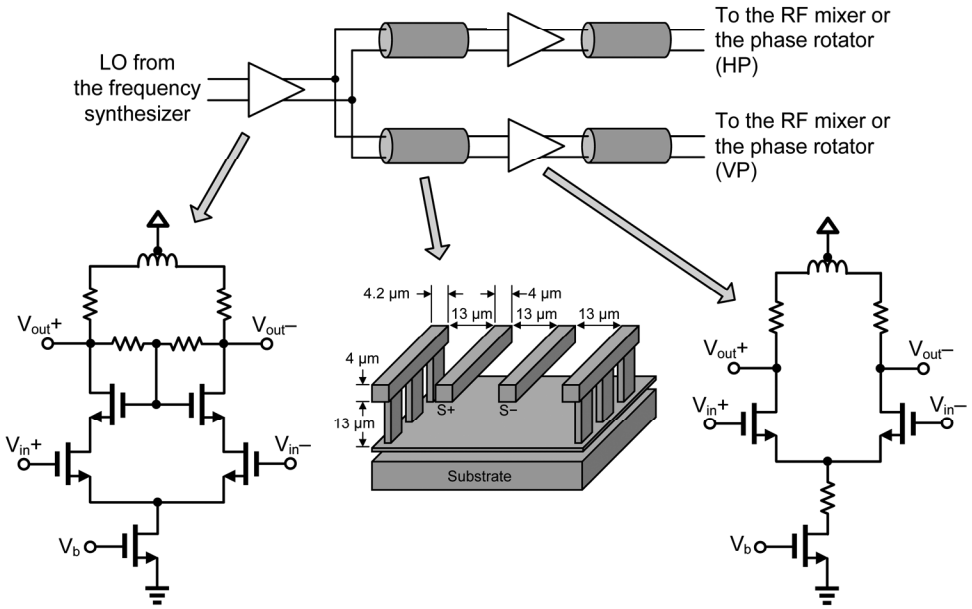

Fig. 11. LO distribution and buffers.

bandwidth up to over 3.5 GHz. Since the TCA provides a single-ended RF signal to the differential RF mixers, one RF input terminal is terminated to a bias voltage by a 2-kΩ resistor and a bypass capacitor.

The HB RF mixer employs a tunable LC load with a 3-bit switched capacitor bank at the IF output, as shown in Fig. 7(b). The resonant frequency of the LC load is tuned in such a way that the conversion gain is maximized at the desired IF frequency. The common-mode feedback circuitry ensures a given bias voltage ($\mathrm{V_{bias}}$) set for the subsequent buffer block.

The schematic of the IF mixers for LB and HB are similar to that of the LB RF mixer. The difference is that the IF mixers employ no shunt-peaking inductors and are degenerated by source resistors to improve linearity of the baseband signal.

C. Baseband Variable-Gain Amplifier (VGA)

The VGA combines five transconductance amplifiers in the current domain with digitally switched bias voltages (Fig. 8). $\mathrm{TA_1}$ and $\mathrm{TA_2}$, $\mathrm{TA_3}$ and $\mathrm{TA_4}$ are identical pairs that constitute current-commutating cells by digital switches ($\mathrm{SW_1}$ and $\mathrm{SW_2}$). Each transconductance amplifier has a differential common-source topology with resistive degeneration. Since the output port is configured with open drains, the output signals from each array element can be easily combined in the current domain using a passive network which imposes little additional impact on the nonlinearity performance. The open-drain output requires an external DC supply of 1.5 V. The VGA achieves a nominal gain of 7 dB with a 11 dB gain variation in five steps when driving a 100-Ω differential output load.

D. Voltage-Controlled Oscillator (VCO)

Two separate LC VCOs are implemented to generate the LO signals for LB and HB, respectively. The schematic is shown in Fig. 9. A cross-coupled PMOS pair ($\mathrm{M_1}$ and $\mathrm{M_2}$) is used to improve the phase noise performance in the $1/f^3$ region. In order to accomplish a wideband tuning range with relatively low VCO gain (resulting in low phase noise), a two-step frequency tuning mechanism is adopted [23]. The first coarse tuning is fulfilled by 2-bit binary-weighted MIM capacitors ($\mathrm{C_{MIM}}$ and

$2C_{MIM}$) in the LC tank. Then, MOS varactors (C_{Var}) are used for the further fine and continuous frequency tuning.

The bias current is controlled digitally (S_1–S_3) to ensure that the VCO operates in the current-limited regime over the wide-band tuning range. This is beneficial for further improvement of phase noise [24]. The simulated phase noise ranges from −112 to −103 dBc/Hz and from −108 to −94 dBc/Hz at 1-MHz offset for the LB and HB VCOs, respectively.

E. Phase-Locked Loop (PLL)

Two fully-programmable PLLs are implemented to independently synthesize the LO frequencies for the two different bands [25]. Fig. 10 presents a block diagram of the PLL circuitry commonly used for both LB and HB. The programmable dynamic divider takes one quarter of the VCO output frequency and provides a further division ratio between 16 and 63. The divided output is retimed to the dynamic divider input for noise improvement and feeds the phase-frequency detector (PFD). To reduce the output jitter, a dead-zone elimination (DZE) circuitry is employed, followed by a charge-pump and a third-order loop filter to feed the VCO control voltage. The core PLL circuitry draws 34 mA at 1.2 V DC.

F. Multiplexer

As the receiver has a dual-IF frequency scheme discussed in Section IV-B, the LO_2 frequency needs to switch between 1/8 ($LO_{2_{1/8}}$) and 1/2 ($LO_{2_{1/2}}$) of the LO_1 frequency by a 2:1 multiplexer. Two cascode transconductance stages, each driven by either $LO_{2_{1/8}}$ or $LO_{2_{1/2}}$, are combined in the current domain. Then, the output signal is selected between the two by complementary switches that turn on or off the bias current of each transconductance stage. Two separate multiplexers are used for the I and Q components of the LO_2 signal.

G. LO Distribution and Buffers

The LO_1 and LO_2 signals generated from the frequency synthesizers are distributed to the RF mixers and the phase rotators, respectively, as shown in Fig. 11. Due to the high-level of integration in the single receiver chip, the LO distribution length becomes as long as 3.7 mm in the worst case (the LO_1 distribution for LB). The LO buffers need to compensate for the insertion loss and bandwidth limitation caused by the long signal distribution. Each path of the LO distribution includes a two-stage buffer, which is a self-biased cascode as the first stage followed by a common-source amplifier with shunt peaking. The shunt-peaking inductance is carefully chosen, such that the 3 dB bandwidth is higher than the maximum LO frequency in the distribution without raising a significant gain peaking and instability issue [26].

The transmission line used for the LO distribution is implemented by a grounded differential coplanar waveguide (CPW) structure, shown in Fig. 11. In order to minimize the insertion loss, the top thick metal layer (4-μm aluminum) is used for the signal lines (S+ and S−). The simulated insertion loss of the CPW with $Z_{odd} = 50\ \Omega$ is 0.35 dB per mm at the highest LO frequency, i.e., 12 GHz. The side and bottom ground planes improve the isolation between adjacent LO signals in distribution [27].

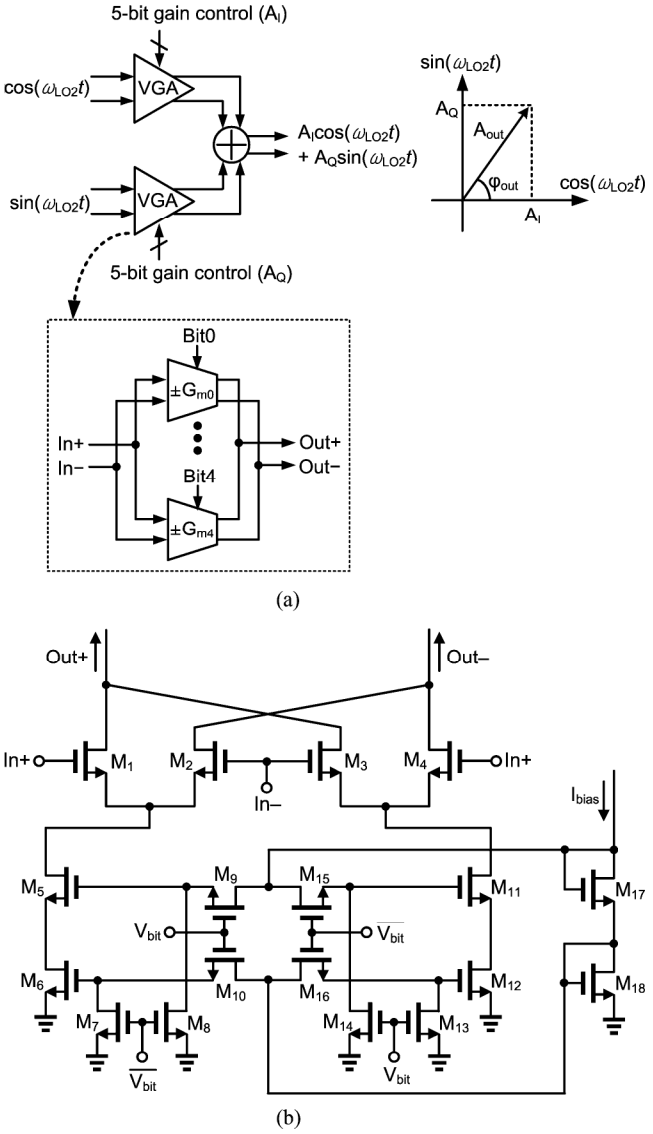

Fig. 12. (a) Block diagram of the 10-bit digital phase rotator. (b) Unit current-commutating cell.

H. Phase Rotator

A block diagram of the digital linear phase rotator is shown in Fig. 12(a). It takes the I and Q components of the LO_2 signal as an input and applies a different gain (A_I and A_Q) independently to each of them using two digitally-controlled VGAs [28]. By adding the two VGA outputs in the current domain, the desired phase (φ_{out}) and amplitude (A_{out}) can be interpolated in the Cartesian coordinates of the I and Q outputs. Each VGA is implemented by combining five binary-weighted current-commutating cells. Fig. 12(b) shows the schematic of a unit current-commutating cell. M_1–M_4 are transconductance transistors with identical dimensions. The output signal (Out+ and Out−) changes its polarity depending on the bias control bit (V_{bit}). This full-scale current-commutating scheme makes the phase interpolating performance less vulnerable to the PVT (process, voltage, and temperature) variations.

Since five bits are assigned to each VGA, the phase rotator is able to interpolate 1024 (2^{10}) different points over all the four

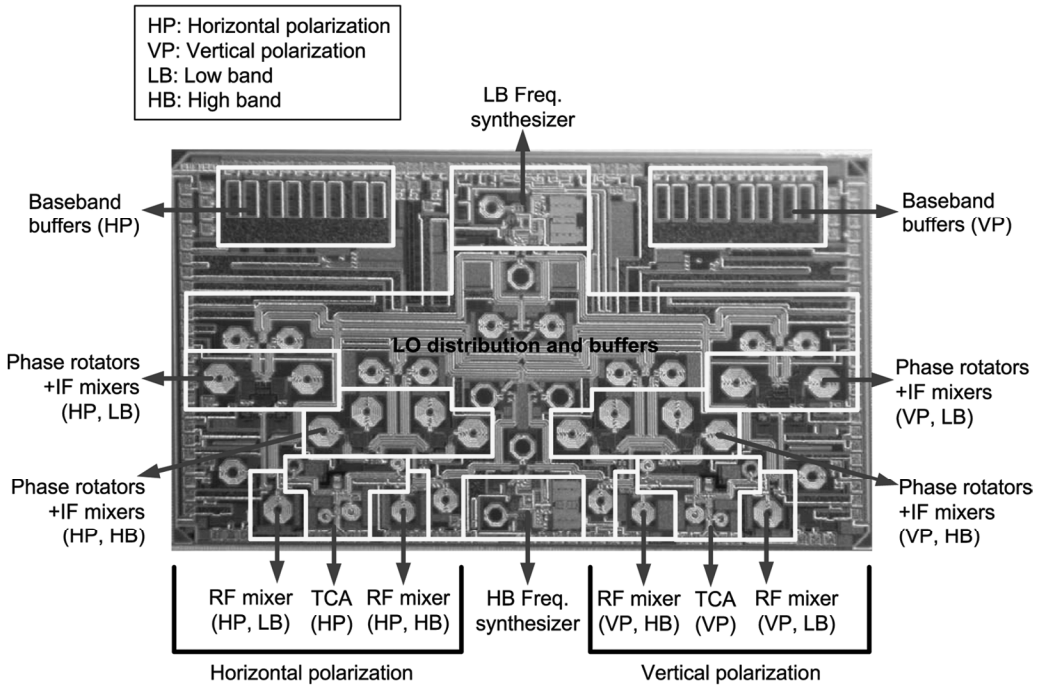

Fig. 13. Chip micrograph.

quadrants of the output Cartesian coordinate. The scheme brings in theory an rms phase error of 0.3° with sufficiently large amplitudes to drive the switching mixers, regardless of the operating frequency.

VI. Experimental Results

The phased-array receiver element is implemented in a 130-nm CMOS process. It provides eight metal layers including top two thick metal layers of 4-μm aluminum and 3-μm copper. Fig. 13 shows a die micrograph of the implemented chip that occupies an area of 3.0×5.2 mm^2.

In this section, the experimental results of the receiver element are presented. Then, followed is the measured array pattern of a four-element phased-array system that is implemented using four receiver chips as a feasibility demonstration toward very large-scale arrays.

For the measurement of the receiver element, a printed circuit board (PCB) is designed on a Duroid substrate of a 0.254-mm thickness. The PCB provides the traces for the DC supplies, reference signal, digital signals, and differential baseband outputs. All signal inputs and outputs are fed with SMA connectors. The PCB is attached on a gold-plated brass board. Then, through a pre-cut aperture of the PCB, the chip is mounted directly on the brass board using silver epoxy in order to provide good substrate grounding and heatsink. The chip pads are wire-bonded to the PCB traces except that the ground pads are wire-bonded directly to the brass board.

A block diagram of the measurement setup is shown in Fig. 14. The RF input signal is fed by a coplanar GSG probe to minimize the feed loss. Off-chip baluns convert the differential baseband output to a single-ended one for the measurement purpose. There are three different DC supplies applied to the chip; 1.6 V and 2.7 V for the RF and LO circuitry and 1.5 V

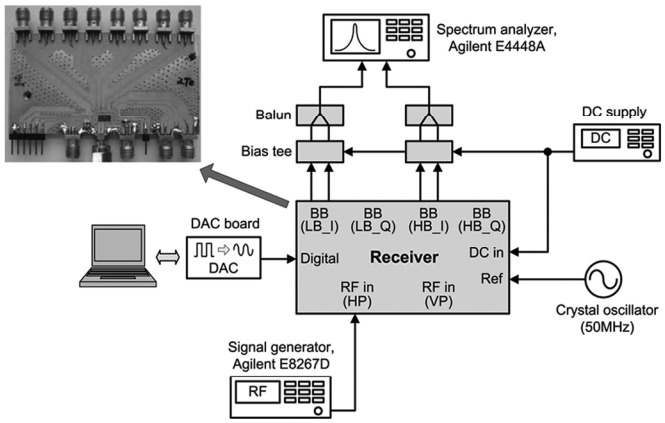

Fig. 14. Receiver measurement setup.

for the baseband buffers. A temperature-compensated crystal oscillator with phase noise of -155 dBc/Hz at 1-kHz offset provides a 50-MHz reference signal for the on-chip PLLs. Digital codewords of 170 bits are generated by an external DAC board.

The measured performance of the on-chip LO generation is shown in Fig. 15, where the LO frequency is plotted versus the VCO control voltage for LB and HB, respectively. Each curve represents one of the four different settings of the 2-bit switched MIM capacitors in the VCO. As expected, the synthesizers are able to generate 4.8–7.8 GHz and 8.8–12.5 GHz of LO signals for LB and HB, respectively without any blind spot. This result satisfies the required LO frequency range for the down-conversion of RF signals over the entire tritave (see Section IV-B). The phase noise of the frequency synthesizers is below -95 dBc/Hz at an offset of 100 kHz over the entire LO

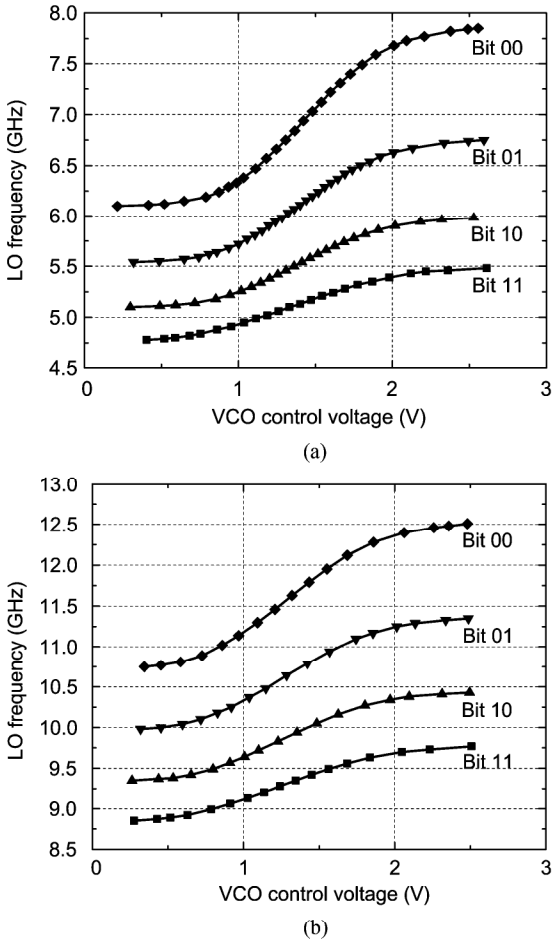

Fig. 15. Measured performance of the on-chip frequency synthesizers: (a) LB; (b) HB.

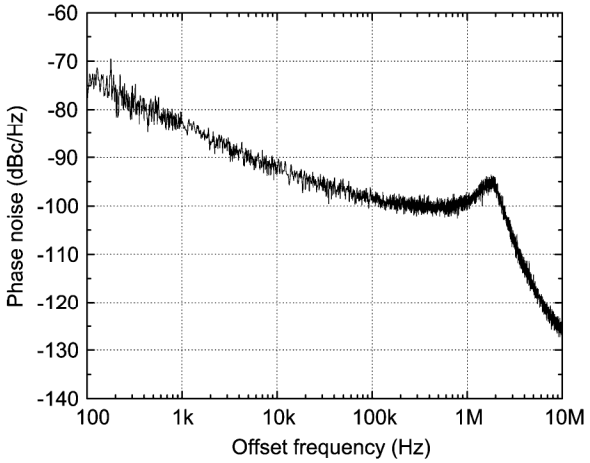

Fig. 16. Measured phase noise of the HB frequency synthesizer at 9.4 GHz.

frequencies of 5–7 GHz and 9–12 GHz. Fig. 16 shows the measured phase noise of the HB frequency synthesizer at 9.4 GHz.

Fig. 17 plots the measured conversion gain of the receiver. The maximum and the minimum gains achievable with different baseband VGA settings are shown in dashed lines. The solid line with markers represents the nominal gain with the optimum VGA settings, which ranges from 16 to 24 dB across the entire

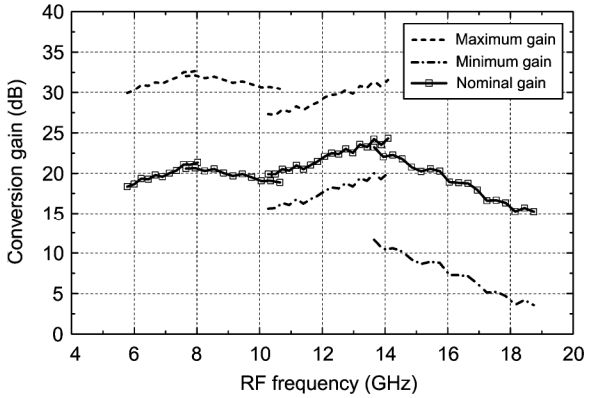

Fig. 17. Measured conversion gain.

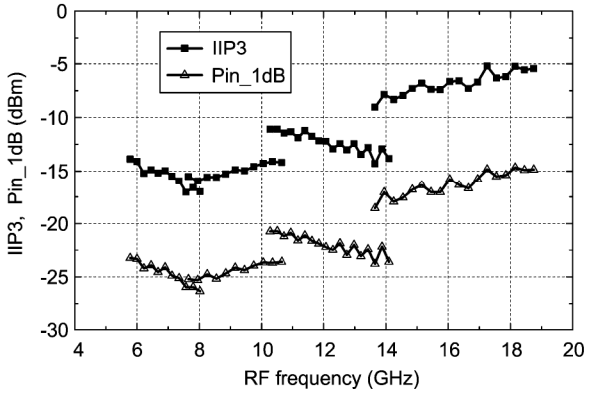

Fig. 18. Measured nonlinearity performance: input-referred IP3 and 1-dB compression.

tritave band. The discontinuities at 7.6, 10.4, and 13.5 GHz are due to the switching of either the frequency band or the IF frequency scheme.

The measured nonlinearity performance is shown in Fig. 18. The third-order intercept point (IP3) is measured by applying a two-tone signal with 10-MHz spacing. The input-referred power of IP3 and 1-dB compression does not vary with different VGA gain settings. This is because the VGA is configured by the full-scale current-commutating cells that keep the same nonlinearity performance regardless of the signal polarity.

The RF input return loss is better than 9.8 dB across the entire band as shown in Fig. 19. The input-matching performance does not vary with different LC load settings of the TCA, due to the high isolation between the input and the output of the cascode stage (Fig. 6).

The noise figure is measured by a standard Y-factor method [29]. Fig. 20 shows the measured noise figure of the CMOS receiver, which ranges from 8 to 14 dB over the entire band. However, taking into account a preceding wideband active antenna module in the complete system (Fig. 3), the noise contribution of the CMOS receiver to the system will be significantly reduced. The noise figure of the complete system that includes the CMOS receiver and the preceding module with a 2.5-dB noise figure and a 20-dB gain is also plotted in the dashed line.

Since the receiver supports a concurrent dual-band and dual-polarization signal, it is very important to characterize the isolation performance between the two bands and between the two

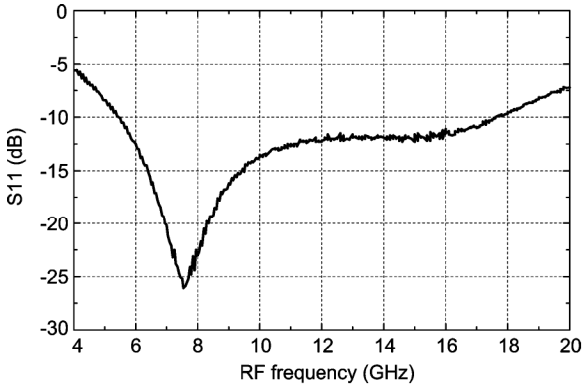

Fig. 19. Measured input matching performance with the TCA input probed on-wafer.

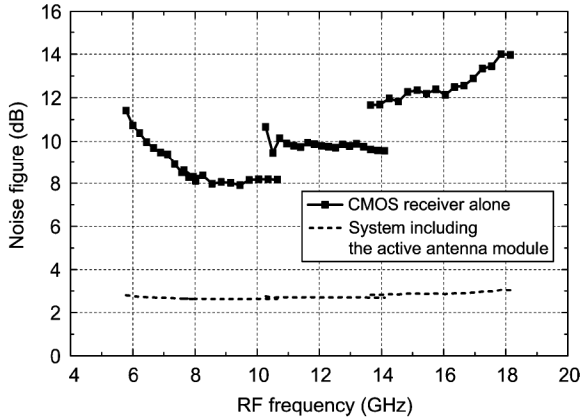

Fig. 20. Measured noise figure of the CMOS receiver (solid line with markers) and the complete system including the active antenna module (dashed line).

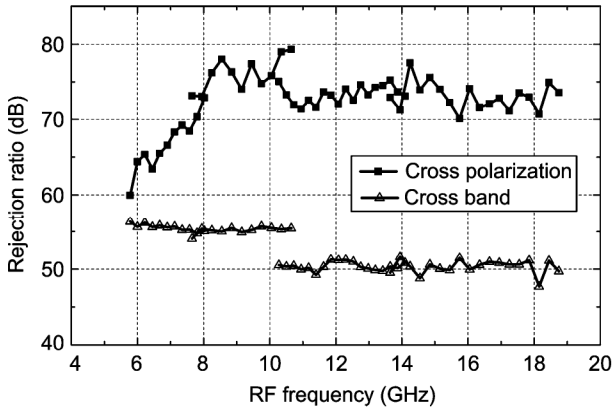

Fig. 21. Measured isolation performance: Cross-band and cross-polarization rejection ratios.

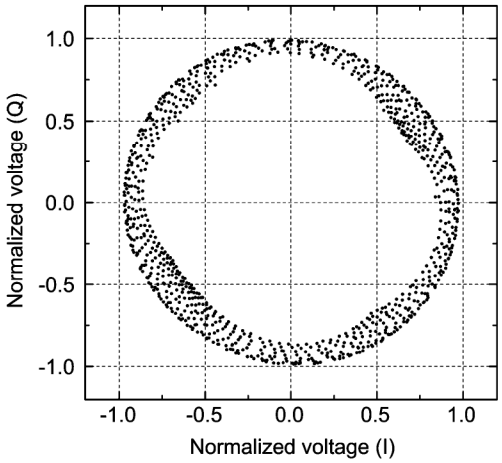

Fig. 22. Measured constellation of the interpolated baseband output at RF frequency of 18 GHz.

polarizations. For the isolation measurement, a rejection ratio is defined as a ratio of the undesired signal power, which is cross-coupled from different bands or polarizations, to the desired signal power at the output port. For example, in order to measure the cross-band rejection ratio at the LB output port, a two-tone signal containing one LB tone and one HB tone is applied with the same input power level. Then, the rejection ratio of the HB signal (the undesired cross-coupled output) is measured with reference to the LB signal (the desired output) at the LB output port. As shown in Fig. 21, the cross-band rejection ratio is more than 48 dB across the entire band. In addition, the cross-polarization rejection ratio is measured to be 63 dB in the worst case. This indicates that the rejection ratio in the entire system will not be limited by the CMOS chip but rather determined by the preceding antenna module.

Finally, the phase-shifting performance of the receiver is characterized. A relative delay of the down-converted baseband signal is measured by a digital oscilloscope while varying the LO phase with 1024 different interpolating points of the phase rotator. Fig. 22 shows a measured constellation of the interpolated baseband output at the RF frequency of 18 GHz. Each single point represents an interpolated output set by each particular phase rotator setting. The nonuniform distribution in the constellation is due to the unavoidable I and Q mismatch in the LO signal and the dispersive interpolation of harmonic components. As can be seen, it is a very dense constellation with a small amplitude variation. When we shift the phase to any arbitrary angle over 360°, the RMS phase error is 0.3° with an RMS amplitude variation of 0.4 dB. The performance at other RF frequencies is summarized in Table I. The worst-case RMS phase error is only 0.5°. It turns out from the array measurement that the fine resolution of the on-chip phase shifting brings accurate beamforming performance.

TABLE I
MEASURED PERFORMANCE OF THE PHASE ROTATOR

RF freq. (GHz)	RMS phase error (deg)	Max. phase error (deg)	RMS amplitude variation (dB)	Max. amplitude variation (dB)
6	0.5	2.7	0.3	1.7
10.35	0.2	1.2	0.2	1.7
14	0.3	1.4	0.2	1.7
18	0.3	1.3	0.4	1.7

A four-element phased-array receiver system is built by employing and incorporating four CMOS receiver chips. To characterize the array performance, we adopts an electrical way of feeding the incoming RF wave, where four external variable phase shifters are used to emulate the incoming wavefront at a given incident angle.

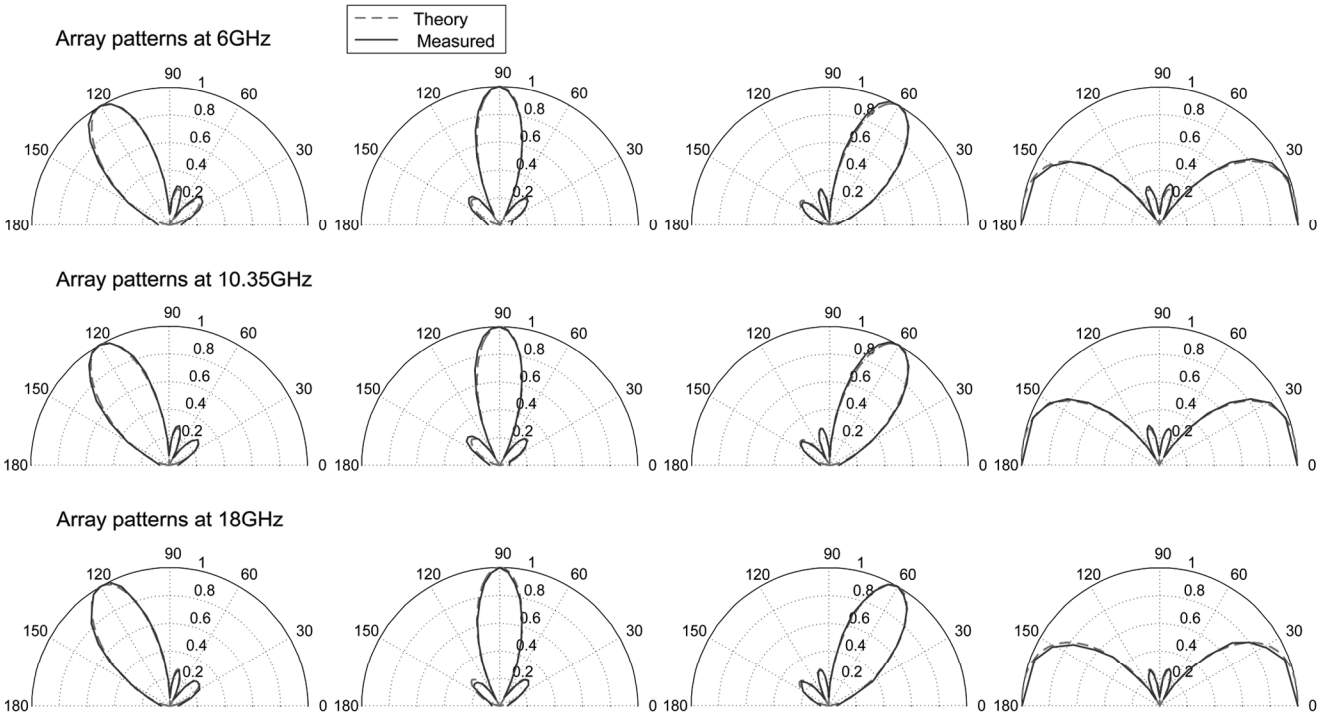

Fig. 23. Measured array patterns of the four-element array with theoretical patterns superimposed. The antenna spacing is assumed to be a half wavelength at each frequency.

TABLE II
MEASURED PERFORMANCE SUMMARY

Receiver Element Performance

Conversion gain (6 – 18GHz)		16.3 ~ 24.3dB
Input-referred 1-dB compression (6 – 18GHz)		−26.3 ~ −14.8dBm
Input-referred IP3 (6 – 18GHz)		−17.0 ~ −5.2dBm
Input return loss (6 – 18GHz)		> 9.8dB
Cross-polarization rejection (6 – 18GHz)		> 63.4dB
Cross-band rejection (6 – 18GHz)		> 48.8dB
LO leakage (6 – 18GHz)		< −24.5dBm
Antenna-to-baseband noise figure† (6 – 18GHz)		2.6 ~ 3.1dB
RMS Phase-shifting error (6 – 18GHz)		< 0.5° (within 0.4-dB RMS amplitude variation)
RF channel spacing		225MHz (Div8 LO_2), 300MHz (Div2 LO_2)
Power consumption	RF and LO circuitry	658mA @2.7V, 217mA @1.6V
	Baseband buffers	34mA @1.5V each buffer
Technology		130nm CMOS
Die area		3.0×5.2 mm^2

†Including the active antenna module in the system.

Phased-Array Performance (four elements)

Number of beams concurrently receivable	4
Phase shifting resolution per element (6 – 18GHz)	Continuous with 0.5° RMS phase error max.
Total phased-array gain (6 – 18GHz)	28.3 ~ 36.3 dB
Beam-forming peak-to-null ratio	> 21.5dB

The measured array patterns at 6, 10.35, and 18 GHz are shown in Fig. 23. Four different beam-pointing angles are set at each different RF frequency. Theoretical patterns are superimposed on the measured ones. It can be seen that the measured beam patterns are well steered in excellent agreement with the theoretical ones. The worst case peak-to-null ratio is 21.5 dB. This good array performance is attributed to the fine resolution of the on-chip phase shifting that enables a precise digital

array calibration. The calibration offsets the process variation between different element chips and the inevitable systematic skews in phase and amplitude originating from the reference and RF signal distribution to array elements. Each element should be calibrated once at each RF frequency. In addition, the array beam-pointing angle can be steered with a high resolution over the entire direction (the incident angle between -90° and 90°) due to the low RMS error of the on-chip phase shifting (see Table I).

Each array element draws 658 mA and 217 mA for the RF and LO circuitry from DC supplies of 2.7 V and 1.6 V, respectively. Each baseband buffer draws 34 mA from a 1.5-V DC supply. It should be noted that this array forms four beams concurrently over a tritave bandwidth, which demands higher power consumption compared to other narrowband single-beam arrays. However, the power consumption can be further reduced by revising the LO distribution circuitry with inductorless design, which will decrease the LO distribution length and thus the power required at the LO buffers. Table II summarizes the measurement results of the receiver element and the four-element phased array.

VII. Conclusion

In this paper, an integrated CMOS phased-array receiver that supports concurrent dual-band and quad-beam signals from 6 to 18 GHz has been presented. Since all receiver-module components are integrated in a single CMOS chip except for the antenna and LNA, the receiver is easily scalable to build a very large-scale (e.g., millions of array elements) phased-array system with low cost, low complexity, and high reliability. For a demonstration of the array performance, a four-element phased-array system has been implemented using four receiver chips. Owing to the fine resolution of on-chip phase shifting and the precise digital calibration, we achieved the array patterns that agree well with the theoretical ones. To the authors' best knowledge, this is the first concurrent multiband multibeam phased-array receiver in a tritave bandwidth, implemented in CMOS.

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Sanggeun Jeon (S'05–M'06) received the B.S. and M.S. degrees in electrical engineering from the Seoul National University, Seoul, Korea, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, in 2004 and 2006, respectively.

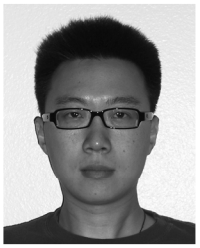
From 1999 to 2002, he was a Full-Time Instructor in electronics engineering at the Korea Air Force Academy. From 2006 to 2008, he was a Research Engineer in the Caltech High-Speed Integrated Circuits Group, where he was involved with CMOS phased-array receiver design. In 2008, he joined the School of Electrical Engineering at Korea University, Seoul, as an Assistant Professor. His research interests include high-efficiency power amplifiers, oscillators, nonlinear stability analysis, and CMOS communication circuits.

Dr. Jeon was the recipient of the Third Place Award in the Student Paper Competition at the 2005 IEEE MTT-S International Microwave Symposium.

Yu-Jiu Wang (S'04) received the B.S. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 2001, and the M.S. degree in electrical engineering from the California Institute of Technology, Pasadena, in 2006, where he is currently pursuing the Ph.D. degree in electrical engineering.

He was a research assistant with the MMIC group in National Taiwan University, where he studied Q-band and V-band compound semiconductor MMICs from 1999 to 2001. He served as a naval officer for the obligatory military service from 2001 to 2003. He was an assistant instructor for the Electronics Laboratory at NTU from 2003 to 2004.

Mr. Wang was the First Prize winner of the National Physics Competition and the Silver Medal winner of the 27th and 28th International Physics Olympiad, in Oslo, Norway, in 1996 and Ontario, Canada, in 1997, respectively. He also led a team to win the championship in the National Entrepreneurship Competition.



Hua Wang received the B.S. degree from Tsinghua University, Beijing, China, in 2003, and the M.S. degree from the California Institute of Technology (Caltech), Pasadena, in 2007. He is currently working toward the Ph.D. degree in electrical engineering at Caltech.

Mr. Wang was the recipient of the Charles Lee Powell Fellowship in 2004 and 2005, the Dr. Ko Future Entrepreneurs Scholarship in 2008, and the ISSCC Analog Devices Inc. Outstanding Student Designer Award in 2008.

Florian Bohn (S'07) received the B.S. degree with honors in electrical engineering from the California Institute of Technology, Pasadena, and the M.S. degree in electrical and computer engineering from the University of California, Santa Barbara, in 2001 and 2003, respectively.

From 2003 to 2005, he worked as an RF IC Design Engineer with Axiom Microdevices Inc., Irvine, CA. At Axiom, he focused on the design and testing of active and passive circuits for GSM/GPRS CMOS power amplifiers. He is currently pursuing the Ph.D. degree in electrical engineering at the California Institute of Technology, where he has worked on frequency synthesizers. His research interests lie in the area of integrated micro- and millimeter-wave transceiver circuits and systems.

Mr. Bohn has received a Connexant Scholarship and an Analog Devices Outstanding Student Designer Award.

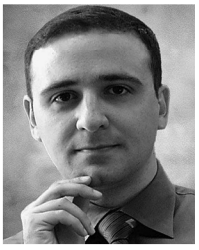
Arun Natarajan received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Madras, in 2001 and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, in 2003 and 2007, respectively.

He joined IBM in 2007 and is presently a Research Staff Member at the IBM T. J. Watson Research Center, Yorktown Heights, NY. His research focuses on the design of high-frequency integrated circuits. His current research interests include RF and analog circuit design, wireless transceivers, and multiple-antenna system design.

Dr. Natarajan received the Caltech Atwood Fellowship in 2001, the Analog Devices Outstanding Student IC Designer Award in 2004, and the IBM Research Fellowship in 2005.

Aydin Babakhani (S'03–M'08) received the B.S. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran, in 2003. He received the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, in 2005 and 2008, respectively. He is currently a Postdoctoral Scholar at the California Institute of Technology.

Mr. Babakhani is the Vice Chair of the IEEE Microwave Theory and Techniques Society Metro LA/SFV Joint Sections MTT-S Chapter 17.1. He was the recipient of the Microwave Graduate Fellowship in 2007, the Grand Prize in the Stanford-Berkeley-Caltech Innovators Challenge in 2006, ISSCC 2005 Analog Devices Inc. Outstanding Student Designer Award, and Caltech Special Institute Fellowship and Atwood Fellowship in 2003. He was also the Gold Medal winner of the National Physics Competition in 1998 and the Gold Medal winner of the 30th International Physics Olympiad in 1999, Padova, Italy.



Ali Hajimiri (S'95–M'99) received the B.S. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1996 and 1998, respectively.

He was a Design Engineer with Philips Semiconductors, where he worked on a BiCMOS chipset for GSM and cellular units from 1993 to 1994. In 1995, he was with Sun Microsystems, where he worked on the UltraSPARC microprocessor's cache RAM design methodology. During the summer of 1997, he was with Lucent Technologies–Bell Labs, Murray Hill, NJ, where he investigated low-phase-noise integrated oscillators. In 1998, he joined the faculty of the California Institute of Technology, Pasadena, where he is a Professor of electrical engineering and the Director of Microelectronics Laboratory. He is a cofounder of Axiom Microdevices Inc. His research interests are high-speed and RF integrated circuits. He is the author of *The Design of Low Noise Oscillators* (Springer, 1999) and has authored or coauthored more than 100 refereed journal and conference technical articles. He holds more than 30 U.S. and European patents.

Dr. Hajimiri is a member of the Technical Program Committee of the IEEE International Solid-State Circuits Conference (ISSCC). He has also served as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–PART II, a Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, a member of the Technical Program Committees of the International Conference on Computer Aided Design (ICCAD), and the Guest Editorial Board of Transactions of Institute of Electronics, Information and Communication Engineers of Japan (IEICE).

Dr. Hajimiri was selected to the top 100 innovators (TR100) list in 2004 and is a Fellow of the Okawa Foundation. He is a Distinguished Lecturer of the IEEE Solid-State and Microwave Societies. He is the recipient of Caltech's Graduate Students Council Teaching and Mentoring Award as well as Associated Students of Caltech Undergraduate Excellence in Teaching Award. He was the Gold Medal winner of the National Physics Competition and the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, The Netherlands. He was a corecipient of the IEEE JOURNAL OF SOLID-STATE CIRCUITS Best Paper Award of 2004, the ISSCC Jack Kilby Outstanding Paper Award, two times corecipient of CICC's Best Paper Awards, and a three times winner of the IBM faculty partnership award as well as National Science Foundation CAREER award.