Resistive-Feedback CMOS Low-Noise Amplifiers for Multiband Applications

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***Abstract*—Extremely compact resistive-feedback CMOS low-noise amplifiers (LNAs) are presented as a cost-effective alternative to multiple narrowband LNAs using high-Q inductors for multiband wireless applications. Limited linearity and high power consumption of the inductorless resistive-feedback LNAs are analyzed and circuit techniques are proposed to solve these issues. A 12-mW resistive-feedback LNA, based on current-reuse transconductance boosting is presented with a gain of 21 dB and a noise figure (NF) of 2.6 dB at 5 GHz. The LNA achieves an output third-order intercept point (IP3) of 12.3 dBm at 5 GHz by reducing loop-gain rolloff and by improving linearity of individual stages. The active die area of the LNA is only 0.012 mm^2.**

A 9.2-mW tuned resistive-feedback LNA utilizing a single compact low-Q on-chip inductor is presented, showing an improved tradeoff between performance, power consumption, and die area. At 5.5 GHz, the fully integrated LNA achieves a measured gain of 24 dB, an NF of 2 dB, and an output IP3 of 21.5 dBm. The LNA draws 7.7 mA from the 1.2-V supply and has a 3-dB bandwidth of 3.94 GHz (4.04–7.98 GHz). The LNA occupies a die area of 0.022 mm^2. Both LNAs are implemented in a 90-nm CMOS process and do not require any costly RF enhancement options.

***Index Terms*—CMOS low-noise amplifier (LNA), feedback amplifiers, multiband wireless receivers.**

I. Introduction

LOW-NOISE amplifiers (LNAs) occupy a significant percentage of the total die area in wireless front-ends today. This is because the performance of the LNA is dependent on the Q's of the multiple on-chip inductors. Since the area requirement of high-Q on-chip inductors is high, the die area occupied by the LNA is also high. Often, costly process steps are required to enhance the Q of the on-chip inductors to further improve the performance of RF circuits. The design of these circuits usually requires a higher number of simulation and verification iterations. Cascode amplifiers with inductive source degeneration [1], the predominant LNA implementation used in CMOS wireless front-ends, require three high-Q inductors for achieving input impedance matching, high gain, and low noise figure (NF). In spite of the high die area requirements, cascode LNAs have been used extensively in narrowband wireless applications because they provide high gain, low noise, and high linearity at relatively low power consumption. With the advent of multiple-input multiple-output (MIMO), multistandard, and multiband wireless systems; however, the use of the area intensive cascode LNAs is becoming increasingly expensive, leading to the pursuit of alternative LNA implementations.

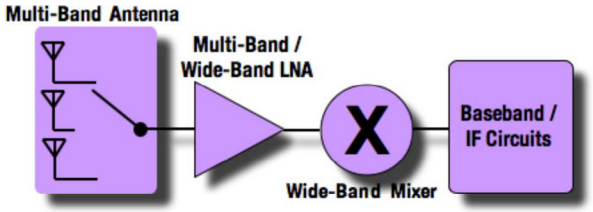

Fig. 1. Multiband receiver implementation using a multiband/wideband LNA.

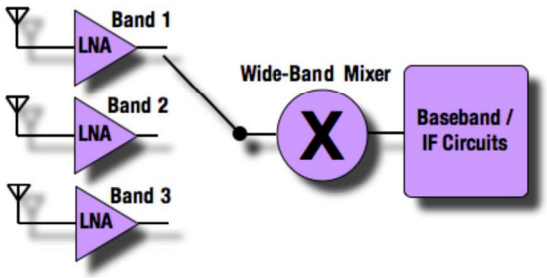

Fig. 2. Multiband receiver implementation using multiple narrowband LNAs.

A multiband receiver can be implemented by using a single multiband or wideband LNA, as shown in Fig. 1. Cascode LNAs based on inductive source degeneration are not suitable for this implementation since it is extremely difficult to switch the three on-chip inductors to make the same cascode LNA work across all the required frequency bands without compromising performance. Multiband receivers can also be implemented by using multiple narrowband LNAs, each designed for a different frequency band, as shown in Fig. 2. If cascode LNAs with inductive degeneration are used for this implementation, the die area and cost will both be prohibitively high.

Inductorless resistive-feedback CMOS LNAs [2]–[4] have been shown to be a viable option for implementing multiband receivers, as shown in Fig. 1. These circuits require very small die area and can be implemented in a digital CMOS process without any additional RF enhancements. Hence, this approach can potentially significantly reduce the cost of the wireless front-end implementation. Resistive-feedback LNAs achieve

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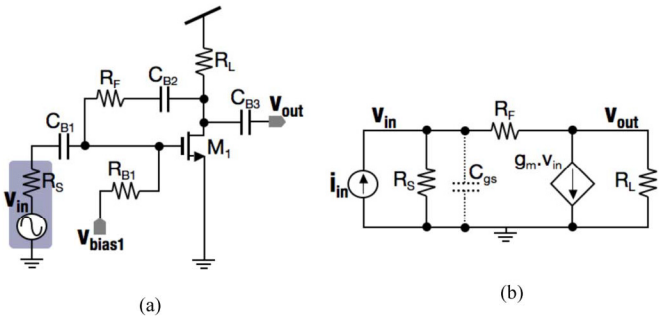


(a) (b)

Fig. 3. Simplified schematic and small-signal model of a shunt-shunt feedback amplifier.

high gain and reasonably low NF [4]. However, novel circuit techniques are required to reduce power consumption and improve linearity.

This paper presents an inductorless resistive-feedback LNA in which a current-reuse transconductance-boosting technique [5] is utilized to reduce the power consumption to 12 mW. The LNA has a gain of 21 dB and an NF of 2.6 dB at 5 GHz. The active die area of this circuit is only 0.012 mm^2. The combination of small die area, broad bandwidth and moderate power consumption make this LNA architecture suitable for low-cost multistandard wireless front-ends, as shown in Fig. 1. By maintaining a moderate loop-gain across the frequency band and reducing the nonlinearities of individual stages, the LNA achieves an output third-order intercept point (IP3) of 12.3 dBm at 5 GHz. Techniques to further improve IP3 by nonlinearity cancellation [6]–[9] are also presented.

A resistive-feedback cascode LNA using a single compact on-chip load inductor is presented next. It has a maximum gain of 24.4 dB, and a 3-dB bandwidth of 3.94 GHz (4.04–7.98 GHz). At 5.5 GHz, the NF is 2 dB, and the output IP3 is 21.5 dBm. Since the inductor Q is not required to be high, the area of this LNA is only 0.022 mm^2. This makes it suitable for multiband receiver implementations, as shown in Fig. 2. This LNA can also be easily modified to operate across multiple frequency bands (as in Fig. 1) since the single low-Q tuned load can be switched to resonate at different frequencies.

The gain, input impedance, NF, and linearity of resistive-feedback LNAs are discussed in Section II. Section III describes circuit techniques to improve linearity and lower power consumption. The design of the inductorless LNA with current-reuse transconductance boosting and the tuned resistive-feedback LNA (using a compact low-Q inductor) are described in Section III. The implementation details of these circuits are discussed in Section IV. The measurement results of both the LNAs are given in Section V along with performance comparison to other reported circuits. Finally, conclusions are presented in Section VI.

II. Resistive-Feedback LNA Theory

Consider a simplified resistive-feedback amplifier, as shown in Fig. 3(a). M_1 represents the input transconductance device, which could be a single transistor or a cascode pair. R_L represents the load resistance including the output resistance of the input transconductance stage. R_F is the resistor implementing the shunt–shunt feedback. R_S is the source resistance and R_{B1} is used for biasing along with dc blocking capacitors C_{B1}, C_{B2}, and C_{B3}. The equivalent small-signal model of the transimpedance amplifier is shown in Fig. 3(b), where g_m represents the transconductance of M_1. $C_{\rm gs}$ represents the capacitance to ground at the gate of M_1. For frequencies well below $1/(2\pi C_{\rm gs} R_S)$, the effect of $C_{\rm gs}$ can be neglected.

A. Voltage Gain

Using the small-signal model in Fig. 3(b), the voltage gain of the amplifier can be derived as

$$A_v = \frac{v_{\rm out}}{v_{\rm in}} = -\left(g_m - \frac{1}{R_F}\right)(R_L \| R_F). \tag{1}$$

Feedback analysis [10] can be done by opening the loop and determining the open-loop transresistance gain (a) and the feedback factor (f), shown as follows:

$$a = -(R_S \,||\, R_F) g_m (R_L \,||\, R_F) \tag{2}$$

$$f = -\frac{1}{R_F}. \tag{3}$$

The voltage gain given by feedback analysis is

$$A_{v(\text{Feedback Theory})} = -g_m (R_L \,||\, R_F). \tag{4}$$

The discrepancy between (1) and (4) is because the feedforward path through R_F is ignored in the feedback analysis. This difference is negligible if $g_m \gg 1/R_F$.

B. Input Impedance Matching

Shunt–shunt feedback reduces the input impedance of the amplifier by a factor of $(1 + af)$. The input resistance $(R_{\rm in})$ of the amplifier is given by

$$R_{\rm in} = \frac{(R_S \,||\, R_F)}{1 + af} \approx \frac{R_S}{1 + af} \tag{5}$$

since $R_F \gg R_S$ (for reasons related to NF, which will explained later). For input impedance matching, $R_{\rm in}$ has to be equal to $R_S/2$. From (5), input matching is achieved with a loop gain (af) just below 1, which also ensures circuit stability. Using (3), the open-loop transresistance gain has to be approximately equal to the value of the feedback resistance for achieving input impedance matching

$$\text{Input Impedance Match Condition: } |a| \approx R_F. \tag{6}$$

C. NF

The contribution of each noise source to the total output noise is evaluated. The NF is then calculated by evaluating the ratio of the total output noise to the output noise due to R_S as follows:

$$\text{NF} \approx 1 + \frac{\gamma_{g_m}}{R_S g_m} + \frac{1}{R_S R_L g_m^2} + \frac{4R_S}{R_F}\left(\frac{-1}{1 + \dfrac{R_F + R_S}{(1 + g_m R_S) R_L}}\right)^2 \tag{7}$$

where γ_{g_m} is the noise excess factor of M_1 [11]. Equation (7) shows that having a large feedback resistance can lower the NF. From (6), a higher R_F requires a higher open-loop gain for input matching, usually leading to higher power consumption.

D. Linearity

Consider a nonlinear amplifier modeled by the power series [12]

$$v_{\text{out}} = a_1 v_{\text{in}} + a_2 v_{\text{in}}^2 + a_3 v_{\text{in}}^3. \tag{8}$$

Negative feedback improves its input IP3 by the following factor:

$$\frac{\text{IP3}|_{\text{CL}}}{\text{IP3}|_{\text{OL}}} = (1+a_1 f)^2 \sqrt{\frac{a_3}{a_3(1+a_1 f) - 2 f a_2^2}} \approx (1+a_1 f)^{3/2} \tag{9}$$

where $2fa_2^2 \ll a_3(1+a_1 f)$, $\text{IP3}|_{\text{CL}}$, and $\text{IP3}|_{\text{OL}}$ represent the close-loop and open-loop IP3, respectively. Equation (9) shows that linearity is not significantly improved by feedback at high frequencies if the open-loop gain of the amplifier rolls off [2].

III. Low-Power High-Linearity Resistive-Feedback LNAs

As discussed in Section II, a high open-loop gain is required to simultaneously achieve low NF and good input matching. The open-loop bandwidth also has to be high to achieve high linearity at high frequencies. These requirements usually lead to high power consumptions in resistive-feedback LNAs [2], [4]. We now present circuit techniques to improve linearity and lower power consumption in resistive-feedback LNAs.

A. Current-Reuse Resistive-Feedback LNA

The schematic of the restive feedback LNA with current-reuse transconductance boosting is shown in Fig. 4. Cascode transistors M_1 and M_3 form the input transconductance stage. A significant portion of the bias current in M_1 is diverted away from the load resistor R_L by transistor M_2. This reduces the dc voltage drop across R_L. Moreover, the transconductance generated by M_2 adds to that of M_1, increasing the effective g_m of the input stage. The current mirror formed by M_7 and M_8 controls the amount of current shunted away from R_L. The amplified signal is fed back to the input transconductance stage through feedback resistor R_F and the source follower formed by M_4, M_5, and R_1. The diode connected M_5 is used in the source follower to generate gate bias voltages for M_1, M_2, and M_3. The dc and ac feedback loops are thus combined, making it possible to remove the dc blocking capacitors required in earlier reports [4]. This reduces the total area requirement, and avoids loading of the source follower by the parasitic capacitance of the dc blocking capacitor to the substrate. The latter improves the LNA linearity. An additional source follower, formed by M_6 and R_2, is incorporated to improve reverse isolation and output driving capability. As discussed in Section II, the linearity at high frequencies can be improved by increasing open-loop bandwidth. This is achieved by device sizing and reducing layout parasitics as much as possible. The overall linearity of the LNA is

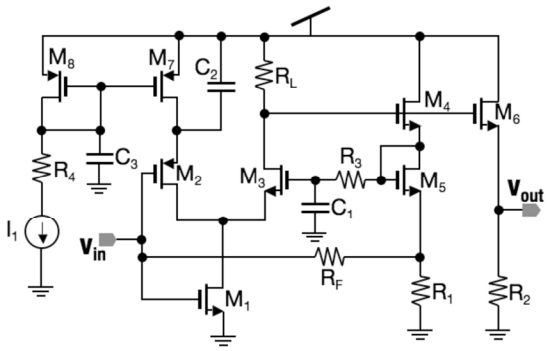


Fig. 4. Schematic of the current-reuse transconductance-boosting resistive-feedback LNA.

improved by making each block of the LNA more linear. Removing the dc block capacitors reduces the loading of the source follower, making it more linear, as explained earlier. Resistors R_1 and R_2 replace active current mirrors, which are nonlinear and have greater capacitance.

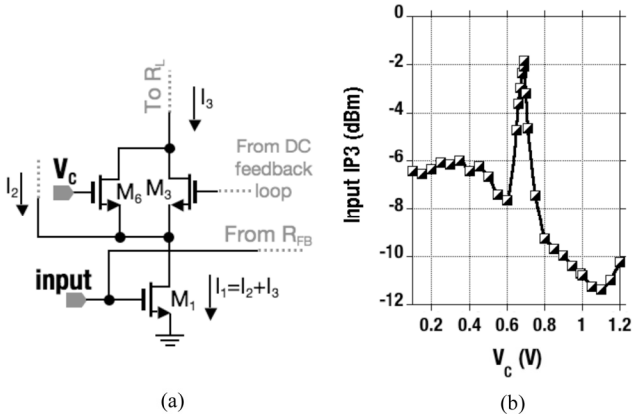
In all resistive-feedback LNAs with g_m-enhanced cascode structure, the width/length (W/L) ratio of the cascode transistor is kept low to achieve a higher bandwidth. The cascode device also has a lower bias current than the input transistor so as to reduce the voltage drop across the load resistor, as explained earlier. The lower W/L ratio and bias current makes the transconductance of the common-gate cascode transistor significantly lower than the common-source input transistor. The gain of the common-source stage is the ratio of these transconductances. The high gain in the common-source input stage preceding the cascode stage makes the g_m nonlinearity in the cascode stage limit the overall circuit linearity. This is because the IIP3 of the combined stages $(\text{IIP3}_{\text{CS-CG}})$ is related to the IIP3 of the common-source stage $(\text{IIP3}_{\text{CS}})$, its gain (G_{CS}), and the IIP3 of the common-gate stage $(\text{IIP3}_{\text{CG}})$ by the following equation:

$$\frac{1}{(\text{IIP3}_{\text{CS-CG}})^2} = \frac{1}{(\text{IIP3}_{\text{CS}})^2} + \left(\frac{G_{\text{CS}}}{\text{IIP3}_{\text{CG}}}\right)^2 \tag{10}$$

Hence, significant improvement in linearity can be obtained if the nonlinearity of the cascode stage is reduced by nonlinearity cancellation. This can be achieved by using derivative superposition [6], [13], as shown in Fig. 5(a). Here, the g_{m3} $(\delta^3 I_D/\delta V_{\text{GS}}^3)$ of the common-gate stage (M_3) is cancelled by the g_{m3} of the subthreshold transistor M_6. The measured input IP3 of the g_m-enhanced cascode LNA is plotted against the gate voltage of M_3 (V_C) in Fig. 5(b). Though significant improvements in IP3 have been demonstrated with derivative superposition at the cost of increased NF (≈0.6 dB) [9], such cancellation techniques may have potential issues in volume applications due to process and temperature variations.

B. Tuned Resistive-Feedback LNA with a Compact Low-Q Load Inductor

Linearity issues due to the high gain in the common-source stage preceding the common-gate cascode stage can be avoided by replacing the load resistance with a low-Q resonant load,



(a) (b)

Fig. 5. Nonlinearity cancellation in a g_m-enhanced cascode LNA with derivative superposition.

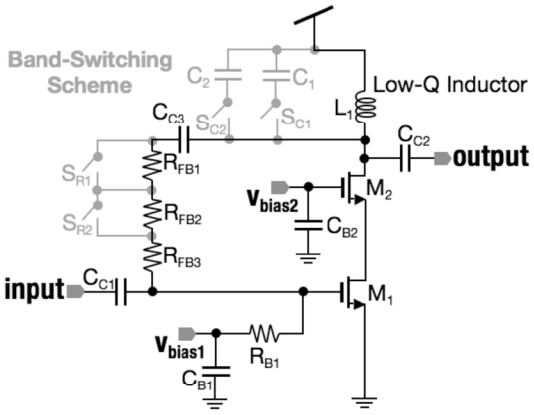


Fig. 6. Schematic of the tuned resistive-feedback LNA utilizing a compact low-Q load inductor.

using a compact on-chip inductor. The bias current of the cascode device can be made equal to that of the input device because the dc voltage drop across the resonant load is negligible. Since all the capacitance at the output node can be resonated out with the inductive load, it is not necessary to make the W/L ratio of the cascode device small.

The schematic of a tuned resistive-feedback LNA is shown in Fig. 6. Transistor M_1 is used as the common-source transconductance stage and M_2 is used as the cascode common-gate stage. A compact low-Q on-chip spiral inductor L_1 and the total capacitance at the output node form the resonant load. The parasitic capacitance of the dc block capacitors (C_{C2} and C_{C3}) to substrate and the drain capacitance of M_2 can, therefore, be resonated out along with the load capacitance at the output node. Resistors $R_{\rm FB1}$, $R_{\rm FB2}$, and $R_{\rm FB3}$ form the shunt-shunt feedback path. Capacitors C_{B1} and C_{B2} and resistor R_{B1} are used for biasing the cascode transistors.

Since this LNA utilizes only a single low-Q load inductor, it can be made extremely compact. Hence, low-cost multiband receivers can be implemented by using multiple tuned resistive-feedback LNAs each designed for a different frequency band, as shown in Fig. 2.

This circuit can be easily modified to operate across different frequency bands for the multiband receiver implementation

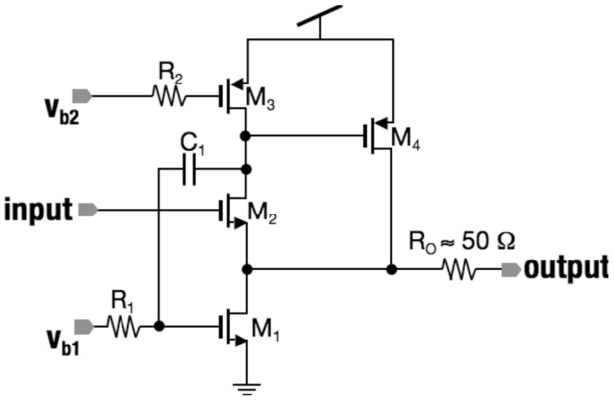


Fig. 7. Schematic of the modified super source follower output buffer.

shown in Fig. 1. The band-switching scheme enabling this implementation is shown in Fig. 6. The resonant frequency f_r can be shifted by using the capacitors C_1 and C_2 and the switches S_{C1} and S_{C2}. At resonance, the load impedance is purely resistive and given by

$$R_{L,fr} = 2\pi f_r L_{fr}\left(Q_{fr} + \frac{1}{Q_{fr}}\right). \tag{11}$$

Here, L_{fr} and Q_{fr} are the inductance and Q of the load inductor at the resonant frequency f_r. All the equations from Section II are still valid if R_L is replaced by $R_{L,\rm fr}$, and if g_m represents the effective transconductance of the cascode stage.

If the switches S_{C1} and S_{C2} are used to shift f_r, the value of $R_{L,\rm fr}$, given by (11), will not be the same in different frequency bands. Thus, the open-loop transimpedance gain (a) given by (2), will also vary from one frequency band to another. To satisfy the input matching condition in (6) across all the frequency bands, the feedback resistance $R_{\rm FB}$ will also have to be switched, as shown in Fig. 6, using switches S_{R1} and S_{R2}.

IV. Implementation of the Resistive-Feedback LNAs

Both of the resistive-feedback LNAs are implemented in a 90-nm seven-metal CMOS process. The only RF enhancement option used is the high-resistivity substrate under RF signal paths. All the capacitors were implemented as inter-digitated metal finger capacitors. Since the output impedance of the LNAs are not 50 Ω, a modified super source follower [4] was used to facilitate measurements. The schematic of this circuit is shown in Fig. 7.

The current-reuse transconductance-boosting resistive-feedback LNA draws 6.7 mA from the 1.8-V supply, thus consuming 12 mW of power. The chip micrograph of this LNA is shown in Fig. 8. The chip is pad limited and the actual LNA dimensions are 40 μm × 310 μm (Area: 0.012 mm^2). This implementation is a very low-cost alternative to the conventional inductor-based circuits for multiband multistandard radios.

The tuned resistive-feedback LNA has a power consumption of 9.2 mW, drawing 7.7 mA from the 1.2-V supply. Band switching is not implemented and the LNA is designed to operate in a single frequency band around 5.5 GHz. The chip micrograph of this circuit is shown in Fig. 9. The LNA dimensions are 155 μm × 145 μm (Area: 0.022 mm^2).

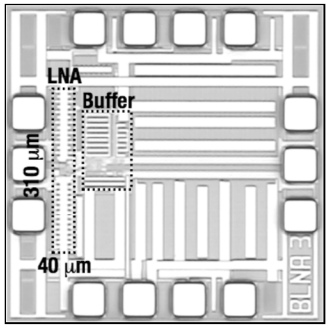


Fig. 8. Chip micrograph of the current-reuse transconductance-boosting resistive-feedback LNA.

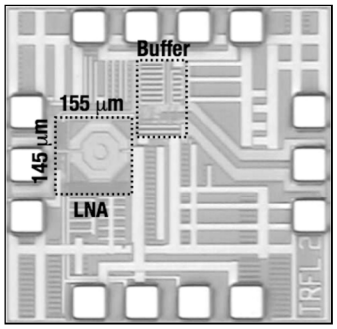


Fig. 9. Chip micrograph of the tuned resistive-feedback LNA.

V. Measurement Results

The measurements for both of the resistive-feedback LNAs were performed with on-wafer probing. Standalone output buffers were measured to deembed their effect on the measurement results of the LNAs.

A. Measurement Results of the Current-Reuse Resistive-Feedback LNA

The standalone output buffer used with the current-reuse transconductance boosting LNA has an insertion loss of 7 dB. Its input IP3 is 15.6 dBm at 5.8 GHz, 18 dBm at 5 GHz, and higher at lower frequencies. The buffer NF is 10 dB, including the noise added by a 50-Ω resistor added at the input for impedance matching.

The measured and simulated gain of the LNA and output buffer is shown in Fig. 10. Also plotted in Fig. 10 are the buffer loss and the deembedded LNA gain. The gain falls from 22 dB at low frequencies to 21 dB at 5 GHz. The 3-dB bandwidth is 7.5 GHz.

The measured and simulated input matching of the LNA are plotted in Fig. 11. It is −10 dB at 5 GHz and better at lower frequencies. The measured NF is plotted against frequency in Fig. 12. The NF is 2.6 dB at 5 GHz and varies between 2.3–2.9 dB from 500 MHz to 7 GHz. The 1.5-dB increase in gain in the measured results is due to slightly higher values for R_L and R_F. This increase in gain leads to improved input matching and noise performance compared to the simulated results.

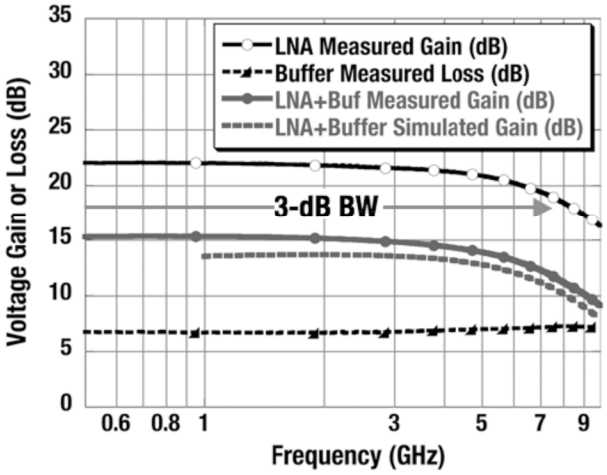


Fig. 10. Measured and simulated gain of the current-reuse transconductance-boosting resistive-feedback LNA and output buffer.

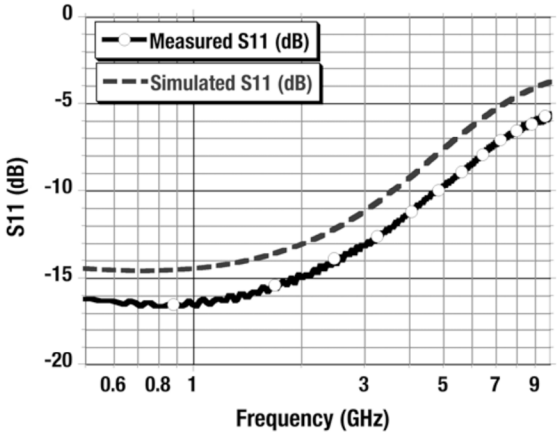


Fig. 11. Measured and simulated input matching of the resistive-feedback LNA.

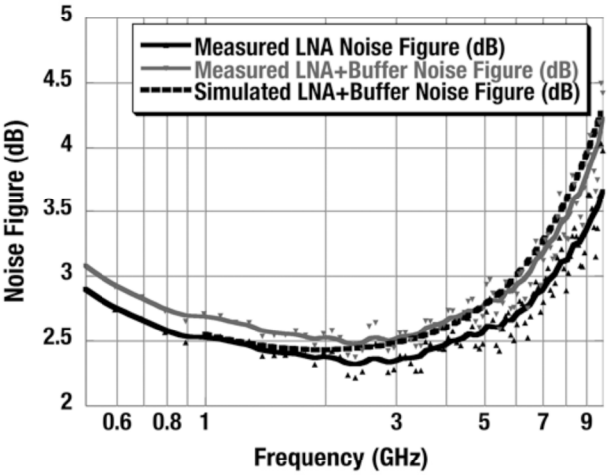


Fig. 12. Measured and simulated NF of the LNA and output buffer.

The input IP3 of the LNA is plotted in Fig. 13 after deembedding the effects of the output buffer. It varies from −2.3 dBm at 500 MHz to −8.8 dBm at 5.8 GHz. The degradation of linearity

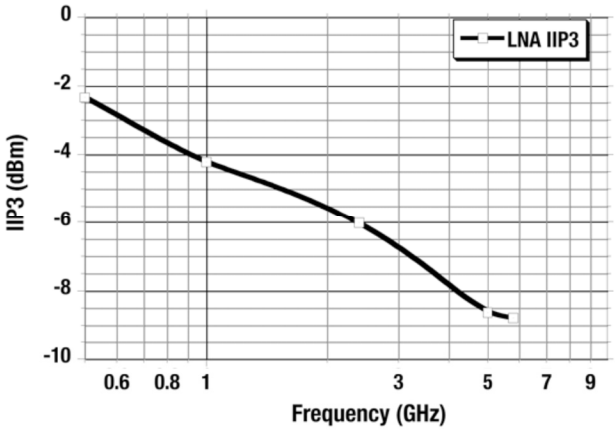


Fig. 13. Measured input IP3 of the current-reuse transconductance-boosting LNA.

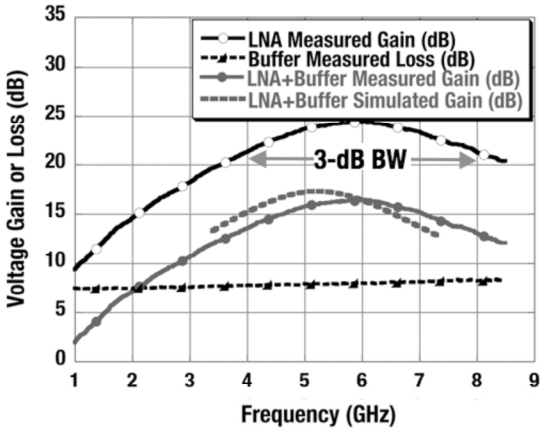


Fig. 14. Measured and simulated gain of the tuned resistive-feedback LNA and output buffer.

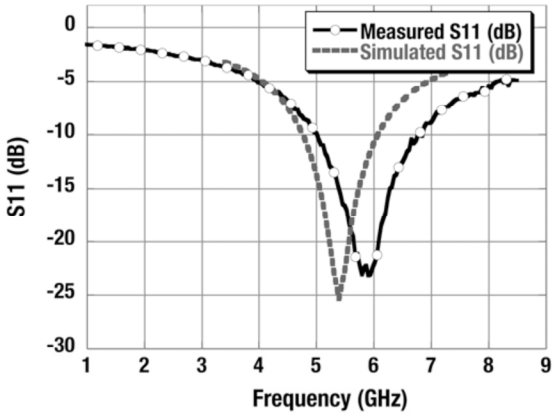


Fig. 15. Measured and simulated input matching of the tuned LNA.

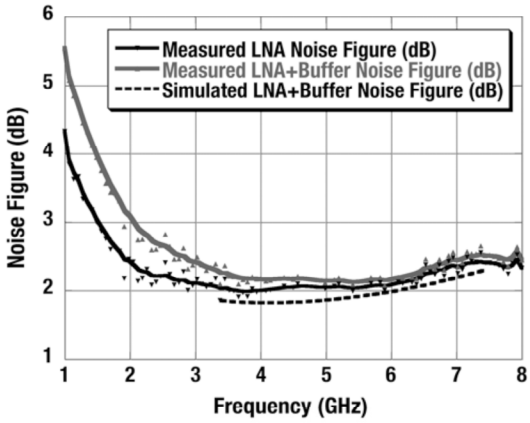


Fig. 16. Measured and simulated NF of the tuned resistive-feedback LNA and output buffer.

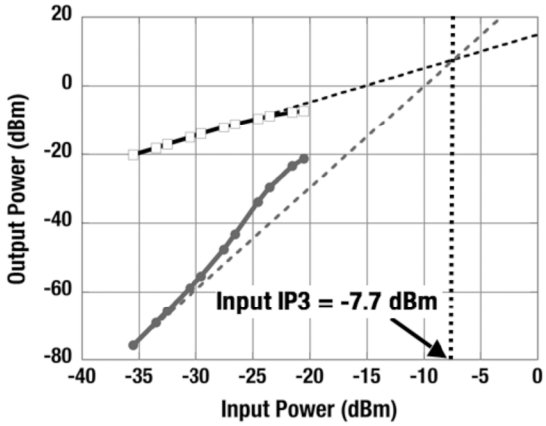


Fig. 17. Input IP3 of the tuned resistive-feedback LNA.

with frequency is due to the loop gain rolloff with frequency, as explained earlier.

B. Measurement Results of the Tuned Resistive-Feedback LNA

The standalone output buffer used with the tuned resistive-feedback LNA is similar to the one used with the current-reuse LNA and has a loss of 8 dB, and an NF of 9.8 dB (including the noise added by the 50-Ω resistor at the input). The output buffer has an input 1-dB compression point of 6.5 dBm and an input IP3 of 18 dBm at 5.5 GHz.

The measured and simulated gain of the LNA and output buffer is plotted in Fig. 14. The buffer loss and the deembedded gain of the LNA without the buffer are also plotted in Fig. 14. The LNA has a maximum gain of 24.4 dB and a 3-dB bandwidth of 3.94 GHz from 4.04 to 7.98 GHz. The measured input matching is plotted in Fig. 15. The input matching is better than −10 dB from 5 to 6.85 GHz.

Fig. 16 shows the measured and simulated NF of the tuned resistive-feedback LNA and the output buffer. The deembedded NF of the LNA without the output buffer is also plotted. The tuned resistive-feedback LNA has an NF of approximately 2 dB between 4–6 GHz.

The IP3 of the LNA and output buffer is plotted in Fig. 17. The input IP3 of the tuned resistive-feedback LNA and output buffer is −7.7 dBm at 5.5 GHz. The IIP3 of the LNA is found to be −2.6 dBm after deembedding the output buffer nonlinearity using the IIP3 of the standalone buffer (18 dBm) and the gain of the LNA (24.1 dB). Therefore, the output IP3 of the LNA is 21.5 dBm. The measured input 1-dB compression point of the LNA and buffer is −18 dBm at 5.5 GHz. The input 1-dB compression point of the LNA without the output buffer is found to be −7.2 dBm after deembedding.

TABLE I
WIDEBAND LNA PERFORMANCE COMPARISON

	[4]	[14]	[15]	[16]	**This Work** Current-Reuse LNA	Tuned LNA
Process	90-nm CMOS	90-nm CMOS	130-nm CMOS	130-nm CMOS	90-nm CMOS	90-nm CMOS
Freq. (GHz)	0.5 – 8.2	0 - 6	3.1 – 10.6	3 – 5	0.5 – 7	4 - 8
Power (mW)	42	9.8	9	45	12	9.2
Area (mm^2)	0.025	0.0017	~0.33	~0.5	0.012	0.022
Voltage Gain (dB)	25	17.4	15.1	25.8	22	24.4
Noise Figure (dB)	1.9 – 2.6	2.5 – 3.3	2.1 – 2.9	3.6 – 4.4	2.3 - 2.9	2 – 2.4
OIP3 (dBm)	8.8 (5.8 GIIz)	7 (5 GIIz)	6.6 - 10	12.8	11.5 (5.8 GHz)	21.5 (5.5 GHz)

The performance of the two resistive-feedback LNAs are tabulated and compared with others reported in Table I. The current-reuse transconductance-boosting resistive-feedback LNA provides comparable performance at lower power consumption while occupying very small die area. The tuned resistive-feedback LNA, though requiring slightly larger die area than the inductorless LNA, provides very high linearity, low noise, and high gain while dissipating low power. This LNA presents a much improved tradeoff between performance, power consumption, and cost, especially for multiband multistandard wireless receivers.

VI. CONCLUSION

Extremely compact LNA circuits based on resistive feedback are presented as a cost-effective alternative to multiple tuned LNAs requiring many high-Q inductors for multiband wireless applications. The relationships between the feedback resistance, NF, input matching, and open-loop gain are presented. The effect of the open-loop bandwidth on the close-loop linearity is also explained. A current-reuse transconductance boosting technique is used to reduce the power consumption in a resistive-feedback LNA to 12 mW. The inductorless LNA achieves a gain of 21 dB and an NF of 2.6 dB at 5 GHz. The rolloff of loop gain and the nonlinearities in the feedback loop are reduced to improve the output IP3 to 12.3 dBm at 5 GHz. The active die area of this LNA is only 0.012 mm^2. A tuned resistive-feedback LNA, using a compact resonant load, is also presented. It achieves a maximum gain of 24.4 dB and a 3-dB bandwidth of 3.94 GHz using a single low-Q on-chip inductor and consuming 9.2 mW of power. The LNA has an active die area of 0.022 mm^2. The NF of the tuned resistive-feedback LNA is approximately 2 dB between 4–6 GHz. At 5.5 GHz, the LNA has an output IP3 of 21.5 dBm. The combination of high linearity, low NF, high broadband gain, small die area, and low power consumption makes this LNA architecture a compelling choice for low-cost multistandard wireless front-ends.

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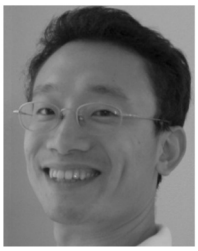

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