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# Optical Performance of Bare Image Sensor Die and Sensors Packaged at the Wafer Level and Protected by a Cover Glass

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## ABSTRACT

The yield of solid state camera modules declines with increasing imager resolution. The easiest means of compensating for this trend is to package the imager die before they are assembled into camera modules. The packaging is preferably accomplished at the wafer level. The package cover is a sheet of glass that forms part of the optical train of the solid state camera. This paper discusses the properties required of the glass and describes a computer model that was constructed to provide quantitative insight into its effect on the optical performance of image sensors. The study corroborates practical measurements that the cover glass has no significant effect on the low light sensitivity of a typical camera module. The cover glass does introduce some reflection losses and minor image aberrations, but these can be managed through the combination of attention to the design of the total optical path and making the cover glass as thin as possible.

Key words: Solid state imager, wafer-level package, cover glass, optical model

## INTRODUCTION

Solid state image sensors are manufactured in vast quantities. Typically each year more than 1 billion image sensors are produced, which primarily find application in portable electronics products such as camera 'phones, digital still cameras and increasingly, laptop computers. Predictions are that this market will continue growing for some years as cell phones with multiple cameras become the norm and automotive driver aids enter the video age, which could entail 10 or more cameras being installed on each vehicle.

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## PACKAGING OF SOLID STATE IMAGERS

In common with most other semiconductor devices, solid state image sensors require some form of enclosure in order to ensure their longevity. Traditionally for imagers this was achieved using chip-on-board (COB) assembly processes. In this scheme the imager is attached to a substrate and wire bonds form interconnections between bond pads on the die and lands on the substrate. The substrate forms the base of the enclosure. Over the die is then placed a lens turret, which houses the optical train of the camera. The lens turret is sealed to the substrate so the lower optical surface in combination with the sidewalls of the turret form an enclosure for the die. This is illustrated in Figure 1.

This structure has two principal drawbacks. The first is that the cost of assembly is incremental for each die packaged. A second limitation is that the imager die is totally unprotected until the final assembly operation when the lens turret is attached. It is therefore not surprising that more than 90% of defects in camera modules are related to contamination by particles[1]. The short-term solution is to invest in clean rooms and operator training. However, many solid state camera module manufacturers are already operating Class 10 environments, or better, so there is not a great deal of scope for further improvement at affordable cost.

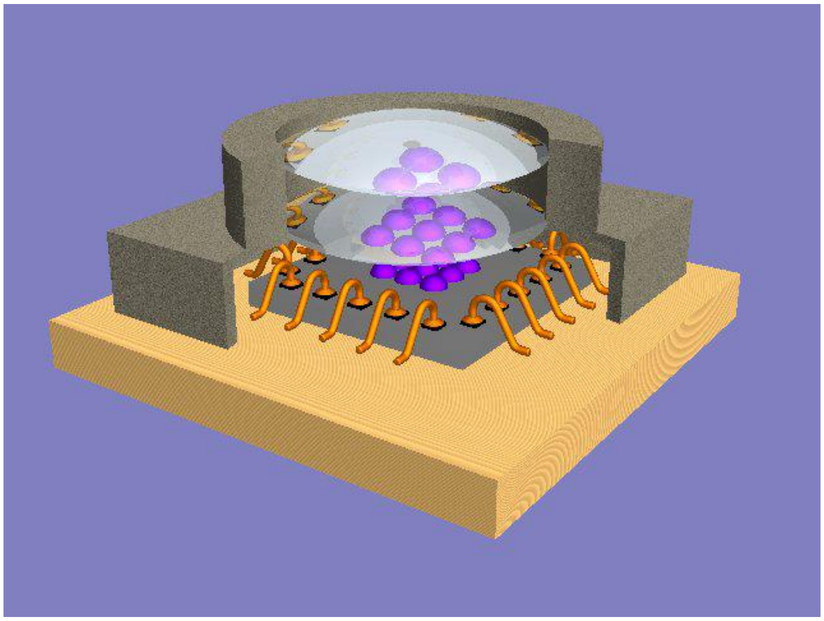

Fig 1 Camera module assembled using chip-on-board processes. The lens turret housing forms a seal over the exposed die. Drawing not to scale. Source: Tessera

## WAFER LEVEL PACKAGING

Wafer-level packaging (WLP) is an alternative approach where the die are packaged while still in wafer form and the wafer is then singulated to free individually packaged die. WLP has the advantage that the costs of packaging are shared among the good die on the wafer, greatly reducing packaging costs per die. A wafer-level cavity package for an image sensor is achieved simply by applying a picture frame of adhesive around each die, attaching a glass wafer and then sawing the assembly to yield individual die, each with a cover over the delicate image sensor area. This process is illustrated schematically in Figure 2.

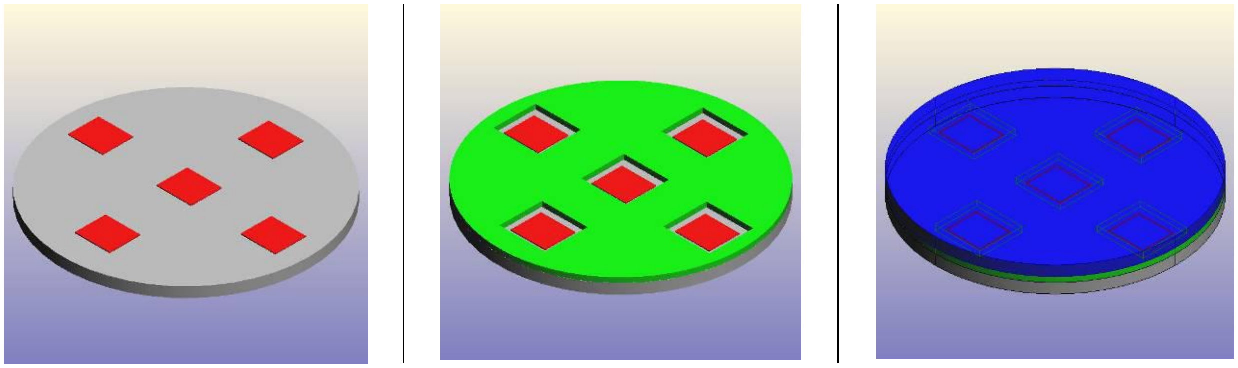

Fig 2 Formation of a wafer-level cavity package. Left - the device wafer containing five die. Middle - application of the seal material to form a picture frame around the perimeter of each die. Right – attachment of a lid material to seal the cavity over each die. Singulation frees the packaged die from the wafer, an example of which is shown in Figure 3. Source: Tessera

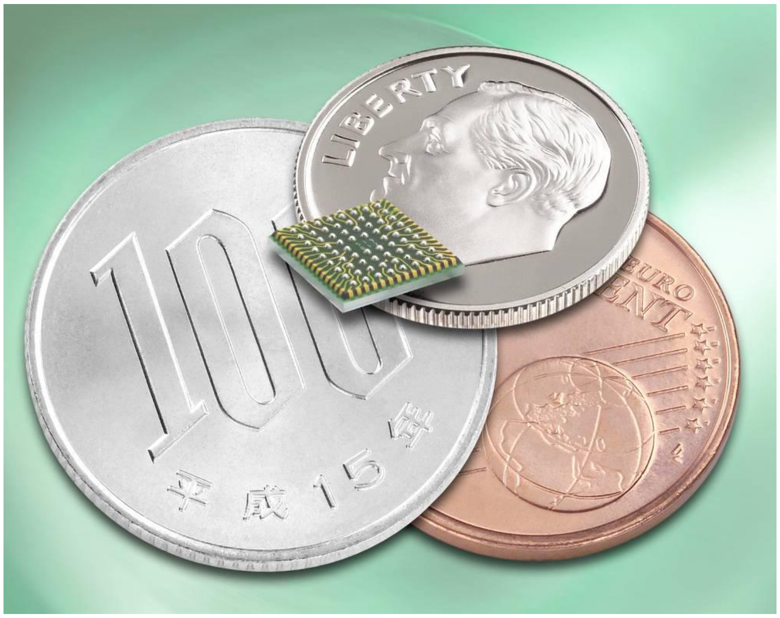

Fig 3 Image sensor packaged at the wafer level[2] and provided with a ball grid array interface to simplify and cheapen attachment to a printed circuit board. Source: Tessera

Wafer-level packaging provides two benefits that have great value for image sensors. Firstly, the dies are protected from the very first step of the assembly process so that yield loss from contamination is minimized. The second benefit is that it is possible to provide the packaged die with a ball grid array interface. This permits the camera module to be soldered to the main printed circuit board of the product at the same time as all the other semiconductor and passive components. It is predicted that by 2010 more than half of all image sensors will be protected by wafer-level packages.

## COVER GLASS

The cover glass used for the wafer-level package must fulfil several criteria. These are:

- Optically transparent. The glass must allow incident radiation of the visible spectrum (400-700nm) to reach the image sensor. The through thickness transparency of the cover glass needs to be as high as possible since any attenuation has a direct bearing on the low light sensitivity of the camera.

- Reasonably closely matched in thermal expansivity to silicon over the temperature range -40°C to +260°C. To benefit from the economics of wafer-level processing, the cover glass is bonded to the silicon die while both are in wafer form. This means that the expansivity of the glass must be closely matched to silicon above room temperature since joining of the glass to silicon entails an elevated temperature process.

- Free of active species that could potentially leach out of the glass and degrade the delicate image sensor. In this regard, the elements normally found in glass that are particularly detrimental are the alkalis. Over time these can leach out of the glass and poison the semiconductor junctions.

- Be available in wafer form, to match the diameter and features of SEMI standard silicon wafers (e.g. flats, notches). Similarly, the glass wafers must be manufacturable to exacting specifications in terms of defects, since most types of blemish in the glass will be visible as artefacts in the image captured by the sensor. A typical scratch/dig specification for image sensor cover glass is 50/05. In addition, the geometric properties such as thickness and total thickness variation (TTV) need to be well controlled.

- Cost attractiveness. The packaging market is driven by challenging price roadmaps, thus high costs for materials and components are not acceptable. A major cost driver in the production of glass wafers is the polishing step. Choosing a hot forming method for the raw glass production that offers the desired thickness directly from the tank saves the expensive polishing step.

## COVER GLASS SELECTION

There are very few glass types that meet the requirements set out above. The one selected for this application has the designation SCHOTT AF 45[3]. Its properties and performance are proven to meet the requirements for 200mm manufacturing lines in mass production for several years. In order to provide a suitable glass type for 300mm production lines as well as single glass WLP solutions, the glass type with the designation SCHOTT AF 32[4] has been developed.

AF 45 as well as AF 32 are melted using selected pure raw materials. This ensures the high luminous transmittance in the visible wavelength, as can be seen from Figure 4.

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