Exhibit C-12: "Splash 2: FPGAs in a Custom Computing Machine," D.A. Buell et al., 1996 ("Buell")

A book chapter entitled, "Splash 2: FPGAs in a custom Computing Machine," by D.A. Buell, J. M. Arnold, and W. J. Kleinfelder, ("Buell") was published in 1996, and is therefore prior art to U.S. Patent No. 7,225,324 ("'324 Patent") at least under 35 U.S.C. §§ 102(a) and (b).

The citations presented herein are exemplary and not exclusive; each prior art reference as a whole discloses each and every limitation of the claims. A citation to a figure or figure reference numeral incorporates by reference the discussion and/or explication of such figure or feature/component referenced by the reference numeral. Further, the mapping in this chart is based on Amazon's present understanding of Plaintiffs' interpretation of the asserted claims of the patent-in-suit as reflected in Plaintiffs' infringement contentions. Nothing in the chart should be regarded as necessarily reflecting how the prior art references would apply to claim elements of the asserted patent under a proper interpretation of the claims. Disclosures cited for dependent claims incorporate by reference the disclosure included herein for the corresponding independent claim.

Asserted Claim of '324 Patent	**Exemplary Disclosure of Buell**
[1A] A **method** for **data processing**	Buell at 97: "With the onset of the Human Genome Initiative [3] and constant advances in genetic sequencing technology, ***genetic sequence data*** are being generated at an ever increasing rate. As a result, biologists are faced with an influx of new sequences that they would like to classify and study by comparing them to ***existing databases***. The analysis of a newly generated sequence typically involves ***searching the databases*** for similar sequences. ***With the enormous size of the databases, fast methods are needed for comparing sequences*** **[11].** In this chapter, we describe ***two systolic array architectures for sequence comparison...***" Buell at 100: "The locality of reference shown in Figure 8.3 can be exploited to produce systolic algorithms in which communication is limited to adjacent ***processors***…. The systolic architecture and ***data flow*** shown in Figure 8.5 were used in the design of P-NAC of Lipton and Lopresti [12], a custom VLSI chip for DNA sequence comparison. Each ***processing*** element (PE) computes the distances along a particular diagonal of the distance matrix."

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Asserted Claim of '324 Patent	Exemplary Disclosure of Buell
	Buell at Figure 8.1:

Asserted Claim of '324 Patent	Exemplary Disclosure of Buell

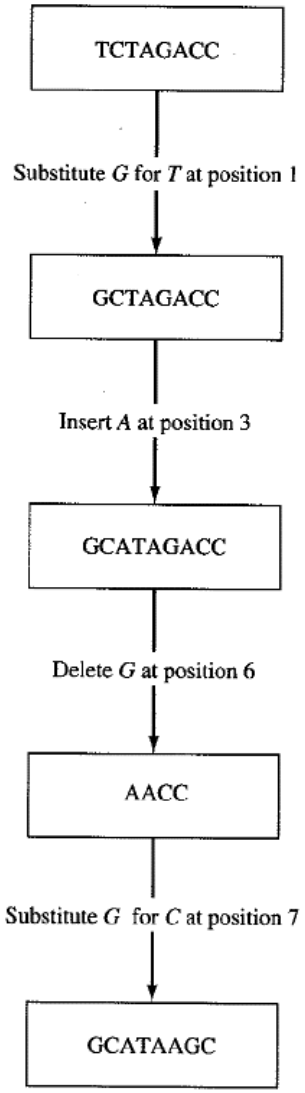

FIGURE 8.1 Listing of Operations to Transform *TCTAGACC* into *GCATAAGC*. Character matches are assumed to have a cost of 0 and are not shown. Assigning a cost of 2 for a substitution, 1 for deletion, and 1 for insertion, the cost of the transformation is 6.

Buell at Figure 8.9 [emphasis added]:

Asserted Claim of '324 Patent	Exemplary Disclosure of Buell

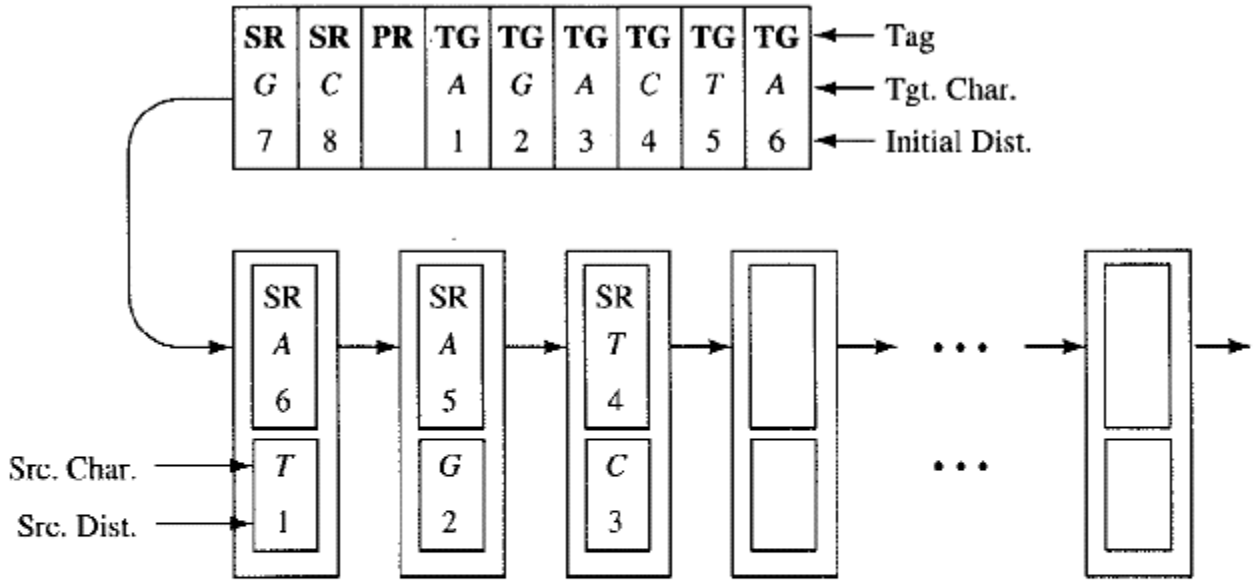

FIGURE 8.9 Data Flow through the Unidirectional Systolic Array. The source sequence is first loaded into the array. The target sequences are then streamed through the array. The tag acts as a simple instruction telling each PE how to process the incoming data. The SR tag instructs an empty PE to load the source character and distance from the input stream. The PR tag marks the end of the source stream. The TG tag signals a target character. Multiple source and target sequences can be carried on the input stream for uninterrupted pipelined processing.

Buell showing a method for processing data at Figure 8.12:

Asserted Claim of '324 Patent	Exemplary Disclosure of Buell

```
loop
  if (TAGin = SR) then
    if (SRCch = Ø) then
      SRCch ← CHRin
      CHRout ← Ø
      DSTout ← PDSTin
    else
      CHRout ← CHRin
    endif
    PDSTout ← PDSTin
  else-if (TAGin = PR) then
    if (SRCch = Ø) then
      DSTout ← PDSTin
    endif
    PDSTout ← DSTin
    CHRout ← CHRin
  else-if (TAGin = TG) then
    if (SRCch ≠ Ø) and (CHRin ≠ Ø) then
      DSTout ← min { PDSTout+ψ(SRCch,CHRin),
                     DSTin+ψ(SRCch,Ø),
                     DSTout+ψ(Ø,CHRin) }
    else-if (SRCch = Ø) then
      DSTout ← DSTin
    endif
    PDSTout ← DSTin
    CHRout ← CHRin
  endif
  TAGout ← TAGin
endloop
```

FIGURE 8.12 Code executed by each PE in the unidirectional array

Buell showing a method for processing data at Figure 8.7:

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