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Details the complete Splash 2 project—the hardware and software systems, their architecture and implementation, and the design process by which the architecture evolved from an earlier version machine. In addition to the description of the machine, this book explains why Splash 2 was engineered. It illustrates several applications in detail, allowing you to gain an understanding of the capabilities and the limitations of this kind of computing device.

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# Pipelined H-Trees for High-Speed Clocking of Large Integrated Systems in Presence of Process Variations

Mohamed Nekili, Guy Bois, and Yvon Savaria, *Member, IEEE*



**Abstract**—This paper addresses the problem of clocking large high-speed digital systems, as well as deterministic skew modeling, a related problem. A conventional method for clocking a large digital system is to use a set of metallic lines organized as a tree. This method is limited by the bandwidth of the clock network. Another limitation of existing solutions is that available skew models do not directly take into account process variations. In order to provide a reliable skew model, and to avoid the frequency limitation, we propose a novel approach that distributes the clock with an H-tree, whose branches are composed of minimum-sized inverters rather than metal. With such a structure, we obtain the highest clocking rate achievable with a given technology. Indeed, clock rates around 1 GHz are possible with a 1.2  $\mu\text{m}$  CMOS technology. From the skew modeling standpoint, we derive an analytic expression of the skew between two leaves of the H-tree, which we consider to be the difference in root-to-leaf delay pairs. The skew upper bound obtained has an order of complexity which, with respect to the H-tree size  $D$ , is the same as the one that may be derived from the Fisher and Kung model for both side-to-side and neighbor-to-neighbor communications, i.e., a  $\Omega(D^2)$ , whereas, the Steiglitz and Kugelmass probabilistic model predicts  $\Theta(D \times \sqrt{\log D})$ . In an H-tree implemented with metallic lines, the leaf-to-leaf skew is obviously bounded by the delay between the root and the leaves. However, with the logic based H-tree proposed in this paper, we arrive at a nonobvious result, which states that the leaf-to-leaf skew grows faster than the root-to-leaf delay in presence of a uniform transistor time constant gradient. This paper also proposes generalizations of the skew model to 1) the case of chips in a wafer subject to a smooth, but nonuniform gradient and 2) the case of H-tree configurations mixing logic and interconnections; in this respect, this paper covers the H-tree configurations based on the combination of logic and interconnections.

**Index Terms**—H-tree, high-speed clocking, pipelining, process variations, skew.

## I. INTRODUCTION

THE evolution of VLSI chips toward larger die sizes and faster clock speeds makes clock design an increasingly important issue. A striking example of what can be accomplished with aggressive clock design is the DEC alpha chip [1],

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designed to operate at more than 200 MHz. At such speeds, clock skew becomes a very significant problem. Available literature dealing with skew [2]–[8], [10], [11] approaches the problem both from deterministic and probabilistic standpoints.

In the deterministic approaches, Friedmann and Powell [6] emphasize the use of a hierarchical clock distribution, while others [2], [3], [8], [11] suggest the length equalization of the different paths followed by the clock throughout the circuit. Shoji [5] suggests an approach that guarantees a symmetry between paths that contribute to propagate "0" and "1." This symmetry ensures proper operation despite some types of process variations [5]. Except for the work of Fisher and Kung [4], which provides bounds on skew, the other authors do not deal with the analytic modeling of system skew.

In the probabilistic approaches, Kugelmass and Steiglitz [7] consider the delay of a clock signal along a given path as a sum of delays along path segments, each of these segments behaving according to a probabilistic law. Then, by assuming independence between these delays, the total delay, as well as the skew, can then be described by a normal law. By assuming independence and the linearity of delay with line length, their approach becomes an oversimplification of the reality. Other authors [10] consider the skew as a dispersion in the physical parameters of a circuit (e.g., geometrical dimensions) and in the process (e.g., sensitivity to temperature).

The work that is most directly related to that presented in this paper is the work of Fisher and Kung [4]. These authors have developed two deterministic skew models (the difference model and the summation model), from which they determined bounds on skew. However, these models do not directly refer to a process variation model. The difference model tends to be unrealistically optimistic, whereas, under the summation model, Fisher and Kung reached a pessimistic result which states that, from a skew standpoint, synchronous systems are not feasible with large two-dimensional arrays.

In order to avoid the frequency limitation when using metallic lines, we propose a logic-based H-tree structure that provides the highest clocking rate achievable with a given technology in Section II. To provide a reliable skew model, Section III suggests a model based on delay differences combined with a model of electrical variations in the process parameters. Under this model, we derive an analytic expression of the skew between any leaf pair, which we consider to be the difference in root-to-leaf delay pairs. Even though the model of electrical variations described in this paper assumes



# VLSI Array Algorithms and Architectures for RSA Modular Multiplication

Yong-Jin Jeong, *Member, IEEE*, and Wayne P. Burleson, *Member, IEEE*

**Abstract**—We present two novel iterative algorithms and their array structures for integer modular multiplication. The algorithms are designed for Rivest–Shamir–Adelman (RSA) cryptography and are based on the familiar iterative *Horner's rule*, but use precalculated complements of the modulus. The problem of deciding which multiples of the modulus to subtract in intermediate iteration stages has been simplified using simple look-up of precalculated complement numbers, thus allowing a finer-grain pipeline. Both algorithms use a carry save adder scheme with modulo reduction performed on each intermediate partial product which results in an output in carry-save format. Regularity and local connections make both algorithms suitable for high-performance array implementation in FPGA's or deep submicron VLSI. The processing nodes consist of just one or two full adders and a simple multiplexor. The stored complement numbers need to be precalculated only when the modulus is changed, thus not affecting the performance of the main computation. In both cases, there exists a bit-level systolic schedule, which means the array can be fully pipelined for high performance and can also easily be mapped to linear arrays for various space/time tradeoffs.

**Index Terms**—Cryptography, modular multiplication, RSA, systolic arrays, VLSI.

## I. INTRODUCTION

CRYPTOGRAPHY systems have been growing in importance recently as a method for improving data security. Public key cryptography (PKC) systems are generally preferred to traditional secret key cryptography systems like the data encryption standard due to the safety of key distribution [3]. The Rivest–Shamir–Adelman (RSA) [10] system is one of the most widely used public key cryptography systems, and its core arithmetic is modular multiplication over a positive integer. Modular multiplication is also a major computation of residue number systems [13] as well as other cryptography systems (e.g., international data encryption algorithm [8], [16], Diffie–Hellman key exchange [3]). In this paper, we develop an array modular multiplier with applications to, but not restricted to, RSA systems.

In RSA, the modulus is a product of two large prime numbers, usually more than 500 bits, and should be changeable for security reasons. But, since the modulus (or key) is not changed very often, we can use precomputation and look-up in our array modular multipliers. We are not aware of anyone

who has utilized this special property of *multirate input data* in the RSA algorithm, that is, the *input message* changes rapidly while the *key* remains unchanged for a long period. In practice, the key is updated infrequently, for example, a few months, weeks, or days, depending on the security requirements. In order to satisfy the ever growing security requirements of high-speed communications, such as personal communication services and wireless local area networks, a *dedicated* VLSI hardware solution is needed because of 1) high throughput requirements, 2) low-power requirements, 3) a high-volume market, 4) the computation is poorly suited to microprocessors or DSP's, and 5) the problem size is expected to continue to grow rather than saturate.

Modular multiplication is generally considered a complicated arithmetic operation because of the inherent multiplication and division operations. There are two main approaches to computing modular multiplication: 1) perform the modulo operation *after* multiplication or 2) *during* multiplication. The modulo operation is accomplished by integer division in which only the remainder is needed for further computation. The first approach requires a  $n \times n$  bit multiplier with a  $2n$ -bit register followed by a  $2n \times n$  bit divider. In the second approach, the modulo operation occurs in each iteration step of integer multiplication. Therefore the first approach requires more hardware while the second requires more addition/subtraction computations due to  $O(n)$  modulo reduction steps. In both cases, most previous research has focused on the fast calculation of a long carry chain. Redundant number systems and a higher radix carry-save form are some of the different number representations that have been used for this purpose [12], [14]. A carry prediction technique has also been used for fast calculation of modular multiplication [1].

Since PKC was introduced, many algorithms and hardware structures have been proposed for modular multiplication, and [4] contains a good review on this topic. Several array structures suited for VLSI implementation have been discussed in [4], [5], [14], and [15]. In [14], Vandemeulebroeck *et al.*, use a *modulo after multiplication* approach using a *signed digit* number representation. It consists of two arrays: one for multiplication and the other for integer division. In [5], Koc and Hung apply Blakley's algorithm [2] and use a sign-estimation method by looking at the five most significant bits in each iteration stage. Although they derive a bit-level systolic array structure, the latency and clock cycle are relatively long due to the control node which estimates the sign of the intermediate result in each stage. In [4] and [15], Eldridge and Walter use Montgomery's algorithm [9] which only works if

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the modulus is relatively prime to the radix, although this is always the case in RSA.

In this paper, we develop two new VLSI array architectures for modular multiplication. The idea is similar to Montgomery's algorithm in which he tries to make each partial product a multiple of the radix to simplify the multiplication by the radix (just by shifting) by only looking at the least significant bits (LSB), thus requiring a post-processing step to get the final answer. In our algorithms, we look at the most significant bits (MSB) to remove higher bit positions while keeping the correct answer in each partial product, keeping it within a certain range. Due to the simple translation of a modulo operation into an addition of a precalculated complement of the modulus, the *modulo during multiplication* approach is used with a carry-save adder structure. Instead we pay for multiplexors to choose the precalculated integer depending on the control which is generated in the leftmost node in each stage. Compared to previous works, we can obtain a higher clock frequency mainly due to the simplified modulo reduction operation. In Section II, we will explain our basic concept for the modulo reduction operation and then describe the two iterative algorithms. Array structures corresponding to these algorithms, analysis, and some modifications are also discussed in this section. Conclusions and discussion are in Section III.

## II. MODULAR MULTIPLICATION ALGORITHM

In a modular multiplication, the  $n$ -bit modulus  $C$  is represented by a binary number system as  $C = \sum_{i=0}^{n-1} c_i 2^i$  where  $c_i \in GF(2)$ . Obviously  $C$  is less than  $2^n$ . We introduce  $K$ , which is called the *complement* of the modulus  $C$ , such that

$$K \equiv 2^n \pmod{C}. \quad (1)$$

In other words, any carry of weight  $2^n$  can be replaced by an addition of  $K$ , which means that the end-around carry implies an extra addition. If  $K$  does not change frequently, we can precalculate multiples of  $K$  and store them in registers for use in the modulo reduction operation. Note that if the MSB of  $C$  is 1,  $K$  is equivalent to  $-C$  in a 2's complement number system.

Now we describe the general modular multiplication algorithm using the *modulo during multiplication* approach. Given any two  $n$ -bit integers,  $A$  and  $B$ , and the  $n$ -bit modulus  $C$ , where  $(C > A, B)$ , the modular multiplication can be described by an iterative procedure using *Horner's rule*

$$\begin{aligned} AB \pmod{C} &= A \cdot \sum_{i=0}^{n-1} b_i 2^i \pmod{C} \\ &= ((\dots (b_{n-1}A)2 + b_{n-2}A)2 \\ &\quad + \dots + b_1A)2 + b_0A \pmod{C}. \end{aligned} \quad (2)$$

We can describe (2) in a recursive form as follows:

$$\begin{aligned} P_0 &= 0 \\ P_i &= 2P_{i-1} + b_{n-1}A \pmod{C} \end{aligned} \quad (3)$$

and  $P_n$  is the final result. Using (1) and (3), we will derive two different bit-level array structures.

### A. Using the CSA Scheme

The carry save addition (CSA) scheme is the most commonly used technique in integer multiplication to reduce the carry propagation penalty [6]. In the CSA scheme, a partial sum and a carry sequence are generated in the intermediate stages and the carry propagation occurs only at the last stage. The basic element of the CSA scheme is a full adder (FA) which is often called a (3, 2) counter. It accepts three inputs, referred to here as  $s_i$ ,  $c_i$ ,  $x_i$  with (associated weight  $2^i$ ), and produces two outputs, carry  $c_o$  (with weight  $2^{i+1}$ ) and sum  $s_o$  (with weight  $2^i$ ). The arithmetic operation of the (3, 2) counter can thus be described by the familiar expression:

$$2c_o + s_o = s_i + c_i + x_i \quad (4)$$

where "+" means an algebraic (not Boolean) addition.

Using the CSA scheme, we have a carry of weight  $2^n$  in the leftmost node in each stage. As shown in (1), this carry can be replaced by the addition of the integer  $K$  for a modulo operation. The basic idea in our approach is that we handle the carries of weight  $2^n$  and higher by using  $K$  wherever they appear, unless the basic CSA structure is broken. From (3), let us denote a partial product  $P_i$  as

$$P_i \equiv 2C_i + S_i \quad (0 \leq i \leq n) \quad (5)$$

then, the valid range of  $P_i$  is

$$0 \leq P_i \leq 3 \cdot 2^n - 3. \quad (6)$$

This means we allow  $P_i$  to be greater than modulus  $C$  at intermediate stages.

Before we begin the derivation of a recursive equation for modulo multiplication, we define a new variable  $K_h$  to handle multiple end-around carries

$$K_h \stackrel{\text{def}}{=} h \cdot K \pmod{C} \quad (7)$$

where  $h$  is a positive integer (1, 2, ...) and  $K$  is defined in (1). Then

$$2^{n+j} \pmod{C} = 2^j \cdot K \pmod{C}.$$

Carries can also appear in a combined mode. As an example, suppose we have two carries of weight  $2^{n+1}$  and one carry of weight  $2^n$ , then  $(2^{n+1} + 2^{n+1} + 2^n) \pmod{C} = 5 \cdot 2^n \pmod{C} = 5 \cdot K \pmod{C} = K_5$ .

Equation (3) contains two modulo reduction steps and can be written by introducing a new partial product term  $T_i$ , as

$$\begin{aligned} \text{i)} \quad T_i &= 2P_{i-1} \pmod{C} \\ \text{ii)} \quad P_i &= (T_i + b_{n-1}A) \pmod{C}. \end{aligned} \quad (8)$$

But step ii) cannot be implemented by the CSA scheme because it has four operands to be added. (Note that the modulo operation implies at least one extra addition of  $K$ .) This can be solved by dividing step ii) into two steps as

$$\begin{aligned} \text{i)} \quad T_i &= 2P_{i-1} \pmod{C} \\ \text{ii-a)} \quad T_i^* &= T_i + b_{n-1}A \\ \text{ii-b)} \quad P_i &= T_i^* \pmod{C}. \end{aligned} \quad (9)$$



In step i),  $2P_{i-1}$  implies one  $2^{n+1}$  term ( $c_{i-1}^{n-1}$ ) and two  $2^n$  terms ( $s_{i-1}^{n-1}$  and  $c_{i-1}^{n-2}$ ), which can generate a maximum of  $4 \cdot 2^n$ .<sup>1</sup> In step ii-a), we do not perform the modulo operation because there are already three operands: two from  $T_i$  in carry save form, and one for  $A$  depending on  $b_{n-i}$ . Instead we want to pass through the MSB carry of  $T_i$  to step ii-b). So, in step ii-b), we will have at most  $2 \cdot 2^n$  (one passed from  $T_i$  and another newly generated in  $T_i^*$ ) as end-around carries. In both the steps i) and ii-b), only one additional operand is allowed. That is why we precalculate the  $K_h$ 's instead of adding  $K$  multiple times.

To explain the algorithm more formally, we define  $\sigma(P_i)$  as follows:

$$\sigma(P_i) \stackrel{\text{def}}{=} P_i - h \cdot 2^n + K_h$$

where

$$h = f(x_1, x_2, x_3, \dots, x_r) \quad (10)$$

and the function  $f(\cdot)$  calculates the total magnitude of end-around carries, and  $x_1, x_2, \dots, x_r$  are bit variables (always carries and sums of the MSB position) which contribute to the translation of (1). Thus

$$f(x_1, x_2, \dots, x_r) = \sum_{k=1}^r \alpha_k x_k \quad (11)$$

where  $\alpha_k = 1$  if  $x_k$  has weight  $2^n$ ,  $\alpha_k = 2$  if the weight is  $2^{n+1}$ ,  $\alpha_k = 4$  if the weight is  $2^{n+2}$ , and so on. In other words,  $\sigma(P_i)$  replaces  $h \cdot 2^n$  with  $K_h$  which is precalculated.

Using (10), we can rewrite algorithm (9) as follows:

$$\begin{aligned} \text{i)} \quad & T_i = \sigma(2P_{i-1}) \\ \text{ii-a)} \quad & T_i^* = T_i + b_{n-i} A \\ \text{ii-b)} \quad & P_i = \sigma(T_i^*) \end{aligned} \quad (12)$$

As we can see in Fig. 1, the function  $f(\cdot)$  of the above algorithm is

$$\begin{aligned} \text{for step i)} \quad & f(\cdot) = 2c_{i-1}^{n-1} + s_{i-1}^{n-1} + c_{i-1}^{n-2} \\ \text{for step ii-b)} \quad & f(\cdot) = \gamma_i^{n-1} + \gamma_i^{*n-1} \end{aligned}$$

where  $\gamma_i^{n-1}, \gamma_i^{*n-1}$  are the MSB carries of  $T_i$  and  $T_i^*$ , respectively (both have the weight  $2^n$ ).

Now we will informally verify that the algorithm (12) satisfies the valid range of (6) for all  $P_i$ 's ( $i = 0, 1, \dots, n$ ). Obviously  $0 \leq P_0 < 3 \cdot 2^n - 3$ . Suppose  $0 \leq P_{i-1} < 3 \cdot 2^n - 3$ , then

$$\begin{aligned} 0 &\leq 2P_{i-1} < 6 \cdot 2^n - 6 \\ 0 &\leq \sigma(2P_{i-1}) < 6 \cdot 2^n - 6 - 4 \cdot 2^n + 2^n = 3 \cdot 2^n - 6 \\ 0 &\leq T_i^* < 4 \cdot 2^n - 6 \end{aligned}$$

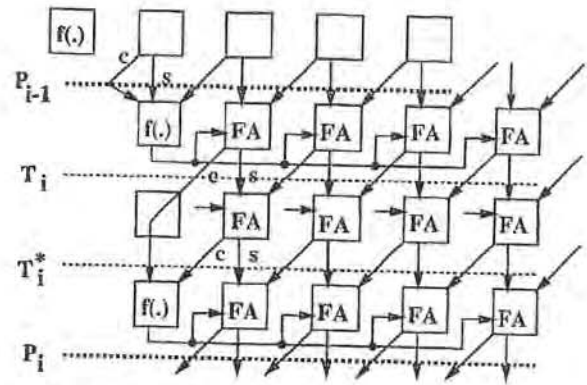


Fig. 1. An iteration stage of modular multiplication using the CSA scheme.

$$\begin{aligned} 0 &\leq \sigma(T_i^*) < 4 \cdot 2^n - 6 - 2 \cdot 2^n + 2^n < 3 \cdot 2^n - 3 \end{aligned}$$

which assures  $0 \leq P_i < 3 \cdot 2^n - 3$ . Therefore the algorithm (12) produces a final output  $P_n$  which is less than  $3 \cdot 2^n - 3$ . It can be directly fed into the next multiplication stage for further iteration if necessary (e.g., exponentiation).

Fig. 2(a) shows a single stage of the dependence graph (DG) which can be directly implemented as a parallel array multiplier. Fig. 2(b) describes the node functions. The nodes  $X_1, X_3$  are control nodes which calculate the control value  $h$  of (10), and hence need simple encoders. The node  $X_2$  is just a wire. Node type A is a FA with a 4-1 multiplexor and an AND gate. Node type B is just a FA with an AND gate and node type C is a FA with a 2-1 multiplexor and an AND gate. Note that node type B does not need a multiplexor and type C needs only  $K_1$  and  $K_2$  because the max value of  $h$  is two in node  $X_3$ . An AND gate is needed in type A and C to accept  $K_0 = 0$  when the control value  $h$  is zero. There exists a systolic schedule which is not linear due to its skewed connection between the stages. Table I shows an example for our new bit-level modular multiplication algorithm using  $n = 12$ , with  $A = 010001000100 (= 1092)$ ,  $B = 010011001101 (= 1229)$ , and  $C = 100000101001 (= 2089)$ . The  $K_h$ 's are precalculated as  $K_1 = K_0 = 011111010111 (= 2007)$ ,  $K_2 = 011110000101 (= 1925)$ ,  $K_3 = 011100110011 (= 1843)$ ,  $K_4 = 011011100001 (= 1761)$ . The final output is

$$\begin{aligned} P_n &= 2(001100010101) + (110111001010) \\ &= 100111110100 \\ & (= 5108) \end{aligned}$$

which equals 930 after modulo reduction to 2089.

By merging two nodes into one in each row as has been done in [5], one can modify the DG in Fig. 2 to derive a simpler DG. This is shown in Fig. 3. Node types AA, BB, CC are newly merged nodes which have two A, B, C type nodes, respectively. It now allows a linear systolic schedule and shows a better overview of the hardware array implementation. If the wordlength  $n$  is an even number, then all nodes except the control nodes will be merged nodes. Here we have the original nodes A, B, C in the LSB place because  $n$  is odd. From

<sup>1</sup>Subscript is for an iteration stage and superscript is for denoting bit positions, that is,  $S_i = \sum_{j=0}^{n-1} s_i^j \cdot 2^j$ . Also note that lower case letters are used for bit-level variables while upper case is for word-level variables.



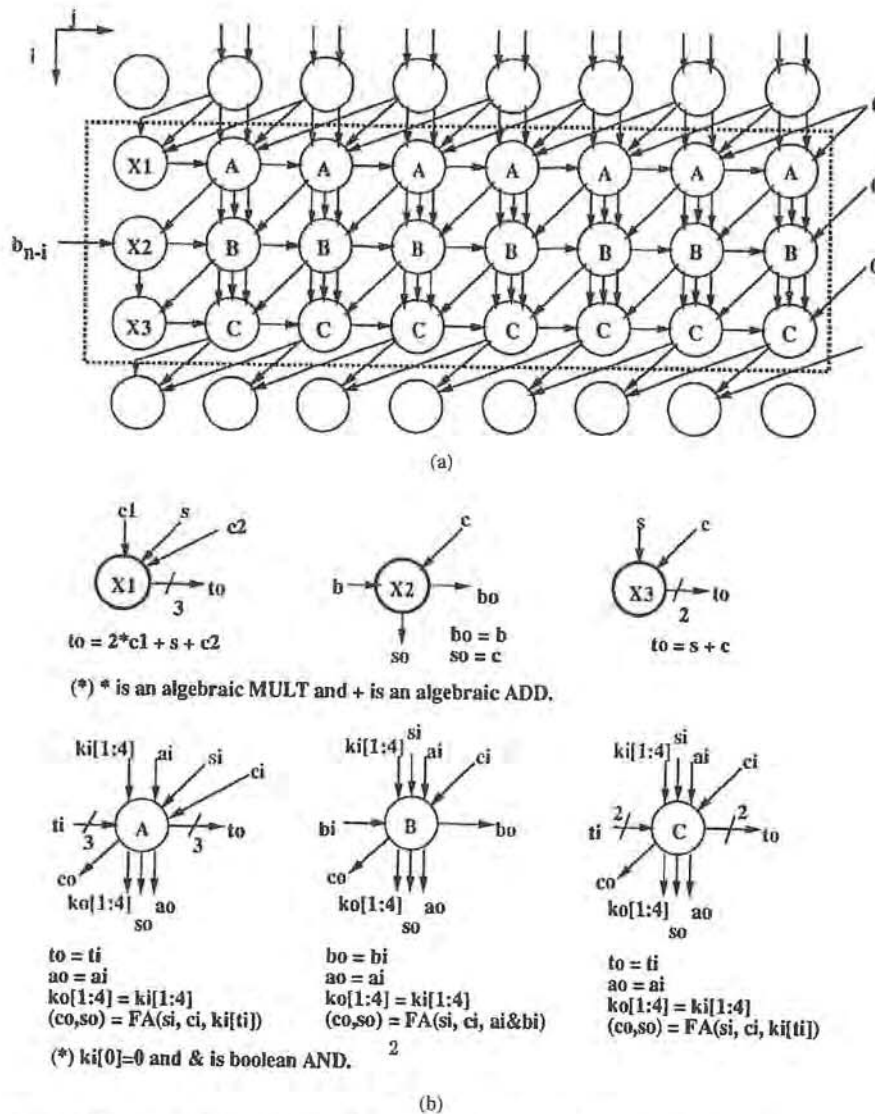


Fig. 2. Array structure for modular multiplication using CSA scheme ( $n = 7$ ): (a)  $i$ th stage of DG for modular multiplication ( $n = 7$ ) and (b) PE node description.

Figs. 2 or 3, we can obtain many different one-dimensional arrays (e.g., bit-serial modulo multiplier) depending on the mapping functions [7].

In our array, the control is generated in a single left-most node which has just four gates (two XOR, one AND, one NOR gate) or two gates (one XOR and one NOR gate). The simplicity of the control nodes gives a much faster clock cycle for the entire array. Thus, it is not the control node but the processing node which determines the clock cycle. Note that all signals in Fig. 2 except the carry ( $c_o$ ) and sum ( $s_o$ ) are *transmittent* signals, which means they are not modified while passing through the array, thus allowing for broadcasting.

Compared to [5], the dependency structure looks the same except for the control nodes due to the basic CSA scheme. However, the main difference is in the function of the control nodes. In [5], the control node (denoted as  $X^5, LU^5, LY^5$ ) is made by merging five or six identical processing nodes and each one ( $X, L, Y, U$ ) is fairly complex (roughly three

XOR's and more than five AND or OR gates). Therefore, the resulting control nodes become five or six times larger, and this is the critical reason for the slow clock cycle time. It is also worthwhile to compare with [4] which claims to be the fastest structure. Our array gives a faster clock cycle (two XOR with one MUX versus five XOR) although it has a longer latency. There is also no restriction on choosing the modulus, thus allowing more general application. Furthermore, we do not need a post processing step because we keep the correct value in all iteration stages. Both methods require a precalculation.

B. Using a Modified CSA Scheme

Now we derive a far simpler array structure from the algorithm (3) by slightly modifying the basic element of the CSA scheme. To directly apply the CSA structure to the modular multiplication algorithm, we have to modify the basic element so that it can accept an additional operand which



TABLE I  
EXAMPLE SHOWING COMPLETE FUNCTION OF FIG. 2 (N = 12)

stage		(carry,sum)	f(.)	b <sub>n-i</sub>
0	P <sub>0</sub>	00 00 00 00 00 00 00 00 00 00 00 00	-	-
1	T <sub>1</sub>	00 00 00 00 00 00 00 00 00 00 00 00	f(.)=0	0
	T <sub>1</sub> *	00 00 00 00 00 00 00 00 00 00 00 00		
	P <sub>1</sub>	00 00 00 00 00 00 00 00 00 00 00 00	f(.)=0	
2	T <sub>2</sub>	00 00 00 00 00 00 00 00 00 00 00 00	f(.)=0	1
	T <sub>2</sub> *	00 01 00 00 01 01 00 00 01 01 00 01		
	P <sub>2</sub>	00 01 00 00 01 01 00 00 01 01 00 01	f(.)=0	
3	T <sub>3</sub>	01 00 00 01 01 00 00 01 01 00 01 00	f(.)=0	0
	T <sub>3</sub> *	01 00 00 01 01 00 00 01 01 00 01 00		
	P <sub>3</sub>	01 00 00 01 01 00 00 01 01 00 01 00	f(.)=0	
4	T <sub>4</sub>	00 01 10 10 01 01 01 10 10 00 01 01	f(.)=1	0
	T <sub>4</sub> *	00 10 01 00 01 01 10 00 01 00 01 01		
	P <sub>4</sub>	01 00 01 00 01 10 00 00 01 00 01 01	f(.)=0	
5	T <sub>5</sub>	00 10 01 11 01 01 00 10 10 10 10 01	f(.)=1	1
	T <sub>5</sub> *	01 00 10 01 01 01 01 00 01 01 00 01		
	P <sub>5</sub>	01 01 00 01 01 01 01 00 01 01 00 01	f(.)=0	
6	T <sub>6</sub>	01 01 10 10 10 10 00 10 01 01 10 01	f(.)=1	1
	T <sub>6</sub> *	01 11 01 01 10 01 01 00 10 11 00 10		
	P <sub>6</sub>	10 01 01 10 00 01 01 01 01 01 01 00	f(.)=0	
7	T <sub>7</sub>	01 11 01 01 10 01 01 01 01 10 00 01	f(.)=2	0
	T <sub>7</sub> *	10 01 01 10 00 01 01 01 10 00 00 01		
	P <sub>7</sub>	00 10 11 01 01 10 01 11 00 01 01 10	f(.)=1	
8	T <sub>8</sub>	01 10 10 11 01 11 01 01 01 11 01 01	f(.)=1	0
	T <sub>8</sub> *	10 01 01 01 10 01 01 01 10 01 01 01		
	P <sub>8</sub>	00 10 10 11 01 10 01 11 00 10 10 10	f(.)=1	
9	T <sub>9</sub>	01 10 10 11 01 11 01 10 01 10 01 01	f(.)=1	1
	T <sub>9</sub> *	10 01 01 01 10 01 10 00 10 00 01 01		
	P <sub>9</sub>	00 10 10 11 01 11 00 10 00 01 10 10	f(.)=1	
10	T <sub>10</sub>	01 10 10 11 10 10 00 01 10 10 01 01	f(.)=1	1
	T <sub>10</sub> *	10 10 01 10 10 01 00 10 10 01 01 10		
	P <sub>10</sub>	01 01 11 10 01 10 01 10 00 10 11 01	f(.)=1	
11	T <sub>11</sub>	10 11 01 11 01 11 00 10 01 10 10 01	f(.)=1	0
	T <sub>11</sub> *	01 01 10 01 10 01 01 00 10 01 00 01		
	P <sub>11</sub>	01 11 01 11 01 10 01 10 00 10 01 10	f(.)=1	
12	T <sub>12</sub>	01 11 10 11 01 10 00 01 00 11 00 01	f(.)=2	1
	T <sub>12</sub> *	10 10 01 01 10 00 00 01 01 01 00 01		
	P <sub>12</sub>	01 01 10 11 01 01 00 10 01 10 01 10	f(.)=1	

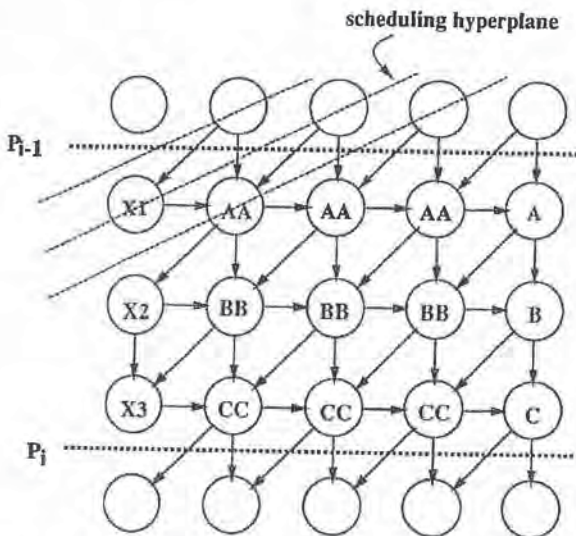


Fig. 3. Regularized DG of Fig. 2 by node merging.

arises from end-around carry terms in the MSB nodes. Now we extend the (3,2) counter to generate a more general adder, which we call a *partially generalized counter* (PGC), as shown

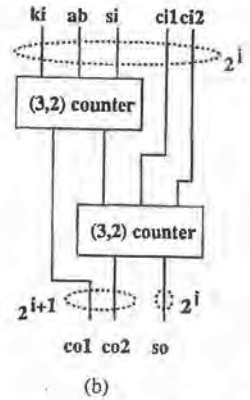
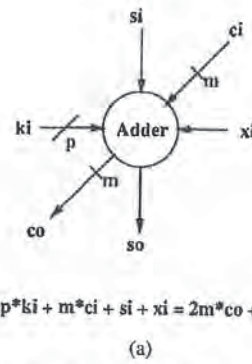


Fig. 4. A partially generalized counter (PGC) and a new adder logic: (a) a PGC element and (b) an adder derived from (a) with  $m = 2, p = 1$ .

in Fig. 4. In Fig. 4(a),  $s_i, c_i$  are a partial sum and a carry of the previous stage. Note that the carry signal is not a single bit, but  $m$ -bits. The variable  $x_i$  is a regular operand which appears in a typical array integer multiplication as  $a_i \& b_j$  (& is logical AND). An extra operand  $k_i$  is introduced with a  $p$ -bit signal for handling the end-around carry terms. So, the arithmetic operation of PGC can be described by

$$2m \cdot c_o + s_o = s_i + m \cdot c_i + x_i + p \cdot k_i \quad (13)$$

where “.” and “+” are algebraic multiplication and addition. If  $m = 1$ , the only possible value of  $p$  is zero, which makes it a typical FA. Therefore, we see that the  $m$  should be at least two to accept an additional operand resulting from end-around carries. Furthermore, if  $m = 2$  the only possible value of  $p$  is one, which results in five inputs and three outputs. This can be easily implemented using two FA's as shown in Fig. 4(b). We can also derive different adders by choosing different  $p$  and  $m$ . However, we want to minimize the number of signal lines to reduce the complexity of the node function.

To apply the newly derived adder in the CSA structure, we need a different CSA form (two carry terms) to express  $P_i$ . Let us denote

$$P_i \equiv 2(C_{i1} + C_{i2}) + S_i, \quad (0 \leq i \leq n) \quad (14)$$

then, the valid range of  $P_i$  is  $0 \leq P_i \leq 5 \cdot 2^n - 5$ . Following the same procedure as the CSA scheme, let us say,  $C_{i1} = \sum_{j=0}^{n-1} c_{i1}^j 2^j, C_{i2} = \sum_{j=0}^{n-1} c_{i2}^j 2^j, S_i = \sum_{j=0}^{n-1} s_i^j 2^j$ . Then, the control generating function  $f(\cdot)$  is

$$f(\cdot) = 2(c_{(i-1)1}^{n-1} + c_{(i-1)2}^{n-1}) + (s_{(i-1)}^{n-1} + C_{(i-1)1}^{n-2} + c_{(i-1)2}^{n-2}). \quad (15)$$

Note that we need seven complement integers,  $K_1, K_2, \dots, K_7$ . Fig. 5 shows an array structure for the modified CSA scheme with node functions. The node type D is a serial connection of two full adders with an 8-1 multiplexor. For the example shown in the previous section, additional  $K_h$ 's should be precalculated as  $K_5 = 011011100001 (= 1679), K_6 = 011011100001 (= 1597), K_7 = 011011100001 (= 1515)$ .

The range of the final output  $P_n$  can be further reduced using two more basic CSA stages as shown in Fig. 6. The first extra CSA stage adds up to sequences of carries and a



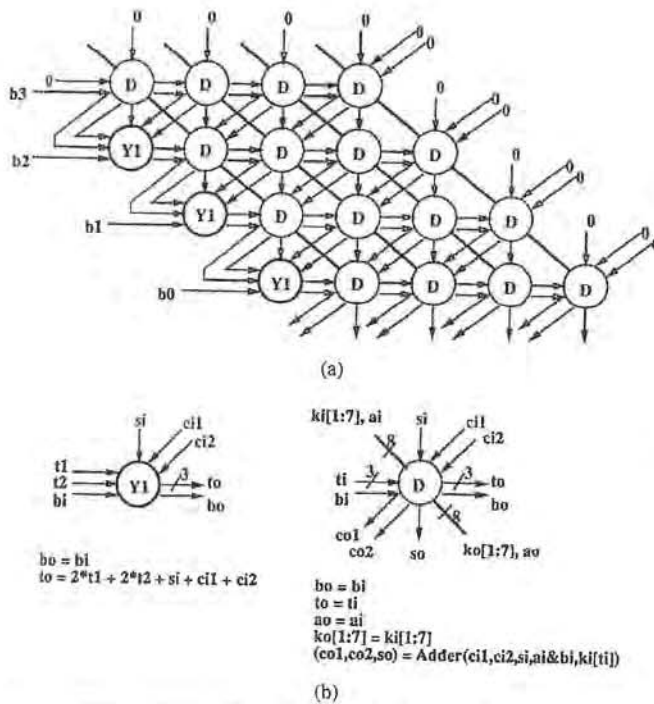


Fig. 5. Array structure for modular multiplication using modified CSA scheme: (a) DG for modular multiplication using CSA scheme ( $n = 4$ ) and (b) PE descriptions.

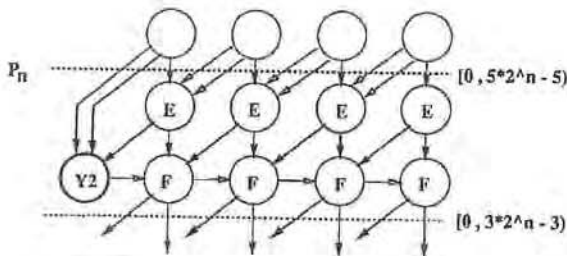


Fig. 6. Extra stages to reduce the range from  $5 \cdot 2^n - 5$  to  $3 \cdot 2^n - 3$ .

sum of  $P_n$  except for the MSB carries. The MSB carries of  $P_n$  are compensated for in the second extra CSA stage. The range  $5 \cdot 2^n - 5$  of  $P_n$  is reduced to  $3 \cdot 2^n - 3$  by replacing maximum  $3 \cdot 2^n$  with  $K_h (K_h < 2^n)$ . At the second CSA stage of Fig. 6, a 4-1 multiplexor is needed instead of an 8-1 multiplexor.

By running SIS [11], a multilevel logic minimization tool, with arbitrary encoding, the control node  $Y_1$  had eight OR gates (including one, three-input OR), nine AND gates (including two, three-input AND), and three inverters, and the combinational logic depth was 12. This is reasonably close to the function of node D (2-bit FA with a multiplexor)<sup>2</sup> in both area and speed. Here again note that all signals are transmittent except carries and a sum.

### III. CONCLUSION AND DISCUSSION

We have shown two new array structures for modular multiplication. Both use the basic CSA structure with some

<sup>2</sup>We used the common mapping to two-input OR gates to measure the logic depth, hence the 2-bit FA has logic depth 9.

TABLE II  
SUMMARY FOR LOGIC OF PE NODES IN TWO ARRAY STRUCTURES

array 1 (Fig. 2)				
X1	X3	A	B	C
(5,3)encoder	(3,2)encoder	(4:1) mux FA AND gate	FA AND gate	(2:1) mux FA AND gate
array 2 (Fig. 5 and Fig. 6)				
Y1	Y2	D	E	F
(8,3) encoder	(4,2) encoder	(8:1) mux 2 FAs AND gate	FA	(4:1) mux FA

modification and do not need any number translation. The complement and its multiples need be updated only when the modulus changes. In RSA applications, the key does not change very often therefore this preprocessing step is acceptable. The details of each processing node in the two array structures are summarized in Table II. The first array needs processing nodes of  $n(X_1 + X_3) + n^2(A + B + C)$ , and the second needs  $(n - 1)Y_1 + Y_2 + n^2D + n(E + F)$ . In each iteration stage, the second array has a smaller number of FA's but the first one has simpler encoders and a multiplexor which lead to a faster clock cycle. Both have a systolic schedule which means they can be fully bit-wise systolized for maximum throughput.

Our approach has advantages over other previous array structures. First, it is more general and has no restrictions in choosing the modulus, hence can be used in any application in which a larger number of computations are required for a relatively long-lasting modulus (RSA, key-exchange, special purpose DSP chip). Second, the algorithm and architecture is simple to understand and verify, hence is easy to modify for a hardware implementation, and does not use any special technique like sign estimation which may imply a significant degree of hardware and verification complexity. We could obtain a faster clock cycle by reducing the complexity of the control nodes in both area and speed. From an algorithmic point of view, the concerns put forward in most previous papers on deciding multiples of the modulus have been eliminated by multiplexing precalculated complement numbers. We have verified our array structures first by C programming and then by implementing two prototype VLSI designs which were verified for function and timing using logic and circuit simulation.

Finally, the RSA algorithm requires more than 500 bits for security reasons, which may make the array multiplier too large ( $\sim 15$  million gates including pipeline stages). To maintain high performance for larger bit-lengths, we need to map the original array onto smaller processor arrays in order to build large "virtual" modular multipliers on fixed sized arrays, called *partitioning* [7]. The regularity of our algorithm makes it easy to find an appropriate partitioning strategy. Because the control nodes which generate the multiplexor control signals are located in the MSB in each iteration, the LPGS (*locally parallel, globally sequential* [7]) scheme is an appropriate choice, needing some extra buffers outside the processor array to contain intermediate data for each block.



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# Attachment 6B

# VLSI Array Algorithms and Architectures for RSA Modular Multiplication

Yong-Jin Jeong, *Member, IEEE*, and Wayne P. Burlison, *Member, IEEE*

**Abstract**—We present two novel iterative algorithms and their array structures for integer modular multiplication. The algorithms are designed for Rivest–Shamir–Adelman (RSA) cryptography and are based on the familiar iterative *Horner’s rule*, but use precalculated complements of the modulus. The problem of deciding which multiples of the modulus to subtract in intermediate iteration stages has been simplified using simple look-up of precalculated complement numbers, thus allowing a finer-grain pipeline. Both algorithms use a carry save adder scheme with modulo reduction performed on each intermediate partial product which results in an output in carry-save format. Regularity and local connections make both algorithms suitable for high-performance array implementation in FPGA’s or deep submicron VLSI. The processing nodes consist of just one or two full adders and a simple multiplexor. The stored complement numbers need to be precalculated only when the modulus is changed, thus not affecting the performance of the main computation. In both cases, there exists a bit-level systolic schedule, which means the array can be fully pipelined for high performance and can also easily be mapped to linear arrays for various space/time tradeoffs.

**Index Terms**—Cryptography, modular multiplication, RSA, systolic arrays, VLSI.

## I. INTRODUCTION

CRYPTOGRAPHY systems have been growing in importance recently as a method for improving data security. *Public key cryptography* (PKC) systems are generally preferred to traditional *secret key cryptography* systems like the *data encryption standard* due to the safety of key distribution [3]. The Rivest–Shamir–Adelman (RSA) [10] system is one of the most widely used public key cryptography systems, and its core arithmetic is modular multiplication over a positive integer. Modular multiplication is also a major computation of *residue number systems* [13] as well as other cryptography systems (e.g., *international data encryption algorithm* [8], [16], Diffie–Hellman key exchange [3]). In this paper, we develop an array modular multiplier with applications to, but not restricted to, RSA systems.

In RSA, the modulus is a product of two large prime numbers, usually more than 500 bits, and should be changeable for security reasons. But, since the modulus (or key) is not changed very often, we can use precomputation and look-up in our array modular multipliers. We are not aware of anyone

who has utilized this special property of *multirate input data* in the RSA algorithm, that is, the *input message* changes rapidly while the *key* remains unchanged for a long period. In practice, the key is updated infrequently, for example, a few months, weeks, or days, depending on the security requirements. In order to satisfy the ever growing security requirements of high-speed communications, such as personal communication services and wireless local area networks, a *dedicated* VLSI hardware solution is needed because of 1) high throughput requirements, 2) low-power requirements, 3) a high-volume market, 4) the computation is poorly suited to microprocessors or DSP’s, and 5) the problem size is expected to continue to grow rather than saturate.

Modular multiplication is generally considered a complicated arithmetic operation because of the inherent multiplication and division operations. There are two main approaches to computing modular multiplication: 1) perform the modulo operation *after* multiplication or 2) *during* multiplication. The modulo operation is accomplished by integer division in which only the remainder is needed for further computation. The first approach requires a  $n \times n$  bit multiplier with a  $2n$ -bit register followed by a  $2n \times n$  bit divider. In the second approach, the modulo operation occurs in each iteration step of integer multiplication. Therefore the first approach requires more hardware while the second requires more addition/subtraction computations due to  $O(n)$  modulo reduction steps. In both cases, most previous research has focused on the fast calculation of a long carry chain. Redundant number systems and a higher radix carry-save form are some of the different number representations that have been used for this purpose [12], [14]. A carry prediction technique has also been used for fast calculation of modular multiplication [1].

Since PKC was introduced, many algorithms and hardware structures have been proposed for modular multiplication, and [4] contains a good review on this topic. Several array structures suited for VLSI implementation have been discussed in [4], [5], [14], and [15]. In [14], Vandemeulebroecke *et al.*, use a *modulo after multiplication* approach using a *signed digit* number representation. It consists of two arrays: one for multiplication and the other for integer division. In [5], Koc and Hung apply Blakley’s algorithm [2] and use a sign-estimation method by looking at the five most significant bits in each iteration stage. Although they derive a bit-level systolic array structure, the latency and clock cycle are relatively long due to the control node which estimates the sign of the intermediate result in each stage. In [4] and [15], Eldridge and Walter use Montgomery’s algorithm [9] which only works if

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the modulus is relatively prime to the radix, although this is always the case in RSA.

In this paper, we develop two new VLSI array architectures for modular multiplication. The idea is similar to Montgomery's algorithm in which he tries to make each partial product a multiple of the radix to simplify the multiplication by the radix (just by shifting) by only looking at the least significant bits (LSB), thus requiring a post-processing step to get the final answer. In our algorithms, we look at the most significant bits (MSB) to remove higher bit positions while keeping the correct answer in each partial product, keeping it within a certain range. Due to the simple translation of a modulo operation into an addition of a precalculated complement of the modulus, the *modulo during multiplication* approach is used with a carry-save adder structure. Instead we pay for multiplexers to choose the precalculated integer depending on the control which is generated in the leftmost node in each stage. Compared to previous works, we can obtain a higher clock frequency mainly due to the simplified modulo reduction operation. In Section II, we will explain our basic concept for the modulo reduction operation and then describe the two iterative algorithms. Array structures corresponding to these algorithms, analysis, and some modifications are also discussed in this section. Conclusions and discussion are in Section III.

## II. MODULAR MULTIPLICATION ALGORITHM

In a modular multiplication, the  $n$ -bit modulus  $C$  is represented by a binary number system as  $C = \sum_{i=0}^{n-1} c_i 2^i$  where  $c_i \in GF(2)$ . Obviously  $C$  is less than  $2^n$ . We introduce  $K$ , which is called the *complement* of the modulus  $C$ , such that

$$K \equiv 2^n \pmod{C}. \quad (1)$$

In other words, any carry of weight  $2^n$  can be replaced by an addition of  $K$ , which means that the end-around carry implies an extra addition. If  $K$  does not change frequently, we can precalculate multiples of  $K$  and store them in registers for use in the modulo reduction operation. Note that if the MSB of  $C$  is 1,  $K$  is equivalent to  $-C$  in a 2's complement number system.

Now we describe the general modular multiplication algorithm using the *modulo during multiplication* approach. Given any two  $n$ -bit integers,  $A$  and  $B$ , and the  $n$ -bit modulus  $C$ , where  $(C > A, B)$ , the modular multiplication can be described by an iterative procedure using *Horner's rule*

$$\begin{aligned} AB \pmod{C} &= A \cdot \sum_{i=0}^{n-1} b_i 2^i \pmod{C} \\ &= ((\dots((b_{n-1}A)2 + b_{n-2}A)2 \\ &\quad + \dots + b_1A)2 + b_0A) \pmod{C}. \end{aligned} \quad (2)$$

We can describe (2) in a recursive form as follows:

$$\begin{aligned} P_0 &= 0 \\ P_i &= 2P_{i-1} + b_{n-1}A \pmod{C} \end{aligned} \quad (3)$$

and  $P_n$  is the final result. Using (1) and (3), we will derive two different bit-level array structures.

### A. Using the CSA Scheme

The carry save addition (CSA) scheme is the most commonly used technique in integer multiplication to reduce the carry propagation penalty [6]. In the CSA scheme, a partial sum and a carry sequence are generated in the intermediate stages and the carry propagation occurs only at the last stage. The basic element of the CSA scheme is a full adder (FA) which is often called a (3, 2) counter. It accepts three inputs, referred to here as  $s_i, c_i, x_i$  with (associated weight  $2^i$ ), and produces two outputs, carry  $c_o$  (with weight  $2^{i+1}$ ) and sum  $s_o$  (with weight  $2^i$ ). The arithmetic operation of the (3, 2) counter can thus be described by the familiar expression:

$$2c_o + s_o = s_i + c_i + x_i \quad (4)$$

where "+" means an algebraic (not Boolean) addition.

Using the CSA scheme, we have a carry of weight  $2^n$  in the leftmost node in each stage. As shown in (1), this carry can be replaced by the addition of the integer  $K$  for a modulo operation. The basic idea in our approach is that we handle the carries of weight  $2^n$  and higher by using  $K$  wherever they appear, unless the basic CSA structure is broken. From (3), let us denote a partial product  $P_i$  as

$$P_i \equiv 2C_i + S_i \quad (0 \leq i \leq n) \quad (5)$$

then, the valid range of  $P_i$  is

$$0 \leq P_i \leq 3 \cdot 2^n - 3. \quad (6)$$

This means we allow  $P_i$  to be greater than modulus  $C$  at intermediate stages.

Before we begin the derivation of a recursive equation for modulo multiplication, we define a new variable  $K_h$  to handle multiple end-around carries

$$K_h \stackrel{\text{def}}{=} h \cdot K \pmod{C} \quad (7)$$

where  $h$  is a positive integer (1, 2, ...) and  $K$  is defined in (1). Then

$$2^{n+j} \pmod{C} = 2^j \cdot K \pmod{C}.$$

Carries can also appear in a combined mode. As an example, suppose we have two carries of weight  $2^{n+1}$  and one carry of weight  $2^n$ , then  $(2^{n+1} + 2^{n+1} + 2^n) \pmod{C} = 5 \cdot 2^n \pmod{C} = 5 \cdot K \pmod{C} = K_5$ .

Equation (3) contains two modulo reduction steps and can be written by introducing a new partial product term  $T_i$ , as

$$\begin{aligned} \text{i) } T_i &= 2P_{i-1} \pmod{C} \\ \text{ii) } P_i &= (T_i + b_{n-1}A) \pmod{C}. \end{aligned} \quad (8)$$

But step ii) cannot be implemented by the CSA scheme because it has four operands to be added. (Note that the modulo operation implies at least one extra addition of  $K$ .) This can be solved by dividing step ii) into two steps as

$$\begin{aligned} \text{i) } T_i &= 2P_{i-1} \pmod{C} \\ \text{ii-a) } T_i^* &= T_i + b_{n-1}A \\ \text{ii-b) } P_i &= T_i^* \pmod{C}. \end{aligned} \quad (9)$$

In step i),  $2P_{i-1}$  implies one  $2^{n+1}$  term ( $c_{i-1}^{n-1}$ ) and two  $2^n$  terms ( $s_{i-1}^{n-1}$  and  $c_{i-1}^{n-2}$ ), which can generate a maximum of  $4 \cdot 2^n$ .<sup>1</sup> In step ii-a), we do not perform the modulo operation because there are already three operands: two from  $T_i$  in carry save form, and one for  $A$  depending on  $b_{n-i}$ . Instead we want to pass through the MSB carry of  $T_i$  to step ii-b). So, in step ii-b), we will have at most  $2 \cdot 2^n$  (one passed from  $T_i$  and another newly generated in  $T_i^*$ ) as end-around carries. In both the steps i) and ii-b), only one additional operand is allowed. That is why we precalculate the  $K_h$ 's instead of adding  $K$  multiple times.

To explain the algorithm more formally, we define  $\sigma(P_i)$  as follows:

$$\sigma(P_i) \stackrel{\text{def}}{=} P_i - h \cdot 2^n + K_h$$

where

$$h = f(x_1, x_2, x_3, \dots, x_r) \quad (10)$$

and the function  $f(\cdot)$  calculates the total magnitude of end-around carries, and  $x_1, x_2, \dots, x_r$  are bit variables (always carries and sums of the MSB position) which contribute to the translation of (1). Thus

$$f(x_1, x_2, \dots, x_r) = \sum_{k=1}^r \alpha_k x_k \quad (11)$$

where  $\alpha_k = 1$  if  $x_k$  has weight  $2^n$ ,  $\alpha_k = 2$  if the weight is  $2^{n+1}$ ,  $\alpha_k = 4$  if the weight is  $2^{n+2}$ , and so on. In other words,  $\sigma(P_i)$  replaces  $h \cdot 2^n$  with  $K_h$  which is precalculated.

Using (10), we can rewrite algorithm (9) as follows:

$$\begin{aligned} \text{i)} \quad & T_i = \sigma(2P_{i-1}) \\ \text{ii-a)} \quad & T_i^* = T_i + b_{n-1} A \\ \text{ii-b)} \quad & P_i = \sigma(T_i^*). \end{aligned} \quad (12)$$

As we can see in Fig. 1, the function  $f(\cdot)$  of the above algorithm is

$$\begin{aligned} \text{for step i)} \quad & f(\cdot) = 2c_{i-1}^{n-1} + s_{i-1}^{n-1} + c_{i-1}^{n-2} \\ \text{for step ii-b)} \quad & f(\cdot) = \gamma_i^{n-1} + \gamma_i^{*n-1} \end{aligned}$$

where  $\gamma_i^{n-1}, \gamma_i^{*n-1}$  are the MSB carries of  $T_i$  and  $T_i^*$ , respectively (both have the weight  $2^n$ ).

Now we will informally verify that the algorithm (12) satisfies the valid range of (6) for all  $P_i$ 's ( $i = 0, 1, \dots, n$ ). Obviously  $0 \leq P_0 < 3 \cdot 2^n - 3$ . Suppose  $0 \leq P_{i-1} < 3 \cdot 2^n - 3$ , then

$$\begin{aligned} 0 &\leq 2P_{i-1} \\ &< 6 \cdot 2^n - 6 \\ 0 &\leq \sigma(2P_{i-1}) \\ &< 6 \cdot 2^n - 6 - 4 \cdot 2^n + 2^n \\ &= 3 \cdot 2^n - 6 \\ 0 &\leq T_i^* \\ &< 4 \cdot 2^n - 6 \end{aligned}$$

<sup>1</sup>Subscript is for an iteration stage and superscript is for denoting bit positions, that is,  $S_i = \sum_{j=0}^{i-1} s_i^j \cdot 2^j$ . Also note that lower case letters are used for bit-level variables while upper case is for word-level variables.

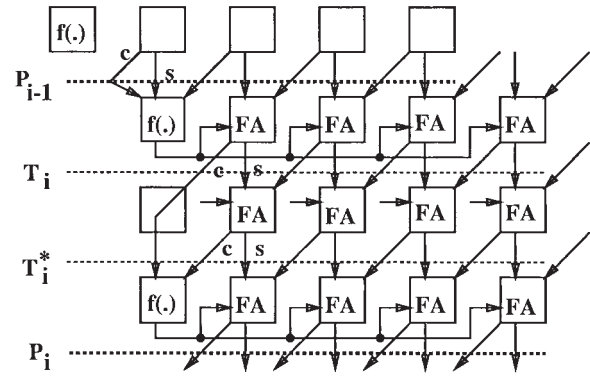


Fig. 1. An iteration stage of modular multiplication using the CSA scheme.

$$\begin{aligned} 0 &\leq \sigma(T_i^*) \\ &< 4 \cdot 2^n - 6 - 2 \cdot 2^n + 2^n \\ &< 3 \cdot 2^n - 3 \end{aligned}$$

which assures  $0 \leq P_i < 3 \cdot 2^n - 3$ . Therefore the algorithm (12) produces a final output  $P_n$  which is less than  $3 \cdot 2^n - 3$ . It can be directly fed into the next multiplication stage for further iteration if necessary (e.g., exponentiation).

Fig. 2(a) shows a single stage of the dependence graph (DG) which can be directly implemented as a parallel array multiplier. Fig. 2(b) describes the node functions. The nodes  $X_1, X_3$  are control nodes which calculate the control value  $h$  of (10), and hence need simple encoders. The node  $X_2$  is just a wire. Node type A is a FA with a 4-1 multiplexor and an AND gate. Node type B is just a FA with an AND gate and node type C is a FA with a 2-1 multiplexor and an AND gate. Note that node type B does not need a multiplexor and type C needs only  $K_1$  and  $K_2$  because the max value of  $h$  is two in node  $X_3$ . An AND gate is needed in type A and C to accept  $K_0 = 0$  when the control value  $h$  is zero. There exists a systolic schedule which is not linear due to its skewed connection between the stages. Table I shows an example for our new bit-level modular multiplication algorithm using  $n = 12$ , with  $A = 010001000100 (= 1092)$ ,  $B = 010011001101 (= 1229)$ , and  $C = 100000101001 (= 2089)$ . The  $K_h$ 's are precalculated as  $K_1 = K = 01111010111 (= 2007)$ ,  $K_2 = 011110000101 (= 1925)$ ,  $K_3 = 011100110011 (= 1843)$ ,  $K_4 = 011011100001 (= 1761)$ . The final output is

$$\begin{aligned} P_n &= 2(001100010101) + (110111001010) \\ &= 1001111110100 \\ & (= 5108) \end{aligned}$$

which equals 930 after modulo reduction to 2089.

By merging two nodes into one in each row as has been done in [5], one can modify the DG in Fig. 2 to derive a simpler DG. This is shown in Fig. 3. Node types AA, BB, CC are newly merged nodes which have two A, B, C type nodes, respectively. It now allows a linear systolic schedule and shows a better overview of the hardware array implementation. If the wordlength  $n$  is an even number, then all nodes except the control nodes will be merged nodes. Here we have the original nodes A, B, C in the LSB place because  $n$  is odd. From

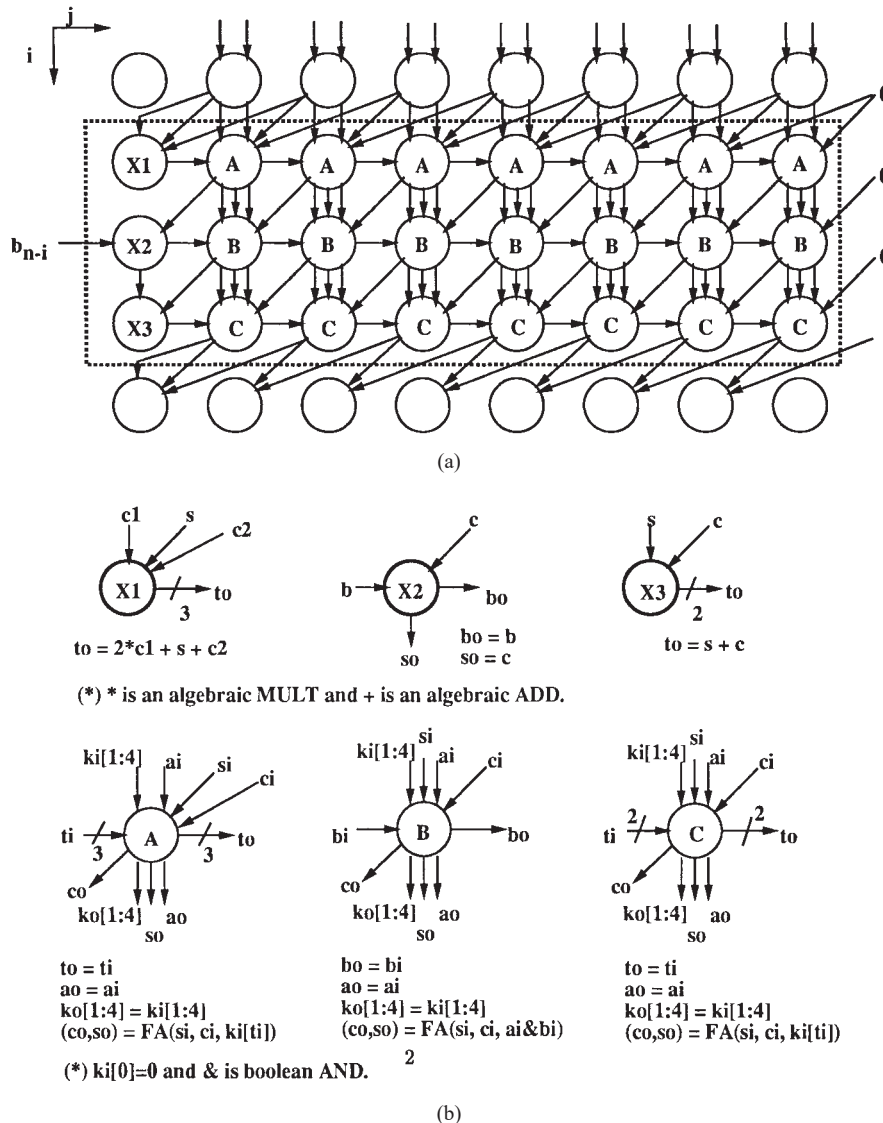


Fig. 2. Array structure for modular multiplication using CSA scheme ( $n = 7$ ): (a)  $i$ th stage of DG for modular multiplication ( $n = 7$ ) and (b) PE node description.

Figs. 2 or 3, we can obtain many different one-dimensional arrays (e.g., bit-serial modulo multiplier) depending on the mapping functions [7].

In our array, the control is generated in a single left-most node which has just four gates (two XOR, one AND, one NOR gate) or two gates (one XOR and one NOR gate). The simplicity of the control nodes gives a much faster clock cycle for the entire array. Thus, it is not the control node but the processing node which determines the clock cycle. Note that all signals in Fig. 2 except the carry ( $c_o$ ) and sum ( $s_o$ ) are *transmittent* signals, which means they are not modified while passing through the array, thus allowing for broadcasting.

Compared to [5], the dependency structure looks the same except for the control nodes due to the basic CSA scheme. However, the main difference is in the function of the control nodes. In [5], the control node (denoted as  $X^5$ ,  $LU^5$ ,  $LY^5$ ) is made by merging five or six identical processing nodes and each one ( $X$ ,  $L$ ,  $Y$ ,  $U$ ) is fairly complex (roughly three

XOR's and more than five AND or OR gates). Therefore, the resulting control nodes become five or six times larger, and this is the critical reason for the slow clock cycle time. It is also worthwhile to compare with [4] which claims to be the fastest structure. Our array gives a faster clock cycle (two XOR with one MUX versus five XOR) although it has a longer latency. There is also no restriction on choosing the modulus, thus allowing more general application. Furthermore, we do not need a post processing step because we keep the correct value in all iteration stages. Both methods require a precalculation.

*B. Using a Modified CSA Scheme*

Now we derive a far simpler array structure from the algorithm (3) by slightly modifying the basic element of the CSA scheme. To directly apply the CSA structure to the modular multiplication algorithm, we have to modify the basic element so that it can accept an additional operand which



TABLE I  
EXAMPLE SHOWING COMPLETE FUNCTION OF FIG. 2 ( $N = 12$ )

stage		(carry,sum)	$f(\cdot)$	$b_{n-i}$
0	$P_0$	00 00 00 00 00 00 00 00 00 00 00 00	-	-
1	$T_1$	00 00 00 00 00 00 00 00 00 00 00 00	$f(\cdot)=0$	0
	$T_1^*$	00 00 00 00 00 00 00 00 00 00 00 00		
	$P_1$	00 00 00 00 00 00 00 00 00 00 00 00	$f(\cdot)=0$	
2	$T_2$	00 00 00 00 00 00 00 00 00 00 00 00	$f(\cdot)=0$	1
	$T_2^*$	00 01 00 00 01 01 00 00 01 01 00 01		
	$P_2$	00 01 00 00 01 01 00 00 01 01 00 01	$f(\cdot)=0$	
3	$T_3$	01 00 00 01 01 00 00 01 01 00 01 00	$f(\cdot)=0$	0
	$T_3^*$	01 00 00 01 01 00 00 01 01 00 01 00		
	$P_3$	01 00 00 01 01 00 00 01 01 00 01 00	$f(\cdot)=0$	
4	$T_4$	00 01 10 10 01 01 01 10 00 10 01 01	$f(\cdot)=1$	0
	$T_4^*$	00 10 01 00 01 01 10 00 01 00 01 01		
	$P_4$	01 00 01 00 01 10 00 00 01 00 01 01	$f(\cdot)=0$	
5	$T_5$	00 10 01 11 01 01 00 10 00 10 10 01	$f(\cdot)=1$	1
	$T_5^*$	01 00 10 01 01 01 01 00 01 01 00 01		
	$P_5$	01 01 00 01 01 01 01 00 01 01 00 01	$f(\cdot)=0$	
6	$T_6$	01 01 10 10 10 10 00 10 01 01 10 01	$f(\cdot)=1$	1
	$T_6^*$	01 11 01 01 10 01 01 00 10 11 00 10		
	$P_6$	10 01 01 10 00 01 01 01 01 01 01 00	$f(\cdot)=0$	
7	$T_7$	01 11 01 01 10 01 01 01 01 10 00 01	$f(\cdot)=2$	0
	$T_7^*$	10 01 01 10 00 01 01 01 10 00 00 01		
	$P_7$	00 10 11 01 01 10 01 11 00 01 01 10	$f(\cdot)=1$	
8	$T_8$	01 10 10 11 01 11 01 01 01 11 01 01	$f(\cdot)=1$	0
	$T_8^*$	10 01 01 01 10 01 01 01 10 01 01 01		
	$P_8$	00 10 10 11 01 10 01 11 00 10 10 10	$f(\cdot)=1$	
9	$T_9$	01 10 10 11 01 11 01 10 01 10 01 01	$f(\cdot)=1$	1
	$T_9^*$	10 01 01 01 10 01 10 00 10 00 01 01		
	$P_9$	00 10 10 11 01 11 00 10 00 01 10 10	$f(\cdot)=1$	
10	$T_{10}$	01 10 10 11 10 10 00 01 10 10 01 01	$f(\cdot)=1$	1
	$T_{10}^*$	10 10 01 10 10 01 00 10 10 01 01 10		
	$P_{10}$	01 01 11 10 01 10 01 10 00 10 11 01	$f(\cdot)=1$	
11	$T_{11}$	10 11 01 11 01 11 00 10 01 10 10 01	$f(\cdot)=1$	0
	$T_{11}^*$	01 01 10 01 10 01 01 00 10 01 00 01		
	$P_{11}$	01 11 01 11 01 10 01 10 00 10 01 10	$f(\cdot)=1$	
12	$T_{12}$	01 11 10 11 01 10 00 01 00 11 00 01	$f(\cdot)=2$	1
	$T_{12}^*$	10 10 01 01 10 00 00 01 01 01 00 01		
	$P_{12}$	01 01 10 11 01 01 00 10 01 10 01 10	$f(\cdot)=1$	

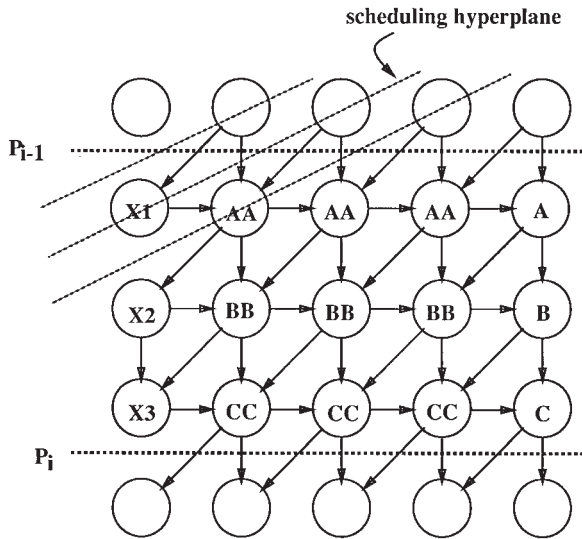


Fig. 3. Regularized DG of Fig. 2 by node merging.

arises from end-around carry terms in the MSB nodes. Now we extend the (3, 2) counter to generate a more general adder, which we call a *partially generalized counter* (PGC), as shown

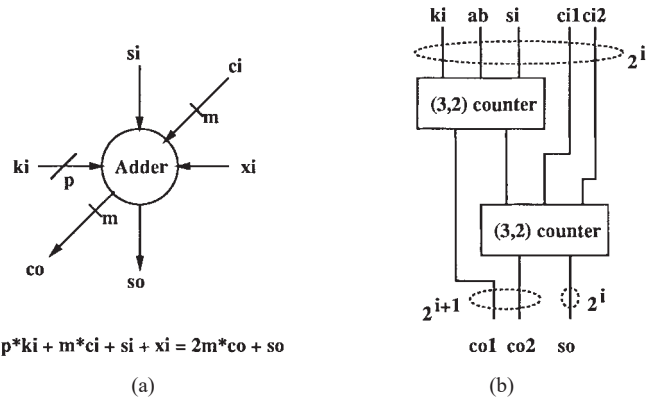


Fig. 4. A partially generalized counter (PGC) and a new adder logic: (a) a PGC element and (b) an adder derived from (a) with  $m = 2, p = 1$ .

in Fig. 4. In Fig. 4(a),  $s_i, c_i$  are a partial sum and a carry of the previous stage. Note that the carry signal is not a single bit, but  $m$ -bits. The variable  $x_i$  is a regular operand which appears in a typical array integer multiplication as  $a_i \& b_j$  (& is logical AND). An extra operand  $k_i$  is introduced with a  $p$ -bit signal for handling the end-around carry terms. So, the arithmetic operation of PGC can be described by

$$2m \cdot c_o + s_o = s_i + m \cdot c_i + x_i + p \cdot k_i \quad (13)$$

where “ $\cdot$ ” and “+” are algebraic multiplication and addition. If  $m = 1$ , the only possible value of  $p$  is zero, which makes it a typical FA. Therefore, we see that the  $m$  should be at least two to accept an additional operand resulting from end-around carries. Furthermore, if  $m = 2$  the only possible value of  $p$  is one, which results in five inputs and three outputs. This can be easily implemented using two FA’s as shown in Fig. 4(b). We can also derive different adders by choosing different  $p$  and  $m$ . However, we want to minimize the number of signal lines to reduce the complexity of the node function.

To apply the newly derived adder in the CSA structure, we need a different CSA form (two carry terms) to express  $P_i$ . Let us denote

$$P_i \equiv 2(C_{i1} + C_{i2}) + S_i, \quad (0 \leq i \leq n) \quad (14)$$

then, the valid range of  $P_i$  is  $0 \leq P_i \leq 5 \cdot 2^n - 5$ . Following the same procedure as the CSA scheme, let us say,  $C_{i1} = \sum_{j=0}^{n-1} c_{i1}^j 2^j, C_{i2} = \sum_{j=0}^{n-1} c_{i2}^j 2^j, S_i = \sum_{j=0}^{n-1} s_i^j 2^j$ . Then, the control generating function  $f(\cdot)$  is

$$f(\cdot) = 2(c_{(i-1)1}^{n-1} + c_{(i-1)2}^{n-1}) + (s_{i-1}^{n-1} + C_{(i-1)1}^{n-2} + c_{(i-1)2}^{n-2}). \quad (15)$$

Note that we need seven complement integers,  $K_1, K_2, \dots, K_7$ . Fig. 5 shows an array structure for the modified CSA scheme with node functions. The node type D is a serial connection of two full adders with an 8-1 multiplexor. For the example shown in the previous section, additional  $K_h$ ’s should be precalculated as  $K_5 = 011011100001 (= 1679), K_6 = 011011100001 (= 1597), K_7 = 011011100001 (= 1515)$ .

The range of the final output  $P_n$  can be further reduced using two more basic CSA stages as shown in Fig. 6. The first extra CSA stage adds up to sequences of carries and a

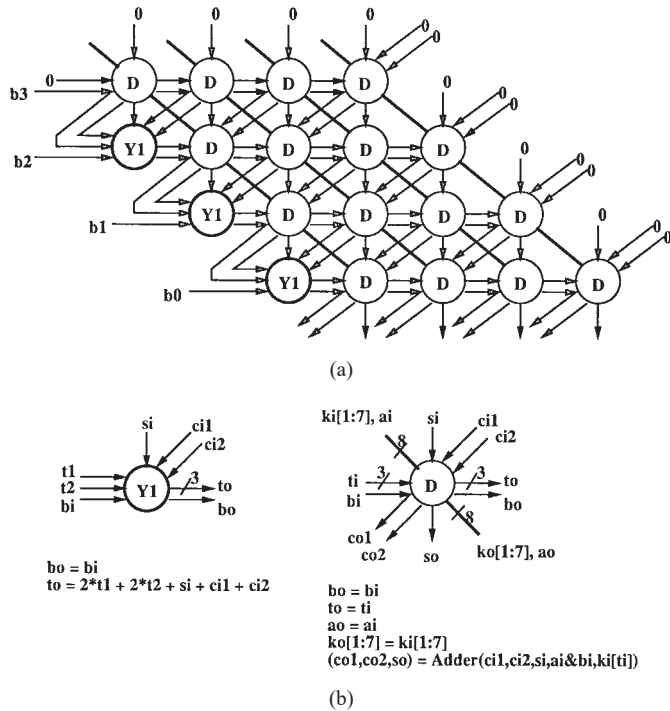


Fig. 5. Array structure for modular multiplication using modified CSA scheme: (a) DG for modular multiplication using CSA scheme ( $n = 4$ ) and (b) PE descriptions.

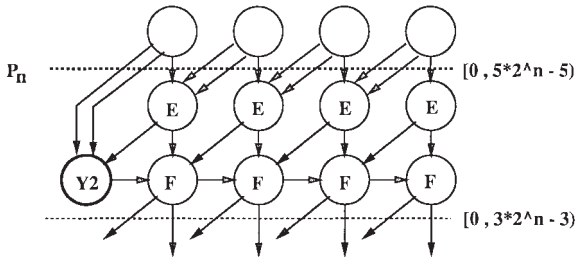


Fig. 6. Extra stages to reduce the range from  $5 \cdot 2^n - 5$  to  $3 \cdot 2^n - 3$ .

sum of  $P_n$  except for the MSB carries. The MSB carries of  $P_n$  are compensated for in the second extra CSA stage. The range  $5 \cdot 2^n - 5$  of  $P_n$  is reduced to  $3 \cdot 2^n - 3$  by replacing maximum  $3 \cdot 2^n$  with  $K_h(K_h < 2^n)$ . At the second CSA stage of Fig. 6, a 4-1 multiplexer is needed instead of an 8-1 multiplexer.

By running SIS [11], a multilevel logic minimization tool, with arbitrary encoding, the control node  $Y_1$  had eight OR gates (including one, three-input OR), nine AND gates (including two, three-input AND), and three inverters, and the combinational logic depth was 12. This is reasonably close to the function of node D (2-bit FA with a multiplexor)<sup>2</sup> in both area and speed. Here again note that all signals are transmittent except carries and a sum.

### III. CONCLUSION AND DISCUSSION

We have shown two new array structures for modular multiplication. Both use the basic CSA structure with some

<sup>2</sup>We used the common mapping to two-input OR gates to measure the logic depth, hence the 2-bit FA has logic depth 9.

TABLE II  
SUMMARY FOR LOGIC OF PE NODES IN TWO ARRAY STRUCTURES

array 1 (Fig. 2)				
X1	X3	A	B	C
(5,3)encoder	(3,2)encoder	(4:1) mux FA AND gate	FA AND gate	(2:1) mux FA AND gate
array 2 (Fig. 5 and Fig. 6)				
Y1	Y2	D	E	F
(8,3) encoder	(4,2) encoder	(8:1) mux 2 FAs AND gate	FA	(4:1) mux FA

modification and do not need any number translation. The complement and its multiples need be updated only when the modulus changes. In RSA applications, the key does not change very often therefore this preprocessing step is acceptable. The details of each processing node in the two array structures are summarized in Table II. The first array needs processing nodes of  $n(X_1 + X_3) + n^2(A + B + C)$ , and the second needs  $(n - 1)Y_1 + Y_2 + n^2D + n(E + F)$ . In each iteration stage, the second array has a smaller number of FA's but the first one has simpler encoders and a multiplexor which lead to a faster clock cycle. Both have a systolic schedule which means they can be fully bit-wise systolized for maximum throughput.

Our approach has advantages over other previous array structures. First, it is more general and has no restrictions in choosing the modulus, hence can be used in any application in which a larger number of computations are required for a relatively long-lasting modulus (RSA, key-exchange, special purpose DSP chip). Second, the algorithm and architecture is simple to understand and verify, hence is easy to modify for a hardware implementation, and does not use any special technique like sign estimation which may imply a significant degree of hardware and verification complexity. We could obtain a faster clock cycle by reducing the complexity of the control nodes in both area and speed. From an algorithmic point of view, the concerns put forward in most previous papers on deciding multiples of the modulus have been eliminated by multiplexing precalculated complement numbers. We have verified our array structures first by C programming and then by implementing two prototype VLSI designs which were verified for function and timing using logic and circuit simulation.

Finally, the RSA algorithm requires more than 500 bits for security reasons, which may make the array multiplier too large (~15 million gates including pipeline stages). To maintain high performance for larger bit-lengths, we need to map the original array onto smaller processor arrays in order to build large "virtual" modular multipliers on fixed sized arrays, called *partitioning* [7]. The regularity of our algorithm makes it easy to find an appropriate partitioning strategy. Because the control nodes which generate the multiplexor control signals are located in the MSB in each iteration, the LPGS (*locally parallel, globally sequential* [7]) scheme is an appropriate choice, needing some extra buffers outside the processor array to contain intermediate data for each block.



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Dr. Burleson is a member of the ACM and Sigma Xi.

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## Abstract

Cylindrical arrays have been shown useful for VLSI implementation of a variety of problems including matrix-matrix multiplication and algebraic path determination. However, spiral feedback paths limit their scalability due to performance degradation in interconnect-delay dominant environments. A recently proposed feedback-pipelining technique can efficiently address this problem when signal paths are non-diametric in the projection direction. However, this method may incur excessive penalties when the latter condition does not hold. In this paper, a new class of cylindrical array is proposed, the *ring-planarized cylindrical array*, which overcomes the barrier to efficient, fully-pipelined arrays projected in directions having diametric signal paths. In contrast to standard cylindrical arrays, processors from each cylinder row are distributed along planar ring structures rather than lines. This construction inherently constrains maximum signal path length to a constant, permitting efficient scalability. Application to the cryptographically relevant modular multiplication problem is demonstrated.

## 1 INTRODUCTION

Systolic arrays remain an essential architectural methodology due to inherent properties of modularity, regularity, local interconnection, and high degree of pipelining [1]. Moreover, as interconnect delay grows increasingly dominant as deep-submicron technology progresses to smaller dimensions, systolic techniques become even more relevant in the quest to attain the highest levels of performance.

Cylindrical arrays belong to the subset of array architectures which exhibit spiral interconnections, and have been utilized in problems such as matrix-matrix multiplication [2] and the algebraic path problem [3]. Although these arrays exhibit some interesting properties, they have been underutilized, due to the fact that the spiral feedback paths are not strictly local. Therefore, the interconnect delay of such paths can become a dominating factor as the array size increases.

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In [4], a folded array methodology and two alternatives were presented to address performance scalability in the modular multiplication problem. The rudimentary embodiment of the former technique can be effectively described in terms of mapping to a standard cylindrical array. However, it was further demonstrated that by applying proper temporal transformations to the array (in the form of rescheduling or cutset pipelining/retiming), the spiral-feedback problem may be addressed architecturally by rendering such signal paths as transmittent, nearest-neighbor interconnections. Although this method permits architectural scaling without interconnect-related clock-rate penalty, it will be demonstrated in this paper that excessive delay counts may be incurred when diametric signal paths exist in the projection direction.

To address this problem, this paper introduces a new cylindrical array paradigm, the *ring-planarized cylindrical array* (RPCA). In contrast to the planarization which yields standard 2-D cylindrical arrays, the new method distributes processors from each cylinder row along planar ring structures rather than lines. RPCA structure inherently limits maximum path length to a constant, eliminating array-size dependence. Modular multiplication for cryptographic applications serves as the context in which the RPCA methodology is applied in this paper. Paper organization is as follows. Section 2 provides background on the modular multiplication problem. Properties of standard cylindrical arrays are discussed in section 3, followed by the introduction of the RPCA technique. A comparison of relevant quantities is provided in section 4, followed by conclusions in section 5.

## 2 BACKGROUND: MODULAR MULTIPLICATION

A fundamental constituent of modern cryptography is the public-key class of cryptosystems, which enable secure transmission of information over public channels without requiring exchange of secret parameters between communicating parties. Modular exponentiation is the basis of many such methods including the popular RSA technique [5], and the modular multiplication operation is elemental to modular exponentiation algorithms. Efficient hardware implementations of modular multiplication are therefore essential to many modern cryptography applications.

Given positive integers  $A$ ,  $B$ , and  $N$ , we define the modular multiplication computation as  $AB \bmod N = AB - \lfloor \frac{AB}{N} \rfloor N$ , i.e., determine the remainder of the product of  $A$  and  $B$  with respect to the modulus  $N$ . Large problem sizes in cryptographic applications (e.g. typical word lengths of 1024 bits or greater for RSA) necessitate efficient iterative modular multiplication algorithms, and many are available [6] [7].

Although the architectural techniques to follow in the next section may be applied generally to many of the available modular multiplication algorithms, we will focus attention on an example which may be deemed as typical in many respects. We choose a useful binary LSD-first algorithm first derived in [8] by algebraic manipulation of the Montgomery method [6], wherein the quotient evaluation step is rendered trivial. This algorithm also corresponds to a binary LSD-first form of the general-radix IRA algorithms described in [7]. The algorithm may be specified as:

**Algorithm 1** *Binary IRA Modular Multiplication Algorithm*

Inputs:  $N$ ,  $0 < A = \sum_{i=0}^n a_i 2^i < 2N$  (where  $n = \lceil \log_2 N \rceil$ ),  $0 < B < 2N$ ,  
 $\hat{N} = \frac{1+N}{2} = \lfloor 2^{-1} \rfloor_N$  ( $N$  odd)

Output:  $0 \leq S_{n+1} < 2N$

$S_{-1} = 0$ ,  $a_{n+1} = 0$ , and let  $m_i$  denote  $\lfloor S_{i-1} \rfloor_2$

for  $i = 0$  to  $n + 1$

$$S_i = \frac{S_{i-1} - \lfloor S_{i-1} \rfloor_2}{2} + a_i B + m_i \cdot \hat{N}$$

where  $\lfloor x \rfloor_y$  denotes  $x \bmod y$ ,  $S_{n+1} = \lfloor AB \cdot 2^{-n-2} \rfloor_N + \epsilon N$  and  $\epsilon \in \{0, 1\}$ . Note that the least significant bit of the partial result of the previous iteration,  $S_{i-1}$ , directly selects the modular correction value, which is a member of  $\{0, \hat{N}\}$ . Moreover the first term on the right-hand-side of the expression for  $S_i$  consists of  $S_{i-1}$  truncated by one bit. Finally, note the presence of a weighting factor in the final result related to the total number of iterations executed. This property is common to any LSD-first modular multiplication algorithm, and is addressed by operand prescaling in the manner prescribed by Montgomery [6].

We now rewrite the core of algorithm 1 in terms of bit-wise computations in algorithm 2 below, having the goal of deriving bit-level systolic modular multiplication arrays [9] [10] [11]. Note that within algorithm 2, assuming a single carry would be invalid (i.e., a 4-operand addition cannot be represented by single sum and carry signals). However, assuming two carries of equal weight reveals no contradiction. Furthermore, the computation is cast to reflect carry-ripple rather than carry-save dependencies to avoid redundant representation of the final result,  $S_{n+1}$ . However, to account for a consequential single possible carry at most significant bit positions, an additional  $j$ -loop iteration is added so that the  $S_{i,n+1}$  output may pass this output to iteration  $i + 1$ .

**Algorithm 2** *Bit-wise Modular Multiplication*

$S_{-1,j} = 0$  for all  $j$ ,  $S_{i,n+2} = 0$  for all  $i$ , and  $a_{n+1}, b_{n+1}, \hat{N}_n, \hat{N}_{n+1} = 0$   
 for  $i = 0$  to  $n + 1$

for  $j = 0$  to  $n + 1$

let  $m_i = S_{i-1,0}$

$$S_{i,j} + 2c_{i,j}^{(1)} + 2c_{i,j}^{(2)} = S_{i-1,j+1} + a_i b_j + m_i \hat{N}_j + c_{i,j-1}^{(1)} + c_{i,j-1}^{(2)}$$

Figure 1(a) depicts a dependence graph (DG) based on the above bit-wise algorithm for a very small problem size (i.e.,  $n = 5$ ). Also shown is the cell I/O description and a valid linear schedule corresponding to  $s^T = [1 \ 2]$  (using a  $[j \ i]$  convention). Mapping via a  $[0 \ 1]$  projection results in the linear array in figure 1(b). Such an array achieves 100% utilization when two independent data streams are interleaved. These data sets are distinguished in the figure by bracketed superscripts. A new pair of data sets may be introduced roughly every  $2n$  clock cycles, resulting in throughput proportional to  $\frac{2}{2n} = \frac{1}{n}$ .

An efficient array is also obtained by projecting in the  $[1 \ 0]$  direction, as shown in figure 1(c). One advantage of this projection is single-ported output, i.e., the



output is available serially at the bottom-most cell position. Another advantage was demonstrated in [12], where favorable word-length scalability properties were demonstrated with a shorter length, Montgomery carry-save array. Finally, it can be observed that a  $[1\ 0]$  projected array can accept a single new data set every  $n + 2$  clock cycles, and dependent computations must be separated by at least  $2(n + 2)$  clock cycles. Neglecting initial latency, such an array outputs one result roughly every  $n$  clock cycles, resulting in throughput proportional to  $\frac{1}{n}$ .

### 3 CYLINDRICAL MODULAR MULTIPLICATION ARRAYS

#### 3.1 Standard Cylindrical Arrays and Feedback Pipelining

Having examined two linear systolic arrays for modular multiplication, we now consider the question of how to achieve structures which enable a performance/area trade-off for array sizes in excess of a linear array but smaller than a full 2-D array. Three such approaches were introduced in [4]. The method of present interest involved applying the folding transformation [13] to a full 2-D array in the  $[0\ 1]$  projection direction. Figure 2 depicts a portion of a full 2-D array having delay assignments consistent with the scheduling shown in figure 1(a). In order to obtain an architecture having  $k$  rows (where  $\frac{n+1}{2} \geq k > 1$ ), we fold a possibly extended 2-D array by a factor of  $\lceil \frac{n+1}{k} \rceil$  as displayed in figure 3(a) for  $k = 3$ .

Close examination reveals that such folded arrays are cylindrical in structure, and are homologous to cylindrical arrays proposed for problems such as matrix-matrix multiplication [2] and the algebraic path problem [3]. In the case currently under consideration, such arrays are advantageous in that they can simultaneously interleave  $2k$  independent data streams, with new sets of inputs or outputs arriving roughly every  $2(n + 1) + 1$  clock cycles. Throughput is therefore roughly proportional to  $\frac{k}{n}$  if a fixed clock rate is assumed, a fact which demonstrates the performance scalability available through this design approach. However, the fixed clock rate assumption may not remain valid as  $k$  is increased in interconnect delay dominant environments due to unmitigated feedback paths. This is evident in the small  $k$  factor example of figure 3(a), where two inter-cell traversals are required (from row 3 to 2, and 2 to 1) as opposed to the limit of one such traversal for an array having strictly nearest neighbor communications.

To remedy this problem, an efficient feedback pipelining method [4] may be employed. Applying cutset pipelining in the original 2-D array along horizontal, periodic feed-forward cutsets having period  $k$ , the corresponding folded array will exhibit pipelined feedback paths having an identical pipelining factor. For example, pipelining by one level along the cutsets indicated in figure 2 followed by folding such that  $k = 3$  yields the array in figure 3(b). It is clear that each feedback path now contains at least two delay elements, which corresponds directly to the number of inter-cell traversals. This fact allows the construction of an architecture having strictly nearest neighbor communications as shown in figure 4, where the feedback paths are rendered as pass-through signals in the second cell row. Extension of the



feedback pipelining procedure for larger  $k$  is straightforward and is displayed in the array of figure 3(c). Note that feedback pipelining effectively increases the interleave factor from  $2k$  to  $3k - 2$  in order to obtain full hardware utilization and throughput proportional to  $\frac{k}{n}$ . Pipelining overhead incurred solely from feedback pipelining amounts to roughly  $3kn$ .

Having demonstrated the method for the  $[0\ 1]$  projection direction, we now pursue application of the methodology for the  $[1\ 0]$  projection. Folding of an unmodified full 2-D array in the  $[1\ 0]$  direction with  $k = 3$  results in the array shown in figure 5(a). Attempting to achieve feedback pipelining by the previous temporal transformation strategy proves fruitless, since vertical cutsets within the modular multiplication array are not feed-forward. Instead, all delays within the folded array must be scaled by a factor of two, resulting in the array of figure 5(b). For general  $k$ , all delay elements in the architecture are scaled by a factor  $(k - 1)D$  in order to fully pipeline the feedback paths, as shown in figure 5(c). Observe that this solution is not nearly as efficient as the  $[0\ 1]$  projection case, due to diametric signal paths along the projection direction. Pipelining overhead is substantially greater, amounting to  $9k^2n$ , and displays a quadratic rather than linear dependence on  $k$ . Similarly, the required interleave factor for full hardware utilization and throughput is elevated to  $k(k - 1)$ .

#### 4 Ring-Planarized Cylindrical Arrays

Since significant penalties are associated with feedback pipelining of folded arrays projected in directions having diametric feedback, the solution may be considered untenable – especially for all but the smallest  $k$  values. However, rather than abandoning such projections in this problem and others wherein the above techniques apply, an alternative solution is now derived based on the cylindrical nature of such arrays.

Although a cylindrical array exhibits strictly nearest neighbor communications in its three-dimensional embodiment as depicted conceptually in figure 6(a), non-ideal, spiral feedback paths are introduced when the array is planarized in standard fashion into a practical two-dimensional structure as in figure 6(b). Procedurally, this planarization may be envisioned as unrolling the cylinder structure into the plane, such that processors on each cylinder row are mapped onto a corresponding line.

As seen in the previous subsection, attempts to lessen the impact of feedback path interconnect delay in such architectures through feedback pipelining is inefficient when diametric signal paths exist along the projection direction. However, as it will now be shown, an alternative solution exists which avoids the significant penalties involved with the standard cylindrical array manifestation. The new approach consists of planarizing the three-dimensional cylindrical array in a manner such that processors from each cylinder row are distributed along planar ring structures rather than on lines as in the standard procedure. Figure 6(c) illustrates the resultant two-dimensional structure, which we denote the *ring-planarized cylindrical array* (RPCA). Notice that although more signal paths exceed nearest-neighbor

length in this rudimentary form of the RPCA, all lengths are bounded according to constants rather than exhibiting any dependence on the circumference of the cylinder (i.e.,  $k$  in the previous development). This fact indicates that the new structure may be scaled without encountering additional overhead due to increasing signal path lengths, as will be demonstrated further below.

Utilizing the RPCA paradigm, we now derive modular multiplication arrays for the  $[1\ 0]$  projection direction. Noting that the maximum signal path length amounts to three inter-cell traversals, we pipeline the pre-folded, full 2-D array along horizontal cutsets by two levels, resulting in the RPCA of figure 7(a).

Although this solution is straightforwardly derived from the RPCA definition, it is not optimal for the particular problem under consideration. An alternative which yields less overall pipelining overhead may be derived by observing that the number of delays associated with each vertical dependency (corresponding to  $\{b, N\}$  variable sets) must be identical to the sum of the delays encountered on each associated horizontal and diagonal member (corresponding to  $\{a, m\}$  variable sets and  $S$  variables, respectively). Therefore, vertical paths always contain more delays than diagonals. Exploitation of this property is achieved through counter-clockwise circular shifting by one position of each successive ring as displayed in the modified RPCA of figure 7(b). Although the longest path still occurs on diagonal dependencies, signal assignment has necessarily been altered, i.e., diagonal and vertical paths now represent  $\{b, N\}$  variable sets and  $S$  variables, respectively. Thus, vertical paths may contain fewer delays than diagonals, permitting a solution with less overhead. Namely, imposition of only one level of pipelining (as opposed to two) at horizontal cutsets in the pre-folded 2-D array achieves full pipelining on the longest path.

Figure 8 renders the modified RPCA in a strictly nearest-neighbor communication architectural form. Diagrams of signal propagation for upper and lower cells within the ring structures are displayed, with gray accents indicating pass-through signals. Note an interleave factor of  $k$  achieves full throughput, and new data sets are introduced every  $n + k + 2$  time steps. In the latter figure,  $k$  additional time steps are present so that all  $a$  variables may be fed from the right hand side of the array structure, rather than requiring internal porting. Dependent computations must be separated by  $3(n + k + 2)$  time steps. Finally, note again that such an array may be easily scaled to other  $k$  values (preferably even) without incurring additional overhead.

## 5 COMPARISON

A brief comparison of some distinguishing features of the various array structures is performed in this section. For each architecture, Table 1 displays the total number of required delay elements, the wire density of internal cells stated in terms of inputs, and the number of inter-cell traversals exhibited by the longest signal path in the architecture. As concluded earlier, it is obvious that the  $[1\ 0]$  projected feedback-pipelined standard cylindrical array exhibits a burdensome, quadratically increasing delay count with respect to  $k$ . However, the  $[0\ 1]$  projected counterpart



Array Type	# Delays	Input Wires/Cell (int.)	Longest Path
Std. Cyl. [0 1]	$9k(n+2)$	10	$k-1$
Std. Cyl. [1 0]	$9k(n+2)$	12	$k-1$
Std. F.P. Cyl. [0 1]	$(12k-6)(n+2)$	10	1
Std. F.P. Cyl. [1 0]	$9k(k-1)(n+2)$	12	1
mod. RPCA [1 0]	$12k(n+2)$	10	1

Table 1: Comparison of properties of standard cylindrical arrays with and without feedback pipelining and the modified RPCA architecture

and the modified RPCA in the [1 0] direction both exhibit a relatively minor overhead of approximately 33% over the non-pipelined feedback arrays. Furthermore, we note that the modified RPCA [1 0] achieves the same wire density of 10 input wires per internal cell as the [0 1] projected cylindrical arrays, as compared to 12 for the [1 0] projected counterparts. Wire density is improved in the modified RPCA over the latter arrays since the former avoids feedback of the multiplicity of horizontal dependencies encountered in the modular multiplication problem.

The above comparison demonstrates that the modified RPCA [1 0] architecture is competitive with the standard feedback pipelined [0 1] cylindrical array. This is significant since the design difficulties arising from diametric signals in the projection direction have been overcome, allowing potential advantages of arrays projected in such a manner to be realized. For the modular multiplication problem, such unique advantages include single ported output, simple word length scaling, and easy partitioning (along horizontal, feed-forward cutsets) for flexible multi-chip or block layout implementation.

## 6 CONCLUSIONS

In this paper, a new architectural paradigm has been introduced, the ring-planarized cylindrical array. In contrast to standard cylindrical arrays, RPCAs eliminate spiral feedback paths which can prove problematic in interconnect delay dominant environments. Furthermore, the RPCA technique is clearly superior to feedback-pipelined standard cylindrical arrays when diametric signal dependencies exist in the projection direction. Within the context of modular multiplication, the new technique is significant since it permits architectural scalability beyond linear arrays for the horizontal projection. Such arrays have unique advantages of single-ported output, word-length scalability, and simple partitioning.

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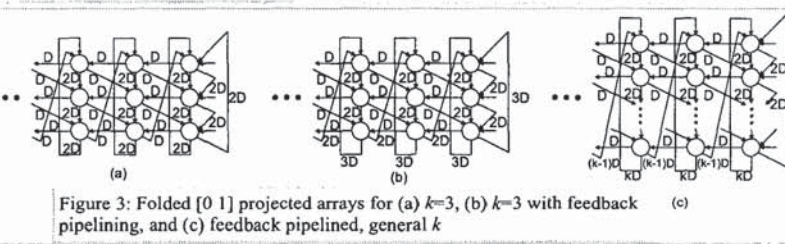
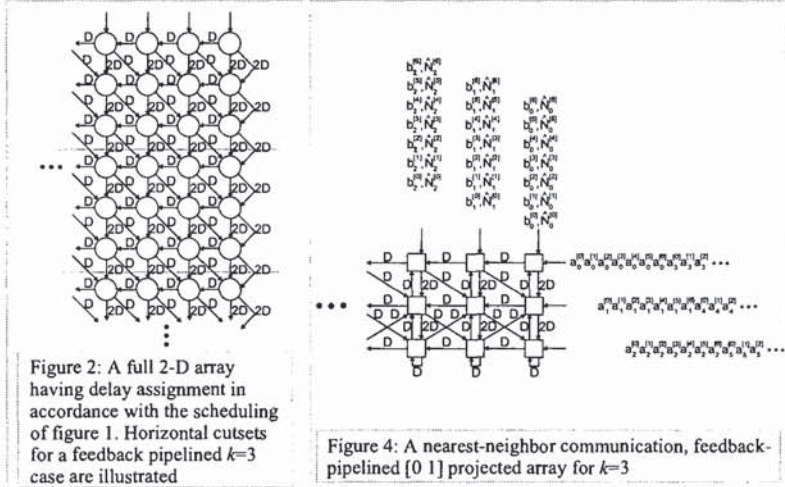
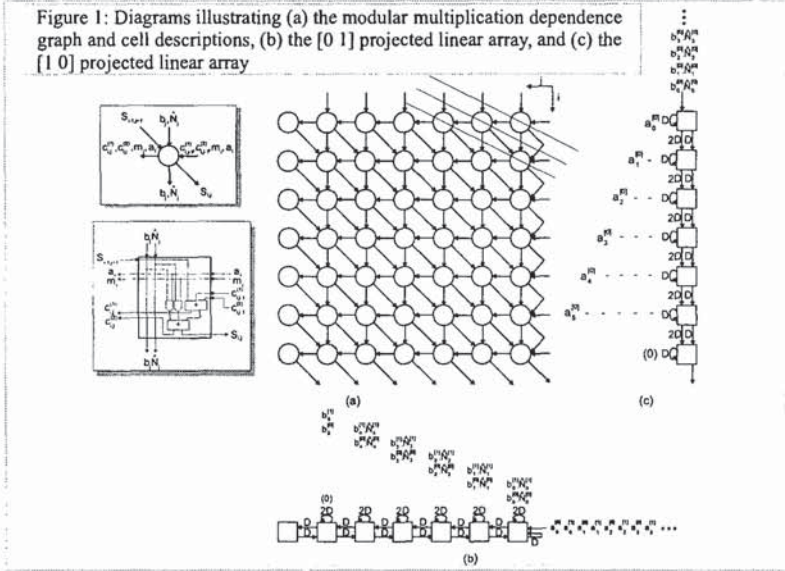


Figure 6: Diagrams depicting (a) three-dimensional cylindrical array, (b) standard planarization, and (c) ring-planarized cylindrical array

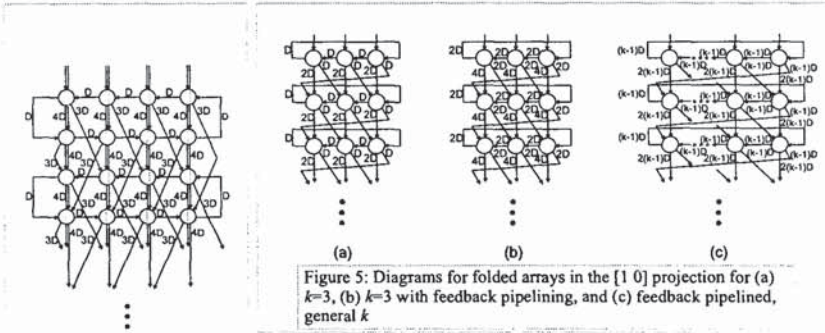
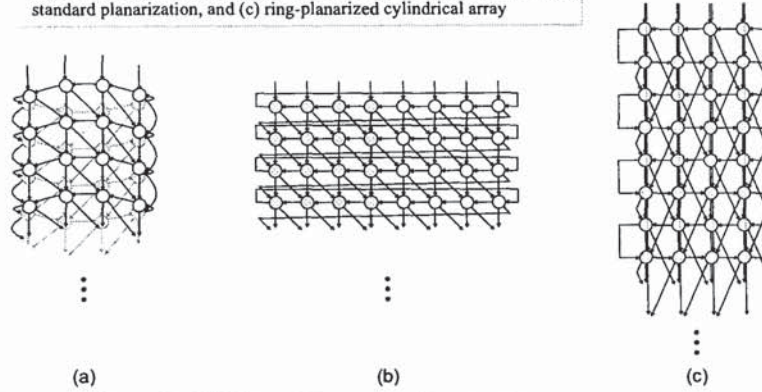


Figure 5: Diagrams for folded arrays in the [1 0] projection for (a)  $k=3$ , (b)  $k=3$  with feedback pipelining, and (c) feedback pipelined, general  $k$

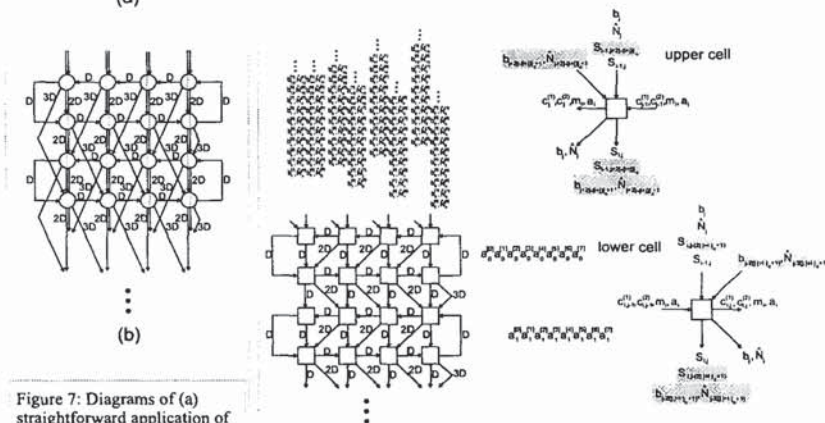


Figure 7: Diagrams of (a) straightforward application of RPCA technique to modular multiplication and (b) successively circularly-shifted RPCA

Figure 8: Illustration of a nearest neighbor communication, modified RPCA array in the [1 0] projection. Gray highlights indicate pass-through signals