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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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First Inventor	Jon M. Huppenthal et al.
Title	MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS
Express Mail Label No.	EV035493558US

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APPLICATION ELEMENTS

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☐ Fee Transmittal Form (submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status. See 37 CFR 1.27
3. ☒ Specification [total pages 34] (preferred Arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) [total sheets 20]
5. ☒ Oath or Declaration [total pages 3]
   a. ☒ UNEXECUTED (original or copy)
   b. ☐ Copy from prior appl. (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 18 completed)
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in prior application, see 37 C.F.R. §§ 1.63(d)(2) and1.33(b).
6. ☐ Application Data Sheet. (See 37 CFR 1.76)
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission (if *applicable, all necessary)*
   a. ☐ Computer Readable Form
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      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers (coversheet/document(s))
10. ☐ 37 CFR. 3.73(b) Statement (*when there is an assignee*) ☐ Power of Attorney
11. ☐ English Translation Document
12. ☐ IDS & Form PTO/SB/08A ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503)
15. ☐ Certified Copy of Priority Document(s)
16. ☐ Nonpublication Request Under 35 USC 122(b)(2)(B)(i).Applicant must attach form PTO/SB/35
17. ☒ Other: Certificate of Mailing

18. **If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:**

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: /

Prior application information: *Examiner:* *Group/Art Unit:*

FOR CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted form the submitted application parts.

19. CORRESPONDENCE ADDRESS

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PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Jon M. Huppenthal and David E. Caliga Serial No. NEW Filed: Herewith	For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

CERTIFICATE OF MAILING BY EXPRESS MAIL

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The undersigned hereby certifies that the following documents:

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2. Utility Patent Application;
3. Unexecuted Declaration for Utility Patent Application;
4. 20 sheets of drawings;
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relating to the above application, were deposited as "Express Mail", Mailing Label No. EV035493558US, with the United States Postal Service, addressed to Box PATENT APPLICATION, The Assistant Commissioner for Patents, Washington, D.C., 20231, 31 October 2002.

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MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

CROSS REFERENCE TO RELATED PATENT APPLICATIONS

The present invention is related to the subject matter of United States Patent Application Ser. No. 09/755,744 filed January 5, 2001 for: "Multiprocessor Computer Architecture Incorporating a Plurality of Memory Algorithm Processors in the Memory Subsystem" and is further related to the subject matter of United States Patent No. 6,454,687 for: "System and Method for Accelerating Web Site Access and Processing Utilizing a Computer System Incorporating Reconfigurable Processors Operating Under a Single Operating System Image", all of which are assigned to SRC Computers, Inc., Colorado Springs, Colorado and the disclosures of which are herein specifically incorporated in their entirety by this reference.

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BACKGROUND OF THE INVENTION

The present invention relates, in general, to the field of computing systems and techniques. More particularly, the present invention relates to multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions.

Currently, most large software applications achieve high performance operation through the use of parallel processing. This technique allows multiple processors to work simultaneously on the same problem to achieve a solution in a fraction of the time required for a single processor to accomplish the same result. The processors in use may be performing many copies of the same operation, or may be performing totally different operations, but in either case all processors are working simultaneously.

The use of such parallel processing has led to the proliferation of both multi-processor boards and large scale clustered systems. However, as more and more performance is required, so is more parallelism, resulting in ever larger systems. Clusters exist today that have tens of thousands of processors and can occupy football fields of space. Systems of such a large physical size present many obvious downsides, including, among other factors, facility requirements, power, heat generation and reliability.

SUMMARY OF THE INVENTION

However, if a processor technology could be employed that offers orders of magnitude more parallelism per processor, these systems could be reduced in size by a comparable factor. Such a processor or processing element is possible through

the use of a reconfigurable processor. Reconfigurable processors instantiate only the functional units needed to solve a particular application, and as a result, have available space to instantiate as many functional units as may be required to solve the problem up to the total capacity of the integrated circuit chips they employ.

At present, reconfigurable processors, such as multi-adaptive processor elements (MAP™, a trademark of SRC Computers, Inc.) can achieve two to three orders of magnitude more parallelism and performance than state-of-the-art microprocessors. Through the advantageous application of adaptive processing techniques as disclosed herein, this type of reconfigurable processing parallelism may be employed in a variety of applications resulting in significantly higher performance than that which can now be achieved while using significantly smaller and less expensive computer systems.

However, in addition to these benefits, there is an additional much less obvious one that can have even greater impact on certain applications and has only become available with the advent of multi-million gate reconfigurable chips. Performance gains are also realized by reconfigurable processors due to the much tighter coupling of the parallel functional units within each chip than can be accomplished in a microprocessor based computing system.

In a multi-processor, microprocessor-based system, each processor is allocated but a relatively small portion of the total problem called a cell. However, to solve the total problem, results of one processor are often required by many adjacent cells because their cells interact at the boundary and

upwards of six or more cells, all having to interact to compute results, would not be uncommon. Consequently, intermediate results must be passed around the system in order to complete the computation of the total problem. This, of necessity, involves numerous other chips and busses that run at much slower speeds than the microprocessor thus resulting in system performance often many orders of magnitude lower than the raw computation time.

On the other hand, in the use of an adaptive processor-based system, since ten to one thousand times more computations can be performed within a single chip, any boundary data that is shared between these functional units need never leave a single integrated circuit chip. Therefore, data moving around the system, and its impact on reducing overall system performance, can also be reduced by two or three orders of magnitude. This will allow both significant improvements in performance in certain applications as well as enabling certain applications to be performed in a practical timeframe that could not previously be accomplished.

Particularly disclosed herein is a method for data processing in a reconfigurable computing system comprising a plurality of functional units. The method comprises: defining a calculation for the reconfigurable computing system; instantiating at least two of the functional units to perform the calculation; utilizing a first of the functional units to operate upon a subsequent data dimension of the calculation and substantially concurrently utilizing a second of the functional units to operate upon a previous data dimension of the calculation.

Further disclosed herein is a method for data processing in a reconfigurable computing system comprising a plurality of functional units. The method comprises: defining a first systolic wall comprising rows of cells forming a subset of the plurality of functional units; computing a value at each of the cells in at least a first row of the first systolic wall; communicating the values between cells in the first row of the cells to produce updated values; communicating the updated values to a second row of the first systolic wall; and substantially concurrently providing the updated values to a first row of a second systolic wall of rows of cells in the subset of the plurality of functional units.

Also disclosed herein is a method for data processing in a reconfigurable processing system which includes setting up a systolic processing form employing a speculative processing strategy.

BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned and other features and objects of the present invention and the manner of attaining them will become more apparent and the invention itself will be best understood by reference to the following description of a preferred embodiment taken in conjunction with the accompanying drawings, wherein:

Fig. 1 is a simplified functional block diagram of typical clustered inter-processor communications path in a conventional multi-processor computing system;

Fig. 2 is a functional block diagram of an adaptive processor communications path illustrating the many functional units ("FU") interconnected by

reconfigurable routing resources within the adaptive processor chip;

Fig. 3A is a graph of the actual performance improvement versus the number of processors utilized and illustrating the deviation from perfect scalability of a particular application utilizing a conventional multi-processor computing system such as that illustrated in Fig. 1;

Fig. 3B is a corresponding graph of the actual performance improvement versus the number of processors utilized and illustrating the performance improvement over a conventional multi-processor computing system utilizing an adaptive processor-based computing system such as that illustrated in Fig. 2;

Fig. 4A is a simplified logic flowchart illustrating a conventional sequential processing operation in which nested Loops A and B are alternately active on different phases of the process;

Fig. 4B is a comparative, simplified logic flowchart illustrating multi-dimensional processing in accordance with the technique of the present invention wherein multiple dimensions of data are processed by both Loops A and B such that the computing system logic is operative on every clock cycle;

Fig. 5A is illustrative of a general process for performing a representative multi-dimensional pipeline operation in the form of a seismic migration imaging function utilizing the parallelism available in the utilization of the adaptive processing techniques of the present invention;

Fig. 5B is a follow-on illustration of the computation phases employed in implementing the exemplary seismic migration imaging function of the preceding figure;

Fig. 6A is a simplified logic flowchart for a particular seismic migration imaging application illustrative of the parallelism provided in the use of an adaptive processor-based computing system;

Fig 6B illustrates the computational process which may be employed by a microprocessor in the execution of the seismic imaging application of the preceding figure;

Fig. 6C illustrates the first step in the computational process which may be employed by an adaptive processor in the execution of the seismic imaging application of Fig. 6A in which a first shot (S1) is started;

Fig. 6D illustrates the second step in the same computational process for the execution of the seismic imaging application of Fig. 6A in which a second shot (S2) is started;

Fig. 6E illustrates the third step in the same computational process for the execution of the seismic imaging application of Fig. 6A in which the operation on the first and second shots is continued through compute;

Fig. 6F illustrates the fourth step in the same computational process showing the subsequent operation on shots S1 and S2;

Fig. 6G illustrates the fifth step in the same computational process followed by the continued downward propagation of shots S1 and S2 over all of the depth slices;

Fig. 7A illustrates a process for performing a representative systolic wavefront operation in the form of a reservoir simulation function also utilizing the parallelism available in the utilization of the

adaptive processing techniques of the present invention;

Fig. 7B illustrates the general computation of fluid flow properties in the reservoir simulation of the preceding figure which are communicated to neighboring cells;

Fig. 7C illustrates the creation of a systolic wall of computation at Time Set 1 which has been started for a vertical wall of cells and in which communication of values between adjacent rows in the vertical wall can occur without storing values to memory;

Fig. 7D is a follow on illustration of the creation of a systolic wall of computation at Time Set 1 and Time Set 2 showing how a second vertical wall of cells is started after the computation for cells in the corresponding row of the first wall has been completed;

Fig. 8A illustrates yet another process for performing a representative systolic wavefront operation in the form of the systolic processing of bioinformatics also utilizing the parallelism available in the utilization of the adaptive processing techniques of the present invention;

Fig. 8B illustrates a systolic wavefront processing operation which further incorporates a speculative processing strategy based upon an evaluation of the rate of change of XB;

Fig. 8C is a further illustration of the systolic wavefront processing operation of the preceding figure incorporating speculative processing;

Fig. 9A illustrates still another process for performing a representative systolic wavefront operation in the form of structure codes calculating

polynomials at grid intersections, again utilizing the parallelism available in the utilization of the adaptive processing techniques of the present invention;

Fig. 9B illustrates the computation start for a vertical wall of grid points at Time Set 1 for a polynomial evaluation performed on grid intersections wherein calculations between rows are done in a stochastic fashion using values from a previous row; and

Fig. 9C is a further illustration of the polynomial evaluation performed on grid intersections of the preceding figure wherein a second wall is started after the cells in the corresponding row of the first wall have been completed.

DESCRIPTION OF A REPRESENTATIVE EMBODIMENT

This application incorporates by reference the entire disclosure of Caliga, D. et al. "Delivering Acceleration: "The Potential for Increased HPC Application Performance Using Reconfigurable Logic", SC2001, November 2001, ACM 1-58113-293-X/01/0011.

With reference now to Fig. 1, a simplified functional block diagram of typical clustered inter-processor communications path in a conventional multi-processor computing system 100 is shown. The computer system comprises a number of memory and input/output ("I/O" controller integrated circuits ("ICs") 102_0 through 102_N, (e.g. "North Bridge") 102 such as the P4X333/P4X400 devices available from VIA Technologies, Inc.; the M1647 device available from Acer Labs, Inc. and the 824430X device available from Intel Corporation. The North Bridge IC 102 is coupled by means of a Front Side Bus ("FSB") to one or more

microprocessors 104_{00} though 104_{03} and 104_{N0} through 104_{N3} such as one of the Pentium® series of processors also available from Intel Corporation.

The North Bridge ICs 102_0 through 102_N are coupled to respective blocks of memory 106_0 through 106_N as well as to a corresponding I/O bridge element 108_0 through 108_N. A network interface card ("NIC") 110_0 through 210_N couples the I/O bus of the respective I/O bridge 108_0 through 108_N to a cluster bus coupled to a common clustering hub (or Ethernet Switch) 112.

Since typically a maximum of four microprocessors 104, each with two or four functional units, can reside on a single Front Side Bus, any communication to more than four must pass over the Front Side Bus, inter-bridge bus, input/output ("I/O") bus, cluster interconnect (e.g. an Ethernet clustering hub 112) and then back again to the receiving processor 104. The I/O bus is typically an order of magnitude lower in bandwidth than the Front Side Bus, which means that any processing involving more than the four processors 104 will be significantly throttled by the loose coupling caused by the interconnect. All of this is eliminated with a reconfigurable processor having hundreds or thousands of functional units per processor.

With reference additionally now to Fig. 2, a functional block diagram of an adaptive processor 200 communications path for implementing the technique of the present invention is shown. The adaptive processor 200 includes an adaptive processor chip 202 incorporates a large number of functional units ("FU") 204 interconnected by reconfigurable routing resources. The adaptive processor chip 202 is coupled to a memory element 206 as well as an interconnect 208

and a number of additional adaptive processor chips 210.

As shown, each adaptive processor chip 202 can contain thousands of functional units 204 dedicated to the particular problem at hand. Interconnect between these functional units is created by reconfigurable routing resources inside each chip 202. As a result, the functional units 204 can share or exchange data at much higher data rates and lower latencies than a standard microprocessor 104 (Fig. 1). In addition, the adaptive processor chips 202 can connect directly to the inter-processor interconnect 208 and do not require the data to be passed through multiple chips in a chipset in order to communicate. This is because the adaptive processor can implement whatever kind of interface is needed to accomplish this connection.

With reference additionally now to Fig. 3A, a graph of the actual performance improvement versus the number of processors utilized in a conventional multi-processor computing system 100 (Fig. 1) is shown. In this figure, the deviation from perfect scalability of a particular application is illustrated for such a system.

With reference additionally now to Fig. 3B, a corresponding graph of the actual performance improvement versus the number of processors utilized in an adaptive processor-based computing system 200 (Fig. 2) is shown. In this figure, the performance improvement provided with an adaptive processor-based computing system 200 over that of a conventional multi-processor computing system 100 is illustrated.

With reference additionally now to Fig. 4A, a simplified logic flowchart is provided illustrating a conventional sequential processing operation 400 in

which nested Loops A (first loop 402) and B (second loop 404) are alternately active on different phases of the process.

As shown, the standard implementation of applications that have a set of nested loops 402,404 is to complete the processing of the first loop 402 before proceeding to the second loop 404. The problem inherent in this approach, particularly when utilized in conjunction with field programmable gate arrays ("FPGAs") is that all of the logic that has been instantiated is not being completely utilized.

With reference additionally now to Fig. 4B, a comparative, simplified logic flowchart is shown illustrating a multi-dimensional process 410 in accordance with the technique of the present invention. The multi-dimensional process 410 is effectuated such that multiple dimensions of data are processed by both Loops A (first loop 412) and B (second loop 414) such that the computing system logic is operative on every clock cycle.

In contrast to the sequential processing operation 400 (Fig. 4A) the solution to the problem of most effectively utilizing available resources is to have an application evaluate a problem in a data flow sense. That is, it will "pass" a subsequent dimension of a given problem through the first loop 412 of logic concurrently with the previous dimension of data being processed through the second loop 414. In practice, a "dimension" of data can be: multiple vectors of a problem, multiple planes of a problem, multiple time steps in a problem and so forth.

With reference additionally now to Fig. 5A, a general process for performing a representative multi-dimensional pipeline operation is shown in the form of

a seismic migration imaging function 500. The process 500 can be adapted to utilize the parallelism available in the utilization of the adaptive processing techniques of the present invention in the form of a multi-adaptive processor (MAP™, a trademark of SRC Computers, Inc., assignee of the present invention) STEP3d routine 502. The MAP STEP3d routine 502 is operation to utilize velocity data 504, source data 506 and receiver data 508 to produce a resultant image 510 as will be more fully described hereinafter.

With reference additionally now to Fig. 5B, the MAP STEP3d routine 502 of the preceding figure is shown in the various computational phases of: MAPTRI_x 520, MAPTRI_y 522, MAPTRI_d+ 524 and MAPTRI_d- 526.

With reference additionally now to Fig. 6A, a simplified logic flowchart for a particular seismic migration imaging application 600 is shown. The seismic migration imaging application 600 is illustrative of the parallelism provided in the use of an adaptive processor-based computing system 200 such as that shown in Fig. 2. The representative application 600 demonstrates a nested loop parallelism in the tri-diagonal solver and the same logic can be implemented for the multiple tri-diagonal solvers in the x, y, d+ and d- directions. The computational phases of: MAPTRI_x 520, MAPTRI_y 522, MAPTRI_d+ 524 and MAPTRI_d- 526 are again illustrated.

With reference additionally now to Fig. 6B, a computational process 610 is shown which may be employed by a microprocessor ("mP") in the execution of the seismic imaging application 600 of the preceding figure. The process 610 includes the step 612 of reading the source field [$S(Z_0)$] and receiver field [$R(Z_0)$] as well as the velocity field [$V(Z_0)$] at

step 614. At step 616 values are computed for $S(Z_{nz}), R(Z_{nz})$ which step is followed by the phases MAPTRI_x 520 and MAPTRI_y 522. At step 618, the image of $Z_{1/2}$ is computed. This is followed by the phases MAPTRI_d+ 524 and MAPTRI_d- 526 to produce the resultant image Z at step 620. The process 610 loops over the depth slices as indicated by reference number 622 and loops over the shots as indicated by reference number 624.

With reference additionally now to Fig. 6C, the first step in a computational process 650 in accordance with the technique of the present invention is shown in which a first shot (S1) is started. The process 650 may be employed by an adaptive processor (e.g. a MAP™ adaptive processor) as disclosed herein in the execution of the seismic imaging application 600 of Fig. 6A. As indicated by the shaded block, the phase MAPTRI_x 520 is active.

With reference additionally now to Fig. 6D, the second step in the computational process 650 is shown at a point at which a second shot (S2) is started. Again, as indicated by the shaded blocks, the phase MAPTRI_x 520 is active for S2, the phase MAPTRI_y 522 is active for S1 and image $Z_{1/2}$ has been produced at step 618. As shown, adaptive processors in accordance with the disclosure of the present invention support computation pipelining in multiple dimensions and the parallelism in Z and shots is shown at step 612.

With reference additionally now to Fig. 6E, the third step in the computational process 650 is shown in which the operation on the first and second shots is continued through compute. As indicated by the shaded blocks, the phase MAPTRI_d+ 524 is active for

S1, the phase MAPTRI_y 522 is active for S2 and image $Z_{1/2}$ has been produced at step 618.

With reference additionally now to Fig. 6F, the fourth step in the computational process 650 is shown illustrating the subsequent operation on shots S1 and S2. The phase MAPTRI_d+ 524 is active for S2, the phase MAPTRI_d- 526 is active for S1 and image Z has been produced at step 620.

With reference additionally now to Fig. 6G, the fifth step in the computational process 650 is shown as followed by the continued downward propagation of shots S1 and S2 over all of the depth slices. The phase MAPTRI_x 520 is active for S1, the phase MAPTRI_d- 526 is active for S2 and image Z has been produced at step 620.

With reference additionally now to Fig. 7A, a process 700 for performing a representative systolic wavefront operation in the form of a reservoir simulation function is shown which utilizes the parallelism available in the adaptive processing techniques of the present invention. The process 700 includes a "k" loop 702, "j" loop 704 and "i" loop 706 as shown.

With reference additionally now to Fig. 7B, the general computation of fluid flow properties in the reservoir simulation process 700 of the preceding figure are illustrated as values are communicated between a group of neighboring cells 710. The group of neighboring cells 710 comprises, in the simplified illustration shown, first, second and third walls of cells 712, 714 and 716 respectively. Each of the walls of cells includes a corresponding number of first, second, third and fourth rows 718, 720, 722 and 724 respectively.

As shown, the computation of fluid flow properties are communicated to neighboring cells 710 and, importantly, this computation can be scheduled to eliminate the need for data storage. In accordance with the technique of the present invention, a set of cells can reside in an adaptive processor and the pipeline of computation can extend across multiple adaptive processors. Communication overhead between multiple adaptive processors may be advantageously minimized through the use of MAP™ adaptive processor chain ports as disclosed in U.S. Patent No. 6,339,819 issued on January 15, 2002 for: "Multiprocessor With Each Processor Element Accessing Operands in Loaded Input Buffer and Forwarding Results to FIFO Output Buffer", assigned to SRC Computers, Inc., assignee of the present invention, the disclosure of which is herein specifically incorporated by this reference.

With reference additionally now to Fig. 7C, the creation of a systolic wall 712 of computation at Time Set 1 is shown. The systolic wall 712 has been started for a vertical wall of cells and communication of values between adjacent rows 718 through 724 in the vertical wall can occur without storing values to memory.

With reference additionally now to Fig. 7D, a follow on illustration of the creation of a systolic wall 712 of computation at Time Set 1 and a second systolic wall 714 at Time Set 2 is shown. In operation, a second vertical wall of cells is started after the computation for cells in the corresponding row of the first wall has been completed. Thus, for example, at time t_0, the first row 718 of systolic wall 712 is completed and the results passed to the first row 718 of the second systolic wall 714. At

time t_1, the second row 720 of the first systolic wall 712 and the first row 718 of the second systolic wall 714 are computed. Thereafter, at time t_2, the third row 722 of the first systolic wall 712 and the second row 720 of the second systolic wall 714 are computed. The process continues in this manner for all rows and all walls.

With reference additionally now to Fig. 8A, yet another process 800 for performing a representative systolic wavefront operation is shown. The process 800 is in the form of the systolic processing of bioinformatics and also utilizes the parallelism available in the adaptive processing techniques of the present invention. As shown, systolic processing in the process 800 can pass previously computed data down within a column (e.g. one of columns 802, 804 and 806) as to subsequent columns as well (e.g. from column 802 to 804; from column 804 to 806 etc.) The computational advantage provided is the processing of the second column 804 can begin after only a few clock cycles following the start of the processing of the first column 802 to compute the first "match" state.

With reference additionally now to Fig. 8B, a systolic wavefront processing operation 810 is shown. The processing operation 810, comprising "i" loop 812 and "k" loop 814 now further incorporates a speculative processing strategy based upon an evaluation of the rate of change of XB.

A straightforward systolic processing operation could be used for performing the operation 810 but for the problem inherent in the computation of XB as its value XB[i] 816 can not be known until the completion of the entire "k" loop 814. After evaluating the rate of change of XB, it was determined that a speculative

processing strategy could be used for the problem. A normal systolic form is set up and the value of XB is held constant for the set of columns computed in the systolic set. At the bottom of each column, the value of XB[i] 816 is then computed.

With reference additionally now to Fig. 8C, a further illustration of the systolic wavefront processing operation 810 incorporating speculative processing of the preceding figure is shown. The speculative processing includes "j" columns 818_0 through 818_j as shown. Each of the columns 818 assumes that XB[i+j] has a constant value. A test is conducted at the bottom of each of the columns 818 to determine with the XB value changes as indicated at steps 820_1 through 820_j. If the value of XB changes at the i+n column, the process is then restarted at that column 818. Since the rate of change of XB is relatively slow, the "cost" of the compute operation can be greatly reduced.

With reference additionally now to Fig. 9A, another process 900 for performing a representative systolic wavefront operation is shown in the form of structure codes calculating polynomials at grid intersections 902. The process 900 advantageously utilizes the parallelism available in the adaptive processing techniques of the present invention.

With reference additionally now to Figs. 9B and 9C, the computation start for a vertical wall 910 of grid points at Time Set 1 is shown for a polynomial evaluation performed on grid intersections 902 (Fig. 9A) wherein calculations between rows 912, 914, 016 and 918 are done in a stochastic fashion using values from a previous row. As shown, a polynomial evaluation is performed on the grid intersections 902

such that a second wall 910_1 is started after the cells in the corresponding row of the first wall 910_0 have been completed.

As can be determined from the foregoing, the multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions disclosed herein can be employed in a myriad of applications including multi-dimensional pipeline computations for seismic applications, search algorithms, information security, chemical and biological applications, filtering and the like as well as for systolic wavefront computations for fluid flow and structures analysis, bioinformatics etc. Some applications may also employ both the multi-dimensional pipeline and systolic wavefront methodologies.

Following are representative applications of the techniques for adaptive processor based computation disclosed herein:

Imaging

Seismic: These applications, typically used in the oil and gas exploration industries, process echo data to produce detailed analysis of subsurface features. The applications use data collected at numerous points and consisting of many repeated parameters. Due to this, these programs are ideal candidates to take advantage of parallel computing. In addition, because the results of the computation on one data point are used in the computation of the next, these programs will particularly benefit from the tight parallelism that can be found in the use of adaptive or reconfigurable processors.

Synthetic Aperture Radar ("SAR"): These applications are typically used in geographical

imaging. The applications use data collected in swaths. Processing consists of repeated operations on data that has been sectioned in cells. These programs are also ideal candidates to take advantage of parallel computing and in particular to benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

JPEG Image compression: These applications partition an image into numerous blocks. These blocks then have a set of operations performed on them. The operations can be parallelized across numerous blocks. The combination of the set of operations and the parallelism will particularly benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

MPEG Image compression: These applications partition a frame into numerous blocks. These blocks then have a set of operations performed on them. The operations can be parallelized across numerous blocks. In addition, there are numerous operations that are performed on adjacent frames. The combination of the set of operations and the parallelism will particularly benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Fluid flow

Reservoir Simulation: These applications, also typically used in the oil and gas production industries, process fluid flow data in the oil and gas subsurface reservoirs to produce extraction models. The application will define a three dimensional ("3d") set of cells that contain the oil and gas reservoir. These programs are ideal candidates to take advantage of parallel or adaptive computing because there are repeated operations on each cell. In addition,

information computed for each cell is then passed to neighboring cells. These programs will particularly benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Weather prediction: Such an application will partition the forecast area into logical grid cells. The computational algorithms will then perform calculations that have polynomials that have nodes associated with the grid cells. These programs are ideal candidates to take advantage of adaptive or parallel computing because there are repeated operations on each cell associated with the set of times computed in the forecast.

Automotive: These applications investigate the aerodynamics of automobile or other aerodynamic structures. The application generally divides the space surrounding the automobile structure into logical cells that are associated with nodes in computational polynomials. These programs are ideal candidates to take advantage of adaptive or parallel computing because there are repeated operations on each cell associated with the set of wind velocities computed in the forecast. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Aerospace: These applications investigate the aerodynamics of aerospace/airplane structures. The application divides the space surrounding the aerospace/airplane structure into logical cells that are associated with nodes in computational polynomials. These programs are ideal candidates to take advantage of parallel computing because there are repeated operations on each cell associated with the set of wind velocities computed in the forecast.

These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Plastic Injection Molding: These applications investigate the molding parameters of injecting liquid plastic into molds. The application divides the space inside the mold into logical cells that are also associated with nodes in computational polynomials. These programs are ideal candidates to take advantage of parallel computing because there are repeated operations on each cell associated with the set of injection parameters. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Structures

Crash Analysis: These applications are typically used in the automotive or aviation industry. The application will partition the entire automobile into components. These components are then subdivided into cells. The application will analyze the effect of a collision on the structure of the automobile. These programs are ideal candidates for parallel computing because there are repeated operations on each cell and they receive computed information from their neighboring cells. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Structural Analysis: These applications investigate the properties of structural integrity. The application divides the structure into logical cells that are associated with nodes in computational polynomials. These programs are ideal candidates to take advantage of parallel computing because there are repeated operations on each cell associated with load

and stress. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Search algorithms

Image searches: These applications are typically used in the security industry for fingerprint matching, facial recognition and the like. The application seeks matches in either a collection of subsets of the total image or the total image itself. The process compares pixels of the model to pixels of a record from an image database. These programs are ideal candidates for parallel computing because of the correlation of comparison results that exist for each pixel in the subsets or entire image. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Data mining: These applications are typically used in commercial market spaces. The application seeks matches in a set of search information (e.g. character strings) in each record in a database. The application then produces a match correlation for all data records. A match correlation is produced from the comparison results for each set of search information with all characters in a database record. These programs are ideal candidates for parallel computing because of the repeated comparison operations that exist all character comparisons of the set of search information with each character in the database record. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Finance

Financial modeling: The application creates numerous strategies for each decision step in the modeling process. The results of a computational step are feed into another set of strategies for subsequence modeling steps. These programs are ideal candidates to take advantage of parallel computing because there are repeated operations on each strategy within a modeling step. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Information Security

Encryption/Decryption: The application applies an algorithm that converts the original data into an encrypted, or "protected", form. The process is applied to each set of N bits in the original data. Decryption reverses the process to deliver the original data. These programs are ideal candidates for parallel computing because there are repeated operations on each N bits of data. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Chemistry/Biology

Genetic pattern matching: These applications are typically used in the bioinformatics industry. The application looks for matches of a particular genetic sequence (or model) to a database of genetic records. The application compares each character in the model to the characters in genetic record. These programs are ideal candidates for parallel computing because of the repeated comparison operations that exist for all character comparisons of the model with each character in the genetic record. These programs will benefit

from the tight parallelism that can be found in adaptive or reconfigurable processors.

Protein Folding: These applications are typically used by pharmaceutical companies. The application investigates the dynamics of the deformation of the protein structure. The application uses a set of equations which are recomputed at various "time" intervals to model the protein folding. These programs are ideal candidates for parallel computing because of the repeated computations on a large set of time intervals in the modeling sequence. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors

Organic structure interaction: These applications are typically used by chemical and drug companies. The application investigates the dynamics of organic structures as they are interacting. The application uses a set of equations which are recomputed at various "time" intervals to model how the organic structure interact. These programs are ideal candidates for parallel computing because of the repeated computations on a large set of time intervals in the modeling sequence. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors

Signals

Filtering: Applications often utilize filtering techniques to "clean-up" a recorded data sequence. This technique is utilized in a wide variety of industries. The application generally applies a set of filter coefficients to each data point in the recorded sequence. These programs are ideal candidates for parallel computing because of the repeated computations to all data points in the

sequence and all sequences. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

While there have been described above the principles of the present invention in conjunction with specific, exemplary applications for the use of adaptive processor-based systems in the implementation of multi-dimensional pipeline and systolic wavefront computations, it is to be clearly understood that the foregoing descriptions are made only by way of example and not as a limitation to the scope of the invention. Particularly, it is recognized that the teachings of the foregoing disclosure will suggest other modifications to those persons skilled in the relevant art. Such modifications may involve other features which are already known per se and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure herein also includes any novel feature or any novel combination of features disclosed either explicitly or implicitly or any generalization or modification thereof which would be apparent to persons skilled in the relevant art, whether or not such relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as confronted by the present invention. The applicants hereby reserve the right to formulate new claims to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

What is claimed is:

CLAIMS:

1. A method for data processing in a reconfigurable computing system comprising a plurality of functional units, said method comprising:

defining a calculation for said reconfigurable computing system;

instantiating at least two of said functional units to perform said calculation;

utilizing a first of said functional units to operate upon a subsequent data dimension of said calculation; and

substantially concurrently utilizing a second of said functional units to operate upon a previous data dimension of said calculation.

2. The method of claim 1 wherein said subsequent and previous data dimensions of said calculation comprise multiple vectors in said calculation.

3. The method of claim 1 wherein said subsequent and previous data dimensions of said calculation comprise multiple planes in said calculation.

4. The method of claim 1 wherein said subsequent and previous data dimensions of said calculation comprise multiple time steps in said calculation.

5. The method of claim 1 wherein said subsequent an previous data dimensions of said calculation comprise multiple grid points in said calculation.

6. The method of claim 1 wherein said calculation comprises a seismic imaging calculation.

7. The method of claim 1 wherein said calculation comprises a synthetic aperture radar imaging calculation.

8. The method of claim 1 wherein said calculation comprises a JPEG image compression calculation.

9. The method of claim 1 wherein said calculation comprises an MPEG image compression calculation.

10. The method of claim 1 wherein said calculation comprises a fluid flow calculation for a reservoir simulation.

11. The method of claim 1 wherein said calculation comprises a fluid flow calculation for weather prediction.

12. The method of claim 1 wherein said calculation comprises a fluid flow calculation for automotive applications.

13. The method of claim 1 wherein said calculation comprises a fluid flow calculation for aerospace applications.

14. The method of claim 1 wherein said calculation comprises a fluid flow calculation for an injection molding application.

15. The method of claim 1 wherein said calculation comprises a structures calculation for crash analysis.

16. The method of claim 1 wherein said calculation is comprises a structures calculation for structural analysis.

17. The method of claim 1 wherein said calculation comprises a search algorithm for an image search.

18. The method of claim 1 wherein said calculation comprises a search algorithm for data mining.

19. The method of claim 1 wherein said calculation comprises a financial modeling application.

20. The method of claim 1 wherein said calculation comprises an encryption algorithm.

21. The method of claim 1 wherein said calculation comprises an decryption algorithm.

22. The method of claim 1 wherein said calculation comprises a genetic pattern matching function.

23. The method of claim 1 wherein said calculation comprises a protein folding function.

24. The method of claim 1 wherein said calculation comprises an organic structure interaction function.

25. The method of claim 1 wherein said calculation comprises a signal filtering application.

26. A method for data processing in a reconfigurable computing system comprising a plurality of functional units, said method comprising:

defining a first systolic wall comprising rows of cells forming a subset of said plurality of functional units;

computing a value at each of said cells in at least a first row of said first systolic wall;

communicating said values between cells in said first row of said cells to produce updated values;

communicating said updated values to a second row of said first systolic wall; and

substantially concurrently providing said updated values to a first row of a second systolic wall of rows of cells in said subset of said plurality of functional units.

27. The method of claim 26 wherein said values correspond to vectors in a computation.

28. The method of claim 26 wherein said values correspond to planes in a computation.

29. The method of claim 26 wherein said values correspond to time steps in a computation.

30. The method of claim 26 wherein said values correspond to grid points in a computation.

31. The method of claim 26 wherein said step of communicating said updated values to a second row of said first systolic wall is carried out without storing said updated values in an extrinsic memory.

32. The method of claim 26 wherein said values correspond to a seismic imaging calculation.

33. The method of claim 26 wherein said values correspond to a synthetic aperture radar imaging calculation.

34. The method of claim 26 wherein said values correspond to a JPEG image compression calculation.

35. The method of claim 26 wherein said values correspond to an MPEG image compression calculation.

36. The method of claim 26 wherein said values correspond to a fluid flow calculation for a reservoir simulation.

37. The method of claim 26 wherein said values correspond to a fluid flow calculation for weather prediction.

38. The method of claim 26 wherein said values correspond to a fluid flow calculation for automotive applications.

39. The method of claim 26 wherein said values correspond to a fluid flow calculation for aerospace applications.

40. The method of claim 26 wherein said values correspond to a fluid flow calculation for an injection molding application.

41. The method of claim 26 wherein said values correspond to a structures calculation for crash analysis.

42. The method of claim 26 wherein said values correspond to a structures calculation for structural analysis.

43. The method of claim 26 wherein said values correspond to a search algorithm for an image search.

44. The method of claim 26 wherein said values correspond to a search algorithm for data mining.

45. The method of claim 26 wherein said values correspond to a financial modeling application.

46. The method of claim 26 wherein said values correspond to an encryption algorithm.

47. The method of claim 26 wherein said values correspond to an decryption algorithm.

48. The method of claim 26 wherein said values correspond to a genetic pattern matching function.

49. The method of claim 26 wherein said values correspond to a protein folding function.

50. The method of claim 26 wherein said values correspond to an organic structure interaction function.

51. The method of claim 26 wherein said values correspond to a signal filtering application.

52. The method of claim 26 wherein said reconfigurable computing system comprises at least one adaptive processor.

53. The method of claim 52 wherein said reconfigurable computing system further comprises at least one microprocessor.

54. A method for data processing in a reconfigurable computing system comprising a plurality of functional units, said method comprising:

performing a calculation by a subset of said plurality of functional units to produce computed data;

passing said computed data from a first column of said calculation to a next column in said calculation;

evaluating a rate of change in at least one variable for each of said columns in said calculation;

continuing said calculation if said variable does not change for a particular column of said calculation; and

restarting said calculation at said column of said calculation where said variable does change.

55. A method for data processing in a reconfigurable computing system comprising:

performing systolic processing on a calculation do be executed by said reconfigurable computing system; and

further performing speculative processing on said calculation by said reconfigurable computing system.

ABSTRACT OF THE DISCLOSURE

Multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions are disclosed which can be employed in a myriad of applications including multi-dimensional pipeline computations for seismic applications, search algorithms, information security, chemical and biological applications, filtering and the like as well as for systolic wavefront computations for fluid flow and structures analysis, bioinformatics etc. Some applications may also employ both the multi-dimensional pipeline and systolic wavefront methodologies disclosed.

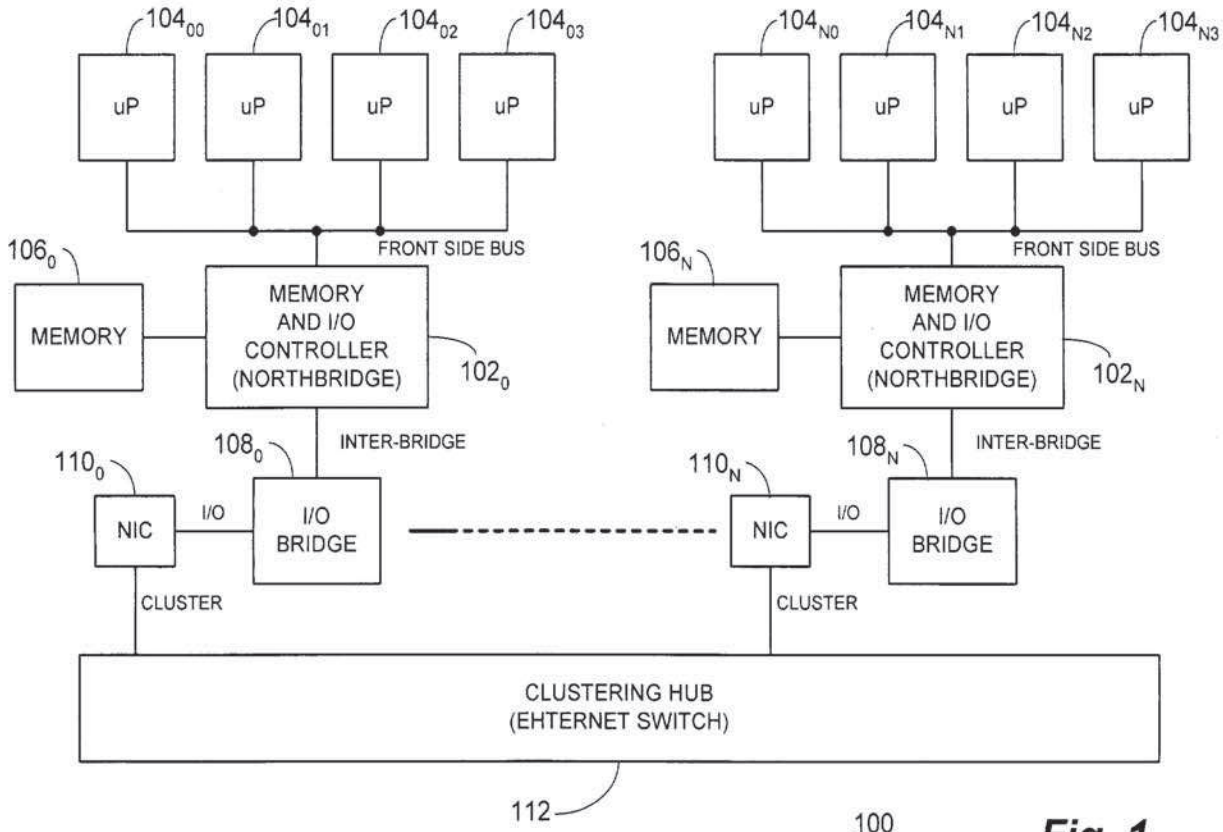


Fig. 1
Prior Art

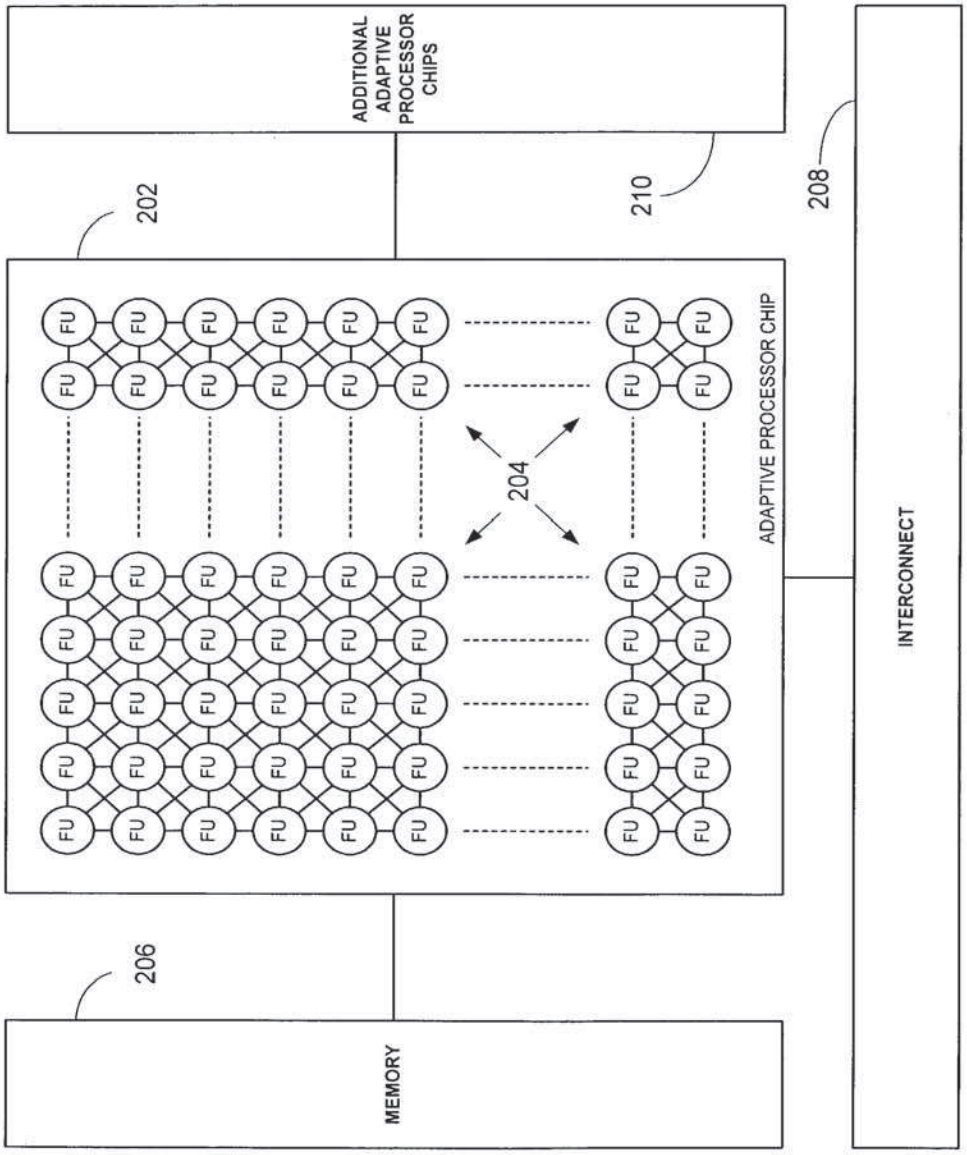

ADDITIONAL ADAPTIVE PROCESSOR CHIPS
210
208
202
ADAPTIVE PROCESSOR CHIP
FU
204
INTERCONNECT
206
MEMORY

Fig. 2

200

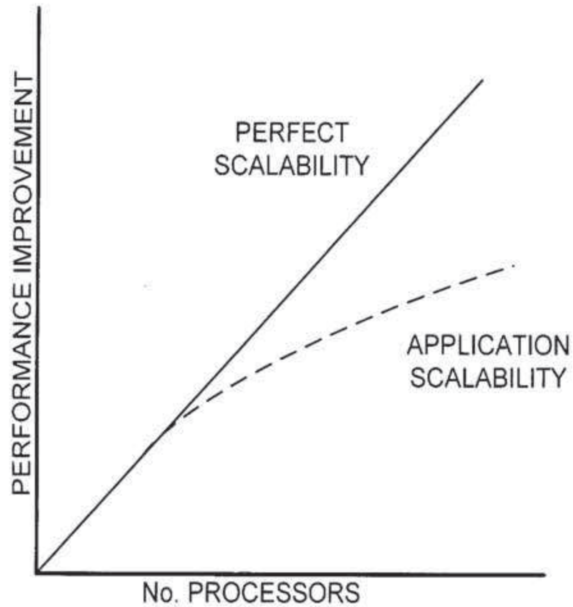


Fig. 3A
PRIOR ART

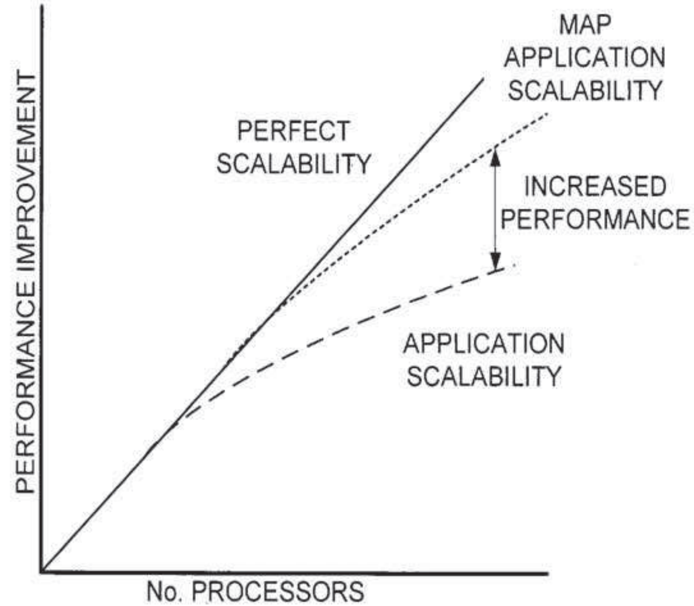


Fig. 3B

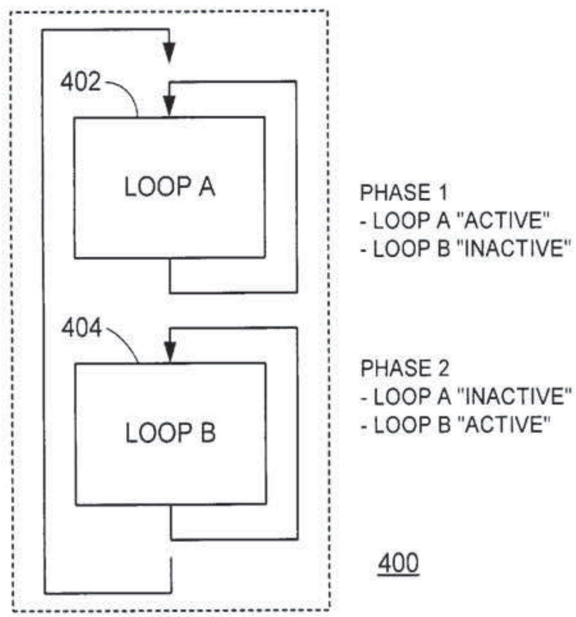


Fig. 4A
Prior Art

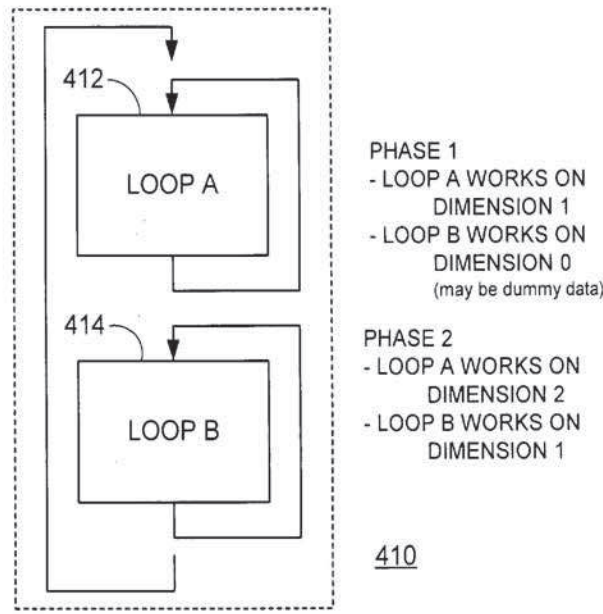


Fig. 4B

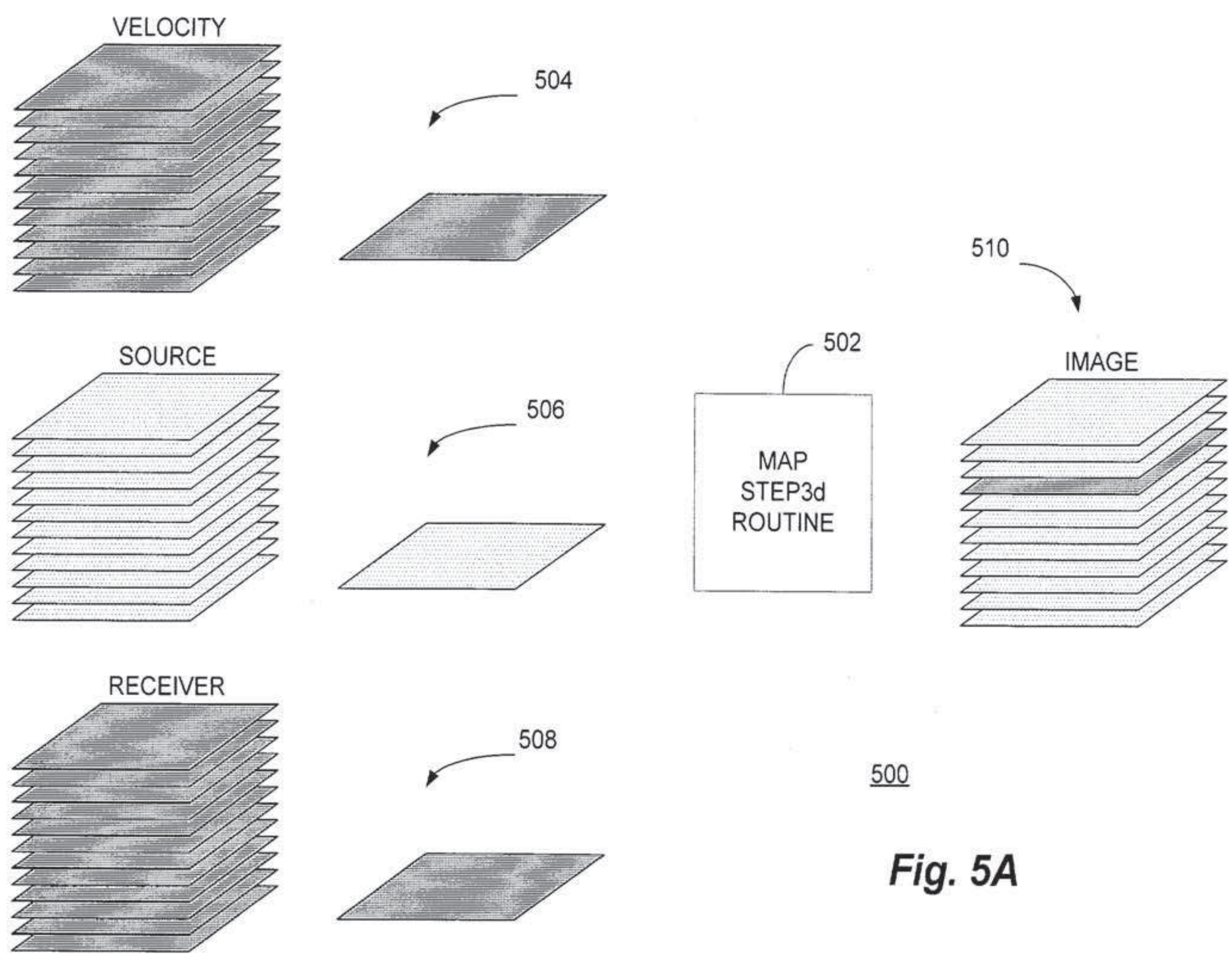

VELOCITY
504
SOURCE
506
RECEIVER
508
502
MAP
STEP3d
ROUTINE
510
IMAGE
500

Fig. 5A

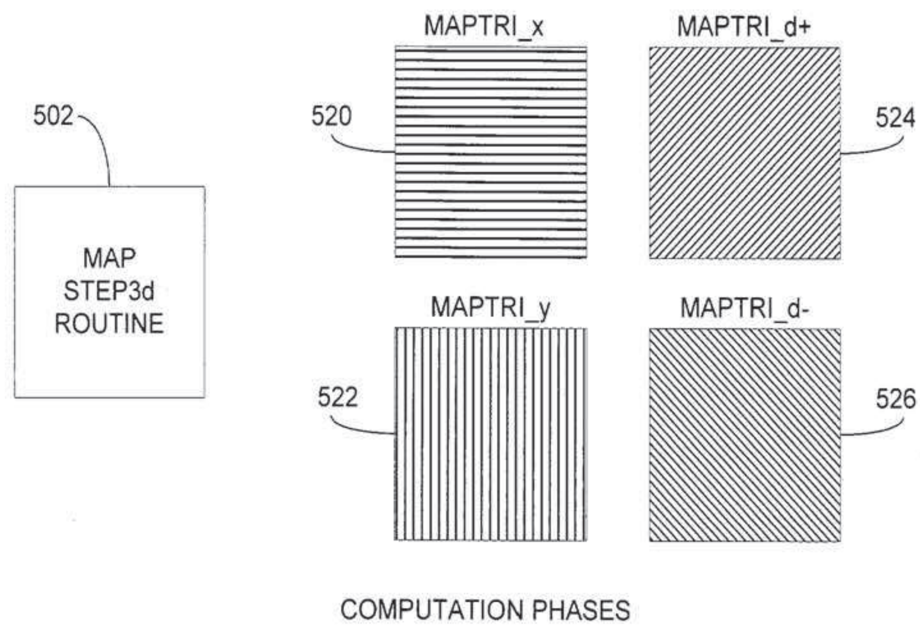

502
MAP
STEP3d
ROUTINE
MAPTRI_x
520
MAPTRI_d+
524
MAPTRI_y
522
MAPTRI_d-
526
COMPUTATION PHASES

Fig. 5B

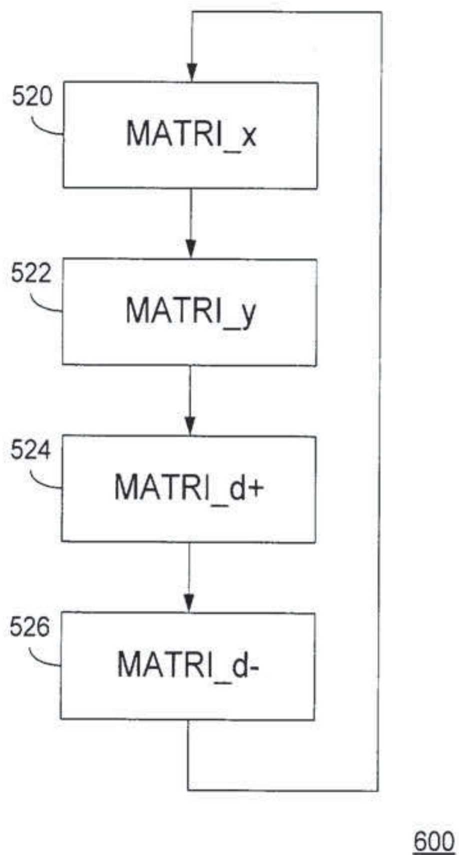

520
MATRI_x
522
MATRI_y
524
MATRI_d+
526
MATRI_d-
600

Fig. 6A

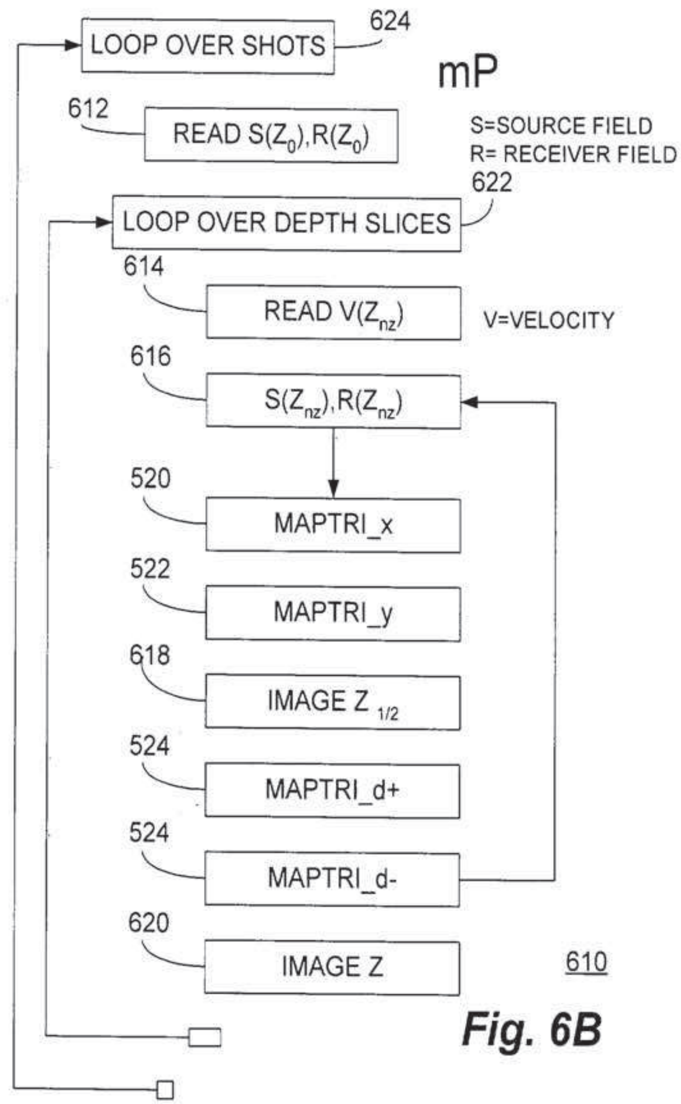

LOOP OVER SHOTS
624
mP
612
READ S(Z0),R(Z0)
S=SOURCE FIELD
R= RECEIVER FIELD
622
LOOP OVER DEPTH SLICES
614
READ V(Znz)
V=VELOCITY
616
S(Znz),R(Znz)
520
MAPTRI_x
522
MAPTRI_y
618
IMAGE Z 1/2
524
MAPTRI_d+
524
MAPTRI_d-
620
IMAGE Z
610

Fig. 6B

MAP STEP 1

START SHOT 1 (S1)

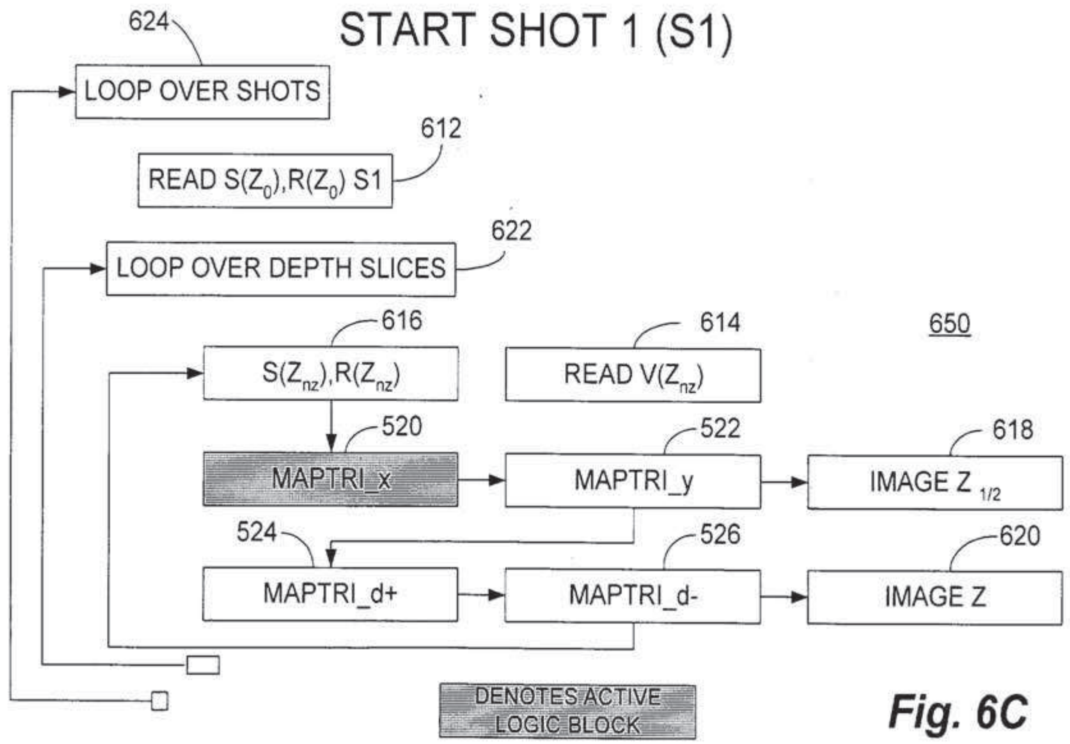


Fig. 6C

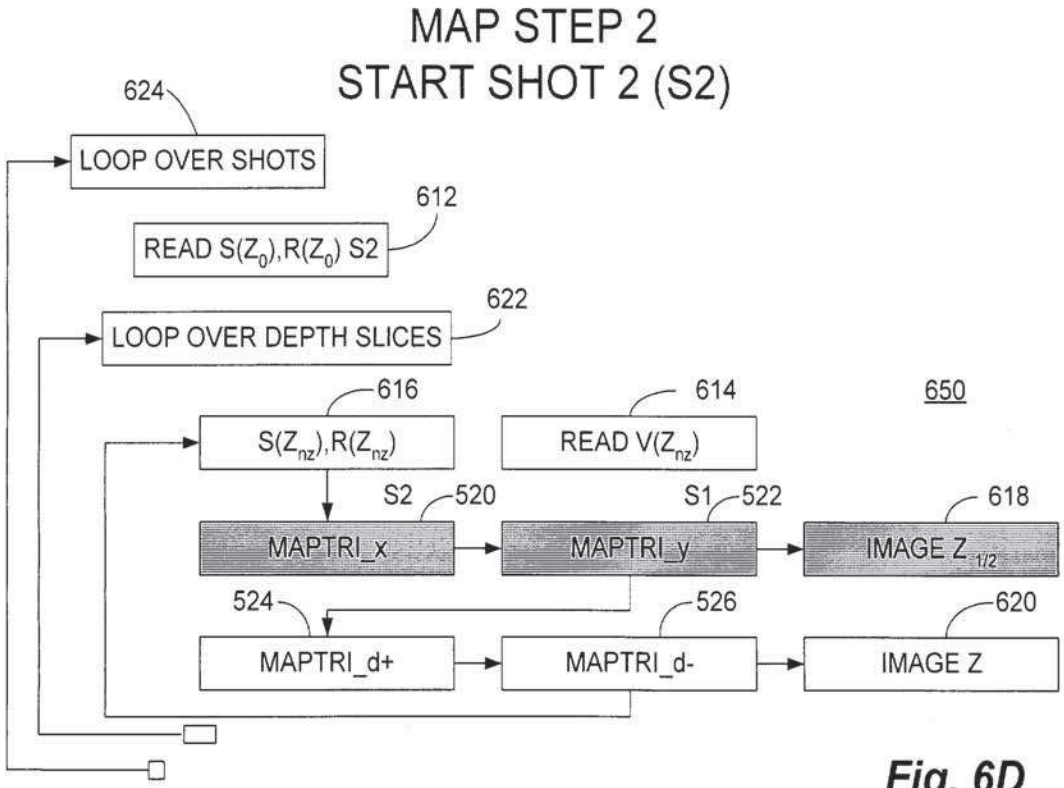


Fig. 6D

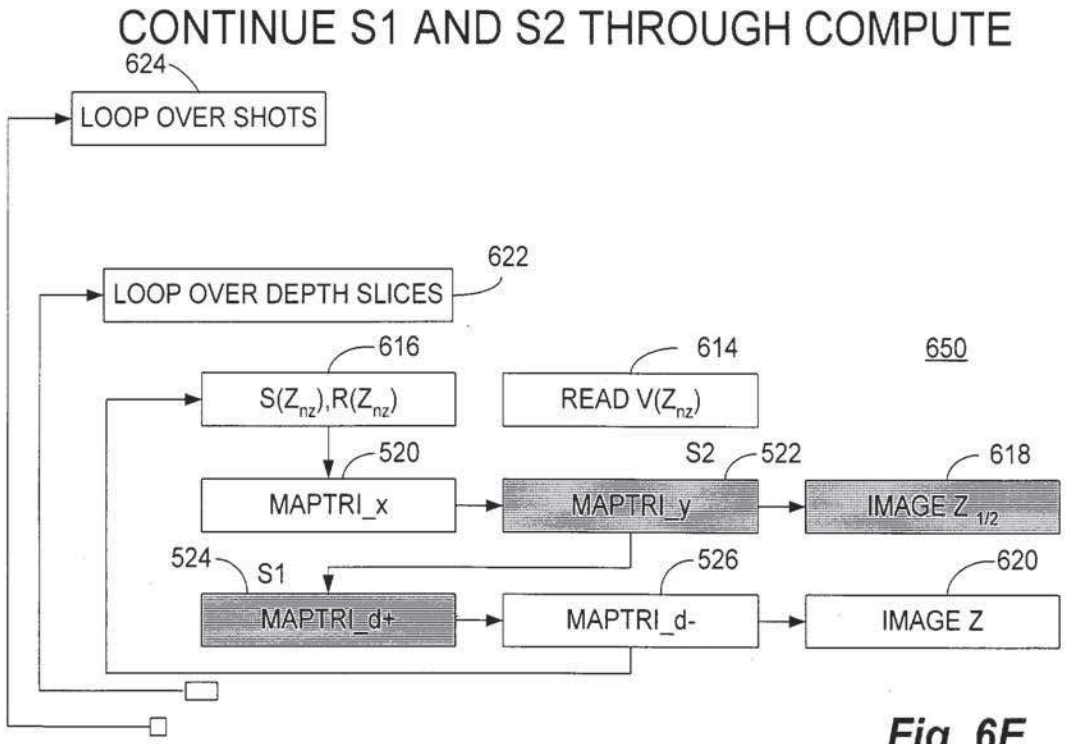


Fig. 6E

STEP 4

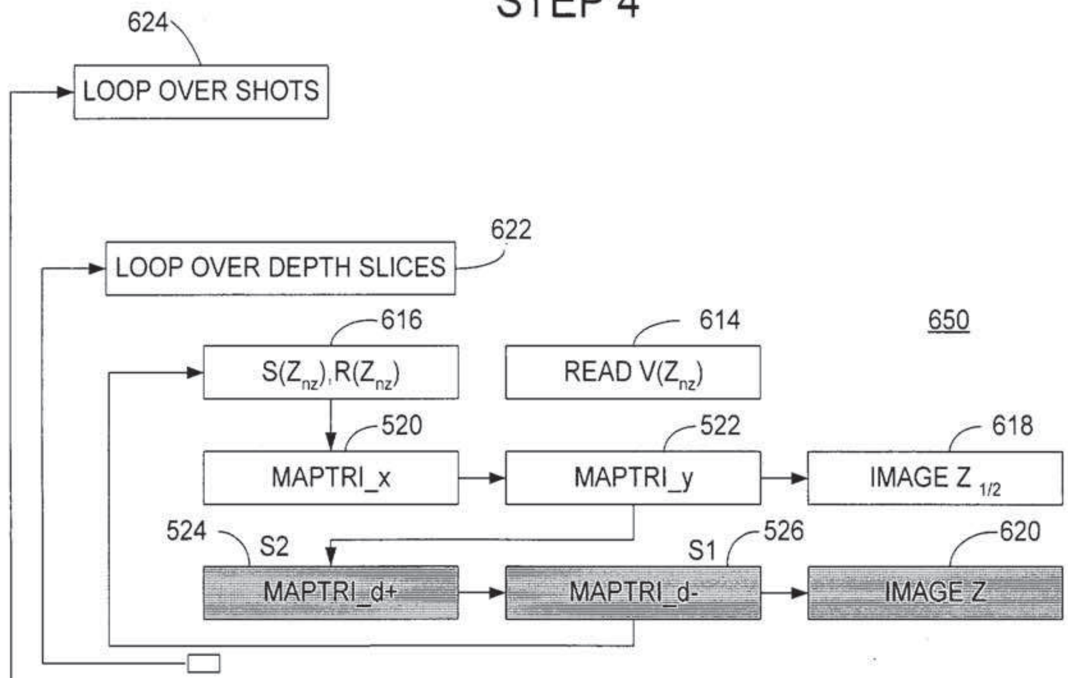


Fig. 6F

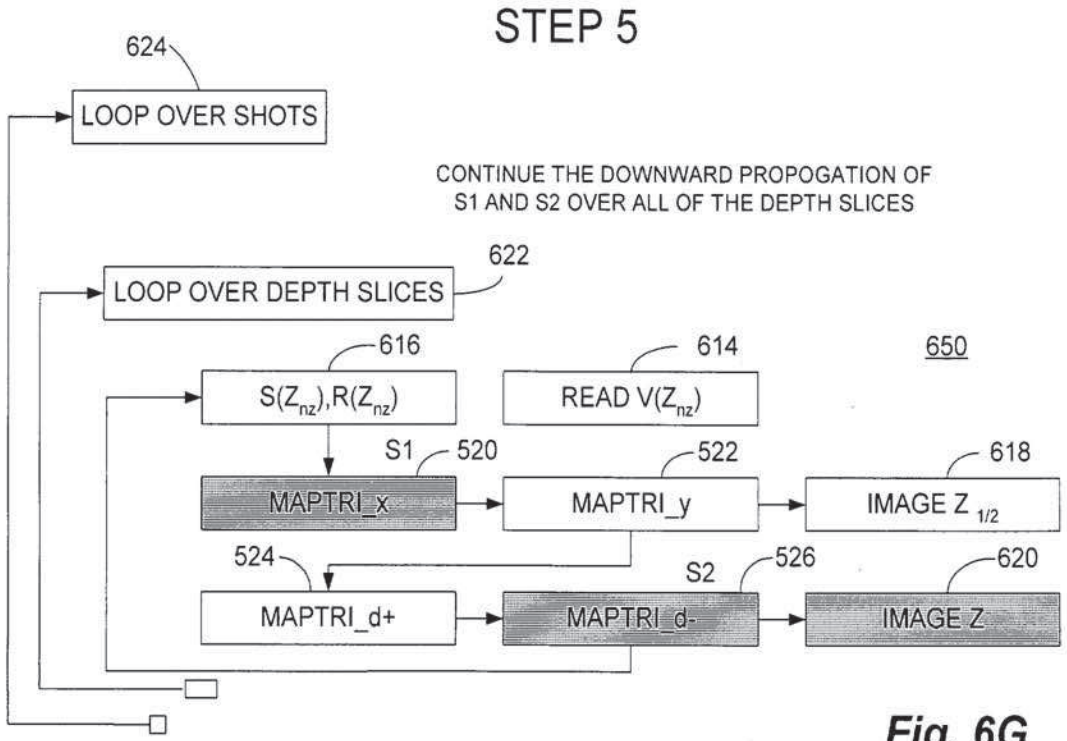


Fig. 6G

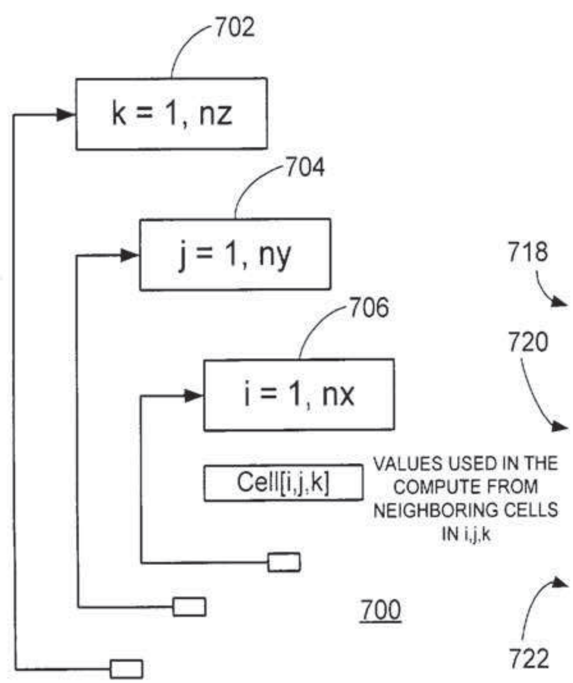

702
k = 1, nz
704
j = 1, ny
706
i = 1, nx
Cell[i,j,k]
VALUES USED IN THE
COMPUTE FROM
NEIGHBORING CELLS
IN i,j,k
700

Fig. 7A

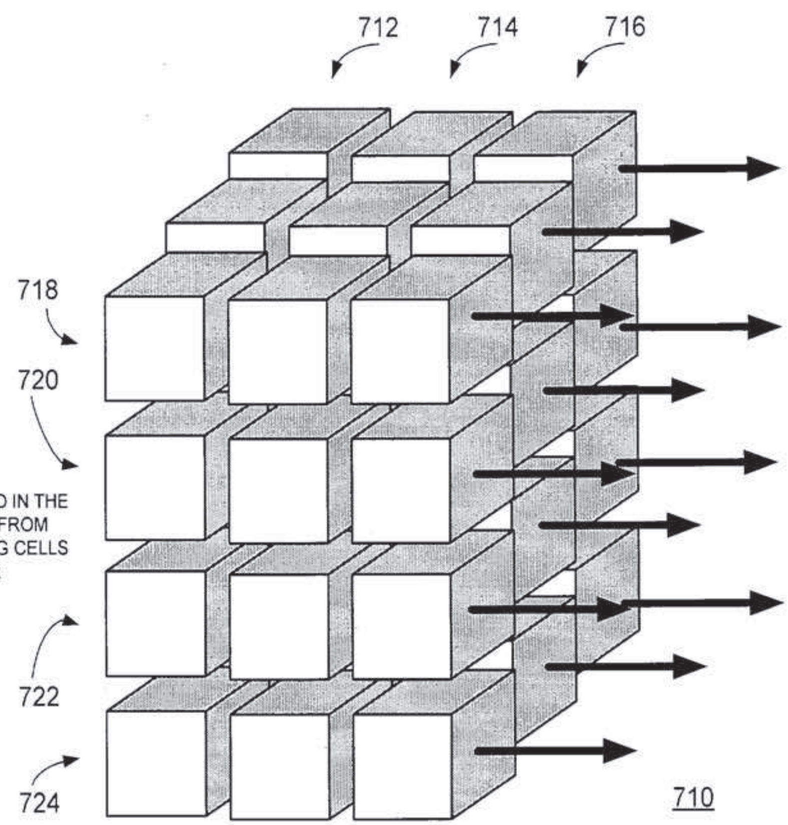

712
714
716
718
720
722
724
710

Fig. 7B

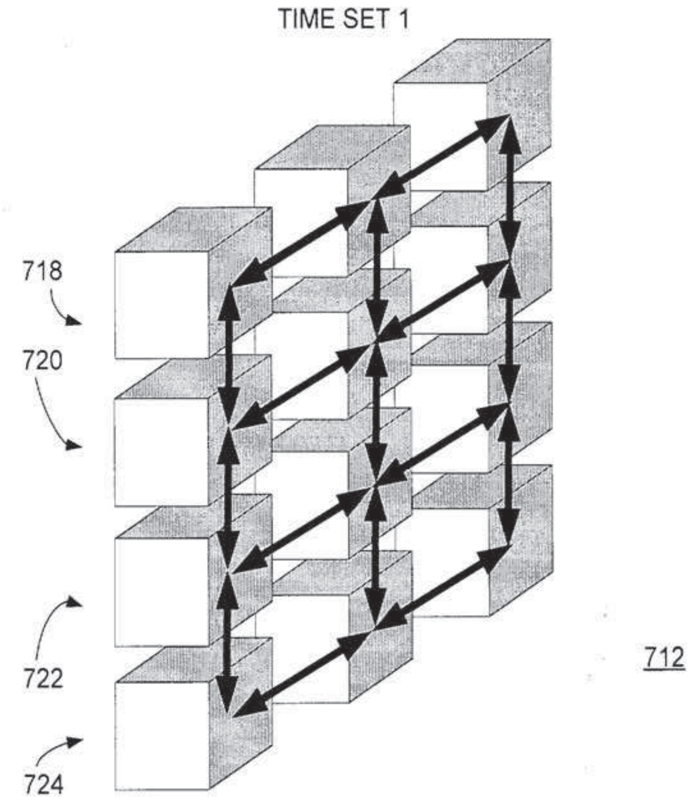


Fig.7C

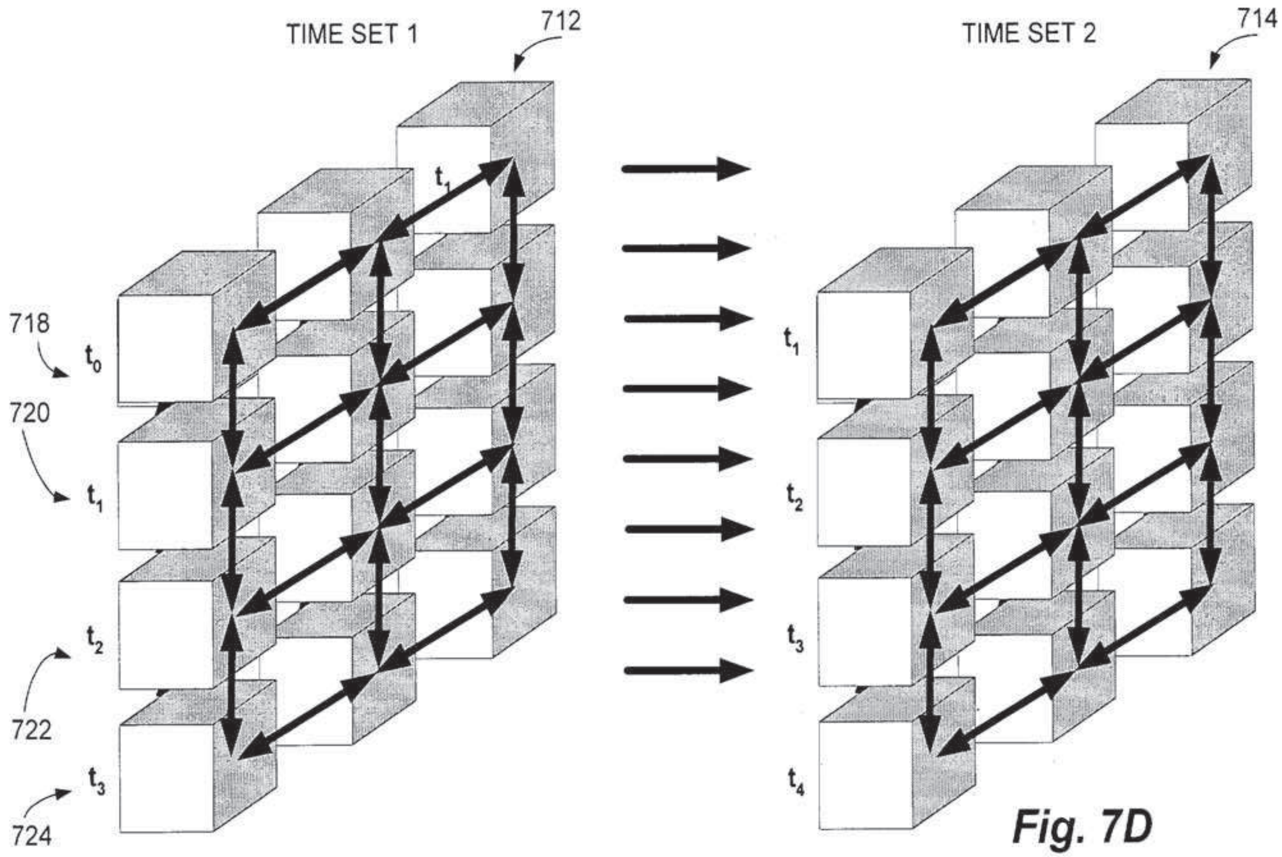


Fig. 7D

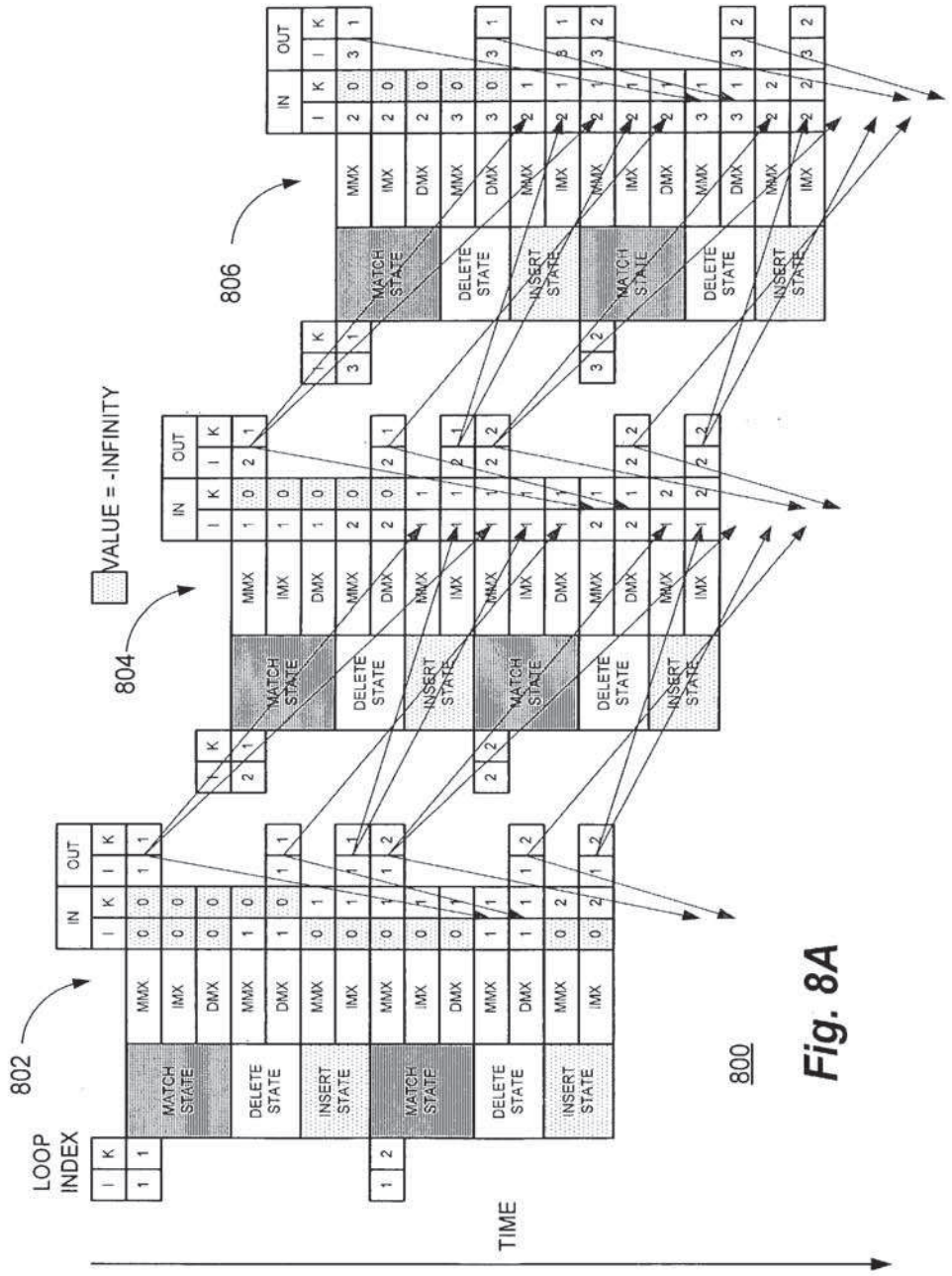

LOOP INDEX
I K
1 1
802
MATCH STATE
DELETE STATE
INSERT STATE
MMX
IMX
DMX
IN
OUT
VALUE = -INFINITY
804
806
TIME
800

Fig. 8A

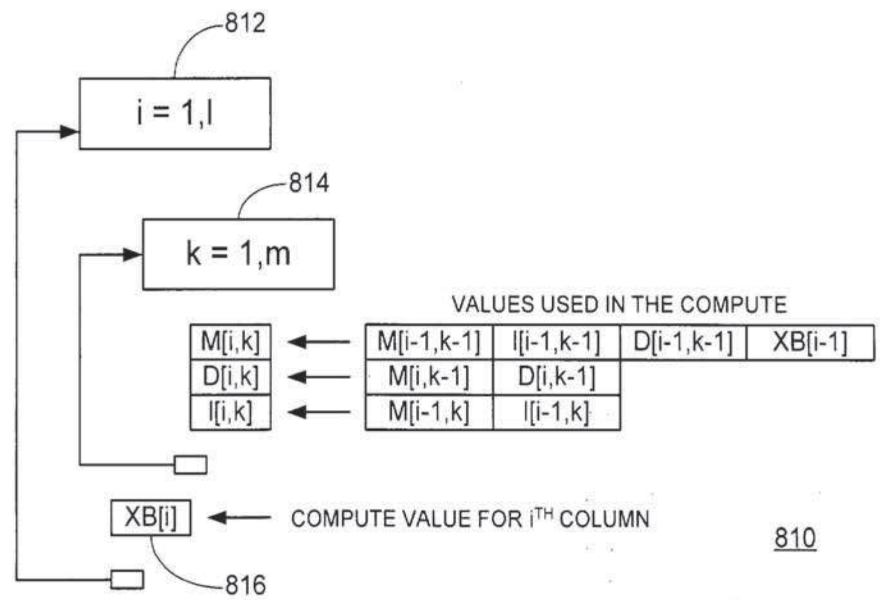
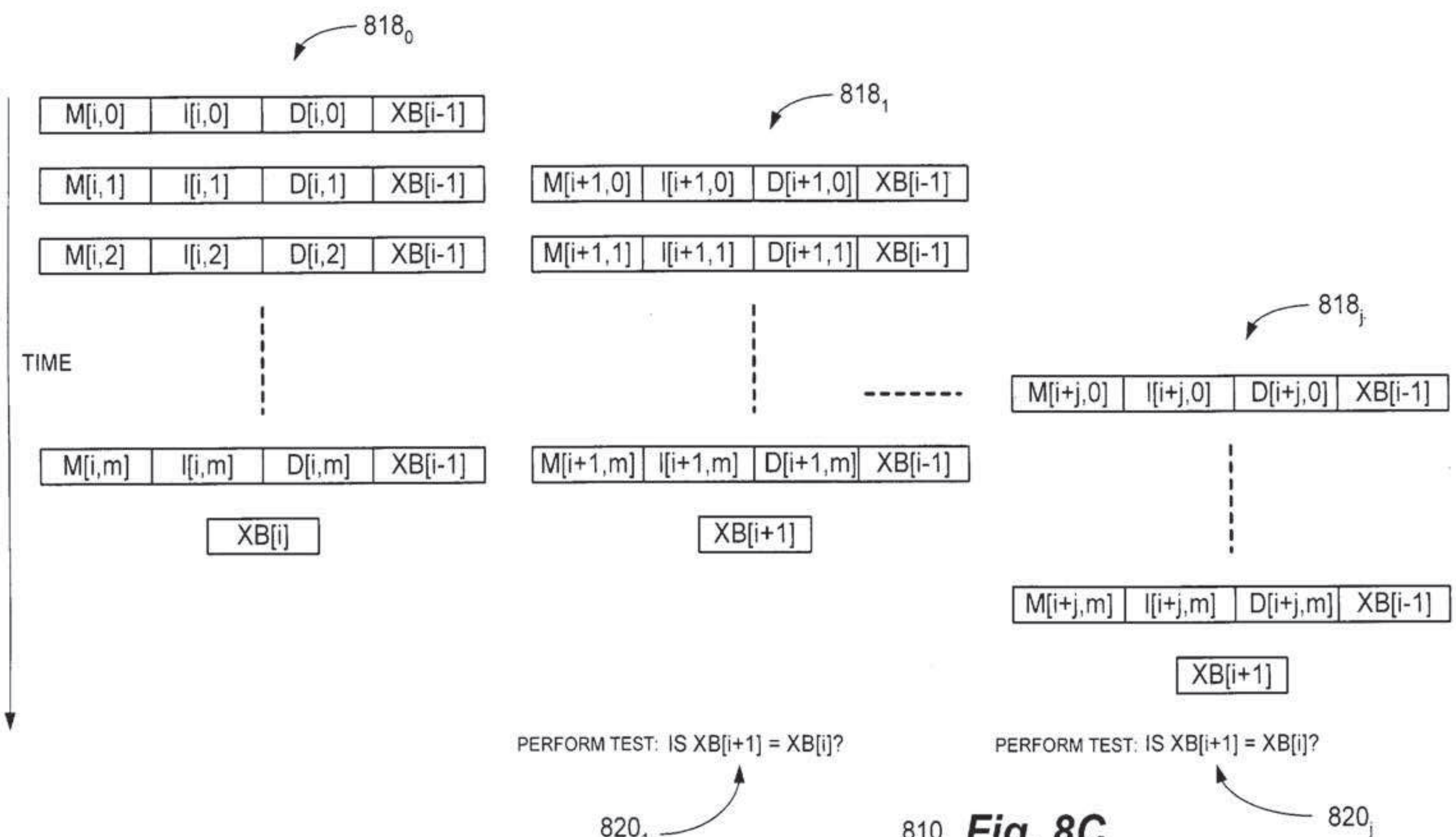

812
i = 1,l
814
k = 1,m
VALUES USED IN THE COMPUTE
M[i,k]
D[i,k]
I[i,k]
M[i-1,k-1]
I[i-1,k-1]
D[i-1,k-1]
XB[i-1]
M[i,k-1]
D[i,k-1]
M[i-1,k]
I[i-1,k]
XB[i]
COMPUTE VALUE FOR iTH COLUMN
816
810

Fig. 8B



810 ***Fig. 8C***

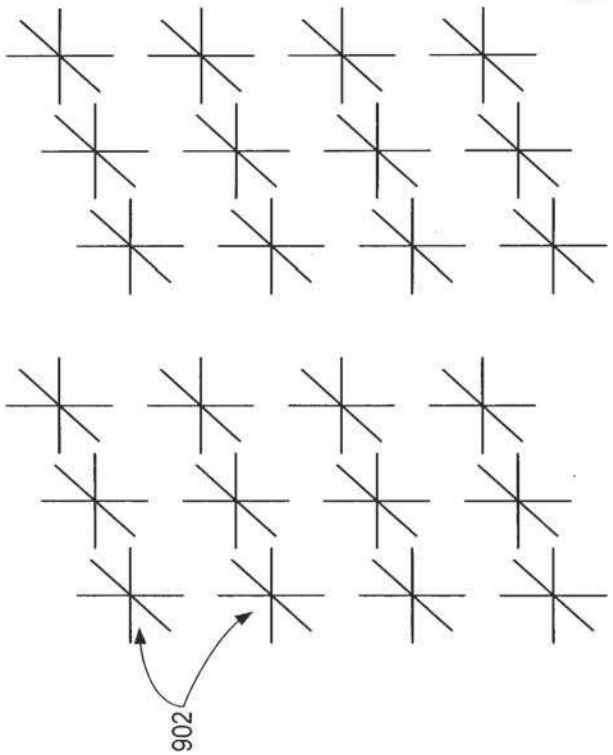


Fig. 9A

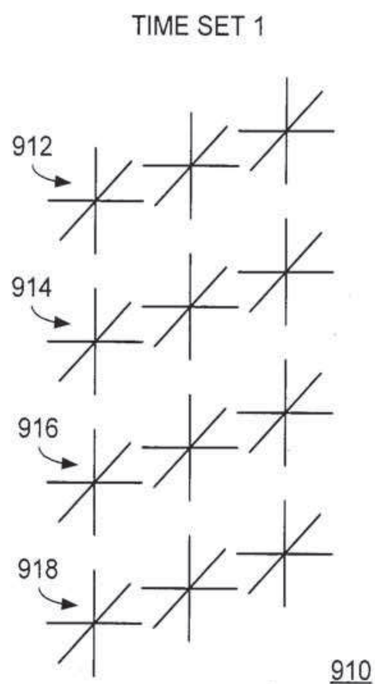


Fig. 9B

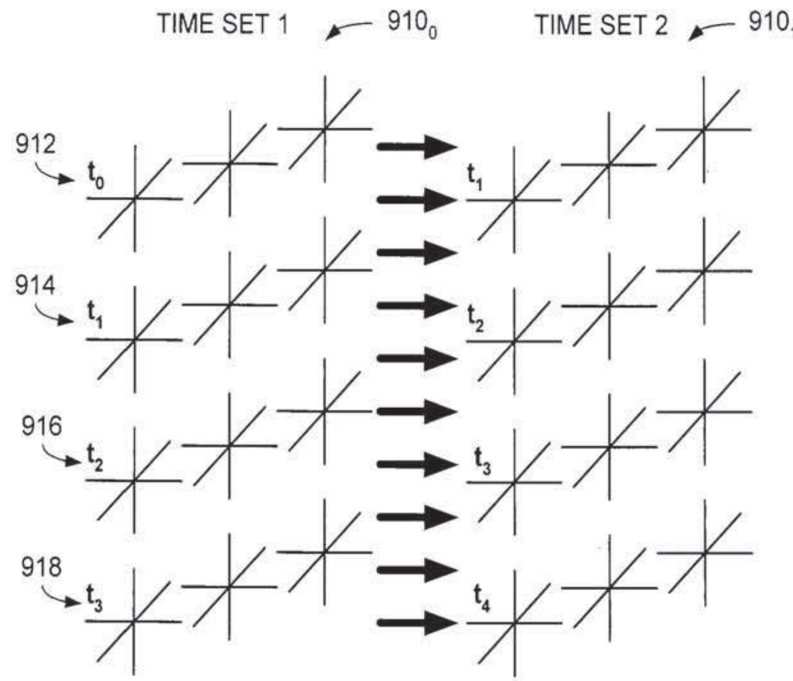


Fig. 9C

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☒ Declaration Submitted with Initial Filing OR ☐ Declaration Submitted after Initial Filing-- surcharge 37 CFR 1.16(e) required

Attorney Docket No.	SRC015
First Named Inventor	Jon M. Huppenthal et al.
COMPLETE IF KNOWN	
Application Number	----------
Filing Date	Herewith
Group Art Unit	
Examiner Name	

As a below named Inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

the specification of which

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) _____ as U.S. Application No. or PCT International Application No. _____

and was amended on (MM/DD/YYYY) _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C § 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Appl. No.(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? Yes	No
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application nos. are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

DECLARATION – Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any U.S. application(s) or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application

U.S. Parent Application or PCT Parent No.	Parent Filing Date (MM/DD/YY)	Parent Patent No. (if applicable)

☐ Additional U.S. or PCT international application nos. listed on PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent Trademark Office connected therewith:

☒ Customer Number 25235 Place bar code label here

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☐ Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number

☐ Additional registered practitioner(s) named on supplemental sheet PTO/SB/02C attached hereto.

Direct all correspondence to: ☒ Customer Number **25235** OR ☐ Correspondence address below

or Bar Code Label

Name					
Address					
City		**State**		**ZIP**	
Country		**Telephone**		**Fax**	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor.

Given Name (first and middle [if any])	Family Name or Surname
Jon M.	**Huppenthal**

Inventor's Signature						Date	
Residence City	**Colorado Springs**	State	**Colorado**	Country	**USA**	Citizenship	**USA**
Mailing Address	**10015 Burgess Road**						
City	**Colorado Springs**	State	**Colorado**	ZIP	**80908**	Country	**USA**

☒Additional inventors are named on _1__supplemental additional inventor(s) sheet(s) PTO/SB/02A attached

DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet Page __1__ of __1___

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])	Family Name or Surname						
David E.	**Caliga**						
Inventor's Signature						Date	
Residence: City	**Colorado Springs**	State	**CO**	Country	**USA**	Citizenship	**USA**
Mailing Address	**8445 Lauralwood Lane**						
City	**Colorado Springs**	State	**CO**	ZIP	**80919**	Country	**USA**

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])	Family Name or Surname						
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Mailing Address							
City		State		ZIP		Country	

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])	Family Name or Surname						
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Mailing Address							
City		State		ZIP		Country	

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number: 10285378

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	55	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	55 minus 20=	* 35
INDEPENDENT CLAIMS	4 minus 3 =	* 1
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	630
X42=		OR	X84=	84
+140=		OR	+280=	
TOTAL		OR	TOTAL	1484

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
Washington, DC 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/285,318	10/31/2002	Jon M. Huppenthal	SRC015

CONFIRMATION NO. 1420

25235
HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

FORMALITIES LETTER

OC000000009216113

Date Mailed: 12/09/2002

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **740** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- Additional claim fees of **$714** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$1584** for a Large Entity

- **$740** Statutory basic filing fee.
- **$130** Late oath or declaration Surcharge.

- Total additional claim fee(s) for this application is **$714**
  - **$630** for **35** total claims over 20 .
  - **$84** for **1** independent claims over 3 .

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

43

Attorney Docket No. SRC015
Client/Matter No. 80404.0018
Express Mail No. EV035495015US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Jon M. Huppenthal and David E. Caliga	Group Art Unit: 2121
Serial No. 10/285,318	Examiner: Not yet assigned
Filed: October 31, 2002	Confirmation No.: 1420
For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS	

RESPONSE TO NOTICE TO FILE MISSING PARTS

BOX MISSING PARTS
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Notice to File Missing Parts of Application, Filing Date Granted, mailed December 9, 2002, submitted herewith is a signed Declaration for Patent Application; a check in the amount of $1,594 to cover $1,464 for the filing fee and $130 to cover the surcharge for a large entity; and a copy of the PTO Notice form. Any fee deficiency associated with this communication may be charged to Deposit Account No. 50-1123.

Also enclosed is a Recordation Form Cover Sheet PTO 1595 with executed Assignment and recording fee of $40.00. Please forward the Assignment to the Recording Branch for recording.

Date: 09 January 2003

William J. Kubida, Registration No. 29,664
HOGAN & HARTSON LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5909 Tel
(303) 899-7333 Fax

FEE TRANSMITTAL for FY 2003

OIPE JAN 09 2003 PATENT & TRADEMARK OFFICE

OIPE JAN 09 2002 PATENT & TRADEMARK OFFICE

☐ Applicant claims small entity status. See 37 CFR 1.27	
TOTAL AMOUNT OF PAYMENT	($) 1,634.00

Complete if Known	
Application Number	10/285,318
Filing Date	October 31, 2002
First Named Inventor	Jon M. Huppenthal et al.
Examiner Name	Not yet assigned
Group / Art Unit	2121
Attorney Docket No.	SRC015

METHOD OF PAYMENT (check all that apply)

☒ check ☐ credit card ☐ money order ☐ other ☐ none

☐ Deposit Account

Deposit Account Number: 50-1123

Deposit Account Name: Hogan & Hartson L.L.P.

The Commissioner is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) for **this** filing

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee ($)	Small Entity Fee ($)	Fee Description	Fee Paid
750	375	Utility Filing Fee	750.00
330	165	Design filing fee	
520	260	Plant filing fee	
750	375	Reissue filing fee	
160	80	Provisional filing fee	

SUBTOTAL (1) ($) 750.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims	55	-20**=	35	X	18	=	630.00
Independent Claims	4	-3**=	1	X	1	=	84.00
Multiple Dependent						=	

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee ($)	Small Entity Fee ($)	Fee Description
18	9	Claims in excess of 20
84	42	Independent claims in excess of 3
280	140	Multiple dependent claim, if not paid
84	42	**Reissue independent claims over original patent
18	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 714.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee ($)	Small Entity Fee ($)	Fee Description	Fee Paid
130	65	Surcharge – late filing fee or oath	130.00
50	25	Surcharge – late provisional filing fee or cover sheet	
130	130	Non-English specification	
2,520	2,520	For filing a request for ex parte reexamination	
920*	920*	Requesting publication of SIR prior to Examiner action	
1,840*	1,840*	Requesting publication of SRI after Examiner action	
110	55	Extension for reply within first month	
410	205	Extension for reply within second month	
930	465	Extension for reply within third month	
1,450	725	Extension for reply within fourth month	
1,970	985	Extension for reply within fifth month	
320	160	Notice of Appeal	
320	160	Filing a brief in support of an appeal	
280	140	Request for oral hearing	
1,510	1,510	Petition to institute a public use proceeding	
110	55	Petition to revive – unavoidable	
1,300	650	Petition to revive – unintentional	
1,300	650	Utility issue fee (or reissue)	
470	235	Design issue fee	
630	315	Plant issue fee	
130	130	Petitions to the Commissioner	
50	50	Processing fee under 37 CFR 1.17(q)	
180	180	Submission of Info Disclosure Stmt	
40	40	Recording each patent assignment per property (times number of properties)	40.00
750	375	Filing a submission after final rejection (37 CFR § 1.129(a))	
750	375	For each additional invention to be examined (37 CFR §1.129(b))	
750	375	Request for Continued Examination	
900	900	Request for expedited examination of a design application	
Other fee (specify)			

*Reduced by Basic Fling Fee Paid SUBTOTAL (3) ($) 170.00

SUBMITTED BY	Complete *(if applicable)*				
Name *(Print/Type)*	William J. Kubida	Registration No. (Attorney/Agent)	29,664	Telephone	(719) 448-5900
Signature				Date	01 Jan 2003

\\\CS - 80404/0018 - 57948 v1

01-10-03

Attorney Docket No. SRC015
Client/Matter No. 80404.0018
Express Mail No. EV035495015US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Jon M. Huppenthal and David E. Caliga	Group Art Unit: 2121
Serial No. 10/285,318	Examiner: Not yet assigned
Filed: October 31, 2002	Confirmation No.: 1420
For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS	

CERTIFICATE OF MAILING BY EXPRESS MAIL

BOX MISSING PARTS
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned hereby certifies that the following documents:

1. Response to Notice to File Missing Parts;
2. Copy of Notice to File Missing Parts of Application Filing Date Granted, form and surcharge payment of $130;
3. Executed Declaration;
4. Fee Transmittal with check in the amount of $1,464;
5. Recordation Form Cover Sheet PTO 1595 with Executed Assignment and Recording Fee of $40.00;
6. Certificate of Mailing By Express Mail;
7. Return postcard;

relating to the above application, were deposited as "Express Mail", Mailing Label No. EV035495015US with the United States Postal Service, addressed to Box Missing Parts, Assistant Commissioner for Patents, Washington, D.C., 20231, on Jan. , 2003

9 January 2003
Date

Mailer

09 January 2003
Date

William J. Kubida, Reg. No. 29,664
HOGAN & HARTSON LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5909 Tel
(303) 899-7333 Fax

\\\CS - 80404/0018 - 57948 v1

Commissioner for Patents
Washington, DC 20231
www.uspto.gov

APPLICATION NUMBER	FILING RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/285,318	10/31/2002	Jon M. Huppenthal	SRC015

CONFIRMATION NO. 1420

25235
HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

FORMALITIES LETTER

OC000000009216113

Date Mailed: 12/09/2002

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **740** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- Additional claim fees of **$714** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$1584** for a Large Entity

- **$740** Statutory basic filing fee.
- **$130** Late oath or declaration Surcharge.

01/13/2003 NHOHAMM1 00000075 10285318

01 FC:1001	750.00 OP
02 FC:1051	130.00 OP
03 FC:1202	630.00 OP
04 FC:1201	84.00 OP

- Total additional claim fee(s) for this application is **$714**
  - **$630** for **35** total claims over 20 .
  - **$84** for **1** independent claims over 3 .

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

Attorney Docket No.	SRC015
First Named Inventor	Jon M. Huppenthal et al.
COMPLETE IF KNOWN	
Application Number	10/285,318
Filing Date	October 31, 2002
Group Art Unit	2121
Examiner Name	Not yet assigned

☐ Declaration Submitted with Initial Filing

☒ Declaration Submitted after Initial Filing--surcharge 37 CFR 1.16(e) required

As a below named Inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

the specification of which

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) 10/31/2002

and was amended on (MM/DD/YYYY) _____

as U.S. Application No. or PCT International Application No. 10/285,318

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C § 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Appl. No.(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? Yes	No
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application nos. are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

DECLARATION – Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any U.S. application(s) or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application

U.S. Parent Application or PCT Parent No.	Parent Filing Date (MM/DD/YY)	Parent Patent No. (if applicable)

☐ Additional U.S. or PCT international application nos. listed on PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent Trademark Office connected therewith:

☒ Customer Number 25235 Place bar code label here

OR

☐ Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number

☐ Additional registered practitioner(s) named on supplemental sheet PTO/SB/02C attached hereto.

Direct all correspondence to: ☒ Customer Number **25235** OR ☐ Correspondence address below

or Bar Code Label

Name					
Address					
City		**State**		**ZIP**	
Country		**Telephone**		**Fax**	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor.

Given Name (first and middle [if any])	Family Name or Surname
Jon M.	**Huppenthal**

Inventor's Signature	Jon Huppenthal					Date	1/6/03
Residence City	**Colorado Springs**	State	**Colorado**	Country	**USA**	Citizenship	**USA**
Mailing Address	**10015 Burgess Road**						
City	**Colorado Springs**	State	**Colorado**	ZIP	**80908**	Country	**USA**

☒Additional inventors are named on _1__supplemental additional inventor(s) sheet(s) PTO/SB/02A attached

DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet Page __1__ of __1___

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])	Family Name or Surname						
David E.	**Caliga**						
Inventor's Signature	D. E. Caliga					Date	1/6/2003
Residence: City	**Colorado Springs**	State	**CO**	Country	**USA**	Citizenship	**USA**
Mailing Address	**8445 Lauralwood Lane**						
City	**Colorado Springs**	State	**CO**	ZIP	**80919**	Country	**USA**

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])	Family Name or Surname						
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Mailing Address							
City		State		ZIP		Country	

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])	Family Name or Surname						
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Mailing Address							
City		State		ZIP		Country	

08/14/03

2121
#4
SP
8-21-03

Express Mail No. EV335405389US
Attorney Docket No. SRC015
Client/Matter No. 80404.0018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Jon M. Huppenthal and David E. Caliga	Group Art Unit: 2121
Serial No. 10/285,318	Examiner: Not yet assigned
Filed: October 31, 2002	Confirmation No.: 1420
For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS	

CERTIFICATE OF MAILING BY EXPRESS MAIL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

The undersigned hereby certifies that the attached:

1. Information Disclosure Statement;
2. Form PTO/SB/08A, with references;
3. Certificate of Mailing; and
4. Return card

relating to the above application, were deposited as "Express Mail" Mailing Label No. EV335405389US, with the United States Postal Service, addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 13 August 2003

13 August 2003
Date

Mailer

Aug. 13, 2003
Date

Peter J. Meza, Reg. No. 32,920
HOGAN & HARTSON LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5900 Tel
(303) 899-7333 Fax

\\\CS - 80404/0018 - 62565 v1

Express Mail No.EV335405389US
Attorney Docket No. SRC015
Client/Matter No. 80404.0018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Jon M. Huppenthal and David E. Caliga	Group Art Unit: 2121
Serial No. 10/285,318	Examiner: Not yet assigned
Filed: October 31, 2002	Confirmation No.: 1420
For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS	

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits for filing under 37 CFR 1.97 a disclosure statement. In submitting these references, no representation is made or implied that the references are or are not material to the examination of this application. The patents, publications or other information of which Applicant is presently aware are listed in Form PTO/SB/08A submitted herewith and copies of all such patents and publications are attached hereto.

No fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

Aug. 13, 2003
Date

Peter J. Meza, Reg. No. 32,920
HOGAN & HARTSON LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5906 Tel
(303) 899-7333 Fax

PTO/SB/08A (10/01) (Substitute for form 1449A/PTO)	ATTY. DOCKET NO. SRC015 Client/Matter No. 80404.0018	APPLICATION NO. 10/285,318
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FIRST NAMED INVENTOR Jon M. Huppenthal and David E. Caliga	
(Use several sheets if necessary)	FILING DATE October 31, 2002	ART UNIT 2121
Sheet ___1___ of ___4___		

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document No. No. – Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-5,230,057	07/20/93	Shido, et al.	
		US-5,892,962	04/06/99	Cloutier	
		US-5,903,771	05/11/1999	Sgro et al.	Figs 1 & 6, col. 3, lines 30-67, col 4, lines 1-51, col 7, lines 1-27.
		US-6,192,439	02/20/2001	Grunewald et al.	Fig 3, col 3, lines 53-67, col 4, lines 1-64.
		US-6,076,152	06/13/2000	Huppenthal et al.	
		US-6,052,773	04/18/2000	DeHon et al.	
		US-6,226,776	05/01/2001	Panchul et al.	
		US-6,023,755	02/08/2000	Casselman	
		US-5,737,766	04/07/1998	Tan	
		US-5,570,040	10/29/1996	Lytle et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Doc cntry code – No. – Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns. Lines Where Relevant Passages or Relevant Figures Appear	TRANSLATION YES	TRANSLATION NO

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher, city and/or country where published
	1	AGARWAL, A., et al., "The Raw Compiler Project", pages 1-12, http://cag-www.lcs.mit.edu/raw, Proceedings of the Second SUIF Compiler Workshop, Augs. 21-23, 1997.
		ALBAHARNA, OSAMA, et al., "On the viability of FPGA-based integrated coprocessors", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 206-215.
		AMERSON, RICK, et al., "Teramac----Configurable Custom Computing", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 32-38.

		BARTHEL, DOMINIQUE August 25-26, 1997, "PVP a Parallel Video coProcessor", Hot Chips IX, Pages 203-210.
		BERTIN, PATRICE, et al., "Programmable active memories: a performance assessment", © 1993 Massachusetts Institute of Technology, Pages 88-102.
		BITTNER, RAY, et al., "Computing kernels implemented with a wormhole RTR CCM", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 98-105.
		BUELL, D., et al. "Splash 2: FPGAs in a Custom Computing Machine – Chapter 1 -- Custom Computing Machines: An Introduction", Pages 1-11, http://www.computer.org/espress/catalog/bp07413/spls-ch1.html (originally believed published in J. of Supercomputing, Vol. IX, 1995, PP. 219-230.
		CASSELMAN, STEVEN, "Virtual Computing and The Virtual Computer", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 43-48.
		CHAN, PAK, et al., "Architectural tradeoffs in field-programmable-device-based computing systems", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 152-161.
		CLARK, DAVID, et al., "Supporting FPGA microprocessors through retargetable software tools", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 195-103.
		CUCCARO, STEVEN, et al., "The CM-2X: a hybrid CM-2/Xilink prototype", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 121-130.
		CULBERTSON, W. BRUCE, et al., "Exploring architectures for volume visualization on the Teramac custom computer", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 80-88.
		CULBERTSON, W. BRUCE, et al., "Defect tolerance on the Teramac custom computer", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 116-123.
		DEHON, ANDRE, "DPGA-Coupled microprocessors: commodity IC for the early 21st century", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 31-39.
		DEHON, A., et al., "MATRIX A Reconfigurable Computing Device with Configurable Instruction Distribution", Hot Chips IX, August 25-26, 1997, Stanford, California, MIT Artificial Intelligence Laboratory.
		DHAUSSY, PHILIPPE, et al., "Global control synthesis for an MIMD/FPGA machine", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 72-81.
		ELLIOTT, DUNCAN, et al., "Computational Ram: a memory-SIMD hybrid and its application to DSP", © 1992 IEEE, Publ. No. 0-7803-0246-X/92, Pages 30.6.1-30.6.4.
		FORTES, JOSE, et al., "Systolic arrays, a survey of seven projects", © 1987 IEEE, Publ. No. 0018-9162/87/0700-0091, Pages 91-103.
		GOKHALE, M., et al., "Processing in Memory: The Terasys Massively Parallel PIM Array" © April 1995, IEEE, Pages 23-31.
		GUNTHER, BERNARD, et al., "Assessing Document Relevance with Run-Time Reconfigurable Machines", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 10-17.
		HAGIWARA, HIROSHI, et al., "A dynamically microprogrammable computer with low-level parallelism", © 1980 IEEE, Publ. No. 0018-9340/80/07000-0577, Pages 577-594.
		HARTENSTEIN, R. W., et al. "A General Approach in System Design Integrating Reconfigurable Accelerators," http://xputers.informatik.uni-kl.de/papers/paper026-1.html, IEEE 1996 Conference, Austin, TX, Oct. 9-11, 1996.
		HARTENSTEIN, REINER, et al., "A reconfigurable data-driven ALU for Xputers", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 139-146.
		HAUSER, JOHN, et al.: "GARP: a MIPS processor with a reconfigurable co-processor", © 1997 IEEE, Publ. No. 0-08186-8159-4/97, Pages 12-21.
		HAYES, JOHN, et al., "A microprocessor-based hypercube, supercomputer", © 1986 IEEE, Publ. No. 0272-1732/86/1000-0006, Pages 6-17.
		HERPEL, H. –J., et al., "A Reconfigurable Computer for Embedded Control Applications", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 111-120.
		HOGL, H., et al., "Enable++: A second generation FPGA processor", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 45-53.
		KING, WILLIAM, et al., "Using MORRPH in an industrial machine vision system". © 1996 IEEE, Publ. No. 08186-7548-9/96, Pages 18-26.

		MANOHAR, SWAMINATHAN, et al., "A pragmatic approach to systolic design", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0463, Pages 463-472.
		MAUDUIT, NICOLAS, et al., "Lneuro 1.0: a piece of hardware LEGO for building neural network systems," © 1992 IEEE, Publ. No. 1045-9227/92, Pages 414-422.
	✓	MIRSKY, ETHAN A., "Coarse-Grain Reconfigurable Computing", Massachusetts Institute of Technology, June 1996.
	✓	MIRSKY, ETHAN, et al., "MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 157-166.
		MORLEY, ROBERT E., Jr., et al., "A Massively Parallel Systolic Array Processor System", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0217, Pages 217-225.
	✓	PATTERSON, DAVID, et al., "A case for intelligent DRAM: IRAM", Hot Chips VIII, August 19-20, 1996, Pages 75-94.
	✓	PETERSON, JANES, et al., "Scheduling and partitioning ANSI-C programs onto multi-FPGA CCM architectures", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 178-187.
	✓	SCHMIT, HERMAN, "Incremental reconfiguration for pipelined applications," © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 47-55.
	✓	SITKOFF, NATHAN, et al., "Implementing a Genetic Algorithm on a Parallel Custom Computing Machine", Publ. No. 0-8186-7086-X/95, Pages 180-187.
		STONE, HAROLD, "A logic-in-memory computer", © 1970 IEEE, IEEE Transactions on Computers, Pages 73-78, January 1990.
		TANGEN, UWE, et al., "A parallel hardware evolvable computer POLYP extended abstract", © 1997 IEEE, Publ. No. 0-8186-8159/4/97, Pages 238-239.
		THORNBURG, MIKE, et al., "Transformable Computers", © 1994 IEEE, Publ. No. 0-8186-5602-6/94, Pages 674-679.
		TOMITA, SHINJI, et al., "A computer low-level parallelism QA-2", © 1986 IEEE, Publ. No. 0-0384-7495/86/0000/0280, Pages 280-289.
		TRIMBERGER, STEVE, et al., "A time-multiplexed FPGA", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 22-28.
		UEDA, HIROTADA, et al., "A multiprocessor system utilizing enhanced DSP's for image processing", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0611, Pages 611-620.
		VILLASENOR, JOHN, et al., "Configurable computing", © 1997 Scientific American, June 1997.
		WANG, QUIANG, et al., "Automated field-programmable compute accelerator design using partial evaluation", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 145-154.
		W.H. Mangione-Smith and B.L. Hutchings. Configurable computing: The Road Ahead. In Proceedings of the Reconfigurable Architectures Workshop (RAW'97), pages 81-96, 1997.
		WIRTHLIN, MICHAEL, et al., "The Nano processor: a low resource reconfigurable processor", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 23-30.
		WIRTHLIN, MICHAEL, et al., "A dynamic instruction set computer", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 99-107.
		WITTIG, RALPH, et al., "One Chip: An FPGA processor with reconfigurable logic", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 126-135.
		YAMAUCHI, TSUKASA, et al., "SOP: A reconfigurable massively parallel system and its control-data flow based compiling method", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 148-156.
		"Information Brief", PCI Bus Technology, © IBM Personal Computer Company, 1997, Pages 1-3.
		YUN, HYUN-KYU AND SILVERMAN, H. F.; "A distributed memory MIMD multi-computer with reconfigurable custom computing capabilities", Brown University, 10-13 Dec. 1997, pp. 7-13.
		HOOVER, CHRIS AND HART, DAVID; "San Diego Supercomputer Center, Timelogic and Sun Validate Ultra-Fast Hidden Markov Model Analysis-One DeCypher-accelerated Sun Fire 6800 beats 2,600 CPUs running Linux-", San Diego Supercomputer Center, http://www.sdsc.edu/Press/02/050802_markovmodel.html, May 8, 2002, pp. 1-3.
		CALIGA, DAVID AND BARKER, DAVID PETER, "Delivering Acceleration: The Potential for Increased HPC Application Performance Using Reconfigurable Logic", SRC Computers, Inc., November 2001, pp. 20.
		HAMMES, J.P., RINKER, R. E., MCCLURE, D. M., BÖHM, A. P. W., NAJJAR, W. A., "The SA-C Compiler Dataflow Description", Colorado State University, June 21, 2001, pp. 1-25.

	p	CALLAHAN, TIMOTHY J. AND WAWRZYNEK, JOHN, "Adapting Software Pipelining for Reconfigurable Computing", University of California at Berkeley, November 17-19, 2000, pp. 8.
	q	RATHA, NALINI K., JAIN, ANIL K. AND ROVER, DIANE T., "An FPGA-based Point Pattern Matching Processor with Application to Fingerprint Matching", Michigan State University, Department of Computer Science, pp. 8.
		DEHON, ANDRÉ, "Comparing Computing Machines", University of California at Berkeley, Proceedings of SPIE Vol. 3526, November 2-3, 1998, pp. 11.
	u	VEMURI, RANGA R. AND HARR, RANDOLPH E., "Configurable Computing: Technology and Applications", University of Cincinnati and Synopsys Inc., IEEE, April 2000, pp. 39-40.
	v	DEHON, ANDRÉ, "The Density Advantage of Configurable Computing", California Institute of Technology, IEEE, April 2000. pp. 41-49.
		HAYNES, SIMON D., STONE, JOHN, CHEUNG, PETER Y.K. AND LUK, WAYNE, "Video Image Processing with the Sonic Architecture", Sony Broadcast & Professional Europe, Imperial College, University of London, IEEE, April 2000, pp. 50-57.
		PLATZNER , MARCO, "Reconfigurable Accelerators for Combinatorial Problems", Swiss Federal Institute of Technology (ETH) Zurich, IEEE, April 2000, pp. 58-60.
	x	CALLAHAN, TIMOTHY J., HAUSER, JOHN R. AND WAWRZYNEK, JOHN, "The Garp Architecture and C Compiler", University of California, Berkeley, IEEE, April 2000. pp. 62-69.
	y	GOLDSTEIN, SETH COPEN, SCHMIT, HERMAN, BUDIU , MIHAI, CADAMBI, SRIHARI, MOE, MATT AND TAYLOR, R. REED, "PipeRench: A Reconfigurable Architecture and Compiler", Carnegie Mellon University, IEEE, April 2000, pp. 70-76.
	z	MUCHNICK, STEVEN S., "Advanced Compiler Design and Implementation", Morgan Kaufmann Publishers, pp. 217.
	aa	HAMMES, JEFFREY P., Dissertation "Compiling SA-C To Reconfigurable Computing Systems", Colorado State University, Department of Computer Science, Summer 2000, pp. 179.
	bb	Automatic Target Recognition, Colorado State University & USAF, http://www.cs.colostate.edu/cameron/applications.html, pp. 1-3.
	cc	CHODOWIEC, PAWEL, KHUON, PO, GAJ, KRIS, Fast Implementations of Secret-Key Block Ciphers Using Mixed Inner- and Outer-Round Pipelining, George Mason University, February 11-13, 2001, pp.9.

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04/16/04

2121

Attorney Docket No. SRC015
Client/Matter No. 80404.0018
Express Mail No. EV331754640US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Confirmation No.: 1420
Jon M. Huppenthal and David E. Caliga	Examiner: Not yet assigned
Serial No. 10/285,318	Art Unit: 2121
Filed: October 31, 2002	
For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS	

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Respectfully submitted,

Date: 14 April 2004

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Sheet 1 of 1

Application Number	10/285,318
Filing Date	October 31, 2002
First Named Inventor	Jon M. Huppenthal et al.
Art Unit	2121
Examiner Name	Not yet assigned
Attorney Docket No.	SRC015

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Document No. No. – Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-6,215,898	04/10/2001	Woodfill et al.	Fig. 3 and col. 9, line 32-col. 16, line 45, and col. 57, line 6-col.67, line 23.
		US-5,020,059	05/28/1991	Gorin et al.	Figs. 5, 9 and col. 7, line 28-col. 9, line 53.
		US-5,471,627	11/28/1995	Means et al.	Fig. 3 and col. 4, line 40- col. 12, line 42.
		US-4,727,503	02/23/1988	McWhirter	Column 3, line 49-col. 4, line 64.
		US-5,477,221	12/19/1995	Chang et al.	Fig. 5 and col. 6, line 48-col. 9, line 6.
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Serial No. 10/285,318

Application of: Jon M. Huppenthal and David E. Caliga

Filed: October 31, 2002

Art Unit: 2121

Examiner: Not yet assigned

Attorney Docket No. SRC015

For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

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Respectfully submitted,

Date: 26 April 2005

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		US-6,385,757	05/07/2002	Gupta et al.	
		US-4,872,133	10/03/1989	Leeland	
		US-5,274,632	12/28/1993	Khan	
		US-5,072,371	12/10/1991	Benner et al.	
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WRITTEN OPINION

(PCT Rule 66)

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Applicant's or agent's file reference: SRC015 PCT	REPLY DUE: within 1 months/days from the above date of mailing

International application No.	International filing date (day/month/year)	Priority date (day/month/year)
PCT/US03/29444	16 September 2003 (16.09.2003)	31 October 2002 (31.10.2002)

International Patent Classification (IPC) or both national classification and IPC

IPC(7): G06F 15/80, 17/16 and US Cl.: 712/15; 708/509

Applicant

SRC COMPUTERS, INC.

1. This written opinion is the first (first, etc.) drawn by this International Preliminary Examining Authority.

2. This opinion contains indications relating to the following items:

- I ☒ Basis of the opinion
- II ☐ Priority
- III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- IV ☐ Lack of unity of invention
- V ☒ Reasoned statement under Rule 66.2 (a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☐ Certain documents cited
- VII ☐ Certain defects in the international application
- VIII ☐ Certain observations on the international application

3. The applicant is hereby invited to reply to this opinion.

When? See the time limit indicated above. ~~The applicant may, before the expiration of that time limit, request this Authority to grant an extension. See rule 66.2(d).~~

How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.

Also For an additional opportunity to submit amendments, see Rule 66.4.
For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4 *bis*.
For an informal communication with the examiner, see Rule 66.6

If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary examination report must be established according to Rule 69.2 is: 28 February 2005 (28.02.2005).

Name and mailing address of the IPEA/US	Authorized officer
Mail Stop PCT, Attn: IPEA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450	Eric Coleman for
Facsimile No. (703)305-3230	Telephone No. (703)-305-3900

Form PCT/IPEA/406 (cover sheet)(July 1998)

WRITTEN OPINION

International application No.
PCT/US03/29444

I. Basis of the opinion

1. With regard to the elements of the international application:*

☒ the international application as originally filed

☒ the description:
pages 1-20, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the claims:
pages 21-23, as originally filed
pages NONE, as amended (together with any statement) under Article 19
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the drawings:
pages 1-20, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☐ the sequence listing part of the description:
pages NONE, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

2. With regard to the language, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination(under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the written opinion was drawn on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages NONE

☐ the claims, Nos. NONE

☐ the drawings, sheets/fig NONE

5. ☐ This opinion has been drawn as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

* *Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed."*

Form PCT/IPEA/408 (Box I) (July 1998)

WRITTEN OPINION

International application No.
PCT/US03/29444

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims 1-13	YES
	Claims NONE	NO
Inventive Step (IS)	Claims 6-12	YES
	Claims 1-5,13	NO
Industrial Applicability (IA)	Claims 1-13	YES
	Claims NONE	NO

2. CITATIONS AND EXPLANATIONS
Please See Continuation Sheet

WRITTEN OPINION

International application No.
PCT/US03/29444

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

TIME LIMIT:
The time limit set for response to a Written Opinion may not be extended. 37 CFR 1.484(d). Any response received after the expiration of the time limit set in the Written Opinion will not be considered in preparing the International Preliminary Examination Report.

V. 2. Citations and Explanations:
Claims 1-2 lack an inventive step under PCT Article 33(3) as being obvious over Gupta (US patent No. 6,385,757) in view of Khan US Patent No. 5,274,832).

Gupta taught the invention substantially as claimed including a data processing ("DP") system comprising: defining a calculation for a reconfigurable computing system instantiating the performance of at least two array functional units (FU00-FU10)(e.g., see col. 17, lines 28-52 and col. 21, lines 22-29) to perform the calculation.

Gupta did not expressly detail utilizing the array functional units to operate on a subsequent data dimension of the calculation and substantially concurrently using the second of the array units to operate on a previous data dimension of the calculation. Khan however taught operating on three dimensions using plural two dimensional arrays that operate concurrently on respective dimensions and are coupled to together to produce the three dimensional array (e.g., see col. 4, lines 35-62 and col. 12, lines 15-55).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Gupta and Khan. One of ordinary skill would have been motivated to incorporate the three dimensional array operation of the Khan reference into the Gupta system to allow the combined system to be able to perform calculations on more complicated (three dimensional) problems.

As to claim 2, Khan taught the calculation comprising plurality of planes (e.g., see col. 12, lines 15-55).

Claim 3 lacks an inventive step under PCT Article 33(3) as being obvious over the prior art as applied in the immediately preceding paragraph and further in view of Leeland (US patent No. 4,872,133). Leeland taught calculation comprised a financial application modeling using a spreadsheet application (e.g., see col. 5, lines 3-32).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Leeland and Gupta. One of ordinary skill would have been motivated to incorporate the Leeland teaching of financial spreadsheet application for an array processor in order to provide an additional use for the combined system.

Claims 4-5 lack an inventive step under PCT Article 33(3) as being obvious over the prior art (Gupta and Khan) as applied in the immediately preceding paragraphs and further in view of Benner (US Patent No. 5,071,371).

Benner taught the calculation comprising fluid flow calculation and structural analysis (e.g., see col. 22, lines 35-52).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Benner and Gupta. One of ordinary skill would have been motivated to incorporate the Benner teaching of fluid flow and structural analysis applications for an array processor in order to provide an additional uses for the combined system.

Claim 13 lacks an inventive step under PCT Article 33(3) as being obvious over Gupta (US Patent No. 6,385,757). Gupta taught the invention substantially as claimed including data processing ("DP") system comprising a reconfigurable processor that provides indication of whether it performs speculative and systolic processing (e.g., see col. 15, lines 6-66). Consequently, one

Form PCT/IPEA/408 (Supplemental Box) (July 1998)

WRITTEN OPINION

International application No.
PCT/US03/29444

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

ordinary skill would have been motivated to perform systolic and speculative processing at least in order to utilize the parameters indicated by Gupta for use in systolic and speculative processing (e.g., see col. 15, lines 56-63).

Claims 6-12 the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the combination of features in independent claims 6 and 12. The combination features in claim 6 comprise defining a first systolic wall comprising rows and cells forming a subset of the plurality of functional units; computing a value at each of the cells in at least a first row of the first systolic wall; communicating the values between cells in the first row of the cells to produce updated values; communicating the updated values to a second row of the first systolic wall; and substantially concurrently providing the updated values to a first row of a second systolic wall of rows of cells in the subset of the plurality of functional units. In claim 12 the combination of features comprise performing a calculation by a subset of the plurality of functional units to produce computed data; passing the computed data from a first column of the calculation to a next column in the calculation; evaluating a rate of change in at least one variable for each of the columns in the calculation; continuing the calculation if the variable does not change for a particular column of the calculation; and restarting the calculation at the column of the calculation where the variable does change.

——————— NEW CITATIONS ———————

US 6,385,757 B1 (GUPTA) 07 May 2002, see column, 2, lines 20-27, column 15, lines 5-66.

US 4,872,133 A (LEELAND) 03 October 1989, see figs. 2,3,5, and col. 3, lines 27-55.

US 5,274,832 A (KHAN) 28 December 1993, see fig.18, col. 5, lines 27-49,col. 8, lines 42-59, and col. 12, lines 1-55.

US 5,072,371 (BENNER) 10 December 1991 see figs. 5,7,14 and col. 22, lines 35-62.

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	16	speculat$3 with systolic$4	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 07:38
L2	343	speculat$3 and systolic$4	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:16
L3	1	speculat$3 and (systolic$4 adj process$3)	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 07:49
L4	140	rate near3 change near3 column$1	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 07:49
L5	1951069	@ay>"2000"	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:16
L6	127	2 not 5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:33
L7	332	column$1 near3 value near3 change$1	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:35
L8	62	restart$3 and 7	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:37
L9	42	until adj value adj change$2	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:36
L10	201	712/15.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:37
L11	46	712/19.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:37
L12	359	712/226.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:37
L13	2	(("6385757") or ("5274832")).PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:50
L14	3	(("6385757") or ("5274832") or ("5071371")).PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:57
L15	4	(("6385757") or ("5274832") or ("5071371") or ("4872133")).PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:03

L16	0	("bennerand(fluidadjflow)").PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:06
L17	74	benner and (fluid adj flow)	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:23
L18	2089	imaging and systolic$5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:23
L19	86	imaging with systolic$5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:38
L20	4	search adj algorithm with systolic$5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:48
L21	3	encryption with systolic$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:57
L22	0	genetic near3 match$3 with systolic$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:57
L23	25	genetic with systolic$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:58
L24	5	dna with systolic$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:00
L25	72	protein with systolic$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:01
L26	12835	dna near3 match$3 systolic$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:02
L27	8	dna near3 match$3 and systolic$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:02

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/285,318	10/31/2002	Jon M. Huppenthal	SRC015	1420

25235 7590 10/07/2005

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/285,318	HUPPENTHAL ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-55 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-55 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5,26-31,52,53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta (US patent No. 6,385,757) in view of Khan US Patent No. 5,274,832).

3. Gupta taught the invention substantially as claimed including a data processing ("DP") system comprising: defining a calculation for a reconfigurable computing system instantiating the performance of at least two array functional units (FU00-FU10)(e.g., see col. 17, lines 28-52 and col. 21, lines 22-29) to perform the calculation.

4. Gupta did not expressly detail utilizing the array functional units to operate on a subsequent data dimension of the calculation and substantially concurrently using the second of the array units to operate on a previous data dimension of the calculation. Khan however taught operating on three dimensions using plural two dimensional arrays that operate concurrently on respective dimensions and are coupled to together to produce the three dimensional array (e.g., see col. 4, lines 35-62 and col. 12, lines 15-55).

5. It would have been obvious to one of ordinary skill in the DP art to combine the

teachings of Gupta and Khan. One of ordinary skill would have been motivated to incorporate the three dimensional array operation of the Khan reference into the Gupta system to allow the combined system to be able to perform calculations on more complicated (three dimensional) problems.

6. As to the further limitations of claim 26, Khan taught (e.g., see fig. 8) a three dimensional systolic array with connections between processors in three dimensions.

7. As to claim 2-5,27-30 Khan taught the calculation comprising plurality of planes, and grid points and plural time-steps and vectors(e.g., see fig. 8 and col. 12, lines 15-55). As per claim 31, the system taught by Khan shows direct connection between the processing elements in the array and therefore the storing of data to an extrinsic memory (i.e., outside the array) would have been unnecessary when the transfer of data between columns was performed (e.g., see fig. 8).

8. As to the limitations of claims 52 and 53 the reconfigurable systolic processor would have been able to adapt to the application an therefore would have been an adaptive processor. As to the processor comprising a microprocessor one of ordinary skill would have been motivated to implement the systolic processor as described above as an microprocessor at least to take advantage of the reduced cost and reduced system size as was well known in the art at the time of the claimed invention.

9. Claims19,45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Leeland (US patent No. 4,872,133).

10. Leeland taught calculation comprised a financial application modeling using a spreadsheet application (e.g., see col. 5, lines 3-32).

11. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Leeland and Gupta. One of ordinary skill would have been motivated to incorporate the Leeland teaching of financial spreadsheet application for an array processor in order to provide an additional use for the combined system.

12. Claim 10-16 and 36-42,54 rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Benner (US Patent No. 5,072,371).

13. Benner taught the calculation comprising fluid flow calculation and structural analysis (e.g., see col. 22, lines 35-52).

14. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Benner and Gupta. One of ordinary skill would have been motivated to incorporate the Benner teaching of fluid flow and structural analysis applications for an array processor in order to provide an additional uses for the combined system.

15. As to the limitation in claim 54 of performing a calculation unit a variable changed is value in a system processing an restarting at that value The Benner system taught systolically performing calculations on fluid flow. Since in such a problem one of ordinary skill would at times be interested when a change in the data occurred and adjust the calculation to pin point the calculation around that certain point then one of ordinary skill would have been motivated to operate the Benner and Gupta and Khan

system to process systolically until a change in data occurred and then restart the calculation at the point of the change to better determine the magnitude of the change in data.

16. Claim 6-9,25,32-35,51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Helbig (US patent No. 4,962,381).

17. Helbig taught the application of a systolic processor for radar, medical ultrasound and other imaging applications (e.g., see col. 1, lines 1-5) Clearly this would have also comprised images processed by standard MPEG and JPEG standards.

18. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Helbig and Gupta. One of ordinary skill would have been motivated to incorporate the Helbig teaching of radar, medical ultrasound and other imaging applications for an systolic processor in order to provide an additional uses for the combined system.

19. As to the limitation of claims 25 and 51, since signal filtering would have been associated with the applications taught by Helbig such as radar then one of ordinary skill would have been motivated to use the Helbig systolic processor in signal filtering applications.

20. Claim 17,18,22-24,43,44,48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Skaletsky (US patent No. 5,784,108).

21. Skaletsky taught using an systolic processor for processing search algorithm for image search such as when a best match was to be found and clearly this would have been applicable to data mining as these are similar applications (e.g., see col. 3, line 13-col. 4, line 57).

22. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Skaletsky and Gupta. One of ordinary skill would have been motivated to incorporate the Skaletsky teaching of search algorithm applications for an systolic processor in order to provide an additional uses for the combined system.

23. As to the limitations of claims 22-24,48-50 in light of the search algorithm teaching especially for finding a best match for data then the use of systolic processors for similar applications such as the genetic pattern matching, protein folding and organic structure interaction would have been an obvious uses for systolic processors (such as taught by Skaletsky) to one of ordinary skill in the DP art.

24. Claim 20,21,46,47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Gai (US patent No. 6,061,706).

25. Gai taught use of systolic processors in encryption/decryption applications to speed the encryption/decryption of public keys (e.g. see col. 1, lines 25-41.

26. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Gai and Gupta. One of ordinary skill would have been motivated to

incorporate the Gai teaching of encryption and decryption applications for an systolic processor in order to provide an additional uses for the combined system.

27. Claims 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta (US patent No. 6,385,757)

28. Gupta taught the invention substantially as claimed including data processing ("DP") system comprising a reconfigurable processor that provides indication of whether it performs speculative and systolic processing (e.g., see col. 15, lines 6-66). Consequently, one ordinary skill would have been motivated to perform systolic and speculative processing at least in order to utilize the parameters indicated by Gupta for use in systolic and speculative processing (e.g., see col. 15, lines 56-63).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 10/285,318	Applicant(s)/Patent Under Reexamination HUPPENTHAL ET AL.	
	Examiner Eric Coleman	Art Unit 2183	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-4,872,133	10-1989	Leeland, Steven B.	708/509
*	B	US-5,274,832	12-1993	Khan, Emdadur R.	708/424
*	C	US-6,385,757	05-2002	Gupta et al.	716/1
*	D	US-5,072,371	12-1991	Benner et al.	712/11
*	E	US-4,962,381	10-1990	Helbig, Sr., Walter A.	342/372
*	F	US-5,784,108	07-1998	Skaletzky et al.	375/240.15
*	G	US-6,061,706	05-2000	Gai et al.	708/491
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PTO/SB/02a(08/03)
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Application Number	10/285,318
Filing Date	October 31, 2002
First Named Inventor	Jon M. Huppenthal et al.
Art Unit	2121
Examiner Name	Not yet assigned
Attorney Docket No.	SRC015

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Document No. No. – Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EC		US-6,385,757	05/07/2002	Gupta et al.	
EC		US-4,872,133	10/03/1989	Leeland	
EC		US-5,274,832	12/28/1993	Khan	
EC		US-6,072,371	12/10/1991	Benner et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T[6]

EXAMINER SIGNATURE		DATE CONSIDERED	10/2/05

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PTO/SB/08A (10/01) (Substitute for form 1449A/PTO)	ATTY. DOCKET NO. SRC015 Client/Matter No. 80404.0018	APPLICATION NO. 10/285,318
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) Sheet 1 of 4	FIRST NAMED INVENTOR Jon M. Huppenthal and David E. Caliga	
	FILING DATE October 31, 2002	ART UNIT 2121

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document No. No. – Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EC.		US-5,230,057	07/20/93	Shido, et al.	
		US-5,892,962	04/06/99	Cloutier	
		US-5,903,771	05/11/1999	Sgro et al.	Figs 1 & 6, col. 3, lines 30-67, col 4, lines 1-51, col 7, lines 1-27.
		US-6,192,439	02/20/2001	Grunewald et al.	Fig 3, col 3, lines 53-67, col 4, lines 1-64.
		US-6,076,152	06/13/2000	Huppenthal et al.	
		US-6,052,773	04/18/2000	DeHon et al.	
		US-6,226,776	05/01/2001	Panchul et al.	
		US-6,023,755	02/08/2000	Casselman	
		US-5,737,766	04/07/1998	Tan	
EC.		US-5,570,040	10/29/1996	Lytle et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Doc cntry code – No. – Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	TRANSLATION YES	TRANSLATION NO

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher, city and/or country where published
EC.	1	AGARWAL, A., et al., "The Raw Compiler Project", pages 1-12, http://cag-www.lcs.mit.edu/raw, Proceedings of the Second SUIF Compiler Workshop, Augs. 21-23, 1997.
EC.		ALBAHARNA, OSAMA, et al., "On the viability of FPGA-based integrated coprocessors", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 206-215.
EC.		AMERSON, RICK, et al., "Teramac---Configurable Custom Computing", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 32-38.

		BARTHEL, DOMINIQUE August 25-26, 1997, "PVP a Parallel Video coProcessor", Hot Chips IX, Pages 203-210.
		BERTIN, PATRICE, et al., "Programmable active memories: a performance assessment", © 1993 Massachusetts Institute of Technology, Pages 88-102.
		BITTNER, RAY, et al., "Computing kernels implemented with a wormhole RTR CCM", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 98-105.
		BUELL, D., et al. "Splash 2: FPGAs in a Custom Computing Machine – Chapter 1 – Custom Computing Machines: An Introduction", Pages 1-11, http://www.computer.org/espress/catalog/bp07413/spls-ch1.html (originally believed published in J. of Supercomputing, Vol. IX, 1995, PP. 219-230.
		CASSELMAN, STEVEN, "Virtual Computing and The Virtual Computer", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 43-48.
		CHAN, PAK, et al., "Architectural tradeoffs in field-programmable-device-based computing systems", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 152-161.
		CLARK, DAVID, et al., "Supporting FPGA microprocessors through retargetable software tools", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 195-103.
		CUCCARO, STEVEN, et al., "The CM-2X: a hybrid CM-2/Xilink prototype", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 121-130.
		CULBERTSON, W. BRUCE, et al., "Exploring architectures for volume visualization on the Teramac custom computer", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 80-88.
		CULBERTSON, W. BRUCE, et al., "Defect tolerance on the Teramac custom computer", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 116-123.
		DEHON, ANDRE, "DPGA-Coupled microprocessors: commodity IC for the early 21st century", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 31-39.
		DEHON, A., et al., "MATRIX A Reconfigurable Computing Device with Configurable Instruction Distribution", Hot Chips IX, August 25-26, 1997, Stanford, California, MIT Artificial Intelligence Laboratory.
		DHAUSSY, PHILIPPE, et al., "Global control synthesis for an MIMD/FPGA machine", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 72-81.
		ELLIOTT, DUNCAN, et al., "Computational Ram: a memory-SIMD hybrid and its application to DSP", © 1992 IEEE, Publ. No. 0-7803-0246-X/92, Pages 30.6.1-30.6.4.
		FORTES, JOSE, et al., "Systolic arrays, a survey of seven projects", © 1987 IEEE, Publ. No. 0018-9162/87/0700-0091, Pages 91-103.
		GOKHALE, M., et al., "Processing in Memory: The Terasys Massively Parallel PIM Array" © April 1995, IEEE, Pages 23-31.
		GUNTHER, BERNARD, et al., "Assessing Document Relevance with Run-Time Reconfigurable Machines", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 10-17.
		HAGIWARA, HIROSHI, et al., "A dynamically microprogrammable computer with low-level parallelism", © 1980 IEEE, Publ. No. 0018-9340/80/07000-0577, Pages 577-594.
	✓	HARTENSTEIN, R. W., et al. "A General Approach in System Design Integrating Reconfigurable Accelerators," http://xputers.informatik.uni-kl.de/papers/paper026-1.html, IEEE 1996 Conference, Austin, TX, Oct. 9-11, 1996.
		HARTENSTEIN, REINER, et al., "A reconfigurable data-driven ALU for Xputers", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 139-146.
		HAUSER, JOHN, et al.: "GARP: a MIPS processor with a reconfigurable co-processor", © 1997 IEEE, Publ. No. 0-08186-8159-4/97, Pages 12-21.
		HAYES, JOHN, et al., "A microprocessor-based hypercube, supercomputer", © 1986 IEEE, Publ. No. 0272-1732/86/1000-0006, Pages 6-17.
		HERPEL, H.-J., et al., "A Reconfigurable Computer for Embedded Control Applications", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 111-120.
		HOGL, H., et al., "Enable++: A second generation FPGA processor", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 45-53.
EC		KING, WILLIAM, et al., "Using MORRPH in an industrial machine vision system". © 1996 IEEE, Publ. No. 08186-7548-9/96, Pages 18-26.

			MANOHAR, SWAMINATHAN, et al., "A pragmatic approach to systolic design", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0463, Pages 463-472.
			MAUDUIT, NICOLAS, et al., "Lneuro 1.0: a piece of hardware LEGO for building neural network systems," © 1992 IEEE, Publ. No. 1045-9227/92, Pages 414-422.
		✓	MIRSKY, ETHAN A., "Coarse-Grain Reconfigurable Computing", Massachusetts Institute of Technology, June 1996.
		✓	MIRSKY, ETHAN, et al., "MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 157-166.
			MORLEY, ROBERT E., Jr., et al., "A Massively Parallel Systolic Array Processor System", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0217, Pages 217-225.
		✓	PATTERSON, DAVID, et al., "A case for intelligent DRAM: IRAM", Hot Chips VIII, August 19-20, 1996, Pages 75-94.
		✓	PETERSON, JANES, et al., "Scheduling and partitioning ANSI-C programs onto multi-FPGA CCM architectures", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 178-187.
		✓	SCHMIT, HERMAN, "Incremental reconfiguration for pipelined applications," © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 47-55.
		✓	SITKOFF, NATHAN, et al., "Implementing a Genetic Algorithm on a Parallel Custom Computing Machine", Publ. No. 0-8186-7086-X/95, Pages 180-187.
			STONE, HAROLD, "A logic-in-memory computer", © 1970 IEEE, IEEE Transactions on Computers, Pages 73-78, January 1990.
			TANGEN, UWE, et al., "A parallel hardware evolvable computer POLYP extended abstract", © 1997 IEEE, Publ. No. 0-8186-8159/4/97, Pages 238-239.
			THORNBURG, MIKE, et al., "Transformable Computers", © 1994 IEEE, Publ. No. 0-8186-5602-6/94, Pages 674-679.
			TOMITA, SHINJI, et al., "A computer low-level parallelism QA-2", © 1986 IEEE, Publ. No. 0-0384-7495/86/0000/0280, Pages 280-289.
			TRIMBERGER, STEVE, et al., "A time-multiplexed FPGA", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 22-28.
			UEDA, HIROTADA, et al., "A multiprocessor system utilizing enhanced DSP's for image processing", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0611, Pages 611-620.
			VILLASENOR, JOHN, et al., "Configurable computing", © 1997 Scientific American, June 1997.
			WANG, QUIANG, et al., "Automated field-programmable compute accelerator design using partial evaluation", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 145-154.
			W.H. Mangione-Smith and B.L. Hutchings. Configurable computing: The Road Ahead. In Proceedings of the Reconfigurable Architectures Workshop (RAW'97), pages 81-96, 1997.
			WIRTHLIN, MICHAEL, et al., "The Nano processor: a low resource reconfigurable processor", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 23-30.
			WIRTHLIN, MICHAEL, et al., "A dynamic instruction set computer", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 99-107.
			WITTIG, RALPH, et al., "One Chip: An FPGA processor with reconfigurable logic", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 126-135.
			YAMAUCHI, TSUKASA, et al., "SOP: A reconfigurable massively parallel system and its control-data flow based compiling method", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 148-156.
			"Information Brief", PCI Bus Technology, © IBM Personal Computer Company, 1997, Pages 1-3.
			YUN, HYUN-KYU AND SILVERMAN, H. F.; "A distributed memory MIMD multi-computer with reconfigurable custom computing capabilities", Brown University, 10-13 Dec. 1997, pp. 7-13.
			HOOVER, CHRIS AND HART, DAVID; "San Diego Supercomputer Center, Timelogic and Sun Validate Ultra-Fast Hidden Markov Model Analysis-One DeCypher-accelerated Sun Fire 6800 beats 2,600 CPUs running Linux-", San Diego Supercomputer Center, http://www.sdsc.edu/Press/02/050802_markovmodel.html, May 8, 2002, pp. 1-3.
			CALIGA, DAVID AND BARKER, DAVID PETER, "Delivering Acceleration: The Potential for Increased HPC Application Performance Using Reconfigurable Logic", SRC Computers, Inc., November 2001, pp. 20.
EC			HAMMES, J.P., RINKER, R. E., MCCLURE, D. M., BÖHM, A. P. W., NAJJAR, W. A., "The SA-C Compiler Dataflow Description", Colorado State University, June 21, 2001, pp. 1-25.