

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICROSOFT CORPORATION,  
Petitioner,

v.

SAINT REGIS MOHAWK TRIBE,  
Patent Owner.

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Cases IPR2018-01605, IPR2018-01606, and IPR2018-01607  
Patent 7,620,800 B2

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Before KALYAN K. DESHPANDE, JUSTIN T. ARBES, and  
CHRISTA P. ZADO, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

DECISION  
Institution of *Inter Partes* Review  
35 U.S.C. § 314(a)

## I. INTRODUCTION

Petitioner Microsoft Corporation filed three Petitions requesting *inter partes* review of claims 1–5, 7–9, 15, 17, 18, and 20–24 of U.S. Patent No. 7,620,800 B2 (Ex. 1005, “the ’800 patent”) pursuant to 35 U.S.C. § 311(a). Patent Owner Saint Regis Mohawk Tribe filed a Preliminary Response pursuant to 35 U.S.C. § 313 in each proceeding. Pursuant to our authorization, Petitioner also filed a Reply and Patent Owner filed a Sur-Reply in each proceeding, as listed in the following chart.<sup>1</sup>

Case Number	Challenged Claims	Petition	Preliminary Response	Reply	Sur-Reply
IPR2018-01605	1, 8, 9, and 20	Paper 1 (“Pet.”)	Paper 15 (“Prelim. Resp.”)	Paper 19 (“Reply”)	Paper 20 (“Sur-Reply”)
IPR2018-01606	1, 7, 15, 17, and 24	Paper 1 (“-1606 Pet.”)	Paper 16 (“-1606 Prelim. Resp.”)	Paper 20	Paper 21
IPR2018-01607	1–5, 18, and 21–23	Paper 1 (“-1607 Pet.”)	Paper 15 (“-1607 Prelim. Resp.”)	Paper 19	Paper 20

Pursuant to 35 U.S.C. § 314(a), the Director may not authorize an *inter partes* review unless the information in the petition and preliminary response “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons that follow, we institute an *inter partes* review as to claims 1–5, 7–9, 15, 17, 18, and 20–24 of the ’800 patent on all grounds

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<sup>1</sup> Unless otherwise noted with the prefix “-1606” or “-1607,” references herein are to the exhibits filed in Case IPR2018-01605.

of unpatentability asserted in the Petitions. Claims 2–5, 7–9, 15, 17, 18, and 20–24 depend from claim 1, and, therefore, analysis of each dependent claim requires the same analysis of independent claim 1. To administer the proceedings more efficiently, we also exercise our authority under 35 U.S.C. § 315(d) to consolidate the three proceedings and conduct the proceedings as one trial. *See also* 37 C.F.R. § 42.122(a) (“Where another matter involving the patent is before the Office, the Board may during the pendency of the *inter partes* review enter any appropriate order regarding the additional matter including providing for the stay, transfer, consolidation, or termination of any such matter.”).

## II. BACKGROUND

### A. *The ’800 Patent*

The ’800 patent<sup>2</sup> discloses “multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions.” Ex. 1005, col. 1, ll. 40–43. Parallel processing “allows multiple processors to work simultaneously on the same problem to achieve a solution” in less time than it would take a single processor. *Id.* at col. 1, ll. 44–49. “[A]s more and more performance is required, so is more parallelism, resulting in ever larger systems” and associated difficulties, including “facility requirements, power, heat generation and reliability.” *Id.* at col. 1, ll. 53–61. The ’800 patent discloses that

if a processor technology could be employed that offers orders of magnitude more parallelism per processor, these systems

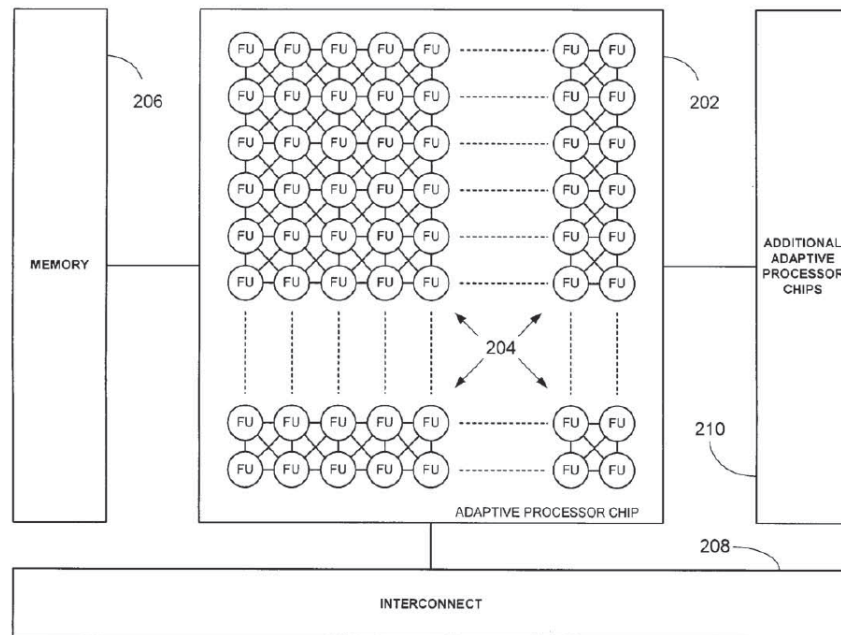
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<sup>2</sup> The ’800 patent is a continuation of U.S. Patent No. 7,225,324 B2 (Ex. 1001, “the ’324 patent”), challenged by Petitioner in Cases IPR2018-01601, IPR2018-01602, and IPR2018-01603.

could be reduced in size by a comparable factor. Such a processor or processing element is possible through the use of a reconfigurable processor. Reconfigurable processors instantiate only the functional units needed to solve a particular application, and as a result, have available space to instantiate as many functional units as may be required to solve the problem up to the total capacity of the integrated circuit chips they employ.

*Id.* at col. 1, l. 65–col. 2, l. 7. The '800 patent describes a known issue where each processor in a multi-processor system is allocated a portion of a problem called a “cell” and “to solve the total problem, results of one processor are often required by many adjacent cells because their cells interact at the boundary.” *Id.* at col. 2, ll. 26–32. Passing intermediate results around the system to complete the problem requires using “numerous other chips and busses that run at much slower speeds than the microprocessor,” diminishing performance. *Id.* at col. 2, ll. 32–38, col. 5, ll. 16–28, Fig. 1 (depicting a conventional multi-processor arrangement). In an adaptive processor-based system, however, “any boundary data that is shared between . . . functional units need never leave a single integrated circuit chip,” reducing “data moving around the system” and improving performance. *Id.* at col. 2, ll. 39–49.

Figure 2 of the '800 patent is reproduced below.



200 **Fig. 2**

Figure 2 is “a functional block diagram of an adaptive processor 200 communications path for implementing the technique of the present invention.” *Id.* at col. 5, ll. 29–32. Adaptive processor 200 includes adaptive processor chip 202, which is coupled to memory element 206, interconnect 208, and additional adaptive processor chips 210. *Id.* at col. 5, ll. 32–37. Adaptive processor chip 202 includes thousands of functional units (“FU”) 204 interconnected by “reconfigurable routing resources” inside adaptive processor chip 202, allowing functional units 204 to “exchange data at much higher data rates and lower latencies than a standard microprocessor.” *Id.* at col. 5, ll. 39–45.

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