

THE HONORABLE JAMES L. ROBART

1  
2  
3  
4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26

**IN THE UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF WASHINGTON  
AT SEATTLE**

SRC LABS, LLC & SAINT REGIS  
MOHAWK TRIBE,

*Plaintiffs,*

v.

MICROSOFT CORPORATION,

*Defendant.*

CASE NO. 2:18-cv-00321-JLR

**DECLARATION OF TAREK EL-  
GHAZAWI**

DECLARATION OF TAREK EL-GHAZAWI  
CASE NO. 2:18-CV-321-JLR-1

**KELLER ROHRBACK. L.L.P.**  
1201 THIRD AVENUE, SUITE 3200  
SEATTLE, WA 98101-3053  
TELEPHONE: (206) 623-1900  
FACSIMILE: (206) 623-3384

1  
2  
3  
4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26

**I. INTRODUCTION**

1. I have been asked by counsel for Plaintiffs to provide opinions regarding how one of ordinary skill in the art would have understood certain claim terms at issue in this lawsuit.

2. All of the opinions stated in this report are based on my current personal knowledge and professional judgment. If called as a witness during the trial in this matter, I am prepared to testify competently about them.

3. I am being compensated for my work in this matter but my compensation does not depend on the opinions I render or the outcome of this litigation. I do not have a personal interest in the outcome of this litigation.

**II. QUALIFICATIONS**

4. My *curriculum vitae* is attached as Exhibit A. A summary of my qualifications relevant to this case is provided below.

5. I am a Professor of Electrical and Computer Engineering at The George Washington University (GWU), I have created the NSF Industry/University Center for High-Performance Reconfigurable Computing at GWU and directed it for about ten years, I have led many industry and federally funded research projects in reconfigurable computing and published closed to three hundred research publications. I received many honors in my field, a few examples follow. I was elected an IEEE Fellow for my contributions to reconfigurable computing and parallel programming (only one in a thousand members get that honor) and was awarded the Alexander von Humboldt research award for the same reasons (100 scientists selected from around the world in any year by the Humboldt Foundation in Germany), I am a

---

DECLARATION OF TAREK EL-GHAZAWI  
CASE No. 2:18-CV-321-JLR-2

**KELLER ROHRBACK. L.L.P.**  
1201 THIRD AVENUE, SUITE 3200  
SEATTLE, WA 98101-3053  
TELEPHONE: (206) 623-1900  
FACSIMILE: (206) 623-3384

1 distinguished speaker for the IEEE Computer Society and served as a distinguished visiting  
2 fellow for the UK Royal Academy of Engineering.

3 **III. BASIS OF OPINIONS**

4 6. My opinions are abased on my years of education, research, experience, as well as my  
5 reading of the patents and prosecution histories. In forming my opinions I have considered the  
6 materials identified in this declaration, the patents, and the file histories.

7 7. I may rely on additional materials and provide additional opinions to respond to  
8 arguments raised by the Defendants.

9 8. This declaration only represents the opinions I have formed to date. I reserve the right to  
10 revise, supplement, or amend my opinions based on new information and my continuing  
11 analysis of the patents.

12 **IV. BACKGROUND OF THE TECHNOLOGY**

13 **A. Traditional Computers**

14 9. Conventional computers, also known as von Neumann machine or von Neumann  
15 Computers. In a traditional computer, hardware is fixed and cannot be changed after  
16 manufacturing while different software programs use the existing fixed hardware to perform  
17 the required application. The software program is simply a sequence of instructions. Both the  
18 software program and the data to operate on reside in the main memory and therefore the  
19 processor is connected to the main memory through bus lines that include data bus and address  
20 bus. The address bus specifies the address of the memory location where the instruction to be  
21 performed or the operand to be manipulated reside. The data bus is used to transfer the  
22 instruction and input data to the processor and take the results back from the processor to the  
23  
24  
25  
26

DECLARATION OF TAREK EL-GHAZAWI  
CASE NO. 2:18-CV-321-JLR-3

**KELLER ROHRBACK. L.L.P.**  
1201 THIRD AVENUE, SUITE 3200  
SEATTLE, WA 98101-3053  
TELEPHONE: (206) 623-1900  
FACSIMILE: (206) 623-3384

1 memory. The processor typically goes through a fixed routine of steps to execute the  
2 instructions of the software program one by one, this routine is called the instruction execution  
3 cycle. The typical steps for such an instruction execution are: Instruction Fetch; Instruction  
4 Decode; Execute; Data Memory Access; and Write back the result.

5 10. Conventional computers suffer many inherent limitations: 1. Their architectural is fixed  
6 (rigid) and cannot be configured; 2. Their architectures is complex to satisfy all general  
7 computations; and 3. They operate in a sequential many. Applications needs and  
8 computations required can however change. Conventional processors will have to use the  
9 available chip resources to execute those computation. This is by contrast to FPGAs that are  
10 malleable and allow customization to create just as needed simple compute architectures and  
11 create as many of those as needed to solve the problem at hand.

### 13 **B. FPGAs**

14 11. An FPGA, or a Field Programmable Gate Array, is an electronic chip that can be  
15 programmed and reprogrammed in the field of application, after manufacturing, to provide  
16 different functionalities as needed. To do so, FPGAs are largely comprising configurable  
17 logical blocks that can be configured to perform the desired logical functions and a set of  
18 connecting configurable interconnects. Configurations are established by a bit stream that is  
19 generated by application engineers using some form of programming interface.

### 21 **C. Relevant Advanced Computing Concepts History of Heterogeneous Computers**

22 12. Many architectural enhancements were developed and leveraged over the years  
23 sometimes as a concept utilized internally to enhance the conventional architectures or to be  
24 used externally to provide computing acceleration. Among these concepts that are relevant  
25

1 here are array processing/spatial parallelism, pipelining, systolic arrays, data flow  
2 architectures, vector processors and heterogeneous (accelerated) computing.

3 13. Array Processing/Spatial Parallelism- when the underlying has a great deal of data  
4 parallelism, in other words multiple data items that need to be processed in the same way at  
5 the same time, this parallelism can be exploited to speed up the computation. In conventional  
6 processors only if multiple independent processing units are available they can be used up to  
7 the available fixed number of such units. In the case of FPGAs, as many units as needed by the  
8 application are created and used thereby enabling better unitization of the chip and a much  
9 more speed of processing.  
10

11 14. Dataflow Processing: This is a form of processing which is data driven, where rather  
12 than executing instructions one by one from the program as in traditional systems (control  
13 flow), activities are executed when their input data are received.  
14

15 15. Pipelining: Pipelining is a form of overlapped processing established by breaking the  
16 processor needed for a computation into physical modules, called stages that correspond to the  
17 subtasks that make up that overall computation. Computations that correspond to different  
18 data can be processed concurrently one by each different stage to gain speed. In conventional  
19 processors a pipeline can be used for instruction processing and a fixed number of pipelines can  
20 be available for arithmetic.  
21

22 16. Systolic Arrays: A systolic arrays is a homogeneous array of interconnected processing  
23 elements to perform synchronized processing of data as they proceed in a wave-front style  
24 through the array. An analogy between the data movement and the blood circulation in the  
25 body is the basis for the name.  
26

DECLARATION OF TAREK EL-GHAZAWI  
CASE NO. 2:18-CV-321-JLR-5

**KELLER ROHRBACK. L.L.P.**  
1201 THIRD AVENUE, SUITE 3200  
SEATTLE, WA 98101-3053  
TELEPHONE: (206) 623-1900  
FACSIMILE: (206) 623-3384

# Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

## Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

## Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

## Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

## API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

## LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

## FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

## E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.