



[54] INTERMEDIATE-GRAIN RECONFIGURABLE PROCESSING DEVICE

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[52] U.S. Cl. 395/800.15; 395/653

[58] Field of Search 395/800.1, 800.15, 395/200.51, 280, 653

[56] References Cited

U.S. PATENT DOCUMENTS

4,597,041	6/1986	Guyer et al.	364/200
4,748,585	5/1988	Chiarulli et al.	364/900
4,754,412	6/1988	Deering	364/736
4,858,113	8/1989	Saccardi	364/200
4,870,302	9/1989	Freeman	307/465
4,873,626	10/1989	Gifford	364/200
5,020,059	5/1991	Gorin et al.	371/11.3
5,233,539	8/1993	Agrawal et al.	364/489
5,239,654	8/1993	Ing-Simmons et al.	395/800
5,241,635	8/1993	Papadopoulos et al.	395/375
5,265,207	11/1993	Zak	395/200.31
5,301,340	4/1994	Cook	395/800
5,305,462	4/1994	Grondalski	395/800.1
5,336,950	8/1994	Popli et al.	307/465
5,426,378	6/1995	Ong	326/39
5,457,644	10/1995	McCollum	364/716
5,684,980	11/1997	Casselman	395/500

OTHER PUBLICATIONS

Takashi Miyamori et al., "A Quantitative Analysis of Reconfigurable Coprocessors for Multimedia Applications," IEEE Symposium on Field-Programmable Custom Computing Machines Conference (FCCM98), Apr. 15-17, 1998.

Charlé Rupp et al., "The Napa Adaptive Processing Architecture", IEEE Symposium on Field-Programmable Custom Computing Machines Conference (FCCM98), Apr. 15-17, 1998, pp. 1-10.

Stephen M. Scalera et al., The Design and Implementation of a Context Switching FPGA, IEEE Symposium on Field-Programmable Custom Computing .

T. Bridges, "The GPA Machine: A Generally Partitionable MSIMD Architecture," Third Symposium on the Frontier of Massively Parallel Computation Proceedings IEEE pp. 196-203 (1990).

P. Clarke, "Pilington Preps Reconfigurable Video DSP," News (Aug. 7, 1995).

D.C. Chen, et al., "A Reconfigurable Multiprocess IC for Rapid Prototyping of Algorithmic-Specific High-Speed DSP Data Paths," IEEE Journal of Solid-State Circuits, vol. 27 (12): 1895-1904 (Dec 1992).

A.K. Yeung, et al., "TA 6.3: A 2.4GOPS Data-Given Reconfigurable Multiprocessor IC for DSP," IEEE International Solid-State Circuits Conference, pp. 108-109, 346 (1995).

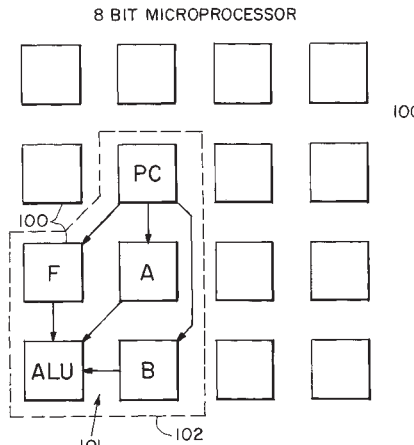
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[57] ABSTRACT

A programmable integrated circuit utilizes a large number of intermediate-grain processing elements which are multibit processing units arranged in a configurable mesh. The coarse-grain resources, such as memory and processing, are deployable in a way that takes advantage of the opportunities for optimization present in given problems. To accomplish this, the interconnect supports three different modes of operation: a static value in which a value set by the configuration data is provided to a functional unit, static source in which another functional unit serves as the value source, and a dynamic source mode in which the source is determined by the value from another functional unit.

31 Claims, 20 Drawing Sheets



OTHER PUBLICATIONS

- J.E. Brewer, et al., "A Monolithic Processing Subsystem," *IEEE Transactions on Components, Packaging, and Manufacturing Technology—Part B*, vol. 17(3) :310–317 (Aug. 1994).
- I. Gilbert, Chapter 11—Mesh Multiprocessing, *The Lincoln Laboratory Journal*, 1(1) :11.1–11.18 (Spring 1988).
- Ira H. Gilbert, et al., "The Monolithic Synchronous Processor," *Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02173* (No Date Given).
- G. Masera, et al., "A Microprogrammable Parallel Architecture for DSP," *IEEE*, pp. 824–827, (1991).
- L. Wang, et al., "Distributed Instruction Set Computer," *Proceedings of the 1988 International Conference on Parallel Processing*, vol. 1, pp. 426–429.
- M. Sowa, et al., "Parallel Execution on the Function-Partitioned Processor with Multiple Instruction Streams," *Systems and Computers in Japan*, 22(4) :22–27 (Nov. 1991).
- T. Alexander, et al., "A Reconfigurable Approach to a Systolic Sorting Architecture," *IEEE*, pp. 1178–1182 (1989).
- Z. Blazek, et al., "Design of a Reconfigurable Parallel RISC-Machine," *North-Holland Microprocessing and Microprogramming 21*, pp. 39–46, (1987).
- S. Morton, et al., "The Dynamically Reconfigurable CAP Array Chip I," *IEEE Journal of Solid-State Circuits*, SC21 (5) :820–826 (Oct. 1986).
- L. Snyder, "A Taxonomy of Synchronous Parallel Machines," *Proceedings of the 1988 International Conference on Parallel Processing*, pp. 281–285 (Aug. 1988).
- L. Snyder, "An Inquiry into the Benefits of Multigauge Parallel Computation," *Proceedings of the 1985 International conference on Parallel Processing*, pp. 488–492 (Aug. 1985).
- A. DeHon, "DPGA Utilization and Application," *FPGA '96—ACM/SIGDA Fourth International Symposium on FPGAs, Monterey, CA* (Feb. 11–13, 1996).
- D. Epstein, "Chromatic Raises the Multimedia Bar," *Microprocessor Report*, pp. 23–27 (Oct. 23, 1995).
- J. Labrousse, et al., "Create-Life: A Modular Design Approach for High Performance ASIC's," *IEEE CH2843*, pp. 427–433 (Jan. 1990).
- M. Slater, "MicroUnity Lift Veil on MediaProcessor," *Microprocessor Report*, pp. 11–18 (Oct. 23, 1995).
- E. Tau, et al., "A First Generation DPGA Implementation," *FPD '95—Third Canadian Workshop of Field-Programmable Devices Montreal, Canada* (May 29–Jun. 1, 1995).
- S. Kartashev, et al., "A Multicomputer System with Dynamic Architecture," *IEEE Transactions on Computers*, vol. C-28, No. 10, pp. 704–721 (Oct. 1979).
- D. Bursky, "Programmable Data Paths Speed Computations," *Electronic Design*, pp. 171–174 (May 1, 1995).
- V. Bove, Jr., et al., "Cheops: A Reconfigurable Data-Flow System for Video Processing," *IEEE Transactions on Circuits and Systems for Video Technology*, pp. 140–149 (1995).
- M. Schaffner, "Processing by Data and Program Blocks," *Transactions on Computers*, vol. C-27, No. 11, pp. 1015–1027 (Nov. 1978).
- J. Nickolls, "The Design of the MasPar MP-1: A Cost Effective Massively Parallel Computer," *IEEE CH2843*, pp. 25–28 (Jan. 1990).
- B. Narasimha, "Performance-Oriented, Fully Routable Dynamic Architecture for a Field Programmable Logic Device," *UCB/ERL M93/42, University of California, Berkeley*, pp. 1–21 (Jun. 1993).
- M. Bolotski, et al., "A 1024 Processor 8ns SIMD Array," *Advanced Research in VLSI 1995*, pp. 1–13 (1995).
- D. Cherepacha, et al., "A Datapath Oriented Architecture for FPGAs," *Second International ACM/SIGDA Workshop on Field Programmable Gate Arrays ACM*, pp. 1–11 (Feb. 1994).
- D. Jones, et al., "A Time-Multiplexed FPGA Architecture for Logic Emulation," *Proceedings of the IEEE 1995 Custom Integrated Circuits Conference*, pp. 495–498 (May 1995).
- G. Nutt, "Microprocessor Implementation of a Parallel Processor," *Proceedings of the Fourth Annual Symposium on Computer Architecture*, pp. 147–152, (1977).
- W. Kim, "MasPar MP-2 PE Chip: A Totally Cool Hot Chip," *Proceedings of Hot Chips V*, pp. 1–5 (Mar. 29, 1993).
- E. Mirsky, et al., "Matrix: Coarse-Grain Reconfigurable Computing (Abstract)," *Published at the 5th Annual MIT Student Workshop on Scalable Computing*, pp. 1–2 (Aug. 1995) (Available on the Internet May 1, 1995).
- E. Mirsky, et al., "Matrix: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources," *Published at FCCM'96—IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 1–10 (Apr. 17–19, 1996).

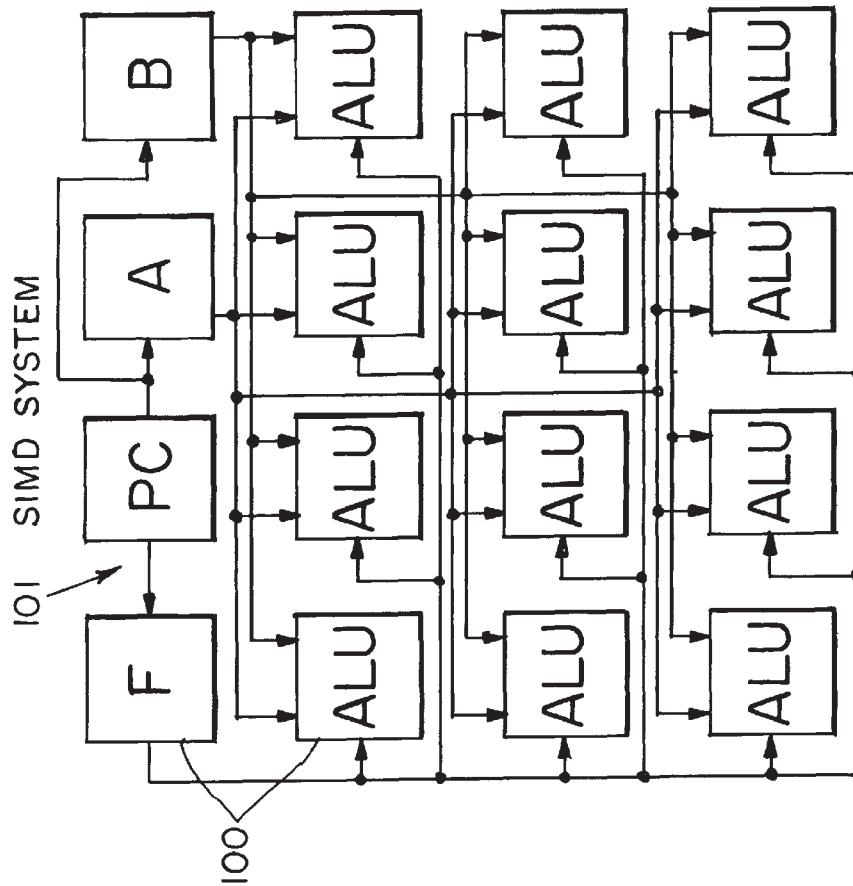


FIG. 1

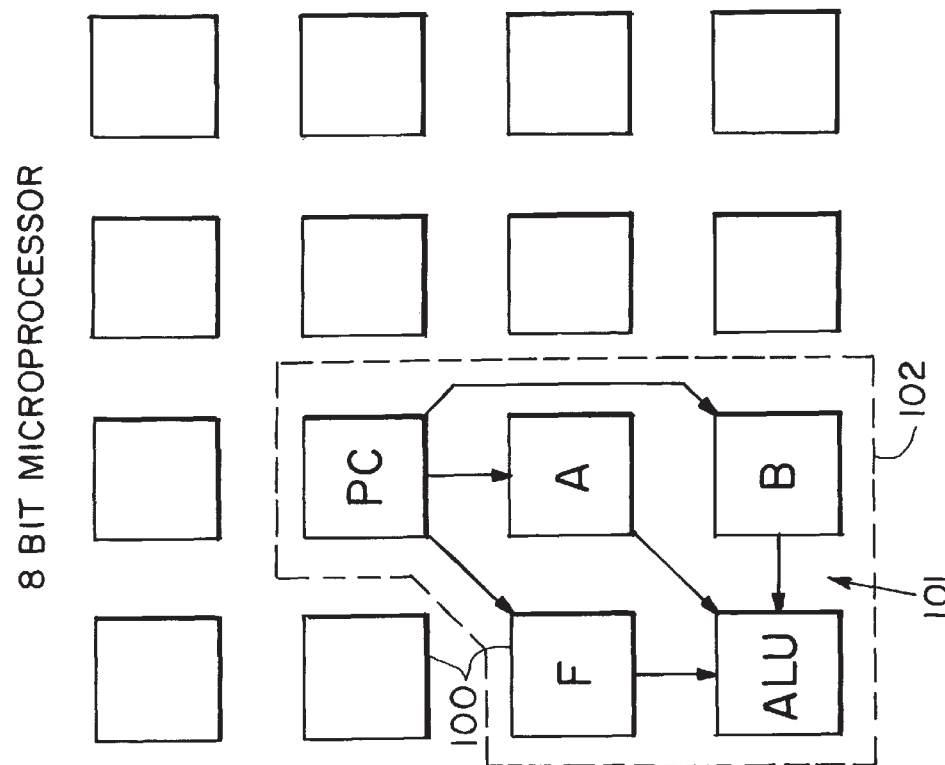


FIG. 2

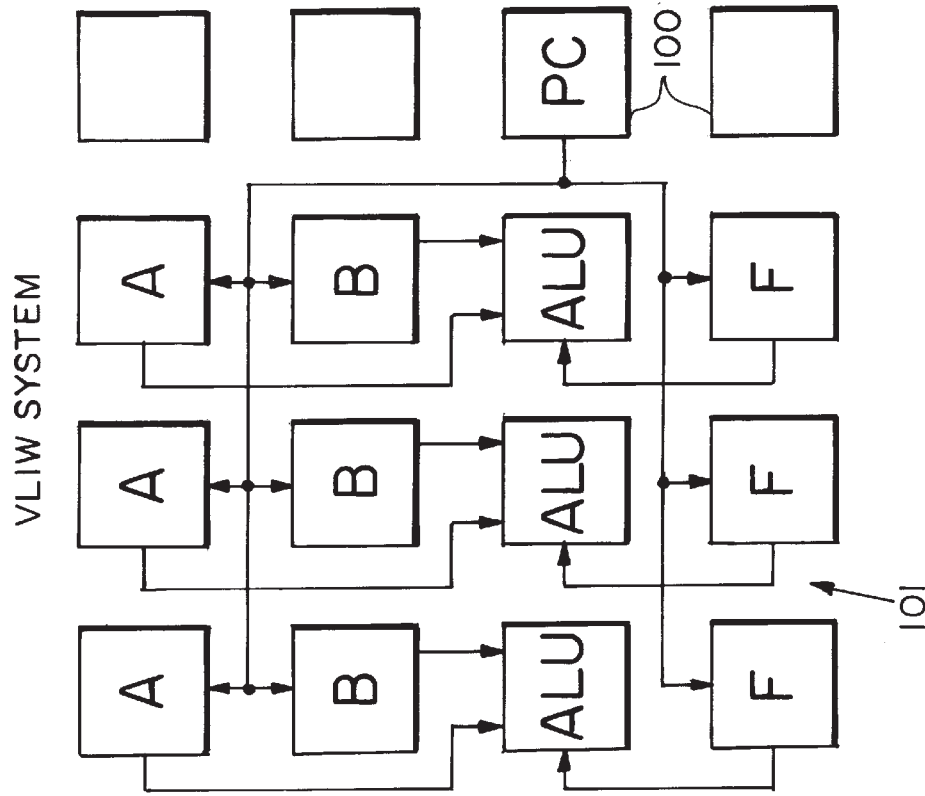


FIG. 4

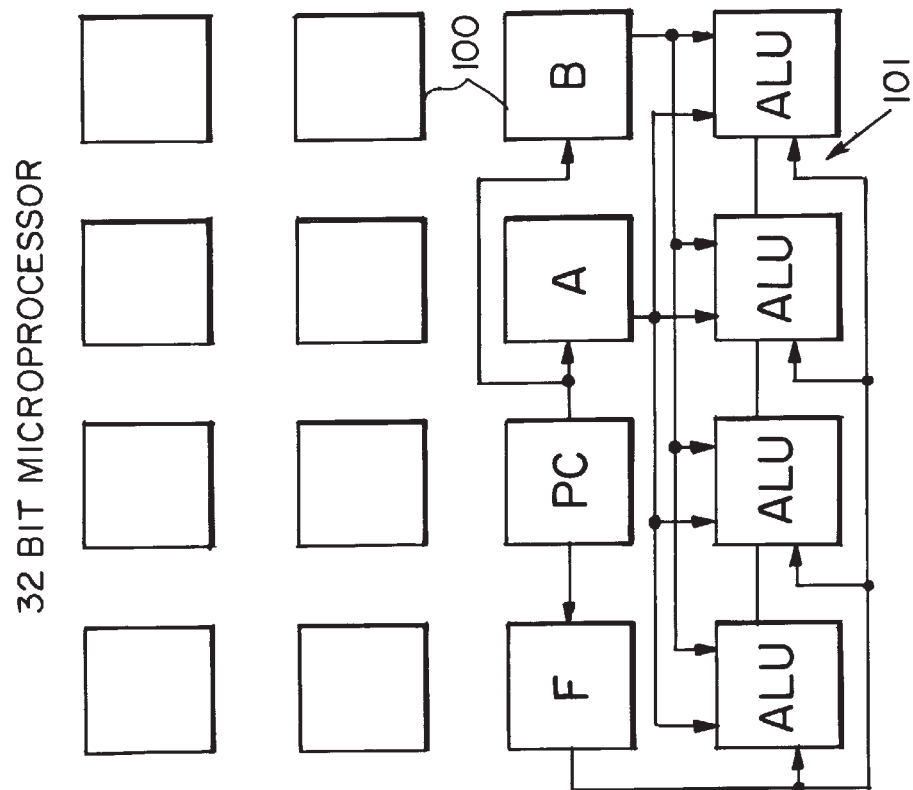


FIG. 3

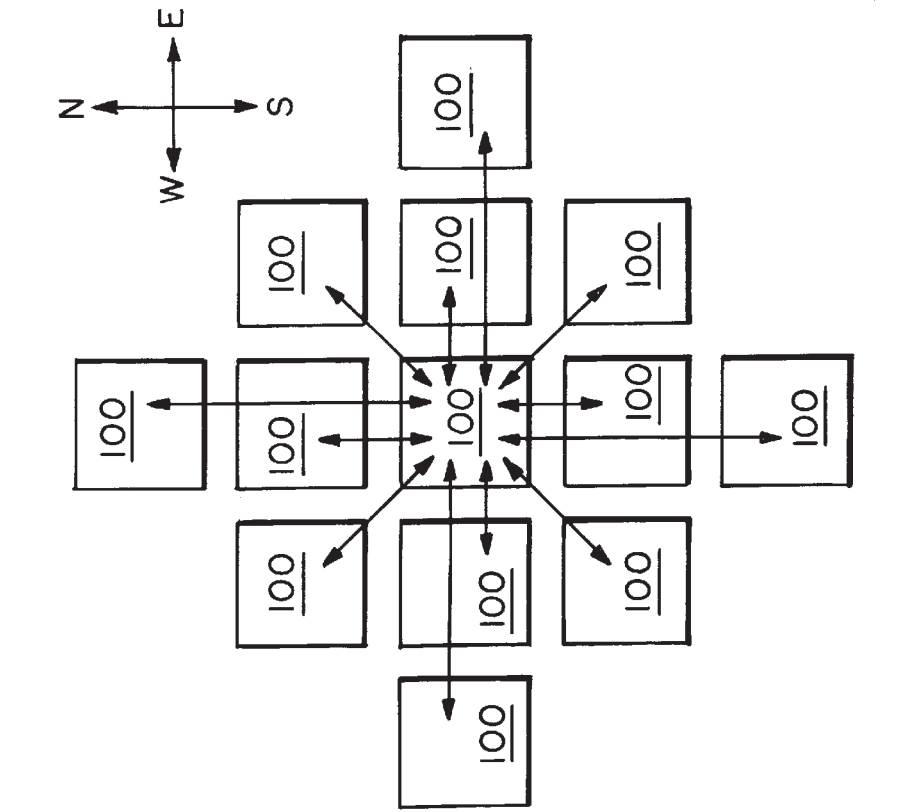


FIG. 7

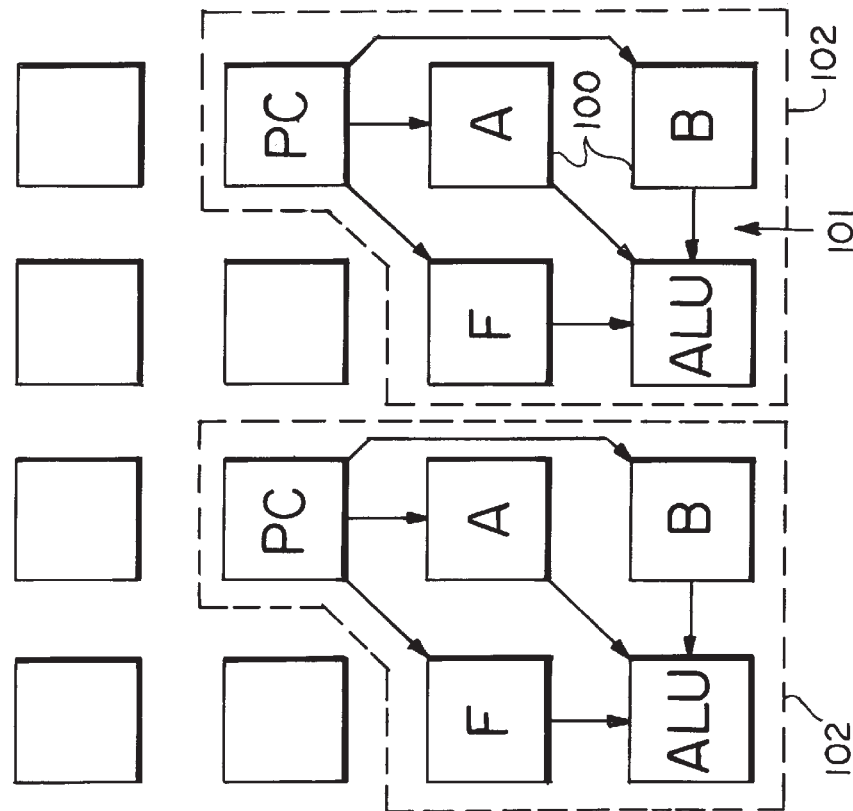


FIG. 5

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