UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF WASHINGTON
AT SEATTLE

SRC LABS, LLC & SAINT REGIS MOHAWK TRIBE, Plaintiffs, v. AMAZON WEB SERVICES, INC., AMAZON.COM, INC., & VADATA, INC., Defendants.	Case No. 2:18-cv-00317-JLR JURY TRIAL DEMANDED

PRELIMINARY NON-INFRINGEMENT AND INVALIDITY CONTENTIONS OF DEFENDANTS AMAZON WEB SERVICES, INC., AMAZON.COM, INC. AND VADATA, INC.

Pursuant to the Court's Minute Order Setting Trial Dates and Related Dates (Dkt. No. 95) and Local Patent Rule 121, defendants Amazon Web Services, Inc., Amazon.com, Inc., and VADATA, Inc. (collectively, "Amazon") provide the following preliminary non-infringement and invalidity contentions to plaintiffs SRC Labs, LLC and Saint Regis Mohawk Tribe (collectively, "SRC") regarding the currently asserted claims of U.S. Patent Nos. 7,149,867 (the "'867 patent"), 7,225,324 (the "'324 patent"), 7,620,800 (the "'800 patent") and 9,153,311 (the "'311 patent") (collectively, the "asserted patents"). Although in its complaint, SRC also asserted U.S. Patent No. 6,434,687 (the "'687 patent"), SRC did not include any infringement allegations for the '687 patent in its infringement contentions, and indeed, did not even mention the '687 patent in those contentions. Accordingly, because it is no longer at issue in this case, Amazon does not provide its preliminary invalidity and non-infringement contentions for the '687 patent herein. Amazon expressly reserves the right to provide its preliminary invalidity and non-infringement contentions for the '687 patent in the event the Court grants SRC leave to amend its infringement contentions to re-assert the '687 patent.

These preliminary contentions are based on Amazon's present understanding of SRC's interpretation of the claims of the asserted patents as advanced by SRC in its preliminary infringement contentions served on June 15, 2018. Nothing in these preliminary contentions should be regarded as necessarily reflecting the proper interpretation of the claims or an interpretation of the claims Amazon agrees with or proposes. Amazon disputes SRC's apparent claim interpretations and intends to propose alternative constructions.

Amazon hereby incorporates all prior art references, charts, theories, and disclosures served on SRC in any prior or pending court action or proceeding before the Patent Trial and Appeal Board involving any of the asserted patents, including without limitation, *SRC Labs, LLC*

et al. v. Microsoft Corp., No. 2:18-cv-00321 (W.D. Wash.).

To the extent additional information regarding SRC's infringement contentions becomes available, Amazon anticipates that it will provide corresponding invalidity contentions which establish that SRC's interpretation of the claims is disclosed by prior art.

Amazon reserves the right to amend these contentions based on information learned in its continuing investigation, new developments in the case, or other circumstances.

I. NON-INFRINGEMENT CLAIM CHARTS

Pursuant to Local Patent Rule 121(a), Amazon has attached as Exhibit A claim charts stating, on an element-by-element basis, why the accused products do not infringe the asserted claims based on Amazon's current understanding of SRC's infringement allegations. The bases identified in the claim charts are not intended to be exhaustive, and are based on SRC's mapping of the accused products in its preliminary infringement contentions. Amazon reserves the right to identify additional non-infringement defenses and theories as the case progresses and also in the event SRC modifies its infringement theory.

II. IDENTIFICATION OF PRIOR ART

The following list identifies each item of prior art, patent, or publication, that anticipates each asserted claim or renders it obvious.

A. Prior Art Patents

Patent Number	Country of Origin	Filing or Priority Date	Date of Issue or Publication	Short Cite
4,698,751	U.S.	July 13, 1984	Oct. 6, 1987	Parvin
5,361,367	U.S.	June 10, 1991	Nov. 1, 1994	Fijany
5,757,959	U.S.	Apr. 5, 1995	May 26, 1998	Lopresti
6,182,206 B1	U.S.	Apr. 17, 1997	Jan. 30, 2001	Baxter
6,119,200	U.S.	Aug. 18, 1998	Sept. 12, 2000	George
6,675,187 B1	U.S.	June 10, 1999	Jan. 6, 2004	Greenberger
6,438,747 B1	U.S.	Aug. 20, 1999	Aug. 20, 2002	Schreiber
7,139,743 B2	U.S.	Apr. 7, 2000	Nov. 21, 2006	Indeck
6,822,959 B2	U.S.	July 31, 2000	Nov. 23, 2004	Galbi

Patent Number	Country of Origin	Filing or Priority Date	Date of Issue or Publication	Short Cite
6,662,285 B1	U.S.	Jan. 9, 2001	Dec. 9, 2003	Douglass
6,981,099 B2	U.S.	Dec. 16, 2002	Dec. 27, 2005	Paulraj
7,055,016 B2	U.S.	Apr. 30, 2003	May 30, 2006	Phelps
7,836,331 B1	U.S.	May 15, 2007	Nov. 16, 2010	Totolos
8,683,166 B1	U.S.	Jan. 31, 2009	Mar. 25, 2014	Flateau
8,476,926 B2	U.S.	Sept. 29, 2009	June 10, 2014	Brunham

B. Prior Art Publications

Title	Date of Publication	Author/Publisher	Short Cite
Building and Using a Highly Parallel Programmable Logic Array	Jan. 1991	Maya Gokhale et al.	Splash
Searching Genetic Databases on Splash 2	1993	Dzung T. Hoang	Hoang
Mapping Nested Loops to Field Programmable Gate Array Based Systems	1995	John Spillane et al.	Spillane
Splash 2: FPGAs in a Custom Computing Machine	1996	D.A. Buell, J. M. Arnold, and W. J. Kleinfelder	Buell
PCI-based WILDFIRE Reconfigurable Computing Engines	October 21, 1996	B. K. Fross et al.	Fross
Architectural Adaptation for Application-Specific Locality Optimizations	1997	Xingbin Zhang et al.	Zhang
Memory Access Schemes for Configurable Processors	2000	Holger Lange et al.	Lange
Artificial Neural Network Implementation on a single FPGA of a Pipelined On-Line Backpropagation	Sept. 2000	Rafael Gadea et al.	Gadea
An FPGA Implementation of Walsh-Hadamard Transforms for Signal Processing	2001	A. Amira et al.	Amira
Evaluation of the Streams-C C-to-FPGA Compiler: An Applications Perspective	February 2001	J. Frigo et al.	Streams-C
An FPGA Implementation of Triangle Mesh Decompression	2002	Tulika Mitra	Mitra
U.S. Patent Application Publication No. 2003/0200382 A1	Oct. 23, 2003	Owen Newton Wells et al.	Wells
U.S. Patent Application Publication No. 2004/0034732 A1	Feb. 19, 2004	Steven J. Valin et al.	Valin
Suzaku Hardware Manual (V. 1.0.4)	December 14, 2004	Atmark Techno, Inc.	Suzaku

Title	Date of Publication	Author/Publisher	Short Cite
System- and application-level support for runtime hardware reconfiguration on SoC platforms	2006	Dimitris Syrivelis and Spyros Lalis	Syrivelis
JEDEC Standard	November 2008	JEDEC Solid State Technology Association	JEDEC
DDR I/II DRAM Controller Core, Atria Logic Inc. Product Information Sheet	2009	Atria Logic Inc.	Atria
Spartan-6 FPGA Memory Controller User Guide	Aug. 9, 2010	Xilinx	Spartan-6 User Guide
DD2SOFT; DDR2 Memory Controller; VHDL Source Code Overview	September. 22, 2010	ComBlock	ComBlock
External Memory Interface Handbook Volume 3: Section III. DDR2 and DDR3 SDRAM Controller with UniPHY User Guide	June 2011	Altera	UniPHY
U.S. Patent Application Publication No. 2011/0264934 A1	Oct. 27, 2011	Branover et al.	Branover
ZedBoard Brochure	2012	Zedboard	ZedBoard Brochure
Zynq-7000 All Programmable SoC Technical Reference Manual	Feb. 11, 2014	Xilinx	Zynq Manual
U.S. Patent Application Publication No. 2014/0043918 A1	Feb. 13, 2014	Jackson L. Ellis et al.	Ellis

C. Prior Art Systems/Services

System/Service	Relevant Dates	Persons/Entities Involved in Prior Use, Sale, and/or Offers for Sale	Short Cite
Splash 2	At least as early as 1991	Splash 2 was designed, developed, used, advertised, published, and also offered for sale and/or sold to its customers this system as evidenced at least by the documents identified herein.	Splash 2
Atria DDR I/II DRAM Controller Core	At least as early as 2009	Atria Logic, Inc. designed, developed, used, advertised, published, and also offered for sale and/or sold	Atria

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