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DeHon et al.

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[54] **INTERMEDIATE-GRAIN RECONFIGURABLE PROCESSING DEVICE**

[75] Inventors: **André DeHon**; **Ethan Mirsky**, both of Cambridge; **Thomas F. Knight, Jr.**, Belmont, all of Mass.

[73] Assignee: **Massachusetts Institute of Technology**, Cambridge, Mass.

[21] Appl. No.: **08/632,371**

[22] Filed: **Apr. 11, 1996**

[51] **Int. Cl.**[6] **G06F 15/80**

[52] **U.S. Cl.** **395/800.15**; 395/653

[58] **Field of Search** 395/800.1, 800.15, 395/200.51, 280, 653

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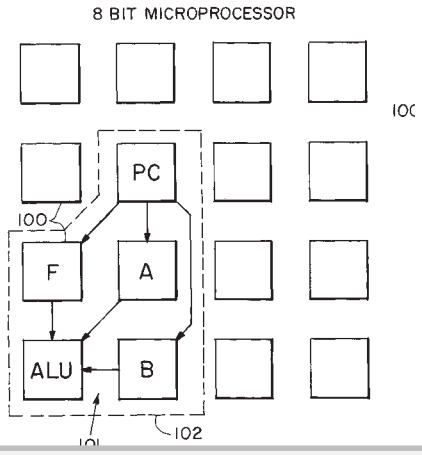
Primary Examiner—Eric Coleman

Attorney, Agent, or Firm—Hamilton, Brook, Smith & Reynolds, P.C.

[57] **ABSTRACT**

A programmable integrated circuit utilizes a large number of intermediate-grain processing elements which are multibit processing units arranged in a configurable mesh. The coarse-grain resources, such as memory and processing, are deployable in a way that takes advantage of the opportunities for optimization present in given problems. To accomplish this, the interconnect supports three different modes of operation: a static value in which a value set by the configuration data is provided to a functional unit, static source in which another functional unit serves as the value source, and a dynamic source mode in which the source is determined by the value from another functional unit.

31 Claims, 20 Drawing Sheets



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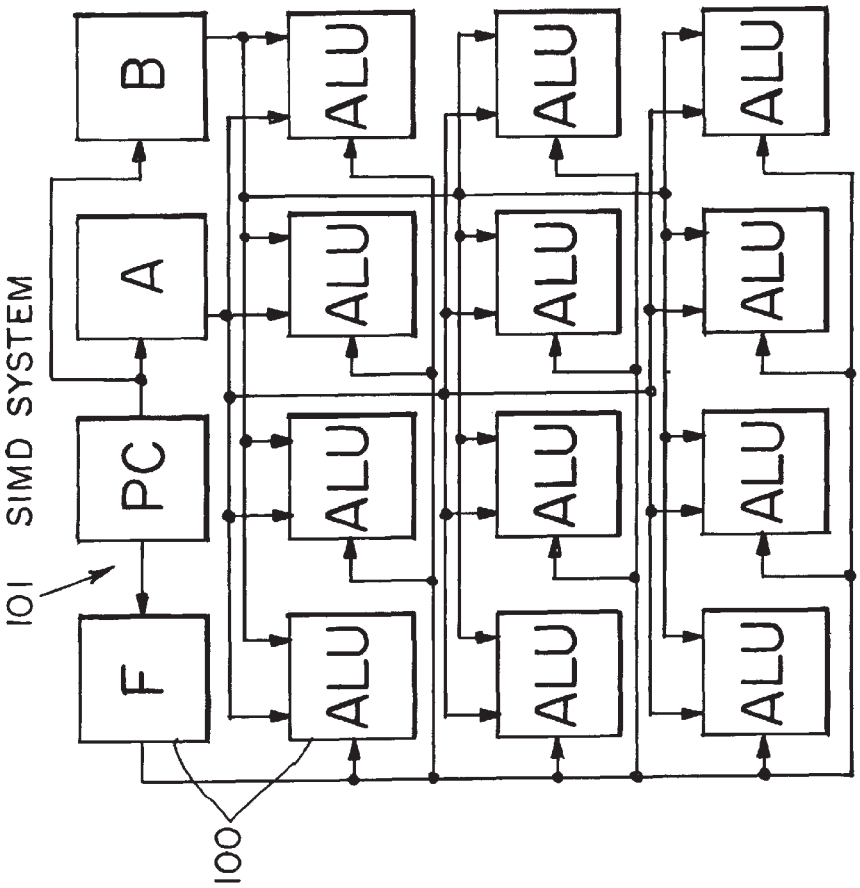

FIG. 2

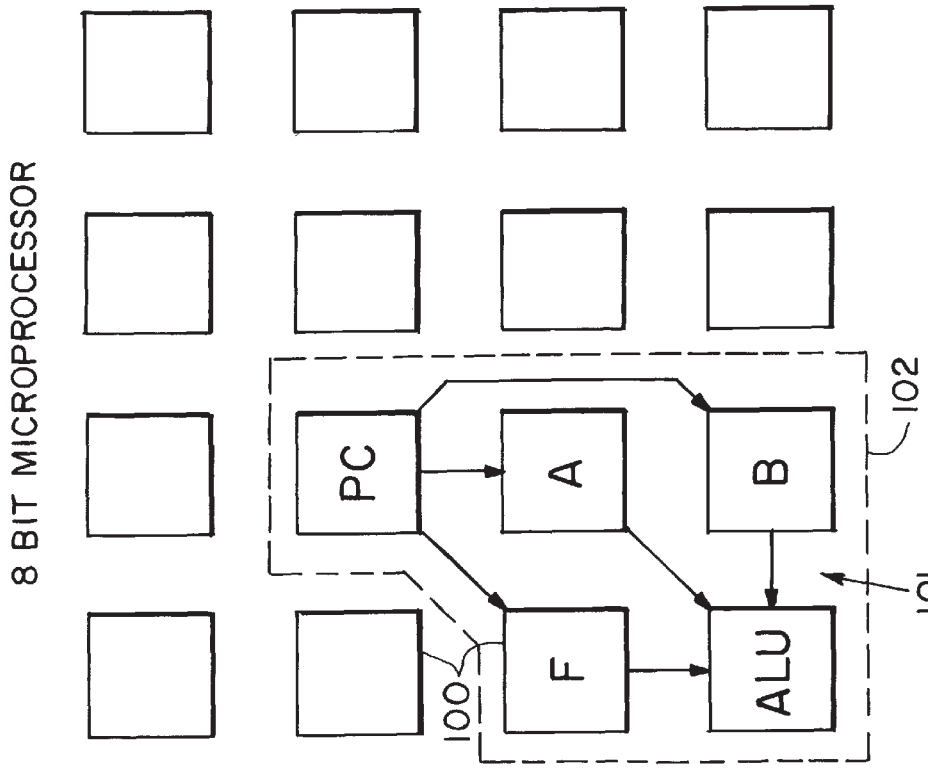

FIG. 1

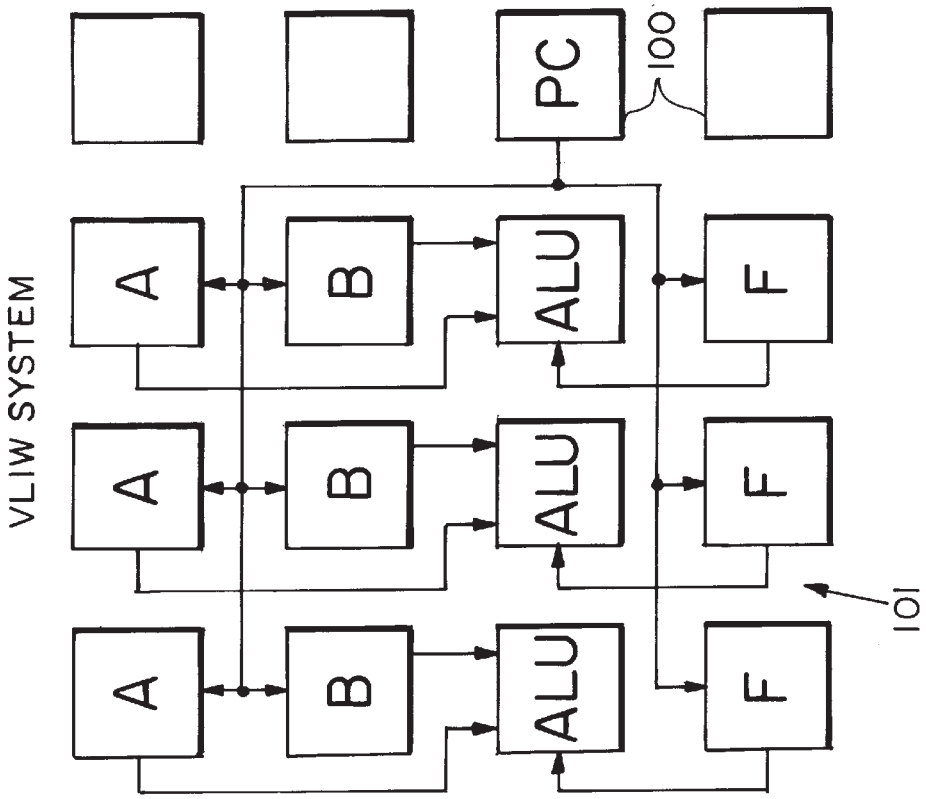

FIG. 4

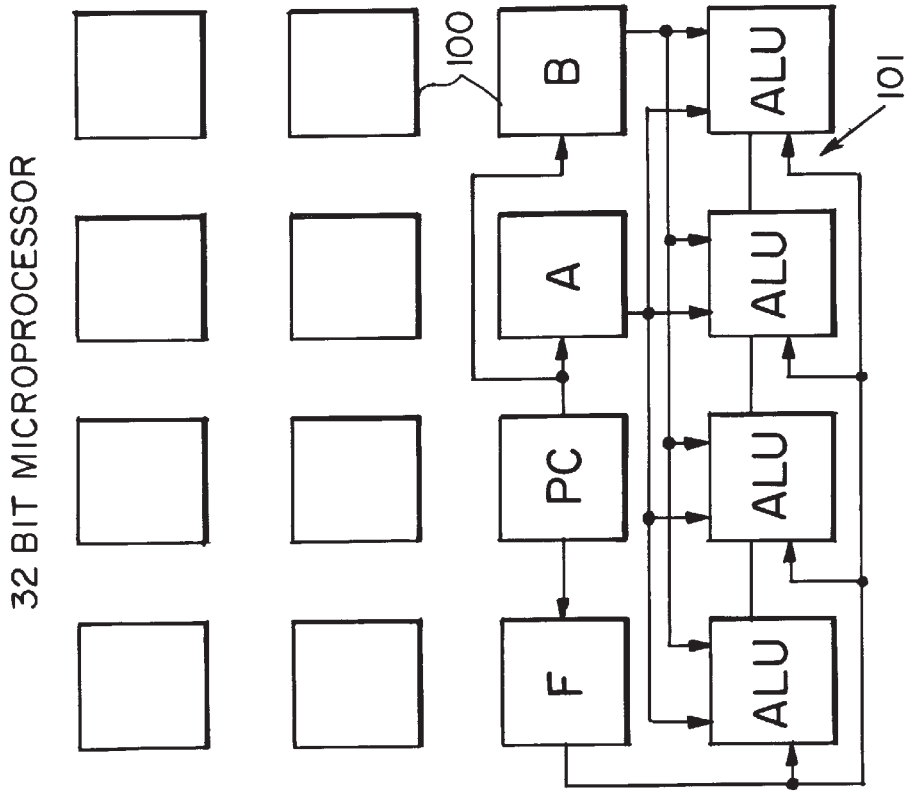

FIG. 3

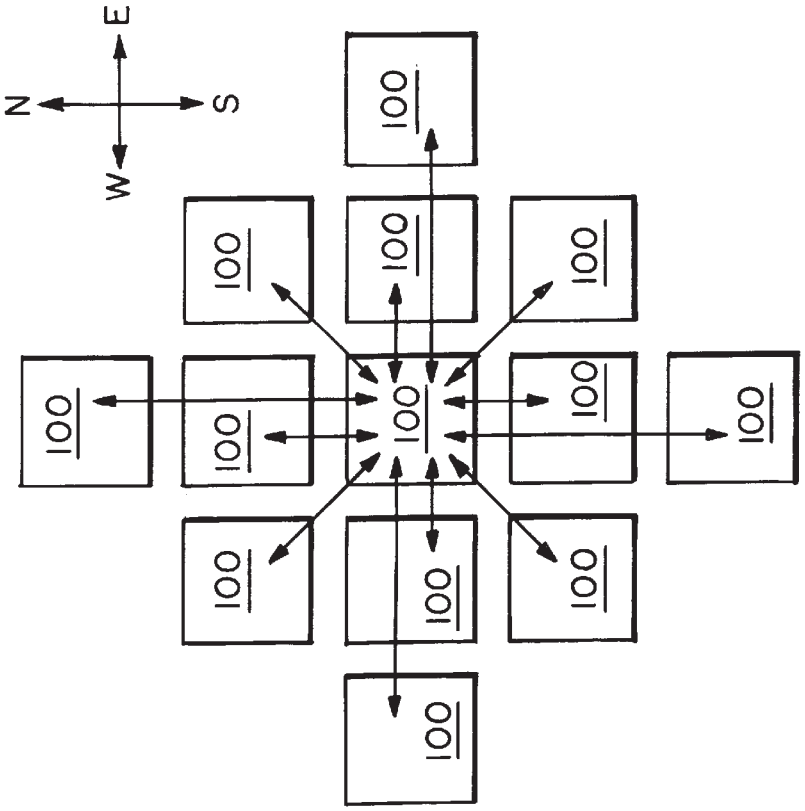

FIG. 7

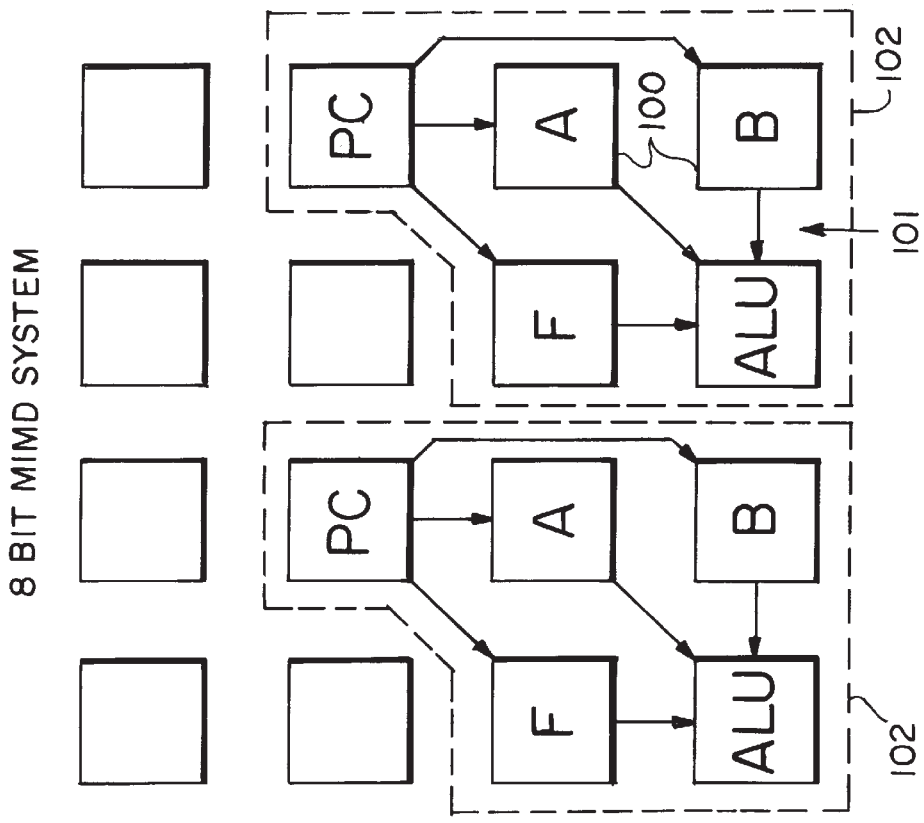

FIG. 5

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