



US006434687B1

(12) **United States Patent**
Huppenthal

(10) **Patent No.:** **US 6,434,687 B1**
(45) **Date of Patent:** **Aug. 13, 2002**

(54) **SYSTEM AND METHOD FOR ACCELERATING WEB SITE ACCESS AND PROCESSING UTILIZING A COMPUTER SYSTEM INCORPORATING RECONFIGURABLE PROCESSORS OPERATING UNDER A SINGLE OPERATING SYSTEM IMAGE**

(75) Inventor: **Jon M. Huppenthal**, Colorado Springs, CO (US)

(73) Assignee: **SRC Computers, Inc.**, Colorado Springs, CO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/888,276**

(22) Filed: **Jun. 22, 2001**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/563,561, filed on May 3, 2000, now Pat. No. 6,339,819, which is a continuation-in-part of application No. 09/481,902, filed on Jan. 12, 2000, now Pat. No. 6,247,110, which is a continuation of application No. 08/992,763, filed on Dec. 17, 1997, now Pat. No. 6,076,152.

(51) **Int. Cl.**⁷ **G06F 15/16**

(52) **U.S. Cl.** **712/32; 707/501.1; 707/513; 709/203; 709/219**

(58) **Field of Search** **707/501.1, 513; 709/203, 219; 712/32**

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,671,377	A	*	9/1997	Bleidt et al.	345/723
5,715,453	A	*	2/1998	Stewart	707/513
5,867,706	A	*	2/1999	Martin et al.	709/105
5,987,480	A	*	11/1999	Donohue et al.	707/501
6,009,410	A	*	12/1999	LeMole et al.	705/14
6,128,663	A	*	10/2000	Thomas	709/228

OTHER PUBLICATIONS

Albaharna, Osama, et al., "On the viability of FPGA-based integrated coprocessors", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, pp. 206-215.

Barthel, Dominique Aug. 25-26, 1997, "PVP a Parallel Video coProcessor", Hot Chips IX, pp. 203-210.

Bittner, Ray, et al., "Computing kernels implemented with a wormhole RTR CCM", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, pp. 98-105.

Babb, Jonathan, et al., "Parallelizing applications into silicon", © 1999 IEEE.

Bertin, Patrice, et al., "Programmable active memories: a performance assessment", © 1993 Massachusetts Institute of Technology, pp. 88-102.

Culbertson, W. Bruce, et al., "Exploring architectures for volume visualization on the Teramac custom computer", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, pp. 80-88.

Culbertson, W. Bruce, et al., "Defect tolerance on the Teramac custom computer", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, pp. 116-123.

(List continued on next page.)

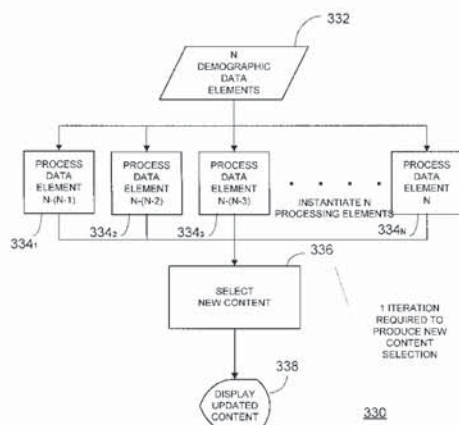
Primary Examiner—Kenneth S. Kim

(74) *Attorney, Agent, or Firm*—William J. Kubida; Hogan & Hartson LLP

(57) **ABSTRACT**

A system and method for accelerating web site access and processing utilizing a multiprocessor computer system incorporating reconfigurable and standard microprocessors as the web site server. One or more reconfigurable processors may be utilized, for example, in accelerating site visitor demographic data processing, real time web site content updating, database searches and other processing associated with e-commerce applications. In a particular embodiment disclosed, all of the reconfigurable and standard microprocessors may be controlled by a single system image of the operating system, although cluster management software may be utilized to cause a cluster of microprocessors to appear to the user as a single copy of the operating system.

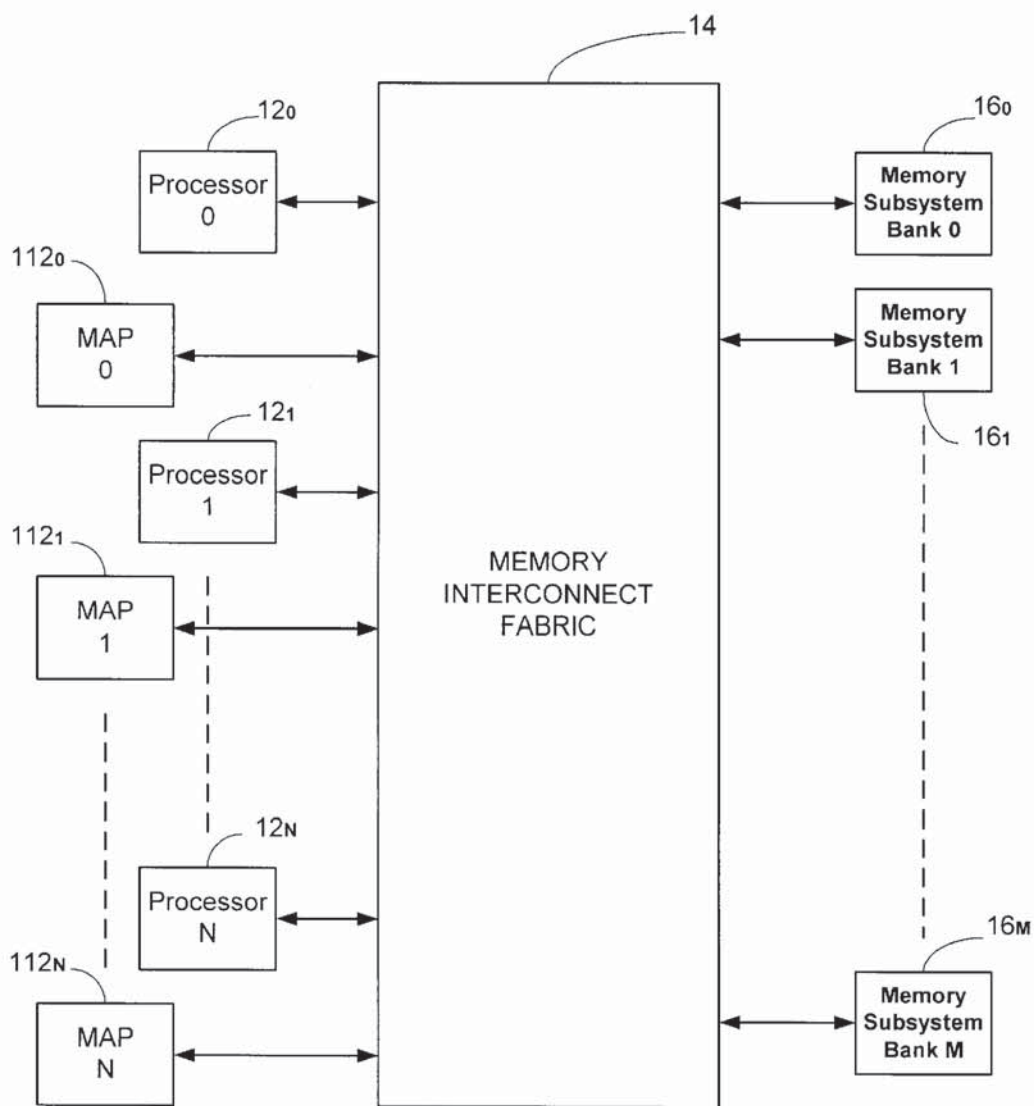
25 Claims, 14 Drawing Sheets



OTHER PUBLICATIONS

- Chan, Pak, et al., "Architectural tradeoffs in field-programmable-device-based computing systems", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, pp. 152-161.
- Clark, David, et al., "Supporting FPGA microprocessors through retargetable software tools", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, pp. 195-103.
- Cuccaro, Steven, et al., "The CM-2X: a hybrid CM-2/Xilinx prototype", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, pp. 121-130.
- Dehon, Andre, "DPGA-Coupled microprocessors: commodity IC for the early 21st century", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, pp. 31-39.
- Dhaussy, Philippe, et al., "Global control synthesis for an MIMD/FPGA machine", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, pp. 72-81.
- Deshpande, Deepali, et al., "Hybrid data/configuration caching for striped FPGAs" © 1999 IEEE.
- Elliott, Duncan, et al., "Computational Ram: a memory-SIMD hybrid and its application to DSP", © 1992 IEEE, Publ. No. 0-7803-0246-X/92, pp. 30.6.1-30.6.4.
- Fortes, Jose, et al., "Systolic arrays, a survey of seven projects", © 1987 IEEE, Publ. No. 0018-9162/87/0700-0091, pp. 91-103.
- Purna, Karthikeya, et al., "Temporal partitioning and scheduling data flow graphs for reconfigurable computers", © 1999 IEEE, Publ. No. 0018-9340/99 pp. 579-590.
- Gibbs, W. Wayt, "Blitzing bits", © 1999 Scientific American Presents, pp. 57-61.
- Gonzalez, Ricardo, "Configurable and extensible processors change system design", Aug. 15-17, 1999, Hot Chips 11 Tutorials, pp. 135-146.
- Graham, Paul, et al., "FPGA-based sonar processing", © 1998 ACM 0-89791-978-5/98, pp. 201-208.
- Hauser, John, et al.: "GARP: a MIPS processor with a reconfigurable co-processor", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, pp. 12-21.
- Hammond, Lance, et al., "The Stanford Hydra CMP", Aug. 15-17, 1999 Hot Chips 11 Tutorials, pp. 23-31.
- Hartenstein, Reiner, et al., "A reconfigurable data-driven ALU for Xputers", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, pp. 139-146.
- Hayes, John, et al., "A microprocessor-based hypercube, supercomputer", © 1986 IEEE, Publ. No. 0272-1732/86/1000-0006, pp. 6-17.
- Hagiwara, Hiroshi, et al., "A dynamically microprogrammable computer with low-level parallelism", © 1980 IEEE, Publ. No. 0018-9340/80/07000-0577, pp. 577-594.
- Hasebe, A., et al., "Architecture of SIPS, a real time image processing system," © 1988 IEEE, Publ. No. CH2603-9/88/0000/0621, pp. 621-630.
- Jean, Jack, et al., "Dynamic reconfiguration to support concurrent applications", © 1999 IEEE, Publ. No. 0018-9340/99, pp. 591-602.
- Kastrup, Bernardo, et al., "Concise: a compiler-driven CPLD-based instruction set accelerator", © 1999 IEEE.
- King, William, et al., "Using MORRPH in an industrial machine vision system", © 1996 IEEE, Publ. No. 08186-7548-9/96, pp. 18-26.
- Manohar, Swaminathan, et al., "A pragmatic approach to systolic design", © 1988 IEEE, Publ. No. CH2603-9/88-0000/0463, pp. 463-472.
- Motomura, Masato, et al., "An embedded DRAM-FPGA chip with instantaneous logic reconfiguration", © 1998 IEEE, Publ. No. 0-8186-8900-5/98, pp. 264-266.
- McConnell, Ray, "Massively parallel computing on the FUZION chip", Aug. 15-17, 1999, Hot Chips 11 Tutorials, pp. 83-94.
- McShane, Erik, et al., "Functionally integrated systems on a chip: technologies, architectures, CAD tools, and applications", © 1998 IEEE, Publ. No. 8-8186-8424-0/98, pp. 67-75.
- Mauduit, Nicolas, et al., "Lneuro 1.0: a piece of hardware LEGO for building neural network systems," © 1992 IEEE, Publ. No. 1045-9227/92 pp. 414-422.
- Patterson, David, et al., "A case for intelligent DRAM: IRAM", Hot Chips VIII, Aug. 19-20, 1996, pp. 75-94.
- Peterson, Janes, et al., "Scheduling and partitioning ANSI-C programs onto multi-FPGA CCM architectures", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, pp. 178-187.
- Rupp, Charley, et al., "The NAPA adaptive processing architecture", © 1998 the Authors, pp. 1-10.
- Saito, Osamu, et al., "A 1M synapse self learning digital neural network chip", © 1998 IEEE, Publ. No. 0-7803-4344/1/98, pp. 94-95.
- Schott, Brian, et al., "Architectures for system-level applications of adaptive computing", © 1999 IEEE.
- Schmit, Herman, "Incremental reconfiguration for pipelined applications," © 1997 IEEE, Publ. No. 0-8186-8159-4/97, pp. 47-55.
- Villasenor, John, et al., "Configurable computing", © 1997 Scientific American, Jun. 1997.
- Stone, Harold, "A logic-in-memory computer", © 1970 IEEE, IEEE Transactions on Computers, pp. 73-78, Jan. 1990.
- Trimberger, Steve, et al., "A time-multiplexed FPGA", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, pp. 22-28.
- Thornburg, Mike, et al., "Transformable Computers", © 1994 IEEE, Publ. No. 0-8186-5602-6/94, pp. 674-679.
- Tangen, Uwe, et al., "A parallel hardware evolvable computer POLYP extended abstract", © 1997 IEEE, Publ. No. 0-8186-8159/4/97, pp. 238-239.
- Tomita, Shinji, et al., "A computer low-level parallelism QA-2", © 1986 IEEE, No. 0-0384-7495/86/0000/0280, pp. 280-289.
- Ueda, Hirotada, et al., "A multiprocessor system utilizing enhanced DSP's for image processing", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0611, pp. 611-620.
- Wang, Quiang, et al., "Automated field-programmable compute accelerator design using partial evaluation", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, pp. 145-154.
- Wirthlin, Michael, et al., "The Nano processor: a low resource reconfigurable processor", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, pp. 23-30.
- Wittig, Ralph, et al., "One Chip: An FPGA processor with reconfigurable logic", © 1996 IEEE, Publ. No. 0-8186-7458-9/96, pp. 126-135.
- Wirthlin, Michael, et al., "A dynamic instruction set computer", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, pp. 99-107.
- Yamauchi, Tsukasa, et al., "SOP: A reconfigurable massively parallel system and its control-data flow based compiling method", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, pp. 148-156.

- Mencer, Oskar, et al., "PAM-Blox: High Performance FPGA Design for Adaptive Computing", © 1998 IEEE, Conference Paper, INSPEC Abstract Nos. B9811-1265B-044, C9811-5210-009.
- Miyamori, Takashi, et al., "A quantitative analysis of reconfigurable coprocessors for multimedia applications", © 1998 IEEE, Conference Paper, INSPEC Abstract Nos. B9811-1265F-011, C9811-5310-010.
- W.H. Mangione-Smith and B.L. Hutchings. Configurable computing: The Road Ahead. In Proceedings of the Reconfigurable Architectures Workshop (RAW'97), pp. 81-96, 1997.
- Mirsky, Ethan A., "Coarse-Grain Reconfigurable Computing", Massachusetts Institute of Technology, Jun. 1996.
- Vemuri, Ranga R. et al., "Configurable Computing: Technology and Applications", Apr. 2000, Computer, pp. 39-40.
- DeHon, Andre, "The Density Advantage of Configurable Computing", Apr. 2000, Computer, pp. 41-49.
- Haynes, Simon D. et al., "Video Image Processing with the Sonic Architecture", Apr. 2000, Computer, pp. 50-57.
- Platzner, Marco, "Reconfigurable Accelerators for Combinatorial Problems", Apr. 2000, Computer, pp. 58-60.
- Callahan, Timothy J. et al., "The Garp Architecture and C Compiler", Apr. 2000, Computer, pp. 62-69.
- Goldstein, Seth Copen et al., "PipeRench: A Reconfigurable Architecture and Compiler", Apr. 2000, Computer, pp. 70-76.
- * cited by examiner



10

Fig. 1

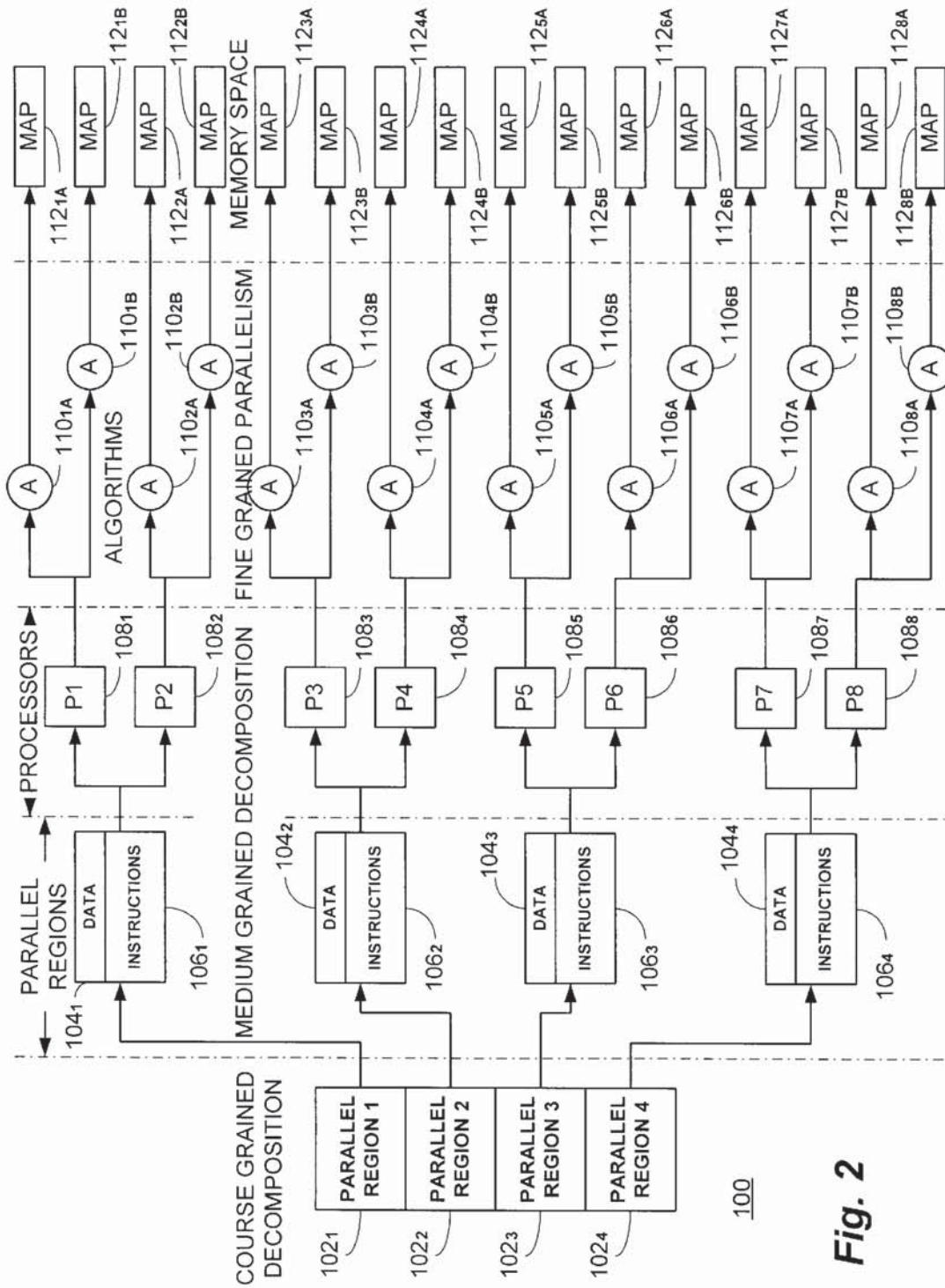


Fig. 2

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.