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# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	SRC015
First Inventor	Jon M. Huppenthal et al.
Title	MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONALS FUNCTIONS
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In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. NEW

Filed: Herewith

For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

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MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

## CROSS REFERENCE TO RELATED PATENT APPLICATIONS

The present invention is related to the subject matter of United States Patent Application Ser. No. 09/755,744 filed January 5, 2001 for: "Multiprocessor 5 Computer Architecture Incorporating a Plurality of Memory Algorithm Processors in the Memory Subsystem" and is further related to the subject matter of United States Patent No. 6,454,687 for: "System and Method for Accelerating Web Site Access and Processing Utilizing a Computer System Incorporating 10 Reconfigurable Processors Operating Under a Single Operating System Image", all of which are assigned to SRC Computers, Inc., Colorado Springs, Colorado and the disclosures of which are herein specifically 15 incorporated in their entirety by this reference.

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## BACKGROUND OF THE INVENTION

The present invention relates, in general, to the field of computing systems and techniques. More particularly, the present invention relates to multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions.

Currently, most large software applications achieve high performance operation through the use of parallel processing. This technique allows multiple processors to work simultaneously on the same problem to achieve a solution in a fraction of the time required for a single processor to accomplish the same result. The processors in use may be performing many copies of the same operation, or may be performing totally different operations, but in either case all processors are working simultaneously.

The use of such parallel processing has led to the proliferation of both multi-processor boards and large scale clustered systems. However, as more and more performance is required, so is more parallelism, resulting in ever larger systems. Clusters exist today that have tens of thousands of processors and can occupy football fields of space. Systems of such a large physical size present many obvious downsides, including, among other factors, facility requirements, power, heat generation and reliability.

#### SUMMARY OF THE INVENTION

However, if a processor technology could be
employed that offers orders of magnitude more
parallelism per processor, these systems could be
reduced in size by a comparable factor. Such a
processor or processing element is possible through

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the use of a reconfigurable processor. Reconfigurable processors instantiate only the functional units needed to solve a particular application, and as a result, have available space to instantiate as many functional units as may be required to solve the problem up to the total capacity of the integrated circuit chips they employ.

At present, reconfigurable processors, such as multi-adaptive processor elements (MAP<sup>TM</sup>, a trademark of SRC Computers, Inc.) can achieve two to three orders of magnitude more parallelism and performance than state-of-the-art microprocessors. Through the advantageous application of adaptive processing techniques as disclosed herein, this type of reconfigurable processing parallelism may be employed in a variety of applications resulting in significantly higher performance than that which can now be achieved while using significantly smaller and less expensive computer systems.

However, in addition to these benefits, there is an additional much less obvious one that can have even greater impact on certain applications and has only become available with the advent of multi-million gate reconfigurable chips. Performance gains are also realized by reconfigurable processors due to the much tighter coupling of the parallel functional units within each chip than can be accomplished in a microprocessor based computing system.

In a multi-processor, microprocessor-based

30 system, each processor is allocated but a relatively small portion of the total problem called a cell.

However, to solve the total problem, results of one processor are often required by many adjacent cells because their cells interact at the boundary and

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upwards of six or more cells, all having to interact to compute results, would not be uncommon.

Consequently, intermediate results must be passed around the system in order to complete the computation of the total problem. This, of necessity, involves numerous other chips and busses that run at much slower speeds than the microprocessor thus resulting in system performance often many orders of magnitude lower than the raw computation time.

On the other hand, in the use of an adaptive processor-based system, since ten to one thousand times more computations can be performed within a single chip, any boundary data that is shared between these functional units need never leave a single integrated circuit chip. Therefore, data moving around the system, and its impact on reducing overall system performance, can also be reduced by two or three orders of magnitude. This will allow both significant improvements in performance in certain applications as well as enabling certain applications to be performed in a practical timeframe that could not previously be accomplished.

Particularly disclosed herein is a method for data processing in a reconfigurable computing system comprising a plurality of functional units. The method comprises: defining a calculation for the reconfigurable computing system; instantiating at least two of the functional units to perform the calculation; utilizing a first of the functional units to operate upon a subsequent data dimension of the calculation and substantially concurrently utilizing a second of the functional units to operate upon a previous data dimension of the calculation.

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Further disclosed herein is a method for data processing in a reconfigurable computing system comprising a plurality of functional units. The method comprises: defining a first systolic wall comprising 5 rows of cells forming a subset of the plurality of functional units; computing a value at each of the cells in at least a first row of the first systolic wall; communicating the values between cells in the first row of the cells to produce updated values; communicating the updated values to a second row of the first systolic wall; and substantially concurrently providing the updated values to a first row of a second systolic wall of rows of cells in the subset of the plurality of functional units.

Also disclosed herein is a method for data processing in a reconfigurable processing system which includes setting up a systolic processing form employing a speculative processing strategy.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned and other features and objects of the present invention and the manner of attaining them will become more apparent and the invention itself will be best understood by reference to the following description of a preferred embodiment taken in conjunction with the accompanying drawings, wherein:

Fig. 1 is a simplified functional block diagram of typical clustered inter-processor communications path in a conventional multi-processor computing system;

. Fig. 2 is a functional block diagram of an adaptive processor communications path illustrating the many functional units ("FU") interconnected by

reconfigurable routing resources within the adaptive processor chip;

Fig. 3A is a graph of the actual performance improvement versus the number of processors utilized and illustrating the deviation from perfect scalability of a particular application utilizing a conventional multi-processor computing system such as that illustrated in Fig. 1;

Fig. 3B is a corresponding graph of the actual
10 performance improvement versus the number of
processors utilized and illustrating the performance
improvement over a conventional multi-processor
computing system utilizing an adaptive processor-based
computing system such as that illustrated in Fig. 2;

15 Fig. 4A is a simplified logic flowchart illustrating a conventional sequential processing operation in which nested Loops A and B are alternately active on different phases of the process;

Fig. 4B is a comparative, simplified logic

20 flowchart illustrating multi-dimensional processing in accordance with the technique of the present invention wherein multiple dimensions of data are processed by both Loops A and B such that the computing system logic is operative on every clock cycle;

25 Fig. 5A is illustrative of a general process for performing a representative multi-dimensional pipeline operation in the form of a seismic migration imaging function utilizing the parallelism available in the utilization of the adaptive processing techniques of the present invention;

Fig. 5B is a follow-on illustration of the computation phases employed in implementing the exemplary seismic migration imaging function of the preceding figure;

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Fig. 6A is a simplified logic flowchart for a particular seismic migration imaging application illustrative of the parallelism provided in the use of an adaptive processor-based computing system;

Fig 6B illustrates the computational process which may be employed by a microprocessor in the execution of the seismic imaging application of the preceding figure;

Fig. 6C illustrates the first step in the computational process which may be employed by an adaptive processor in the execution of the seismic imaging application of Fig. 6A in which a first shot (S1) is started;

Fig. 6D illustrates the second step in the same computational process for the execution of the seismic imaging application of Fig. 6A in which a second shot (S2) is started;

Fig. 6E illustrates the third step in the same computational process for the execution of the seismic imaging application of Fig. 6A in which the operation on the first and second shots is continued through compute;

Fig. 6F illustrates the fourth step in the same computational process showing the subsequent operation on shots S1 and S2;

Fig. 6G illustrates the fifth step in the same computational process followed by the continued downward propagation of shots S1 and S2 over all of the depth slices;

Fig. 7A illustrates a process for performing a representative systolic wavefront operation in the form of a reservoir simulation function also utilizing the parallelism available in the utilization of the

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adaptive processing techniques of the present invention:

Fig. 7B illustrates the general computation of fluid flow properties in the reservoir simulation of the preceding figure which are communicated to neighboring cells;

Fig. 7C illustrates the creation of a systolic wall of computation at Time Set 1 which has been started for a vertical wall of cells and in which communication of values between adjacent rows in the vertical wall can occur without storing values to memory;

Fig. 7D is a follow on illustration of the creation of a systolic wall of computation at Time Set 1 and Time Set 2 showing how a second vertical wall of cells is started after the computation for cells in the corresponding row of the first wall has been completed;

Fig. 8A illustrates yet another process for performing a representative systolic wavefront operation in the form of the systolic processing of bioinformatics also utilizing the parallelism available in the utilization of the adaptive processing techniques of the present invention;

Fig. 8B illustrates a systolic wavefront processing operation which further incorporates a speculative processing strategy based upon an evaluation of the rate of change of XB;

Fig. 8C is a further illustration of the systolic wavefront processing operation of the preceding figure incorporating speculative processing;

Fig. 9A illustrates still another process for performing a representative systolic wavefront operation in the form of structure codes calculating

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polynomials at grid intersections, again utilizing the parallelism available in the utilization of the adaptive processing techniques of the present invention;

Fig. 9B illustrates the computation start for a vertical wall of grid points at Time Set 1 for a polynomial evaluation performed on grid intersections wherein calculations between rows are done in a stochastic fashion using values from a previous row;

and

Fig. 9C is a further illustration of the polynomial evaluation performed on grid intersections of the preceding figure wherein a second wall is started after the cells in the corresponding row of the first wall have been completed.

## DESCRIPTION OF A REPRESENTATIVE EMBODIMENT

This application incorporates by reference the entire disclosure of Caliga, D. et al. "Delivering Acceleration: "The Potential for Increased HPC Application Performance Using Reconfigurable Logic", SC2001, November 2001, ACM 1-58113-293-X/01/0011.

With reference now to Fig. 1, a simplified functional block diagram of typical clustered interprocessor communications path in a conventional multiprocessor computing system 100 is shown. The computer system comprises a number of memory and input/output ("I/O" controller integrated circuits ("ICs") 1020 through 102N, (e.g. "North Bridge") 102 such as the P4X333/P4X400 devices available from VIA Technologies, Inc.; the M1647 device available from Acer Labs, Inc. and the 824430X device available from Intel Corporation. The North Bridge IC 102 is coupled by means of a Front Side Bus ("FSB") to one or more

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microprocessors  $104_{00}$  though  $104_{03}$  and  $104_{N0}$  through  $104_{N3}$  such as one of the Pentium® series of processors also available from Intel Corporation.

The North Bridge ICs  $102_0$  through  $102_N$  are coupled to respective blocks of memory  $106_0$  through  $106_N$  as well as to a corresponding I/O bridge element  $108_0$  through  $108_N$ . A network interface card ("NIC")  $110_0$  through  $210_N$  couples the I/O bus of the respective I/O bridge  $108_0$  through  $108_N$  to a cluster bus coupled to a common clustering hub (or Ethernet Switch) 112.

Since typically a maximum of four microprocessors 104, each with two or four functional units, can reside on a single Front Side Bus, any communication to more than four must pass over the Front Side Bus, inter-bridge bus, input/output ("I/O") bus, cluster interconnect (e.g. an Ethernet clustering hub 112) and then back again to the receiving processor 104. The I/O bus is typically an order of magnitude lower in bandwidth than the Front Side Bus, which means that any processing involving more than the four processors 104 will be significantly throttled by the loose coupling caused by the interconnect. All of this is eliminated with a reconfigurable processor having hundreds or thousands of functional units per processor.

With reference additionally now to Fig. 2, a functional block diagram of an adaptive processor 200 communications path for implementing the technique of the present invention is shown. The adaptive processor 200 includes an adaptive processor chip 202 incorporates a large number of functional units ("FU") 204 interconnected by reconfigurable routing resources. The adaptive processor chip 202 is coupled to a memory element 206 as well as an interconnect 208

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and a number of additional adaptive processor chips 210.

As shown, each adaptive processor chip 202 can contain thousands of functional units 204 dedicated to 5 the particular problem at hand. Interconnect between these functional units is created by reconfigurable routing resources inside each chip 202. As a result, the functional units 204 can share or exchange data at much higher data rates and lower latencies than a standard microprocessor 104 (Fig. 1). In addition, the adaptive processor chips 202 can connect directly to the inter-processor interconnect 208 and do not require the data to be passed through multiple chips in a chipset in order to communicate. This is because the adaptive processor can implement whatever kind of interface is needed to accomplish this connection.

With reference additionally now to Fig. 3A, a graph of the actual performance improvement versus the number of processors utilized in a conventional multiprocessor computing system 100 (Fig. 1) is shown. In this figure, the deviation from perfect scalability of a particular application is illustrated for such a system.

With reference additionally now to Fig. 3B, a corresponding graph of the actual performance improvement versus the number of processors utilized in an adaptive processor-based computing system 200 (Fig. 2) is shown. In this figure, the performance improvement provided with an adaptive processor-based computing system 200 over that of a conventional multi-processor computing system 100 is illustrated.

With reference additionally now to Fig. 4A, a simplified logic flowchart is provided illustrating a conventional sequential processing operation 400 in

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which nested Loops A (first loop 402) and B (second loop 404) are alternately active on different phases of the process.

As shown, the standard implementation of applications that have a set of nested loops 402,404 is to complete the processing of the first loop 402 before proceeding to the second loop 404. The problem inherent in this approach, particularly when utilized in conjunction with field programmable gate arrays ("FPGAs") is that all of the logic that has been instantiated is not being completely utilized.

With reference additionally now to Fig. 4B, a comparative, simplified logic flowchart is shown illustrating a multi-dimensional process 410 in accordance with the technique of the present invention. The multi-dimensional process 410 is effectuated such that multiple dimensions of data are processed by both Loops A (first loop 412) and B (second loop 414) such that the computing system logic is operative on every clock cycle.

In contrast to the sequential processing operation 400 (Fig. 4A) the solution to the problem of most effectively utilizing available resources is to have an application evaluate a problem in a data flow sense. That is, it will "pass" a subsequent dimension of a given problem through the first loop 412 of logic concurrently with the previous dimension of data being processed through the second loop 414. In practice, a "dimension" of data can be: multiple vectors of a problem, multiple planes of a problem, multiple time steps in a problem and so forth.

With reference additionally now to Fig. 5A, a general process for performing a representative multi-dimensional pipeline operation is shown in the form of

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a seismic migration imaging function 500. The process 500 can be adapted to utilize the parallelism available in the utilization of the adaptive processing techniques of the present invention in the form of a multi-adaptive processor (MAP<sup>TM</sup>, a trademark of SRC Computers, Inc., assignee of the present invention) STEP3d routine 502. The MAP STEP3d routine 502 is operation to utilize velocity data 504, source data 506 and receiver data 508 to produce a resultant image 510 as will be more fully described hereinafter.

With reference additionally now to Fig. 5B, the MAP STEP3d routine 502 of the preceding figure is shown in the various computational phases of: MAPTRI\_x 520, MAPTRI\_y 522, MAPTRI\_d+ 524 and MAPTRI\_d- 526.

With reference additionally now to Fig. 6A, a simplified logic flowchart for a particular seismic migration imaging application 600 is shown. The seismic migration imaging application 600 is illustrative of the parallelism provided in the use of an adaptive processor-based computing system 200 such as that shown in Fig. 2. The representative application 600 demonstrates a nested loop parallelism in the tri-diagonal solver and the same logic can be implemented for the multiple tri-diagonal solvers in the x, y, d+ and d- directions. The computational phases of: MAPTRI\_x 520, MAPTRI\_y 522, MAPTRI\_d+ 524 and MAPTRI\_d- 526 are again illustrated.

With reference additionally now to Fig. 6B, a computational process 610 is shown which may be employed by a microprocessor ("mP") in the execution of the seismic imaging application 600 of the preceding figure. The process 610 includes the step 612 of reading the source field  $[S(Z_0)]$  and receiver field  $[R(Z_0)]$  as well as the velocity field  $[V(Z_0)]$  at

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step 614. At step 616 values are computed for  $S(Z_{nz})$ ,  $R(Z_{nz})$  which step is followed by the phases MAPTRI\_x 520 and MAPTRI\_y 522. At step 618, the image of  $Z_{1/2}$  is computed. This is followed by the phases MAPTRI\_d+ 524 and MAPTRI\_d- 526 to produce the resultant image Z at step 620. The process 610 loops over the depth slices as indicated by reference number 622 and loops over the shots as indicated by reference number 624.

10 With reference additionally now to Fig. 6C, the first step in a computational process 650 in accordance with the technique of the present invention is shown in which a first shot (S1) is started. The process 650 may be employed by an adaptive processor (e.g. a MAP<sup>TM</sup> adaptive processor) as disclosed herein in the execution of the seismic imaging application 600 of Fig. 6A. As indicated by the shaded block, the phase MAPTRI x 520 is active.

With reference additionally now to Fig. 6D, the second step in the computational process 650 is shown at a point at which a second shot (S2) is started. Again, as indicated by the shaded blocks, the phase MAPTRI\_x 520 is active for S2, the phase MAPTRI\_y 522 is active for S1 and image  $Z_{1/2}$  has been produced at step 618. As shown, adaptive processors in accordance with the disclosure of the present invention support computation pipelining in multiple dimensions and the parallelism in Z and shots is shown at step 612.

With reference additionally now to Fig. 6E, the third step in the computational process 650 is shown in which the operation on the first and second shots is continued through compute. As indicated by the shaded blocks, the phase MAPTRI d+ 524 is active for

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S1, the phase MAPTRI\_y 522 is active for S2 and image  $Z_{1/2}$  has been produced at step 618.

With reference additionally now to Fig. 6F, the fourth step in the computational process 650 is shown illustrating the subsequent operation on shots S1 and S2. The phase MAPTRI\_d+ 524 is active for S2, the phase MAPTRI\_d- 526 is active for S1 and image Z has been produced at step 620.

With reference additionally now to Fig. 6G, the fifth step in the computational process 650 is shown as followed by the continued downward propagation of shots S1 and S2 over all of the depth slices. The phase MAPTRI\_x 520 is active for S1, the phase MAPTRI\_d- 526 is active for S2 and image Z has been produced at step 620.

With reference additionally now to Fig. 7A, a process 700 for performing a representative systolic wavefront operation in the form of a reservoir simulation function is shown which utilizes the parallelism available in the adaptive processing techniques of the present invention. The process 700 includes a "k" loop 702, "j" loop 704 and "i" loop 706 as shown.

With reference additionally now to Fig. 7B, the general computation of fluid flow properties in the reservoir simulation process 700 of the preceding figure are illustrated as values are communicated between a group of neighboring cells 710. The group of neighboring cells 710 comprises, in the simplified illustration shown, first, second and third walls of cells 712, 714 and 716 respectively. Each of the walls of cells includes a corresponding number of first, second, third and fourth rows 718, 720, 722 and 724 respectively.

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As shown, the computation of fluid flow properties are communicated to neighboring cells 710 and, importantly, this computation can be scheduled to eliminate the need for data storage. In accordance with the technique of the present invention, a set of cells can reside in an adaptive processor and the pipeline of computation can extend across multiple adaptive processors. Communication overhead between multiple adaptive processors may be advantageously minimized through the use of MAP™ adaptive processor chain ports as disclosed in U.S. Patent No. 6,339,819 issued on January 15, 2002 for: "Multiprocessor With Each Processor Element Accessing Operands in Loaded Input Buffer and Forwarding Results to FIFO Output Buffer", assigned to SRC Computers, Inc., assignee of the present invention, the disclosure of which is herein specifically incorporated by this reference.

With reference additionally now to Fig. 7C, the creation of a systolic wall 712 of computation at Time Set 1 is shown. The systolic wall 712 has been started for a vertical wall of cells and communication of values between adjacent rows 718 through 724 in the vertical wall can occur without storing values to memory.

With reference additionally now to Fig. 7D, a follow on illustration of the creation of a systolic wall 712 of computation at Time Set 1 and a second systolic wall 714 at Time Set 2 is shown. In operation, a second vertical wall of cells is started after the computation for cells in the corresponding row of the first wall has been completed. Thus, for example, at time t<sub>0</sub>, the first row 718 of systolic wall 712 is completed and the results passed to the first row 718 of the second systolic wall 714. At

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time  $t_1$ , the second row 720 of the first systolic wall 712 and the first row 718 of the second systolic wall 714 are computed. Thereafter, at time  $t_2$ , the third row 722 of the first systolic wall 712 and the second row 720 of the second systolic wall 714 are computed. The process continues in this manner for all rows and all walls.

With reference additionally now to Fig. 8A, yet another process 800 for performing a representative systolic wavefront operation is shown. The process 800 is in the form of the systolic processing of bioinformatics and also utilizes the parallelism available in the adaptive processing techniques of the present invention. As shown, systolic processing in the process 800 can pass previously computed data down within a column (e.g. one of columns 802, 804 and 806) as to subsequent columns as well (e.g. from column 802 to 804; from column 804 to 806 etc.) The computational advantage provided is the processing of the second column 804 can begin after only a few clock cycles following the start of the processing of the first column 802 to compute the first "match" state.

With reference additionally now to Fig. 8B, a systolic wavefront processing operation 810 is shown. The processing operation 810, comprising "i" loop 812 and "k" loop 814 now further incorporates a speculative processing strategy based upon an evaluation of the rate of change of XB.

A straightforward systolic processing operation could be used for performing the operation 810 but for the problem inherent in the computation of XB as its value XB[i] 816 can not be known until the completion of the entire "k" loop 814. After evaluating the rate of change of XB, it was determined that a speculative

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processing strategy could be used for the problem. A normal systolic form is set up and the value of XB is held constant for the set of columns computed in the systolic set. At the bottom of each column, the value of XB[i] 816 is then computed.

With reference additionally now to Fig. 8C, a further illustration of the systolic wavefront processing operation 810 incorporating speculative processing of the preceding figure is shown. The speculative processing includes "j" columns 8180 through 818; as shown. Each of the columns 818 assumes that XB[i+j] has a constant value. A test is conducted at the bottom of each of the columns 818 to determine with the XB value changes as indicated at steps 820; through 820;. If the value of XB changes at the i+n column, the process is then restarted at that column 818. Since the rate of change of XB is relatively slow, the "cost" of the compute operation can be greatly reduced.

With reference additionally now to Fig. 9A, another process 900 for performing a representative systolic wavefront operation is shown in the form of structure codes calculating polynomials at grid intersections 902. The process 900 advantageously utilizes the parallelism available in the adaptive processing techniques of the present invention.

With reference additionally now to Figs. 9B and 9C, the computation start for a vertical wall 910 of grid points at Time Set 1 is shown for a polynomial evaluation performed on grid intersections 902 (Fig. 9A) wherein calculations between rows 912, 914, 016 and 918 are done in a stochastic fashion using values from a previous row. As shown, a polynomial evaluation is performed on the grid intersections 902

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such that a second wall  $910_1$  is started after the cells in the corresponding row of the first wall  $910_0$  have been completed.

As can be determined from the foregoing, the

multi-adaptive processing systems and techniques for
enhancing parallelism and performance of computational
functions disclosed herein can be employed in a myriad
of applications including multi-dimensional pipeline
computations for seismic applications, search

algorithms, information security, chemical and
biological applications, filtering and the like as
well as for systolic wavefront computations for fluid
flow and structures analysis, bioinformatics etc.
Some applications may also employ both the multidimensional pipeline and systolic wavefront
methodologies.

Following are representative applications of the techniques for adaptive processor based computation disclosed herein:

## 20 Imaging

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Seismic: These applications, typically used in the oil and gas exploration industries, process echo data to produce detailed analysis of subsurface features. The applications use data collected at numerous points and consisting of many repeated parameters. Due to this, these programs are ideal candidates to take advantage of parallel computing. In addition, because the results of the computation on one data point are used in the computation of the next, these programs will particularly benefit from the tight parallelism that can be found in the use of adaptive or reconfigurable processors.

Synthetic Aperture Radar ("SAR"): These applications are typically used in geographical

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imaging. The applications use data collected in swaths. Processing consists of repeated operations on data that has been sectioned in cells. These programs are also ideal candidates to take advantage of parallel computing and in particular to benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

JPEG Image compression: These applications partition an image into numerous blocks. These blocks then have a set of operations performed on them. The operations can be parallelized across numerous blocks. The combination of the set of operations and the parallelism will particularly benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

MPEG Image compression: These applications partition a frame into numerous blocks. These blocks then have a set of operations performed on them. The operations can be parallelized across numerous blocks. In addition, there are numerous operations that are performed on adjacent frames. The combination of the set of operations and the parallelism will particularly benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

#### 25 Fluid flow

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Reservoir Simulation: These applications, also typically used in the oil and gas production industries, process fluid flow data in the oil and gas subsurface reservoirs to produce extraction models. The application will define a three dimensional ("3d") set of cells that contain the oil and gas reservoir. These programs are ideal candidates to take advantage of parallel or adaptive computing because there are repeated operations on each cell. In addition,

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information computed for each cell is then passed to neighboring cells. These programs will particularly benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Weather prediction: Such an application will partition the forecast area into logical grid cells. The computational algorithms will then perform calculations that have polynomials that have nodes associated with the grid cells. These programs are ideal candidates to take advantage of adaptive or parallel computing because there are repeated operations on each cell associated with the set of times computed in the forecast.

Automotive: These applications investigate the aerodynamics of automobile or other aerodynamic structures. The application generally divides the space surrounding the automobile structure into logical cells that are associated with nodes in computational polynomials. These programs are ideal candidates to take advantage of adaptive or parallel computing because there are repeated operations on each cell associated with the set of wind velocities computed in the forecast. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Aerospace: These applications investigate the aerodynamics of aerospace/airplane structures. The application divides the space surrounding the aerospace/airplane structure into logical cells that are associated with nodes in computational polynomials. These programs are ideal candidates to take advantage of parallel computing because there are repeated operations on each cell associated with the set of wind velocities computed in the forecast.

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These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Plastic Injection Molding: These applications
investigate the molding parameters of injecting liquid
plastic into molds. The application divides the space
inside the mold into logical cells that are also
associated with nodes in computational polynomials.
These programs are ideal candidates to take advantage
of parallel computing because there are repeated
operations on each cell associated with the set of
injection parameters. These programs will benefit
from the tight parallelism that can be found in
adaptive or reconfigurable processors.

#### 15 Structures

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Crash Analysis: These applications are typically used in the automotive or aviation industry. The application will partition the entire automobile into components. These components are then subdivided into cells. The application will analyze the effect of a collision on the structure of the automobile. These programs are ideal candidates for parallel computing because there are repeated operations on each cell and they receive computed information from their neighboring cells. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Structural Analysis: These applications investigate the properties of structural integrity. The application divides the structure into logical cells that are associated with nodes in computational polynomials. These programs are ideal candidates to take advantage of parallel computing because there are repeated operations on each cell associated with load

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and stress. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

#### Search algorithms

Image searches: These applications are typically used in the security industry for fingerprint matching, facial recognition and the like. The application seeks matches in either a collection of subsets of the total image or the total image itself.

The process compares pixels of the model to pixels of a record from an image database. These programs are ideal candidates for parallel computing because of the correlation of comparison results that exist for each pixel in the subsets or entire image. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Data mining: These applications are typically used in commercial market spaces. The application seeks matches in a set of search information (e.g. character strings) in each record in a database. The application then produces a match correlation for all data records. A match correlation is produced from the comparison results for each set of search information with all characters in a database record. These programs are ideal candidates for parallel computing because of the repeated comparison operations that exist all character comparisons of the set of search information with each character in the database record. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

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#### Finance

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Financial modeling: The application creates numerous strategies for each decision step in the modeling process. The results of a computational step are feed into another set of strategies for subsequence modeling steps. These programs are ideal candidates to take advantage of parallel computing because there are repeated operations on each strategy within a modeling step. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

#### Information Security

Encryption/Decryption: The application applies an algorithm that converts the original data into an encrypted, or "protected", form. The process is applied to each set of N bits in the original data. Decryption reverses the process to deliver the original data. These programs are ideal candidates for parallel computing because there are repeated operations on each N bits of data. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

#### Chemistry/Biology

Genetic pattern matching: These applications are typically used in the bioinformatics industry. The application looks for matches of a particular genetic sequence (or model) to a database of genetic records. The application compares each character in the model to the characters in genetic record. These programs are ideal candidates for parallel computing because of the repeated comparison operations that exist for all character comparisons of the model with each character in the genetic record. These programs will benefit

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from the tight parallelism that can be found in adaptive or reconfigurable processors.

Protein Folding: These applications are typically used by pharmaceutical companies. The application investigates the dynamics of the deformation of the protein structure. The application uses a set of equations which are recomputed at various "time" intervals to model the protein folding. These programs are ideal candidates for parallel computing because of the repeated computations on a large set of time intervals in the modeling sequence. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors

Organic structure interaction: These applications are typically used by chemical and drug companies. The application investigates the dynamics of organic structures as they are interacting. The application uses a set of equations which are recomputed at various "time" intervals to model how the organic structure interact. These programs are ideal candidates for parallel computing because of the repeated computations on a large set of time intervals in the modeling sequence. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors

#### Signals

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Filtering: Applications often utilize filtering techniques to "clean-up" a recorded data sequence. This technique is utilized in a wide variety of industries. The application generally applies a set of filter coefficients to each data point in the recorded sequence. These programs are ideal candidates for parallel computing because of the repeated computations to all data points in the

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sequence and all sequences. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

While there have been described above the principles of the present invention in conjunction with specific, exemplary applications for the use of adaptive processor-based systems in the implementation of multi-dimensional pipeline and systolic wavefront computations, it is to be clearly understood that the foregoing descriptions are made only by way of example 10 and not as a limitation to the scope of the invention. Particularly, it is recognized that the teachings of the foregoing disclosure will suggest other modifications to those persons skilled in the relevant art. Such modifications may involve other features which are already known per se and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that 20 the scope of the disclosure herein also includes any novel feature or any novel combination of features. disclosed either explicitly or implicitly or any generalization or modification thereof which would be apparent to persons skilled in the relevant art, 25 whether or not such relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as confronted by the present invention. The applicants hereby reserve the right to formulate new claims to 30 such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

What is claimed is:

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#### CLAIMS:

- 1. A method for data processing in a reconfigurable computing system comprising a plurality of functional units, said method comprising:
- 5 defining a calculation for said reconfigurable computing system;

instantiating at least two of said functional units to perform said calculation;

utilizing a first of said functional units to

10 operate upon a subsequent data dimension of said

calculation; and

substantially concurrently utilizing a second of said functional units to operate upon a previous data dimension of said calculation.

- 15 2. The method of claim 1 wherein said subsequent and previous data dimensions of said calculation comprise multiple vectors in said calculation.
- The method of claim 1 wherein said subsequent and previous data dimensions of said calculation comprise
   multiple planes in said calculation.
  - 4. The method of claim 1 wherein said subsequent and previous data dimensions of said calculation comprise multiple time steps in said calculation.
- 5. The method of claim 1 wherein said subsequent an 25 previous data dimensions of said calculation comprise multiple grid points in said calculation.
  - 6. The method of claim 1 wherein said calculation comprises a seismic imaging calculation.

- 7. The method of claim 1 wherein said calculation comprises a synthetic aperture radar imaging calculation.
- 8. The method of claim 1 wherein said calculation comprises a JPEG image compression calculation.
  - 9. The method of claim 1 wherein said calculation comprises an MPEG image compression calculation.
- The method of claim 1 wherein said calculation comprises a fluid flow calculation for a reservoir simulation.
  - 11. The method of claim 1 wherein said calculation comprises a fluid flow calculation for weather prediction.
- 12. The method of claim 1 wherein said calculation 15 comprises a fluid flow calculation for automotive applications.
  - 13. The method of claim 1 wherein said calculation comprises a fluid flow calculation for aerospace applications.
- 20 14. The method of claim 1 wherein said calculation comprises a fluid flow calculation for an injection molding application.
  - 15. The method of claim 1 wherein said calculation comprises a structures calculation for crash analysis.
- 25 16. The method of claim 1 wherein said calculation is comprises a structures calculation for structural analysis.

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- 17. The method of claim 1 wherein said calculation comprises a search algorithm for an image search.
- 18. The method of claim 1 wherein said calculation comprises a search algorithm for data mining.
- 5 19. The method of claim 1 wherein said calculation comprises a financial modeling application.
  - 20. The method of claim 1 wherein said calculation comprises an encryption algorithm.
- 21. The method of claim 1 wherein said calculation 10 comprises an decryption algorithm.
  - 22. The method of claim 1 wherein said calculation comprises a genetic pattern matching function.
  - 23. The method of claim 1 wherein said calculation comprises a protein folding function.
- 15 24. The method of claim 1 wherein said calculation comprises an organic structure interaction function.
  - 25. The method of claim 1 wherein said calculation comprises a signal filtering application.
- 26. A method for data processing in a reconfigurable 20 computing system comprising a plurality of functional units, said method comprising:

defining a first systolic wall comprising rows of cells forming a subset of said plurality of functional units;

25 computing a value at each of said cells in at least a first row of said first systolic wall;

communicating said values between cells in said first row of said cells to produce updated values;

communicating said updated values to a second row of said first systolic wall; and

substantially concurrently providing said updated values to a first row of a second systolic wall of rows of cells in said subset of said plurality of functional units.

- 27. The method of claim 26 wherein said values correspond to vectors in a computation.
- 28. The method of claim 26 wherein said values10 correspond to planes in a computation.
  - 29. The method of claim 26 wherein said values correspond to time steps in a computation.
  - 30. The method of claim 26 wherein said values correspond to grid points in a computation.
- 15 31. The method of claim 26 wherein said step of communicating said updated values to a second row of said first systolic wall is carried out without storing said updated values in an extrinsic memory.
- 32. The method of claim 26 wherein said values correspond to a seismic imaging calculation.
  - 33. The method of claim 26 wherein said values correspond to a synthetic aperture radar imaging calculation.
- 34. The method of claim 26 wherein said values25 correspond to a JPEG image compression calculation.
  - 35. The method of claim 26 wherein said values correspond to an MPEG image compression calculation.

- 36. The method of claim 26 wherein said values correspond to a fluid flow calculation for a reservoir simulation.
- 37. The method of claim 26 wherein said values correspond to a fluid flow calculation for weather prediction.
  - 38. The method of claim 26 wherein said values correspond to a fluid flow calculation for automotive applications.
- 10 39. The method of claim 26 wherein said values correspond to a fluid flow calculation for aerospace applications.
  - 40. The method of claim 26 wherein said values correspond to a fluid flow calculation for an
- 15 injection molding application.
  - 41. The method of claim 26 wherein said values correspond to a structures calculation for crash analysis.
- 42. The method of claim 26 wherein said values
  20 correspond to a structures calculation for structural analysis.
  - 43. The method of claim 26 wherein said values correspond to a search algorithm for an image search.
- 44. The method of claim 26 wherein said values25 correspond to a search algorithm for data mining.
  - 45. The method of claim 26 wherein said values correspond to a financial modeling application.

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- 46. The method of claim 26 wherein said values correspond to an encryption algorithm.
- 47. The method of claim 26 wherein said values correspond to an decryption algorithm.
- 5 48. The method of claim 26 wherein said values correspond to a genetic pattern matching function.
  - 49. The method of claim 26 wherein said values correspond to a protein folding function.
- 50. The method of claim 26 wherein said values correspond to an organic structure interaction function.
  - 51. The method of claim 26 wherein said values correspond to a signal filtering application.
- 52. The method of claim 26 wherein said reconfigurable computing system comprises at least one adaptive processor.
  - 53. The method of claim 52 wherein said reconfigurable computing system further comprises at least one microprocessor.
- 20 54. A method for data processing in a reconfigurable computing system comprising a plurality of functional units, said method comprising:

performing a calculation by a subset of said plurality of functional units to produce computed data;

passing said computed data from a first column of said calculation to a next column in said calculation;

evaluating a rate of change in at least one variable for each of said columns in said calculation;

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continuing said calculation if said variable does not change for a particular column of said calculation; and

restarting said calculation at said column of said calculation where said variable does change.

55. A method for data processing in a reconfigurable computing system comprising:

performing systolic processing on a calculation do be executed by said reconfigurable computing system; and

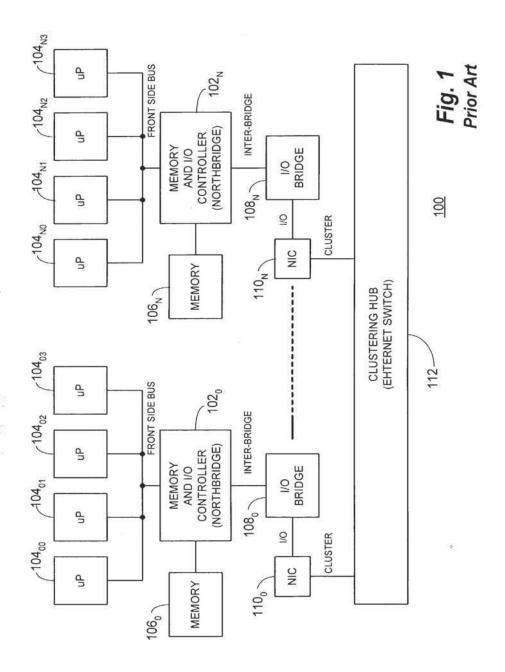
further performing speculative processing on said calculation by said reconfigurable computing system.

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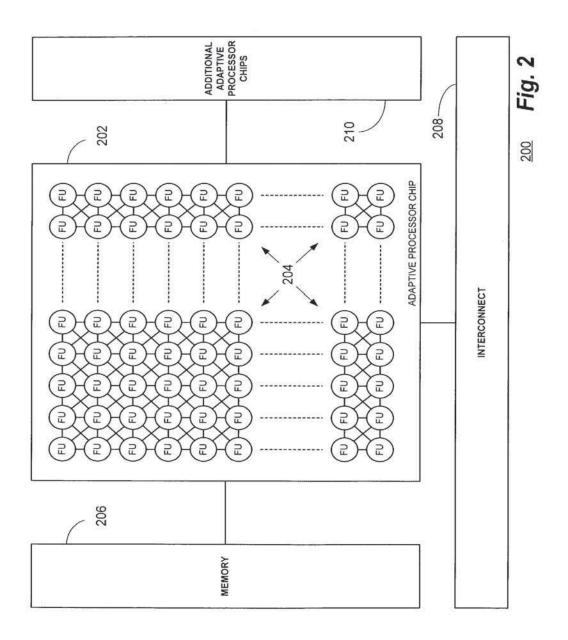
## ABSTRACT OF THE DISCLOSURE

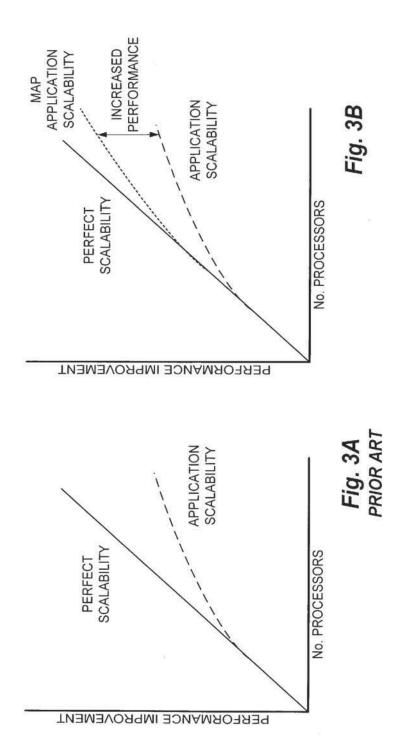
Multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions are disclosed which can be employed in a myriad of applications including multi-dimensional pipeline computations for seismic applications, search algorithms, information security, chemical and biological applications, filtering and the like as well as for systolic wavefront computations for fluid flow and structures analysis, bioinformatics etc. Some applications may also employ both the multi-dimensional pipeline and systolic wavefront methodologies disclosed.

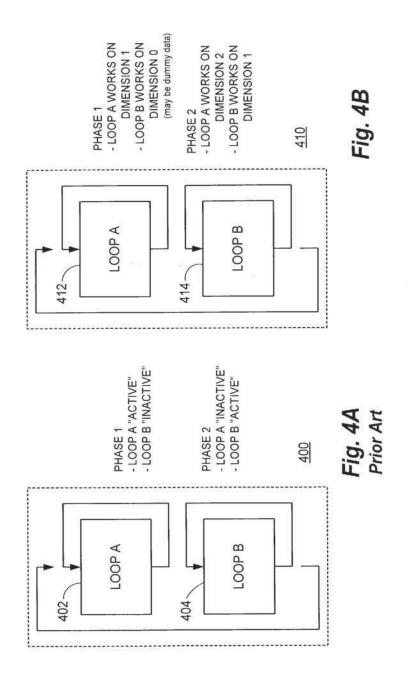
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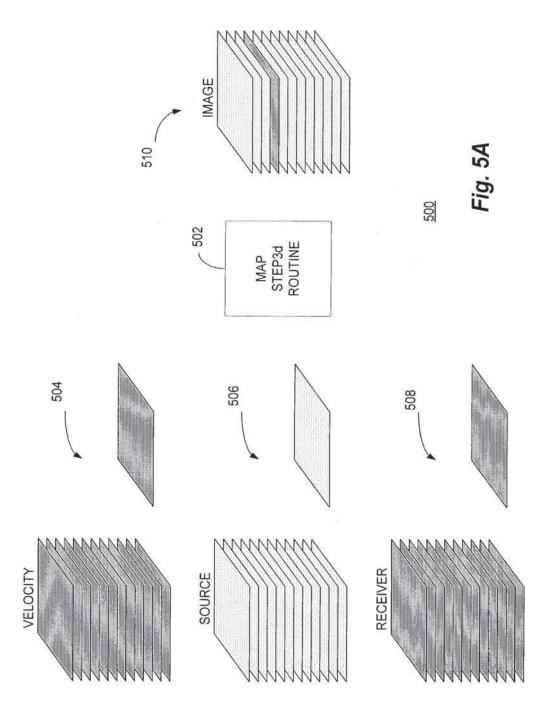


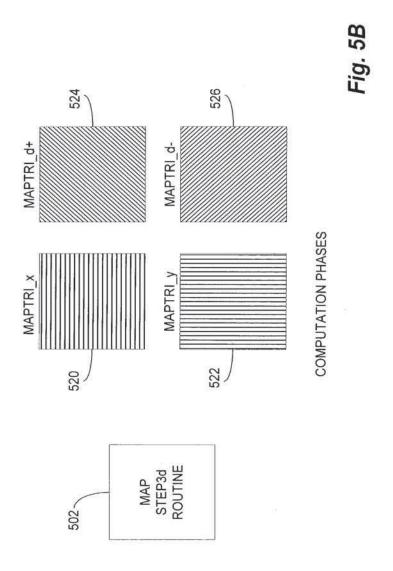
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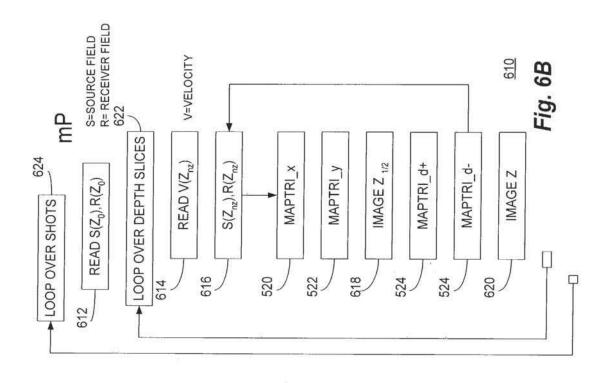


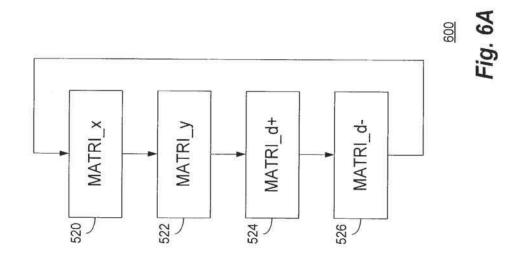


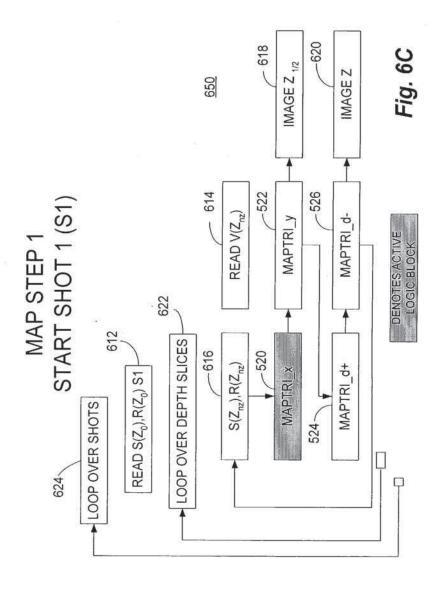


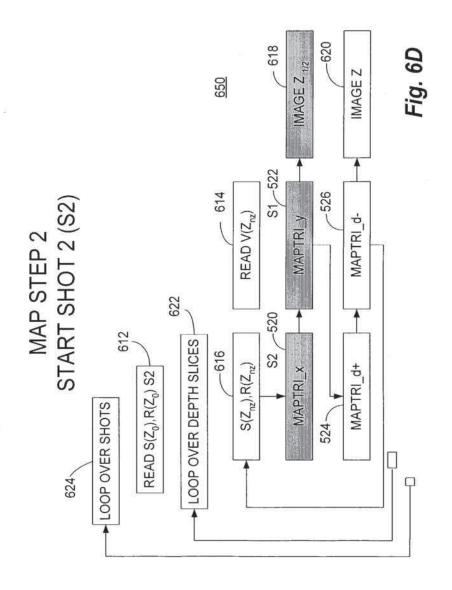


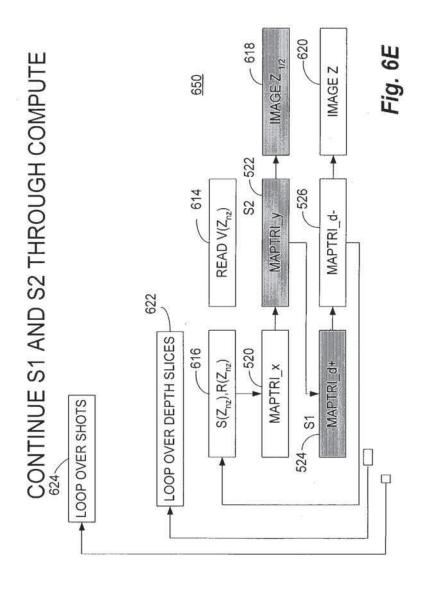


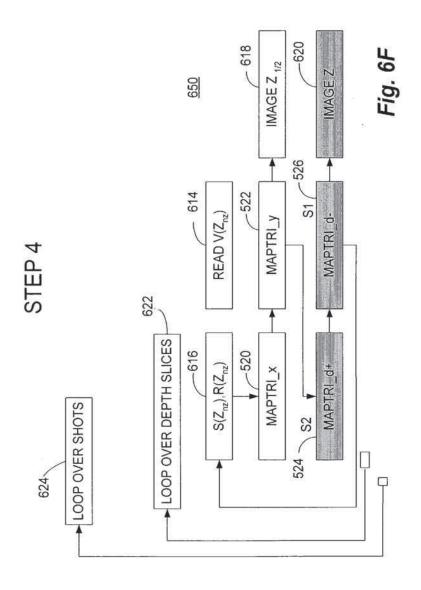


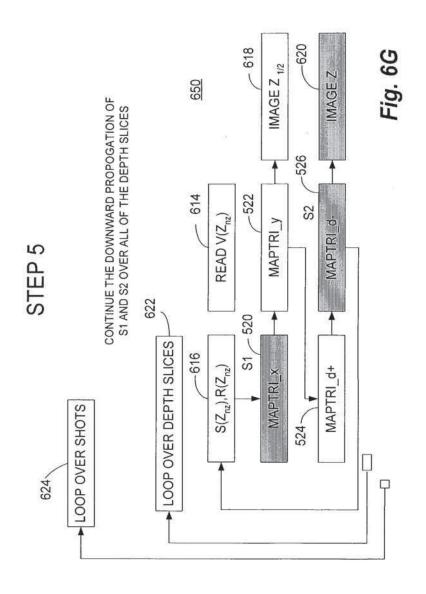


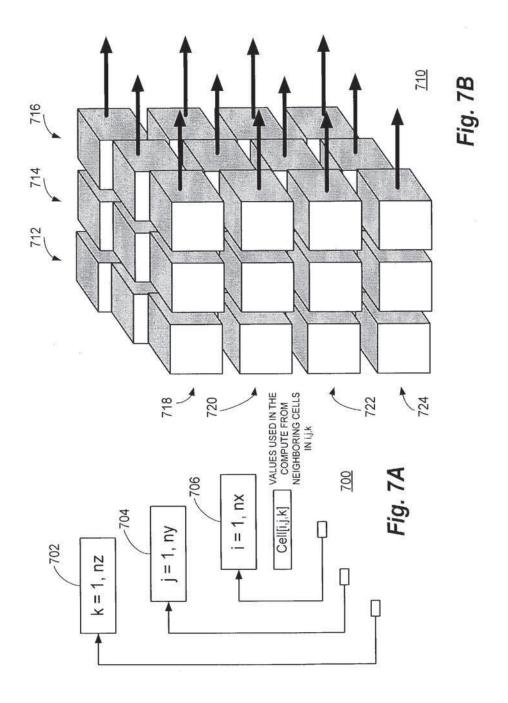


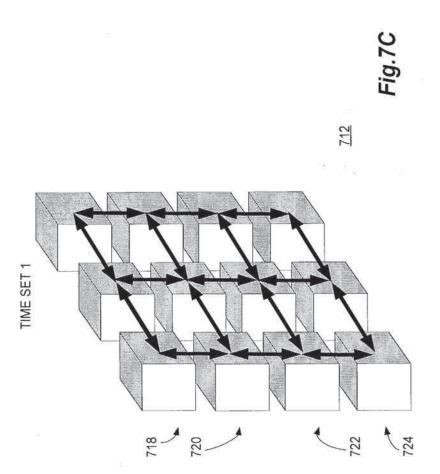


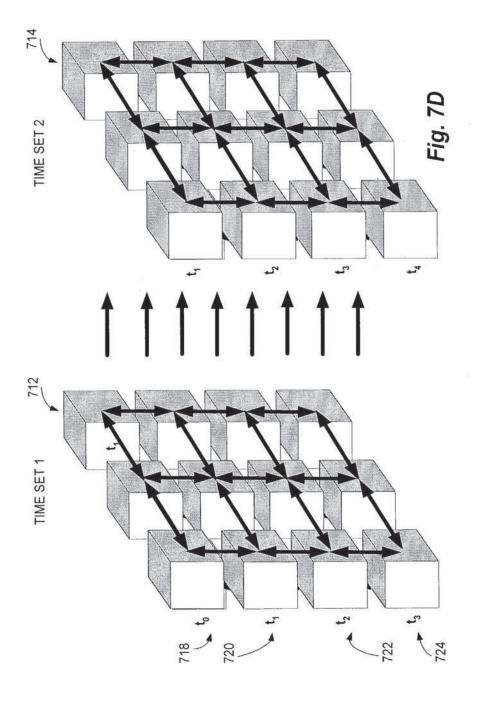


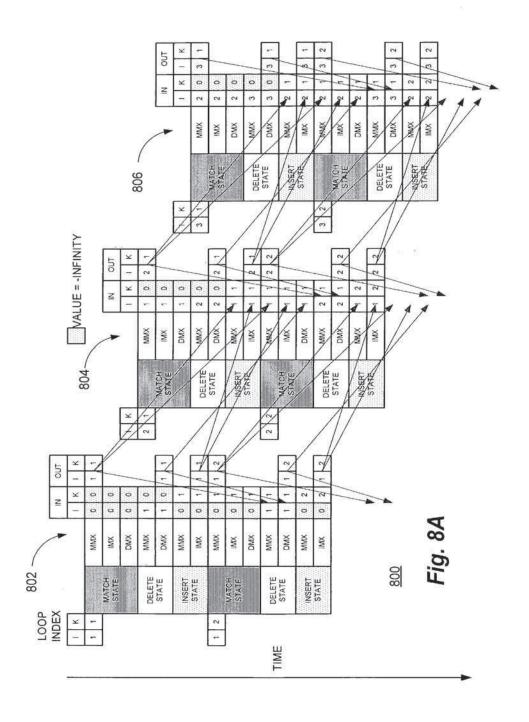


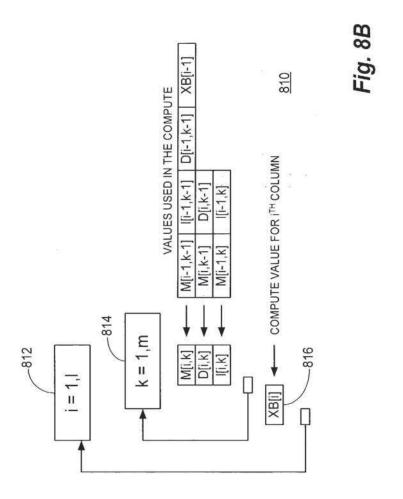


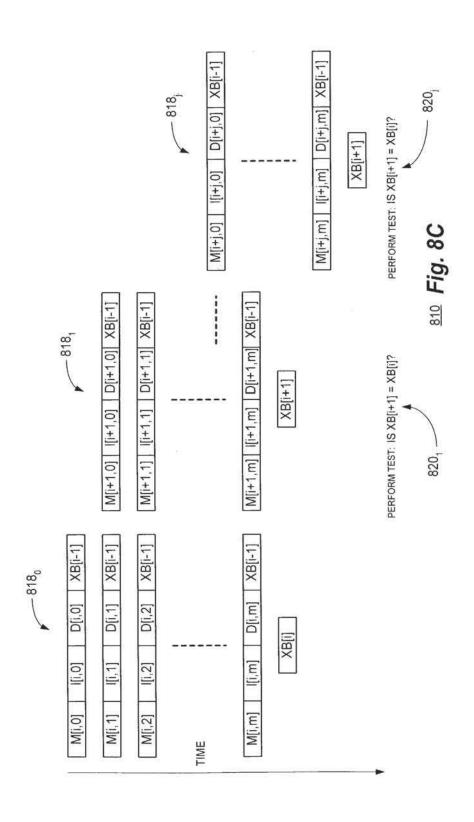




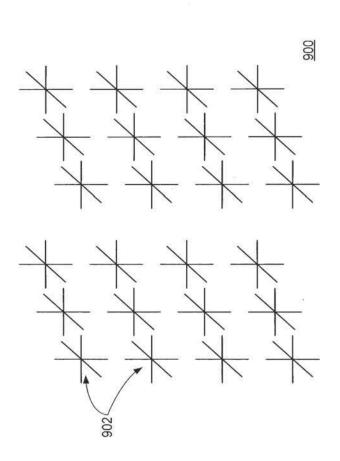


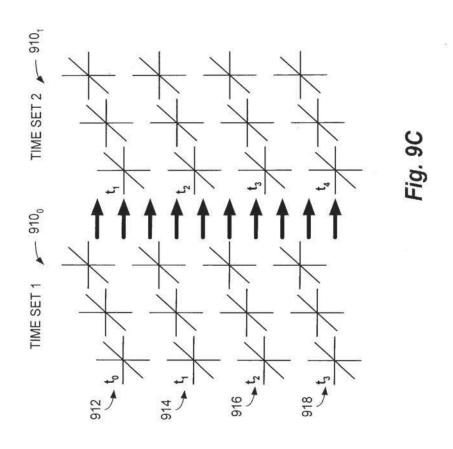


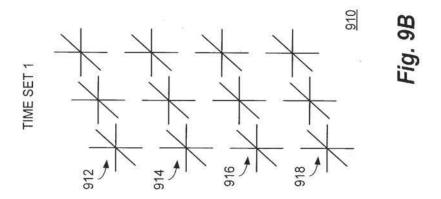












#### **DECLARATION FOR** SRC015 Attorney Docket No. **UTILITY OR DESIGN First Named Inventor** Jon M. Huppenthal et al. PATENT APPLICATION COMPLETE IF KNOWN (37 CFR 1.63) **Application Number** ☐ Declaration □ Declaration Filing Date Herewith Submitted Submitted after Initial Filing--surcharge 37 CFR 1.16(e) required with Initial Group Art Unit Filing **Examiner Name**

As a below named Inventor, I hereby declare that:										
My residence, mailing address, and citizenship are as stated below next to my name.										
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:										
MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS										
the specification of which										
is attached hereto										
OR										
was filed on (MM/DD/YYYY)	as U.S. Application PCT International A									
and was amended on (MM/DD/YYYY)	(if applicable)		S9 1175							
I hereby state that I have reviewed and understand the claims, as amended by any amendment specifically ref	contents of the abov erred to above.	e identified spe	cification, inclu	ding the						
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I hereby claim foreign priority benefits under 35 U.S.C patent or inventor's certificate, or § 365(a) of any PCT i other than the United States of America, listed below a application for patent or inventor's certificate, or of any the application on which priority is claimed.	nternational applicati nd have also identifie	on which desig	nated at least o	any foreign						
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Additional foreign application nos. are listed on a su	upplemental priority d	ata sheet PTO/	SB/02B attache	ed hereto:						
I hereby claim the benefit under 35 U.S.C. § 119(e) of										
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# **DECLARATION** – Utility or Design Patent Application

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# **DECLARATION**

# ADDITIONAL INVENTOR(S) Supplemental Sheet Page \_\_1\_\_ of \_\_1\_\_

Name of Additiona	I Joint Inventor, if any:	□Аре	etition ha	s been filed	for this un	signed invent	or				
Given Name (first	and middle [if any])	Family	Family Name or Surname								
David E.		Calig	a								
Inventor's Signature											
Residence: City	Colorado Springs	State	co	Country	USA	Citizenship	USA				
Mailing Address	8445 Lauralwood L	ane									
City	Colorado Springs	State	со	ZIP	80919	Country	USA				
Name of Additiona	I Joint Inventor, if any:	☐ A petition	on has be	een filed for	this unsig	ned inventor					
Given Name (first	Family Name or Surname										
Inventor's Signature		00 AW				Date					
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Name of Additiona	al Joint Inventor, if any:	□Ар	etition ha	s been filed	for this u	nsigned invent	or				
Given Name (first	and middle [if any])	Fami	ly Name	or Surname							
Inventor's Signature						Date					
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FORM PTO-875 (Rev. 8/01)

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Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE



Commissioner for Patants Washington, DC 20231 www.uspto.gov

APPLICATION NUMBER FILING/RECEIPT DATE FIRST NAMED APPLICANT ATTORNEY DOCKET NUMBER

10/285,318

HOGAN & HARTSON LLP

1200 SEVENTEENTH ST DENVER, CO 80202

ONE TABOR CENTER, SUITE 1500

25235

10/31/2002

Jon M. Huppenthal

SRC015

CONFIRMATION NO. 1420 FORMALITIES LETTER

\*OC000000009216113\*

Date Mailed: 12/09/2002

### NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

#### Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
   Applicant must submit \$ 740 to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).
- · The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

#### Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

 Additional claim fees of \$714 as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

## SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is \$1584 for a Large Entity

- \$740 Statutory basic filing fee.
- \$130 Late oath or declaration Surcharge.





- Total additional claim fee(s) for this application is \$714
  - \$630 for 35 total claims over 20 .
  - \$84 for 1 independent claims over 3 .

A copy of this notice MUST be returned with the reply.

Customer Service Center

Initial Patent Examination Division (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE







13

Attorney Docket No. SRC015 Client/Matter No. 80404.0018 Express Mail No. EV035495015US

#### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. 10/285,318

Filed: October 31, 2002

For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

Group Art Unit: 2121

Examiner: Not yet assigned

Confirmation No.: 1420

#### RESPONSE TO NOTICE TO FILE MISSING PARTS

BOX MISSING PARTS Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

In response to the Notice to File Missing Parts of Application, Filing Date Granted, mailed December 9, 2002, submitted herewith is a signed Declaration for Patent Application; a check in the amount of \$1,594 to cover \$1,464 for the filing fee and \$130 to cover the surcharge for a large entity; and a copy of the PTO Notice form. Any fee deficiency associated with this communication may be charged to Deposit Account No. 50-1123.

Also enclosed is a Recordation Form Cover Sheet PTO 1595 with executed Assignment and recording fee of \$40.00. Please forward the Assignment to the Recording Branch for recording.

Date: 09 mum 2003

William J. Kubida, Registration No. 29,664

**HOGAN & HARTSON LLP** 

One Tabor Center

1200 17th Street, Suite 1500

Denver, Colorado 80202

(719) 448-5909 Tel

(303) 899-7333 Fax

\\\CS - 80404/0018 - 57948 v1

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O' Thor FY 2	003	Filing Date	October 31, 2002
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JAN	E O	Examiner Name	Not yet assigned
Applicant claims small entity statu	s. See 37 CERTOEMAS	Group / Art Unit	2121
OTAL AND OF PAYMENT	(\$) 1,634.00	Attorney Docket No.	SRC015

MI	ETHOD OF	PAYMENT (check all tha	t apply)		454	FEE CALCULATIO	N (continued)	
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SUBMITTED		nplete (if applicable)						
Name (Print/	THREE VAST	Nam J. Kubida	11		stration No. rney/Agent)	29,664	Telephone	(719) 448-5900
Signature	X	elec its	Del				Date 0	January

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Attorney Docket No. SRC015 Client/Matter No. 80404.0018 Express Mail No. EV035495015US

STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. 10/285,318

Filed: October 31, 2002

For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

Group Art Unit: 2121

Examiner: Not yet assigned

Confirmation No.: 1420

### CERTIFICATE OF MAILING BY EXPRESS MAIL

**BOX MISSING PARTS** Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

The undersigned hereby certifies that the following documents:

- 1. Response to Notice to File Missing Parts;
- Copy of Notice to File Missing Parts of Application Filing Date Granted, form and surcharge payment of \$130;
- 3. Executed Declaration;
- 4. Fee Transmittal with check in the amount of \$1,464;
- 5. Recordation Form Cover Sheet PTO 1595 with Executed Assignment and Recording Fee of \$40.00;
- 6. Certificate of Mailing By Express Mail;
- 7. Return postcard;

relating to the above application, were deposited as "Express Mail", Mailing Label No. EV035495015US with the United States Postal Service, addressed to Box Missing Parts, Assistant Commissioner for Patents, Washington, D.C., 20231 galan

Date

William J. Kubida, Reg. No. 29,664

HOGAN & HARTSON LLP

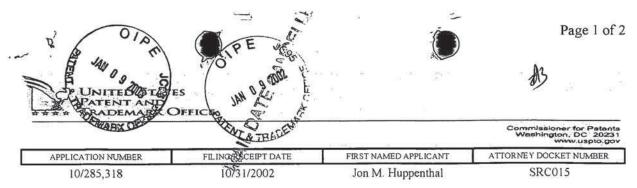
One Tabor Center

1200 17th Street, Suite 1500

Denver, Colorado 80202

(719) 448-5909 Tel

(303) 899-7333 Fax



25235 HOGAN & HARTSON LLP ONE TABOR CENTER, SUITE 1500 1200 SEVENTEENTH ST DENVER, CO 80202 CONFIRMATION NO. 1420
FORMALITIES LETTER
\*OC000000009216113\*

Date Mailed: 12/09/2002

# NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

## Filing Date Granted

#### Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

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o \$740 Statutory basic filing fee.

• \$740 Statutory basic filing fee. 01 FC:1001 750.00 UP 130.00 UP

- Total additional claim fee(s) for this application is \$714
  - \$630 for 35 total claims over 20 .
  - \$84 for 1 independent claims over 3.

A copy of this notice MUST be returned with the reply.

Customer Service Center

Initial Patent Examination Division (703) 308-1202

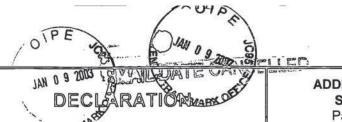
PART 3 - OFFICE COPY

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	DECLARATION FOR	Attorney Docket No.	SRC015
ე ტ	UTILITY OR DESIGNED PATENT APPLICATION	First Named Inventor	Jon M. Huppenthal et al.
AND ALL ST	PATENT APPLICATION	COMPL	LETE IF KNOWN
C COM	(37 CFR 4\63)	Application Number	10/285,318
WENT & I	Declaration Submitted  Declaration Submitted	Filing Date	October 31, 2002
with Mitial %		Group Art Unit	2121
	JAN 0 9 2003 1.16(e) required	Examiner Name	Not yet assigned
	M M		

A A												
As a below transed investor, I hereby declare that:												
My residence, mailing address, and citizenship are as stated below next to my name.												
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:												
MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS												
the specification of which												
is attached hereto												
OR												
	Application No. or rnational Application No. 10/285,318											
and was amended on (MM/DD/YYYY) (if application)	able)											
I hereby state that I have reviewed and understand the contents of claims, as amended by any amendment specifically referred to all	f the above identified specification, including the love.											
I acknowledge the duty to disclose information which is material to for continuation-in-part applications, material information which be application and the national or PCT international filing date of the	ecame available between the filing date of the prior											
I hereby claim foreign priority benefits under 35 U.S.C § 119(a)-(o patent or inventor's certificate, or § 365(a) of any PCT internations other than the United States of America, listed below and have all application for patent or inventor's certificate, or of any PCT internation the application on which priority is claimed.	al application which designated at least one country so identified below, by checking the box, any foreign											
Prior Foreign Appl. No.(s) Country Foreign Filin (MM/DD/Y)												
Additional foreign application nos. are listed on a supplementa	I priority data sheet PTO/SB/02B attached hereto:											
I hereby claim the benefit under 35 U.S.C. § 119(e) of any United	States provisional application(s) listed below.											
Application Number(s) Filing Date (MM/DD/YYYY)												

# DECLARATION - Utility or Design Patent Application

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Jon M.		-/		nupp	entha				
Inventor's Signature	Jan 1	appent	5	3			ħ	Date //6/6	23
Residence Cit	ty Colorado S	prings State	Colo	rado	Coun	try	USA	Citizenship	USA
Mailing Addre	ss 10015 Burg	ess Road							
City	Colorado S	prings State	Colo	rado	ZIP	8	0908	Country	USA
⊠Additional i	nventors are named	on _1suppleme	ntal add	litional	invento	r(s) s	heet(s)	PTO/SB/02A	attached



# ADDITIONAL INVENTOR(S) Supplemental Sheet Page \_\_1\_\_ of \_\_1\_\_

Name of Additiona	I Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor									
Given Name (first	and middle [if any])	Family Name or Surname									
David E.		Caliga									
Inventor's Signature	SJ e. (	?aloge			_	Date	1/4/2003				
Residence: City	Colorado Springs	State	со	Country	USA	Citizenship	USA				
Mailing Address	8445 Lauralwood L	ane									
City	Colorado Springs	State	со	ZIP	80919	Country	USA				
Name of Additiona	I Joint Inventor, if any:	□ A petition	on has b	een filed for	this unsig	ned inventor					
Given Name (first	Family Name or Surname										
Inventor's Signature				82.4		Date					
Residence: City		State		Country		Citizenship					
Mailing Address											
City		State		ZIP		Country					
Name of Additiona	I Joint Inventor, if any:	□Аре	etition ha	s been filed	for this ur	nsigned inven	tor				
Given Name (first	and middle [if any])	Famil	y Name	or Surname	u .	85.52-116					
Inventor's Signature	T					Date					
Residence: City		State		Country		Citizenship	1				
Mailing Address					-						
City		State		ZIP		Country					



08/14/03

Express Mail No. EV335405389US Attorney Docket No. SRC015 Client/Matter No. 80404,0018

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. 10/285,318

Filed: October 31, 2002

For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS Group Art Unit: 2121

Examiner: Not yet assigned

Confirmation No.: 1420

RECEIVED

AUG 1 8 2003

Technology Center 2100

CERTIFICATE OF MAILING BY EXPRESS MAIL

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 Sir:

The undersigned hereby certifies that the attached:

- 1. Information Disclosure Statement;
- Form PTO/SB/08A, with references;
- Certificate of Mailing; and
- 4. Return card

relating to the above application, were deposited as "Express Mail" Mailing Label No. EV335405389US, with the United States Postal Service, addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 13 Amaging 2013

13 August 2003

Date

Aug. 13, 2003

Mailer

Peter J. Meza, Reg. No. 32,920 HOGAN & HARTSON LLP

One Tabor Center

1200 17th Street, Suite 1500

Denver, Colorado 80202

(719) 448-5900 Tel (303) 899-7333 Fax

IIICS - 80404/0018 - 62565 v1



Express Mail No. EV335405389US Attorney Docket No. SRC015 Client/Matter No. 80404.0018

#### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. 10/285,318

Filed: October 31, 2002

For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

Group Art Unit: 2121

Examiner: Not yet assigned

Confirmation No.: 1420

RECEIVED

AUG 1 8 2003

Technology Center 2100

# INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Applicant hereby submits for filing under 37 CFR 1.97 a disclosure statement. In submitting these references, no representation is made or implied that the references are or are not material to the examination of this application. The patents, publications or other information of which Applicant is presently aware are listed in Form PTO/SB/08A submitted herewith and copies of all such patents and publications are attached hereto.

No fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

Peter J. Meza, Reg. No. 32,920

HOGAN & HARTSONLL

One Tabor Center

1200 17th Street, Suite 1500

Denver, Colorado 80202

(719) 448-5906 Tel

(303) 899-7333 Fax

IIICS - 80404/0018 - 62565 v1

PTO/SB/08A (10/01)
(Substitute for form 1449ARTO) TRA

## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

Sheet \_\_\_1\_\_ of \_\_\_4\_\_

ATTY.	DOCKET	NO.	SR	C01	5
Client	Matter No	0. 80	404.	001	8

APPLICATION NO. 10/285,318

FIRST NAMED INVENTOR

Jon M. Huppenthal and David E. Caliga

RECEIVED

FILING DATE October 31, 2002 ART UNIT 2121

AUG 1 8 2003

### U.S. PATENT DOCUMENTS

Technology Center 2100

Examiner Initials	Cite No.	Document No. No. – Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-5,230,057	07/20/93	Shido, et al.	
10000		US-5,892,962	04/06/99	Cloutier	FO. 2 114F
		US-5,903,771	05/11/1999	Sgro et al.	Figs 1 & 6, col. 3, lines 30-67, col 4, lines 1-51, col 7, lines 1-27.
		US-6,192,439	02/20/2001	Grunewald et al.	Fig 3, col 3, lines 53-67, col 4, lines 1-64.
		US-6,076,152	06/13/2000	Huppenthal et al.	
		US-6,052,773	04/18/2000	DeHon et al.	
		US-6,226,776	05/01/2001	Panchul et al.	
		US-6,023,755	02/08/2000	Casselman	
		US-5,737,766	04/07/1998	Tan	
1 311,120,000		US-5,570,040	10/29/1996	Lytle et al.	
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## FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Doc cntry code – No. – Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns. Lines Where Relevant Passages or Relevant Figures Appear	TRANSL	ATION
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		-57cm-5c5					

## OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher, city and/or country where published
1000	7	AGARWAL, A., et al., "The Raw Compiler Project", pages 1-12, <a href="http://cag-www.lcs.mit.edu/raw">http://cag-www.lcs.mit.edu/raw</a> , Proceedings of the Second SUIF Compiler Workshop, Augs. 21-23, 1997.
		ALBAHARNA, OSAMA, et al., "On the viability of FPGA-based integrated coprocessors", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 206-215.
		AMERSON, RICK, et al., "TeramacConfigurable Custom Computing", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 3 38.

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13	N N	Sheet 2 of _
Br	2	BARTHEL, DOMINIQUE August 25-26, 1997, "PVP a Parallel Video coProcessor", Hot Chips IX, Pages 203-210.
PARNT & TO	1	BERTIN, PATRICE, et al., "Programmable active memories: a performance assessment", © 1993 Massachusetts Institute o —Technology, Pages 88-102.
	7	BITTNER, RAY, et al., "Computing kernels implemented with a wormhole RTR CCM", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 98-105.
	+	BUELL, D., et al. "Splash 2: FPGAs in a Custom Computing Machine – Chapter 1 – Custom Computing Machines: An Introduction", Pages 1-11, <a href="http://www.computer.org/espress/catalog/bp07413/spls-ch1.html">http://www.computer.org/espress/catalog/bp07413/spls-ch1.html</a> (originally believed published in J. of Supercomputing, Vol. IX, 1995, PP. 219-230.
*	7	CASSELMAN, STEVEN, "Virtual Computing and The Virtual Computer", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 43 48.
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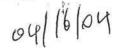
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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. 10/285,318

Filed: October 31, 2002

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MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM

AND PERFORMANCE OF COMPUTATIONAL

**FUNCTIONS** 

Confirmation No.: 1420

Examiner:

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Jon M. Huppenthal and David E. Caliga

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Confirmation No.: 1420

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Substitute for t	orm 1449A/PTO			Application Number	10/285,318
				Filing Date	October 31, 2002
INFORMATION DISCLOSURE				First Named Inventor	Jon M. Huppenthal et al.
SIA	STATEMENT BY APPLICANT			Art Unit	2121
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			U.S. PATENT	DOCUMENTS		
Examiner Initials	Cite No.1	Document No. No. – Kind Code <sup>2</sup>	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Releva Passages or Relevant Figures Appea	
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Application of: Jon M. Huppenthal and David E. Caliga

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Art Unit: 2121

Examiner: Not yet assigned Attorney Docket No. SRC015

For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR

ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

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In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. 10/285,318

Filed: October 31, 2002

Filed. October 51, 2007

For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND

TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL

**FUNCTIONS** 

Confirmation No.: 1420

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Pursuant to 37 C.F.R. § 1.97(c), it is hereby certified that each item in this Information Disclosure Statement was cited in a communication from a foreign patent office (copy enclosed) in counterpart European application, <a href="PCT/US03/29444">PCT/US03/29444</a>, mailed <a href="Mailed 02 MAR 2005">02 MAR 2005</a>, not more than three months prior to the filing of the statement (37 C.F.R. Section 1.97(e)). No petition fee is believed required, however, any fees associated with this communication may be made to Deposit Account No. 50-1123.

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Substitute for	r form 1449A/PT			Application Number	10/285,318	
				Filing Date	October 31, 2002	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				First Named Inventor	Jon M. Huppenthal et al.	
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SRC015 PCT		1	within 1 months/days from the above date of mailing
International application No.	International filing date	(day/month/year)	Priority date (day/month/year)
PCT/US03/29444	16 September 2003 (16.	09 2003)	
International Patent Classification (IPC)	or both national classificat	tion and IPC	31 October 2002 (31.10.2002)
IPC(7): G06F 15/80, 17/16 and US C1.: Applicant SRC COMPUTERS, INC.	712/15; 708/509		
-50 10 5014			
2. This opinion contains indicate  I Basis of the opinion  II Priority  III Non-establishment  IV Lack of unity of it  V Reasoned statement  citations and explat  VII Certain documents  VII Certain defects in the Certain observation  3. The applicant is hereby invite  When? See the time in  this Authority.	tof opinion with regard to avenuion at under Rule 66.2 (a)(ii) a mations supporting such sustained the international applications on the international applications of the inter	ng items; novelty, inventive s with regard to novel atement  n lication  applicant may, beforeste 66.2(4).	eliminary Examining Authority.  Interp and industrial applicability  y, inventive step or industrial applicability;
1927	me me implement of the mine	axunenus, see kuies	ate, by amendments, according to Rule 66.3. 66.8 and 66.9.
For an informa	t communication with the	amendments and/or	arguments, see Rule 66.4 bis.
If no reply is filed, the interna	uional preliminary examin	ation report will be	established on the basis of this opinion.
The final date by which the interest examination report must be estimated.	CTDZDDDSI fireliminaru		
Name and mailing address of the IPEAN	IIS I		
Mail Stop PCT, Attr: IPEA/US	1	A	
Commissioner for Patents P.O. Box 1450		Authorized officer	James P. Matthew
P.O. Box 1450 Alexandria, Virginia 22313-1450 esimile No. (703)305-3230		Authorized officer Fric Coleman Telephone No. (703	James R. Matthew

PAGE 4/8 \* RCVD AT 4/26/2005 4:17:29 PM [Eastern Daylight Time] \* SVR:USPTO-EFXRF-1/2 \* DNIS:8729306 \* CSID:+ \* DURATION (mm-ss):02-24

A STATE OF THE STA	International application No.
WRITTEN OPINION	PCT/US03/29444
I. Basis of the opinion	
1. With regard to the elements of the international application:*	10
the international application as originally filed	
the description:	
pages 1-20 as originally filed	
pages NONE , filed with the demand	
pages NONE , filed with the letter of	
the claims:	
pages 21-23 , as originally filed	
pages NONE , as amended (together with any st	atement) under Article 19
pages NONE , filed with the demand	- AND AND SET LITERATURE CONTROL CONTROL CONTROL
pages NONE, filed with the letter of	
the drawings:	<del> </del>
pages 1-20 , as originally filed	5
pages NONE . filed with the demand	
pages NONE, filed with the letter of	
the sequence listing part of the description:	
pages NONE as originally filed	
pages NONE , filed with the demand	
pages NONE , filed with the letter of	
the language of a translation furnished for the purposes of the language of publication of the international application the language of the translation furnished for the purposes of 55.2 and/or 55.3).	(under Rule 48.3(b)).
With regard to any nucleotide and/or amino acid sequence discopinion was drawn on the basis of the sequence listing:	closed in the international application, the written
contained in the international application in printed form.	
filed together with the international application in computer	randahla faux
furnished subsequently to this Authority in written form.	readable form.
furnished subsequently to this Anthority in computer readab	1. 6.
The statement that the subsequently forming the reader	ie form.
The statement that the subsequently furnished written sequer international application as filed has been furnished.	
The statement that the information recorded in computer real has been furnished.	dable form is identical to the written sequence listing
The amendments have resulted in the cancellation of:	
the description, pages NONE	
the claims. Nos. NONE	
the drawings, sheets/fig NONE	
This opinion has been drawn as if (some of) the amendments had no beyond the disclosure as filed, as indicated in the Supplemental Box	(Rule 70,2(c)).
eplacement sheets which have been furnished to the receiving Office in re opinion as "originally filed."	sponse to an invitation under Article 14 are referred to in
PCT/IPFA//OS /Box D /July 1009	

PAGE 5/8 \* RCVD AT 4/26/2005 4:17:29 PM [Eastern Daylight Time] \* SVR:USPTO-EFXRF-1/2 \* DNIS:8729306 \* CSID; + \* DURATION (mm-ss):02-24

WRITTEN OPINIO	N .		PCT/US03/29444		
Reasoned statement under Rule 66.2(a) citations and explanations supporting st	y, inventive step or industrial appl	step or industrial applicability;			
STATEMENT					
Novelty (N)	Claims	1-13		YES	
		NONE		NO	
Inventive Step (IS)	Claims	6-12		YES	
andan v and (15)		1-5,13		NO	
Industrial Applicability (IA)	Claims	1-13		YES	
		NONE		NO	
CITATIONS AND EXPLANATIONS case Sec Continuation Sheet					
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PAGE 6/8 \* RCVD AT 4/26/2005 4:17:29 PM [Eastern Daylight Time] \* SVR:USPTO-EFXRF-1/2 \* DNIS:8729306 \* CSID:+ \* DURATION (mm-ss):02-24

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04-26-2005 13:21

WRITTEN OPINION

International application No. PCT/US03/29444

Supplemental Box

(To be used when the space in any of the preceding boxes is not sufficient)

TIME LIMIT:

The time limit set for response to a Written Opinion may not be extended. 37 CFR 1.484(d). Any response received after the expiration of the time limit set in the Written Opinion will not be considered in preparing the International Preliminary Examination

V. 2. Citations and Explanations:

Claims 1-2 Jack an inventive step under PCT Article 33(3) as being obvious over Gupta (US patent No. 6,385,757) in view of Khan

Gupta taught the invention substantially as claimed including a data processing ("DP") system comprising: defining a calculation for a reconfigurable computing system instantiating the performance of at least two array functional units (FU00-FUIO)(e.g., see col. 17, lines 28-52 and col. 21, lines 22-29) to perform the calculation.

Gupta did not expressly detail utilizing the array functional units to operate on a subsequent data dimension of the calculation and substantially concurrently using the second of the array units to operate on a previous data dimension of the calculation. Khan however taught operating on three dimensions using plural two dimensional arrays that operate concurrently on respective dimensions and are coupled to together to produce the three dimensional array (e.g., see col. 4, lines 35-62 and col. 12, lines 15-55).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Gupta and Khan. One of ordinary skill would have been motivated to incorporate the three dimensional array operation of the Khan reference into the Gupta system to allow the combined system to be able to perform calculations on more complicated (three dimensional) problems. As to claim 2, Knan taught the calculation comprising plurality of planes (e.g., see col. 12, lines 15-55).

Claim 3 lacks as inventive step under PCT Article 33(3) as being obvious over the prior art as applied in the immediately preceding paragraph and further in view of Leeland (US patent No. 4,872,133). Leeland taught calculation comprised a financial application modeling using a spreadsheet application (e.g., see col. 5, lines 3-32).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Leeland and Gupta. One of

ordinary skill would have been motivated to incorporate the Leeland teaching of financial spreadsheet application for an array processor in order to provide an additional use for the combined system.

Claims 4-5 lack an inventive step under PCT Article 33(3) as being obvious over the prior art (Gupta and Khan) as applied in the immediately preceding paragraphs and further in view of Benner (US Patent No. 5,071,371).

Benner taught the calculation comprising fluid flow calculation and structural analysis (e.g., see col. 22, lines 35-52). It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Benner and Gupta. One of ordinary skill would have been motivated to incorporate the Benner teaching of fluid flow and structural analysis applications for an array processor in order to provide an additional uses for the combined system.

Claim 13 tacks an inventive step under PCT Article 33(3) as being obvious over Gupta (US Patent No. 6,385,757). Gupta raught the invention substantially as claimed including data processing ("DP") system comprising a reconfigurable processor that provides indication of whether it performs speculative and systolic processing (e.g., see col. 15, lines 6-66). Consequently, one

Form PCT/IPEA/408 (Supplemental Box) (July 1998)

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WRITTEN OPINION

International application No. PCT/US03/29444

Supplemental Box

(To be used when the space in any of the preceding boxes is not sufficient)

ordinary skill would have been motivated to perform systolic and speculative processing at least in order to utilize the parameters indicated by Gupta for use in systolic and speculative processing (e.g., see col. 15, lines 56-63).

Claims 6-12 the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the combination of features in independent claims 6 and 12. The combination features in claim 6 comprise defining a first systolic wall comprising rows and cells forming a subset of the plurality of functional units; computing a value at each of the cells in at least a first row of the first systolic wall; communicating the values between cells in the first row of the cells to produce updated values; communicating the updated values to a second row of the first systolic wall; and substantially concurrently providing the updated values to a first row of a second systolic wall of rows of cells in the subset of the plurality of functional units. In claim 12 the combination of features comprise performing a calculation by a subset of the plurality of functional units to produce computed data; passing the computed data from a first column of the calculation to a next column in the calculation; evaluating a rate of change in at least one variable for each of the columns in the calculation; comining the calculation where the variable does not change for a particular column of the calculation; and restarting the calculation at the column of the calculation where the variable does change.

US 6,385,757 B1 (GUPTA) 07 May 2002, see column, 2, lines 20-27, column 15, lines 5-66.

US 4,872,133 A (LEELAND) 03 October 1989, see figs. 2,3,5, and col. 3, lines 27-55.

US 5,274,832 A (KHAN) 28 December 1993, see fig.18, col. 5, lines 27-49,col. 8, lines 42-59, and col. 12, lines 1-55.

US 5,072,371 (BENNER) 10 December 1991 see figs. 5,7,14 and col. 22, lines 35-62.

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PAGE 8/8 \* RCVD AT 4/26/2005 4:17:29 PM [Eastern Daylight Time] \* SVR:USPTO-EFXRF-1/2 \* DNIS:8729306 \* CSID:+ \* DURATION (mm-ss):02-24

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
E	16	speculat\$3 with systolic\$4	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 07:38
L2	343	speculat\$3 and systolic\$4	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:16
L3	1	speculat\$3 and (systolic\$4 adj process\$3)	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 07:49
L4	140	rate near3 change near3 column\$1	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 07:49
L5	1951069	@ay>"2000"	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:16
L6	127	2 not 5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:33
17	332	column\$1 near3 value near3 change\$1	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:35
L8	62	restart\$3 and 7	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:37
L9	42	until adj value adj change\$2	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:36
L10	201	712/15.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:37
65	46	712/19.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:37
L12	359	712/226.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:37
L13	2	(("6385757") or ("5274832")).PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:50
L14	3	(("6385757") or ("5274832") or ("5071371")).PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:57
L15	4	(("6385757") or ("5274832") or ("5071371") or ("4872133")).PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:03

L16	0	("bennerand(fluidadjflow)").PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:06
L17	74	benner and (fluid adj flow)	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:23
L18	2089	imaging and systolic\$5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:23
L19	86	imaging with systolic\$5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:38
L20	4	search adj algorithm with systolic\$5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:48
L21	3	encryption with systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:57
L22	0	genetic near3 match\$3 with systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:57
L23	25	genetic with systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:58
L24	5	dna with systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:00
L25 -	72	protein with systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:01
L26	12835	dna near3 match\$3 systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:02
L27	8	dna near3 match\$3 and systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:02



## UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION N	0.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/285,318 10/31/2002 Jon M. Huppenthal		SRC015 1420			
25235	7590	10/07/2005		EXAM	INER
		SON LLP TER, SUITE 1500		COLEMA	N, ERIC
	ENTEEN'			ART UNIT	PAPER NUMBER
DENVER	, CO 802	202		2183	
				DATE MAIL ED. 10/07/2001	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)					
	10/285,318	HUPPENTHAL ET AL.					
Office Action Summary	Examiner	Art Unit					
	Eric Coleman	2183					
The MAILING DATE of this communication ap eriod for Reply	ppears on the cover sheet wit	th the correspondence address					
A SHORTENED STATUTORY PERIOD FOR REPL WHICHEVER IS LONGER, FROM THE MAILING ID.  - Extensions of time may be available under the provisions of 37 CFR 1. after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period.  - Failure to reply within the set or extended period for reply will, by statut Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNIC .136(a). In no event, however, may a re d will apply and will expire SIX (6) MONT te, cause the application to become AB/	CATION.  pply be timely filed  THS from the mailing date of this communication.  ANDONED (35 U.S.C. § 133).					
tatus							
1) Responsive to communication(s) filed on							
2a) ☐ This action is <b>FINAL</b> . 2b) ☑ Thi	is action is non-final.						
3) Since this application is in condition for allows							
closed in accordance with the practice under	Ex parte Quayle, 1935 C.D.	. 11, 453 O.G. 213.					
isposition of Claims							
4) Claim(s) 1-55 is/are pending in the application	n.						
4a) Of the above claim(s) is/are withdra	awn from consideration.						
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1-55</u> is/are rejected.							
7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/o	or election requirement.						
pplication Papers							
9) The specification is objected to by the Examin	er.						
10) The drawing(s) filed on is/are: a) acc	cepted or b) objected to b	by the Examiner.					
Applicant may not request that any objection to the	e drawing(s) be held in abeyand	ce. See 37 CFR 1.85(a).					
Replacement drawing sheet(s) including the correct	-	1,000					
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
riority under 35 U.S.C. § 119							
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>							
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tachment(s)	"D	STEER ST					
Notice of References Cited (PTO-892)	4) I Intonuou Ci	Immary (PTO-413)					
	☑ Notice of References Cited (PTO-892)       4)       ☐ Interview Summary (PTO-413)         ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)       Paper No(s)/Mail Date         ☑ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)       5)       ☐ Notice of Informal Patent Application (PTO-152)						

U.S. Patent and Trademark Office PTOL-326 (Rev. 7-05)

Office Action Summary

Part of Paper No./Mail Date 100305

Art Unit: 2183

#### **DETAILED ACTION**

## Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- Claims 1-5,26-31,52,53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta (US patent No. 6,385,757) in view of Khan US Patent No. 5,274,832).
- 3. Gupta taught the invention substantially as claimed including a data processing ("DP") system comprising: defining a calculation for a reconfigurable computing system instantiating the performance of at least two array functional units (FU00-FU10)(e.g., see col. 17, lines 28-52 and col. 21, lines 22-29) to perform the calculation.
- 4. Gupta did not expressly detail utilizing the array functional units to operate on a subsequent data dimension of the calculation and substantially concurrently using the second of the array units to operate on a previous data dimension of the calculation. Khan however taught operating on three dimensions using plural two dimensional arrays that operate concurrently on respective dimensions and are coupled to together to produce the three dimensional array (e.g., see col. 4, lines 35-62 and col. 12, lines 15-55).
- 5. It would have been obvious to one of ordinary skill in the DP art to combine the

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teachings of Gupta and Khan. One of ordinary skill would have been motivated to incorporate the three dimensional array operation of the Khan reference into the Gupta system to allow the combined system to be able to perform calculations on more complicated (three dimensional) problems.

- 6. As to the further limitations of claim 26, Khan taught (e.g., see fig. 8) a three dimensional systolic array with connections between processors in three dimensions.
- 7. As to claim 2-5,27-30 Khan taught the calculation comprising plurality of planes, and grid points and plural time-steps and vectors(e.g., see fig. 8 and col. 12, lines 15-55). As per claim 31, the system taught by Khan shows direct connection between the processing elements in the array and therefore the storing of data to an extrinsic memory (i.e., outside the array) would have been unnecessary when the transfer of data between columns was performed (e.g., see fig. 8).
- 8. As to the limitations of claims 52 and 53 the reconfigurable systolic processor would have been able to adapt to the application an therefore would have been an adaptive processor. As to the processor comprising a microprocessor one of ordinary skill would have been motivated to implement the systolic processor as described above as an microprocessor at least to take advantage of the reduced cost and reduced system size as was well known in the art at the time of the claimed invention.
- Claims19,45 are rejected under 35 U.S.C. 103(a) as being unpatentable over
   Gupta and Khan as applied to claims 1-2,26 above, and further in view of Leeland (US patent No. 4,872,133).

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 Leeland taught calculation comprised a financial application modeling using a spreadsheet application (e.g., see col. 5, lines 3-32).

- 11. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Leeland and Gupta. One of ordinary skill would have been motivated to incorporate the Leeland teaching of financial spreadsheet application for an array processor in order to provide an additional use for the combined system.
- 12. Claim 10-16 and 36-42,54 rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Benner (US Patent No. 5,072,371).
- 13. Benner taught the calculation comprising fluid flow calculation and structural analysis (e.g., see col. 22, lines 35-52).
- 14. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Benner and Gupta. One of ordinary skill would have been motivated to incorporate the Benner teaching of fluid flow and structural analysis applications for an array processor in order to provide an additional uses for the combined system.
- 15. As to the limitation in claim 54 of performing a calculation unit a variable changed is value in a system processing an restarting at that value The Benner system taught systolically performing calculations on fluid flow. Since in such a problem one of ordinary skill would at times be interested when a change in the data occurred and adjust the calculation to pin point the calculation around that certain point then one of ordinary skill would have been motivated to operate the Benner and Gupta and Khan

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system to process systolically until a change in data occurred and then restart the calculation at the point of the change to better determine the magnitude of the change in data.

- 16. Claim 6-9,25,32-35,51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Helbig (US patent No. 4,962,381).
- 17. Helbig taught the application of a systolic processor for radar, medical ultrasound and other imaging applications (e.g., see col. 1, lines 1-5) Clearly this would have also comprised images processed by standard MPEG and JPEG standards.
- 18. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Helbig and Gupta. One of ordinary skill would have been motivated to incorporate the Helbig teaching of radar, medical ultrasound and other imaging applications for an systolic processor in order to provide an additional uses for the combined system.
- 19. As to the limitation of claims 25 and 51, since signal filtering would have been associated with the applications taught by Helbig such as radar then one of ordinary skill would have been motivated to use the Helbig systolic processor in signal filtering applications.
- 20. Claim 17,18,22-24,43,44,48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Skaletsky (US patent No. 5,784,108).

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21. Skaletsky taught using an systolic processor for processing search algorithm for image search such as when a best match was to be found and clearly this would have been applicable to data mining as these are similar applications (e.g., see col. 3, line 13-col. 4, line 57).

- 22. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Skaletsky and Gupta. One of ordinary skill would have been motivated to incorporate the Skaletsky teaching of search algorithm applications for an systolic processor in order to provide an additional uses for the combined system.
- 23. As to the limitations of claims 22-24,48-50 in light of the search algorithm teaching especially for finding a best match for data then the use of systolic processors for similar applications such as the genetic pattern matching, protein folding and organic structure interaction would have been an obvious uses for systolic processors (such as taught by Skaletsky) to one of ordinary skill in the DP art.
- 24. Claim 20,21,46,47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Gai (US patent No. 6,061,706).
- 25. Gai taught use of systolic processors in encryption/decryption applications to speed the encryption/decryption of public keys (e.g. see col. 1, lines 25-41.
- 26. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Gai and Gupta. One of ordinary skill would have been motivated to

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incorporate the Gai teaching of encryption and decryption applications for an systolic processor in order to provide an additional uses for the combined system.

Claims 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta
 (US patent No. 6,385,757)

28. Gupta taught the invention substantially as claimed including data processing ("DP") system comprising a reconfigurable processor that provides indication of whether it performs speculative and systolic processing (e.g., see col. 15, lines 6-66). Consequently, one ordinary skill would have been motivated to perform systolic and speculative processing at least in order to utilize the parameters indicated by Gupta for use in systolic and speculative processing (e.g., see col. 15, lines 56-63).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN PRIMARY EXAMINER

#### Application/Control No. Applicant(s)/Patent Under Reexamination 10/285,318 HUPPENTHAL ET AL. Notice of References Cited Examiner Art Unit Page 1 of 1 2183 Eric Coleman **U.S. PATENT DOCUMENTS** Document Number Date Classification Country Code-Number-Kind Code MM-YYYY 10-1989 Leeland, Steven B. 708/509 US-4,872,133 US-5,274,832 12-1993 Khan, Emdadur R. 708/424 В 05-2002 Gupta et al. C US-6,385,757 716/1 D US-5,072,371 12-1991 Benner et al. 712/11 E US-4,962,381 10-1990 Helbig, Sr., Walter A. 342/372 Skaletzky et al. F US-5,784,108 07-1998 375/240.15 US-6,061,706 05-2000 Gai et al. 708/491 G US-US-L US-J US-K US-L US-M FOREIGN PATENT DOCUMENTS Document Number Country Code-Number-Kind Code Date Name Classification Country MM-YYYY N 0 P Q R S T **NON-PATENT DOCUMENTS** Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) U W

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office PTO-892 (Rev. 01-2001)

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Substitute for form 1449A/PTO				Application Number	10/285,318
				Filing Date	October 31, 2002
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				First Named Inventor	Jon M. Huppenthal et al.
			27111	Art Unit	2121
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FIRST NAMED INVENTOR

Jon M. Huppenthal and David E. Caliga

FILING DATE October 31, 2002 ART UNIT RECEIVED

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