US007225324B2

(12) **United States Patent**
Huppenthal et al.

(10) **Patent No.: US 7,225,324 B2**
(45) **Date of Patent: May 29, 2007**

(54) **MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 550 days.

(21) Appl. No.: **10/285,318**

(22) Filed: **Oct. 31, 2002**

(65) **Prior Publication Data**

US 2004/0088527 A1 May 6, 2004

(51) **Int. Cl.**
G06F 17/00 (2006.01)

(52) **U.S. Cl.** **712/226**

(58) **Field of Classification Search** 712/15, 712/19, 226, 215

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,727,503	A		2/1988	McWhirter
4,872,133	A	*	10/1989	Leeland 708/509
4,962,381	A	*	10/1990	Helbig, Sr. 342/372
5,020,059	A		5/1991	Gorin et al.
5,072,371	A	*	12/1991	Benner et al. 712/11
5,230,057	A		7/1993	Shido et al.
5,274,832	A	*	12/1993	Khan 708/424
5,471,627	A		11/1995	Means et al.
5,477,221	A		12/1995	Chang et al.
5,570,040	A		10/1996	Lytle et al.
5,640,586	A	*	6/1997	Pechanek et al. 712/13
5,737,766	A		4/1998	Tan
5,784,108	A	*	7/1998	Skaletzky et al. 375/240.15
5,892,962	A		4/1999	Cloutier
5,903,771	A		5/1999	Sgro et al.
5,915,123	A	*	6/1999	Mirsky et al. 712/16
5,956,518	A	*	9/1999	DeHon et al. 712/15
6,023,755	A		2/2000	Casselman
6,052,773	A		4/2000	DeHon et al.
6,061,706	A	*	5/2000	Gai et al. 708/491
6,076,152	A		6/2000	Huppenthal et al.
6,192,439	B1		2/2001	Grunewald et al.
6,215,898	B1	*	4/2001	Woodfill et al. 382/154
6,226,776	B1		5/2001	Panchul et al.
6,289,440	B1	*	9/2001	Casselman 712/227
6,385,757	B1	*	5/2002	Gupta et al. 716/1

OTHER PUBLICATIONS

Rosenberg, J. M., Dictionary of Computers, Information Processing &Telecommunications, 1984, John Wiley&Sons, 2ed, pp. 496.*

(Continued)

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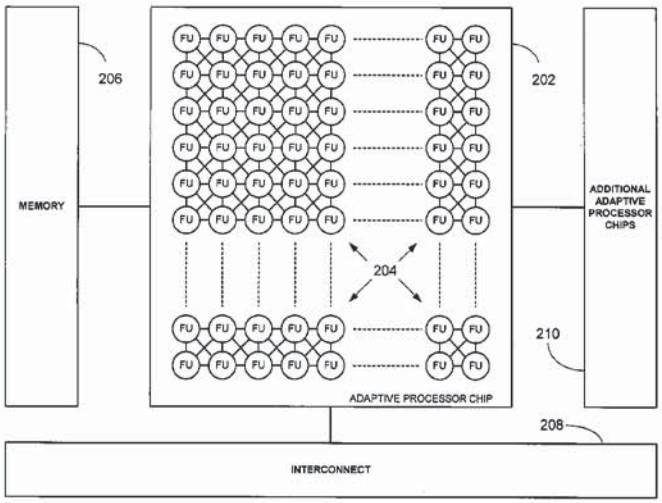
(57) **ABSTRACT**

Multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions are disclosed which can be employed in a myriad of applications including multi-dimensional pipeline computations for seismic applications, search algorithms, information security, chemical and biological applications, filtering and the like as well as for systolic wavefront computations for fluid flow and structures analysis, bioinformatics etc. Some applications may also employ both the multi-dimensional pipeline and systolic wavefront methodologies disclosed.

52 Claims, 20 Drawing Sheets



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OTHER PUBLICATIONS

Agarwal, A., et al., "The Raw Compiler Project", pp. 1-12, http://cag-www.lcs.mit.edu/raw, Proceedings of the Second SUIF Compiler Workshop, Aug. 21-23, 1997.

Albaharna, Osama, et al., "On the viability of FPGA-based integrated coprocessors", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, pp. 206-215.

Amerson, Rick, et al., "Teramac—Configurable Custom Computing", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, pp. 32-38.

Barthel, Dominique Aug. 25-26, 1997, "PVP a Parallel Video coProcessor", Hot Chips IX, pp. 203-210.

Bertin, Patrice, et al., "Programmable active memories: a performance assessment", © 1993 Massachusetts Institute of Technology, pp. 88-102.

Bittner, Ray, et al., "Computing kernels implemented with a wormhole RTR CCM", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, pp. 98-105.

Buell, D., et al. "Splash 2: FPGAs in a Custom Computing Machine—Chapter 1—Custom Computing Machines: An Introduction", pp. 1-11, http://www.computer.org/espress/catalog/bp07413/spls-ch1.html (originally believed published in J. of Supercomputing, vol. IX, 1995, pp. 219-230.

Casselman, Steven, "Virtual Computing and The Virtual Computer", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, pp. 43-48.

Chan, Pak, et al., "Architectural tradeoffs in field-programmable-device-based computing systems", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, pp. 152-161.

Clark, David, et al., "Supporting FPGA microprocessors through retargetable software tools", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, pp. 195-103.

Cuccaro, Steven, et al., "The CM-2X: a hybrid CM-2/Xilink prototype", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, pp. 121-130.

Culbertson, W. Bruce, et al., "Exploring architectures for volume visualization on the Teramac custom computer", © 1996 IEEE, Pub. No. 0-8186-7548-9/96, pp. 80-88.

Culbertson, W. Bruce, et al., "Defect tolerance on the Teramac custom computer", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, pp. 116-123.

Dehon, Andre, "DPGA-Coupled microprocessors: commodity IC for the early 21st century", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, pp. 31-39.

Dehon, A., et al., "MATRIX A Reconfigurable Computing Device with Configurable Instruction Distribution", Hot Chips IX, Aug. 25-26, 1997, Stanford, California, MIT Artificial Intelligence Laboratory.

Dhaussy, Philippe, et al., "Global control synthesis for an MIMD/FPGA machine", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, pp. 72-81.

Elliott, Duncan, et al., "Computational Ram: a memory-SIMD hybrid and its application to DSP", © 1992 IEEE, Publ. No. 0-7803-0246-X/92, pp. 30.6.1-30.6.4.

Fortes, Jose, et al., "Systolic arrays, a survey of seven projects", © 1987 IEEE, Publ. No. 0018-9162/87/0700-0091, pp. 91-103.

Gokhale, M., et al., "Processing in Memory: The Terasys Massively Parallel PIM Array" © Apr. 1995, IEEE, pp. 23-31.

Gunther, Bernard, et al., "Assessing Document Relevance with Run-Time Reconfigurable Machines", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, pp. 10-17.

Hagiwara, Hiroshi, et al., "A dynamically microprogrammable computer with low-level parallelism", © 1980 IEEE, Publ. No. 0018-9340/80/07000-0577, pp. 577-594.

Hartenstein, R. W., et al. "A General Approach in System Design Integrating Reconfigurable Accelerators," http://xputers.informatik.uni-kl.de/papers/paper026-1.html, IEEE 1996 Conference, Austin, TX, Oct. 9-11, 1996.

Hartenstein, Reiner, et al., "A reconfigurable data-driven ALU for Xputers", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, pp. 139-146.

Hauser, John, et al.: "GARP: a MIPS processor with a

Hayes, John, et al., "A microprocessor-based hypercube, supercomputer", © 1986 IEEE, Publ. No. 0272-1732/86/1000-0006, pp. 6-17.

Herpel, H.-J., et al., "A Reconfigurable Computer for Embedded Control Applications", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, pp. 111-120.

Hogl, H., et al., "Enable++: A second generation FPGA processor", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, pp. 45-53.

King, William, et al., "Using MORRPH in an industrial machine vision system", © 1996 IEEE, Publ. No. 08186-7548-9/96, pp. 18-26.

Manohar, Swaminathan, et al., "A pragmatic approach to systolic design", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0463, pp. 463-472.

Mauduit, Nicolas, et al., "Lneuro 1.0: a piece of hardware LEGO for building neural network systems," © 1992 IEEE, Publ. No. 1045-9227/92, pp. 414-422.

Mirsky, Ethan A., "Coarse-Grain Reconfigurable Computing", Massachusetts Institute of Technology, Jun. 1996.

Mirsky, Ethan, et al., "MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, pp. 157-166.

Morley, Robert E., Jr., et al., "A Massively Parallel Systolic Array Processor System", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0217, pp. 217-225.

Patterson, David, et al., "A case for intelligent DRAM: IRAM", Hot Chips VIII, Aug. 19-20, 1996, pp. 75-94.

Peterson, Janes, et al., "Scheduling and partitioning ANSI-C programs onto multi-FPGA CCM architectures", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, pp. 178-187.

Schmit, Herman, "Incremental reconfiguration for pipelined applications," © 1997 IEEE, Publ. No. 0-8186-8159-4/97, pp. 47-55.

Sitkoff, Nathan, et al., "Implementing a Genetic Algorithm on a Parallel Custom Computing Machine", Publ. No. 0-8186-7086-X/95, pp. 180-187.

Stone, Harold, "A logic-in-memory computer", © 1970 IEEE, IEEE Transactions on Computers, pp. 73-78, Jan. 1990.

Tangen, Uwe, et al., "A parallel hardware evolvable computer POLYP extended abstract", © 1997 IEEE, Publ. No. 0-8186-8159/4/97, pp. 238-239.

Thornburg, Mike, et al., "Transformable Computers", © 1994 IEEE, Publ. No. 0-8186-5602-6/94, pp. 674-679.

Tomita, Shinji, et al., "A computer low-level parallelism QA-2", © 1986 IEEE, Publ. No. 0-0384-7495/86/0000/0280, pp. 280-289.

Trimberger, Steve, et al., "A time-multiplexed FPGA", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, pp. 22-28.

Ueda, Hirotada, et al., "A multiprocessor system utilizing enhanced DSP's for image processing", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0611, pp. 611-620.

Villasenor, John, et al., "Configurable computing", © 1997 Scientific American, Jun. 1997.

Wang, Quiang, et al., "Automated field-programmable compute accelerator design using partial evaluation", © 1997 IEEE, Publ. No. 0-8186-8159-4/97. pp. 145-154.

W.H. Manglone-Smith and B.L. Hutchings. Configurable computing: The Road Ahead. In Proceedings of the Reconfigurable Architectures Workshop (RAW'97), pp. 81-96, 1997.

Wirthlin, Michael, et al., "The Nano processor: a low resource reconfigurable processor", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, pp. 23-30.

Wirthlin, Michael, et al., "A dynamic instruction set computer", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, pp. 99-107.

Wittig, Ralph, et al., "One Chip: An FPGA processor with reconfigurable logic", © 1996 IEEE, Publ. 0-8186-7548-9/96, pp. 126-135.

Yamauchi, Tsukasa, et al., "SOP: A reconfigurable massively parallel system and its control-data flow based compiling method", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, pp. 148-156.

DOCKET ALARM
Find authenticated court documents without watermarks at docketalarm.com.

Yun, Hyun-Kyu and Silverman, H. F.; "A distributed memory MIMD multi-computer with reconfigurable custom computing capabilities", Brown University, Dec. 10-13, 1997, pp. 7-13.

Hoover, Chris and Hart, David; "San Diego Supercomputer Center, Timelogic and Sun Validate Ultra-Fast Hidden Markov Model Analysis-One DeCypher-accelerated Sun Fire 6800 beats 2,600 CPUs running Linux-", San Diego Supercomputer Center, http://www.sdsc.edu/Press/02/050802_markovmodel.html, May 8, 2002, pp. 1-3.

Caliga, David and Barker, David Peter, "Delivering Acceleration: The Potential for Increased HPC Application Performance Using Reconfigurable Logic", SRC Computers, Inc., Nov. 2001, pp. 20.

Hammes, J.P., Rinker, R. E.; McClure, D, M., Böhm, A. P. W., Najjar, W. A., "The SA-C Compiler Dataflow Description", Colorado State University, Jun. 21, 2001, pp. 1-25.

Callahan, Timothy J. and Wawrzynek, John, "Adapting Software Pipelining for Reconfigurable Computing", University of California at Berkeley, Nov. 17-19, 2000, pp. 8.

Ratha, Nalini K., Jain, Anil K. and Rover, Diane T., "An FPGA-based Point Pattern Matching Processor with Application to Fingerprint Matching", Michigan State University, Department of Computer Science, pp. 8.

Dehon, André, "Comparing Computing Machines", University of California at Berkeley, Proceedings of SPIE vol. 3526, Nov. 2-3, 1998, pp. 11.

Vemuri, Ranga R. and Harr, Randolph E., "Configurable Computing: Technology and Applications", University of Cincinnati and Synopsys Inc., IEEE, Apr. 2000, pp. 39-40.

Dehon, André, "The Density Advantage of Configurable Computing", California Institute of Technology, IEEE, Apr. 2000. pp. 41-49.

Haynes, Simon D., Stone, John, Cheung, Peter Y.K. and Luk, Wayne, "Video Image Processing with the Sonic Architecture", Sony Broadcast & Professional Europe, Imperial College, University of London, IEEE, Apr. 2000, pp. 50-57.

Platzner , Marco, "Reconfigurable Accelerators for Combinatorial Problems", Swiss Federal Institute of Technology (ETH) Zurich, IEEE, Apr. 2000, pp. 58-60.

Callahan, Timothy J., Hauser, John R. And Wawrzynek, John, "The Garp Architecture and C Compiler", University of California, Berkeley, IEEE, April 2000, pp. 62-69.

Goldstein, Seth Copen, Schmit, Herman, Budiu , Mihai, Cadambi, Srihari, Moe, Matt and Taylor, R. Reed, "PipeRench: A Reconfigurable Architecture and Compiler", Carnegie Mellon University, IEEE, Apr. 2000, pp. 70-76.

Muchnick, Steven S., "Advanced Compiler Design and Implementation", Morgan Kaufmann Publishers, pp. 217.

Hammes, Jeffrey P., Dissertation "Compiling SA-C To Reconfigurable Computing Systems", Colorado State University, Department of Computer Science, Summer 2000, pp. 179.

Automatic Target Recognition, Colorado State University & USAF, http://www.cs.colostate.edu/cameron/applications.html, pp. 1-3.

Chodowiec, Pawel, Khuon, Po, Gaj, Kris, Fast Implementations of Secret-Key Block Ciphers Using Mixed Inner- and Outer-Round Pipelining, George Mason University, Feb. 11-13, 2001, pp. 9.

Miyamori, Takashi, "REMARC: Reconfigurable Multimedia Array Coprocessor", IEICE Transactions on Information and Systems, Information & Systems Society, Tokyo, JP, vol. E82-D, No. 2, Feb. 1999, pp. 389-397, XP000821922.

Gross Thomas, et al., "Compilation for a High-performance Systolic Array", Sigplan Notices USA, vol. 21, No. 7, Jul. 1986, pp. 27-38, XP002418625.

Rauchwerger, Lawrence, et al., "The LRPD Test: Speculative Run-Time Parallelization of Loops with Privatization and Reduction Parallelization", IEEE Transaction on Parallel and Distributed Systems, IEEE Service Center, Los Alamitos, CA, vol. 10, No. 2, Feb. 1999, pp. 160-180, XP000908318.

Arnold Jeffrey M. et al., "The Splash 2 Processor and Applications", Computer Design: VLSI in Computers and Processors, 1993, ICCD '93 Proceedings, 1993 IEEE International Conference on Cambridge, MA, Oct. 3-6 1993, Los Alamitos, CA, IEEE Comput. Soc., Oct. 3, 1993, pp. 482-485, XP010134571.

Hwang, Kai, "Computer Architecture and Parallel Processing", Data Flow Computers and VLSI Computations, 1985, McGraw Hill, Chapter 10, pp. 732-807, XP-002418655.

Hartenstein, Reiner W., et al. "A Synthesis System for Bus-based Wavefront Array Architectures", Proceedings, International Conference on Application-Specific Systems, Architecture and Processors, 1996, pp. 274-283, XP002132819.

Alexander, Thomas, et al. "A Reconfigurable Approach To A Systolic Sorting Architecture", ISCAS 89, May 8, 1989, pp. 1178-1182, XP010084477.

Wu, Youfeng, et al. "Better Exploration of Region-Level Value Locality with Integrated Computation Reuse and Value Prediction", Proceedings of the 28th International Symposium on Computer Architecture, ISCA 2001, Goteberg, Sweden, Jun. 30-Jul. 4, 2001, International Symposium on Computer Architecture, (ISCA), Los Alamitos, CA, IEEE Comp. Soc, US, Jun. 30, 2001, pp. 93-103, XP010552866.

* cited by examiner

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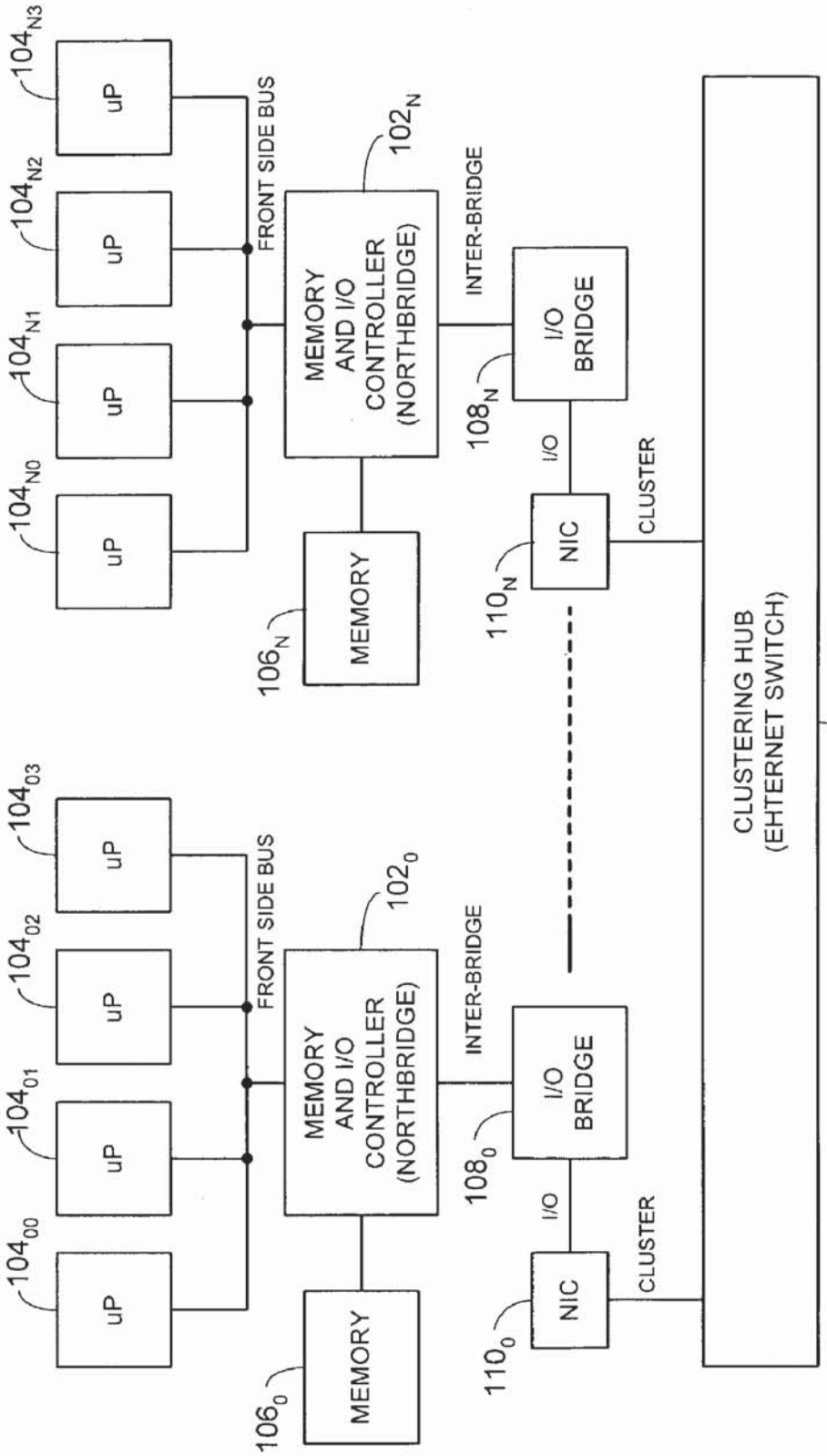

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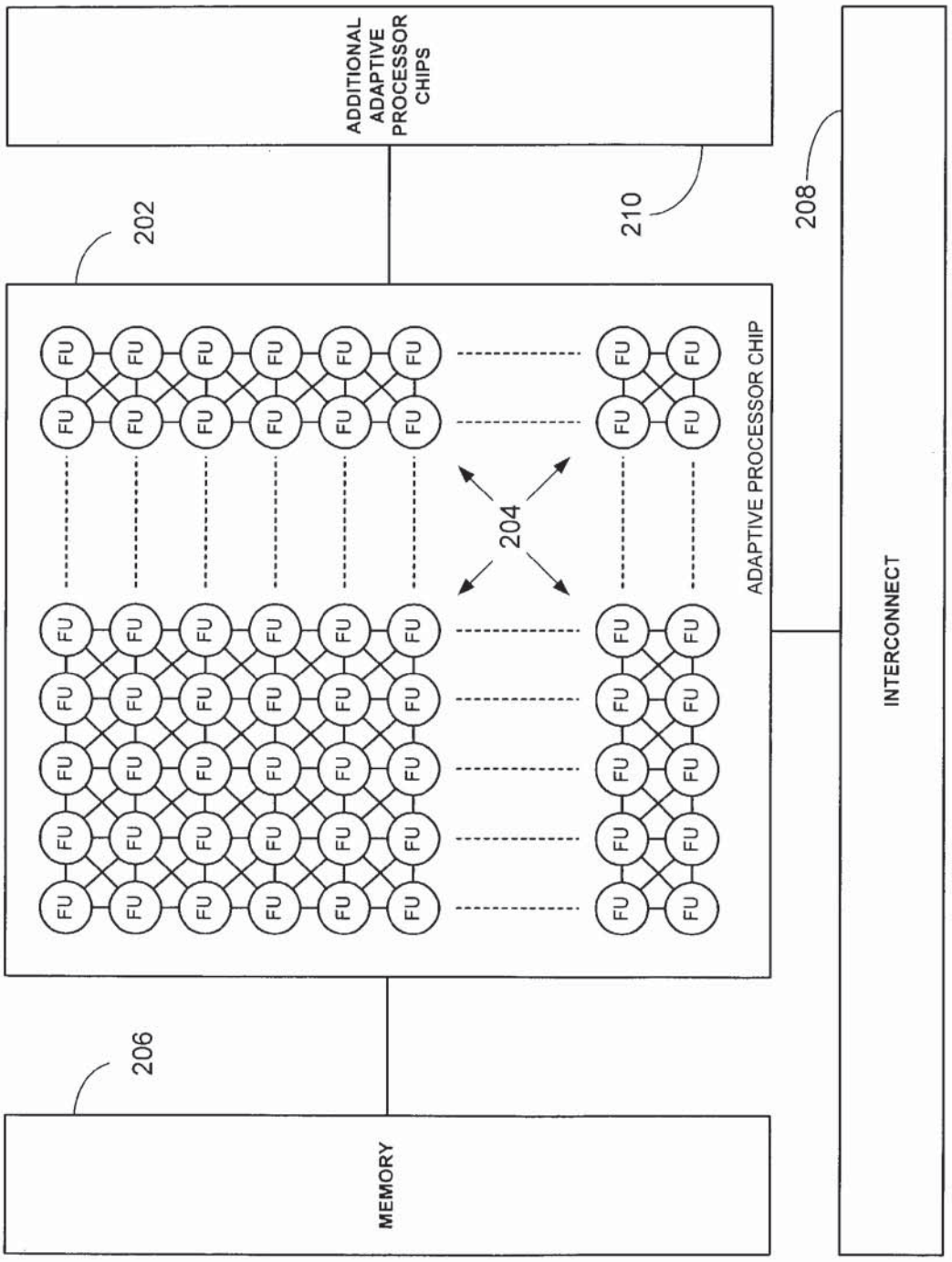

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