Exhibit F-11: Chunky SLD

An article entitled, "Automated Target Recognition on SPLASH 2," by Rencher et al., ("Chunky SLD"), was pu
Symposium on Field-Programmable Custom Computer Machines, pp. 192-200 in 1997, and is therefore prior art
7,620,800 ("'800 Patent") at least under 35 U.S.C. §§ 102(a) and (b).

As described in detail below, Chunky SLD anticipates the asserted claim(s) of the '800 Patent. To the extent it is
SLD does not expressly disclose certain limitations in the asserted claim, such limitations are inherent. Furtherm
found that Chunky SLD does not anticipate the asserted claim, Chunky SLD renders the asserted claim obvious,
combination with other prior art identified in the cover pleading or herein.

This chart is subject to all reservations, objections, and disclaimers in Microsoft's Invalidity Contentions and any
supplement, or modification thereof, which are incorporated herein by reference in their entirety.

Asserted Claim of '800 Patent	**Exemplary Disclosure of Chunky SLD**
[1A] A method for data processing in a reconfigurable computing system, the reconfigurable computing system comprising at least one reconfigurable processor, the reconfigurable processor comprising a plurality of functional units, said method comprising:	At least under Plaintiff's apparent theories of infringement and interpretations alleging that any of Defendant's accused products satisfy this claim limitation or in combination with one or more references, discloses: Chunky SLD at Abstract: "Automated target recognition is an application area purpose hardware to achieve reasonable performance. FPGA-based platforms level of performance for ATR systems if the implementation can be adapted t and routing resources of these architectures. This paper discusses a mapping e linear-systolic implementation of an ATR algorithm is mapped to the SPLASH column-oriented processors were used throughout the design to achieve high p limited nearest-neighbor communication. The distributed SPLASH2 memorie achieve a high degree of parallelism. The resulting design is scalable and can multiple SPLASH2 boards with a linear increase in performance." Chunky SLD at 196: "The actual SPLASH2 platform consists of a board with (plus one for control) arranged in a linear systolic array. Each chip has a limit its two nearest neighbors. Each Xilinx 4010 is connected to a 512 kbyte memo The memory can handle back-to-back reads, or back-to-back writes, but requi around) cycle when changing from write to read. There is also a crossbar conn

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chips that allows some level of random connection between chips. Up to 16 b
chained together to provide a large linear-systolic array of 256 elements."

Chunky SLD at Figure 6:

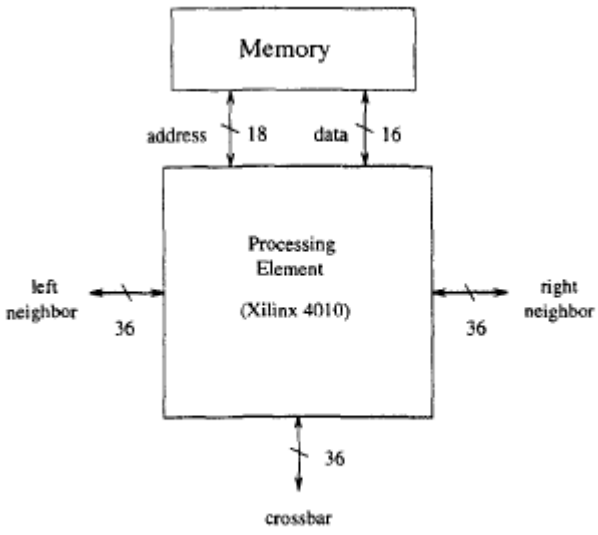

Figure 6: Single Processing Element of SPLASH 2.

Chunky SLD at Figure 7:

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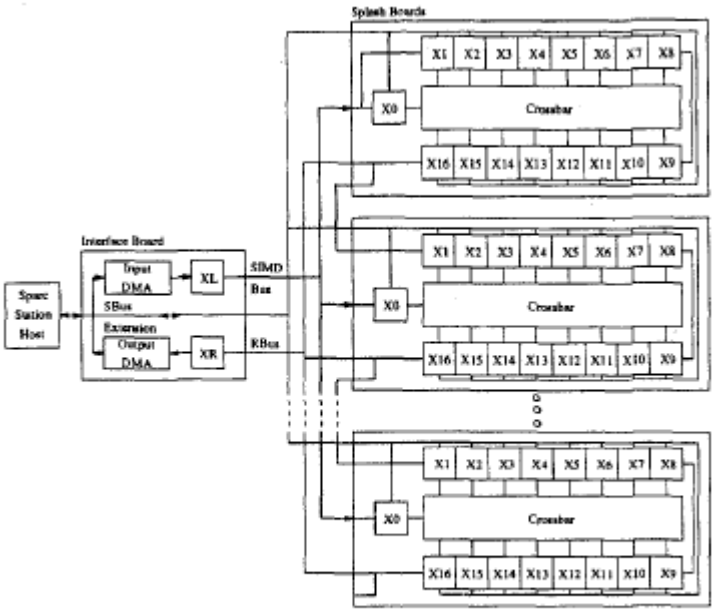

Figure 7: SPLASH 2 platform.

Chunky SLD at Figure 8:

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	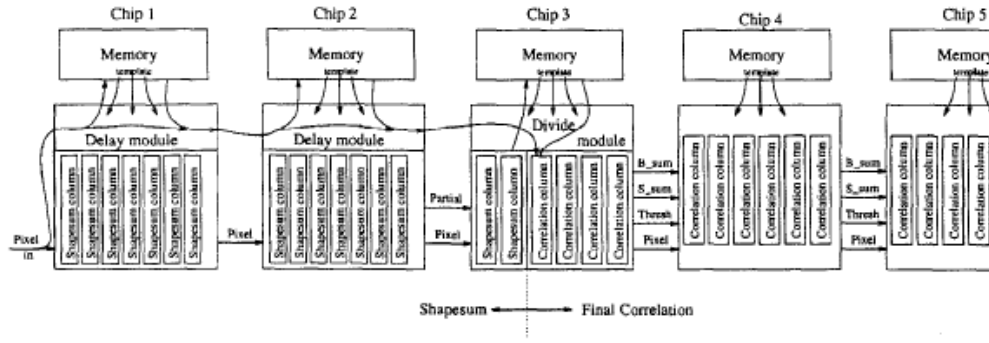 Figure 8: SPLASH 2 Implementation. To the extent Plaintiff asserts this limitation is not expressly or inherently disc apparent claim construction, or any other claim construction, the claimed subj been obvious to a person of ordinary skill in the art considering this reference the knowledge of one of ordinary skill in the art at the time of the alleged inve disclosures in one or more of the references identified in Section I.B.2 of the c
[1B] transforming an algorithm into a data driven calculation that is implemented by said reconfigurable computing system at the at least one reconfigurable processor;	At least under Plaintiff's apparent theories of infringement and interpretations alleging that any of Defendant's accused products satisfy this claim limitation or in combination with one or more references, discloses: Chunky SLD at Abstract: "Automated target recognition is an application area purpose hardware to achieve reasonable performance. FPGA-based platforms level of performance for ATR systems if the implementation can be adapted t and routing resources of these architectures. This paper discusses a mapping e linear-systolic implementation of an ATR algorithm is mapped to the SPLASH column-oriented processors were used throughout the design to achieve high p limited nearest-neighbor communication. The distributed SPLASH2 memories achieve a high degree of parallelism. The resulting design is scalable and can multiple SPLASH2 boards with a linear increase in performance."

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Chunky SLD at 195: “Chunky SLD was implemented on the SPLASH2 board shown itself to be a useful platform and has had numerous applications mapped 10, 111. The implementation was done in VHDL and simulated/synthesized u place and route was done automatically using Xilinx place and route tools.”

Chunky SLD at 196: “The actual SPLASH2 platform consists of a board with (plus one for control) arranged in a linear systolic array. Each chip has a limit its two nearest neighbors. Each Xilinx 4010 is connected to a 512 kbyte memo The memory can handle back-to-back reads, or back-to-back writes, but requi around) cycle when changing from write to read. There is also a crossbar conn chips that allows some level of random connection between chips. Up to 16 b chained together to provide a large linear-systolic array of 256 elements.”

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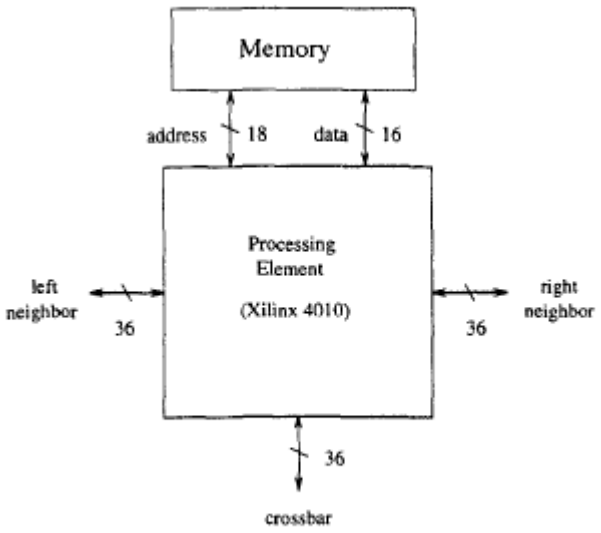

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