

Asserted Claim of '800 Patent	Exemplary Disclosure of RaPiD
<p>[1A] A method for data processing in a reconfigurable computing system, the reconfigurable computing system comprising at least one reconfigurable processor, the reconfigurable processor comprising a plurality of functional units, said method comprising:</p>	<p>At least under Plaintiff's apparent theories of infringement and interpretations of the claim limitation, RaPiD at 106, in combination with one or more references, discloses:</p> <p>RaPiD at Abstract: "The goal of the RaPiD (Reconfigurable Pipelined Datapath) architecture is to provide high performance configurable computing for a range of computationally-intensive applications that demand special-purpose hardware. This is accomplished by mapping a large amount of computation into a deep pipeline using a configurable array of coarse-grained computing elements."</p> <p>RaPiD at 106: "Unfortunately, the promise of configurable computing has yet to be realized because of some very successful examples [1, 9]. There are two main reasons for this."</p> <p>RaPiD at 111: "Since a 2-D DCT performs two multiplies by the same weight matrix, the multiply is only once: one column per cell in both the first 8 cells and last 8 cells. The transpose of the weight matrix multiplies is performed with two local memories per cell: one to store products of the current sub-image and the other to store the products of the previous sub-image. During the current sub-image, the transpose of the previous sub-image computation is passed through the cells. The datapath for one RaPiD cell of a 2-D DCT is shown in Figure 10."</p>

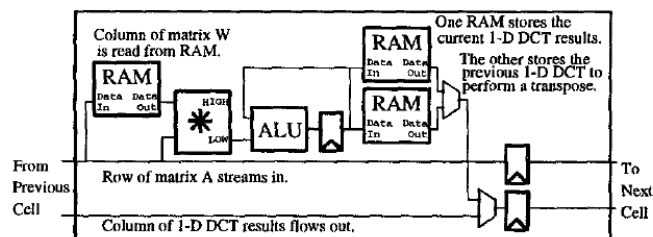


Figure 10: Netlist for one cell of 2-D DCT. The top pipelined bus streams in the **A** matrix while the bottom bus streams out resulting 1-D DCT, transposed. The top bus also streams the **W** columns into the local memories prior to the computation.

RaPiD at 115: "References

[1] J. M. Arnold et al. The Splash 2 processor and applications. In Proceedings IEEE Conference on Computer Design: VLSI in Computers and Processors, pages 482-504. IEEE Soc. Press, 1993."

To the extent Plaintiff asserts this limitation is not expressly or inherently disclosed by the prior art, or by apparent claim construction, or any other claim construction, the claimed subject matter has not been obvious to a person of ordinary skill in the art considering this reference in combination with the knowledge of one of ordinary skill in the art at the time of the alleged invention, and the disclosures in one or more of the references identified in Section I.B.2 of the cover sheet.

[1B] transforming an algorithm into a data driven calculation that is implemented by said reconfigurable computing system at the at least one reconfigurable processor;

At least under Plaintiff's apparent theories of infringement and interpretations of the claims, the combination of the accused product with the prior art, including the combination with one or more references, discloses:

RaPiD at Equations 5 and 6:

$$z_{mj} = \sum_{n=0}^{N-1} a_{mn} w_{nj}, \quad (5)$$

and thus

$$y_{ji} = \sum_{m=0}^{N-1} z_{mj} w_{mi} \quad (6)$$

for $0 \leq i, j \leq N - 1$.

RaPiD at 111: “As seen in Equation 5 and Equation 6, both z_{mj} and y_{ji} are equivalent to matrix multiplies. However, since the z_{mj} values are produced in row-major order but y_{ji} is produced in column-major order, the results from the z_{mj} DCT must be transposed prior to computing y_{ji} , as illustrated in Figure 8. In addition, since both input streams are read in row-major order, it is more desirable to produce row-major output (potentially reducing memory stalls), requiring a transpose of the transform (i.e. output y_{ij} instead of y_{ji}). The resulting computation is $((A \times W)^T \times W)$.”

To the extent Plaintiff asserts this limitation is not expressly or inherently disclosed in the prior art, it is apparent claim construction, or any other claim construction, the claimed subject matter would have been obvious to a person of ordinary skill in the art considering this reference in combination with the knowledge of one of ordinary skill in the art at the time of the alleged invention. The disclosures in one or more of the references identified in Section I.B.2 of the cover page of the patent are hereby incorporated by reference into this document.

[1C] forming at least two of said functional units at the at least one reconfigurable processor to perform said calculation

At least under Plaintiff's apparent theories of infringement and interpretations of the claim, alleging that any of Defendant's accused products satisfy this claim limitation, RaPiD's combination with one or more references, discloses:

RaPiD at 110: "5.1 1-D DCT

An N-point 1-D DCT partitions an input vector A into N-element sub-vectors, and each subvector A_h computes

$$y_{hi} = \sum_{n=0}^{N-1} a_{hn} \cos \frac{\pi i}{2N} (2n + 1) \quad (1)$$

for $0 \leq i \leq N - 1$, where a_{hn} is the n-th element of sub-vector A_h (and the (hN + n)-th element of vector A).¹ The N^2 cosine terms are constant over all subvectors and hence can be precomputed weights W where $w_{ni} = \cos \pi i / 2N(2n + 1)$. This reduces Equation 1 to

$$y_{hi} = \sum_{n=0}^{N-1} a_{hn} w_{ni}, \quad (2)$$

for $0 \leq i \leq N - 1$. By viewing input vector A and weights W as matrices A and W, Equation 2 reduces to the matrix multiply $Y = A \times W$. Thus, to compute a 1-D DCT, RaPiD performs a matrix multiply. To implement an 8 point 1-D DCT on an 8 x 8 input matrix A (i.e. a 64-element vector), the entire 8 x 8 weight matrix W is stored in RaPiD's local memories, one column per cell. Each cell of the resulting pipeline is configured as shown in Figure 7. The A matrix is passed through the pipeline array in row-major order. Within each cell, the local memory address is incremented by one, and a register accumulates the dot product of the stored column and the incoming row. When a cell receives the last element of a row, the resulting product is passed down an output pipeline. The register address is cleared, and the cell is ready to compute the product of the next row on the next clock cycle. This effectively computes the matrix multiply of A x W."

RaPiD at Equations 5 and 6:

$$z_{mj} = \sum_{n=0}^{N-1} a_{mn} w_{nj}, \quad (5)$$

and thus

$$y_{ji} = \sum_{m=0}^{N-1} z_{mj} w_{mi} \quad (6)$$

for $0 \leq i, j \leq N - 1$.

RaPiD at 111: “As seen in Equation 5 and Equation 6, both z_{mj} and y_{ji} are equivalent to matrix multiplies. However, since the z_{mj} values are produced in row-major order but the y_{ji} values are produced in column-major order, the results from the z_{mj} DCT must be transposed prior to computing the y_{ji} DCT, as illustrated in Figure 8. In addition, since both input streams are read in row-major order, it is more desirable to produce row-major output (potentially reducing memory stalls), requiring the y_{ji} to be transposed to produce y_{ij} (i.e. output y_{ij} instead of y_{ji}). The resulting computation is $((A \times W)^T \times W)^T$.”

RaPiD at Figure 8:

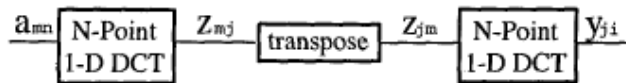


Figure 8: 2-D $N \times N$ DCT

RaPiD at 111: “We show the implementation of an 8×8 2-D DCT on a 16-cell RaPiD. Consider an $M \times N$ image and an 8×8 weight matrix W . First, the image is divided into sub-images of size 8×8 . The computation for each sub-image A is outlined in Figure 9.

RaPiD at 111: “Since a 2-D DCT performs two multiplies by the same weight matrix, the transpose operation is only performed once: one column per cell in both the first 8 cells and last 8 cells. The transpose operation is performed with two local memories per cell: one to store products of the current sub-image and the other to store the products of the previous sub-image. During the

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