THE HONORABLE JAMES L. ROBART

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF WASHINGTON
AT SEATTLE

SRC LABS, LLC & SAINT REGIS MOHAWK TRIBE,

Plaintiffs,

v.

MICROSOFT CORPORATION,

Defendant.

CASE NO. 2:18-cv-00321-JLR

DECLARATION OF TAREK EL-GHAZAWI

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I. INTRODUCTION

1. I have been asked by counsel for Plaintiffs to provide opinions regarding how one of ordinary skill in the art would have understood certain claim terms at issue in this lawsuit.

2. All of the opinions stated in this report are based on my current personal knowledge and professional judgment. If called as a witness during the trial in this matter, I am prepared to testify competently about them.

3. I am being compensated for my work in this matter but my compensation does not depend on the opinions I render or the outcome of this litigation. I do not have a personal interest in the outcome of this litigation.

II. QUALIFICATIONS

4. My *curriculum vitae* is attached as Exhibit A. A summary of my qualifications relevant to this case is provided below.

5. I am a Professor of Electrical and Computer Engineering at The George Washington University (GWU), I have created the NSF Industry/University Center for High-Performance Reconfigurable Computing at GWU and directed it for about ten years, I have led many industry and federally funded research projects in reconfigurable computing and published closed to three hundred research publications. I received many honors in my field, a few examples follow. I was elected an IEEE Fellow for my contributions to reconfigurable computing and parallel programming (only one in a thousand members get that honor) and was awarded the Alexander von Humboldt research award for the same reasons (100 scientists selected from around the world in any year by the Humboldt Foundation in Germany), I am a

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distinguished speaker for the IEEE Computer Society and served as a distinguished visiting fellow for the UK Royal Academy of Engineering.

III. BASIS OF OPINIONS

6. My opinions are abased on my years of education, research, experience, as well as my reading of the patents and prosecution histories. In forming my opinions I have considered the materials identified in this declaration, the patents, and the file histories.

7. I may rely on additional materials and provide additional opinions to respond to arguments raised by the Defendants.

8. This declaration only represents the opinions I have formed to date. I reserve the right to revise, supplement, or amend my opinions based on new information and my continuing analysis of the patents.

IV. BACKGROUND OF THE TECHNOLOGY

A. Traditional Computers

9. Conventional computers, also known as von Neumann machine or von Neumann Computers. In a traditional computer, hardware is fixed and cannot be changed after manufacturing while different software programs use the existing fixed hardware to perform the required application. The software program is simply a sequence of instructions. Both the software program and the data to operate on reside in the main memory and therefore the processor is connected to the main memory through bus lines that include data bus and address bus. The address bus specifies the address of the memory location where the instruction to be performed or the operand to be manipulated reside. The data bus is used to transfer the instruction and input data to the processor and take the results back from the processor to the

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memory. The processor typically goes through a fixed routine of steps to execute the instructions of the software program one by one, this routine is called the instruction execution cycle. The typical steps for such an instruction execution are: Instruction Fetch; Instruction Decode; Execute; Data Memory Access; and Write back the result.

10. Conventional computers suffer many inherent limitations: 1. Their architectural is fixed (rigid) and cannot be configured; 2. Their architectures is complex to satisfy all general computations; and 3. They operate in a sequential many. Applications needs and computations required can however change. Conventional processors will have to use the available chip resources to execute those computation. This is by contrast to FPGAs that are malleable and allow customization to create just as needed simple compute architectures and create as many of those as needed to solve the problem at hand.

B. FPGAs

11. An FPGA, or a Field Programmable Gate Array, is an electronic chip that can be programmed and reprogrammed in the field of application, after manufacturing, to provide different functionalities as needed. To do so, FPGAs are largely comprising configurable logical blocks that can be configured to perform the desired logical functions and a set of connecting configurable interconnects. Configurations are established by a bit stream that is generated by application engineers using some form of programming interface.

C. Relevant Advanced Computing Concepts History of Heterogeneous Computers

12. Many architectural enhancements were developed and leveraged over the years sometimes as a concept utilized internally to enhance the conventional architectures or to be used externally to provide computing acceleration. Among these concepts that are relevant

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here are array processing/spatial parallelism, pipelining, systolic arrays, data flow architectures, vector processors and heterogeneous (accelerated) computing.

13. Array Processing/Spatial Parallelism- when the underlying has a great deal of data parallelism, in other words multiple data items that need to be processed in the same way at the same time, this parallelism can be exploited to speed up the computation. In conventional processors only if multiple independent processing units are available they can be used up to the available fixed number of such units. In the case of FPGAs, as many units as needed by the application are created and used thereby enabling better unitization of the chip and a much more speed of processing.

14. Dataflow Processing: This is a form of processing which is data driven, where rather than executing instructions one by one from the program as in traditional systems (control flow), activities are executed when their input data are received.

15. Pipelining: Pipelining is a form of overlapped processing established by breaking the processor needed for a computation into physical modules, called stages that correspond to the subtasks that make up that overall computation. Computations that correspond to different data can be processed concurrently one by each different stage to gain speed. In conventional processors a pipeline can be used for instruction processing and a fixed number of pipelines can be available for arithmetic.

16. Systolic Arrays: A systolic arrays is a homogeneous array of interconnected processing elements to perform synchronized processing of data as they proceed in a wave-front style through the array. An analogy between the data movement and the blood circulation in the body is the basis for the name.

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