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(54) MULTIPROCESSOR COMPUTER ARCHITECTURE INCORPORATING A PLURALITY OF MEMORY ALGORITHM PROCESSORS IN THE MEMORY SUBSYSTEM

(52) U.S. Cl. 712/15

(57) ABSTRACT

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A multiprocessor computer architecture incorporating a plurality of programmable hardware memory algorithm processors ("MAP") in the memory subsystem. The MAP may comprise one or more field programmable gate arrays ("FPGAs") which function to perform identified algorithms in conjunction with, and tightly coupled to, a microprocessor and each MAP is globally accessible by all of the system processors for the purpose of executing user definable algorithms. A circuit within the MAP signals when the last operand has completed its flow thereby allowing a given process to be interrupted and thereafter restarted. Through the use of read only memory ("ROM") located adjacent the FPGA, a user program may use a single command to select one of several possible pre-loaded algorithms thereby decreasing system reconfiguration time. A computer system memory structure MAP disclosed herein may function in normal or direct memory access ("DMA") modes of operation and, in the latter mode, one device may feed results directly to another thereby allowing pipelining or parallelizing execution of a user defined algorithm. The system of the present invention also provides a user programmable performance monitoring capability and utilizes parallelizer software to automatically detect parallel regions of user applications containing algorithms that can be executed in the programmable hardware.

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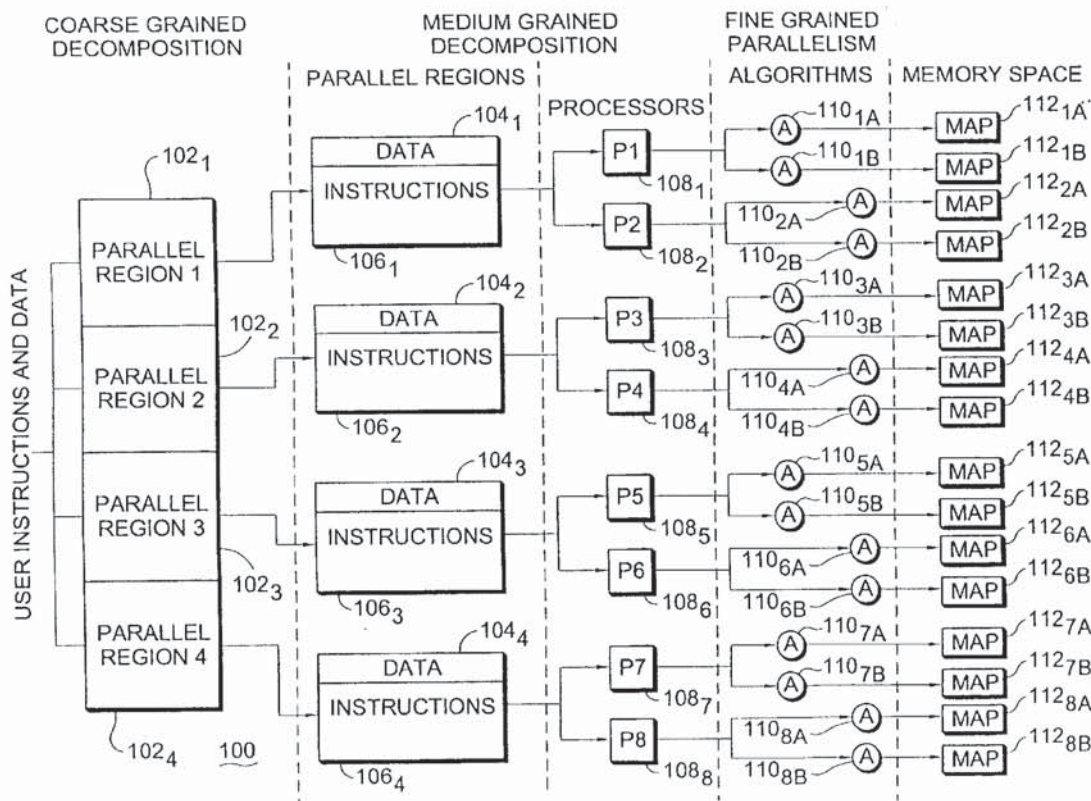
(22) Filed: Jan. 5, 2001

Related U.S. Application Data

(60) Division of application No. 09/481,902, filed on Jan. 12, 2000, now Pat. No. 6,247,110, which is a continuation of application No. 08/992,763, filed on Dec. 17, 1997, now Pat. No. 6,076,152.

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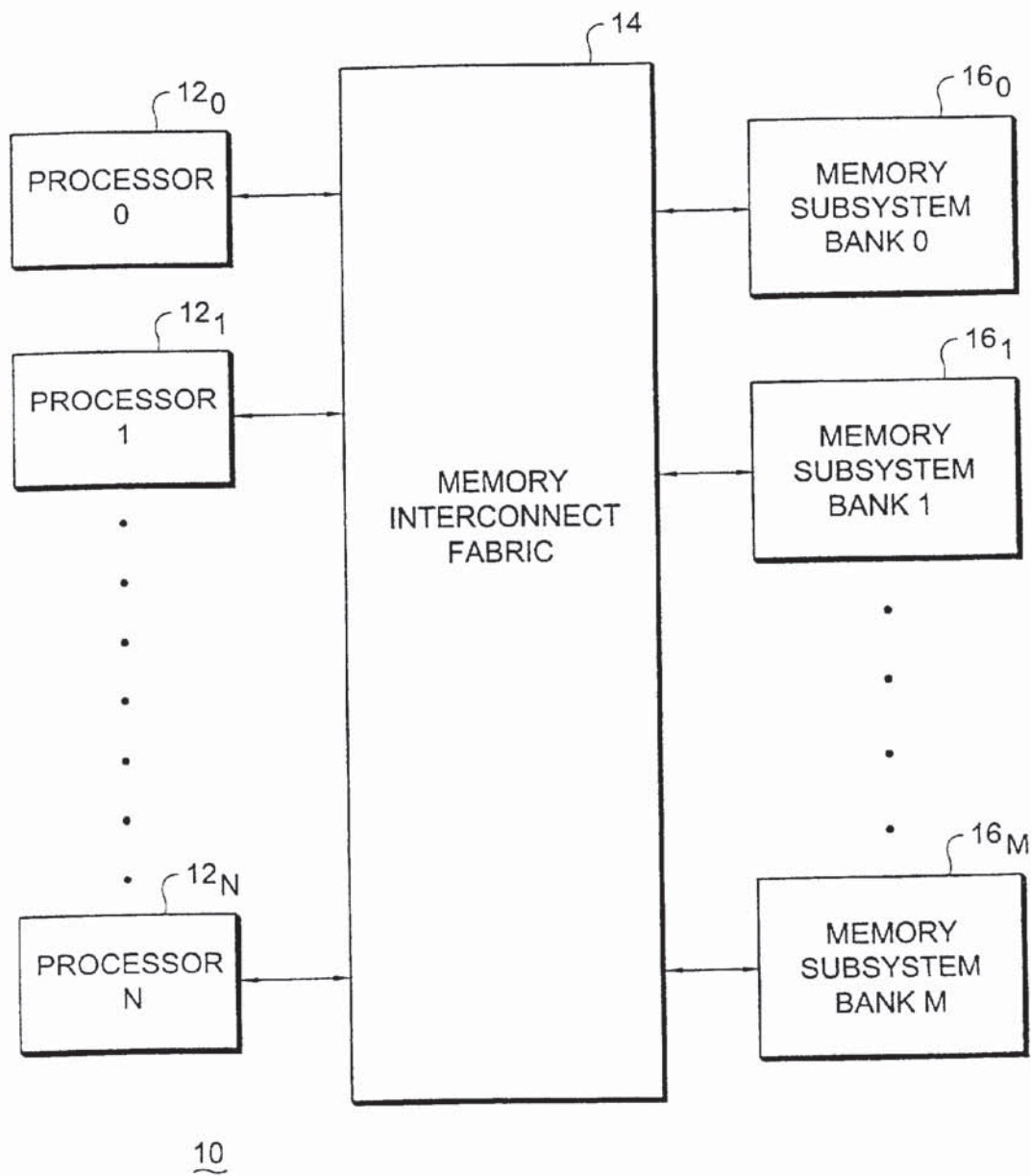


FIG. 1

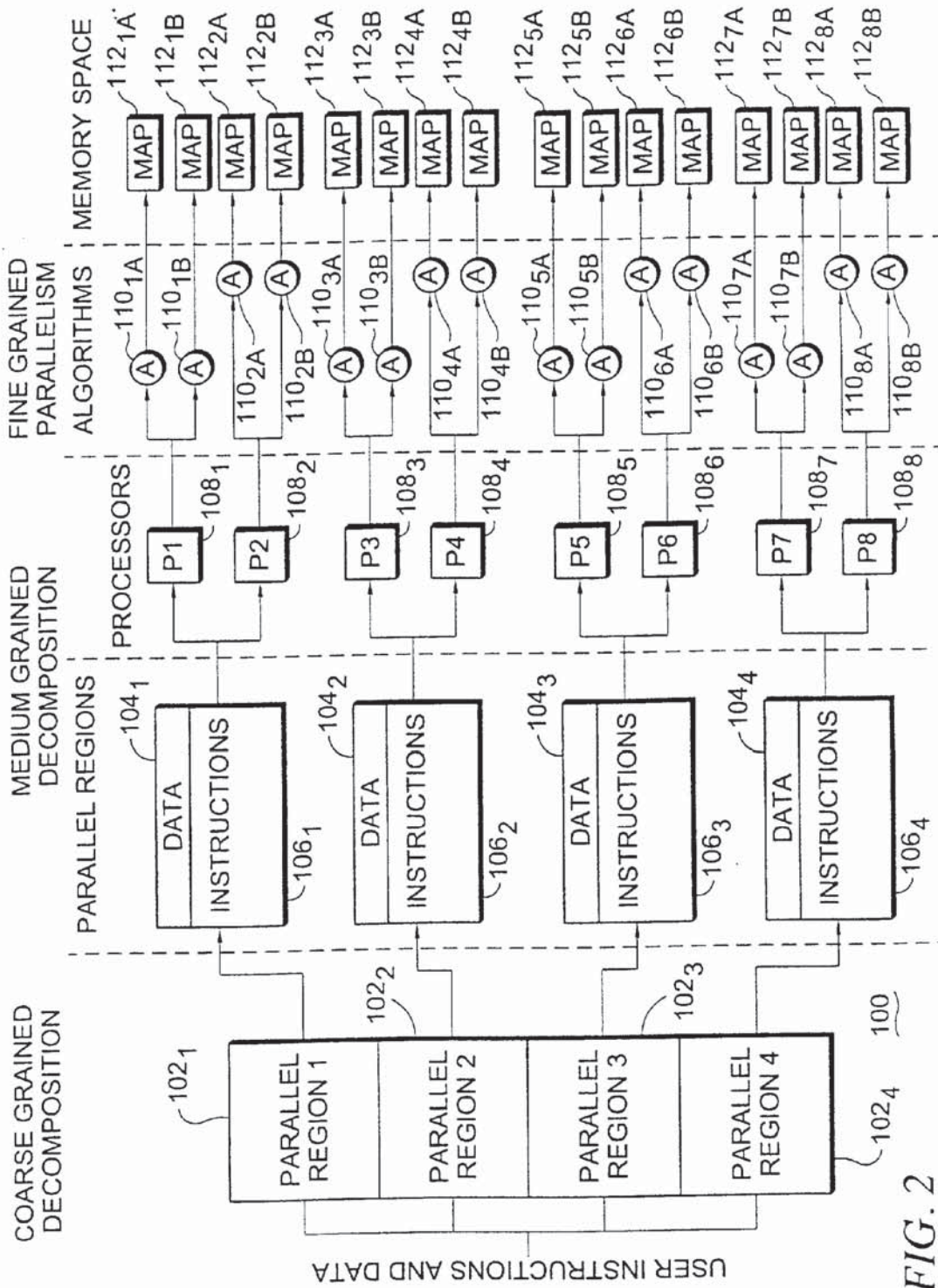
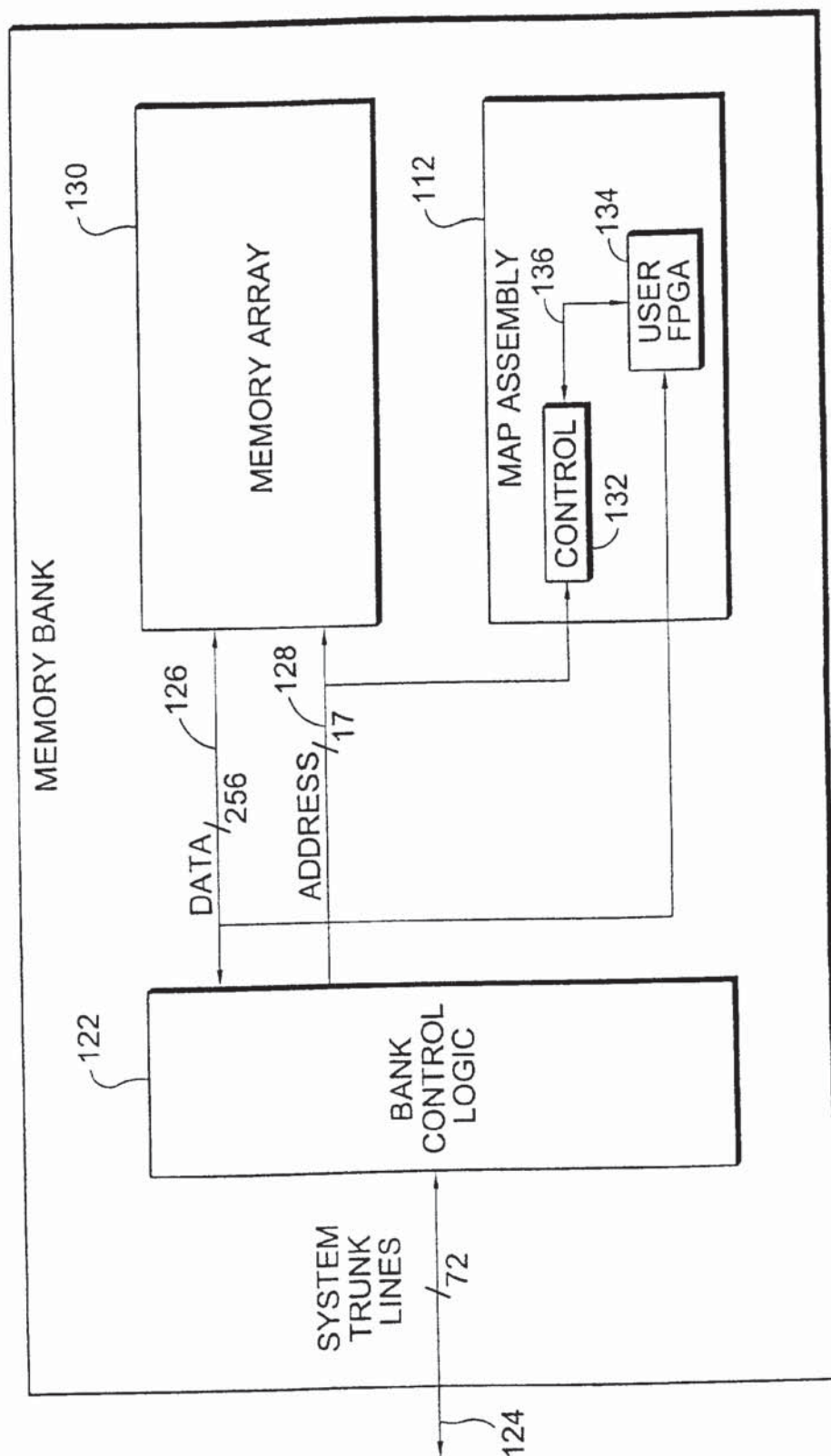


FIG. 2



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FIG. 3

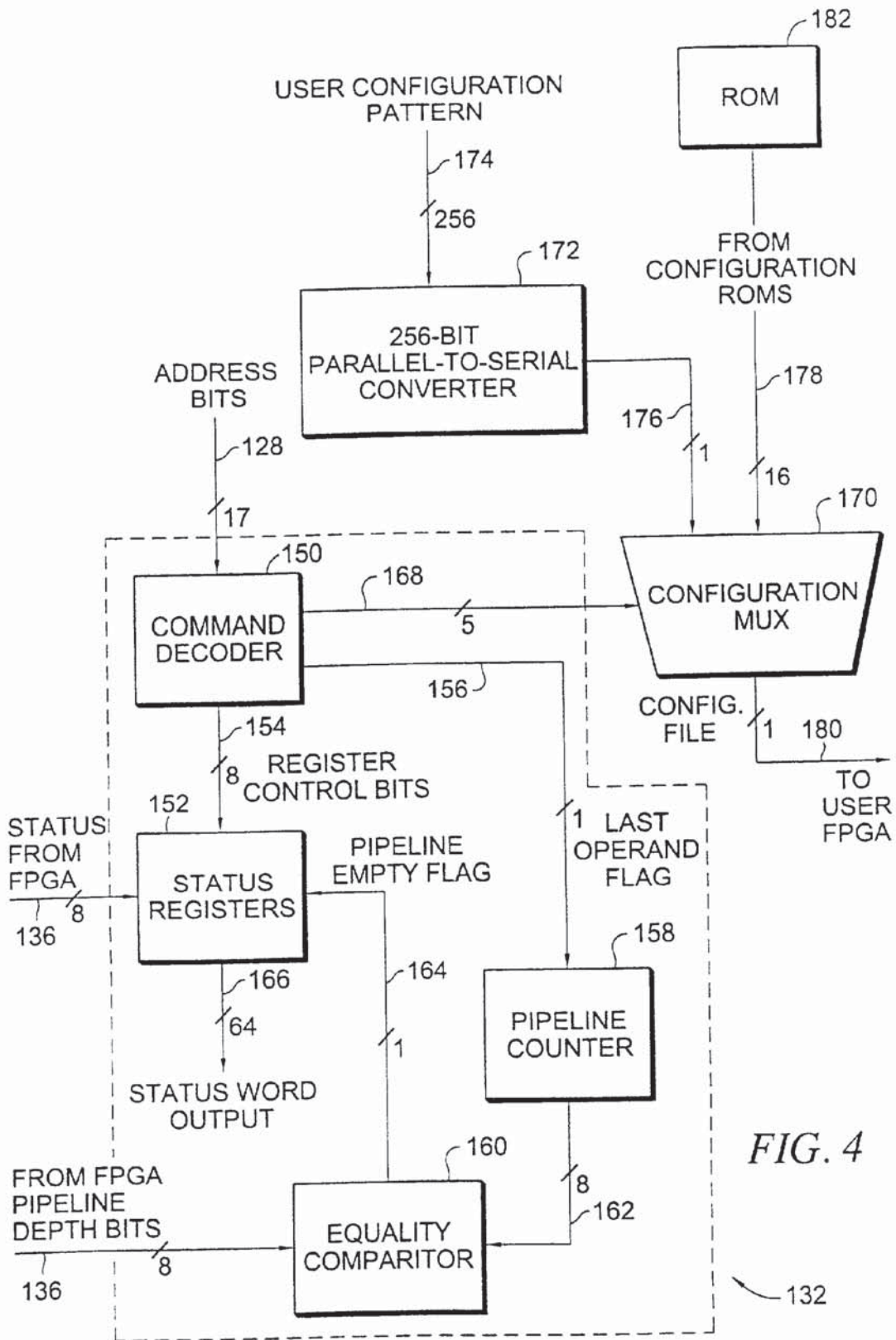


FIG. 4

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