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11002 U.S. PTO
10/285318

UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 CFR 1.53(b))</small>	Attorney Docket No.	SRC015
	First Inventor	Jon M. Huppenthal et al.
	Title	MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS
	Express Mail Label No.	EV035493558US

APPLICATION ELEMENTS	Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
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|---|---|
| <p>1. <input type="checkbox"/> Fee Transmittal Form
<small>(submit an original and a duplicate for fee processing)</small></p> <p>2. <input type="checkbox"/> Applicant claims small entity status.
See 37 CFR 1.27</p> <p>3. <input checked="" type="checkbox"/> Specification [total pages <u>34</u>]
<small>(preferred Arrangement set forth below)</small></p> <ul style="list-style-type: none"> - Descriptive title of the Invention - Cross References to Related Applications - Statement Regarding Fed sponsored R&D - Reference to sequence listing, a table, or a computer program listing appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings - Detailed Description - Claim(s) - Abstract of the Disclosure <p>4. <input checked="" type="checkbox"/> Drawing(s) [total sheets <u>20</u>]</p> <p>5. <input checked="" type="checkbox"/> Oath or Declaration [total pages <u>3</u>]</p> <p>a. <input checked="" type="checkbox"/> UNEXECUTED (original or copy)</p> <p>b. <input type="checkbox"/> Copy from prior appl. (37 C.F.R. § 1.63(d))
<small>(for continuation/divisional with Box 18 completed)</small></p> <p>i. <input type="checkbox"/> DELETION OF INVENTOR(S)
<small>Signed statement attached deleting inventor(s) named in prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).</small></p> | <p>6. <input type="checkbox"/> Application Data Sheet. (See 37 CFR 1.76)</p> <p>7. <input type="checkbox"/> CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)</p> <p>8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)</p> <p>a. <input type="checkbox"/> Computer Readable Form</p> <p>b. <input type="checkbox"/> Specification Sequence Listing on:</p> <p>i. <input type="checkbox"/> CD-ROM or CD-R (2 copies); or</p> <p>ii. <input type="checkbox"/> paper</p> <p>c. <input type="checkbox"/> Statements verifying identity of above copies</p> |
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ACCOMPANYING APPLICATION PARTS	
9. <input type="checkbox"/> Assignment Papers (coversheet/document(s))	
10. <input type="checkbox"/> 37 CFR. 3.73(b) Statement <input type="checkbox"/> Power of Attorney <small>(when there is an assignee)</small>	
11. <input type="checkbox"/> English Translation Document	
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13. <input type="checkbox"/> Preliminary Amendment	
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15. <input type="checkbox"/> Certified Copy of Priority Document(s)	
16. <input type="checkbox"/> Nonpublication Request Under 35 USC 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35	
17. <input checked="" type="checkbox"/> Other: Certificate of Mailing	

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:


Continuation Divisional Continuation-in-part (CIP) of prior application No.: /

Prior application information: Examiner: Group/Art Unit:

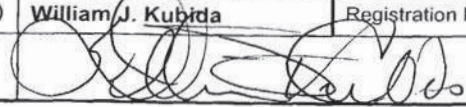
FOR CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

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(Signature)		Date	<u>31 October 2002</u>

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PATENT
EXPRESS MAIL NO. EV035493558US
Attorney Docket No. SRC015
Client/Matter No. 80404.0018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. NEW

Filed: Herewith

For: MULTI-ADAPTIVE PROCESSING
SYSTEMS AND TECHNIQUES FOR
ENHANCING PARALLELISM AND
PERFORMANCE OF
COMPUTATIONAL FUNCTIONS

CERTIFICATE OF MAILING BY EXPRESS MAIL

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Assistant Commissioner for Patents
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Sir:

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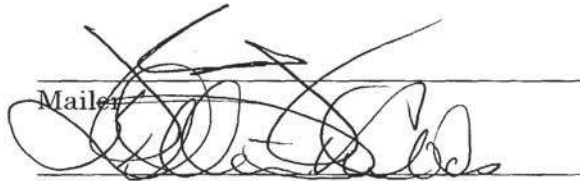
1. Utility Patent Application Transmittal;
2. Utility Patent Application;
3. Unexecuted Declaration for Utility Patent Application;
4. 20 sheets of drawings;
5. Return postcard; and
6. Certificate of Mailing By Express Mail

relating to the above application, were deposited as "Express Mail", Mailing Label No. EV035493558US, with the United States Postal Service, addressed to Box PATENT APPLICATION, The Assistant Commissioner for Patents, Washington, D.C., 20231,

31 October 2002.

31 October 2002
Date

31 October 2002
Date



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BACKGROUND OF THE INVENTION

The present invention relates, in general, to the field of computing systems and techniques. More particularly, the present invention relates to multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions.

Currently, most large software applications achieve high performance operation through the use of parallel processing. This technique allows multiple processors to work simultaneously on the same problem to achieve a solution in a fraction of the time required for a single processor to accomplish the same result. The processors in use may be performing many copies of the same operation, or may be performing totally different operations, but in either case all processors are working simultaneously.

The use of such parallel processing has led to the proliferation of both multi-processor boards and large scale clustered systems. However, as more and more performance is required, so is more parallelism, resulting in ever larger systems. Clusters exist today that have tens of thousands of processors and can occupy football fields of space. Systems of such a large physical size present many obvious downsides, including, among other factors, facility requirements, power, heat generation and reliability.

SUMMARY OF THE INVENTION

However, if a processor technology could be employed that offers orders of magnitude more parallelism per processor, these systems could be reduced in size by a comparable factor. Such a processor or processing element is possible through

the use of a reconfigurable processor. Reconfigurable processors instantiate only the functional units needed to solve a particular application, and as a result, have available space to instantiate as many
5 functional units as may be required to solve the problem up to the total capacity of the integrated circuit chips they employ.

At present, reconfigurable processors, such as multi-adaptive processor elements (MAPTM, a trademark
10 of SRC Computers, Inc.) can achieve two to three orders of magnitude more parallelism and performance than state-of-the-art microprocessors. Through the advantageous application of adaptive processing techniques as disclosed herein, this type of
15 reconfigurable processing parallelism may be employed in a variety of applications resulting in significantly higher performance than that which can now be achieved while using significantly smaller and less expensive computer systems.

20 However, in addition to these benefits, there is an additional much less obvious one that can have even greater impact on certain applications and has only become available with the advent of multi-million gate reconfigurable chips. Performance gains are also
25 realized by reconfigurable processors due to the much tighter coupling of the parallel functional units within each chip than can be accomplished in a microprocessor based computing system.

In a multi-processor, microprocessor-based
30 system, each processor is allocated but a relatively small portion of the total problem called a cell. However, to solve the total problem, results of one processor are often required by many adjacent cells because their cells interact at the boundary and

Further disclosed herein is a method for data processing in a reconfigurable computing system comprising a plurality of functional units. The method comprises: defining a first systolic wall comprising 5 rows of cells forming a subset of the plurality of functional units; computing a value at each of the cells in at least a first row of the first systolic wall; communicating the values between cells in the first row of the cells to produce updated values; 10 communicating the updated values to a second row of the first systolic wall; and substantially concurrently providing the updated values to a first row of a second systolic wall of rows of cells in the subset of the plurality of functional units.

Also disclosed herein is a method for data 15 processing in a reconfigurable processing system which includes setting up a systolic processing form employing a speculative processing strategy.

BRIEF DESCRIPTION OF THE DRAWINGS

20 The aforementioned and other features and objects of the present invention and the manner of attaining them will become more apparent and the invention itself will be best understood by reference to the following description of a preferred embodiment taken 25 in conjunction with the accompanying drawings, wherein:

Fig. 1 is a simplified functional block diagram of typical clustered inter-processor communications path in a conventional multi-processor computing 30 system;

Fig. 2 is a functional block diagram of an adaptive processor communications path illustrating the many functional units ("FU") interconnected by

reconfigurable routing resources within the adaptive processor chip;

Fig. 3A is a graph of the actual performance improvement versus the number of processors utilized and illustrating the deviation from perfect
5 scalability of a particular application utilizing a conventional multi-processor computing system such as that illustrated in Fig. 1;

Fig. 3B is a corresponding graph of the actual
10 performance improvement versus the number of processors utilized and illustrating the performance improvement over a conventional multi-processor computing system utilizing an adaptive processor-based computing system such as that illustrated in Fig. 2;

Fig. 4A is a simplified logic flowchart
15 illustrating a conventional sequential processing operation in which nested Loops A and B are alternately active on different phases of the process;

Fig. 4B is a comparative, simplified logic
20 flowchart illustrating multi-dimensional processing in accordance with the technique of the present invention wherein multiple dimensions of data are processed by both Loops A and B such that the computing system logic is operative on every clock cycle;

Fig. 5A is illustrative of a general process for
25 performing a representative multi-dimensional pipeline operation in the form of a seismic migration imaging function utilizing the parallelism available in the utilization of the adaptive processing techniques of the present invention;

Fig. 5B is a follow-on illustration of the
30 computation phases employed in implementing the exemplary seismic migration imaging function of the preceding figure;

which nested Loops A (first loop 402) and B (second loop 404) are alternately active on different phases of the process.

As shown, the standard implementation of applications that have a set of nested loops 402,404 is to complete the processing of the first loop 402 before proceeding to the second loop 404. The problem inherent in this approach, particularly when utilized in conjunction with field programmable gate arrays ("FPGAs") is that all of the logic that has been instantiated is not being completely utilized.

With reference additionally now to Fig. 4B, a comparative, simplified logic flowchart is shown illustrating a multi-dimensional process 410 in accordance with the technique of the present invention. The multi-dimensional process 410 is effectuated such that multiple dimensions of data are processed by both Loops A (first loop 412) and B (second loop 414) such that the computing system logic is operative on every clock cycle.

In contrast to the sequential processing operation 400 (Fig. 4A) the solution to the problem of most effectively utilizing available resources is to have an application evaluate a problem in a data flow sense. That is, it will "pass" a subsequent dimension of a given problem through the first loop 412 of logic concurrently with the previous dimension of data being processed through the second loop 414. In practice, a "dimension" of data can be: multiple vectors of a problem, multiple planes of a problem, multiple time steps in a problem and so forth.

With reference additionally now to Fig. 5A, a general process for performing a representative multi-dimensional pipeline operation is shown in the form of

step 614. At step 616 values are computed for $S(Z_{nz}), R(Z_{nz})$ which step is followed by the phases MAPTRI_x 520 and MAPTRI_y 522. At step 618, the image of $Z_{1/2}$ is computed. This is followed by the phases
5 MAPTRI_d+ 524 and MAPTRI_d- 526 to produce the resultant image Z at step 620. The process 610 loops over the depth slices as indicated by reference number 622 and loops over the shots as indicated by reference number 624.

10 With reference additionally now to Fig. 6C, the first step in a computational process 650 in accordance with the technique of the present invention is shown in which a first shot (S1) is started. The process 650 may be employed by an adaptive processor
15 (e.g. a MAPTM adaptive processor) as disclosed herein in the execution of the seismic imaging application 600 of Fig. 6A. As indicated by the shaded block, the phase MAPTRI_x 520 is active.

20 With reference additionally now to Fig. 6D, the second step in the computational process 650 is shown at a point at which a second shot (S2) is started. Again, as indicated by the shaded blocks, the phase MAPTRI_x 520 is active for S2, the phase MAPTRI_y 522 is active for S1 and image $Z_{1/2}$ has been produced at
25 step 618. As shown, adaptive processors in accordance with the disclosure of the present invention support computation pipelining in multiple dimensions and the parallelism in Z and shots is shown at step 612.

30 With reference additionally now to Fig. 6E, the third step in the computational process 650 is shown in which the operation on the first and second shots is continued through compute. As indicated by the shaded blocks, the phase MAPTRI_d+ 524 is active for

information computed for each cell is then passed to neighboring cells. These programs will particularly benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

5 Weather prediction: Such an application will partition the forecast area into logical grid cells. The computational algorithms will then perform calculations that have polynomials that have nodes associated with the grid cells. These programs are
10 ideal candidates to take advantage of adaptive or parallel computing because there are repeated operations on each cell associated with the set of times computed in the forecast.

15 Automotive: These applications investigate the aerodynamics of automobile or other aerodynamic structures. The application generally divides the space surrounding the automobile structure into logical cells that are associated with nodes in computational polynomials. These programs are ideal
20 candidates to take advantage of adaptive or parallel computing because there are repeated operations on each cell associated with the set of wind velocities computed in the forecast. These programs will benefit from the tight parallelism that can be found in
25 adaptive or reconfigurable processors.

30 Aerospace: These applications investigate the aerodynamics of aerospace/airplane structures. The application divides the space surrounding the aerospace/airplane structure into logical cells that are associated with nodes in computational polynomials. These programs are ideal candidates to take advantage of parallel computing because there are repeated operations on each cell associated with the set of wind velocities computed in the forecast.

These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

5 Plastic Injection Molding: These applications investigate the molding parameters of injecting liquid plastic into molds. The application divides the space inside the mold into logical cells that are also associated with nodes in computational polynomials. These programs are ideal candidates to take advantage
10 of parallel computing because there are repeated operations on each cell associated with the set of injection parameters. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

15 **Structures**

Crash Analysis: These applications are typically used in the automotive or aviation industry. The application will partition the entire automobile into components. These components are then subdivided into
20 cells. The application will analyze the effect of a collision on the structure of the automobile. These programs are ideal candidates for parallel computing because there are repeated operations on each cell and they receive computed information from their
25 neighboring cells. These programs will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Structural Analysis: These applications investigate the properties of structural integrity.
30 The application divides the structure into logical cells that are associated with nodes in computational polynomials. These programs are ideal candidates to take advantage of parallel computing because there are repeated operations on each cell associated with load

Finance

Financial modeling: The application creates numerous strategies for each decision step in the modeling process. The results of a computational step
5 are feed into another set of strategies for
subsequence modeling steps. These programs are ideal candidates to take advantage of parallel computing because there are repeated operations on each strategy within a modeling step. These programs will benefit
10 from the tight parallelism that can be found in
adaptive or reconfigurable processors.

Information Security

Encryption/Decryption: The application applies an algorithm that converts the original data into an
15 encrypted, or "protected", form. The process is
applied to each set of N bits in the original data. Decryption reverses the process to deliver the original data. These programs are ideal candidates for parallel computing because there are repeated
20 operations on each N bits of data. These programs
will benefit from the tight parallelism that can be found in adaptive or reconfigurable processors.

Chemistry/Biology

Genetic pattern matching: These applications are
25 typically used in the bioinformatics industry. The
application looks for matches of a particular genetic sequence (or model) to a database of genetic records. The application compares each character in the model to the characters in genetic record. These programs
30 are ideal candidates for parallel computing because of
the repeated comparison operations that exist for all character comparisons of the model with each character in the genetic record. These programs will benefit

CLAIMS:

1. A method for data processing in a reconfigurable computing system comprising a plurality of functional units, said method comprising:
 - 5 defining a calculation for said reconfigurable computing system;
 - instantiating at least two of said functional units to perform said calculation;
 - utilizing a first of said functional units to
 - 10 operate upon a subsequent data dimension of said calculation; and
 - substantially concurrently utilizing a second of said functional units to operate upon a previous data dimension of said calculation.
- 15 2. The method of claim 1 wherein said subsequent and previous data dimensions of said calculation comprise multiple vectors in said calculation.
3. The method of claim 1 wherein said subsequent and previous data dimensions of said calculation comprise
- 20 multiple planes in said calculation.
4. The method of claim 1 wherein said subsequent and previous data dimensions of said calculation comprise multiple time steps in said calculation.
5. The method of claim 1 wherein said subsequent and
- 25 previous data dimensions of said calculation comprise multiple grid points in said calculation.
6. The method of claim 1 wherein said calculation comprises a seismic imaging calculation.

ABSTRACT OF THE DISCLOSURE

Multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions are disclosed which can be employed in a myriad of applications including multi-dimensional pipeline computations for seismic applications, search algorithms, information security, chemical and biological applications, filtering and the like as well as for systolic wavefront computations for fluid flow and structures analysis, bioinformatics etc. Some applications may also employ both the multi-dimensional pipeline and systolic wavefront methodologies disclosed.

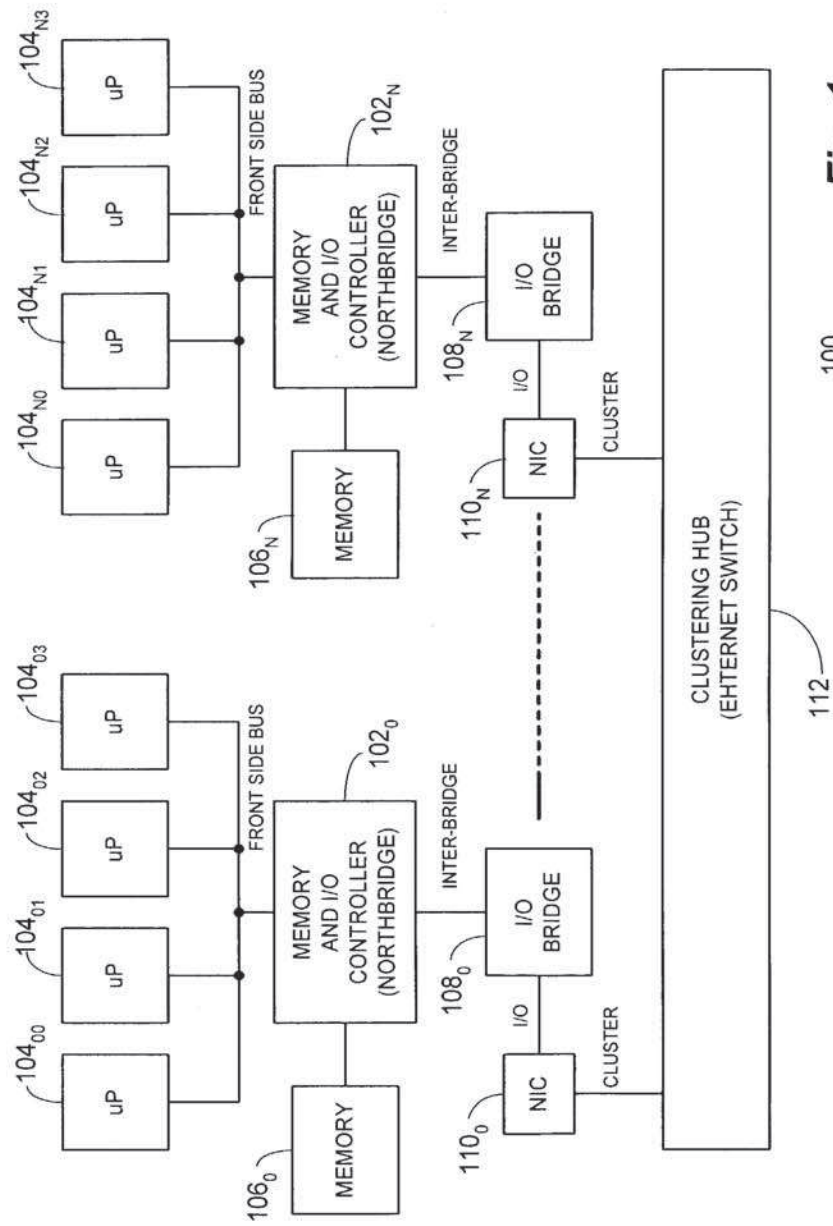
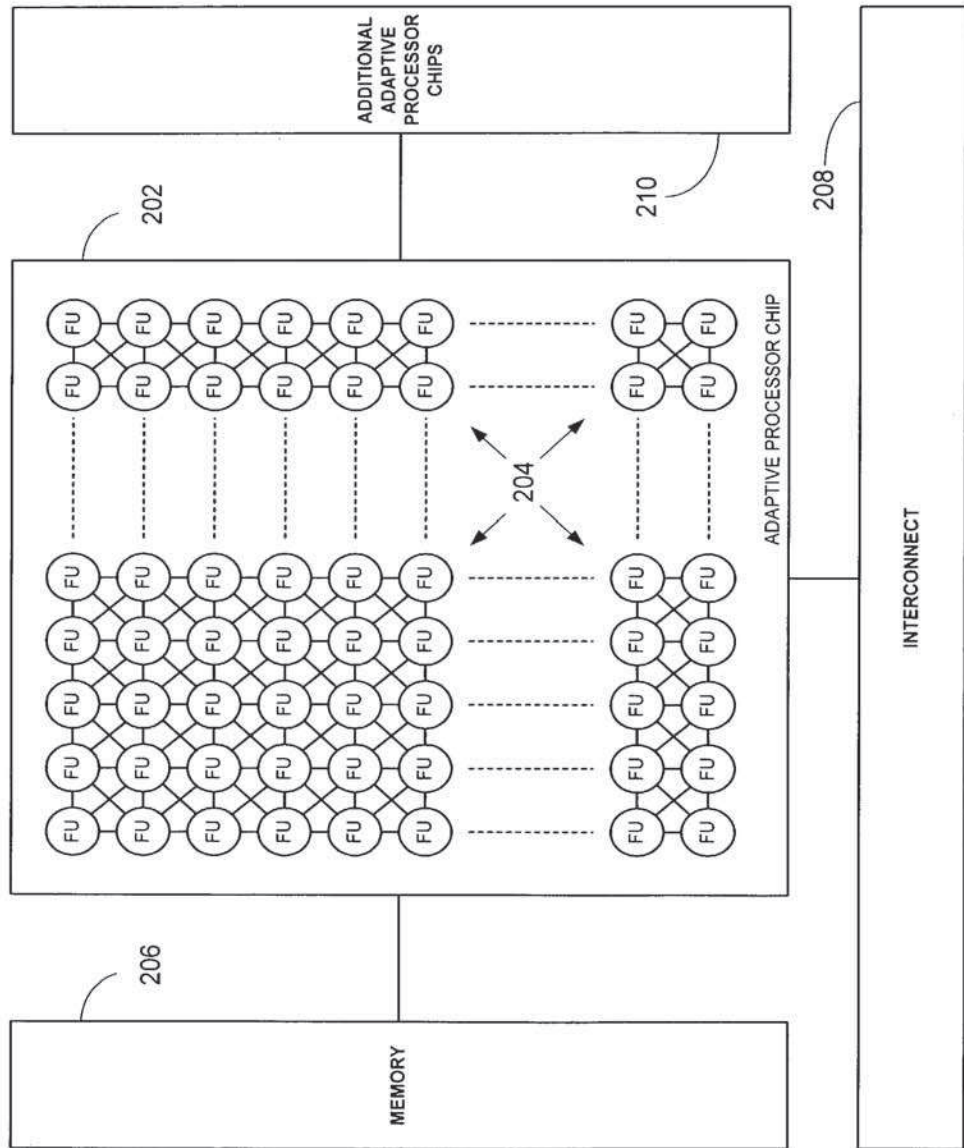


Fig. 1
Prior Art



200 Fig. 2

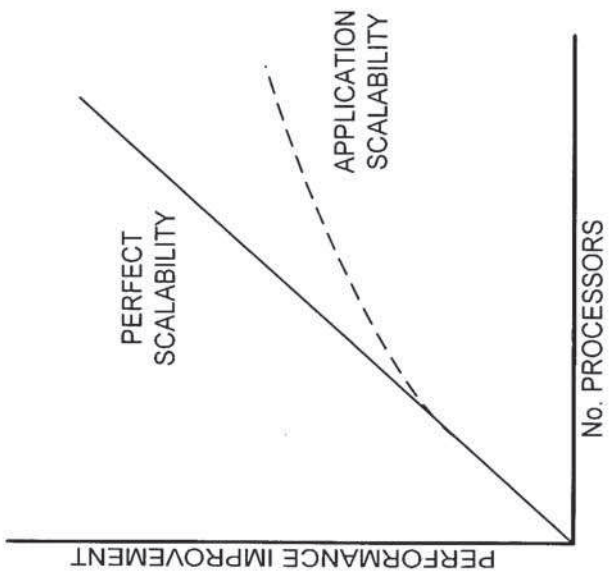


Fig. 3A
PRIOR ART

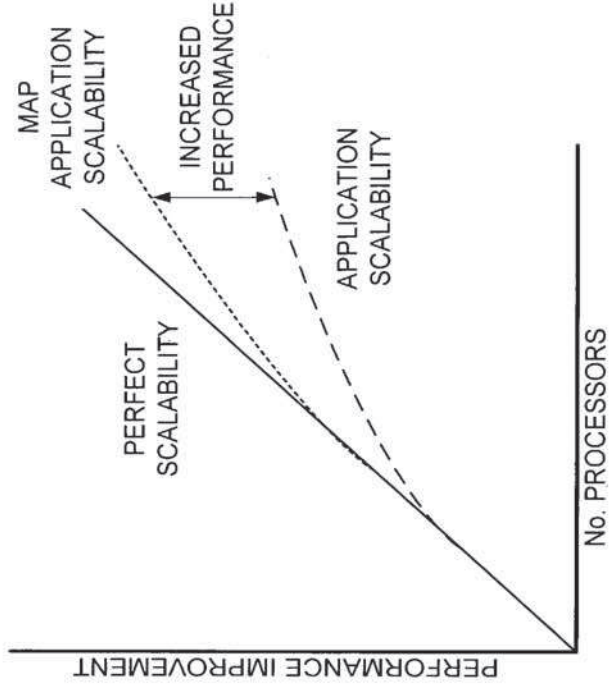
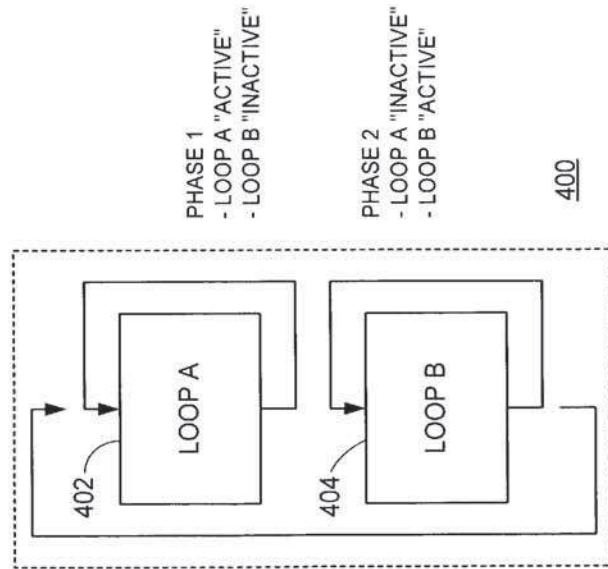


Fig. 3B

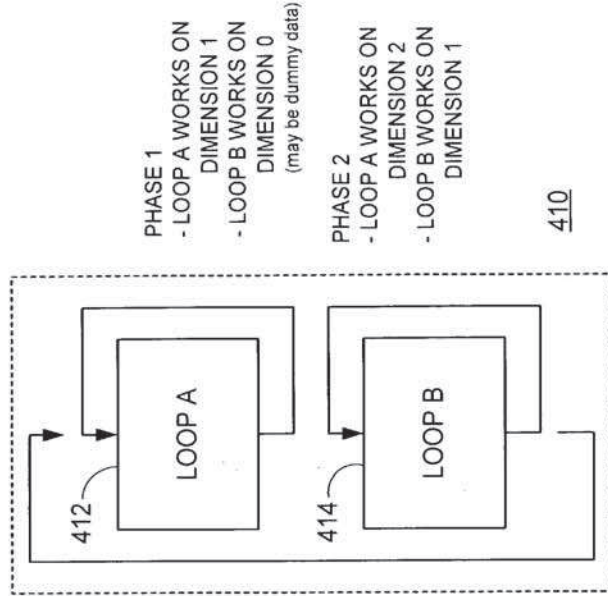


PHASE 1
 - LOOP A "ACTIVE"
 - LOOP B "INACTIVE"

PHASE 2
 - LOOP A "INACTIVE"
 - LOOP B "ACTIVE"

400

Fig. 4A
 Prior Art



PHASE 1
 - LOOP A WORKS ON
 DIMENSION 1
 - LOOP B WORKS ON
 DIMENSION 0
 (may be dummy data)

PHASE 2
 - LOOP A WORKS ON
 DIMENSION 2
 - LOOP B WORKS ON
 DIMENSION 1

410

Fig. 4B

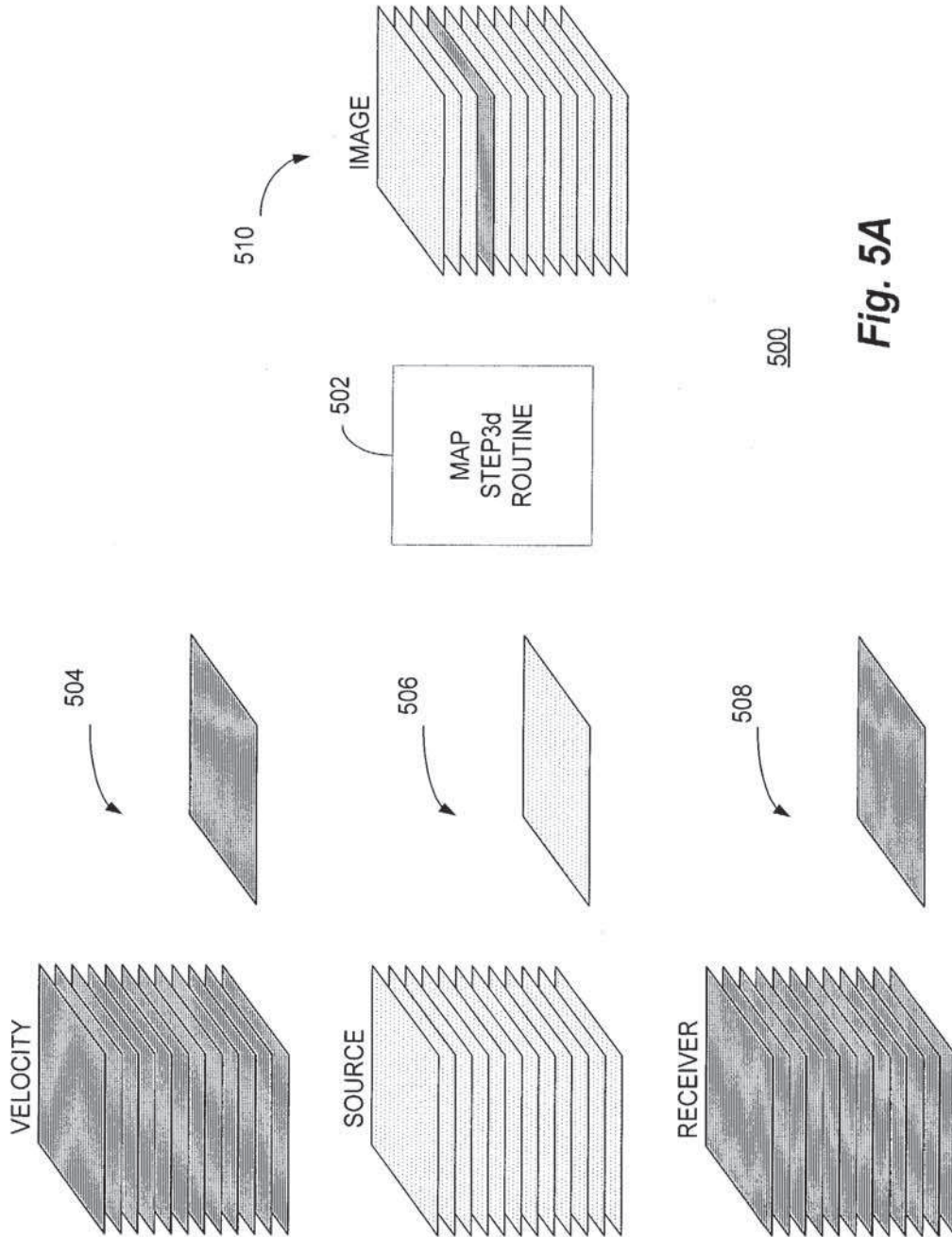
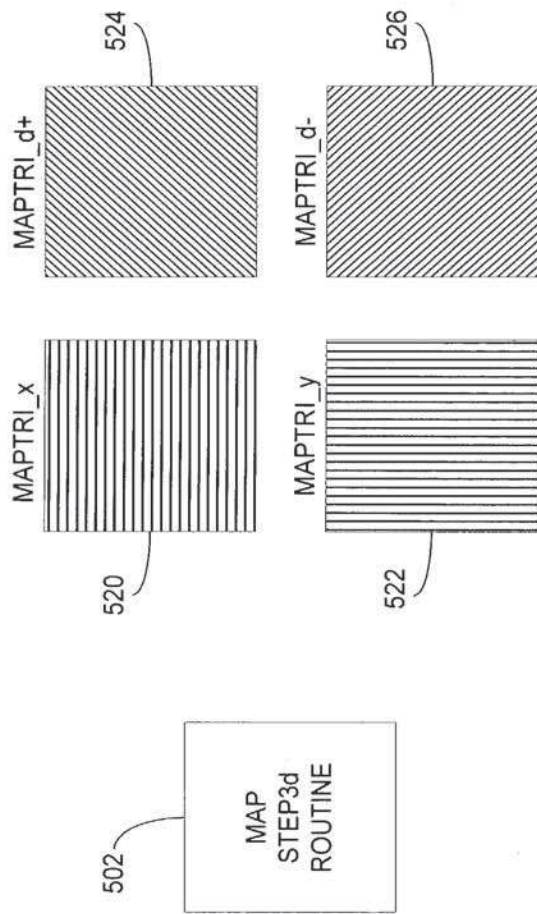


Fig. 5A



COMPUTATION PHASES

Fig. 5B

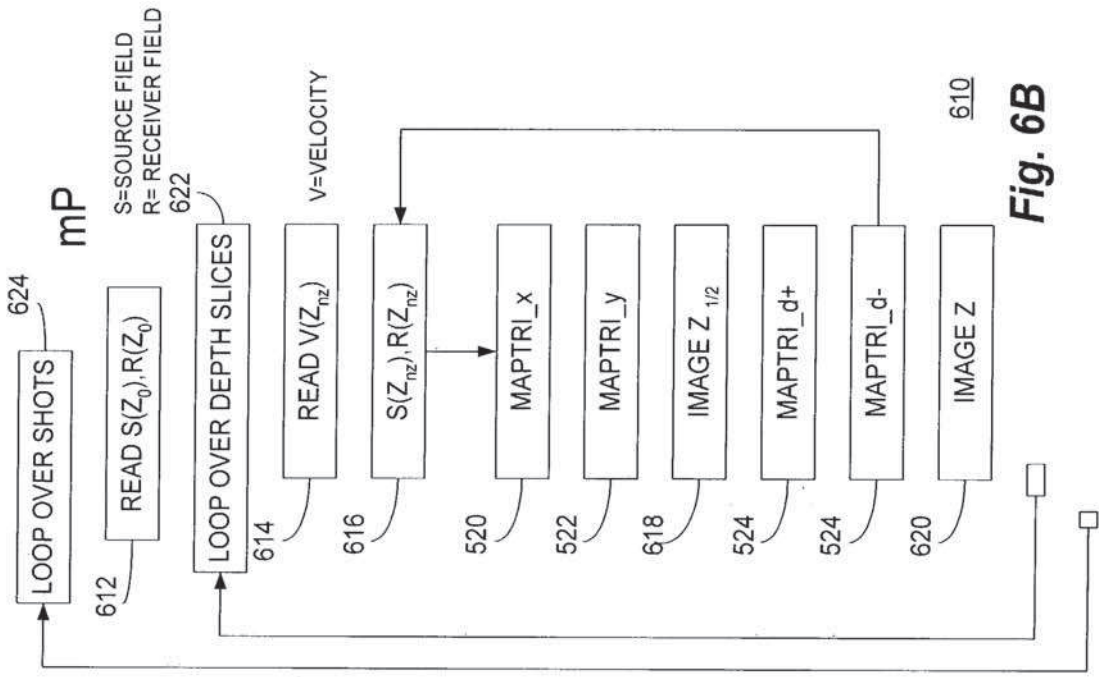
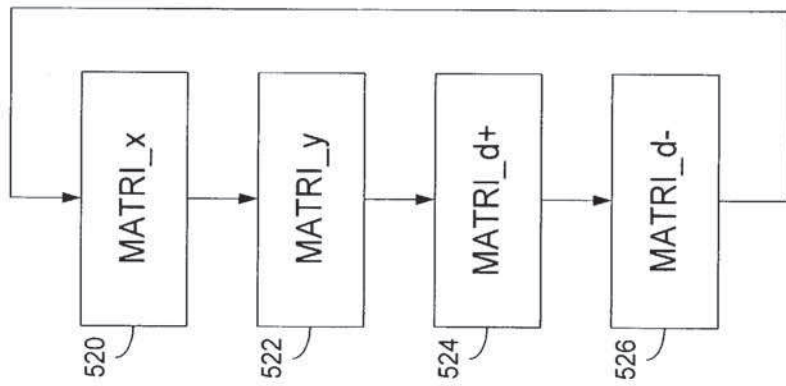


Fig. 6B



600

Fig. 6A

MAP STEP 1
START SHOT 1 (S1)

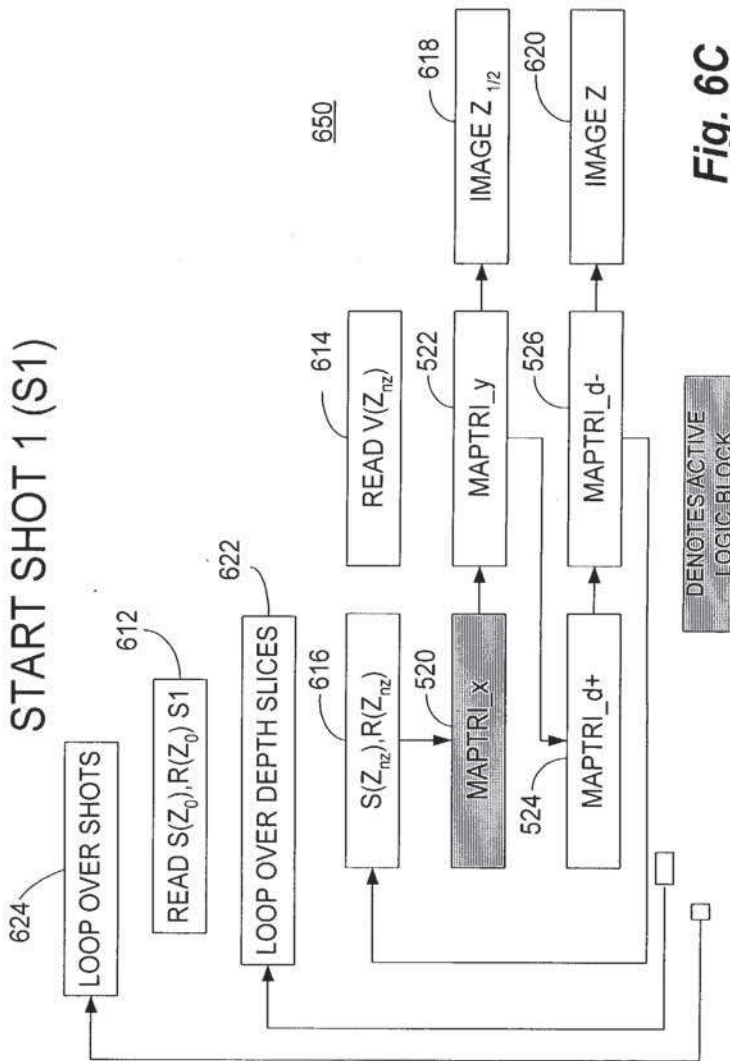


Fig. 6C

MAP STEP 2
START SHOT 2 (S2)

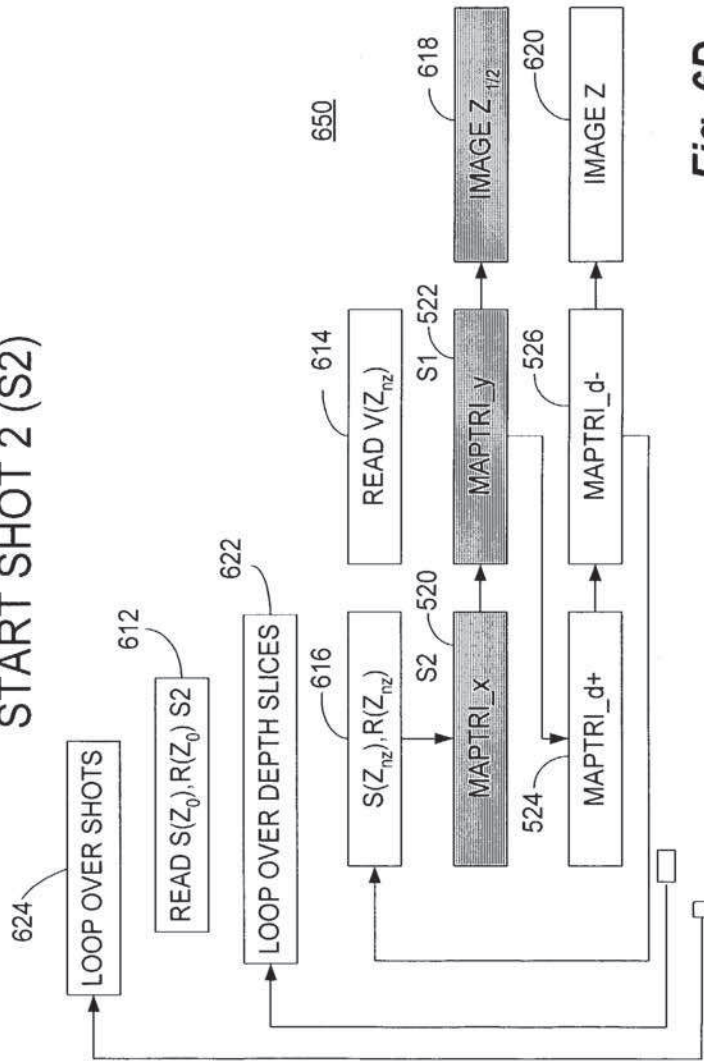


Fig. 6D

CONTINUE S1 AND S2 THROUGH COMPUTE

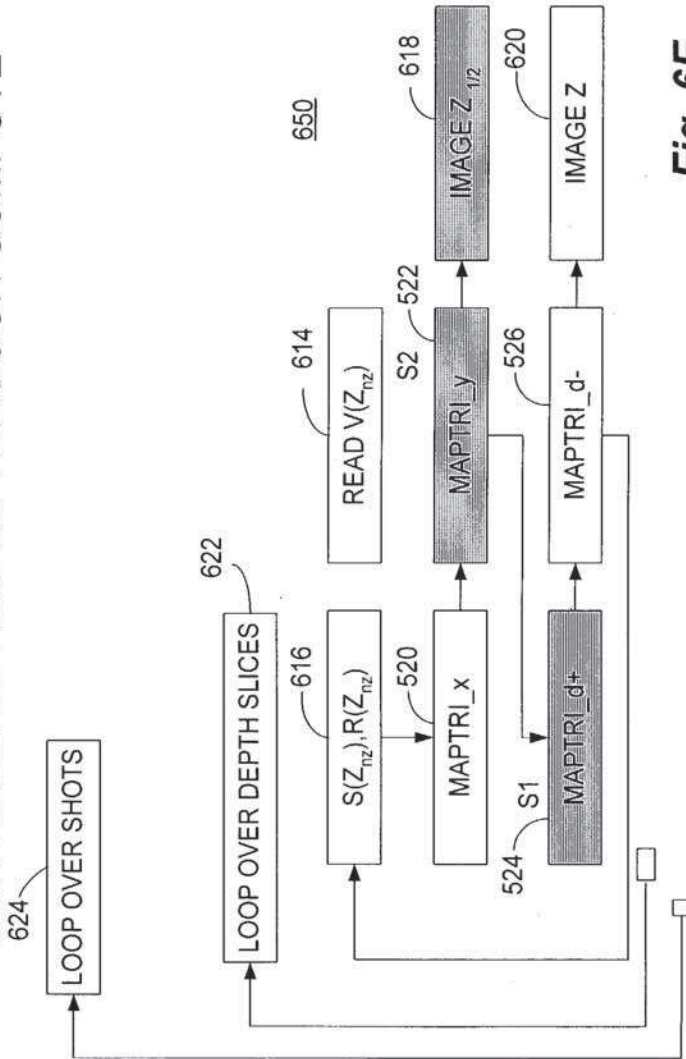


Fig. 6E

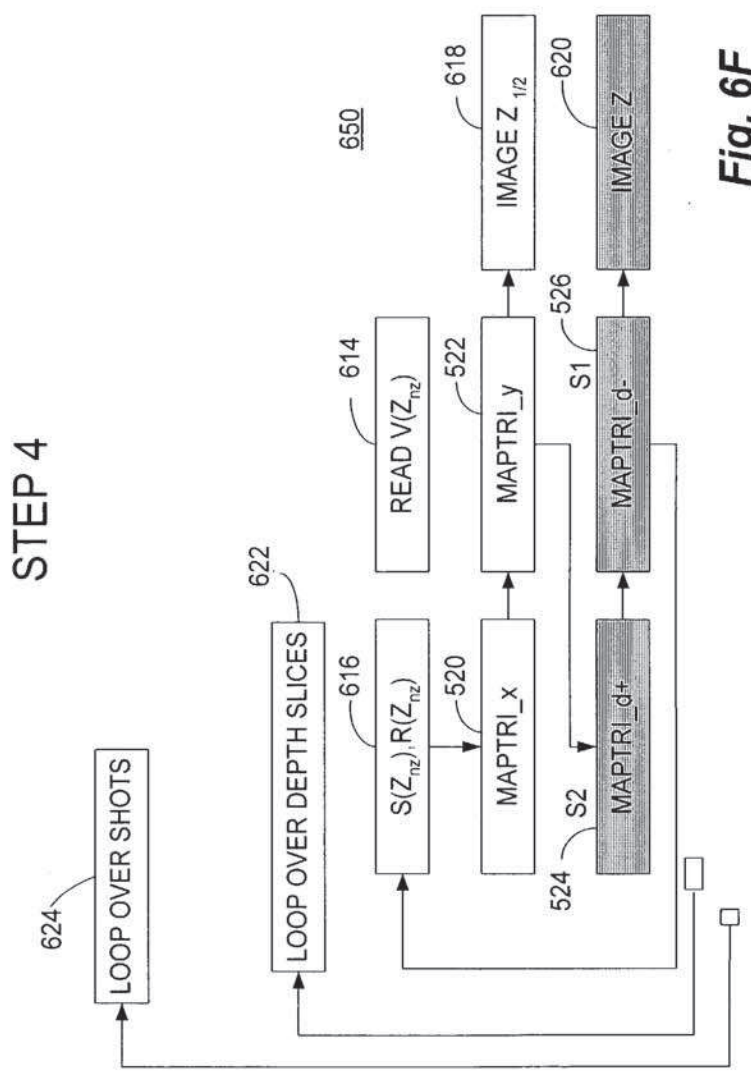


Fig. 6F

STEP 5

CONTINUE THE DOWNWARD PROPGATION OF S1 AND S2 OVER ALL OF THE DEPTH SLICES

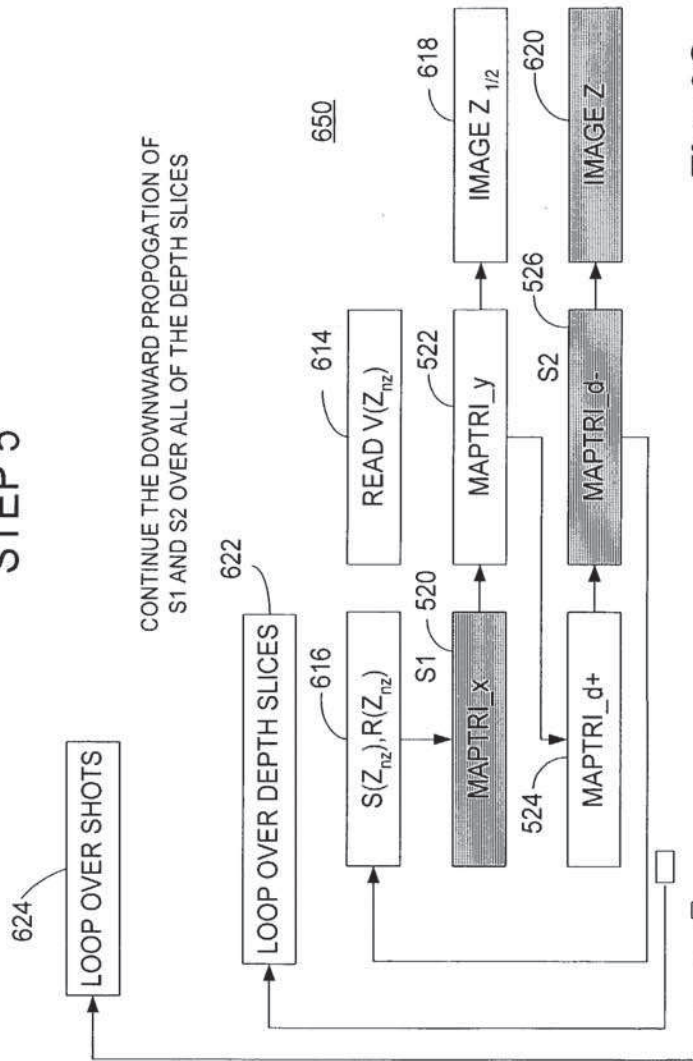


Fig. 6G

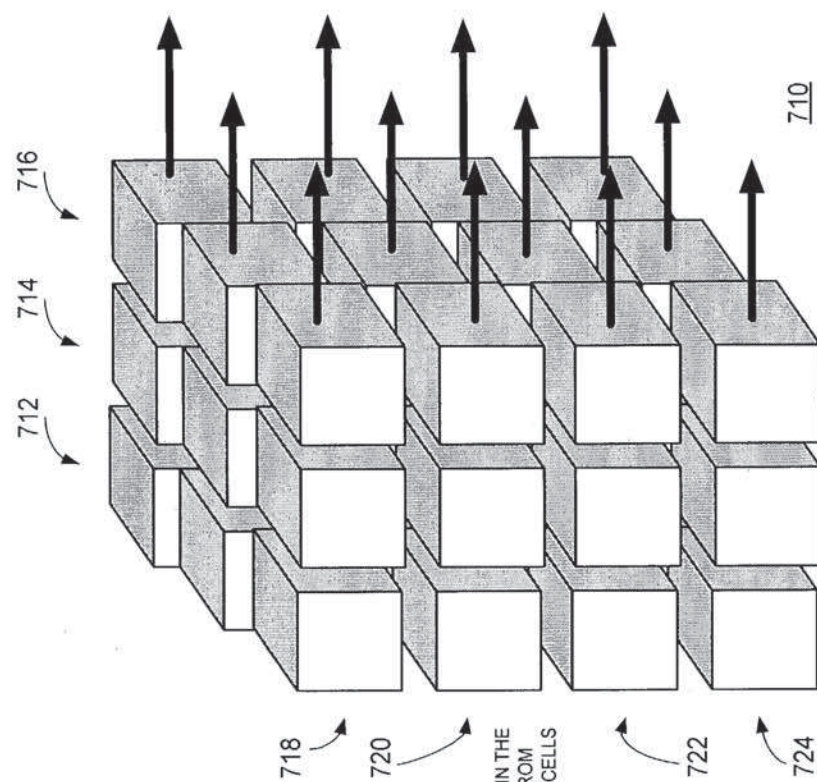


Fig. 7B

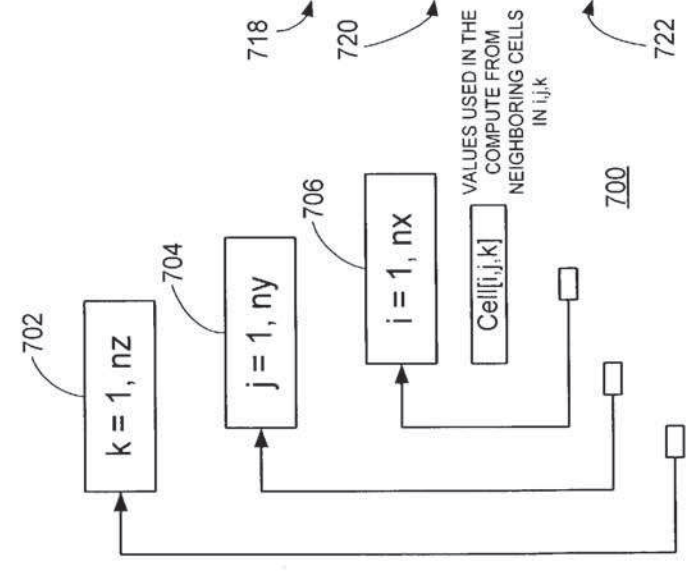
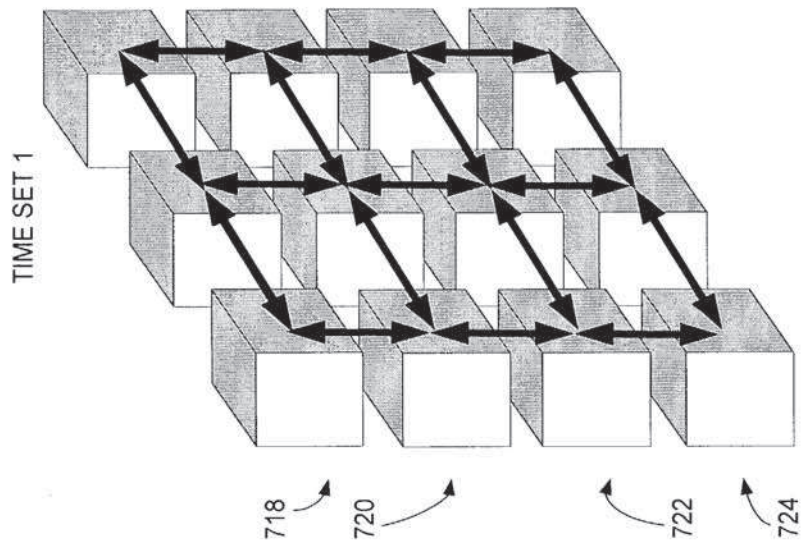


Fig. 7A



712

Fig.7C

FILED 08/21/2019

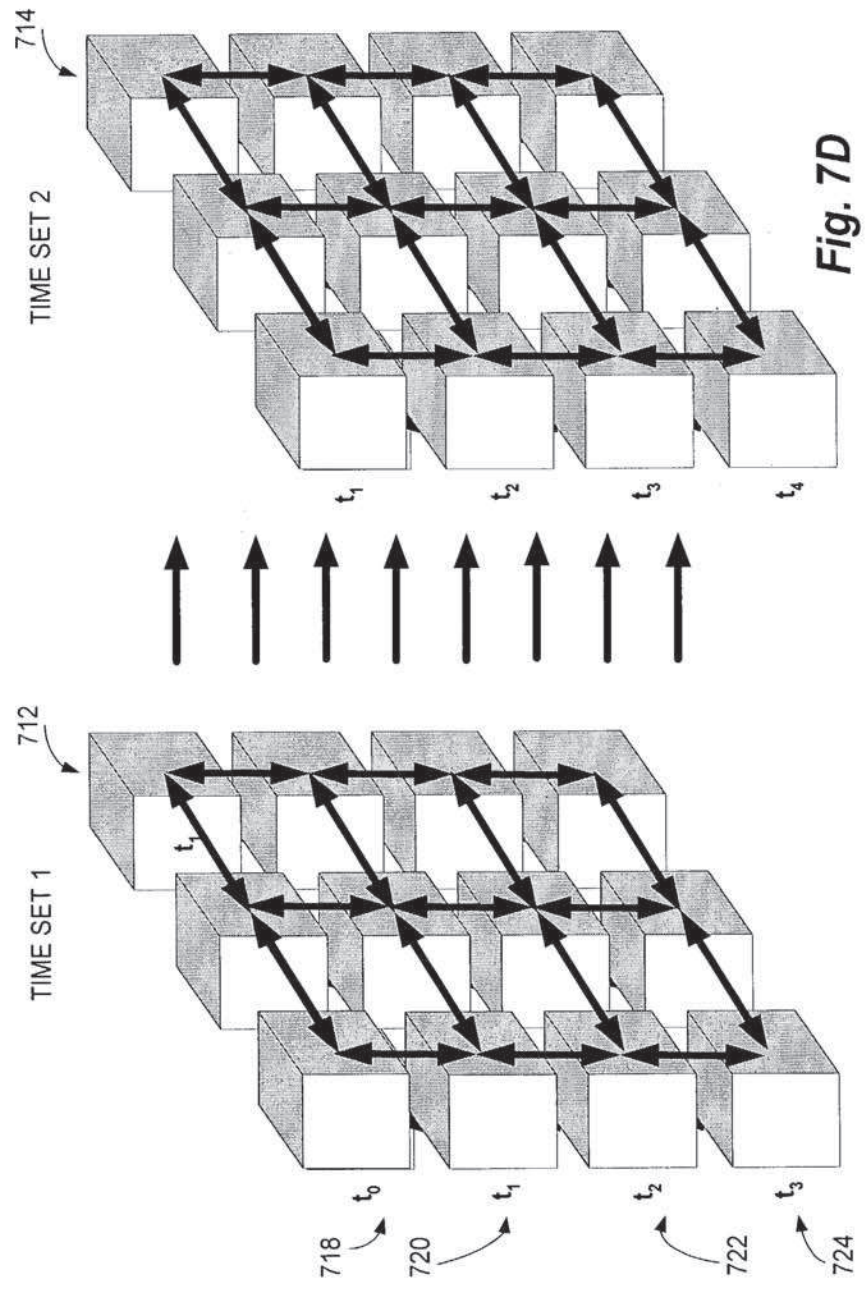


Fig. 7D

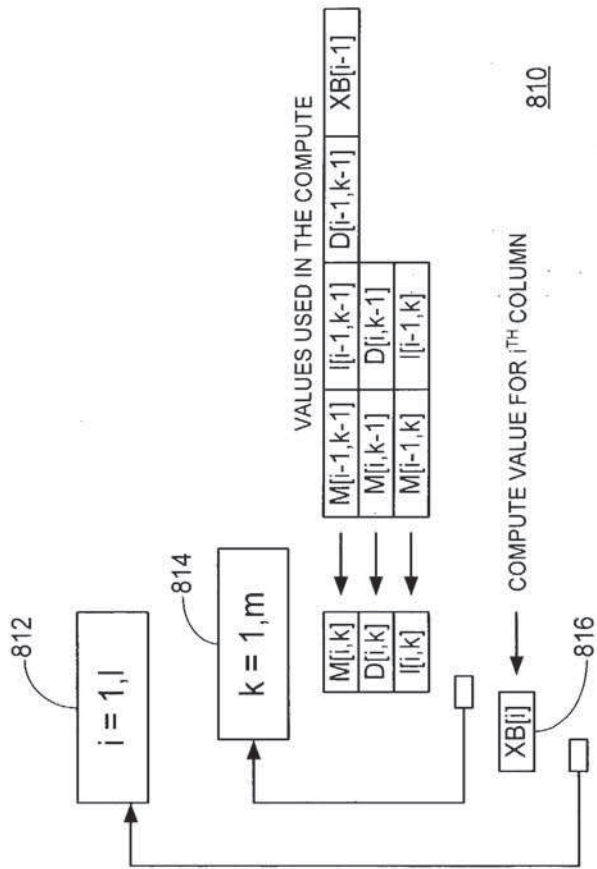
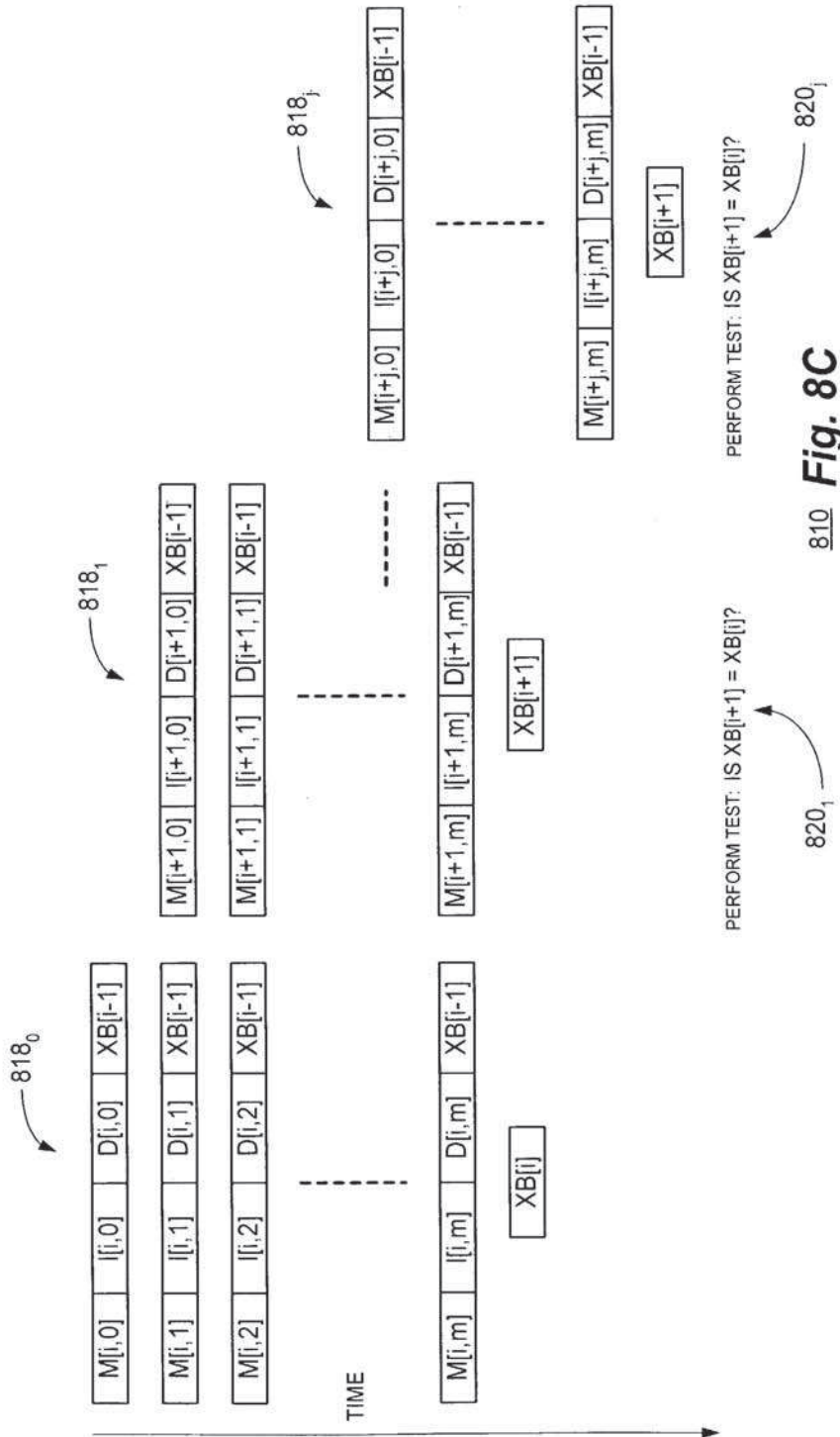


Fig. 8B



810 Fig. 8C

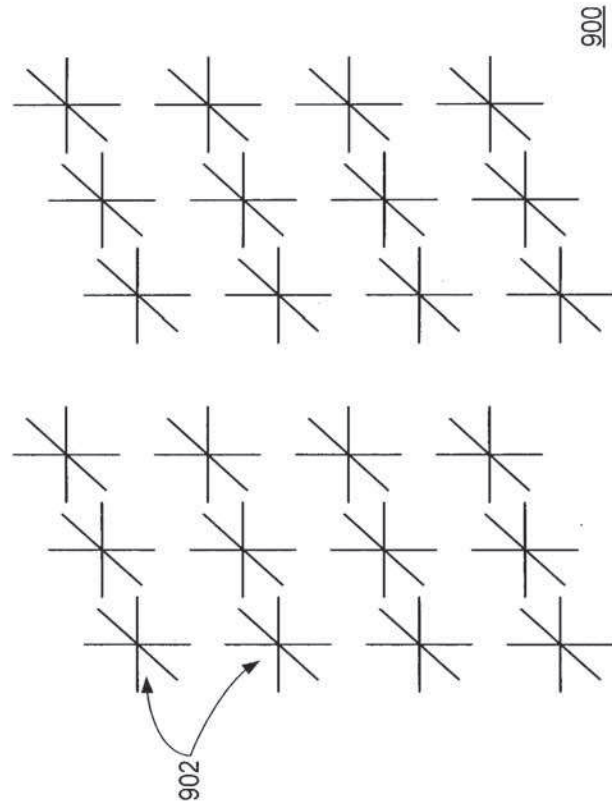


Fig. 9A

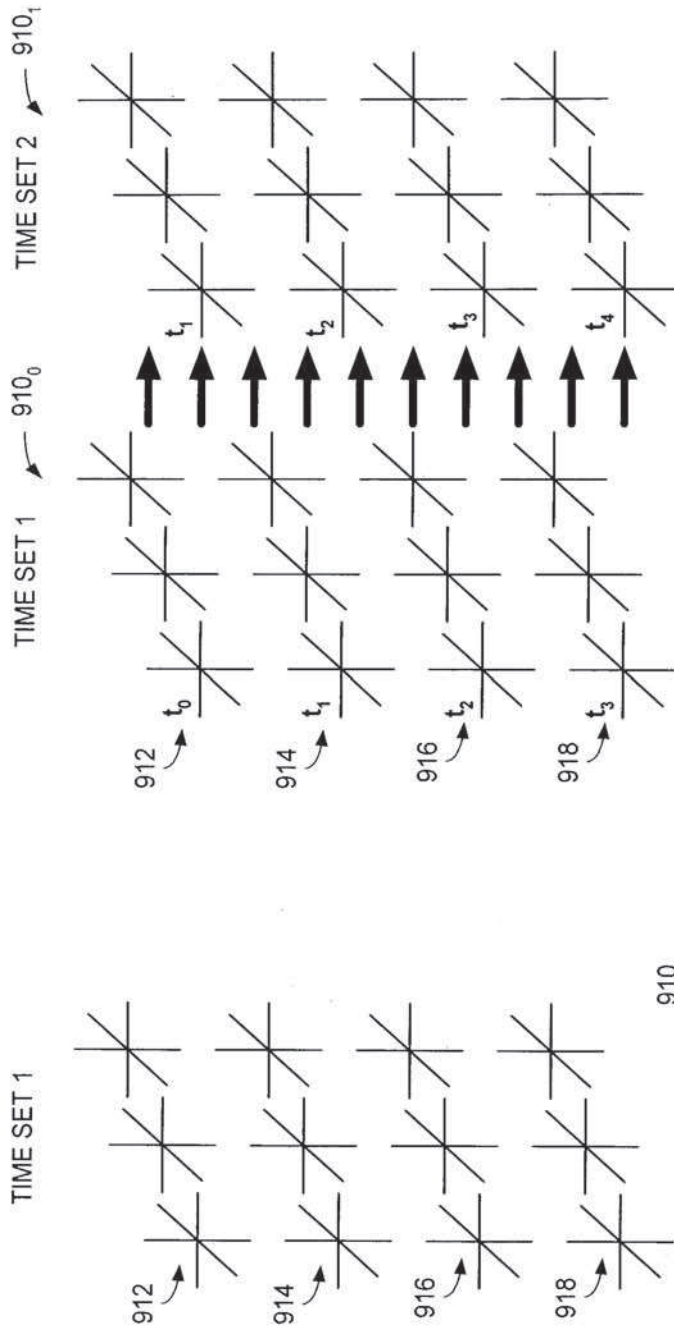


Fig. 9C

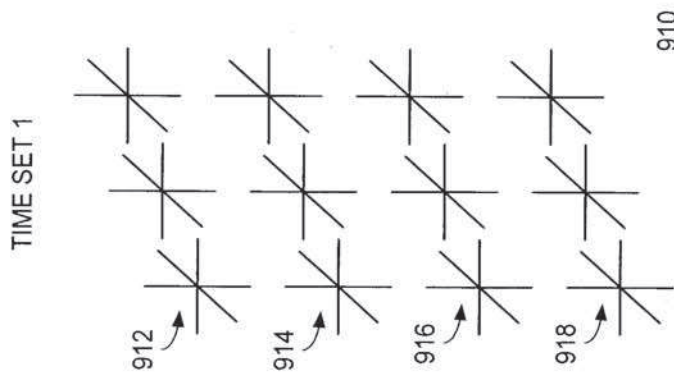


Fig. 9B

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)	Attorney Docket No.	SRC015
	First Named Inventor	Jon M. Huppenthal et al.
	<i>COMPLETE IF KNOWN</i>	
	Application Number	-----
<input checked="" type="checkbox"/> Declaration Submitted with Initial Filing OR <input type="checkbox"/> Declaration Submitted after Initial Filing--surcharge 37 CFR 1.16(e) required	Filing Date	Herewith
	Group Art Unit	
	Examiner Name	

As a below named Inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING
 PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

the specification of which

is attached hereto

OR

was filed on (MM/DD/YYYY) as U.S. Application No. or PCT International Application No.

and was amended on (MM/DD/YYYY) (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C § 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Appl. No.(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				Yes	No
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Additional foreign application nos. are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

DECLARATION – Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any U.S. application(s) or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application

U.S. Parent Application or PCT Parent No.	Parent Filing Date (MM/DD/YY)	Parent Patent No. (if applicable)

Additional U.S. or PCT international application nos. listed on PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent Trademark Office connected therewith:


Customer Number **25235** Place bar code label here 00 

OR

Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number

Additional registered practitioner(s) named on supplemental sheet PTO/SB/02C attached hereto.

Direct all correspondence to: Customer Number **25235** OR Correspondence address below
or Bar Code Label 

Name					
Address					
City		State		ZIP	
Country		Telephone		Fax	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: A petition has been filed for this unsigned inventor.

Given Name (first and middle [if any]) _____ Family Name or Surname _____

Jon M. _____ **Huppenthal** _____

Inventor's Signature _____ Date _____

Residence City **Colorado Springs** State **Colorado** Country **USA** Citizenship **USA**

Mailing Address **10015 Burgess Road**

City **Colorado Springs** State **Colorado** ZIP **80908** Country **USA**

Additional inventors are named on 1 supplemental additional inventor(s) sheet(s) PTO/SB/02A attached

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number

1028538

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	55	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	55 minus 20 = *	35
INDEPENDENT CLAIMS	4 minus 3 = *	1
MULTIPLE DEPENDENT CLAIM PRESENT		<input type="checkbox"/>

SMALL ENTITY TYPE OR

OTHER THAN SMALL ENTITY

RATE	FEE	OR	RATE	FEE
BASIC FEE	370.00		BASIC FEE	740.00
X\$ 9=			X\$18=	630
X42=			X84=	84
+140=			+280=	
TOTAL			TOTAL	1984

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total *	Minus **	=
	Independent *	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			<input type="checkbox"/>

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X\$ 9=			X\$18=	
X42=			X84=	
+140=			+280=	
TOTAL ADDIT. FEE			TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total *	Minus **	=
	Independent *	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			<input type="checkbox"/>

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X\$ 9=			X\$18=	
X42=			X84=	
+140=			+280=	
TOTAL ADDIT. FEE			TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total *	Minus **	=
	Independent *	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			<input type="checkbox"/>

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X\$ 9=			X\$18=	
X42=			X84=	
+140=			+280=	
TOTAL ADDIT. FEE			TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.



Commissioner for Patents
Washington, DC 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/285,318	10/31/2002	Jon M. Huppenthal	SRC015

25235
HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

CONFIRMATION NO. 1420

FORMALITIES LETTER



OC00000009216113

Date Mailed: 12/09/2002

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
Applicant must submit \$ 740 to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).
- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- Additional claim fees of **\$714** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

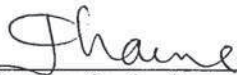
SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$1584** for a Large Entity

- **\$740** Statutory basic filing fee.
- **\$130** Late oath or declaration Surcharge.

- Total additional claim fee(s) for this application is \$714
 - \$630 for 35 total claims over 20 .
 - \$84 for 1 independent claims over 3 .

*A copy of this notice **MUST** be returned with the reply.*



Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE



85

Attorney Docket No. SRC015
Client/Matter No. 80404.0018
Express Mail No. EV035495015US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. 10/285,318

Filed: October 31, 2002

For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND
TECHNIQUES FOR ENHANCING PARALLELISM AND
PERFORMANCE OF COMPUTATIONAL FUNCTIONS

Group Art Unit: 2121

Examiner: Not yet assigned

Confirmation No.: 1420

RESPONSE TO NOTICE TO FILE MISSING PARTS

BOX MISSING PARTS

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Notice to File Missing Parts of Application, Filing Date Granted, mailed December 9, 2002, submitted herewith is a signed Declaration for Patent Application; a check in the amount of \$1,594 to cover \$1,464 for the filing fee and \$130 to cover the surcharge for a large entity; and a copy of the PTO Notice form. Any fee deficiency associated with this communication may be charged to Deposit Account No. 50-1123.

Also enclosed is a Recordation Form Cover Sheet PTO 1595 with executed Assignment and recording fee of \$40.00. Please forward the Assignment to the Recording Branch for recording.

Date: 09 January 2003

William J. Kubida, Registration No. 29,664
HOGAN & HARTSON LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5909 Tel
(303) 899-7333 Fax

COMPLETE FEE TRANSMITTAL
For FY 2003

JAN 09 2003

JAN 09 2002

PATENT & TRADEMARK OFFICE

Complete if Known	
Application Number	10/285,318
Filing Date	October 31, 2002
First Named Inventor	Jon M. Huppenthal et al.
Examiner Name	Not yet assigned
Group / Art Unit	2121
Attorney Docket No.	SRC015

Applicant claims small entity status. See 37 CFR 1.01(b).

TOTAL AMOUNT OF PAYMENT	(\$)	1,634.00
-------------------------	------	-----------------

METHOD OF PAYMENT (check all that apply)

check credit card money order other none

Deposit Account

Deposit Account Number: **50-1123**

Deposit Account Name: **Hogan & Hartson L.L.P.**

The Commissioner is hereby authorized to: (check all that apply)

Charge fee(s) indicated below Credit any overpayments

Charge any additional fee(s) for this filing

Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account

FEE CALCULATION (continued)

FEE CALCULATION

1. BASIC FILING FEE			
Large Entity Fee (\$)	Small Entity Fee (\$)	Fee Description	Fee Paid
750	375	Utility Filing Fee	750.00
330	165	Design filing fee	
520	260	Plant filing fee	
750	375	Reissue filing fee	
160	80	Provisional filing fee	
SUBTOTAL (1)			(\$) 750.00

3. ADDITIONAL FEES			
Large Entity Fee (\$)	Small Entity Fee (\$)	Fee Description	Fee Paid
130	65	Surcharge - late filing fee or oath	130.00
50	25	Surcharge - late provisional filing fee or cover sheet	
130	130	Non-English specification	
2,520	2,520	For filing a request for ex parte reexamination	
920*	920*	Requesting publication of SIR prior to Examiner action	
1,840*	1,840*	Requesting publication of SRI after Examiner action	
110	55	Extension for reply within first month	
410	205	Extension for reply within second month	
930	465	Extension for reply within third month	
1,450	725	Extension for reply within fourth month	
1,970	985	Extension for reply within fifth month	
320	160	Notice of Appeal	
320	160	Filing a brief in support of an appeal	
280	140	Request for oral hearing	
1,510	1,510	Petition to institute a public use proceeding	
110	55	Petition to revive - unavoidable	
1,300	650	Petition to revive - unintentional	
1,300	650	Utility issue fee (or reissue)	
470	235	Design issue fee	
630	315	Plant issue fee	
130	130	Petitions to the Commissioner	
50	50	Processing fee under 37 CFR 1.17(q)	
180	180	Submission of Info Disclosure Stmt	
40	40	Recording each patent assignment per property (times number of properties)	40.00
750	375	Filing a submission after final rejection (37 CFR § 1.129(a))	
750	375	For each additional invention to be examined (37 CFR § 1.129(b))	
750	375	Request for Continued Examination	
900	900	Request for expedited examination of a design application	
		Other fee (specify)	
*Reduced by Basic Filing Fee Paid			SUBTOTAL (3)
			(\$) 170.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims			Fee from below			Fee Paid
Total Claims	55	-20**=	35	X	18	=	630.00	
Independent Claims	4	-3**=	1	X	1	=	84.00	
Multiple Dependent								

***or number previously paid, if greater; For Reissues, see below*

Large Entity Fee (\$)	Small Entity Fee (\$)	Fee Description
18	9	Claims in excess of 20
84	42	Independent claims in excess of 3
280	140	Multiple dependent claim, if not paid
84	42	**Reissue independent claims over original patent
18	9	**Reissue claims in excess of 20 and over original patent
SUBTOTAL (2)		(\$) 714.00

SUBMITTED BY Complete (if applicable)			
Name (Print/Type) William J. Kubida	Registration No. (Attorney/Agent) 29,664	Telephone (719) 448-5900	
Signature	Date 09 January 2007		

01-10-03

HLV

MP/1/1



Attorney Docket No. SRC015
Client/Matter No. 80404.0018
Express Mail No. EV035495015US

AB

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. 10/285,318

Filed: October 31, 2002

For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND
TECHNIQUES FOR ENHANCING PARALLELISM AND
PERFORMANCE OF COMPUTATIONAL FUNCTIONS

Group Art Unit: 2121

Examiner: Not yet assigned

Confirmation No.: 1420

CERTIFICATE OF MAILING BY EXPRESS MAIL

BOX MISSING PARTS
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned hereby certifies that the following documents:

1. Response to Notice to File Missing Parts;
2. Copy of Notice to File Missing Parts of Application Filing Date Granted, form and surcharge payment of \$130;
3. Executed Declaration;
4. Fee Transmittal with check in the amount of \$1,464;
5. Recordation Form Cover Sheet PTO 1595 with Executed Assignment and Recording Fee of \$40.00;
6. Certificate of Mailing By Express Mail;
7. Return postcard;

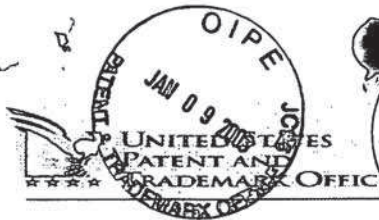
relating to the above application, were deposited as "Express Mail", Mailing Label No. EV035495015US with the United States Postal Service, addressed to Box Missing Parts, Assistant Commissioner for Patents, Washington, D.C., 20231, Jan, 2003

9 January 2003
Date

09 January 2003
Date

Mailed

William J. Kubida, Reg. No. 29,664
HOGAN & HARTSON LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5909 Tel
(303) 899-7333 Fax



AB

Commissioner for Patents
Washington, DC 20231
www.uspto.gov

APPLICATION NUMBER	FILING RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/285,318	10/31/2002	Jon M. Huppenthal	SRC015

CONFIRMATION NO. 1420

FORMALITIES LETTER



OC00000009216113

25235
HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

Date Mailed: 12/09/2002

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- o The statutory basic filing fee is missing.
Applicant must submit \$ 740 to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).
- o The oath or declaration is unsigned.
- o To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- o Additional claim fees of \$714 as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$1584** for a Large Entity

- o \$740 Statutory basic filing fee.
- o \$130 Late oath or declaration Surcharge.

01/13/2003 NHOHAAA1 00000075 10285318		
01 FC:1001		750.00 OF
02 FC:1051		130.00 OF
03 FC:1202		630.00 OF
04 FC:1201		84.00 OF

- Total additional claim fee(s) for this application is \$714
 - \$630 for 35 total claims over 20 .
 - \$84 for 1 independent claims over 3 .

*A copy of this notice **MUST** be returned with the reply.*

Shaine

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)	Attorney Docket No.	SRC015
	First Named Inventor	Jon M. Huppenthal et al.
COMPLETE IF KNOWN		
<input type="checkbox"/> Declaration Submitted with Initial Filing <input checked="" type="checkbox"/> Declaration Submitted after Initial Filing--surcharge 37 CFR 1.16(e) required	Application Number	10/285,318
	Filing Date	October 31, 2002
	Group Art Unit	2121
	Examiner Name	Not yet assigned

As a below-named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

the specification of which

is attached hereto

OR

was filed on (MM/DD/YYYY)

10/31/2002

as U.S. Application No. or PCT International Application No.

10/285,318

and was amended on (MM/DD/YYYY)

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C § 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Appl. No.(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				Yes	No
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

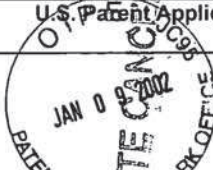
Additional foreign application nos. are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)


DECLARATION - Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any U.S. application(s) or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application

U.S. Patent Application or PCT Parent No. 	Parent Filing Date (MM/DD/YY) 	Parent Patent No. (if applicable)
--	-----------------------------------	---------------------------------------

Additional U.S. or PCT international application nos. listed on PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent Trademark Office connected therewith:


Customer Number **25235** Place bar code label here 00 

OR

Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number

Additional registered practitioner(s) named on supplemental sheet PTO/SB/02C attached hereto.

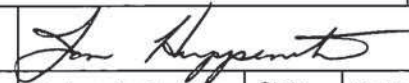
Direct all correspondence to: Customer Number **25235** OR Correspondence address below
 or Bar Code Label 

Name		Address	
City	State	ZIP	
Country	Telephone	Fax	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: A petition has been filed for this unsigned inventor.

Given Name (first and middle [if any]) Jon M.	Family Name or Surname Huppenthal
---	---

Inventor's Signature 	Date 1/6/03		
Residence City Colorado Springs	State Colorado	Country USA	Citizenship USA
Mailing Address 10015 Burgess Road			
City Colorado Springs	State Colorado	ZIP 80908	Country USA

Additional inventors are named on 1 supplemental additional inventor(s) sheet(s) PTO/SB/02A attached

  DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet Page <u> 1 </u> of <u> 1 </u>
---	---

Name of Additional Joint Inventor, if any:		<input type="checkbox"/> A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])		Family Name or Surname					
David E.		Caliga					
Inventor's Signature	<i>D. E. Caliga</i>					Date	1/6/2003
Residence: City	Colorado Springs	State	CO	Country	USA	Citizenship	USA
Mailing Address	8445 Luralwood Lane						
City	Colorado Springs	State	CO	ZIP	80919	Country	USA
Name of Additional Joint Inventor, if any:		<input type="checkbox"/> A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])		Family Name or Surname					
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Mailing Address							
City		State		ZIP		Country	
Name of Additional Joint Inventor, if any:		<input type="checkbox"/> A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])		Family Name or Surname					
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Mailing Address							
City		State		ZIP		Country	



08/14/03

2121
#4
SP
8-21-03

Express Mail No. EV335405389US
Attorney Docket No. SRC015
Client/Matter No. 80404.0018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. 10/285,318

Filed: October 31, 2002

For: MULTI-ADAPTIVE PROCESSING SYSTEMS
AND TECHNIQUES FOR ENHANCING
PARALLELISM AND PERFORMANCE OF
COMPUTATIONAL FUNCTIONS

Group Art Unit: 2121

Examiner: Not yet assigned

Confirmation No.: 1420

RECEIVED

AUG 18 2003

Technology Center 2100

RECEIVED

AUG 20 REC'D

TC 2100

CERTIFICATE OF MAILING BY EXPRESS MAIL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

The undersigned hereby certifies that the attached:

1. Information Disclosure Statement;
2. Form PTO/SB/08A, with references;
3. Certificate of Mailing; and
4. Return card

relating to the above application, were deposited as "Express Mail" Mailing Label No. EV335405389US, with the United States Postal Service, addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 13 August 2003

13 August 2003
Date

Aug. 13, 2003
Date

Mailer

Peter J. Meza
Peter J. Meza, Reg. No. 32,920
HOGAN & HARTSON LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5900 Tel
(303) 899-7333 Fax



Express Mail No. EV335405389US
Attorney Docket No. SRC015
Client/Matter No. 80404.0018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. 10/285,318

Filed: October 31, 2002

For: MULTI-ADAPTIVE PROCESSING SYSTEMS
AND TECHNIQUES FOR ENHANCING
PARALLELISM AND PERFORMANCE OF
COMPUTATIONAL FUNCTIONS

Group Art Unit: 2121

Examiner: Not yet assigned

Confirmation No.: 1420

RECEIVED

AUG 18 2003

Technology Center 2100

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits for filing under 37 CFR 1.97 a disclosure statement. In submitting these references, no representation is made or implied that the references are or are not material to the examination of this application. The patents, publications or other information of which Applicant is presently aware are listed in Form PTO/SB/08A submitted herewith and copies of all such patents and publications are attached hereto.

No fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

Aug. 13, 2003
Date


Peter J. Meza, Reg. No. 32,920
HOGAN & HARTSON LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5906 Tel
(303) 899-7333 Fax



PTO/SB/08A (10/01) (Substitute for form 1449A) INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) Sheet <u>1</u> of <u>4</u>	ATTY. DOCKET NO. SRC015 Client/Matter No. 80404.0018	APPLICATION NO. 10/285,318
	FIRST NAMED INVENTOR Jon M. Huppenthal and David E. Caliga	
	FILING DATE October 31, 2002	ART UNIT 2121

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U.S. PATENT DOCUMENTS

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Examiner Initials	Cite No.	Document No. No. - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		US-5,892,962	04/06/99	Cloutier	
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		US-6,192,439	02/20/2001	Grunewald et al.	Fig 3, col 3, lines 53-67, col 4, lines 1-64.
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Examiner Initials	Cite No.	Foreign Patent Doc cntry code - No. - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	TRANSLATION	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jon M. Huppenthal and David E. Caliga

Serial No. 10/285,318

Filed: October 31, 2002

For: MULTI-ADAPTIVE PROCESSING SYSTEMS AND
TECHNIQUES FOR ENHANCING PARALLELISM
AND PERFORMANCE OF COMPUTATIONAL
FUNCTIONS

Confirmation No.: 1420

Examiner: Not yet assigned

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Jon M. Huppenthal and David E. Caliga
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Respectfully submitted,

Date:

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		Filing Date October 31, 2002
		First Named Inventor Jon M. Huppenthal et al.
		Art Unit 2121
		Examiner Name Not yet assigned
Sheet 1 of 1		Attorney Docket No. SRC015

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		US-6,215,898	04/10/2001	Woodfill et al.	Fig. 3 and col. 9, line 32-col. 16, line 45, and col. 57, line 6-col.67, line 23.
		US-5,020,059	05/28/1991	Gorin et al.	Figs. 5, 9 and col. 7, line 28-col. 9, line 53.
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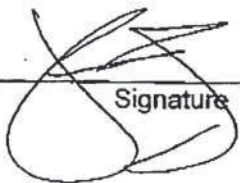
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Jon M. Huppenthal and David E. Caliga
Serial No. 10/285,318
Filed: October 31, 2002
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TECHNIQUES FOR ENHANCING PARALLELISM
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Respectfully submitted,

Date: 26 April 2005



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			Filing Date	October 31, 2002
			First Named Inventor	Jon M. Huppenthal et al.
			Art Unit	2121
			Examiner Name	Not yet assigned
			Attorney Docket No.	SRC015
Sheet	1	of	1	

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		US-4,872,133	10/03/1989	Leeland	
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		US-5,072,371	12/10/1991	Benner et al.	
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		Country Code ⁴	Number ⁵ Kind Code ⁶				

EXAMINER SIGNATURE	DATE CONSIDERED
<p><small>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language translation is attached.</small></p> <p><small>This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) and application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</small></p>	

PATENT COOPERATION TREATY

From the INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
 CAROL W. BURTON
 HOGAN & HARTSON, LLP
 1200 17TH STREET, SUITE 1500
 DENVER, CO 80202

PCT

WRITTEN OPINION

(PCT Rule 66)

Applicant's or agent's file reference		Date of Mailing (day/month/year)
SRC015 PCT		02 MAR 2005
International application No.	International filing date (day/month/year)	Priority date (day/month/year)
PCT/US03/29444	16 September 2003 (16.09.2003)	31 October 2002 (31.10.2002)
International Patent Classification (IPC) or both national classification and IPC		
IPC(C): G06F 15/80, 17/16 and US Cl.: 712/15; 708/509		
Applicant		
SRC COMPUTERS, INC.		

1. This written opinion is the first (first, etc.) drawn by this International Preliminary Examining Authority.

2. This opinion contains indications relating to the following items:

- I Basis of the opinion
- II Priority
- III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- IV Lack of unity of invention
- V Reasoned statement under Rule 66.2 (a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI Certain documents cited
- VII Certain defects in the international application
- VIII Certain observations on the international application

3. The applicant is hereby invited to reply to this opinion.

When? See the time limit indicated above. The applicant may, before the expiration of that time limit, request this Authority to grant an extension. See rule 66.3(d).

How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.

Also For an additional opportunity to submit amendments, see Rule 66.4. For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4 bis. For an informal communication with the examiner, see Rule 66.6

If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary examination report must be established according to Rule 69.2 is: 28 February 2005 (28.02.2005)

Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703)305-3230	Authorized officer Eric Coleman <i>James A. Matthews</i> Telephone No. (703)-305-3900
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Form PCT/IPEA/406 (cover sheet)(July 1998)

WRITTEN OPINION

International application No.

PCT/US03/29444

I. Basis of the opinion

1. With regard to the elements of the international application:*

- the international application as originally filed
- the description:
 pages 1-20, as originally filed
 pages NONE, filed with the demand
 pages NONE, filed with the letter of _____
- the claims:
 pages 21-23, as originally filed
 pages NONE, as amended (together with any statement) under Article 19
 pages NONE, filed with the demand
 pages NONE, filed with the letter of _____
- the drawings:
 pages 1-20, as originally filed
 pages NONE, filed with the demand
 pages NONE, filed with the letter of _____
- the sequence listing part of the description:
 pages NONE, as originally filed
 pages NONE, filed with the demand
 pages NONE, filed with the letter of _____

2. With regard to the language, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item. These elements were available or furnished to this Authority in the following language _____ which is:

- the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).
- the language of publication of the international application (under Rule 48.3(b)).
- the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, the written opinion was drawn on the basis of the sequence listing:

- contained in the international application in printed form.
- filed together with the international application in computer readable form.
- furnished subsequently to this Authority in written form.
- furnished subsequently to this Authority in computer readable form.
- The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- the description, pages NONE
- the claims, Nos. NONE
- the drawings, sheets/fig NONE

5. This opinion has been drawn as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

* Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed."

Form PCT/IPEA/408 (Box I) (July 1998)

WRITTEN OPINION

International application No.
PCT/US03/29444

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims <u>1-13</u>	YES
	Claims <u>NONE</u>	NO
Inventive Step (IS)	Claims <u>6-12</u>	YES
	Claims <u>1-5,13</u>	NO
Industrial Applicability (IA)	Claims <u>1-13</u>	YES
	Claims <u>NONE</u>	NO

2. CITATIONS AND EXPLANATIONS
Please See Continuation Sheet

Form PCT/IPEA/408 (Box V) (July 1998)

WRITTEN OPINION

International application No.
PCT/US03/29444Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)**TIME LIMIT:**

The time limit set for response to a Written Opinion may not be extended. 37 CFR 1.484(d). Any response received after the expiration of the time limit set in the Written Opinion will not be considered in preparing the International Preliminary Examination Report.

V. 2. Citations and Explanations:

Claims 1-2 lack an inventive step under PCT Article 33(3) as being obvious over Gupta (US patent No. 6,385,757) in view of Khan US Patent No. 5,274,832).

Gupta taught the invention substantially as claimed including a data processing ("DP") system comprising: defining a calculation for a reconfigurable computing system insumating the performance of at least two array functional units (FU00-FU10)(e.g., see col. 17, lines 28-52 and col. 21, lines 22-29) to perform the calculation.

Gupta did not expressly detail utilizing the array functional units to operate on a subsequent data dimension of the calculation and substantially concurrently using the second of the array units to operate on a previous data dimension of the calculation. Khan however taught operating on three dimensions using plural two dimensional arrays that operate concurrently on respective dimensions and are coupled to together to produce the three dimensional array (e.g., see col. 4, lines 35-62 and col. 12, lines 15-55).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Gupta and Khan. One of ordinary skill would have been motivated to incorporate the three dimensional array operation of the Khan reference into the Gupta system to allow the combined system to be able to perform calculations on more complicated (three dimensional) problems.

As to claim 2, Khan taught the calculation comprising plurality of planes (e.g., see col. 12, lines 15-55).

Claim 3 lacks an inventive step under PCT Article 33(3) as being obvious over the prior art as applied in the immediately preceding paragraph and further in view of Leeland (US patent No. 4,872,133). Leeland taught calculation comprised a financial application modeling using a spreadsheet application (e.g., see col. 5, lines 3-32).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Leeland and Gupta. One of ordinary skill would have been motivated to incorporate the Leeland teaching of financial spreadsheet application for an array processor in order to provide an additional use for the combined system.

Claims 4-5 lack an inventive step under PCT Article 33(3) as being obvious over the prior art (Gupta and Khan) as applied in the immediately preceding paragraphs and further in view of Benner (US Patent No. 5,071,371).

Benner taught the calculation comprising fluid flow calculation and structural analysis (e.g., see col. 22, lines 35-52).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Benner and Gupta. One of ordinary skill would have been motivated to incorporate the Benner teaching of fluid flow and structural analysis applications for an array processor in order to provide an additional uses for the combined system.

Claim 13 lacks an inventive step under PCT Article 33(3) as being obvious over Gupta (US Patent No. 6,385,757). Gupta taught the invention substantially as claimed including data processing ("DP") system comprising a reconfigurable processor that provides indication of whether it performs speculative and systolic processing (e.g., see col. 15, lines 6-66). Consequently, one

Form PCT/IPEA/408 (Supplemental Box) (July 1998)

WRITTEN OPINION

International application No.
PCT/US03/29444**Supplemental Box**

(To be used when the space in any of the preceding boxes is not sufficient)

ordinary skill would have been motivated to perform systolic and speculative processing at least in order to utilize the parameters indicated by Gupta for use in systolic and speculative processing (e.g., see col. 15, lines 56-63).

Claims 6-12 the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the combination of features in independent claims 6 and 12. The combination features in claim 6 comprise defining a first systolic wall comprising rows and cells forming a subset of the plurality of functional units; computing a value at each of the cells in at least a first row of the first systolic wall; communicating the values between cells in the first row of the cells to produce updated values; communicating the updated values to a second row of the first systolic wall; and substantially concurrently providing the updated values to a first row of a second systolic wall of rows of cells in the subset of the plurality of functional units. In claim 12 the combination of features comprise performing a calculation by a subset of the plurality of functional units to produce computed data; passing the computed data from a first column of the calculation to a next column in the calculation; evaluating a rate of change in at least one variable for each of the columns in the calculation; continuing the calculation if the variable does not change for a particular column of the calculation; and restarting the calculation at the column of the calculation where the variable does change.

NEW CITATIONS

US 6,385,757 B1 (GUPTA) 07 May 2002, see column, 2, lines 20-27, column 15, lines 5-66.

US 4,872,133 A (LEELAND) 03 October 1989, see figs. 2,3,5, and col. 3, lines 27-55.

US 5,274,832 A (KHAN) 28 December 1993, see fig.18, col. 5, lines 27-49, col. 8, lines 42-59, and col. 12, lines 1-55.

US 5,072,371 (BENNER) 10 December 1991 see figs. 5,7,14 and col. 22, lines 35-62.

Form PCT/IPEA/408 (Supplemental Box) (July 1998)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	16	speculat\$3 with systolic\$4	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 07:38
L2	343	speculat\$3 and systolic\$4	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:16
L3	1	speculat\$3 and (systolic\$4 adj process\$3)	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 07:49
L4	140	rate near3 change near3 column\$1	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 07:49
L5	1951069	@ay>"2000"	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:16
L6	127	2 not 5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:33
L7	332	column\$1 near3 value near3 change\$1	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:35
L8	62	restart\$3 and 7	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 08:37
L9	42	until adj value adj change\$2	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:36
L10	201	712/15.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:37
L11	46	712/19.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:37
L12	359	712/226.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:37
L13	2	((("6385757") or ("5274832"))).PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:50
L14	3	((("6385757") or ("5274832") or ("5071371"))).PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 09:57
L15	4	((("6385757") or ("5274832") or ("5071371") or ("4872133"))).PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:03

L16	0	("bennerand(fluidadjflow")).PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:06
L17	74	benner and (fluid adj:flow)	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:23
L18	2089	imaging and systolic\$5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:23
L19	86	imaging with systolic\$5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:38
L20	4	search adj algorithm with systolic\$5	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:48
L21	3	encryption with systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:57
L22	0	genetic near3 match\$3 with systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:57
L23	25	genetic with systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 10:58
L24	5	dna with systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:00
L25	72	protein with systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:01
L26	12835	dna near3 match\$3 systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:02
L27	8	dna near3 match\$3 and systolic\$3	US-PGPUB; USPAT; EPO	OR	OFF	2005/10/03 11:02



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/285,318	10/31/2002	Jon M. Huppenthal	SRC015	1420
25235	7590	10/07/2005	EXAMINER COLEMAN, ERIC	
HOGAN & HARTSON LLP ONE TABOR CENTER, SUITE 1500 1200 SEVENTEENTH ST DENVER, CO 80202			ART UNIT	
			PAPER NUMBER 2183	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/285,318	Applicant(s) HUPPENTHAL ET AL	
	Examiner Eric Coleman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on ____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-55 is/are pending in the application.
 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) Claim(s) ____ is/are allowed.
- 6) Claim(s) 1-55 is/are rejected.
- 7) Claim(s) ____ is/are objected to.
- 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on ____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. ____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-5,26-31,52,53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta (US patent No. 6,385,757) in view of Khan US Patent No. 5,274,832).

3. Gupta taught the invention substantially as claimed including a data processing ("DP") system comprising: defining a calculation for a reconfigurable computing system instantiating the performance of at least two array functional units (FU00-FU10)(e.g., see col. 17, lines 28-52 and col. 21, lines 22-29) to perform the calculation.

4. Gupta did not expressly detail utilizing the array functional units to operate on a subsequent data dimension of the calculation and substantially concurrently using the second of the array units to operate on a previous data dimension of the calculation. Khan however taught operating on three dimensions using plural two dimensional arrays that operate concurrently on respective dimensions and are coupled to together to produce the three dimensional array (e.g., see col. 4, lines 35-62 and col. 12, lines 15-55).

5. It would have been obvious to one of ordinary skill in the DP art to combine the

teachings of Gupta and Khan. One of ordinary skill would have been motivated to incorporate the three dimensional array operation of the Khan reference into the Gupta system to allow the combined system to be able to perform calculations on more complicated (three dimensional) problems.

6. As to the further limitations of claim 26, Khan taught (e.g., see fig. 8) a three dimensional systolic array with connections between processors in three dimensions.

7. As to claim 2-5,27-30 Khan taught the calculation comprising plurality of planes, and grid points and plural time-steps and vectors(e.g., see fig. 8 and col. 12, lines 15-55). As per claim 31, the system taught by Khan shows direct connection between the processing elements in the array and therefore the storing of data to an extrinsic memory (i.e., outside the array) would have been unnecessary when the transfer of data between columns was performed (e.g., see fig. 8).

8. As to the limitations of claims 52 and 53 the reconfigurable systolic processor would have been able to adapt to the application and therefore would have been an adaptive processor. As to the processor comprising a microprocessor one of ordinary skill would have been motivated to implement the systolic processor as described above as a microprocessor at least to take advantage of the reduced cost and reduced system size as was well known in the art at the time of the claimed invention.

9. Claims 19,45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Leeland (US patent No. 4,872,133).

10. Leeland taught calculation comprised a financial application modeling using a spreadsheet application (e.g., see col. 5, lines 3-32).

11. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Leeland and Gupta. One of ordinary skill would have been motivated to incorporate the Leeland teaching of financial spreadsheet application for an array processor in order to provide an additional use for the combined system.

12. Claim 10-16 and 36-42,54 rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Benner (US Patent No. 5,072,371).

13. Benner taught the calculation comprising fluid flow calculation and structural analysis (e.g., see col. 22, lines 35-52).

14. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Benner and Gupta. One of ordinary skill would have been motivated to incorporate the Benner teaching of fluid flow and structural analysis applications for an array processor in order to provide an additional uses for the combined system.

15. As to the limitation in claim 54 of performing a calculation unit a variable changed is value in a system processing an restarting at that value The Benner system taught systolically performing calculations on fluid flow. Since in such a problem one of ordinary skill would at times be interested when a change in the data occurred and adjust the calculation to pin point the calculation around that certain point then one of ordinary skill would have been motivated to operate the Benner and Gupta and Khan

system to process systolically until a change in data occurred and then restart the calculation at the point of the change to better determine the magnitude of the change in data.

16. Claim 6-9,25,32-35,51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Helbig (US patent No. 4,962,381).

17. Helbig taught the application of a systolic processor for radar, medical ultrasound and other imaging applications (e.g., see col. 1, lines 1-5) Clearly this would have also comprised images processed by standard MPEG and JPEG standards.

18. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Helbig and Gupta. One of ordinary skill would have been motivated to incorporate the Helbig teaching of radar, medical ultrasound and other imaging applications for an systolic processor in order to provide an additional uses for the combined system.

19. As to the limitation of claims 25 and 51, since signal filtering would have been associated with the applications taught by Helbig such as radar then one of ordinary skill would have been motivated to use the Helbig systolic processor in signal filtering applications.

20. Claim 17,18,22-24,43,44,48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Skaletsky (US patent No. 5,784,108).

21. Skaletsky taught using an systolic processor for processing search algorithm for image search such as when a best match was to be found and clearly this would have been applicable to data mining as these are similar applications (e.g., see col. 3, line 13-col. 4, line 57).

22. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Skaletsky and Gupta. One of ordinary skill would have been motivated to incorporate the Skaletsky teaching of search algorithm applications for an systolic processor in order to provide an additional uses for the combined system.

23. As to the limitations of claims 22-24,48-50 in light of the search algorithm teaching especially for finding a best match for data then the use of systolic processors for similar applications such as the genetic pattern matching, protein folding and organic structure interaction would have been an obvious uses for systolic processors (such as taught by Skaletsky) to one of ordinary skill in the DP art.

24. Claim 20,21,46,47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta and Khan as applied to claims 1-2,26 above, and further in view of Gai (US patent No. 6,061,706).

25. Gai taught use of systolic processors in encryption/decryption applications to speed the encryption/decryption of public keys (e.g. see col. 1, lines 25-41).

26. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Gai and Gupta. One of ordinary skill would have been motivated to

incorporate the Gai teaching of encryption and decryption applications for an systolic processor in order to provide an additional uses for the combined system.

27. Claims 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta (US patent No. 6,385,757)

28. Gupta taught the invention substantially as claimed including data processing ("DP") system comprising a reconfigurable processor that provides indication of whether it performs speculative and systolic processing (e.g., see col. 15, lines 6-66).


Consequently, one ordinary skill would have been motivated to perform systolic and speculative processing at least in order to utilize the parameters indicated by Gupta for use in systolic and speculative processing (e.g., see col. 15, lines 56-63).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC



ERIC COLEMAN
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 10/285,318	Applicant(s)/Patent Under Reexamination HUPPENTHAL ET AL	
	Examiner Eric Coleman	Art Unit 2183	Page 1 of 1

U.S. PATENT DOCUMENTS

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A US-4,872,133	10-1989	Leeland, Steven B.	708/509
*	B US-5,274,832	12-1993	Khan, Emdadur R.	708/424
*	C US-6,385,757	05-2002	Gupta et al.	716/1
*	D US-5,072,371	12-1991	Benner et al.	712/11
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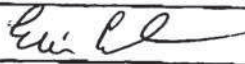
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	10/285,318
		Filing Date	October 31, 2002
		First Named Inventor	Jon M. Huppenthal et al.
		Art Unit	2121
		Examiner Name	Not yet assigned
		Attorney Docket No.	SRC015
Sheet	1	of	1

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PTO/SB/08A (10/01) (Substitute for form 1449A)	ATTY. DOCKET NO. SRC015 Client/Matter No. 80404.0018	APPLICATION NO. 10/285,318
	FIRST NAMED INVENTOR Jon M. Huppenthal and David E. Caliga	
	FILING DATE October 31, 2002	ART UNIT 2121

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 Sheet 1 of 4

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