Homayoun

Reference 18

(12) **United States Patent**

Casselman

(10) **Patent No.:** **US 7,856,545 B2**

(45) **Date of Patent:** **Dec. 21, 2010**

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(54) **FPGA CO-PROCESSOR FOR ACCELERATED COMPUTATION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 727 days.

(21) Appl. No.: **11/829,801**

(22) Filed: **Jul. 27, 2007**

(65) **Prior Publication Data**

US 2008/0028186 A1 Jan. 31, 2008

Related U.S. Application Data

(60) Provisional application No. 60/820,730, filed on Jul. 28, 2006.

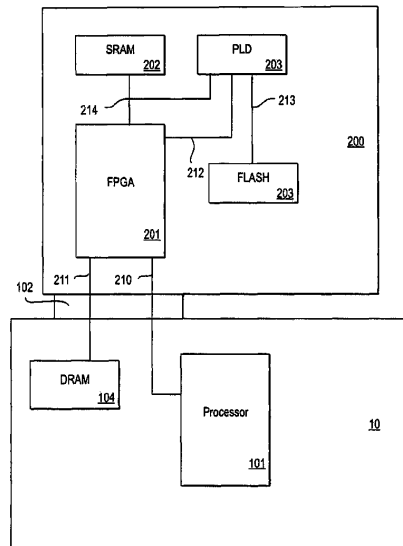(51) **Int. Cl.**
G06F 15/00 (2006.01)
G06F 15/76 (2006.01)

(52) **U.S. Cl.** **712/34**

(58) **Field of Classification Search** 712/34
See application file for complete search history.

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(57) **ABSTRACT**

A co-processor module for accelerating computational performance includes a Field Programmable Gate Array ("FPGA") and a Programmable Logic Device ("PLD") coupled to the FPGA and configured to control start-up configuration of the FPGA. A non-volatile memory is coupled to the PLD and configured to store a start-up bitstream for the start-up configuration of the FPGA. A mechanical and electrical interface is for being plugged into a microprocessor socket of a motherboard for direct communication with at least one microprocessor capable of being coupled to the motherboard. After completion of a start-up cycle, the FPGA is configured for direct communication with the at least one microprocessor via a microprocessor bus to which the microprocessor socket is coupled.

14 Claims, 6 Drawing Sheets

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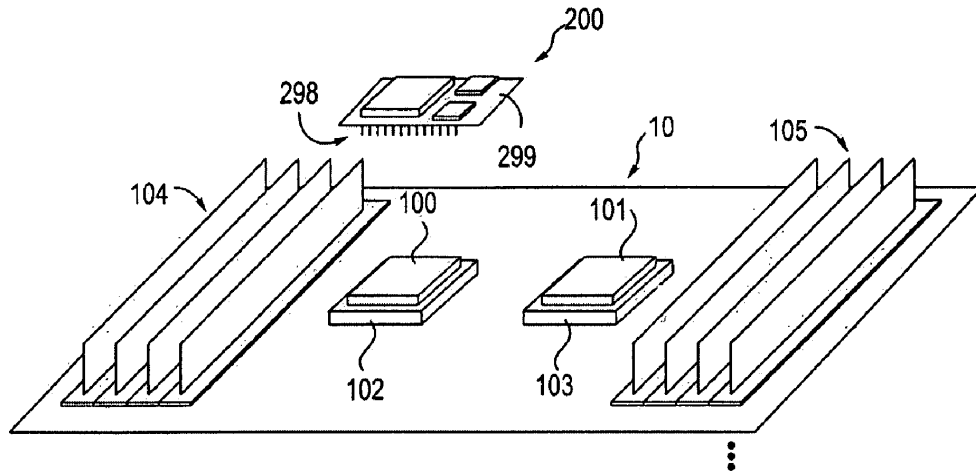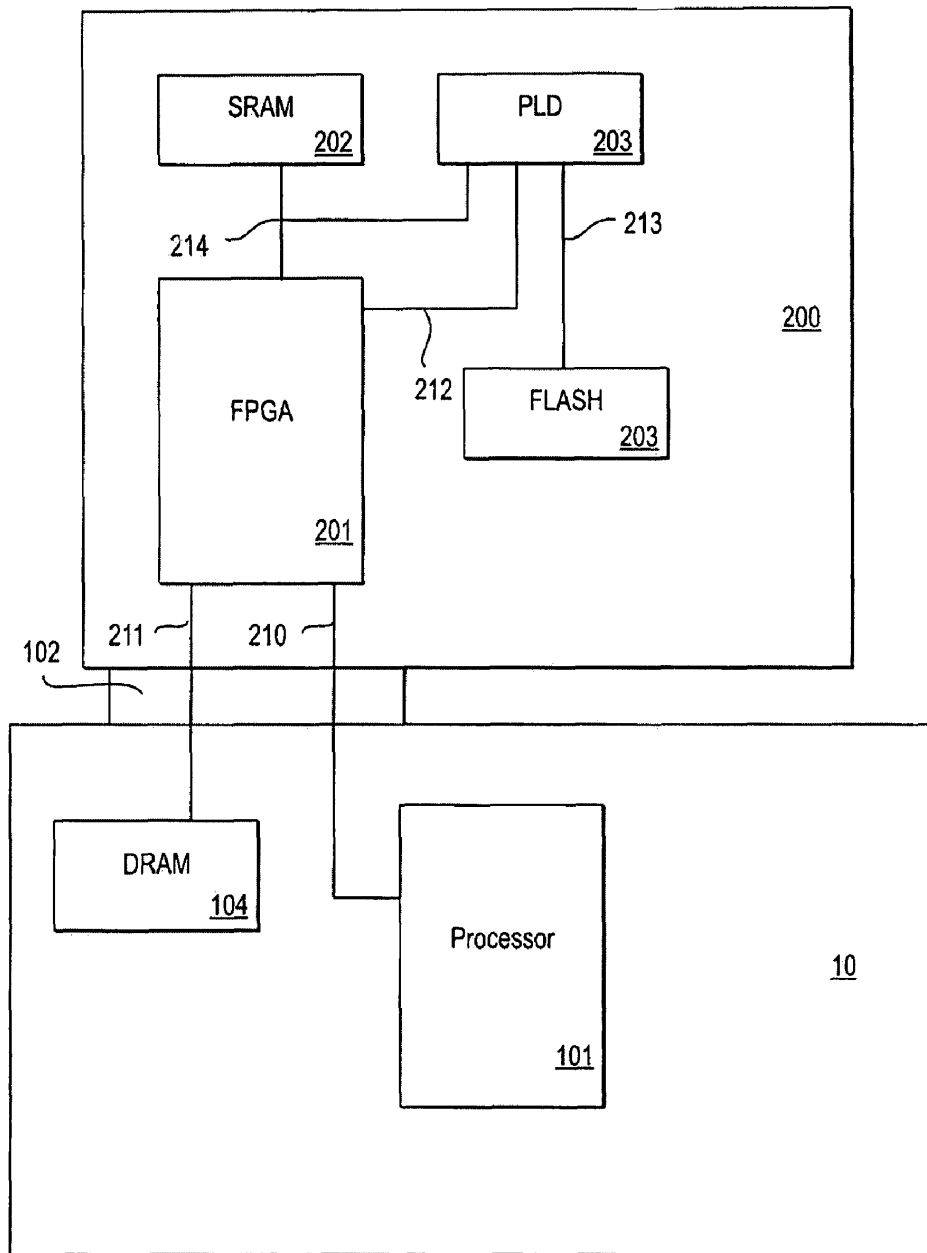
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FIG. 1

FIG. 2

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