Homayoun

Reference 6

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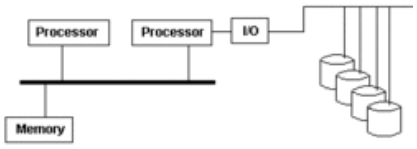
Asymmetric multiprocessing

An **asymmetric multiprocessing** (**AMP**) system is a multiprocessor computer system where not all of the multiple interconnected central processing units (CPUs) are treated equally. For example, a system might allow (either at the hardware or operating system level) only one CPU to execute operating system code or might allow only one CPU to perform I/O operations. Other AMP systems might allow any CPU to execute operating system code and perform I/O operations, so that they were symmetric with regard to processor roles, but attached some or all peripherals to particular CPUs, so that they were asymmetric with respect to the peripheral attachment.

Asymmetric multiprocessing was the only method for handling multiple CPUs before symmetric multiprocessing (SMP) was available. It has also been used to provide less expensive options[1] on systems where SMP was available. Additionally, AMP is used in applications that are dedicated, such as embedded systems, when individual processors can be dedicated to specific tasks at design time.[2]

Contents



Asymmetric multiprocessing

Background and history

For the room-size computers of the 1960s and 1970s, a cost-effective way to increase compute power was to add a second CPU. Since these computers were already close to the fastest available (near the peak of the price:performance ratio), two standard-speed CPUs were much less expensive than a CPU that ran twice as fast. Also, adding a second CPU was less expensive than a second complete computer, which would need its own peripherals, thus requiring much more floor space and an increased operations staff.

Notable early AMP offerings by computer manufacturers were the Burroughs B5000, the DECsystem-1055, and the IBM System/360 model 65MP. There were also dual-CPU machines built at universities.[3]

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The problem with adding a second CPU to a computer system was that the operating system had been developed for single-CPU systems, and extending it to handle multiple CPUs efficiently and reliably took a long time. To fill this gap, operating systems intended for single CPUs were initially extended to provide minimal support for a second CPU. In this minimal support, the operating system ran on the “boot” processor, with the other only allowed to run user programs. In the case of the Burroughs B5000, the second processor's hardware was not capable of running "control state" code.[4]

Other systems allowed the operating system to run on all processors, but either attached all the peripherals to one processor or attached particular peripherals to particular processors.

Burroughs B5000 and B5500

An option on the Burroughs B5000 was “Processor B”. This second processor, unlike “Processor A” had no connection to the peripherals, though the two processors shared main memory, and Processor B could not run in Control State.[4] The operating system ran only on Processor A. When there was a user job to be executed, it might be run on Processor B, but when that job tried to access the operating system the processor halted and signaled Processor A. The requested operating system service was then run on Processor A.

On the B5500, either Processor A or Processor B could be designated as Processor 1 by a switch on the engineer's panel, with the other processor being Processor 2; both processors shared main memory and had hardware access to the I/O processors hence the peripherals, but only Processor 1 could respond to peripheral interrupts.[5] When a job on Processor 2 required an operating system service it would be rescheduled on Processor 1, which was responsible for both initiating I/O processor activity and responding to interrupts indicating completion. In practice, this meant that while user jobs could run on either Processor 1 or Processor 2 and could access intrinsic library routines that didn't require kernel support, the operating system would schedule them on the latter whenever possible.[6]

CDC 6500 and 6700

Control Data Corporation offered two configurations of its CDC 6000 series that featured two central processors. The CDC 6500[7] was a CDC 6400 with two central processors. The CDC 6700 was a CDC 6600 with the CDC 6400 central processor added to it.

These systems were organized quite differently from the other multiprocessors in this article. The operating system ran on the peripheral processors, while the user's application ran on the CPUs. Thus, the terms ASMP and SMP do not properly apply to these multiprocessors.

DECsystem-1055

Digital Equipment Corporation (DEC) offered a dual-processor version of its DECsystem-1050 which used two KA10 processors.[8][9] This offering was extended to later processors in the PDP-10 line.

PDP-11/74

Digital Equipment Corporation developed, but never released, a multiprocessor PDP-11, the PDP-11/74,[10] running a multiprocessor version of RSX-11M.[11] In that system, either processor could run operating system code, and could perform I/O, but not all peripherals were accessible to all processors; most peripherals were attached to one or the other of the CPUs, so that a processor to which a peripheral wasn't attached would, when it needed to perform an I/O operation on that peripheral, request the processor to which the peripheral was attached to perform the operation.[11]

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VAX-11/782

DEC's first multi-processor VAX system, the VAX-11/782, was an asymmetric dual-processor system; only the first processor had access to the I/O devices.[12]

Univac 1108-II

The Univac 1108-II and its successors had up to three CPUs.[13][14] These computers ran the UNIVAC EXEC 8 operating system, but it is not clear from the surviving documentation where that operating system was on the path from asymmetric to symmetric multiprocessing.

IBM System/370 model 168

Two options were available for the IBM System/370 Model 168 for attaching a second processor.[15] One was the IBM 3062 Attached Processing Unit, in which the second processor had no access to the channels, and was therefore similar to the B5000's Processor B or the second processor on a VAX-11/782. The other option offered a complete second CPU, and was thus more like the System/360 model 65MP.

See also

- 3B20C
- Multi-core (computing)
- Software lockout
- Giant lock
- Symmetric multiprocessing
- Heterogeneous computing

Notes

1. IBM (December 1976). *IBM System/370 System Summary* (http://www.bitsavers.org/pdf/ibm/370/systemSummary/GA22-7001-6_370_System_Summary_Dec76.pdf) (PDF). Seventh Edition. pp. 6–12, 6-15-6.16.1. GA22·7001·6.
2. A Survey Of Techniques for Architecting and Managing Asymmetric Multicore Processors (https://www.researchgate.net/publication/283733254_A_Survey_Of_Techniques_for_Architecting_and_Managing_Asymmetric_Multicore_Processors), ACM Computing Surveys, 2015.
3. Early Computers at Stanford: the dual processor computer at the AI lab (http://forum.stanford.edu/wiki/index.php/Early_Computers_at_Stanford#DEC_PDP-10_2)
4. "Operational Characteristics of the Processors for the Burroughs B5000" (http://www.bitsavers.org/pdf/burroughs/B5000_5500_5700/5000-21005_B5000_operChar.pdf) (PDF). Burroughs.
5. "A Narrative Description of the B5500 MCP" (http://www.bitsavers.org/pdf/burroughs/B5000_5500_5700/1023579_Narrative_Description_Of_B5500_MCP_Oct66.pdf) (PDF). p. 18.
6. A Narrative Description of the B5500 MCP, pages 29 (initiate routine) and 40 (a note on parallel processing) (http://www.bitsavers.org/pdf/burroughs/B5000_5500_5700/1023579_Narrative_Description_Of_B5500_MCP_Oct66.pdf)
7. "CONTROL DATA 6400/6500/6600 COMPUTER SYSTEMS Reference Manual" (http://ed-thelen.org/comp-hist/CDC-6600RefMan.pdf) (PDF).
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9. DECsystem-10 Technical Summary page 2-1 (http://www.bitsavers.org/pdf/dec/pdp10/TOPS10_softwareNotebooks/vol01/DECsystem-10_Technical_Summary_1981.pdf)

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10. "(PDP-11) Multiprocessor FAQ" (http://www.miim.com/faq/hardware/multipro.html).
11. "RSX-11M multiprocessing" (http://www.bitsavers.org/pdf/dec/pdp11/1174/RSX11-mP_FuncSpec_Apr77.pdf) (PDF). Digital Equipment Corporation.
12. VAX Product Sales Guide, pages 1-23 and 1-24 (http://www.bitsavers.org/pdf/dec/vax/EG-21731-18_VAX_Product_Sales_Guide_Apr82.pdf): the VAX-11/782 is described as an asymmetric multiprocessing system in 1982
13. "Univac 1108-II announcement" (http://archive.computerhistory.org/resources/text/Remington_Rand/SperryRand.UNIVAC1108II.1965.102646105.pdf) (PDF). Sperry Rand.
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15. IBM (January 1976). *IBM System/370 Model 168 Functional Characteristics* (http://www.bitsavers.org/pdf/ibm/370/funcChar/GA22-7010-4_370-168_funcChar_Jul76.pdf) (PDF). Fifth Edition. GA22·7010-4.

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External links

- OpenMP tutorial for parallel programming (http://www.llnl.gov/computing/tutorials/openMP/)
- Multicore News blog (http://www.multicorezone.com)
- History of Multi-Processing (http://ei.cs.vt.edu/~history/Parallel.html)
- Linux and Multiprocessing (http://www.ibm.com/developerworks/library/l-linux-smp/)
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