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(54) **MULTIPROCESSOR WITH EACH PROCESSOR ELEMENT ACCESSING OPERANDS IN LOADED INPUT BUFFER AND FORWARDING RESULTS TO FIFO OUTPUT BUFFER**

(75) Inventors: **Jon M. Huppenthal**; **Paul A. Leskar**, both of Colorado Springs, CO (US)

(73) Assignee: **SRC Computers, Inc.**, Colorado Springs, CO (US)

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Related U.S. Application Data

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(52) **U.S. Cl.** **712/16**; 326/39; 326/41; 712/37

(58) **Field of Search** 326/39, 41; 712/16, 712/37

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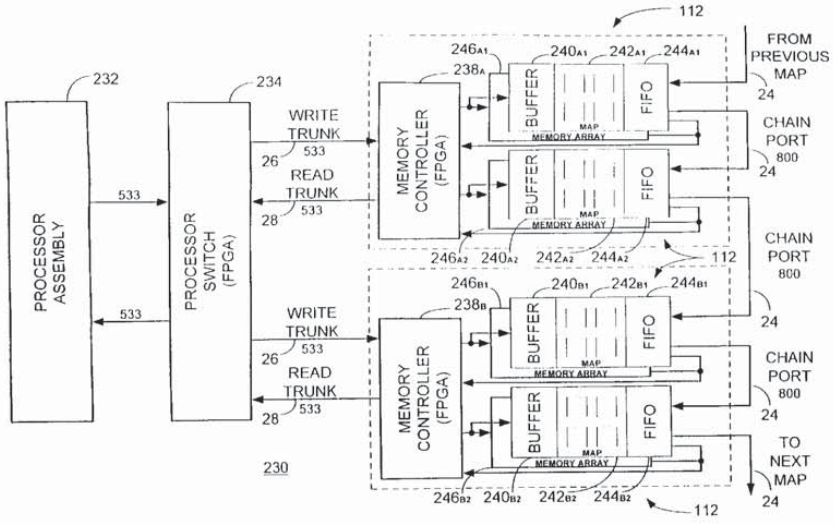
Primary Examiner—Kenneth S. Kim
(74) *Attorney, Agent, or Firm*—William J. Kubida; Kent A. Lembke; Hogan & Hartson LLP

(57) **ABSTRACT**

An enhanced memory algorithmic processor ("MAP") architecture for multiprocessor computer systems comprises an assembly that may comprise, for example, field programmable gate arrays ("FPGAs") functioning as the memory algorithmic processors. The MAP elements may further include an operand storage, intelligent address generation, on board function libraries, result storage and multiple input/output ("I/O") ports. The MAP elements are intended to augment, not necessarily replace, the high performance microprocessors in the system and, in a particular embodiment of the present invention, they may be connected through the memory subsystem of the computer system resulting in it being very tightly coupled to the system as well as being globally accessible from any processor in a multiprocessor computer system.

47 Claims, 11 Drawing Sheets



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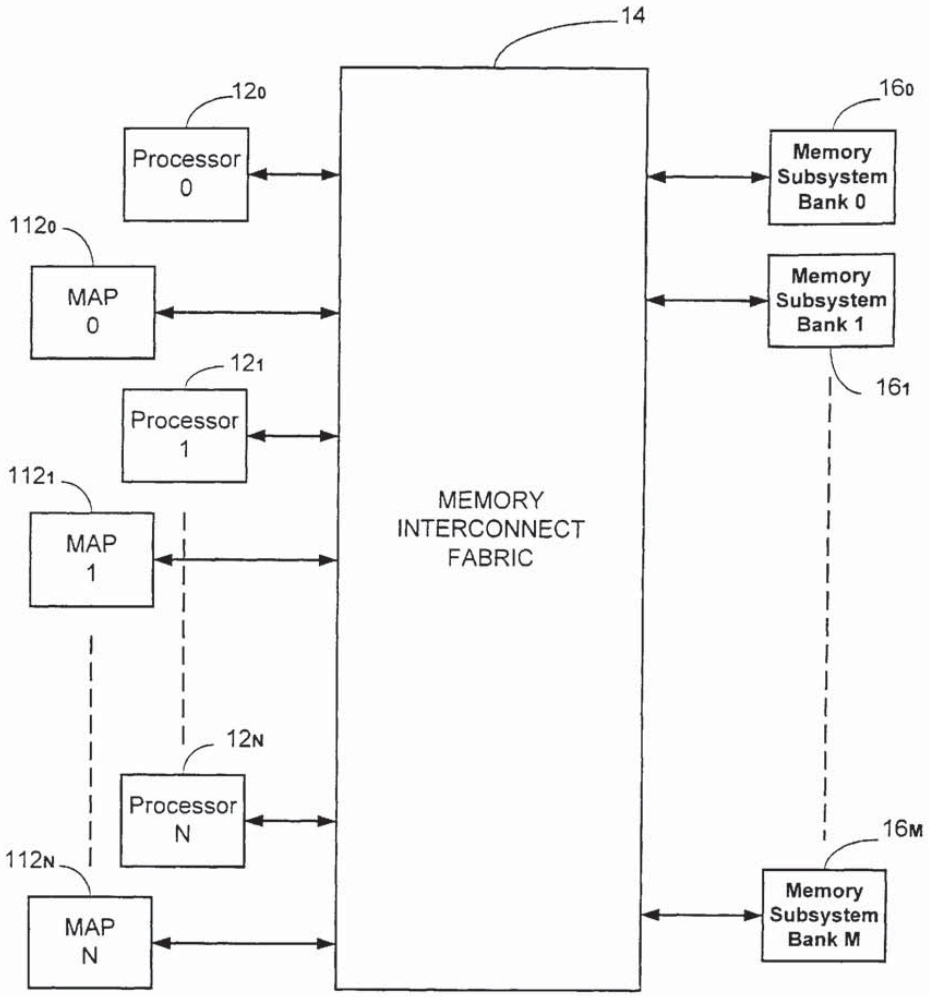

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Fig. 1

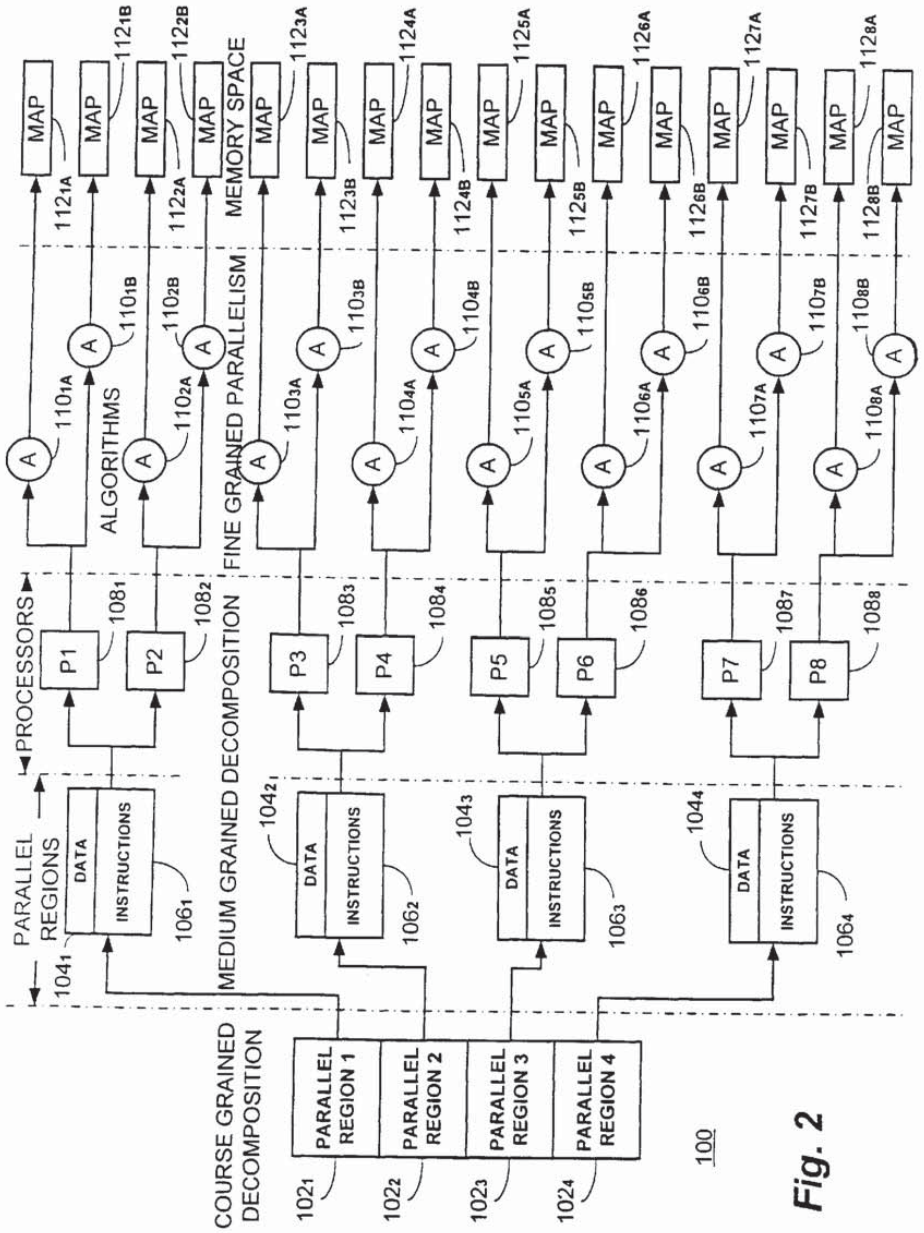

Fig. 2

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