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Paper 72
Date: April 9, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROSOFT CORPORATION,
Petitioner,

v.

FG SRC LLC,[1]
Patent Owner.

IPR2018-01605[2]
Patent 7,620,800 B2

Before KALYAN K. DESHPANDE, JUSTIN T. ARBES, and CHRISTA P. ZADO, *Administrative Patent Judges.*

ARBES, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

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[1] Patent Owner filed updated mandatory notice information indicating that DirectStream, LLC ("DirectStream") assigned the challenged patent to FG SRC LLC. Paper 69, 1. Accordingly, the caption for this proceeding has been changed.

[2] Cases IPR2018-01606 and IPR2018-01607 have been consolidated with this proceeding.

I. INTRODUCTION

A. Background and Summary

Petitioner Microsoft Corporation filed three Petitions, collectively requesting *inter partes* review of claims 1–5, 7–9, 15, 17, 18, and 20–24 of U.S. Patent No. 7,620,800 B2 (Ex. 1005, "the '800 patent") pursuant to 35 U.S.C. § 311(a), as listed in the following chart.[3]

Case Number	Challenged Claims	Petition
IPR2018-01605	1, 8, 9, and 20	Paper 1 ("Pet.")
IPR2018-01606	1, 7, 15, 17, and 24	Paper 1 ("-1606 Pet.")
IPR2018-01607	1–5, 18, and 21–23	Paper 1 ("-1607 Pet.")

On April 12, 2019, we instituted an *inter partes* review as to all challenged claims on all grounds of unpatentability asserted in the Petitions, and exercised our authority under 35 U.S.C. § 315(d) to consolidate the three proceedings and conduct the proceedings as one trial. Paper 21 ("Decision on Institution" or "Dec. on Inst."). Patent Owner FG SRC LLC subsequently filed a Patent Owner Response (Paper 36, "PO Resp."), Petitioner filed a Reply (Paper 49, "Reply"), and Patent Owner filed a Sur-Reply (Paper 59, "Sur-Reply"). Petitioner filed a Motion to Exclude (Paper 60, "Pet. Mot.") certain evidence submitted by Patent Owner, to which Patent Owner filed an Opposition (Paper 63, "PO Opp.") and Petitioner filed a Reply (Paper 66, "Pet. Mot. Reply"). Patent Owner filed a Motion to Exclude (Paper 61, "PO Mot.") certain evidence submitted by Petitioner, to which Petitioner filed an Opposition (Paper 62, "Pet. Opp.")

[3] Unless otherwise noted, references herein are to the exhibits filed in Case IPR2018-01605.

and Patent Owner filed a Reply (Paper 65, "PO Mot. Reply"). An oral hearing was held on February 4, 2020, and a transcript of the hearing is included in the record (Paper 71, "Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–5, 7–9, 15, 17, 18, and 20–24 are unpatentable.

B. Related Matters

The parties indicate that the '800 patent is the subject of the following district court cases: *SRC Labs, LLC v. Microsoft Corp.*, No. 2:18-cv-00321 (W.D. Wash.), and *SRC Labs, LLC v. Amazon Web Servs., Inc.*, No. 2:18-cv-00317 (W.D. Wash.). *See* Pet. 4–5; Paper 69, 1.

C. The '800 Patent

The '800 patent[4] discloses "multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions." Ex. 1005, col. 1, ll. 40–43. Parallel processing "allows multiple processors to work simultaneously on the same problem to achieve a solution" in less time than it would take a single processor. *Id.* at col. 1, ll. 44–49. "[A]s more and more performance is required, so is more parallelism, resulting in ever larger systems" and associated difficulties,

[4] The '800 patent is a continuation of U.S. Patent No. 7,225,324 B2 (Ex. 1001, "the '324 patent"), is challenged by Petitioner in Case IPR2018-01601. We enter a Final Written Decision in Case IPR2018-01601 concurrently with this Decision.

including "facility requirements, power, heat generation and reliability." *Id.* at col. 1, ll. 53–61. The '800 patent discloses that

> if a processor technology could be employed that offers orders of magnitude more parallelism per processor, these systems could be reduced in size by a comparable factor. Such a processor or processing element is possible through the use of a reconfigurable processor. Reconfigurable processors instantiate only the functional units needed to solve a particular application, and as a result, have available space to instantiate as many functional units as may be required to solve the problem up to the total capacity of the integrated circuit chips they employ.

Id. at col. 1, l. 65–col. 2, l. 7. The '800 patent describes a known issue where each processor in a multi-processor system is allocated a portion of a problem called a "cell" and "to solve the total problem, results of one processor are often required by many adjacent cells because their cells interact at the boundary." *Id.* at col. 2, ll. 26–32. Passing intermediate results around the system to complete the problem requires using "numerous other chips and busses that run at much slower speeds than the microprocessor," diminishing performance. *Id.* at col. 2, ll. 32–38, col. 5, ll. 16–28, Fig. 1 (depicting a conventional multi-processor arrangement). In an adaptive processor-based system, however, "any boundary data that is shared between . . . functional units need never leave a single integrated circuit chip," reducing "data moving around the system" and improving performance. *Id.* at col. 2, ll. 39–49.

Figure 2 of the '800 patent is reproduced below.

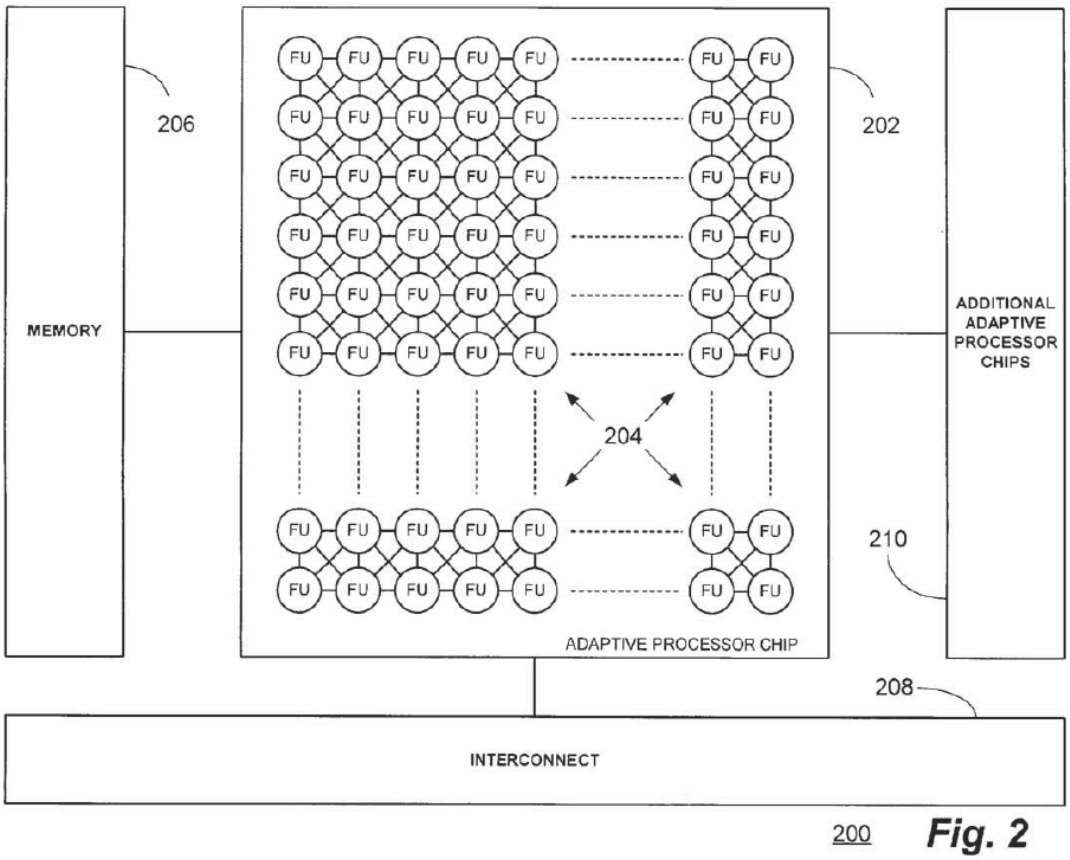

Fig. 2

Figure 2 is "a functional block diagram of an adaptive processor 200 communications path for implementing the technique of the present invention." *Id.* at col. 5, ll. 29–32. Adaptive processor 200 includes adaptive processor chip 202, which is coupled to memory element 206, interconnect 208, and additional adaptive processor chips 210. *Id.* at col. 5, ll. 32–37. Adaptive processor chip 202 includes thousands of functional units ("FU") 204 interconnected by "reconfigurable routing resources" inside adaptive processor chip 202, allowing functional units 204 to "exchange data at much higher data rates and lower latencies than a standard microprocessor." *Id.* at col. 5, ll. 39–45.

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