Asserted Claim of '800 Patent	Exemplary Disclosure of Splash 2
[1A] A method for data processing in a reconfigurable computing system, the reconfigurable computing system comprising at least one reconfigurable processor, the reconfigurable processor comprising a plurality of functional units, said method comprising:	At least under Plaintiff's apparent theories of infringement and interpretations of the clain any of Defendant's accused products satisfy this claim limitation, Buell alone or in combi or more references, discloses: Buell at 11: "The basic building block from which Splash 2 is made is the Xilinx XC4010 mentioned in Chapter 1, the XC4010 contains a 20 × 20 array of Configurable Logic Bloc Buell at 11: "Figure 2.2 illustrates the routing structure of the XC4000 series FPGA. Con are three types of signal routing resources including a single-length interconnect between boxes: "S" in Figure 2.2), a double-length interconnect between alternate switch boxes, ar lines that span the width and height of the chip. The switch boxes contain programmable allow each segment to connect to three others. Configuration of the FPGA is done by loac on-chip RAM; the hardware to do this in Splash 2 is implicit in our description in this cha general architecture and is discussed in greater length in Chapter 6."

Asserted Claim of '800 Patent	Exemplary Disclosure of Splash 2
	Buell at FIG. 2.2:

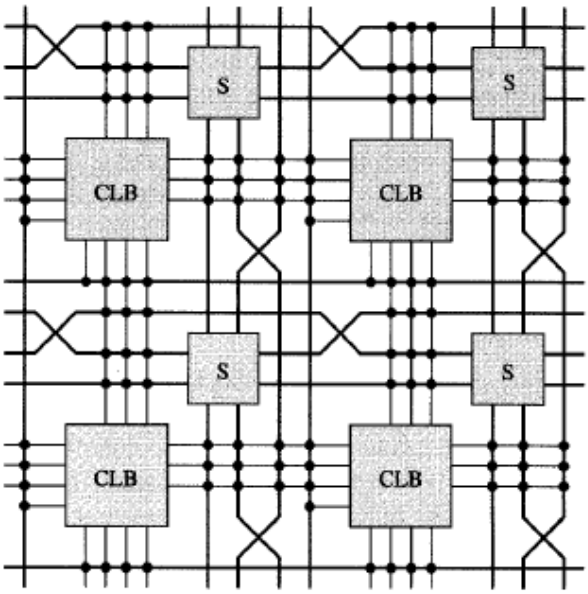


FIGURE 2.2 Xilinx XC4
Structure

Asserted Claim of '800 Patent	Exemplary Disclosure of Splash 2
	Buell at FIG. 2.4

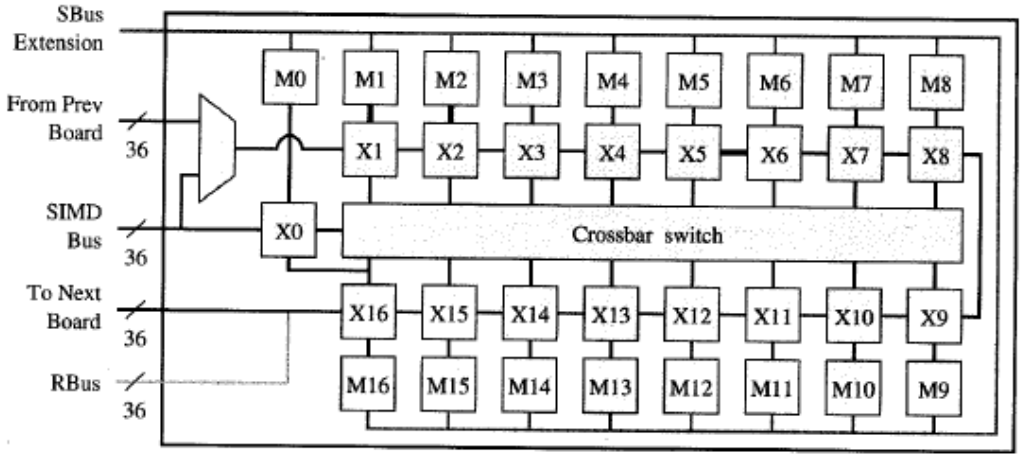
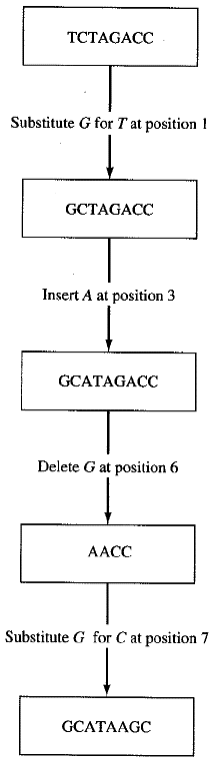


FIGURE 2.4 Array Board Architecture

Buell at 16: "The Splash 2 Array Board is detailed in Figure 2.4. Each Array Board contai
XC4010 FPGA chips as processing elements. Sixteen of these, X1 through X16, form the
and are connected with a 36-bit-wide data path linearly and via a crossbar. To each FPGA
512 Kbytes of memory. Throughout the Splash 2 system, the normal data object has been
32 bits, augmented where possible and sensible with four tag bits. Here, in the connection
memory, we find the one instance in which this design has been compromised. Three 36-b
paths, 18 bits for a memory address, and 32 bits for memory data would have left far too f
total pins for controlling each FPGA. The compromise was to reduce the memory data wi

Asserted Claim of '800 Patent	Exemplary Disclosure of Splash 2
	Buell at 97: "With the onset of the Human Genome Initiative [3] and constant advances in sequencing technology, genetic sequence data are being generated at an ever increasing ra biologists are faced with an influx of new sequences that they would like to classify and st comparing them to existing databases. The analysis of a newly generated sequence typical searching the databases for similar sequences. With the enormous size of the databases, fa needed for comparing sequences [11]. Buell at Figure 8.1:  **FIGURE 8.1** Listing of Operations to Transform $TCTAGACC$ into $GCATAAGC$. Character matches are assumed to have a cost of 0 and are not shown. Assigning a cost of 2 for a substitution, 1 for deletion, and 1 for insertion, the cost of the transformation is 6.

Asserted Claim of '800 Patent	Exemplary Disclosure of Splash 2
	Buell at 97: "ln this chapter, we describe two systolic array architectures for sequence co their implementations on the Splash 2 programmable logic array." Buell at 100: "The locality of reference shown in Figure 8.3 can be exploited to produce s algorithms in which communication is limited to adjacent processors…. The systolic architecture and data flow shown in Figure 8.5 were used in the design of P-N and Lopresti [12], a custom VLSI chip for DNA sequence comparison. Each processing el computes the distances along a particular diagonal of the distance matrix." Buell at 107: "8.3.3 Bidirectional Array For the DNA version of the bidirectional array, each of the 16 array FPGAs (Xl to X16) c making a total of 384 PEs in a one-board Splash 2 system. The protein version packs 64 P board Splash 2 system. Timing results from XDELAY give a theoretical maximum throug million characters per second for the DNA version and 3.5 million characters per second f version."

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