George A. Zimmerman
(424) 398-0273 (residence), (310) 920-3860 (mobile/business)
george@cmephyconsulting.com
1430 9th Street
Manhattan Beach, CA 90266

SUMMARY

High-technology leader with proven combination of technology & business leadership for advanced technologies including development of core technology, licensing, strategy development, standardization, partnerships, strategic alliances, mergers & acquisitions. Recognized expert in broadband communications, physical-layer wireline technology and interference management techniques.

EXPERIENCE

President & Principal Consultant, CME Consulting, Inc. (5/11 - present)
Independent consultant on high-performance communications technology and solutions, specializing in wireline communications. Consulting on next generation technologies, technology development, standards, intellectual property, and business development. Example engagements include:

- Multi-gigabit video/home networking PHY feasibility study
- 25G, 40GBASE-T, and 50GBASE-T design feasibility studies with current and existing cabling
- 25Gbps Ethernet architectures, design feasibility and standardization
- Next Generation structured cabling architecture and applications
- Automotive Gigabit Ethernet PHY architecture design and analysis
- Single pair Ethernet PHY architecture design and analysis (including cabing and powering)
- 4 Pair Power over Ethernet standardization and applications
- Business planning for new market developments in wireline technologies
- Standards strategy and consulting
- Standards guidance, representation and sheparding
- Litigation support services, including testifying expert in patent infringement actions

Consulting Clients include:

- Silicon Image, Inc. (6/11 – 9/11) (a designer and manufacturer of HDMI video chipsets)
- Commscope, Inc. (5/11 – current) (a designer and manufacturer of cabling systems, including LAN cabling)
- Nexans, Inc. (4/12 – 8/12) (a designer and manufacturer of cabling systems, including LAN cabling)
- Aquantia, Inc. (2/13 – current) (a designer and manufacturer of 10Gbps Ethernet chipsets)
- BMW Group (1/17 – current) (a designer and manufacturer of automobiles) through Technica Engineering, and (6/13 – 3/14) through Berner & Mattner AG;
- Linear Technology Corporation (8/14- 3/17) (a designer and manufacturer of high performance analog integrated circuits, including Power over Ethernet controllers)
- Cisco Systems (11/15-current) related to Power over Ethernet regulation in the NFPA.
- Analog Devices (1/17-current), related to IEEE 802.3 standards for single-pair 10Mb/s Ethernet
- APL Group (a consortium including Rockwell Automation, Siemens, Pepperl+Fuchs, Endress-Hauser, focused on industrial networking) (3/17-current), related to the single-pair Ethernet for industrial applications.
- See below under “Litigation Support Experience” for expert witness engagements

Board Member, NBASE-T Alliance (2/2016 – present)
The NBASE-T Alliance (http://www.nbaset.org) focuses on building the ecosystem and consensus required to enable a new 2.5GBASE-T/5GBASE-T Ethernet standard. Working with key stakeholders, the consortium releases specifications that define 2.5 and 5 Gigabit per second (Gbps) speeds at up to 100 meters using the large, installed base of copper cabling in enterprise networks. More than 35 companies have joined the alliance, representing all major facets of enterprise networking infrastructure such as access points, Ethernet switching, and computing, as well as the necessary technologies required to deliver these applications including physical layer ICs (PHYs),

processors, connectors, controllers, switches, FPGAs, Power-over-Ethernet ICs, cables and test equipment. The alliance was founded in 2014 by Aquantia, Cisco, Freescale and Xilinx.

Technical Committee Chair, Ethernet Alliance (12/2015 – present)
The Ethernet Alliance (http://www.ethernetalliance.org) is a global, non-profit, industry consortium of member organizations that are dedicated to the continued success and advancement of Ethernet technologies. Members include system and component vendors, industry experts, and university and government professionals. Ethernet Alliance members work together to take Ethernet standards to the marketplace. They support and originate activities that span from incubation of new Ethernet technologies to interoperability testing to demonstrations to education.

Chief Technical Officer, SolarFlare Communications, Irvine, CA (1/01 – 5/11)
CEO, Solarflare Communications, Irvine, CA (5/02 – 5/03)
Member, Board of Directors, SolarFlare Communications, Irvine, CA (1/01 – 9/04)

- *Technical Leadership:* Technology visionary and founder of next-generation physical-layer communications fabless semiconductor company. Conceived and developed core technology, and led team to develop worlds-first 10GBASE-T 10 Gigabit Ethernet over Cat5e and Cat6 cabling. Developed industry ecosystem and standards for IEEE 802.3an (10GBASE-T) and energy-efficient version (IEEE 802.3az). Responsible for 8 key issued US patents (additional pending). Initiated and led IEEE 802.3an 10GBASE-T standards process to completion, with numerous technical contributions. Demonstrated world's first 10 Gigabit Ethernet link over 50m of Category 5e and Category 6 copper cabling (2004). Led team to develop silicon & demonstrate world's first standard (802.3an) compliant 10GBASE-T link over 100m Cat6a cabling (2006). Led 802.3az "Energy Efficient Ethernet" standards development, contributing key PHY expertise to develop low power idle concepts.
- *Business Leadership:* Created business plan resulting in Series A funding from Foundation Capital and Sequoia Capital (March 2001). Recruited, built and led early development team consisting of systems engineers, digital and analog VLSI designers for a CMOS COT process. Successfully built out initial management team to add VP of Engineering and VP of Sales and led company to initial product. As CEO, raised Series B funding in an oversubscribed up round (October 2002). Recruited replacement interim CEO and later current CEO, Russell Stern in fall 2003.

Member, Board of Directors, Aktino Corporation, Irvine, CA (5/03 – 5/05)
Advisory Board, Aktino Corporation, Irvine, CA (5/05-5/09)
Focused vision and helped prepare initial business plan which was successfully funded. Outside member of board of directors, and advisor to founding team of Telecommunications startup based on multi-wire physical-layer communications technology. As member of board of directors, advised on first 2 years of company's development. Stepped off board after successful Series B round, continued to serve as an advisor on standards, technology and early business issues.

Vice President of Strategic Planning, PairGain Technologies, Tustin, CA (4/99 – 6/00)
Chief Scientist, PairGain Technologies, Tustin, CA (5/95 – 6/00)
Responsible for technology strategy, wireline technology origination and standardization, new business development and technology marketing in $280M/yr (1998) DSL networking systems market leader, including:

- *Technology strategies & new technology developments.* Conception, definition and execution of corporate new technology strategies. Accomplishments include:
  - *ADSL/G.lite*: Authored corporate G.lite/DMT ADSL technology strategy, negotiated technology licenses and managed PairGain's Universal ADSL Working Group (UAWG) and ITU-T G.lite efforts;
  - *HDSL2*: Definition and execution of 3+ year corporate strategy for HDSL2 single-pair T1 technology development and technology transition from 2-pair HDSL. Invented HDSL2-standard OPTIS transmission scheme allowing single-pair transmission of 1.5Mbps data at the same quality as 2-pair HDSL, formed OPTIS coalition and drove ANSI HDSL2 standard (T1.418) incorporating PairGain's technology;
- *Intellectual Property Management & Licensing.* Developed and negotiated technology and patent licensing agreements, including both IPR licenses to PairGain and PairGain licenses of third party IPR. Defined and executed DMT ADSL licensing to Rockwell Semiconductor Systems;
- *Technology Standardization.* Represent PairGain in xDSL standardization activities, personally authoring technical guidelines for spectral compatibility for xDSL systems (T1.417-2000), and driving the development of

HDSL2 technology (T1.418-2000). Contributing member of ITU-T Study Group 15/Q4 (driving G.991 & G. 992, including G.dmt, G.lite and G.shdsl), Universal ADSL Working Group (UAWG) and ANSI-Accredited Committee T1E1.4. Contributing member of Home Phone line Networking Alliance (HomePNA).

- *Corporate strategy & business development.* Key driver in execution of sale of microelectronics group to Globespan technologies for $346 million at closing. Recommended corporate alliance or merger for improving shareholder value & success factors in DSL networking - company merged with ADC for $2.7B in June 2000;
- *Corporate presentations:* frequent speaker at market forums, financial conferences, and technology forums;

Lecturer, California Institute of Technology, Pasadena, CA (4/92-6/94)

Ph.D. Advisor to Michael J. Flanagan following Edward Posner's death, 7/93-6/94
Introduction to Linear Systems: Fall 1993, Winter 1994
Communications Systems Fundamentals: Spring 1992, 1993 and 1994

Member of Technical Staff, Jet Propulsion Laboratory, Pasadena, CA (7/85-5/95)

Management and team leadership in signal processing and communications research and development. Research, development, design and analysis of innovative signal processing algorithms and architectures for digital and mixed-signal systems and ASICs. Advanced development project and proposal leadership and presentation of new systems to internal and external customers.
Successful proposals include:

- Tiny Transponder, an ultra-miniature coherent spacecraft radio with 10 custom ASICs & MMICs ($9M),
- Channelized Signal Processor, a 4 megachannel digital filter bank and programmable processor ($2.2M)
- Sky Survey Signal Processor, a multimegachannel digital spectrum analyzer and CW detector ($12M),
- Spur-reduced DDS research and proof-of-concept ($ 300 k), and High-linearity D/A conversion research and proof-of-concept ($ 250 k).

Work Area Manager: Deep Space Network (DSN) Signal Processing Work Area.
Managed work area for research and development in advanced signal processing for NASA's DSN. Technical and fiscal management of work units within work area. Responsible for schedule and budget planning and performance, on $900 K annual budget reporting to NASA headquarters program manager.

Work Unit Leader: VLSI Applications Work Unit.
Technical, budgetary & schedule team leadership of research and development activities in VLSI algorithms and architectures. Research results include low-complexity, spur-reduced direct digital frequency synthesis, and dynamic element matching D/A converters, and proved in prototype hardware.

Systems Engineer / Architect / Analyst for NASA SETI Sky Survey (aka High Resolution Microwave Survey (HRMS)). Technical, schedule and review responsibility for large system definition including antennas, receivers, digital signal processing hardware and software for searching for extraterrestrial intelligent signals (SETI). Specific duties included program-planning, signal processing algorithm research, design option analysis, performance analysis, functional requirements definition and reviews. Authored and presented successful proposal for the HRMS signal processing hardware, and developed innovative signal-processing approaches to increase performance while reducing cost (> $2 M reduction).

Consulting Engineer on development of a high-speed, constraint length 15 Viterbi decoder. Advised on program planning and evaluation of design and architecture options.

Project Engineer on a Government project at JPL involving mixed signal processing algorithm research and demonstration. Designed digital signal processing boards comprising a digital spectrum analyzer, specified and designed system interfaces, and integrated system (IF-digital-software). Developed, tested and analyzed performance of algorithms in the lab and in the field.

Digital Design Engineer for an Advanced Digital SAR (Synthetic Aperture RADAR) Processor, the primary SAR data processor for the Magellan mission to Venus.

Independent Consultant, self-employed (1989-1995)
Communications and signal processing analysis, simulation and specification. Algorithmic, architectural and bit-level definition and simulation of mixed-signal ASICs and systems; including delta-sigma A/D and D/A converters and filters, error correction coding, audio compression and spread-spectrum communications networks.

Technician, GALIL Motion Control, Mountain View, CA (2/85-6/85)
Built, tested and troubleshot prototype and production digital motion control circuits.

Technical Intern, NCR Corp., Engineering & Manufacturing, San Diego, CA (6/84-9/84)
Improved clock synchronization and distribution for a modular, multi-board parallel processing unit.

Computer Programmer, St. Francis Medical Center, Lynwood, CA (6-9/83, 6-9/81, 6-9/80)
Created and maintained structured COBOL programs.

LITIGATION SUPPORT EXPERIENCE

Expert Engagement: (USITC Successfully Resolved 3/2012)
Type of Matter: Patent Infringement (testifying expert, wrote reports & rebuttals, deposition taken)
Law Firm: Kirkland & Ellis, LLP
Case Name: Cisco Systems, Inc. v. MOSAID Technologies, Inc, USITC Investigation No. 337-TA-778
Services Provided: Testifying Expert for Cisco (respondent)
Continuing Retention in Delaware District Case

Expert Engagement: (Closed, District of Delaware, 8/2013-4/2014)
Type of Matter: Patent Infringement (testifying expert, wrote declaration)
Law Firm: Kirkland & Ellis, LLP
Case Name: Cisco Systems, Inc. v. MOSAID Technologies, Inc, C.A. No. 10-687-GMS
Services Provided: Testifying Expert for Cisco (respondent) (continued district case related to previous ITC matter)

Expert Engagement: (USITC Successfully Resolved 7/2012)
Type of Matter: Patent Infringement (lead expert, wrote reports & rebuttals, deposition taken, settled before trial)
Law Firm: Kirkland & Ellis, LLP; McDermott, Will & Emery, LLP; Crowell & Moring, LLP
Case Name: Cisco, HP, Extreme Networks, Avaya v. Chrimar Systems, Inc, - USITC Investigation No. 337-TA-817
Services Provided: Testifying Expert for Cisco, HP, Extreme Networks, and Avaya (respondents)
Continuing Retention in Northern District of California Case

Expert Engagement: (Active, Northern District of California)
Type of Matter: Patent Infringement (expert, presented tutorial in court – awaiting further scheduling)
Law Firm: Kirkland & Ellis, LLP;
Case Name: Chrimar Systems, Inc. et. al. v. Cisco Systems Inc., et. al., No. C 13-01300 JSW Services Provided:
Testifying Expert for Cisco (respondents), (continued district case related to previous ITC matter)

Expert Engagement: (Active 8/2012-)
Type of Matter: Patent Infringement
Law Firm: Crowell & Moring, LLP, Winston & Strawn, LLP
Case Name: Network-1 Security Solutions, Inc. v. Alcatel-Lucent USA Inc. et. al., Case No. 6:11-cv-00492-LED (E.D. Tex.), Including US Patent and Appeals Board CASE IPR2013-00071
Services Provided: Consulting Expert for Respondents Avaya & Dell, Testifying Expert in IPR matter

Expert Engagement (*Closed, Western District of Texas, Austin Division,3/2013-4/2016*)
Type of Matter: Patent Infringement
Law Firm: Dechert, LLP
Case Names: Intellectual Ventures II LLC v. AT&T, CenturyLink & Windstream), Civil Action No. 1:13-CV-00116-LY (Lead case)
Services Provided: Consulting Expert for Plaintiff Intellectual Ventures,

EDUCATION

California Institute of Technology, Pasadena, CA. MS Electrical Engineering '88, Ph.D. '90.
Doctoral study on interference cancellation for multi-access communications. Information theoretically motivated, developed and analyzed new interference-canceling receivers for use in multi-access FM communications. Tested receivers in simulation on fading channels demonstrating considerable improvement in frequency reuse for analog FM cellular telephony. Extensive patent filed based on thesis. Advisor: Dr. Edward C. Posner.

Stanford University, Palo Alto, CA. BS Electrical Engineering '85.

RESEARCH INTERESTS

- High-performance wireline transmission and applications
- Energy-efficient networking
- Applied signal processing for high-performance and multi-access communications
- Quantization and coding theory in signal processing systems

PATENTS

- U.S. Patent No. 9,883,457, METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION OF A COMMUNICATIONS DEVICE DURING PERIODS IN WHICH THE COMMUNICATIONS DEVICE RECEIVES IDLE FRAMES FROM ANOTHER COMMUNICATIONS DEVICE, G. Zimmerman, March 16, 2015.
- US. Patent No. 8,984,304: ACTIVE IDLE COMMUNICATION SYSTEM, G. Zimmerman, November 12, 2007.
- U.S. Patent No. 8,912,934: SYSTEMS WITH BIAS OFFSET AND GAIN MISMATCH REMOVAL FROM PARALLEL TRANSMITTED SIGNALS, G. Zimmerman and W. Jones, December 16, 2014.
- U.S. Patent No. 8,743,674: FREQUENCY DOMAIN ECHO AND NEXT CANCELLATION, G. Parnaby, G. Zimmerman, C. Pagnanelli, W. Jones, June 3, 2014.
- U.S. Patent No. 8,363,535: FREQUENCY DOMAIN ECHO AND NEXT CANCELLATION, G. Parnaby, G. Zimmerman, C. Pagnanelli, W. Jones, January 29, 2013.
- U.S. Patent No. 8,294,606: SUB-CHANNEL DISTORTION MITIGATION IN PARALLEL DIGITAL SYSTEMS, G. Zimmerman and W. Jones, October 23, 2012.
- U.S. Patent No. 7,808,407: SUB-CHANNEL DISTORTION MITIGATION IN PARALLEL DIGITAL SYSTEMS, G. Zimmerman and W. Jones, October 5, 2010.
- U.S. Patent No. 7,742,386: MULTIPLE CHANNEL INTERFERENCE CANCELLATION, W. Jones and G. Zimmerman, June 22, 2010.
- U.S. Patent No. 7,567,666: METHOD AND APPARATUS FOR CROSSTALK MITIGATION, G. Zimmerman and W. Jones, July 28, 2009.
- U.S. Patent No. 7,352,687: MIXED DOMAIN CANCELLATION, W. Jones, G. Zimmerman and C. Pagnanelli, April 1, 2008.
- U.S. Patent No. 7,257,181: METHOD AND APPARATUS FOR CHANNEL EQUALIZATION, W. Jones and G. Zimmerman, August 14, 2007.
- U.S. Patent No. 7,164,764: METHOD AND APPARATUS FOR PRECODE CROSSTALK MITIGATION, G. Zimmerman and W. Jones, January 16, 2007.
- U.S. Patent No. 7,002,897: MULTIPLE CHANNEL INTERFERENCE CANCELLATION, W. Jones and G. Zimmerman, February 21, 2006.
- U.S. Patent No. 6,912,208: METHOD AND APPARATUS FOR JOINT EQUALIZATION AND CROSSTALK MITIGATION, G. Zimmerman and W. Jones, June 28, 2005..
- U.S. Patent No. 5,459,680: METHOD AND APPARATUS FOR SPUR-REDUCED DIGITAL SINUSOID SYNTHESIS, G. Zimmerman and M. Flanagan, October 17, 1995.
- U.S. Patent No. 5,068,859: LARGE CONSTRAINT LENGTH HIGH SPEED VITERBI DECODER BASED ON A MODULAR HIERARCHICAL DECOMPOSITION OF THE DeBRUIJN GRAPH, by O. Collins, et al, November 26, 1991.

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