DATA SHEET

SCC2691

Universal asynchronous receiver/transmitter (UART)

Product data sheet
Supersedes data of 1998 Sep 04

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Universal asynchronous receiver/transmitter (UART) SCC2691

DESCRIPTION

The Philips Semiconductors SCC2691 Universal Asynchronous Receiver/Transmitter (UART) is a single-chip CMOS-LSI communications device that provides a full-duplex asynchronous receiver/transmitter. It is fabricated with Philips Semiconductors CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of the receiver and transmitter can be selected independently as one of 18 fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

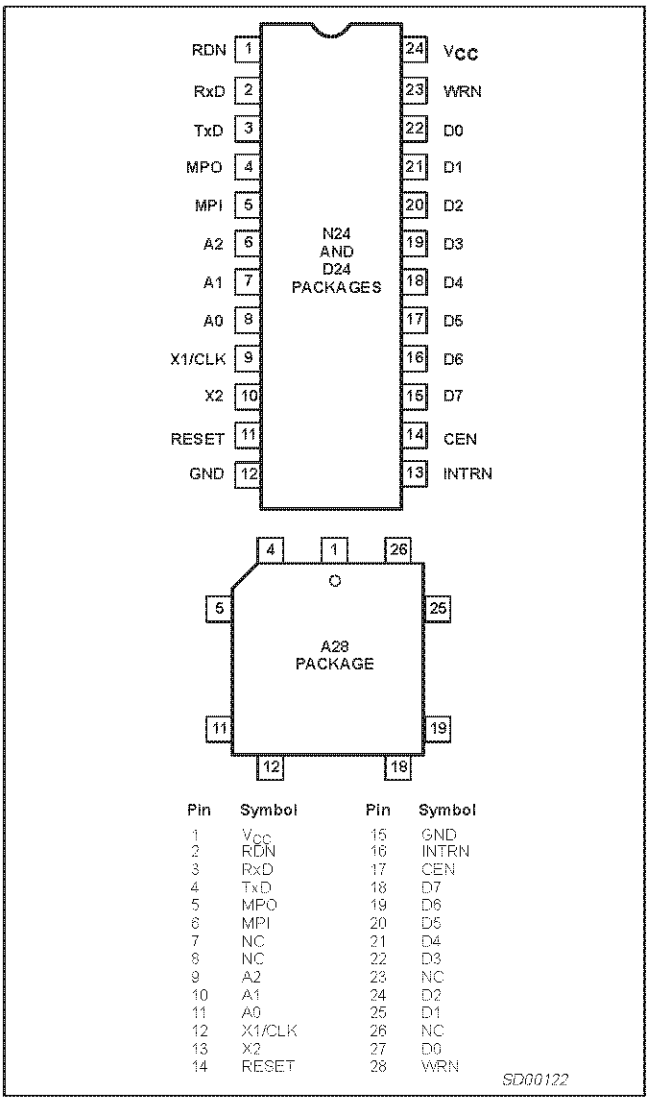
The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes.

The UART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

- Full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Baud rate for the receiver and transmitter selectable from:
  - 22 fixed rates: 50 to 115.2K baud
  - Non-standard rates to 115.2 kb
  - Non-standard user-defined rate derived from programmable timer/ counter
  - External 1X or 16X clock
- Parity, framing, and overrun detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote Loopback
- Multi-function programmable 16-bit counter/timer

PIN CONFIGURATIONS



Pin	Symbol	Pin	Symbol
1	V_{CC}	15	GND
2	RDN	16	INTRN
3	RxD	17	CEN
4	TxD	18	D7
5	MPO	19	D6
6	MPI	20	D5
7	NC	21	D4
8	NC	22	D3
9	A2	23	NC
10	A1	24	D2
11	A0	25	D1
12	X1/CLK	26	NC
13	X2	27	D0
14	RESET	28	WRN

Figure 1. Pin Configurations

- Single interrupt output with seven maskable interrupting conditions
- On-chip crystal oscillator
- Low power mode
- TTL compatible
- Single +5V power supply
- Commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature versions available
- SOL, PLCC and 300 mil wide DIP packages available

ORDERING INFORMATION

PACKAGES	COMMERCIAL	INDUSTRIAL	VERSION
	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	V_{CC} = +5V ±10%, T_A = –40°C to +85°C	
24-Pin Plastic Dual In-Line Package (DIP)	SCC2691AC1N24	SCC2691AE1N24	SOT222–1
28-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCC2691AC1A28	SCC2691AE1A28	SOT261-2
24-Pin Plastic Small Outline Large (SOL) Package	SCC2691AC1D24		SOT137-1

BLOCK DIAGRAM

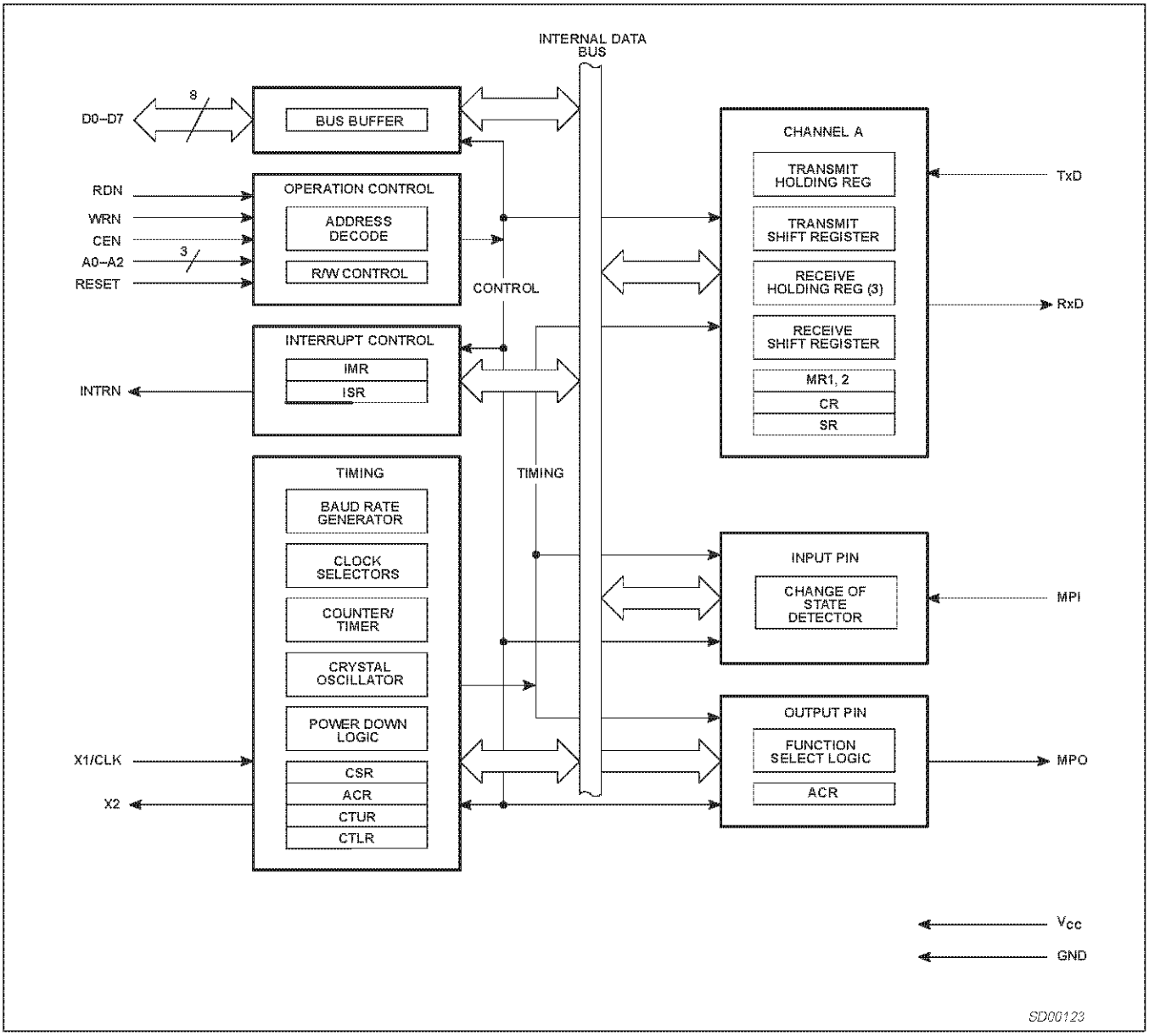


Figure 2. Block Diagram

PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
D0–D7	22–15	27, 25, 24, 22–18	I	**Data Bus:** Active-high 8-bit bidirectional 3-State data bus. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the UART take place over this bus. The direction of the transfer is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is high, the data bus is in the 3-State condition.
CEN	14	17	I	**Chip Enable:** Active-low input. When low, data transfers between the CPU and the UART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A2 inputs. When CEN is high, the UART is effectively isolated from the data bus and D0–D7 are placed in the 3-State condition.
WRN	23	28	I	**Write Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the data bus to be transferred to the register selected by A0–A2. The transfer occurs on the trailing (rising) edge of the signal.
RDN	1	2	I	**Read Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the register selected by A0–A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN.
A0–A2	8–6	11–9	I	**Address Inputs:** Active-high address inputs to select the UART registers for read/write operations.
RESET	11	14	I	**Reset:** Master reset. A high on this pin clears the status register (SR), the interrupt mask register (IMR), and the interrupt status register (ISR), sets the mode register pointer to MR1, and places the receiver and transmitter in the inactive state causing the TxD output to go to the marking (high) state. Clears Test modes.
INTRN	13	16	O	**Interrupt Request:** This active-low output is asserted upon occurrence of one or more of seven maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s). This open-drain output requires a pull-up resistor.
X1/CLK	9	12	I	**Crystal 1:** Crystal connection or an external clock input. A crystal of a clock the appropriate frequency (nominally 3.6864 MHz) must be supplied at all times. For crystal connections see Figure 7, Clock Timing.
X2	10	13	I	**Crystal 2:** Crystal connection. See Figure 7. If a crystal is not used it is best to keep this pin not connected although it is permissible to ground it.
RxD	2	3	I	**Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock.
TxD	3	4	O	**Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (high) condition when the transmitter is idle or disabled and when the UART is operating in local loopback mode. If external transmitter is specified, the data is shifted on the falling edge of the transmitter clock.
MPO	4	5	O	**Multi-Purpose Output:** One of the following functions can be selected for this output pin by programming the auxiliary control register: **RTSN** – Request to send active-low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full. **C/TO** – The counter/timer output. **TxC1X** – The 1X clock for the transmitter. **TxC16X** – The 16X clock for the transmitter. **RxC1X** – The 1X clock for the receiver. **RxC16X** – The 16X clock for the receiver. **TxRDY** – The transmitter holding register empty signal. Active-low output. (Open drain) **RxRDY/FFULL** – The receiver FIFO not empty/full signal. Active-low output. (Open drain)
MPI	5	6	I	**Multi-Purpose Input:** This pin can serve as an input for one of the following functions: **GPI** – General purpose input. The current state of the pin can be determined by reading the ISR. **CTSN** – Clear-to-send active-low input. **CTCLK** – Counter/timer external clock input. **RTCLK** – Receiver and/or transmitter external clock input. This may be a 1X or 16X clock as programmed by CSR[3:0] or CSR[7:4]. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
V_{CC}	24	1	I	**Power Supply:** +5V supply input.
GND	12	15	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to + 7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} ±10%	V
P_D	Power Dissipation	300	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperature, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See Ordering Information table for applicable operating temperature and V_{CC} supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage					
	All except X1/CLK		2			V
	X1/CLK		$0.8V_{CC}$		V_{CC}	V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}[4]	Output high voltage (except open drain outputs)	I_{OH} = –400µA	2.4			V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	–10		10	µA
I_{LL}	Data bus 3-State leakage current	V_O = 0.4 to V_{CC}	–10		10	µA
I_{OD}	Open-drain output leakage current	V_O = 0.4 to V_{CC}	–10		10	µA
I_{XIL}	X1/CLK low input current	V_{IN} = 0, X2 floated	–100	–30	0	µA
I_{XIH}	X1/CLK high input current	V_{IN} = V_{CC}, X2 floated	0	30	100	µA
I_{X2L}	X2 low output current	V_{OUT} = 0, X1/CLK = V_{CC}	–100			µA
I_{X2H}	X2 high output current	V_{OUT} = V_{CC}, X1/CLK = 0V			100	µA
I_{CCA}	Power supply current, active	0°C to +70°C		0.8	2.0	mA
		–40°C to +85°C		1.0	2.5	mA
I_{CCD}	Power down current[5]				500	µA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering Information table for applicable operating temperature and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0V and 3.0V with a transition time of 20ns max. For X1/CLK, this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2V and output voltages of 0.8V and 2V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test condition for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. For power down current levels in the 1µA region see the UART application note.

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