CHIP INTERLEAVING FOR CDMA CELLULAR SYSTEMS

by

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Abstract

We consider the forward link of a direct sequence CDMA cellular system operating in an environment with time varying multi-path fading and introduce a chip interleaving scheme. We study the probability of symbol error for various cases of the interleaving parameters for the cases of a one-path and a two-path Rayleigh fading channel. The chip interleaver output is combined with equal gain combining before the detector. Simulation results for the symbol error probability for each chip interleaving configuration and different interleaving degrees are obtained. Additionally, the effects of hard and soft decision decoding on the performance of the system are considered. The chip interleaving simulation results are compared to the symbol block interleaving used in the IS-95 CDMA cellular system standard. The results show that chip interleaving improves the performance of the CDMA link over that which is based solely on symbol interleaving.

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Chapter 1

Introduction

Wireless communications is one of the fastest growing industries. The subscriptions to wireless communications services are doubling every 20 months, and the number of subscribers has reached 50 million in less than 20 years. This growth rate is due to the development of inexpensive, rapidly deployable wireless systems and mobile units. The viability of wireless communications to provide telephony services is a result of the development of the cellular concept and the associated concept of frequency re-use. The cellular concept constitutes the partitioning of a large area into a number of cells and the allocation of a portion of the total radio spectrum to each of the cells. This frequency allocation results in a pattern of repetition of frequency allocation according to a basic set of cells known as the frequency re-use cluster size. Within each cell, the transmission link from the base station (BS) to the mobile station (MS) is called the forward link, whereas the transmission link from the MS to the BS is called the reverse link. The BS performs functions such as call setup, radio channel assignment, message scheduling on broadcast channels, and power control. The base stations from different cells are connected to a switch known as the mobile telephone switching office (MTSO). The MTSO is the interface between the BS and the wire-line network. A full duplex channel is composed of the forward and reverse links which are separated by a large frequency so as to allow simultaneous transmission. The North America cellular system channel structure contains a 45 MHz bandwidth separation between these two radio links [1].

The three basic multiple access schemes are Frequency Division Multiple Access

(FDMA), Time Division Multiple Access (TDMA), and Code Division Multiple Access (CDMA). They are illustrated in Fig. 1.1. With FDMA the total channel band-

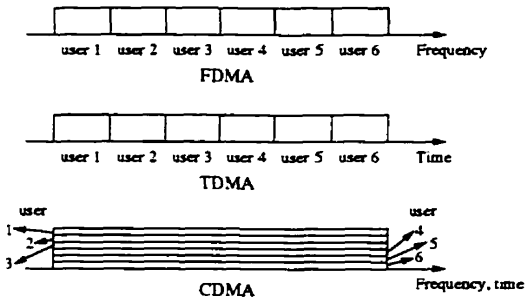


Figure 1.1: Three basic multiple access schemes.

width is divided into a number of smaller frequency bands. Each of these frequency bands is called a radio channel. Each channel is assigned to a specific user, which uses it throughout the call. With TDMA each user transmits a wideband signal occupying the whole system spectrum for a portion of the time [2]. CDMA utilizes the total channel bandwidth for signal transmission. Users are differentiated by their unique code assignment [3]. Several cellular communication standards based on these multiple access schemes have been established. The analog system standard which is known as Advanced Mobile Phone Service (AMPS) is based on FDMA, which is also known as the first generation wireless system. Current digital cellular standards, IS-54 and GSM use a hybrid of FDMA and TDMA. On the other hand, the cellular standard IS-95, was adopted in 1993 [4], is based on CDMA [5].

Following the development of digital cellular standards in 1981, we have witnessed a gradual switch from the analog to the digital systems. One of the major system performance degradations is that due to multipath propagation. The multipath propagation causes the signal to undergo constructive and destructive interference which results in a fading process. Much research has been conducted in devising techniques to mitigate the fading. These techniques include the use of equalizers, diversity schemes, and in particular the rake receiver. In order to combat the fading problem in the CDMA systems, we introduce new techniques based on chip interleaving. These techniques are relatively simple to implement and result in an improvement over the standard technique of symbol interleaving.

1.1 CDMA Systems

The two common spread spectrum techniques are direct sequence spreading (DS) [6][7][8] and frequency hopping (FH). In frequency hopping, the carrier frequency of the transmitted signal is pseudo-randomly changed according to a pseudo-random m-ary sequence. On the other hand, in a DS spread spectrum system, the phase of the carrier is varied according to a binary pseudo-noise (PN) sequence or PN code. In this thesis we consider a DS-SS communication system. The PN codes are generated by linear feedback shift registers. In the IS-95 system the forward channel utilizes a QPSK spreading scheme. Two DS signals are generated, one modulates an in-phase carrier and the other modulates a quadrature carrier. Fig. 1.2 shows the inphase quadrature PN spreading code used in IS-95.

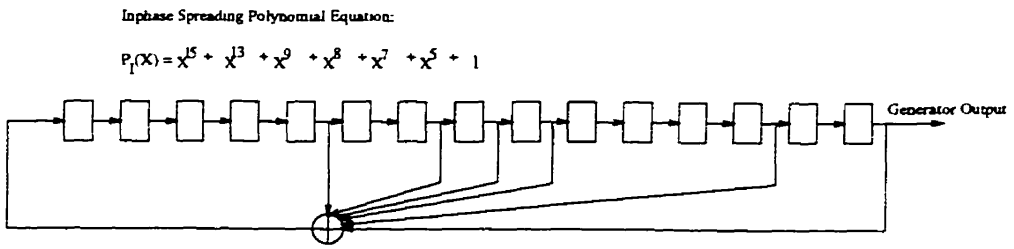


Figure 1.2: Inphase linear shift register for the IS-95 quadrature spreading PN sequence.

In CDMA cellular communications, the different base stations utilize pilot signals which are generated as different phase shifts of a fixed PN code of period equal to 2^{15}. These are referred to as different offsets of the pilot signal. The pilot signal is unmodulated and is transmitted at a higher energy level than the traffic carrying signals. Orthogonal PN codes are used in the forward link in order to reduce multiple access interference. On the other hand, the reverse link uses non-orthogonal codes, because it is difficult to align the transmissions of all the signals in the reverse link. [9]. This thesis concentrates on the forward link of a cellular system. Fig. 1.3 shows the block diagram of a typical direct sequence spread spectrum system.

In the DS scheme the data signal is multiplied by a PN sequence as shown in Fig. 1.3. Each symbol in the PN sequence is called a chip. Fig. 1.4 shows an example

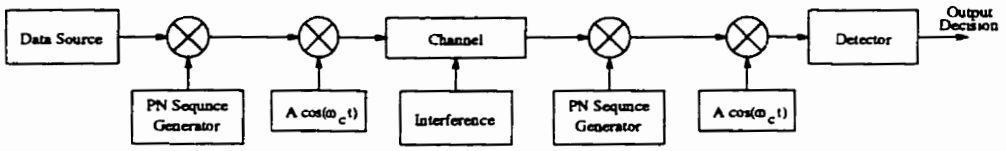


Figure 1.3: Spread spectrum communication.

of a spread data bit by a PN code. The receiver multiplies the received signal with an

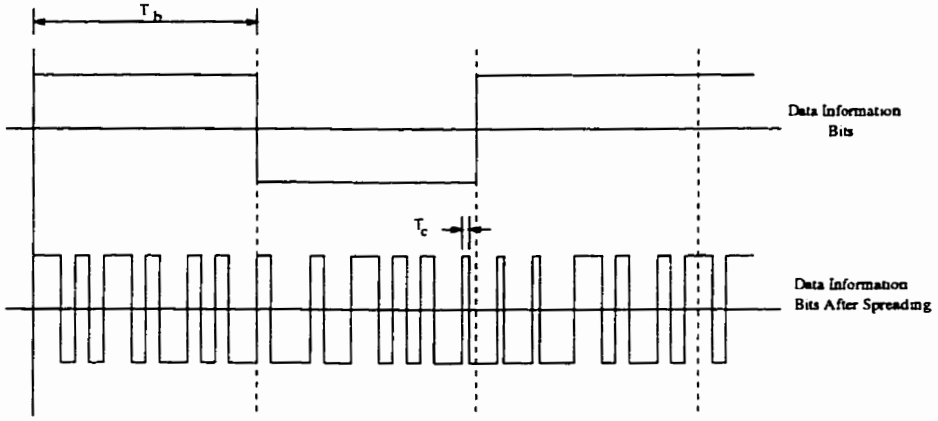


Figure 1.4: Direct-sequence spreading of information bits.

exact copy of the PN sequence with the appropriate phase (in the sequence period) and the result is low-pass filtered. Some of the important issues and features in the CDMA systems are presented in the next subsection.

1.1.1 Important Issues and Features in CDMA

Some of the important features in a CDMA cellular system are the pilot signal, the use of soft hand off, power control, and the Rake receiver. The pilot signal provides many functions to the CDMA systems. Besides using the pilot signal to identify different base stations as mentioned in the last section, it is used to generate a local PN code and carrier phase for coherent demodulation. The use of a pilot signal also facilitates the implementation of soft hand-off. The mobile searches over the different codes phases of the pilot signal, instructs the base station to transmit the signal over

the base stations that give the strongest signal. This type of hand off is sometimes referred to as "make before break" hand off.

The user capacity in the CDMA cellular systems is limited by the multiple access interference, and power control is employed to reduce this interference. The goal is to transmit the smallest possible power level so as to achieve an acceptable signal to noise ratio at the receiver. Reverse link power control attempts to achieve equal power signals which are received from different MS at the BS [10]. The BS sends a command to the MS so that the MS can constantly adjust its transmit power level. This is known as the closed loop power control. Forward link power control is based on the received frame error rate at the MS and the BS adjusts its transmit power to the MS so that the MS receives a signal with sufficient SNR [11].

The Rake receiver also plays an important role in CDMA cellular communications [12]. When the received signal contains multipath components which have a relative delay of at least one chip, the received signal components are resolvable at the receiver. The Rake receiver collects signal energy from the resolvable multipath components. The signal energy can be combined by three different schemes; maximal ratio combining, equal gain combining, and selective combining. The Rake receiver is used both in the forward and reverse links of the IS-95 CDMA cellular systems.

1.1.2 IS-95 Standard

IS-95 is an interim digital cellular standard which adopts the CDMA technology. There are two major areas in this standard: the reverse link and the forward link. The forward link is an important area for system performance improvement since the mobile receiver has a limitation on hardware implementation; we want a small and less power-consuming mobile receiver. Our research focuses on improving the system performance for the forward link of CDMA cellular systems. We use IS-95 as a guideline for our research and simulation parameters. This standard specifies the modulation technique, long PN code generation, orthogonal code, forward link power control, interleaving scheme, and forward error correcting code (FEC). Fig. 1.5 shows the IS-95 forward link transmission block diagram.

The orthogonal code used in the forward link is based on the 64×64 Hadamard matrices. The forward link has up to seven paging channels, one synchronization

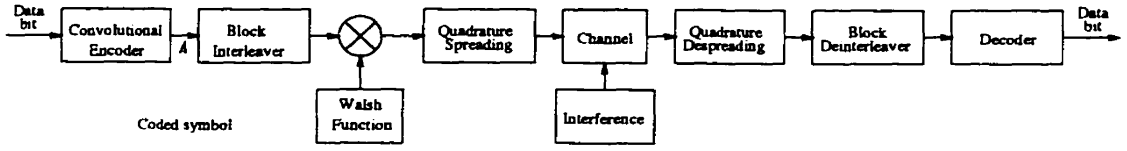


Figure 1.5: The forward link of CDMA cellular standard, IS-95.

channel, one pilot channel, and 54 traffic channels. The all zero sequence in the Hadamard matrix is used for the pilot channel, and the other 63 orthogonal codes are used for the other channels. Only the receiver which has the right orthogonal code can retrieve its information from the received signal [13]. The forward link uses a rate 1/2 convolutional channel encoding. One bit of information is encoded into two symbols. Each speech frame contains 384 symbols which are read into a block interleaving table. The symbols are interleaved for transmission. This has the effect of making the system robust against rapid fading.

At the receiver, the received signal is despread by the same PN code as that used at the transmitter. After coherent demodulation and detection, the decision is read into the deinterleaver so that the received information sequence is rearranged to its original speech sequence. The ability of the deinterleaving process to break up any length of burst error depends on its interleaving degree. The bit error rate performance from the chip interleaving scheme is compared to the above symbol block interleaving. A wireless channel has time varying characteristic. The type of signal distortion caused by the time varying effect is called fading. Before we discuss the objective of chip interleaving, section 1.2 discusses the characteristic of fading channel and burst errors.

1.2 Wireless Channel Characteristics

When a signal is transmitted in a wireless environment, the transmitted signal is subjected to reflection and refraction. Because of this multi-path environment, the received signal's amplitude constitutes a sum of multiple signal components, which sum constructively or destructively at the receiver. This amplitude variation in the received signal is known as signal fading. In addition, the signal is also subject to the

Doppler shift effect due to the movement of the receiver [14]. When the receiver is moving directly towards the transmitter, the received signal will be shifted higher in frequency, whereas if the receiver is moving directly away from the transmitter, the received signal will be shifted lower in frequency. We can express the Doppler shift of the ith received signal as in (1.1),

$$\Delta w_i = w_m \cos\theta_i, \tag{1.1}$$

where w_m is the maximum Doppler shift and θ_i is the arrival angle of ith signal path to the direction of motion of the receiver. The maximum Doppler shift is related to the signal carrier frequency f_c and the velocity of the receiver v, as in (1.2),

$$w_m = \frac{2\pi}{c} v f_c, \tag{1.2}$$

where c is the speed of light. The Doppler shift effect produces the spaced-time correlation function for the received signal, from which we can find the coherence time of the channel. The coherence time is essentially a measure of the rate of channel variation in time. For example a fast changing channel has a small coherence time compared to the data duration. When there are a large number of received signal paths, the received signal can be modeled as a complex-value Gaussian random process. Therefore the characteristic of the received signal's envelope can be modeled as the Rayleigh distribution or Ricean distribution, depending on whether there is a strong specular path [15]. In other cases, the received signal's envelope can be modeled as Nagakami-m distribution. We model our simulation channel as a Rayleigh distributed channel.

The above fading process is known as fast fading. Besides fast fading, the received signal is also subject to a shadowing effect. This is also known as slow fading. Slow fading is caused by the signal blockage between the receiver and transmitter. The most common experience is when a user is under a bridge. One way of solving this problem is to transmit a larger power signal to the receiver. Besides shadowing, path loss also causes signal distortion. Path loss is proportional to the distance between the receiver and transmitter. As the distance between the receiver and the transmitter increases, the transmitted signal strength becomes weaker.

Because of the signal fading effect, a wireless channel is characterized as a bursty error channel. The errors in a bursty error channel tend to occur in clusters. A common error control strategy is using random error correcting codes along with interleavers [16]. Diversity schemes are usually employed to mitigate fading. The following two sections discuss these distortion mitigation techniques.

1.2.1 Signal Fading Mitigation Techniques

Diversity schemes can effectively combat fading. There are three basic diversity schemes; antenna diversity, time diversity, and frequency diversity. Their use is appropriately selected depending on the application. Antenna diversity is achieved by receiving signals from multiple antennas at the receiver. These antennas are separated a few wavelengths apart so that the received signals are uncorrelated at different antennas. Usually the separation is required to be at least tens of wavelengths apart to achieve an independent fading path at the receiver antenna. Therefore antenna diversity is not feasible for the forward link communication, since the mobile receiver is too small to provide enough spacing for the antennas.

With time diversity the same information is transmitted in different time slots such that the probability that all the signals encounter a simultaneous deep fade is very small. When the separation of the time slot is bigger than the coherence time of the channel the errors in the different slots are uncorrelated. With frequency diversity the same information is transmitted in different frequency bands [17]. If the separation between the carriers is greater than the coherence BW of the channel, then we obtain uncorrelated errors in the bits transmitted on the two carriers. Both of these diversity schemes, time and frequency, require additional bandwidth for signal transmission.

1.2.2 Burst Error Mitigation Techniques

A burst-error channel can be modeled with two states; a "good state" and a "bad state" [18]. When the channel is in the good state, the probability that transmission errors occur is very small. When the channel is in the good state it is less likely to shift to the bad state; however once the channel is in a bad state, it is more likely to shift

from the bad state to the good state. The channel shifts to the bad state whenever the transmission medium encounters bad changes, for example a "deep fade". Once the channel is in the bad state, transmission errors are more likely to happen. This type of error is frequently caused by fading effect in the wireless channel. This occurs when the duration of fade is longer than a few symbol times.

The burst of errors is specified by the length of the error cluster and the guard space between these clusters. The guard space is many times longer than the burst length. In order to break up the burst of errors at the receiver, an interleaver is incorporated with the random error correcting code at the transmitter. The interleaver can transform a memory channel into a memoryless channel. Other burst error correcting techniques include the burst-error-correcting code [18]. However interleaving is preferable to the burst-error-correcting code because an interleaver is simple and easy to implement. Moreover an interleaver is suitable for small and power limited receivers.

The purpose of interleaving is to spread the errors throughout the speech frame. The interleaving process scrambles the transmit data bit sequence at the transmitter before modulation. After demodulation at the receiver, the deinterleaver arranges the received bit sequence back to the original sequence before decoding. Therefore any length of burst errors from the channel is broken up before the decoding process. Interleaving can combine with the FEC to mitigate the effect of burst error. There are two types of interleaving schemes: block interleaving and convolutional interleaving [19]. These different interleaving schemes are discussed in Chapter 3. Chip interleaving is a combination of block interleaving and time diversity. The main purpose is to prevent a whole data symbol to undergo deep fade.

1.3 Chip Interleaving

As mentioned previously, in a spread spectrum communication, each data symbol is spread by the PN sequence. Therefore a data symbol contains a number of chips. Chip interleaving can be introduced in the CDMA cellular systems to improve the bit error rate (BER) performance under a fast fading channel. In next two sections, we discuss the research objectives and the overview of the thesis.

1.3.1 Research Objectives

The main purpose of introducing chip interleaving is to prevent the whole data symbol from encountering a deep fade. Chip interleaving can be thought as a combination of interleaving and time diversity. It is "interleaving" because the successive symbols from the speech frame are transmitted far apart from each other through the channel. It is a "time diversity" because the same symbol is divided into many smaller parts and transmitted at different time slots through the channel. If 1/3 of the data symbol parts encounters a deep fade we can recover the signal from the other 2/3 parts of the data symbol.

Chip interleaving does not cause any additional bandwidth expansion in CDMA systems. At the same time we can achieve additional 2-3 dB SNR improvement at 10^{-3} BER. Because of the low complexity in implementation, chip interleaving is preferable to using any high complexity powerful code to gain a few dBs in SNR. The simulation results have shown that chip interleaving improves the SNR significantly over the symbol interleaving performance when the signal is subjected to fast fading. In CDMA cellular systems, this is truly the hidden advantage we have not discovered in the past. Figure 1.6 shows one possibility of chip interleaving implementation.

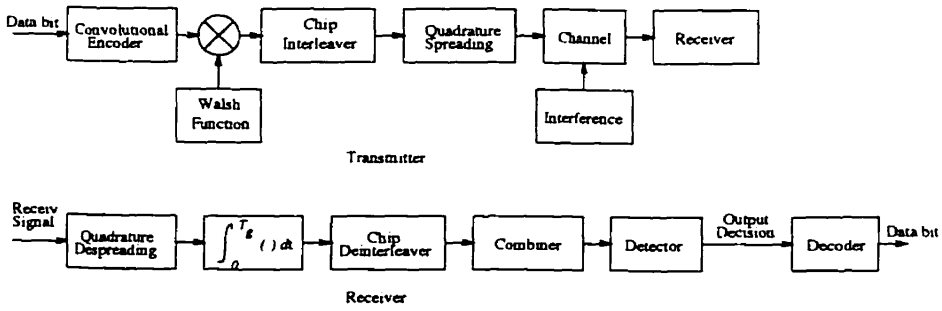


Figure 1.6: Chip interleaving at the transmitter

1.3.2 Thesis Overview

We will compare the effect of chip interleaving in the forward link versus the effect of symbol interleaving under the Rayleigh fading channel model. A comparison of the

results of hard decision decoding and soft decision decoding is made. Chapter 2 looks at the spread spectrum performance under the multipath channel. Chapter 3 explains various interleaving schemes. Chapter 4 presents simulation results for the proposed chip interleaving scheme. Finally Chapter 5 concludes the thesis by presenting the insights resulting from this research and gives directions for future research.

Chapter 2

Direct Sequence Spread Spectrum Signals in Multipath Channels

We begin this chapter by introducing the basic concept and parameters of direct sequence spread spectrum signal (DS-SS) in Section 2.1. Section 2.2 presents the multipath fading phenomenon. Section 2.3 discusses the use of convolutional codes and the Viterbi decoding algorithm. Section 2.4 explains ideal symbol interleaving and discusses its simulation results under a fast fading channel. Finally, Section 2.5 explains ideal chip interleaving and looks at its simulation results.

2.1 Direct Sequence Spread Spectrum Signal

The original purpose of spread spectrum communication is to combat intentional jamming signals [20]. However spread spectrum communication technique has other uses than the anti-jamming use. Other uses include a transmitting signal with a low probability of intercept signal to prevent intruders: suppressing multi-user interference: providing multiple resolvable paths at the receiver to combat fading. Chip interleaving is a technique where the different chips of a data symbol are transmitted through different time slots to combat fast fading.

In DS spreading, each information bit is multiplied by a PN code. After the multiplication, a bit produces a large number of time chips which occupy subintervals of the bit duration. Each of these time subintervals is denoted as T_c, and is called the

chip duration. The multiplication of the message bit stream, $m(t)$, and the spreading waveform, $p(t)$, is shown in (2.1).

$$m(t)P(t). \tag{2.1}$$

The DS spreading waveform is,

$$P(t) = \sum_{i=-\infty}^{\infty} p_i v(t - iT_c). \tag{2.2}$$

where $\{p_i\}$ is a pseudo-noise sequence generated from a linear shift register, and p_i represents a chip. Each of these chips is mapped into a wideband waveform, $v(t)$, which has a duration of T_c. The energy contained in each chip pulse is,

$$\int_0^{T_c} v^2(t)dt = E_c. \tag{2.3}$$

The pseudo-noise sequence has equal probability of being 1 or -1 as in (2.4).

$$p_i = \begin{cases} 1. & \text{with probability } \frac{1}{2} \\ -1. & \text{with probability } \frac{1}{2}. \end{cases} \tag{2.4}$$

The two main types of direct-sequence systems are binary direct-sequence systems and quadriphase direct sequence systems. A quadriphase direct-sequence system is more resistant to the multiple access interference than the binary DS system [21]. Therefore a quadriphase DS system is superior to the binary DS systems. However both types of spreading signals have equal performance in a channel affected by white Gaussian noise. The quadriphase DS spreading modulates the same information onto the inphase and quadrature carrier. Fig.2.1 shows the block diagram of the receiver. The quadriphase DS system is used in IS-95.

In quadriphase spreading, two PN codes are used for the inphase and quadrature phase carrier spreading. The data modulation is a BPSK modulation scheme. Therefore a BPSK signal is spread by the inphase PN signal, $P_I(t)$, and a quadrature phase signal, $P_Q(t)$. The received signal is (2.5),

$$y(t) = \sqrt{S}m(t)P_I(t)\cos(w_c t + \theta) + \sqrt{S}m(t)P_Q(t)\sin(w_c t + \theta), 0 \le t \le T_s. \tag{2.5}$$

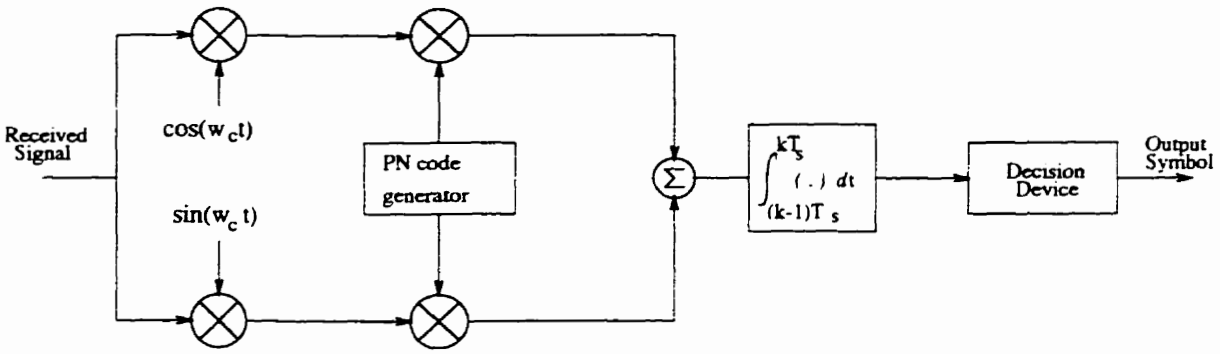


Figure 2.1: Quadriphase direct-sequence receiver.

where w_c is the carrier frequency, θ is the carrier phase shift, and T_s is the symbol duration. S is the average received signal power, is given by,

$$S = \alpha^2. \tag{2.6}$$

where α^2 is the power variations due to fast fading. Since the information bit stream and the chip stream need to be clocked together, the number of chips within a bit interval has to be an integer. The chip rate, W chip/s, is G times larger than the information rate, R b/s. The ratio of W to R is called the processing gain, G.

$$G = \frac{W}{R}. \tag{2.7}$$

We can derive the jamming-to-signal margin J/S from the processing gain, G, as in (2.8).

$$(J/S)dB = 10 \log \frac{G}{(S/N)_{min}}. \tag{2.8}$$

where $(S/N)_{min}$ is the required signal-to-noise ratio for the desired BER. The jamming-to-signal margin indicates the excess received interference over received signal which can be tolerated at the receiver input. The received signal is despread by multiplying it with the inphase and quadrature PN signal at the quadriphase receiver. When a PN sequence signal, $P(t)$, multiplies itself again, the result is unity as in (2.9),

$$P^2(t) = 1. \tag{2.9}$$

The information data can be recovered easily from the spreading signal when synchronization is achieved and despreading is carried out. The synchronization process has two parts; acquisition and tracking [22]. We assume perfect code, phase, and symbol synchronization for our analysis and simulation throughout the thesis. The next section discusses the multipath channel model. Understanding the channel characteristic provides an insight into designing the receiver and diversity scheme effectively to combat the fading problem in the wireless communication channel.

2.2 Fading Multipath Channel

A multipath channel contains a continuum of many signal paths. The received signal's amplitude constitutes a sum of multiple signal components which sum to form the received signal. The variation in the received signal amplitude is mainly due to the relative phase changes of the different multiple signal components. As the number of waveforms becomes larger, we can approximate the sum of the signal waveforms as a Gaussian random variable. Hence the envelope of the signal is modeled as Rayleigh distributed when there is no specular signal path at the receiver. The received signal phase can be modeled as an independent phase and uniformly distributed over $[0, 2\pi]$. We can express the channel low pass time-variant impulse response as, $c(t;\tau)$,

$$c(\tau;t) = \alpha(\tau;t)e^{-j2\pi f_c t}. \tag{2.10}$$

From (2.10), $\alpha(\tau;t)$ denotes the channel attenuation for the multipath component due to the response at time t that was applied at time $t-\tau$. For a discrete multipath fading channel, the channel output can be represented by,

$$y(t) = \sum_{l=-\infty}^{\infty} \alpha_l(t)x((t-\tau);\theta_l(t)) + \mathcal{N}(t), \tag{2.11}$$

where at any time t, the envelope terms are independent Rayleigh random variables and all phase terms are independent and uniformly distributed over $[0, 2\pi]$. The $\mathcal{N}(t)$ in (2.11) is the additive white Gaussian noise with double sided power spectral density $N_0/2$. We assume that the signal's amplitude is constant for a bit interval. Therefore

$\alpha_l(t)$ and $\theta_l(t)$ are constant during a bit duration, T_b. Thus,

$$y(t) = \sum_{l=-\infty}^{\infty} \alpha_l x(t-\tau):\theta_l) + \mathcal{N}(t). \tag{2.12}$$

The above equation assumes an independent Rayleigh distributed fading amplitude and a uniform distributed received signal phase. α_l has a Rayleigh distribution as in (2.13).

$$f_\alpha(\alpha) = \frac{\alpha}{\sigma_\alpha^2} e^{-\frac{\alpha^2}{2\sigma_\alpha^2}}, \alpha \geq 0. \tag{2.13}$$

where the variance of α is σ_α^2. In a practical channel, successive received symbols cannot regarded as independent under a fading environment. The time and frequency correlation functions are used to define the characteristic of the fading channel.

The two main parameters, which are the delay spread and the Doppler spread, tell us about the signal correlation in the time and frequency domain. We approximate the coherence bandwidth BW_c in terms of the delay spread, T_m, as in (2.14).

$$BW_c \approx \frac{1}{T_m}. \tag{2.14}$$

The Doppler spread, B_d, is related to the coherence time $(\Delta t)_c$.

$$(\Delta t)_c \approx \frac{1}{B_d}. \tag{2.15}$$

When the data rate is bigger than the delay spread, as in (2.16),

$$T_b \gg Tm, \tag{2.16}$$

then we can assume that no intersymbol interference exists. In addition, if the data rate is bigger than the coherence time of the channel as in (2.17), then the channel is varying slowly,

$$T_b \gg (\Delta t)_c. \tag{2.17}$$

From the above assumptions, we say that the channel attenuation is constant for at least a data bit time. Finally, since we are dealing with wide band signal transmission,

we assume that,

$$W \gg (\Delta f)_c. \tag{2.18}$$

From (2.18), the channel is said to be a frequency selective fading channel. This allows the multipath signals to be resolvable at the receiver, hence a multiple of independent fading signals are being received [23]. Since we model our channel as a Rayleigh fading channel, then no specular signal is available at the receiver.

2.3 Convolutional Coding

Convolutional coding is used for channel error correcting purposes. It is designed for a memoryless channel, where the errors are statistically independent. We look at some of the parameters for the convolutional code, and the one used in the IS-95. There are several different decoding algorithms for convolutional coding. We concentrate only on the maximum likelihood decoding. In this section we first look at the convolutional code, then we discuss the Viterbi algorithm.

2.3.1 Convolutional Codes

Convolutional code is a linear code. Its encoder contains memory and uses a finite-state shift register to produce coded bits or symbols. The output sequence equation can be expressed either by the generator sequences of the code or the generator matrices. The expression in (2.19) shows the generator sequences for the convolutional code in IS-95.

$$\begin{aligned} \mathbf{g}_0 &= (111101011) \\ \mathbf{g}_1 &= (101110001). \end{aligned} \tag{2.19}$$

The characteristic of the convolutional code is specified by (n, k, m); m is the number of memory in the encoder, k is the number of input bits, and n is the number of encoded output bits. The convolutional code rate is k/n. The constraint length of the convolutional code, K, is $m_{max} + 1$, where m_{max} is the number of memory of the longest shift register. At any instance of time, the output symbols depend not only

on the current input, but also on the $K-1$ previous inputs bits, since each input bit remains in the encoder for up to K time units. The longer the constraint length the more efficient the code on correcting random errors; however it also increases the complexity of the decoding process.

There are n numbers of modulo-2 adder in the encoder. The operation of the convolutional encoder can be expressed by the state diagram. The state of the convolutional code is the contents of the shift register. Therefore for the above convolutional code, there are 2^{m_T} states, where m_T is the total number of memory in the encoder. Fig. 2.2 shows the convolutional encoder which is used in the forward link specified by IS-95. In this case m_T is 8, and there are 256 states. We can find the transfer function of the code from the state diagram. The transfer function allows us to find the distance properties of the code [24], however the computation become impractical as K exceeds 4, then the free distance can be found by computer search. The convolutional code used in IS-95 has maximal minimum free distance of 12 [25].

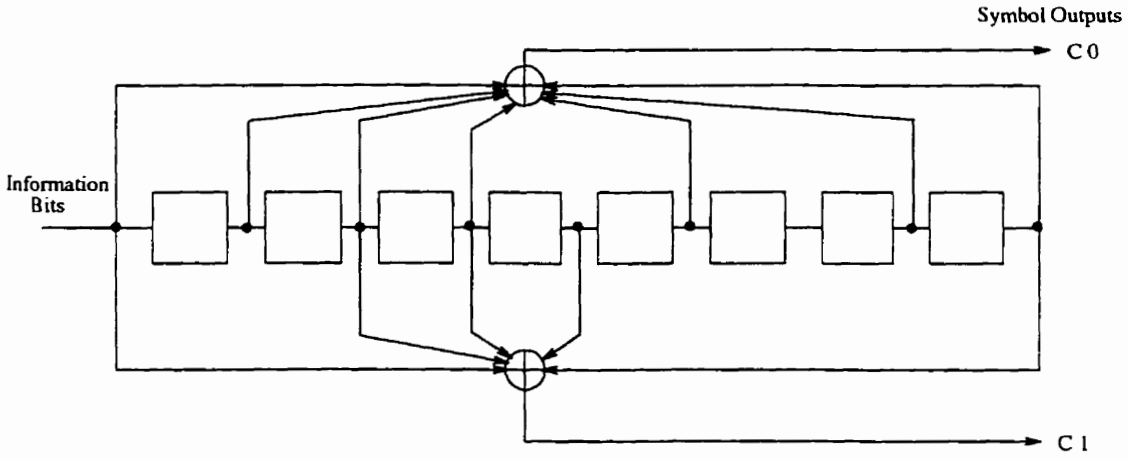


Figure 2.2: A (2,1,8) convolutional encoder.

2.3.2 Viterbi Decoding Algorithm

The Viterbi decoding algorithm for the convolutional code is a maximum likelihood decoding. The state diagram of the convolutional code can be extended in time to become a trellis diagram. The decoding process searches all the possible paths

through the trellis diagram by computing the log likelihood function and recording the survival paths. After finding all the possible paths, the trellis is traced backward to find the most likelihood paths [26].

The branches in the trellis diagram are labeled with the coded symbols and the associate input information bits. Since the received codeword is compared to all the possible codewords labeled at the branches in the trellis diagram, there are $2^{m\tau}$ number of computations at each unit of time. From $t = 1$ to $t = 8$, one branch entering each node (state) and 2^k branches leaving each node in the trellis diagram. After $t = m$, there are also 2^k branches entering each node. For the above convolutional code, $k = 1$, so there are 2 branches leaving and entering each node after $t = 8$. Given an information sequence of length L with an input sequence of kL bits, the trellis diagram must have $L + m$ stages in time. For the 184 information bits, and $k = 1$, the trellis diagram has $184 + 8$ stages in time. There are 2^{kL} distinct paths through the trellis, and at each stage there are $2^{m\tau}$ metrics need to be computed. Computation at each stage increases exponentially with k and K. The literature has showed that, any convolutional encoder with memory greater than 9 has little increase in performance, but a major increase in complexity [25].

The maximum likelihood decoder selects the received code word according to the estimates of the decoding sequence which maximized the probability $p(\mathbf{r}|\mathbf{y}')$. The received word is $\mathbf{r}$, and $\mathbf{y}'$ is the maximum likelihood estimated code word of the transmitted sequence. $\mathbf{r}$ and $\mathbf{y}'$ are shown in (2.20),

$$\begin{aligned} \mathbf{r} &= (r_0^0, r_0^1, r_0^2, \ldots, r_0^{(n-1)}, r_1^0, r_1^1, r_1^2, \ldots, r_1^{(n-1)}, \ldots r_{L+m-1}^{(n-1)}) \\ \mathbf{y}' &= (y_0'^0, y_0'^1, y_0'^2, \ldots, y_0'^{(n-1)}, y_1'^0, y_1'^1, y_1'^2, \ldots, y_1'^{(n-1)}, \ldots y_{L+m-1}'^{(n-1)}) \end{aligned} \tag{2.20}$$

r_i^n denotes the received ith bit and nth symbol, and y_i' denotes the estimated decoder output bit. If we assume a statistically independent channel, then $p(\mathbf{r}|\mathbf{y}')$ is the product of each individual $p(r_i|y_i')$. In order to make the computation simple so that only addition or subtraction is used, we can take the logarithm of $p(\mathbf{r}|\mathbf{y}')$. Since logarithms are monotonically increasing, when we estimate the maximum logarithm of the probability, this is also the maximum estimation of the probability. This

Code Symbol	Quantization Level							
	0	1	2	3	4	5	6	7
0	-0.812	-0.842	-0.869	-0.896	-0.921	-0.947	-0.971	-0.100
1	-0.100	-0.971	-0.947	-0.921	-0.896	-0.869	-0.842	-0.812

Table 2.1: Metric table for an 8 levels quantization.

Code Symbol	Quantization Level							
	0	1	2	3	4	5	6	7
0	7	6	5	4	3	2	1	0
1	0	1	2	3	4	5	6	7

Table 2.2: Integer Metric table for an 8 levels quantization.

log likelihood function is the metric for path $\mathbf{y}'$. For hardware implementation and simulation purposes, the bit metric is expressed as follows,

$$M(r_i|y_i') = a[\log p(r_i|y_i') + b], \tag{2.21}$$

where a is any positive real number, and b is any real number. The partial path metric for the current node is the sum of current and previous bit metric. The surviving paths are those paths with the minimum partial path metric. When hard decision decoding is performed, the Hamming distance property is used. On the other hand, the soft decision decoding uses the Euclidean distance measure. The soft decision decoding process is basically the same as the hard decision decoding, except that the bit metric is quantized into multi-levels. Table 2.1 shows the logarithm to the base 10 of the bit metric. The integer metric table for the 8-level soft decision decoding is shown in table 2.2.

2.4 Coding and Ideal Symbol Interleaving for DS/SS Signal

As mentioned in section 2.2, fading causes burst errors which are due to the strongly correlated received fading signal components. This section presents the simulation

results on the symbol block interleaving for the forward link of the DS-CDMA systems. We simulate the bit error rate performance under a Rayleigh fading channel. The ideal interleaving causes the successive deinterleaver output symbols to be uncorrelated. The errors are statistically independent at the ideal symbol block interleaver output. The received signal components are assumed to undergo statistically independent fading. The received signal is corrupted by the additive white Gaussian noise (AWGN) with power spectral density $N_0/2$. The signal is received synchronously. Coherent demodulation is assisted by the pilot signal. At the BS, data is BPSK modulated and QPSK spreading.

In order to use the convolutional code for channel error correction in a fading channel, interleaving is implemented after the channel encoder. Due to intractable analysis of the bit error rate performance for the interleaving process in a time correlated fading channel, all performances are evaluated from simulation. Fig. 2.3 shows three different simulation results; no interleaving, IS-95 symbol block interleaving, and ideal symbol block interleaving.

The channel coding employs a convolution code from the one specified in the IS-95. The time correlated fading channel is generated according to Jake's model [27]. The maximum Doppler frequency for the simulation is 60 Hz. The symbol block interleaving from the IS-95 is explained in Chapter 3, section 3.3. The statistically independent fading amplitude is generated from an independent Rayleigh random number generator. Fig. 2.3 shows that at 10^{-3} BER, the ideal symbol block interleaving is 11 dB better than the no interleaving case. On the other hand, the IS-95 symbol block interleaving improves 5 dB in SNR from the no interleaving case at 10^{-3} BER. The ideal interleaving suggests that if we can spread the burst error further apart, we can achieve a better SNR.

Figure 2.4 shows the results for soft decision decoding and hard decision decoding in a symbol block interleaving case. The soft decision decoding symbol block interleaving is 3.5dB better than the hard decision decoding. In Chapter 4 we see how chip interleaving can achieve close to the ideal symbol block interleaving case.

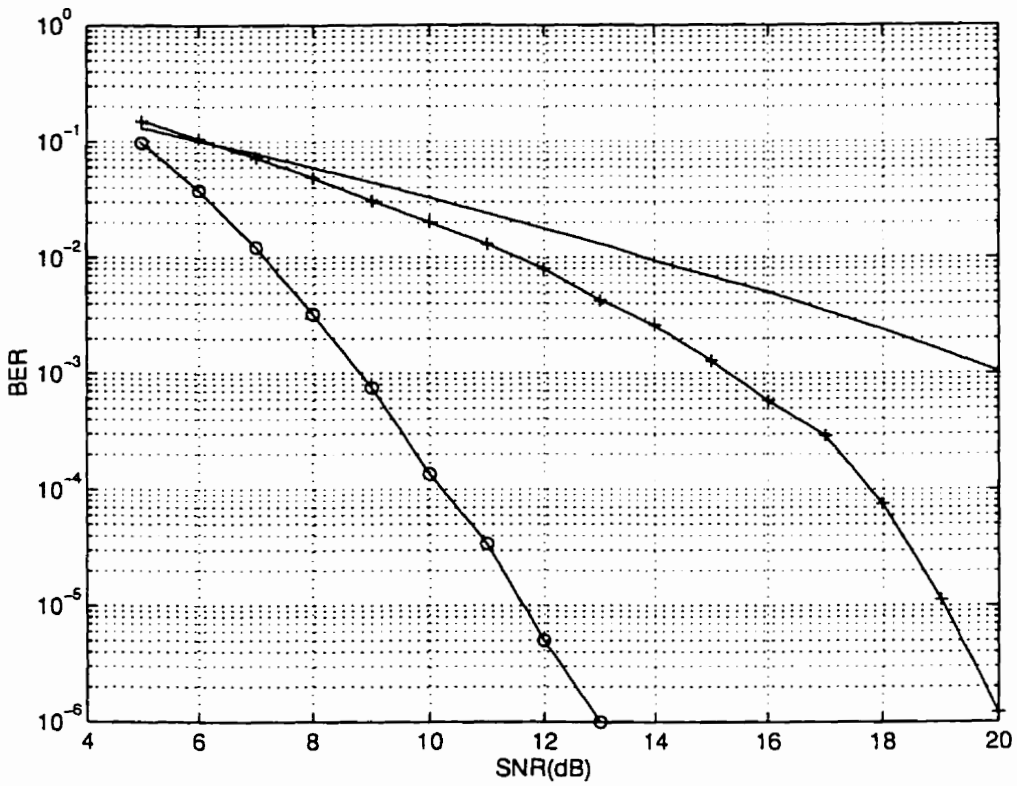


Figure 2.3: Simulation results for ideal symbol block interleaving, IS-95 symbol block interleaving, and no interleaving for hard decision decoding under one-path Rayleigh fading channel. Maximum Doppler frequency is 60 Hz.
Legend: Ideal symbol block interleaving ('o'), IS-95 symbol block interleaving ('+'), no symbol interleaving (solid line).

2.5 Ideal Chip Interleaving Performance

Chip interleaving divides a data symbol into a number of smaller parts. These parts are sent through the channel at different time slots by the interleaving process. Each of these divided parts is called a group because each part contains a group of chips. At the ideal chip interleaver output, the transmitted groups of chips fade independently. For a symbol which is divided into N groups, these N groups are transmitted in N well separated time slots. The nth group is transmitted in nth time slot. Errors caused by the fading become statistically independent after the ideal chip interleaving process. The duration of each group is denoted as T_g. The nth time slot attenuation is

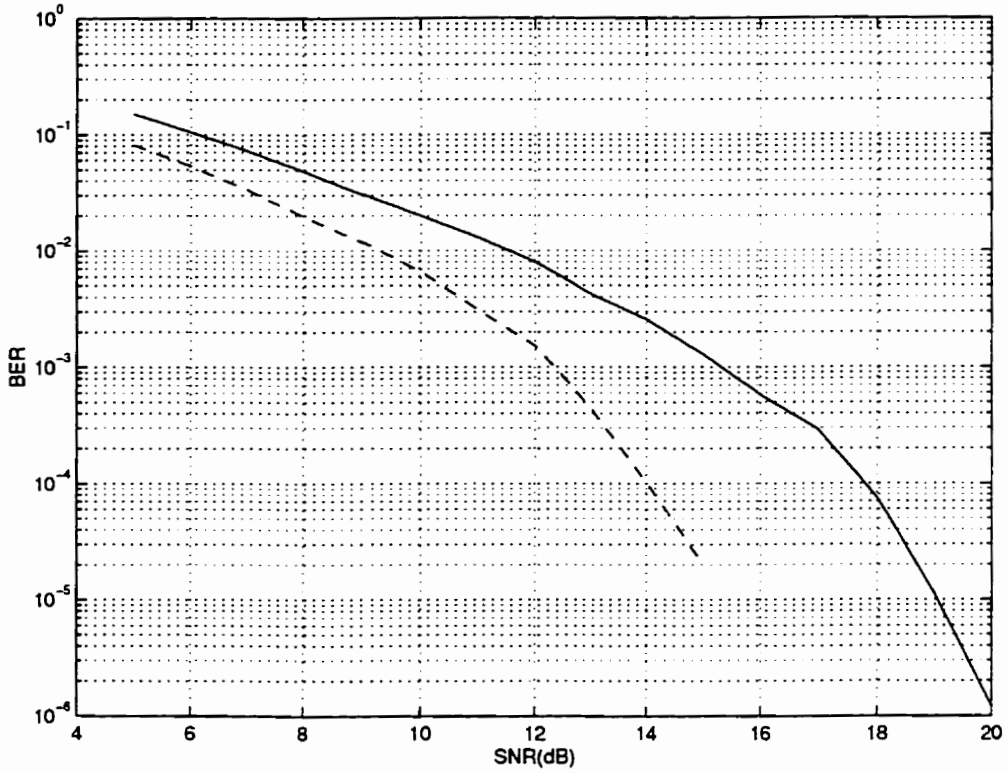


Figure 2.4: Simulation results of IS-95 symbol block interleaving for hard and soft decision decoding. Maximum Doppler frequency is 60 Hz.
Legend: Soft decision decoding (dash line), hard decision decoding (solid line).

α_n, which has a Rayleigh distribution characteristic. The received quaternary DS/SS signal for the nth time slot is,

$$r_n(t) = \sqrt{S_n} m(t) P_I(t) \cos(w_c t + \theta) + \sqrt{S_n} m(t) P_Q(t) \sin(w_c t + \theta) + \mathcal{N}(t). \quad (2.22)$$

S_n is the average received signal power; $S_n = \alpha_n^2$. $P_I(t)$ and $P_Q(t)$ are the in-phase and quadrature phase spreading signal respectively, and $m(t)$ is the message signal. We assume a perfect forward link power control. The coding rate for each data bit is R. The bit energy is denoted as E_b. Let E_s denotes the signal energy for each data symbol. Then we have $E_b = E_s/R$. E_g is the signal energy for the nth symbol part. The relationship between the energy contains in each group of chips, bit energy,

coding rate is (2.23),

$$E_g = \frac{E_b}{N} R = \frac{RG}{N} E_c. \tag{2.23}$$

Therefore the number of chips, G_g, in each group is

$$G_g = \frac{RG}{N}. \tag{2.24}$$

The energy contains in a group of chips is E_g,

$$E_g = \frac{E_s}{N}. \tag{2.25}$$

At the receiver, the nth received signal is multiplied by a replica of the in-phase and quadrature phase spreading sequence. The correlator input is integrated over a group interval, T_g as in (2.26),

$$y_n = \int_0^{T_g} 2r_n(t)[P_I(t)\cos(w_c t + \theta) + P_Q(t)\sin(w_c t + \theta)]dt. \tag{2.26}$$

The correlator output for the nth received signal is,

$$y_n = \pm 2\sqrt{S_n} T_g + Z_1, \tag{2.27}$$

where Z_1 is the noise term. The variance of Z_1 is denoted as $Var(Z_1)$, which is the sum of the variances from the inphase and quadrature phase branches. The double-sided power spectra density of the AWGN is $N_0/2$. Using the result from [21], $Var(Z_1)$ is (2.28),

$$Var(Z_1) = 2N_0 T_g \tag{2.28}$$

The correlator outputs are fed into the chip deinterleaver. The deinterleaver arranges the received groups of chips so that the groups from the same symbol data can be combined. The combiner combines energy from the N groups of chips as in (2.29),

$$U = \sum_{n=1}^{N} a_n y_n, \tag{2.29}$$

where a_n is the weighting factor for the nth signal input. A maximal ratio combining is done by choosing $a_n = \frac{U_n}{Var(Z_1)}$, where we assume all the additive noise powers are

equal. The estimation of the channel state information a_n is extremely difficult for such a short duration of time. Therefore all the simulations use equal gain combining techniques, where $a_n = 1$. The combined energy is sent to the decision detector. After the decision is made, the Viterbi decoding algorithm is carried out for error correction.

As we can see from the simulation result in Fig. 2.5, the chip interleaving is superior to the symbol interleaving, because of the N additional diversity we obtained from the chip interleaving. Chapter 4 shows results on BER performance for chip interleavers where the chip interleaving degrees are limited by the speech frame length. Fig. 2.5 shows the ideal cases for the IS-95 symbol block interleaving and the maximum separation distributed chip interleaving schemes. The five different interleaving configurations are classified by the number of chips contained in each group. They are the 16-chip group, 8-chip group, 4-chip group, 2-chip group, and 1-chip group. For instance, the 16-chip group configuration represents 16 chips in a group. The total number of chips within a symbol is 64 chips, therefore, a 16-chip group configuration has 4 groups within a symbol duration, which is expressed as a 4 16-chip groups per symbol configuration. The five chip interleaving configurations perform at least 6 dB better than the ideal symbol interleaving case. As a result, chip interleaving can improve the SNR significantly from the symbol block interleaving for the bit error rate performance when the signal is subjected to fast fading.

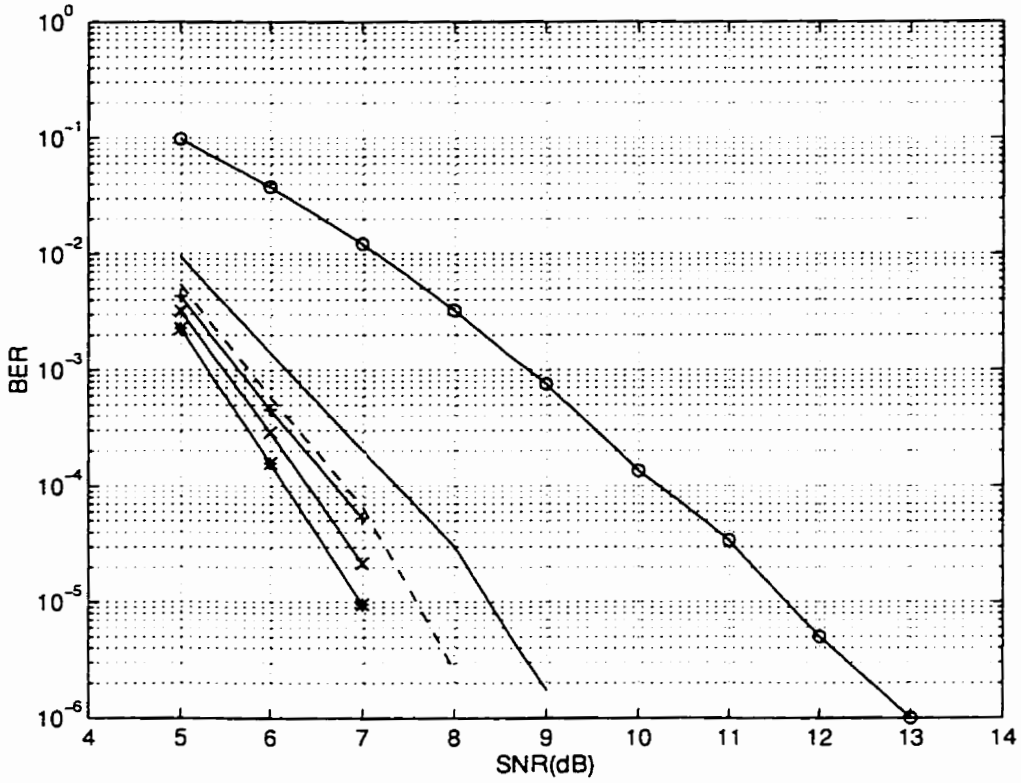


Figure 2.5: Simulation results for ideal chip interleaving and ideal symbol block interleaving.

Legend: Ideal symbol block interleaving('o'), 16-chip group(solid line), 8-chip group(dash line), 4-chip group('+'), 2-chip group('×'), 1-chip group('∗').

Chapter 3

Interleaving Scheme

The interleaving process can transform a bursty error channel into a statistically independent error channel. Time diversity is a form of interleaving which is commonly used in digital wireless communication systems to combat fading. Section 3.1 discusses time diversity and interleaving. Section 3.2 explains convolutional interleaving. This is followed by a block interleaving discussion in section 3.3. Finally, section 3.4 introduces chip interleaving.

3.1 Time Diversity and Interleaving

Time diversity is a scheme whereby the same information signal is sent at different time slots through the channel. When two time slots that contain the same information signal are separated by a time greater than the coherence time, $(\Delta t)_c$, of the channel, the signals from these two separate transmissions fade independently. As a result, the signals from different time slots are uncorrelated with each other. This is an attempt to break up the cluster of errors.

Interleaving is also an effective method to combat the burst error. Instead of sending the same information signals several times over the channel, the information bit sequence is interleaved at the transmitter so that after deinterleaving at the receiver, the transmission errors have minimum correlation. This can be achieved by separating the transmission of two successive information bits in the time domain by no less than $(\Delta t)_c$. Interleaving does not require additional bandwidth. It is easy to

incorporate into a communication system so that a random error correcting code can be used.

Time diversity and interleaving can be combined in the CDMA cellular systems without adding a major modification to the existing systems. The resultant scheme is chip interleaving. It can efficiently mitigate fast fading. Chip interleaving improves the bit error rate performance when it is compared to the conventional block symbol interleaving. There are two types of interleaving: convolutional and block interleaving. Before we look at chip interleaving, we first discuss convolutional and block interleaving.

3.2 Symbol Convolutional Interleaving

Symbol convolutional interleaving can be further classified into two different types: conventional symbol convolutional interleaving and embedded symbol convolutional interleaving. A conventional symbol convolutional interleaving has an interleaver placed between a channel encoder and a modulator at the transmitter. The deinterleaver is placed between a demodulator and a channel decoder at the receiver [28]. A communication system using the block codes or convolutional codes employ the conventional convolutional interleaving schemes. An embedded symbol convolutional interleaver is one in which the interleaver and deinterleaver are combined with the encoder and decoder respectively. Therefore the embedded symbol convolutional interleaver and deinterleaver is employed by a system which uses the convolutional codes.

3.2.1 Conventional Symbol Convolutional Interleaver

The conventional symbol convolutional interleaver and deinterleaver have J stages of shift registers and $J+1$ delay lines. The number of shift registers at one particular delay line is always one register less than the next delay line in the interleaver, and one more than the next delay line in the deinterleaver. The $J+1$ delay lines of the conventional symbol convolutional interleaver and deinterleaver are shown in Fig. 3.1 and Fig. 3.2 respectively. The D in the figures is the shift register or the delay element.

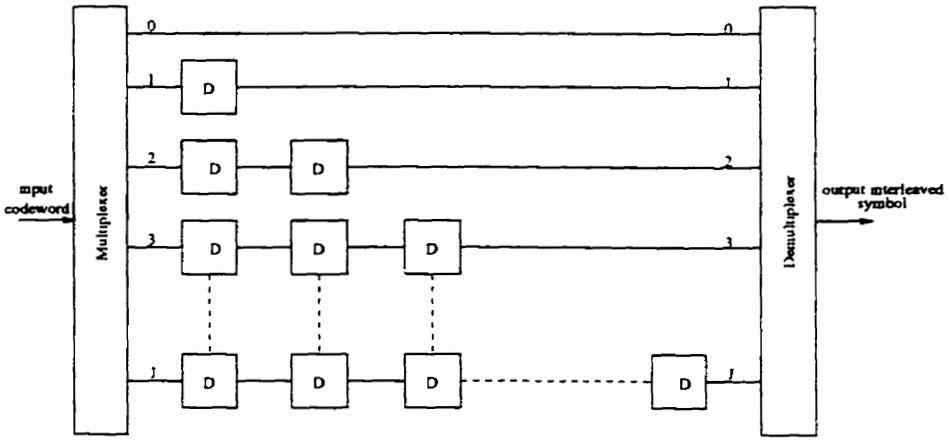


Figure 3.1: Conventional symbol convolutional interleaver.

The multiplexer and demultiplexer switch between the delay lines at each clock time simultaneously. The input and output symbols are read from delay line 0 to delay line J at each clock time and the process repeats till the end of a speech frame. While a symbol is read into the shift register from the left, every stored symbol in the delay elements is shifted to the right to the next delay element or shifted out if it is at the last delay element. Each delay element either can store one symbol or more than one symbol depending on the types of error correcting code and the interleaving degree needed in the communication systems. Two successive interleaver input symbols are separated by λ symbols apart at the interleaver output. λ is defined as the symbol interleaving degree. At the output of the interleaver, the successive symbol for a codeword will be separated by JD number of symbols. If the code word has an error correcting capability of t, then it can correct any burst error with a burst length less than $[(JD+1)(t-1)+1]$ [24].

Fig. 3.3 shows an example of the conventional symbol convolutional interleaving. There are three delay lines and three delay elements in this interleaver. Each delay element stores one symbol, S. The interleaver is initialized with zeros. This interleaver has an interleaving degree of $mD = 3$. The example shows that S_4 and S_5 are separated by three symbols at the output of the interleaver. The conventional symbol convolutional interleaving is suitable for a long constraint length convolutional code. However, the embedded symbol convolutional interleaver is easier to implement in a

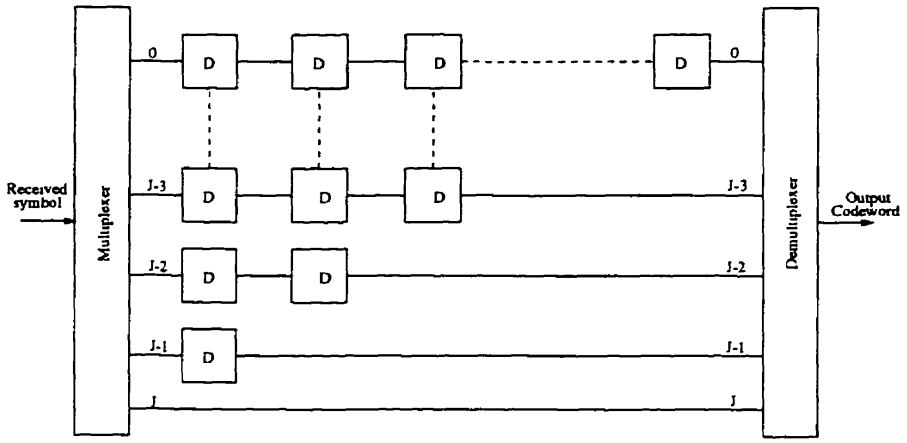


Figure 3.2: Conventional symbol convolutional deinterleaver.

communication system which uses a short constraint length convolutional code.

3.2.2 Embedded Symbol Convolutional Interleaver

Fig. 3.4 and Fig. 3.5 show the block diagram for the embedded symbol convolutional interleaver and deinterleaver. We need to insert λ extra delay elements for each shift register at the encoder so that the output symbols are separated by λ symbols. This scheme saves the memory storage and provides greater interleaving degree with less delay elements for a certain short constraint length convolutional code.

Fig. 3.4 and Fig. 3.5 show that the encoder is replaced by λ extra delay elements per original encoder shift register. The bigger the interleaving degree the greater the number of the delay elements needing to be replaced at the encoder. Therefore for a m memory convolutional code, the total shift registers at the encoder is λnm. In addition the interleaver needs $(\lambda-1)(n-1)/2$ delay elements. So a total of $(\lambda nm + (\lambda-1)(n-1)/2)$ unit elements are needed. As the constraint length of the encoder increases, the total delay elements are increasing in multiples of m, and the complexity of the embedded convolutional interleaving also increases and becomes difficult to implement. As a result, either a conventional convolutional interleaver or block interleaver is suitable for a long constraint length convolutional code. The difference between the convolutional interleaver and block interleaver is that the con-

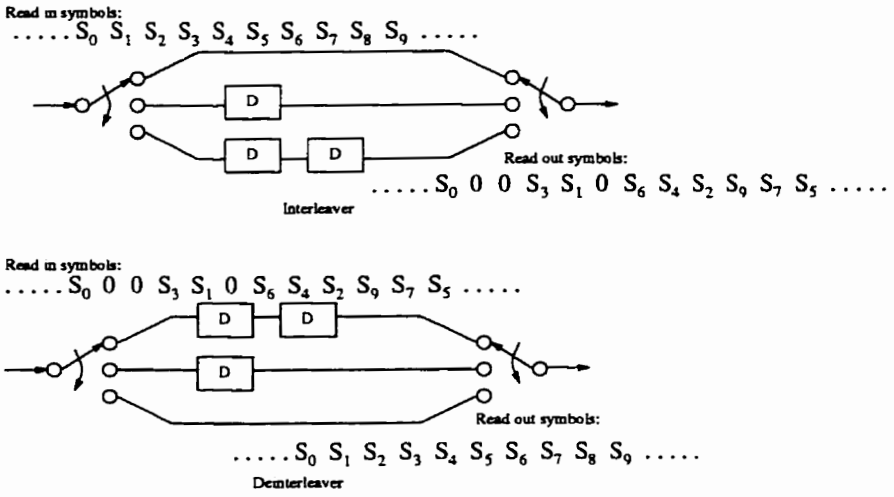


Figure 3.3: A conventional symbol convolutional interleaving (m=3, D=1 symbol).

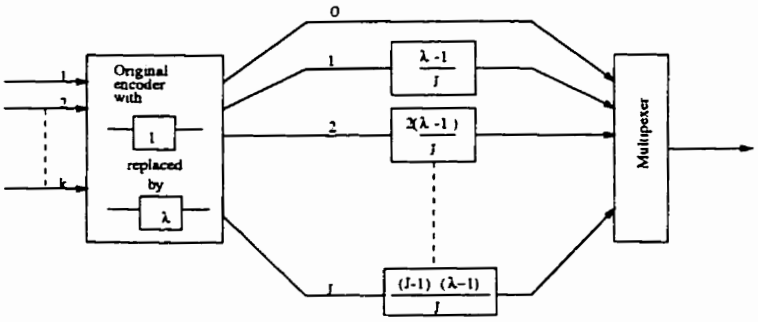


Figure 3.4: Embedded symbol convolutional interleaver.

volutional interleaver does not need a large memory to store symbols. On the other hand, block interleaving is simpler to implement than the convolutional interleaving scheme.

3.3 Symbol Block Interleaving

A block interleaver consists of a R rows by C columns array as shown in Fig. 3.6. The symbols can be read into the interleaver either column by column, or row by row. If the symbols are read in column by column, then they are read out row by

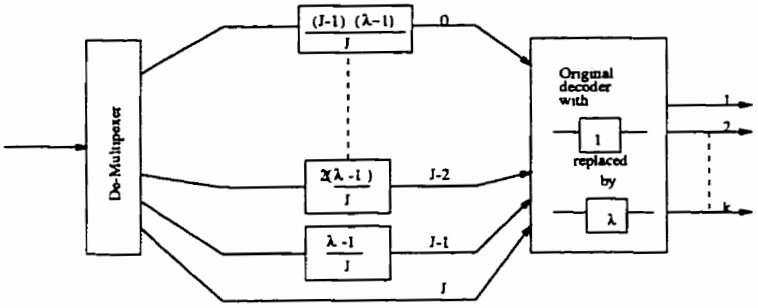


Figure 3.5: Embedded symbol convolutional deinterleaver.

row, and the interleaving degree is $C-1$. However if the symbols are read in row by row, then the symbols are read out column by column, and the interleaving degree is $R-1$. In both cases, the interleaving degree, λ, is defined in term of the number of symbols, which is similar to the convolutional interleaving scheme. The symbol block

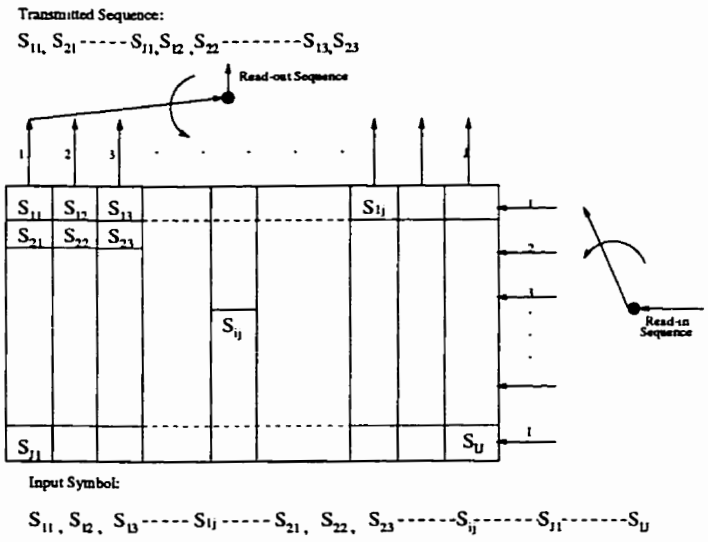


Figure 3.6: Symbol block interleaving scheme

interleaving for our simulation is the one that reads in the symbols row by row, and reads out the symbols column by column as shown in Fig. 3.6.

For a linear block correcting code, the length of the row usually corresponds to the length of the code word. On the other hand, the numbers of rows chosen for

the convolutional code is arbitrary, and it is determined from the interleaving degree needed to combat burst errors. Therefore if the correction capability of the code is t, the $R \times C$ interleaver can correct any burst length greater than $(Rt+1)$. For example a ten rows by six columns interleaver has an interleaving degree, $\lambda = 10 - 1 = 9$. Therefore any successive symbols at the interleaver input are nine symbols apart at the interleaver output. Fig. 3.7 shows an example of the input and output sequence for the 10×6 block interleaver. If the duration of fade is greater than the interleaving degree, the successive deinterleaver output symbols are affected by the same fade. The example in Fig. 3.7 shows that six successive symbols are being affected by the fade. If no interleaving is employed, then the random error correcting code is not able to correct such a long sequence of errors. However when the interleaving is employed, these burst errors are separated by C number of symbols, and they become isolated errors throughout the speech frame. Hence, interleaving minimizes the correlation among the errors.

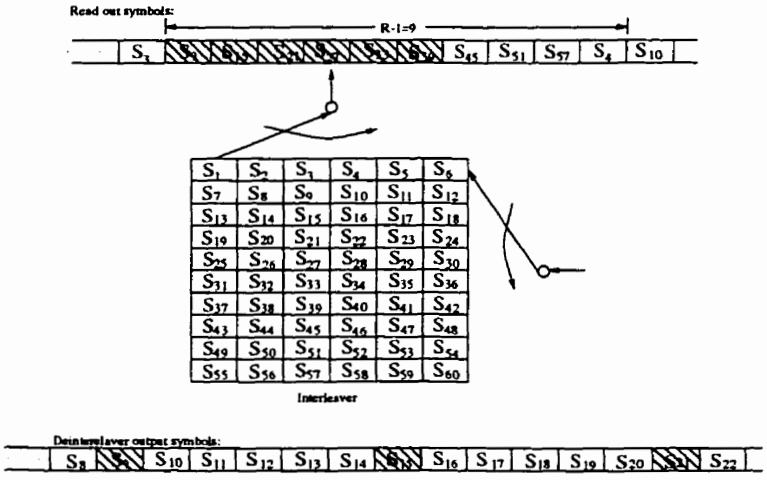


Figure 3.7: A 10 by 6 symbol block interleaving.

A symbol block interleaver is used in the IS-95 together with the convolutional code. Its interleaver diagram is shown in Fig. 3.8. The encoded symbol is read into a table, which is a 6 rows by 64 columns interleaver. The symbol is read into the table row by row, and read out column by column. However the read out procedure is not successive (Refer to Appendix A). The first column to be read out is column

1, followed by column 33, 17, 49, 9 and so on. At first glance, the read out procedure appears to be random; however it follows an interleaving algorithm which can achieve an interleaving degree of 32. This interleaver provides a big λ so that it has more resistance against the burst error. The bit error rate performance of this symbol block interleaving is compared to the chip interleaving under a fast fading channel. In the next section, we introduce a chip interleaving scheme, and define the chip interleaving degree which is different from the symbol interleaving degree.

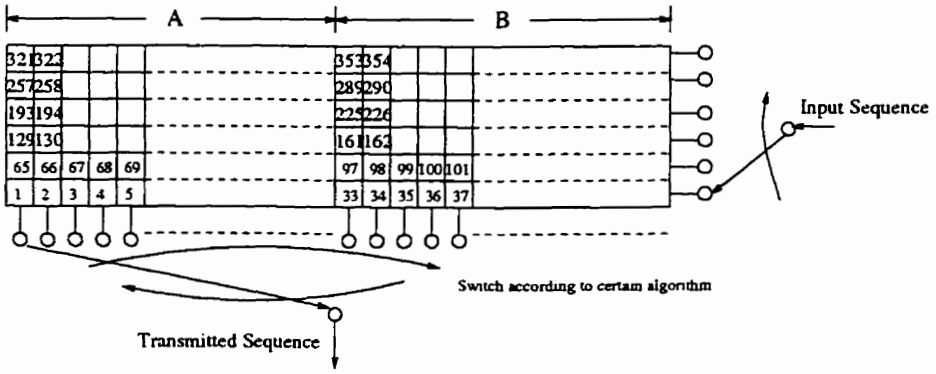


Figure 3.8: CDMA cellular standard IS-95 forward link block interleaving

3.4 Chip Block Interleaving

As mentioned in Chapter 1, an intact symbol is divided into smaller parts and transmitted through different time slots by the interleaving process. As a result, chip interleaving can be viewed as a combination of time diversity and interleaving. When an information bit is spread by multiplying it with a long sequence of PN code, each information bit contains a number of chips. This information bit is divided into smaller parts and each part contains several chips. Since we use the IS-95 as our research guideline, we do not want to impose major modifications on the standard. Fig. 3.9 shows each information bit spread by the PN code, each bit containing 128 chips. In the forward link, the rate 1/2 convolutional encoder encodes each bit into two symbols, therefore each symbol contains 64 (128/2) chips. After the symbol spreading, several chips are grouped together. One group after another group is read

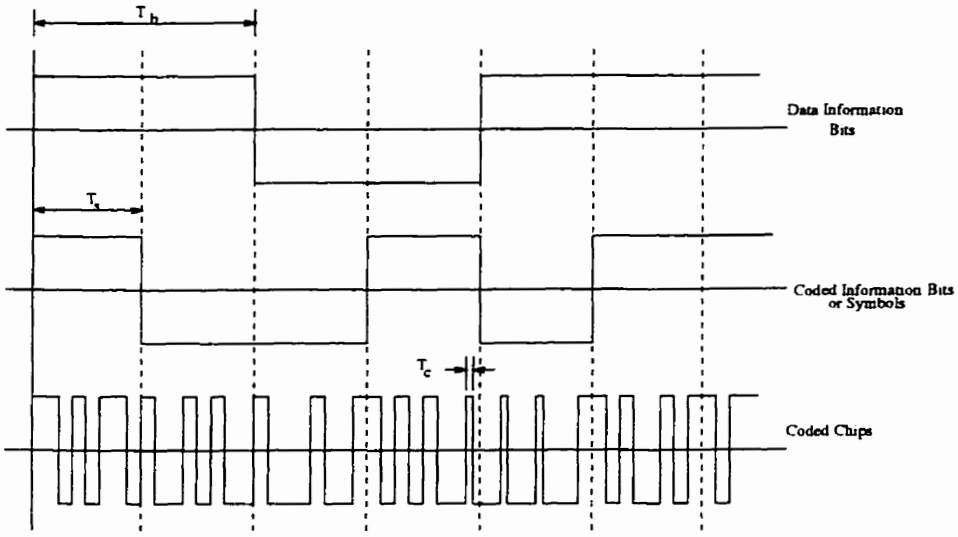


Figure 3.9: Information bit and symbol DS spreading

into the interleaver. Then the groups are read out from the interleaver again for transmission. Fig. 3.10 shows two of the symbols in a speech frame. Each of these symbols is divided into 4 groups. Since each symbol contains 64 chips and each group has 16 chips, this configuration is called the 4 16-chip groups per symbol chip interleaving.

The chip interleaving showed in Fig. 3.10 has a maximum separation interleaving degree, because the separation between two successive groups are maximized and distributed throughout the speech frame. For this 4 16-chip groups per symbol configuration, a 20 ms speech frame is divided into four time intervals. Each of the four groups of chips are placed at the beginning of each intervals. Hence, within each time interval of the speech frame contains 384 16-chip groups from the 384 symbols. The maximum separation interleaving degree is the maximum separation that can be achieved under a fixed length of speech frame. If we want to separate the groups even further from one another, the length of the speech frame needs to be increased and this results in a major modification to the standard. The 4 16-chip groups per symbol interleaver is shown in Fig. 3.11. Each row of this interleaver table corresponds to a symbol. Since this symbol is divided into 4 parts, each part contains 16 chips. The 16 chips from the first row are read out continuously. Then the 16 chips in the second row are read out. This is repeated to the last row of the table. The 16 chips of first

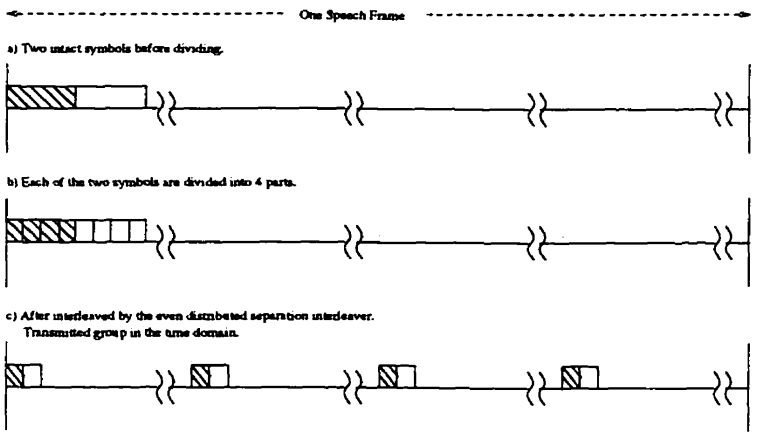


Figure 3.10: A maximum separation distributed 4 16-chip groups/symbol transmitted signal.

row from column 17 to 32 are read out, followed by the 16 chip in the next row. The process continues until the whole interleaver is empty.

We can take each 16-chip group as an entity, and the interleaver is simplified as in Fig. 3.12. X denotes the group, i represents the symbol, and j is the divided part of a symbol. For example, in the notation X2-3, the 'X' refers to a 16-chip group, the '2' refers to the second symbol in the speech frame, and the '3' refers to the third part of a divided symbol. We can further divide a symbol into more groups. As a symbol is divided into more groups, the diversity increases, but the number of chips in a group decreases. Because of fixed length of the speech frame, as the amount of diversity increases, the separation between these groups decreases. Table 3.1 shows five possible symbol divisions for the IS-95. Fig. 3.13 shows the transmission of the groups after the chip interleaving for the other four configurations with the maximum separation interleaving degree. These four types of chip interleaving contain a different number of chips per symbol and a different number of groups per symbol. For example Fig 3.13(c) shows a 32 groups per symbol chip interleaving with each group containing two chips; i.e. a 2-chip group configuration. Fig. 3.14 shows the interleavers for the five chip configurations of the maximum separation. The groups are read into the interleaver row by row, and read out from the interleaver column by column.

Chip interleaving sends the same information in N different time slots, thus achiev-

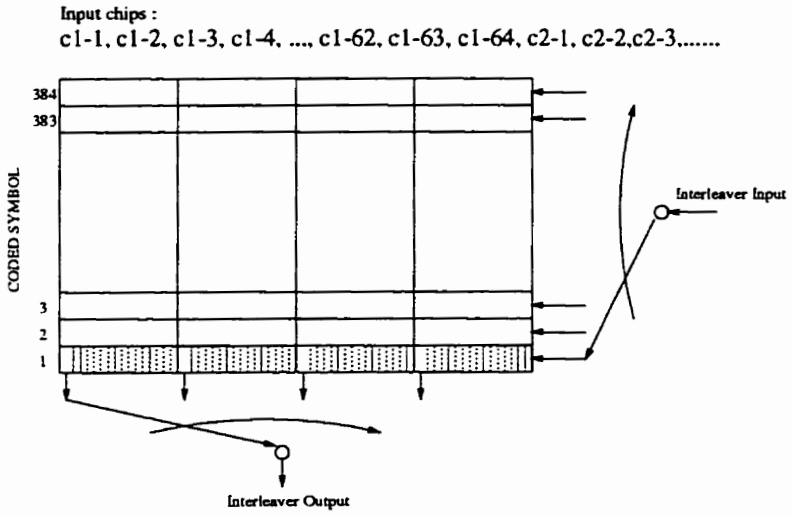


Figure 3.11: A maximum separation interleaving degree of the 4 16-chip groups/symbol chip interleaver.

groups/bit	groups/symbol	number of chips/group
8	4	16
16	8	8
32	16	4
64	32	2
128	64	1

Table 3.1: Five different chip interleaving configurations.

ing N diversity order. When the time slots separation is at least equal to or exceeds the coherence time of the channel, the received signal from the same information will be affected by independent fading. Therefore we define the chip time separation at the chip interleaver output between two first chip in two successive same information group as the interleaving degree. Table 3.2 shows six possible interleaving degrees for a particular chip interleaving configuration. The principle of chip interleaving is to collect the energy from different groups of the same symbol through the fading channel. Therefore it prevents a symbol from staying in a simultaneous deep fade.

A chip interleaving configuration can be further classified by different interleaving degrees. Because of the speech frame length constraint, different chip interleaving

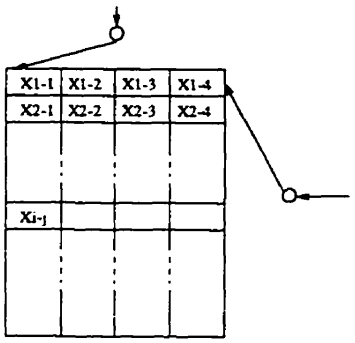


Figure 3.12: A maximum separation 4 16-chip groups/symbol chip interleaver.

configurations have different possible numbers of interleaving degrees. A Certain number of chip interleaving configurations do not necessarily have all the possible interleaving degrees shown in table 3.2. For example a 16-chip group interleaving has four possible chip interleaving degrees. These are shown in Fig. 3.15. Interleaving degree A is the maximum separation for the 16-chip interleaving. Interleaving degree C is the maximum separation for the 4-chip group interleaving configuration as shown in Fig. 3.17. The separations for the 4 16-chip groups are further reduced to separation D and E as shown in Fig. 3.15. From the figure, the interleaving degree becomes smaller as the separation between the groups is reduced.

We consider the 20 ms speech frame in our simulation. An 8-chip group configuration is shown in Fig. 3.16, there are a total of four different separations or interleaving degrees. On the other hand, there are three different separations for a 16-chip group interleaving as shown in Fig. 3.17. The 2-chip group and 1-chip group configurations have two types of separations respectively as shown in Fig. 3.18 and Fig. 3.19.

From different separations we can compare the different performance due to the different number of groups from a symbol, and also the number of chips per symbol. Simulation results are presented in the next chapter. These results show that the performances are affected by different parameters of the chip interleaving process. We also look at the effect of a two-path fading model in the last part of the next chapter. From this section we see that not much modification is introduced into the existing system. From the simulation results in the next chapter, it appears that chip interleaving is 2 to 3 dB better in SNR for the bit error rate performance compared

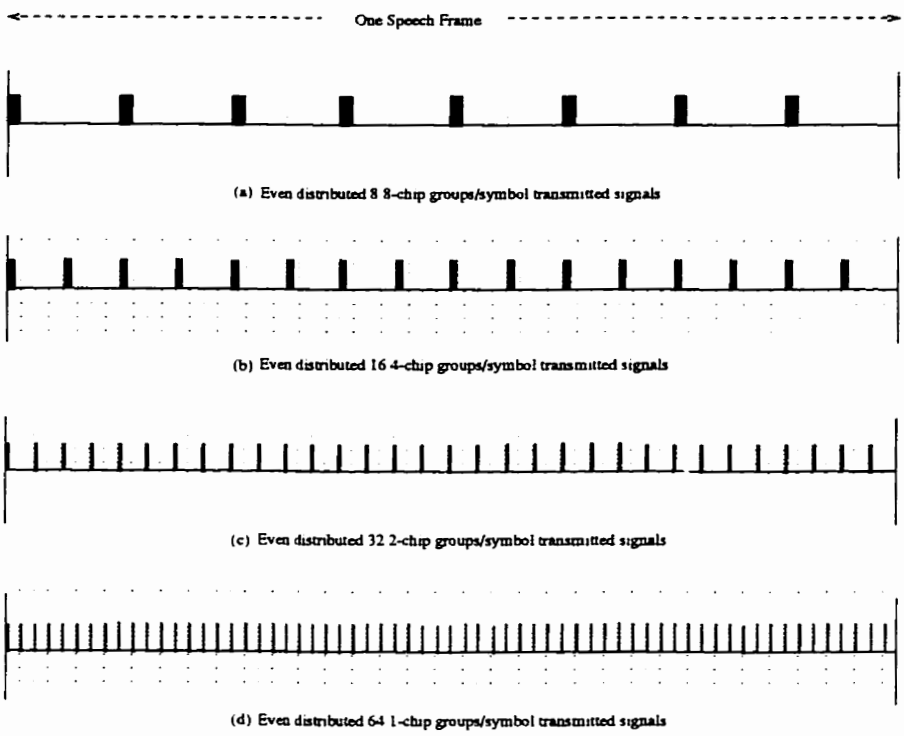


Figure 3.13: Four maximum separation chip interleaving configurations shown in four speech frames.

chip interleaving scheme	interleaving degree
A	$6144T_c$
B	$3072T_c$
C	$1536T_c$
D	$768T_c$
E	$384T_c$
F	$192T_c$

Table 3.2: Six different interleaving degrees for chip interleaving scheme.

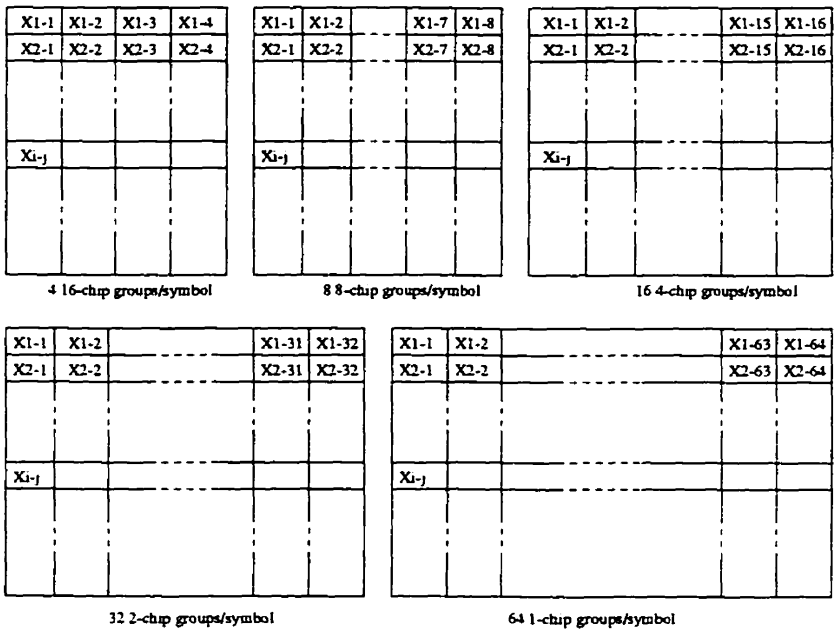


Figure 3.14: Five maximum separation chip interleavers

to the conventional block interleaving used in the IS-95.

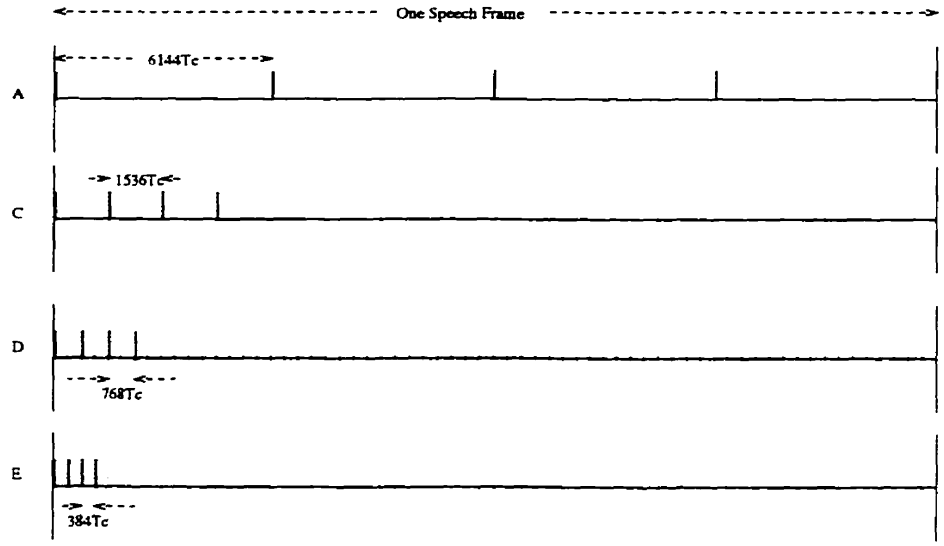


Figure 3.15: Four 16-chip group interleaving degrees shown in time domain.

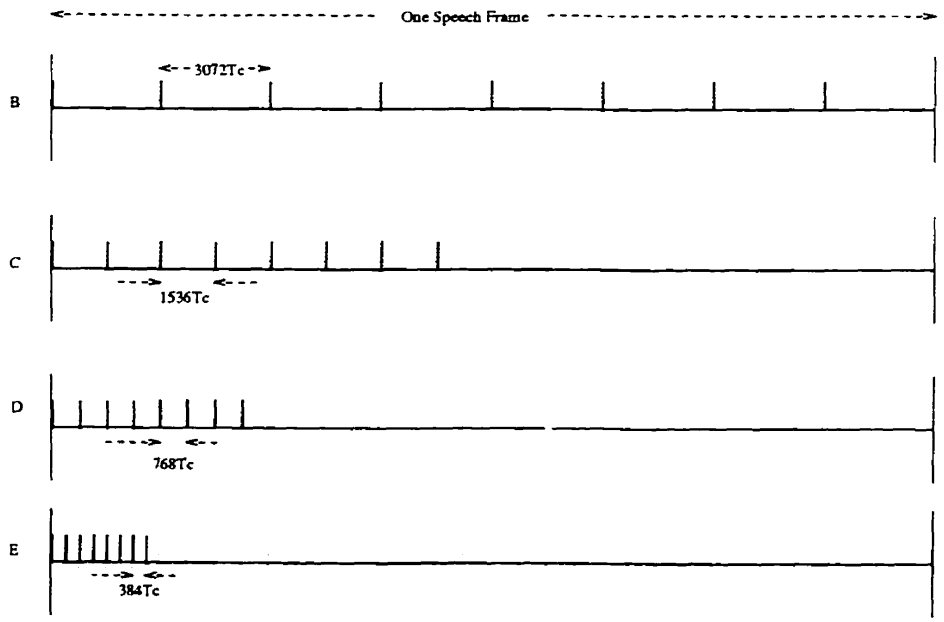


Figure 3.16: Four 8-chip group chip interleaving degrees shown in time domain.

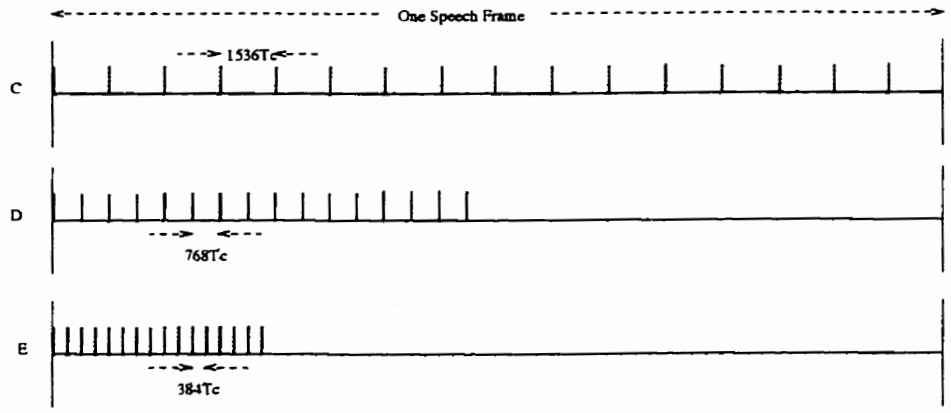


Figure 3.17: Three 4-chip group chip interleaving degrees shown in time domain.

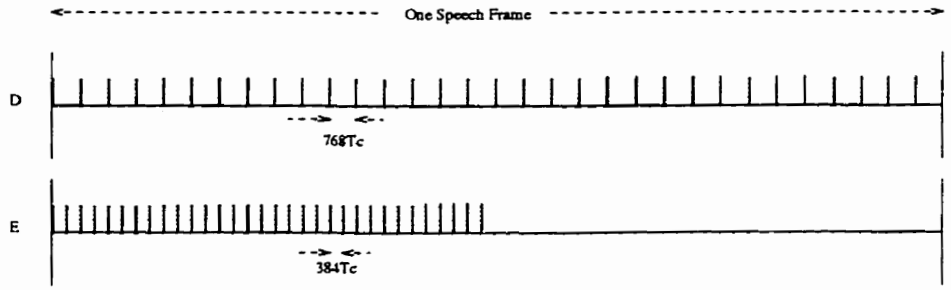


Figure 3.18: Two 2-chip group chip interleaving degrees shown in time domain.

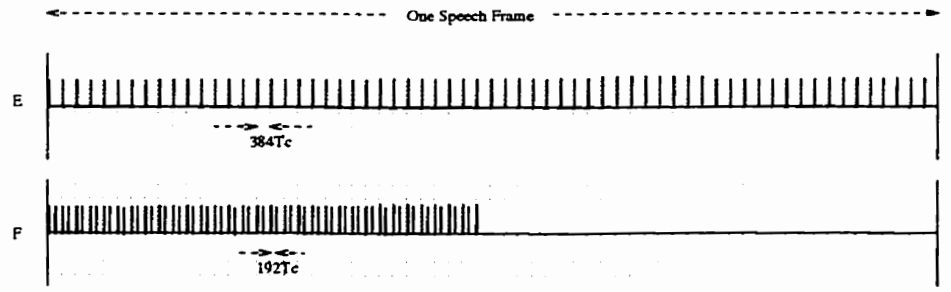


Figure 3.19: Two 1-chip group chip interleaving degrees shown in time domain.

Chapter 4

Chip Interleaving Scheme Performance

We compare the simulation results between various chip interleaving configurations and interleaving degrees for the chip interleaving scheme. These simulation results show the effect of the number of chips per group and the separations between groups on the BER performance. Section 4.1 describes the system for our simulation. We discuss the simulation results of chip interleaving and hard decision decoding in section 4.2, and soft decision decoding in section 4.3. The above simulations are based on the one-path Rayleigh fading channel model . Section 4.4 discusses the chip interleaving simulation results for a two-path Rayleigh fading channel model.

4.1 System Description

In the forward link of IS-95, the BS has four different vocoder rates: 1200 b/s, 2400 b/s, 4800 b/s, and 9600 b/s. The vocoder switches between these four different rates depending on the speech activity. If the speech is fully transmitted, the 9600 b/s rate is used. The data bit in the forward link simulation is encoded into two symbols. Each speech frame contains 192 data bits and corresponds to 384 symbols per 20 ms speech frame. After the information data is encoded, the symbols are read into a block interleaver. The interleaved symbol is covered by the Walsh function and further spread by the inphase and quadrature spreading code. In our chip interleaving

system, the symbol block interleaver is substituted by the chip interleaver. This chip interleaving was described in Chapter 3, section 3.4. The channel bandwidth of 1.25 Mhz is used in our simulation. The chip rate is 1.2288 Mcps.

In the chip interleaving, the received data is despread by the spreading code before the deinterleaving process. The correlation output is sampled at T_g. The correlator output is fed into the chip deinterleaver. When the deinterleaver is full, the groups are read out and then combined before being fed to the threshold detector. The block diagram of the above process was shown in Fig. 1.6 in Chapter 3. A detailed block diagram presentation of chip deinterleaving is shown in Appendix B.

In our simulation, the transmitted signal goes through a Rayleigh selective fading channel. The maximum Doppler shift for all the simulation is 60 Hz, which corresponds to a vehicle speed of 72 km/h at the carrier frequency of 900 MHz. Jake's model is used to generate a sequence of time-correlated Rayleigh random numbers. The channel attenuation is fixed for one symbol period, therefore the chips within the symbol interval have the same fading amplitude. The combiner uses an equal gain combining technique. First we investigate the single path Rayleigh fading model using two different decision decodings.

4.2 Chip Interleaving and Hard Decision Decoding

Five different chip interleaving configurations and their interleaving degrees are shown in table 4.1 and table 4.2. The five types of chip interleaving configurations are 4 16-chip groups/symbol, 8 8-chip groups/symbol, 16 4-chip groups/symbol, 32 2-chip groups/symbol, and 64 1-chip groups/symbol. The Viterbi decoding is utilized in the simulation. Fig. 4.1 shows the simulation results for the five chip interleaving configurations with maximum separation as explained in Chapter 3, section 3.4.

Fig. 4.1 shows that the 16 4-chip groups per symbol chip interleaving configuration outperforms other chip interleaving configurations. Table 4.3 shows the chip interleaving degree for each of the maximum separation chip interleaving configurations. The maximum separation of 64 1-chip groups per symbol configuration performs more

group/bit	group/symbol	number of chips/group
8	4	16
16	8	8
32	16	4
64	32	2
128	64	1

Table 4.1: Five different chip interleaving configurations.

chip interleaving scheme	interleaving degree
A	$6144T_c$
B	$3072T_c$
C	$1536T_c$
D	$768T_c$
E	$384T_c$
F	$192T_c$

Table 4.2: Five interleaving degree for chip interleaving.

poorly than the 16 4-chip groups per symbol, mainly because of the small chip interleaving degree for the 1-chip group configuration. When we look at the 4 16-chip groups, although it has a bigger interleaving degree, it performs more poorly than the 16 4-chip group configuration. This is due to the smaller number of groups per symbol for the 16-chip group compared to the 4-chip group configuration. Fig. 4.2 to Fig. 4.6 show different chip interleaving configurations with various interleaving degrees. All the graphs show that the bigger the interleaving degree, the better the bit error rate performance. When the successive groups of chips from a symbol are

Chip interleaving configuration	interleaving degree
16-chip/group	$6144T_c$
8-chip/group	$3072T_c$
4-chip/group	$1536T_c$
2-chip/group	$768T_c$
1-chip/group	$384T_c$

Table 4.3: Five different chip interleaving configurations and their chip interleaving degree for the maximum separation chip interleaving scheme.

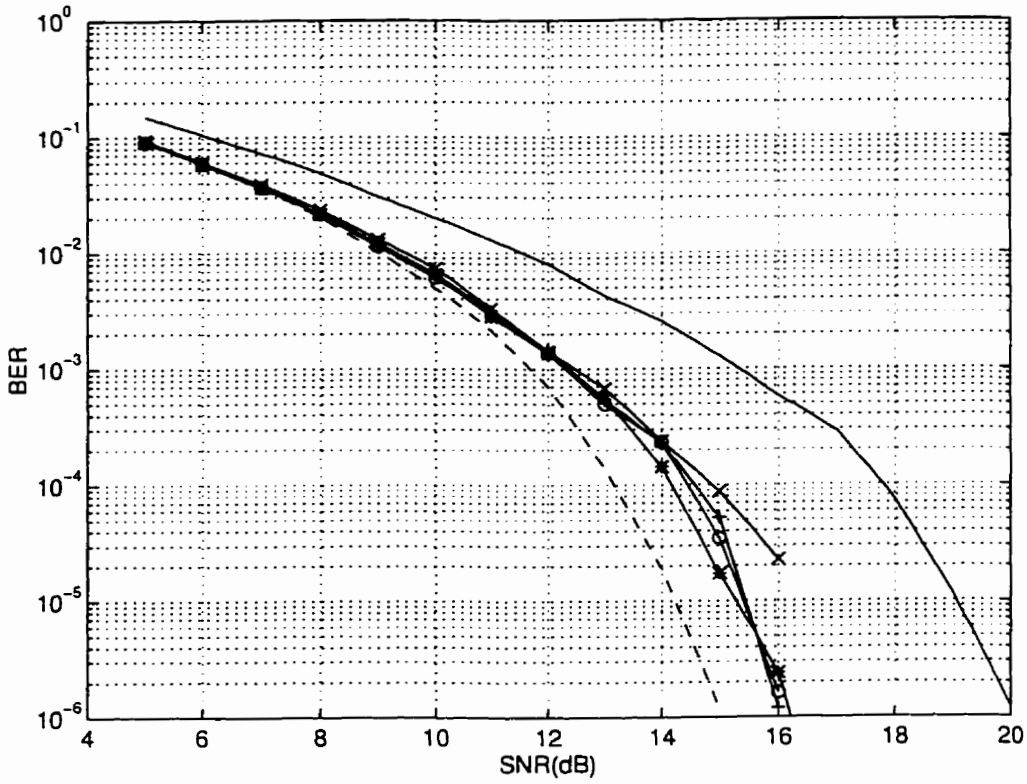


Figure 4.1: Five different chip interleaving configurations for maximum separation, and IS-95 symbol block interleaving. (Hard decision decoding)
Legend: Symbol block interleaving(solid line), 4 16-chip groups/symbol('×'), 8 8-chip groups/symbol('+'), 16 4-chip groups/symbol(dash line), 32 2-chip groups/symbol('o'), 64 1-chip groups/symbol(''). Maximum Doppler frequency=60 Hz.*

interleaved with a big interleaving degree, the time correlation between the successive groups is minimized. Fig. 4.2 shows that for a 16-chip configuration, the A scheme is 3 dB better than the E scheme at 10^{-3} BER, while Fig. 4.4 for a 4-chip configuration shows that the C scheme is 2.3 dB better than the E scheme.

Fig. 4.7 shows the simulation results of four different chip interleaving configurations for interleaving degree D. This graph shows the effect of a different number of groups per symbol on bit error rate performance with the same interleaving degree, i.e. we hold the interleaving degree constant and vary the degree of diversity. From this figure we see that as we increase the number of groups per symbol while holding

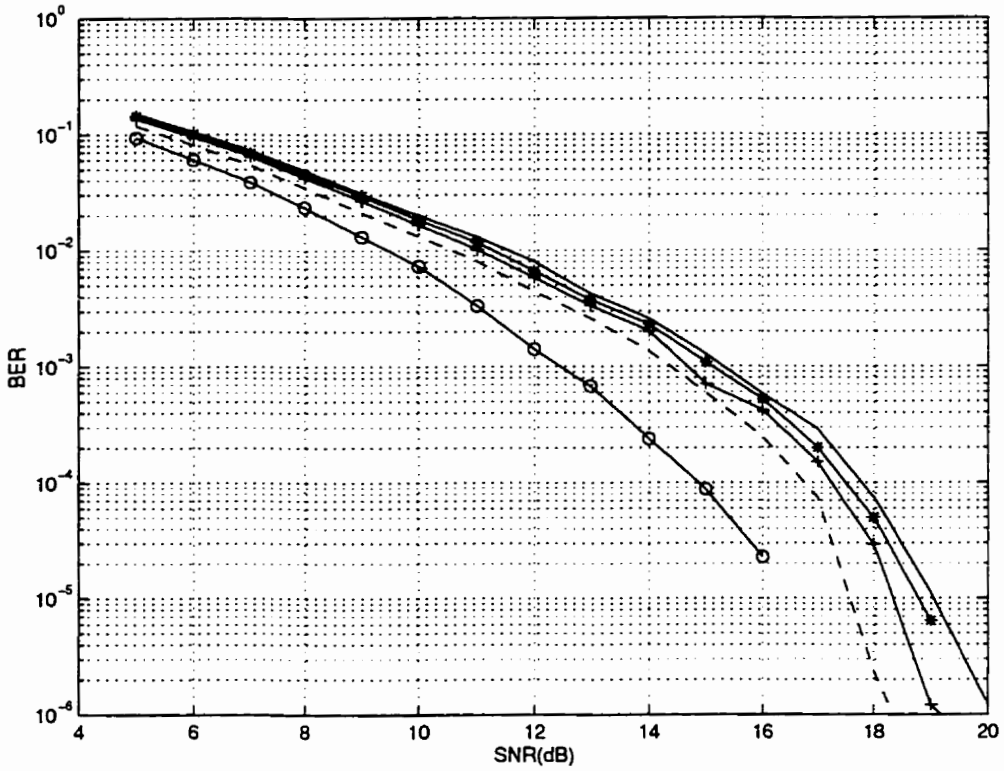


Figure 4.2: Four different chip interleaving degrees for 4 16-chip groups/symbol configuration. (Hard decision decoding)

Legend: Symbol interleaving(solid line), and four different chip interleaving degrees: E('$*$'), D('+'), C(dash line), A('o').

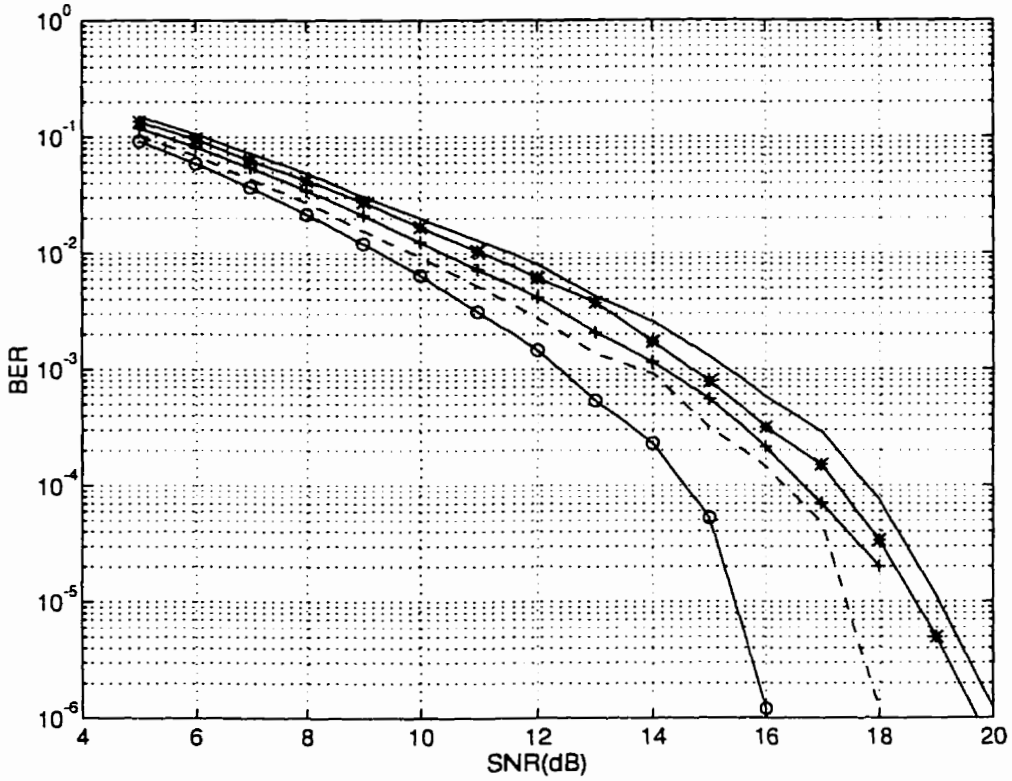


Figure 4.3: Four different chip interleaving degrees for 8 8-chip groups/symbol configuration. (Hard decision decoding)

Legend: Symbol interleaving(solid line), and four different chip interleaving degrees: E('∗'), D('+'), C(dash line), B('o').

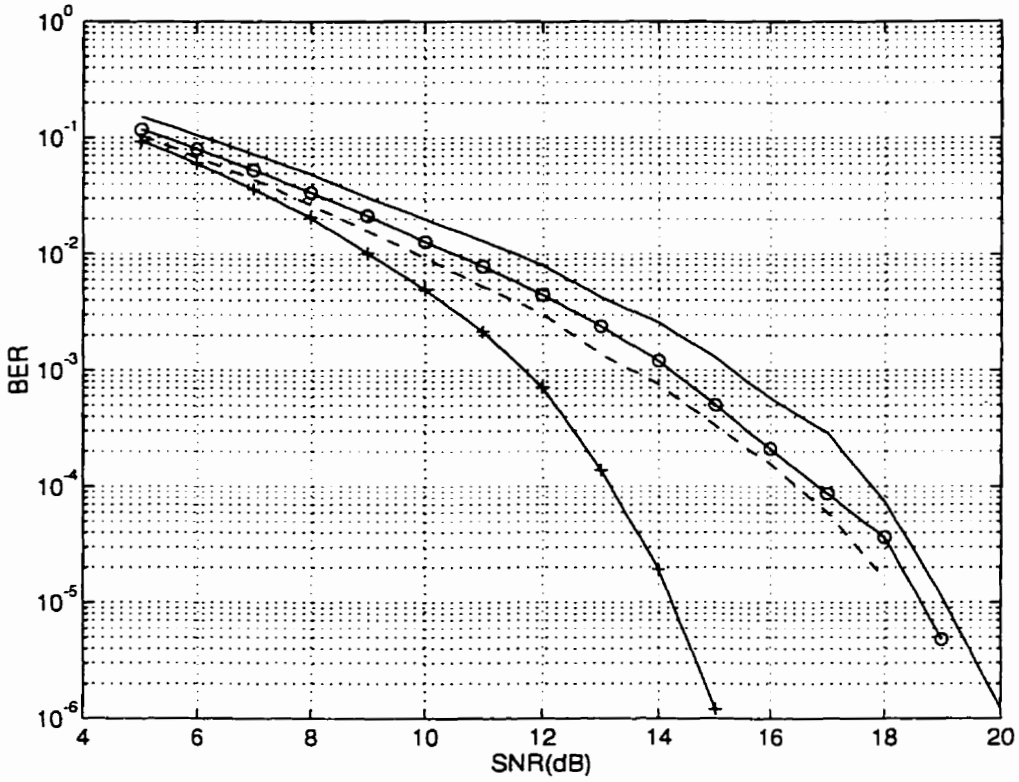


Figure 4.4: Three different chip interleaving degrees for 16 4-chip groups/symbol configuration. (Hard decision decoding)

Legend: Symbol interleaving(solid line), and three different chip interleaving degrees: E('o'), D(dash line), C('+').

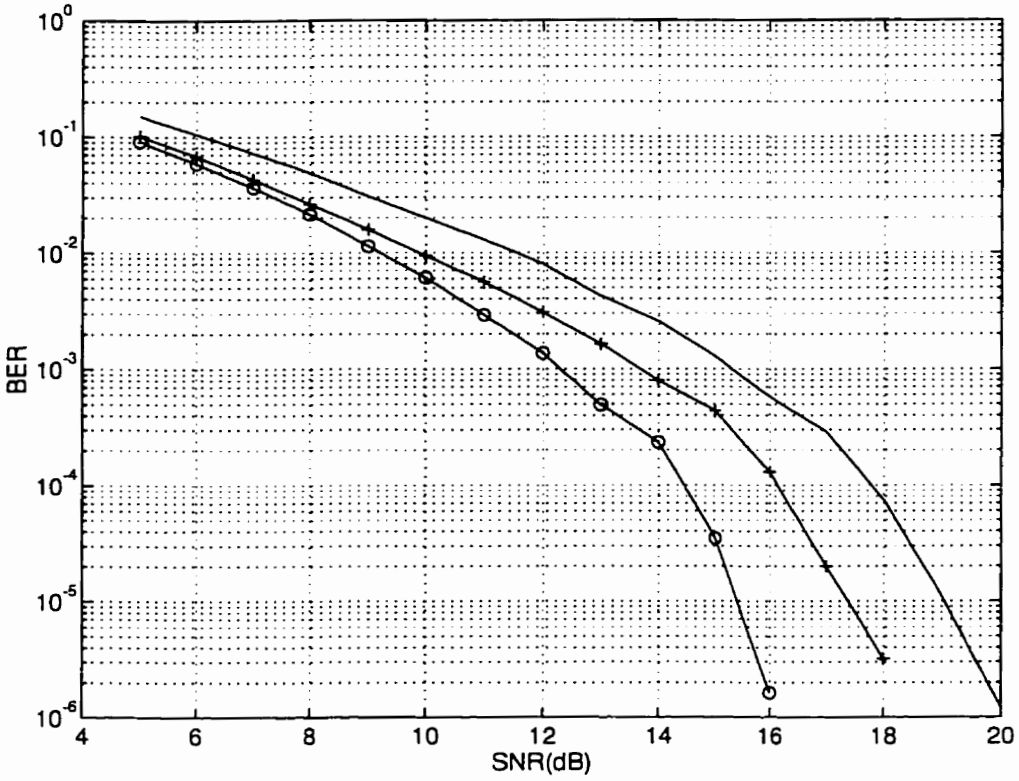


Figure 4.5: Two different chip interleaving degrees for 32 2-chip groups/symbol configuration. (Hard decision decoding)
Legend: Symbol interleaving(solid line), and two chip interleaving degrees: E('+'), D('o').

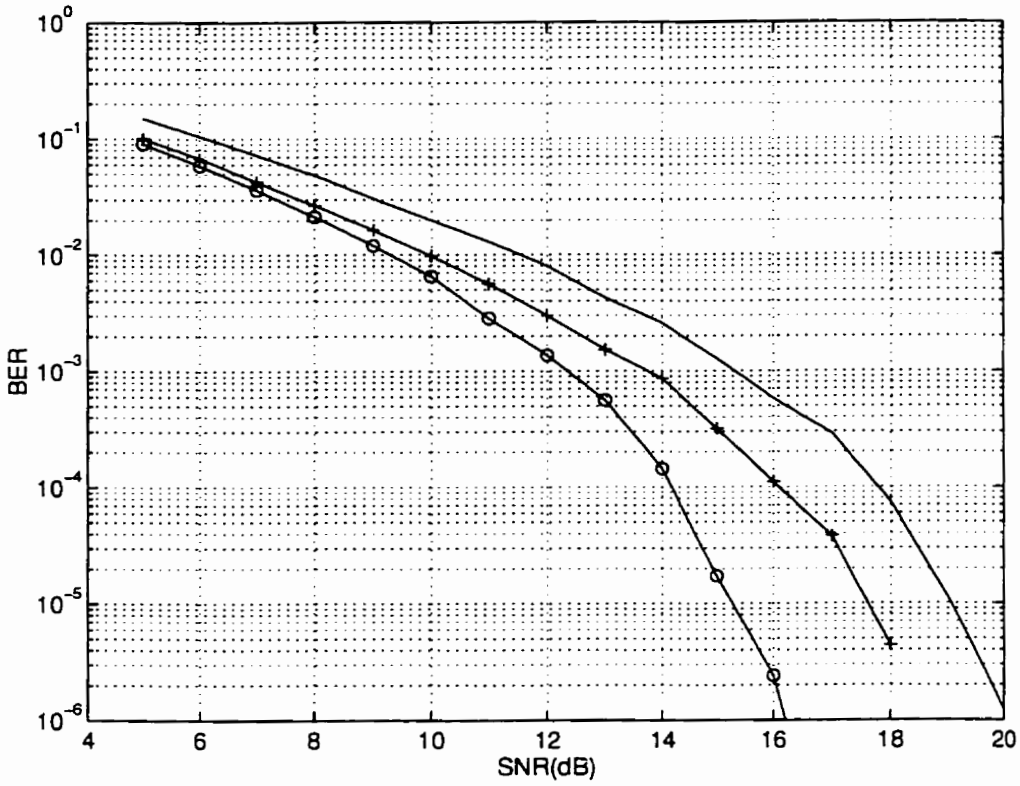


Figure 4.6: Two different chip interleaving degrees for 64 1-chip groups/symbol configuration. (Hard decision decoding)
Legend: Symbol interleaving(solid line), and two chip interleaving degrees: F('+'), E('o').

the interleaving degree constant, the performance is improving. Fig. 4.8 shows the simulation results of five different chip interleaving configurations for interleaving degree E. As we can see from the graph, the 64 1-chip groups per symbol performs better than the other configurations. This shows that as the number of groups increases, this provides more diversity to the receiver, hence it improves the performance. In addition, as we increase the interleaving degree for a certain chip interleaving configuration, we improve the performance. Thus for a one-path channel model, the optimum performance is when we can achieve the maximum amount of diversity by dividing a symbol into more parts, and yet minimize the time correlation of the received signal by interleaving the groups further from each other.

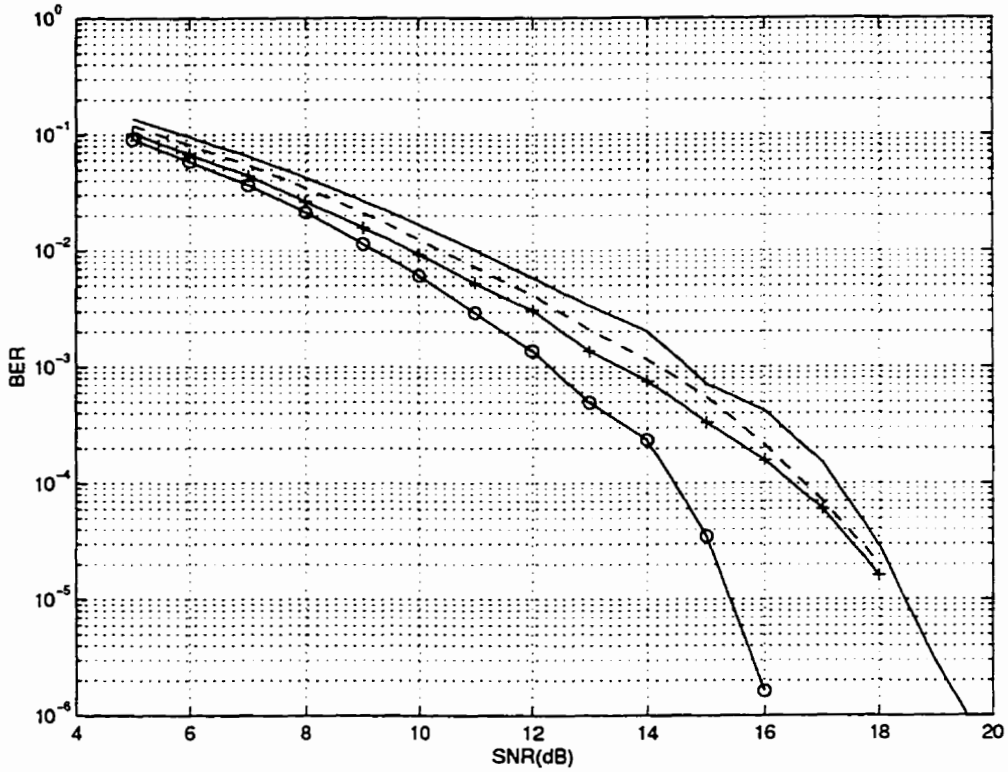


Figure 4.7: Four chip interleaving configurations for interleaving degree D. (Hard decision decoding)

Legends: 4 16-chip groups/symbol (solid line), 8 8-chip groups/symbol(dash line), 16 4-chip groups/symbol('+'), 32 2-chip groups/symbol('o').

4.3 Chip Interleaving and Soft Decision Decoding

Soft decision decoding uses an eight level quantization metric for maximum likelihood decoding, as shown in Chapter 2, section 2.2. Fig. 4.9 shows the soft decision decoding simulation results for symbol block interleaving and chip interleaving. From this figure we see that the soft decision decoding symbol block interleaving performs 2 dB worse than the maximum separation of 16 4-chip groups per symbol configuration at 10^{-3} BER. Fig. 4.10 to Fig. 4.14 show the comparison between hard decision decoding and soft decision decoding for five different chip interleaving configurations. All the results show that the soft decision decoding outperforms the hard decision decoding by about $1dB$ at 10^{-3} BER. We also see that as the number of groups increases the soft

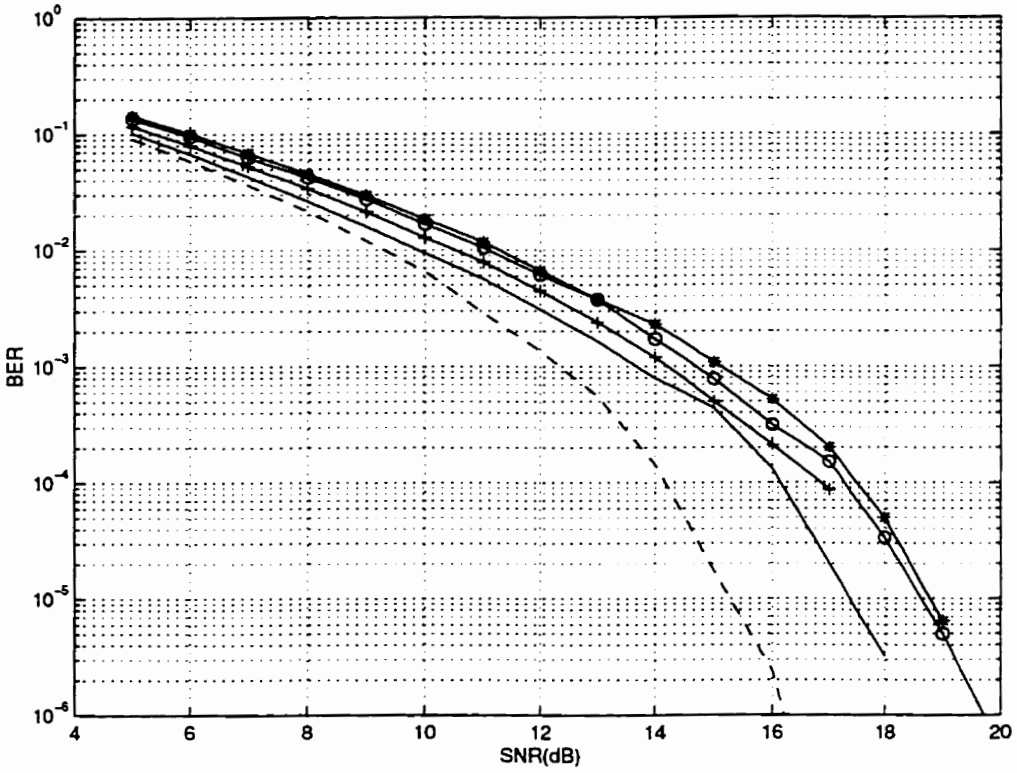


Figure 4.8: Five chip interleaving configurations for interleaving degree E. (Hard decision decoding)

Legend: 4 16-chip groups/symbol ('∗'), 8 8-chip groups/symbol('o'), 16 4-chip groups/symbol('+'). 32 2-chip groups/symbol(solid line), 64 1-chip groups/symbol(dash line).

decision decoding does not improve much. Fig. 4.14 shows that the simulation results of the 64 1-chip groups per symbol interleaving has roughly the same performance with both hard and soft decision decoding. As a result, the eight level soft decision decoding has equivalent bit error rate performance as hard decision decoding when we interleave each chip from a symbol under a one-path Rayleigh fading channel.

4.4 Chip Interleaving and the Rake Receiver

In this section we investigate the two-path fading channel model. We assume that there are two resolvable paths available at the receiver, that these paths undergo independent Rayleigh fading. The Rake receiver uses the equal gain combining method to combine the two paths, therefore the two channel taps weights of the Rake receiver are set to unity. The power of the received second path is 3dB less than the first arrived path. We include the interpath interference in the Rake receiver for our simulation. Fig. 4.15 shows the simulation results of the one-path and two-path symbol block interleaving performances. The two-path model is 3.5dB in SNR better than the one path model at 10^{-3} BER. The two-path model for all the chip interleaving configurations is roughly 2 dB better in SNR than the two-path symbol block interleaving.

We observe from Fig. 4.15 that as the number of groups increases, the performance in SNR also becomes better. This is different from the one-path model where the 16 4-chip groups per symbol has the best performance among others. From these comparisons we conclude that the more the diversity, the better the performance. From the ideal chip interleaving, this is also the case. When we provide additional uncorrelated paths to the receiver, this directly increases the degree of diversity at the receiver. Therefore the two-path model has the performance similar to the ideal chip interleaving case; that is, the performance is increasing in a monotonical manner according to the number of groups per symbol for the chip interleaving. Fig. 4.16 to Fig. 4.20 show the comparison between the one-path model and two-path model of the maximum separation for the five different chip interleaving configurations with hard decision decoding. On the average, the Rake receiver has 2 dB improvement in SNR at 10^{-3} BER compared to the one-path model.

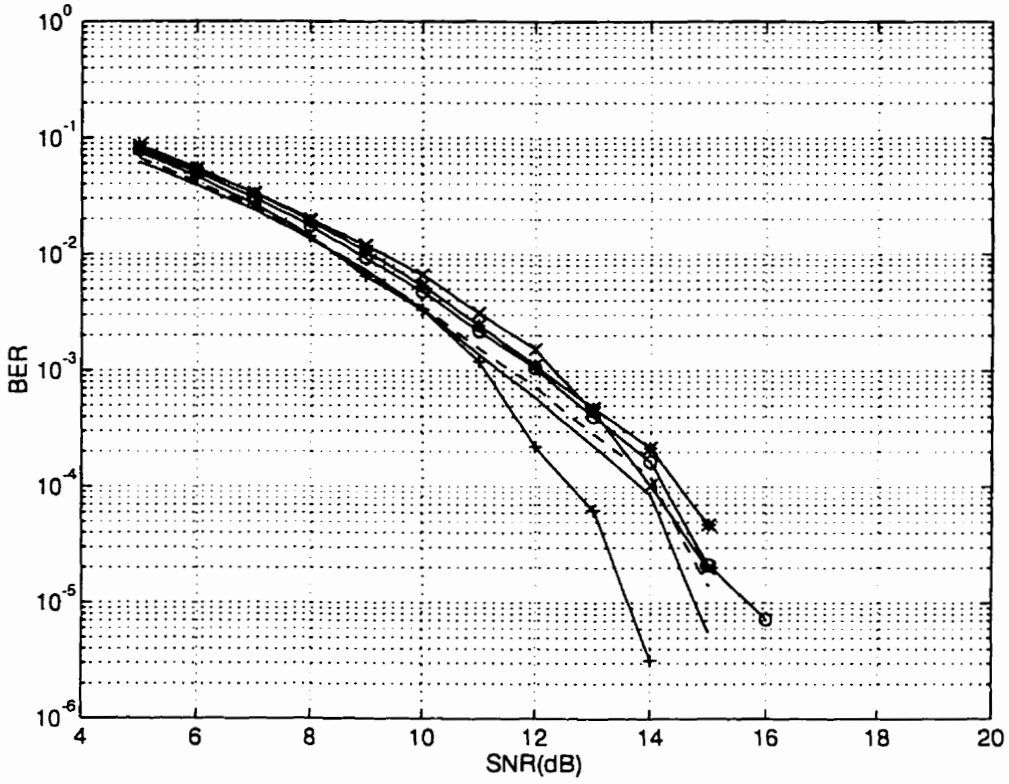


Figure 4.9: Five different chip interleaving configurations for maximum separation and IS-95 symbol block interleaving. (Soft decision decoding)
Legend: Symbol interleaving('×'), 4 16-chip groups/symbol (solid line), 8 8-chip groups/symbol (dash line), 16 4-chip groups/symbol('+'), 32 2-chip groups/symbol('o'), 64 1-chip groups/symbol('∗').

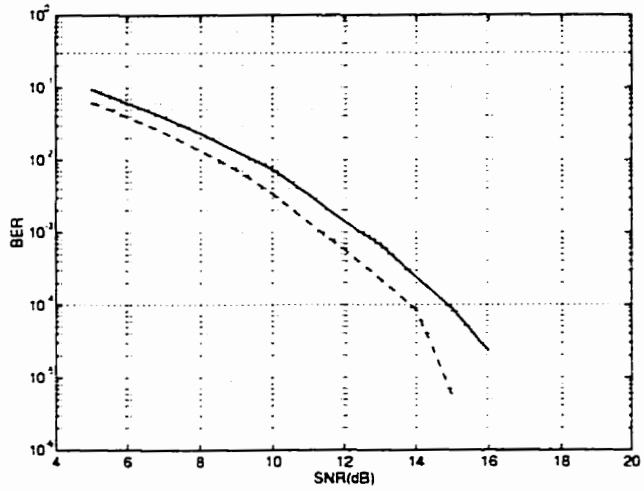


Figure 4.10: Comparison between hard decision decoding and soft decision decoding for 4 16-chip groups/symbol configuration with maximum separation.
Legends: Hard decoding(solid line), soft decoding(dash line).

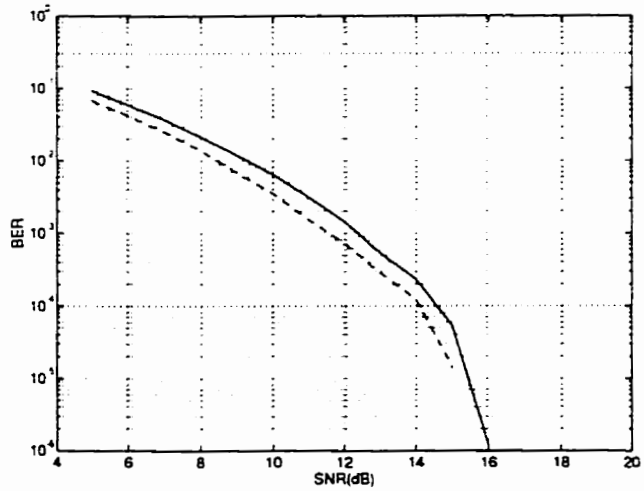


Figure 4.11: Comparison between hard decision decoding and soft decision decoding for 8 8-chip groups/symbol configuration with maximum separation.
Legends: Hard decoding(solid line), soft decoding(dash line).

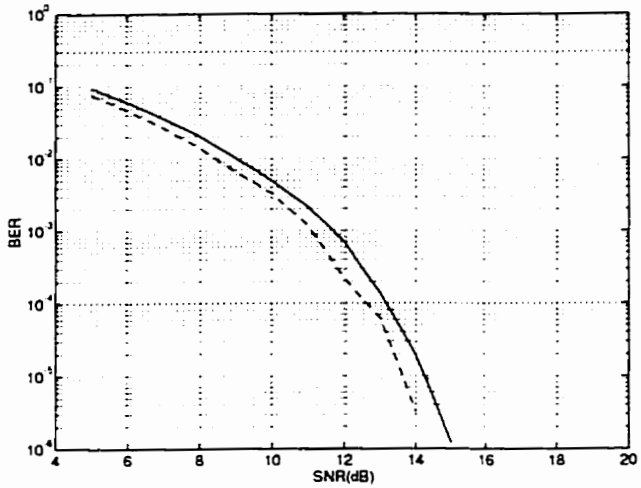


Figure 4.12: Comparison between hard decision decoding and soft decision decoding for 16 4-chip groups/symbol configuration with maximum separation.
Legends: Hard decoding(solid line), soft decoding(dash line).

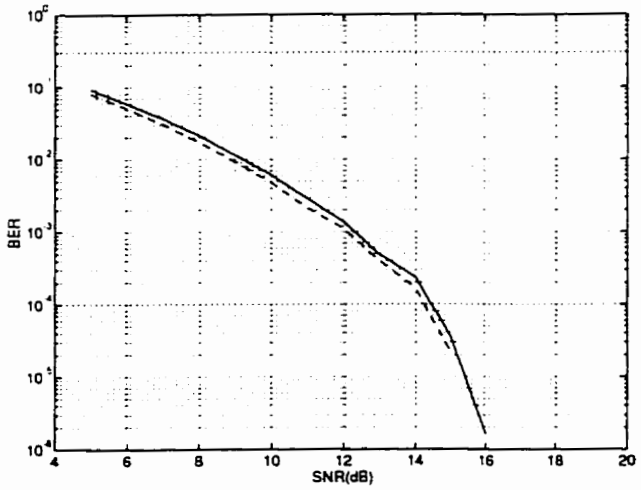


Figure 4.13: Comparison between hard decision decoding and soft decision decoding for 32 2-chip groups/symbol configuration with maximum separation.
Legends: Hard decoding(solid line), soft decoding(dash line).

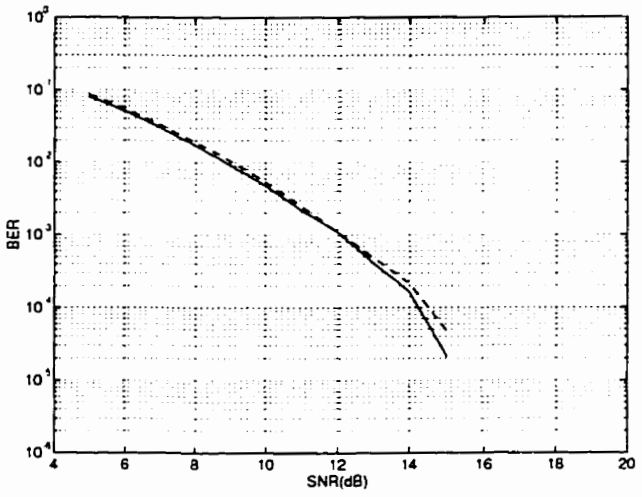


Figure 4.14: Comparison between hard decision decoding and soft decision decoding for 64 1-chip groups/symbol configuration with maximum separation.
Legends: Hard decoding(solid line), soft decoding(dash line).

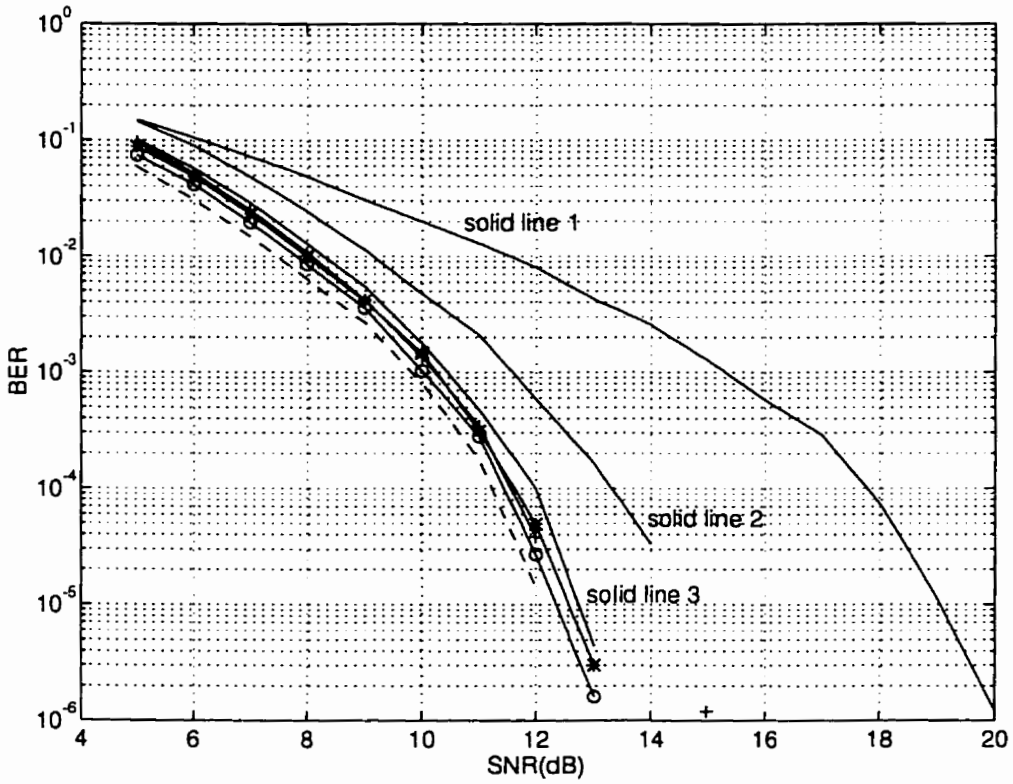


Figure 4.15: Two-path model: Five different chip interleaving configurations for maximum separation. (Hard decision decoding)

Legends: Symbol block interleaving: one path model(solid line 1), two path model(solid line 2); 4 16-chip groups/symbol(solid line 3), 8 8-chip groups/symbol('+'), 16 4-chip groups/symbol(''), 32 2-chip groups/symbol('o'), 64 1-chip groups/symbol(dash line).*

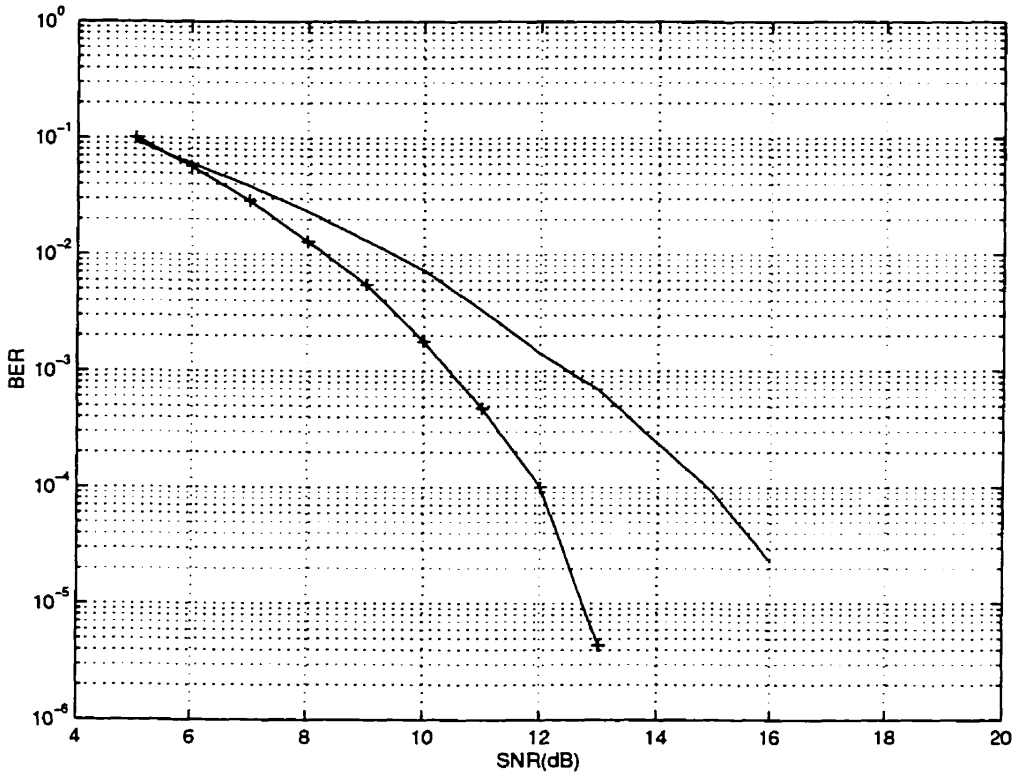


Figure 4.16: Even distributed separation for 4 16-chip groups/symbol chip interleaving configuration.(Hard decision decoding)
Legends: one path model(solid line), two path model('+')

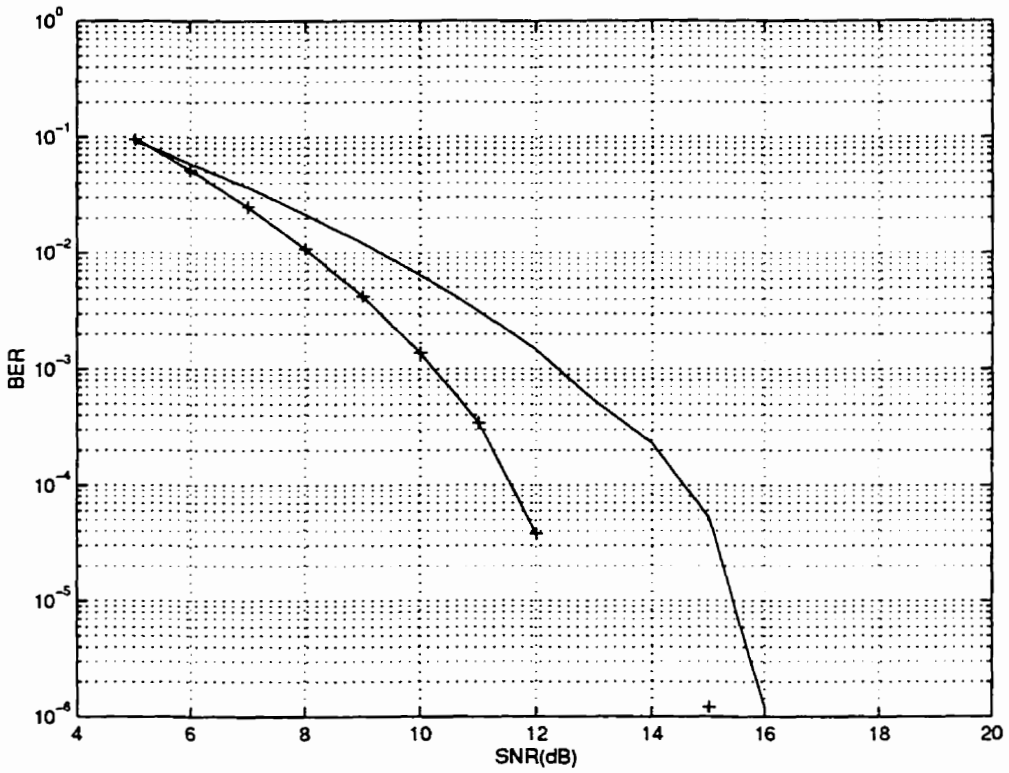


Figure 4.17: Even distributed separation for 8 8-chip groups/symbol chip interleaving configuration.(Hard decision decoding)
Legends: one path model(solid line), two path model('+')

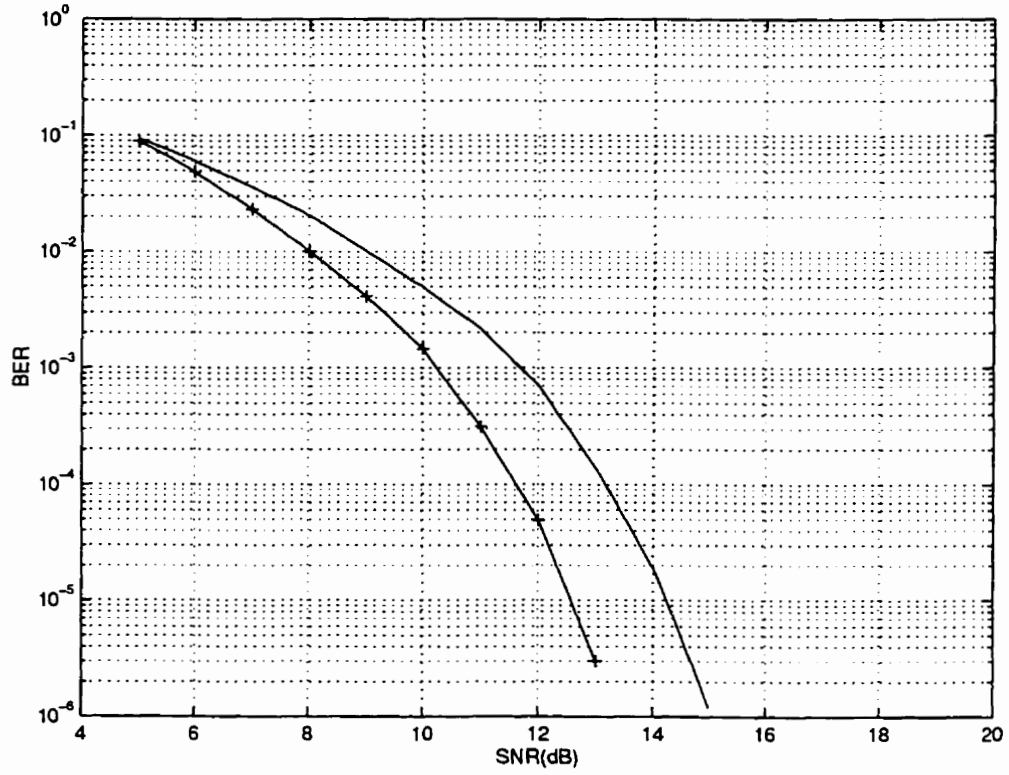


Figure 4.18: Even distributed separation for 16 4-chip groups/symbol chip interleaving configuration.(Hard decision decoding)
Legends: one path model(solid line), two path model('+')

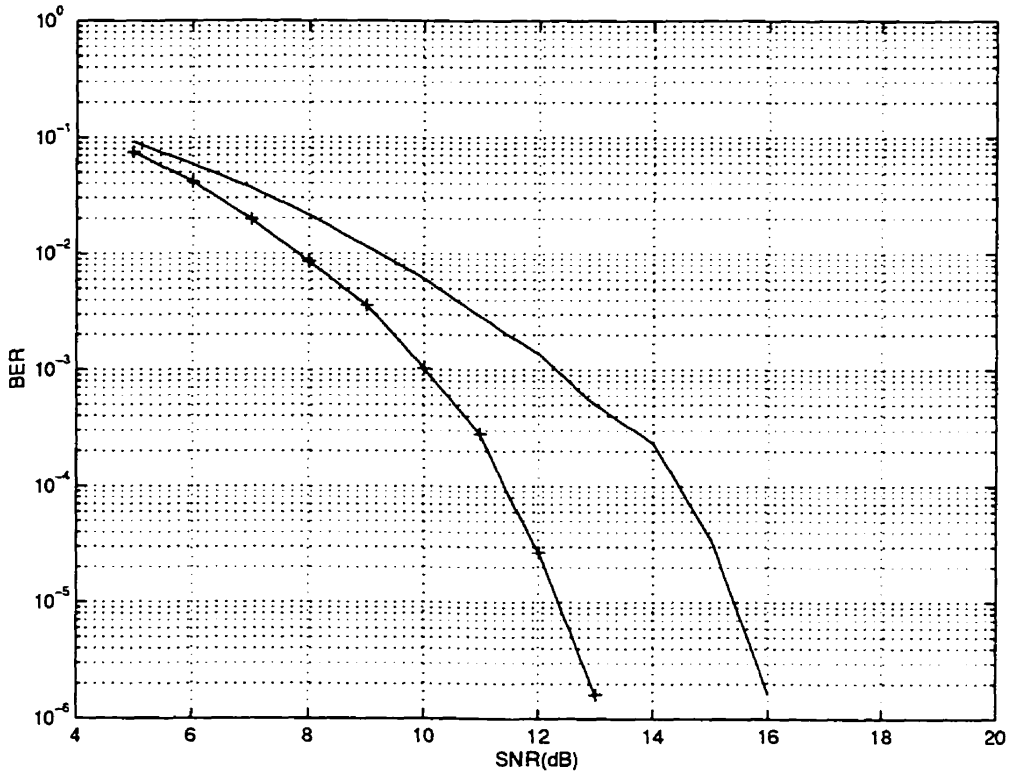


Figure 4.19: Even distributed separation for 32 2-chip groups/symbol chip interleaving configuration.(Hard decision decoding)
Legends: one path model(solid line), two path model('+')

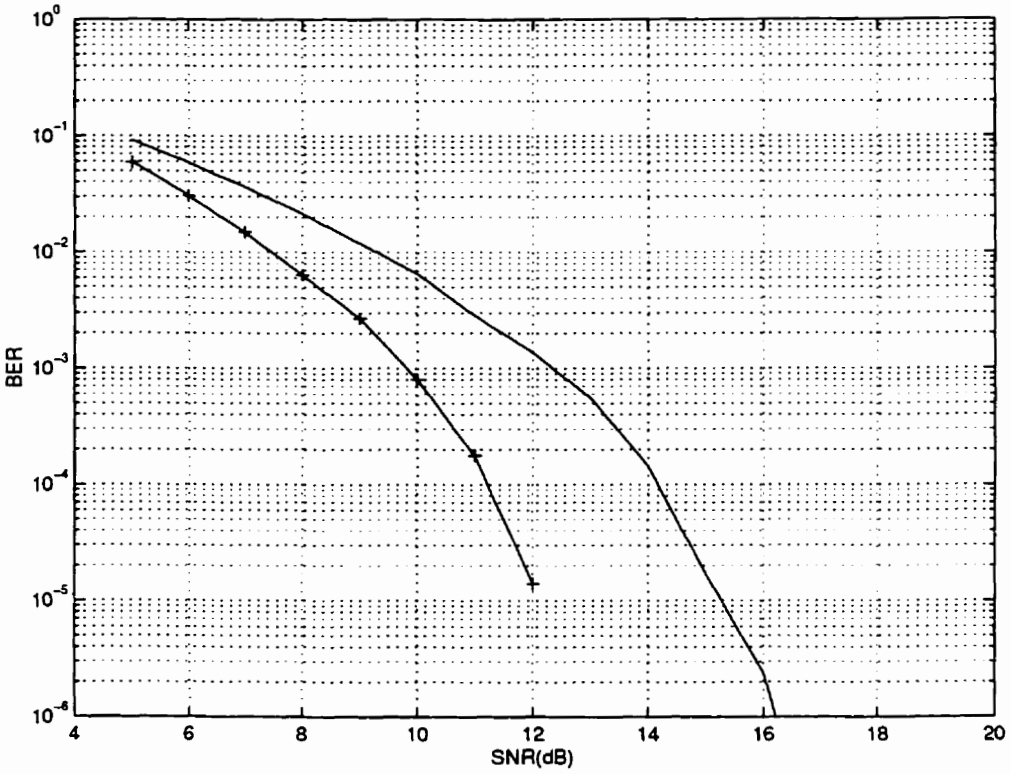


Figure 4.20: Even distributed separation for 64 1-chip groups/symbol chip interleaving configuration.(Hard decision decoding)
Legends: one path model(solid line), two path model('+')

Chapter 5

Conclusion

The simulation results show that chip block interleaving has better bit error rate performance than symbol block interleaving. Chip interleaving improves the SNR by an additional 3 dB at 10^{-3} BER, when compared to symbol block interleaving under hard decision decoding condition. Section 5.1 discusses the insights provided by the research and summarizes the simulation results. Section 5.2 looks at some of the future research topics for chip interleaving.

5.1 Simulation Results Summary and Research Insights

Among the chip interleaving configurations under the one-path model, the 16 4-chip groups per symbol chip interleaving configuration has the best performance. From Fig. 5.1 the simulation results show that 4-chip group configuration which used hard decision decoding improves the SNR by 0.5 dB at the bit error rate of 10^{-3} when compared to soft decision decoding of symbol block interleaving. On the other hand, soft decision decoding for the 16 4-chip groups interleaving performs 0.5 dB better than its hard decision decoding counterpart. As a result, without going into a complex soft decision decoding for symbol block interleaving, we can achieve a better result just by using the hard decision decoding chip interleaving scheme.

Fig. 5.2 shows that the 16 4-chip groups per symbol chip interleaving configuration has reduced the SNR gap between the ideal symbol block interleaving and the IS-95

symbol block interleaving. These results are obtained under hard decision decoding. The 6 dB gap has been reduced to only 3 dB by the 4-chip group interleaving. Chip interleaving has tremendously improved the bit error rate performance for the fast fading channel. The simulation results indicate that chip interleaving can reduce the correlation of the symbol errors more effectively than symbol block interleaving. Ultimately, chip interleaving is more efficient in mitigating the fast fading and burst errors than symbol block interleaving for the forward link of the CDMA cellular systems.

The two-path fading channel model for the chip interleaving performs 2 dB better in SNR than the one-path fading channel model at 10^{-3} BER for all the chip interleaving configurations under hard decision decoding, except the 16 4-chip groups per symbol configuration which has 1 dB improvement. These simulation results are presented in Fig. 4.16 to Fig. 4.20. The 64 1-chip groups per symbol performs better than the 16 4-chip groups per symbol interleaving in the two-path model, which is identical to the ideal one-path chip interleaving case. The ideal chip interleaving suggests that without the speech-frame-length limitation, the more the groups of chips per symbol, the better the bit error rate performance. In order to achieve the results as close as the ideal chip interleaving performance under a speech-frame-length constraint, we can use the Rake receiver for an additional 2 dB gain in SNR at 10^{-3} BER.

5.2 Topics for Future Research

We have concentrated our research on using the chip block interleaving to combat fast fading. We could use the convolutional interleaver instead of the block interleaver for the chip interleaving scheme. The convolutional interleaver does not require as much memory as the block interleaver for the chip interleaving process, and it could achieve the same performance as the block interleaver.

We could investigate the impact of imperfect chip synchronization on the BER performance for both the symbol block interleaving and chip interleaving. We could optimize the soft decision decoding metric for the chip interleaving scheme to gain better bit error rate performance.

Other than the Rayleigh fading channel, BER performance of chip interleaving

can be investigated under other environments, for example a Ricean distributed channel. Our research has concentrated on a slowly varying fast fading channel; we could investigate the performance of chip interleaving under a fast varying fast fading channel, i.e. when the channel coherence time is smaller than a symbol duration. This might result from the high speed MS. So that we could investigate the error rate performance under the condition where the maximum Doppler shift is greater than 60 Hz.

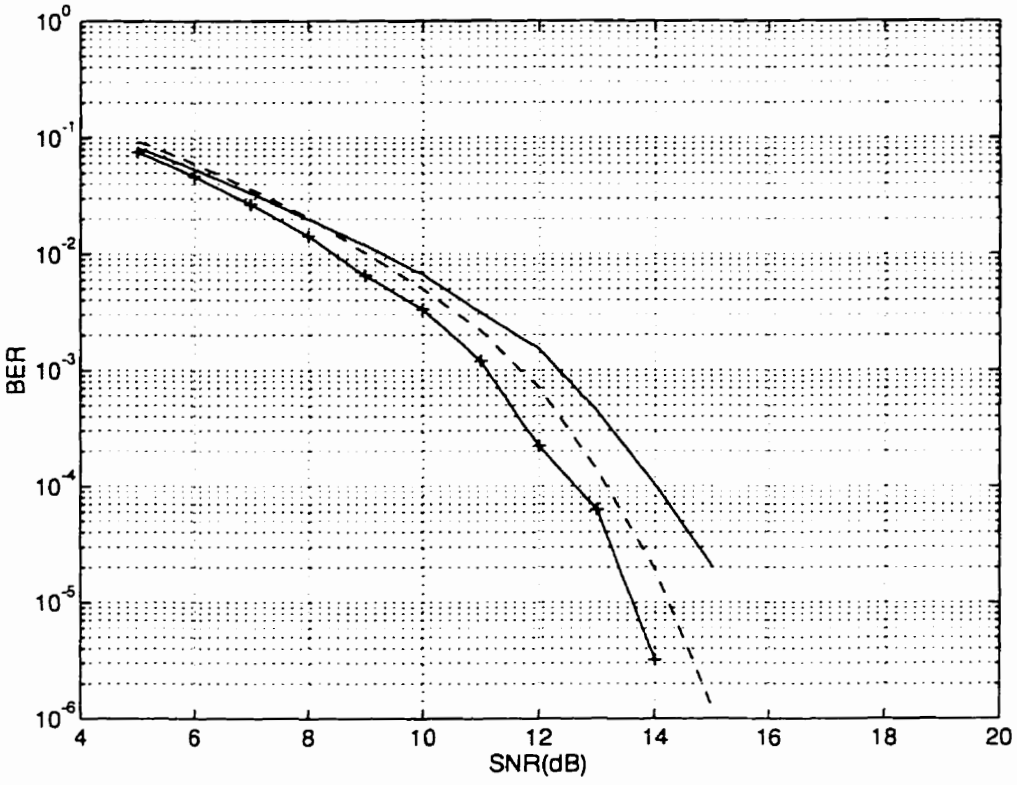


Figure 5.1: One-path model: Comparison between the best hard decision decoding chip interleaving and the soft decision decoding symbol block interleaving. Maximum Doppler shift of 60 Hz.

Legends: Soft decision decoding symbol block interleaving(solid line), and 16 4-chip groups/symbol chip interleaving: hard decision decoding(dash line), soft decision decoding('+').

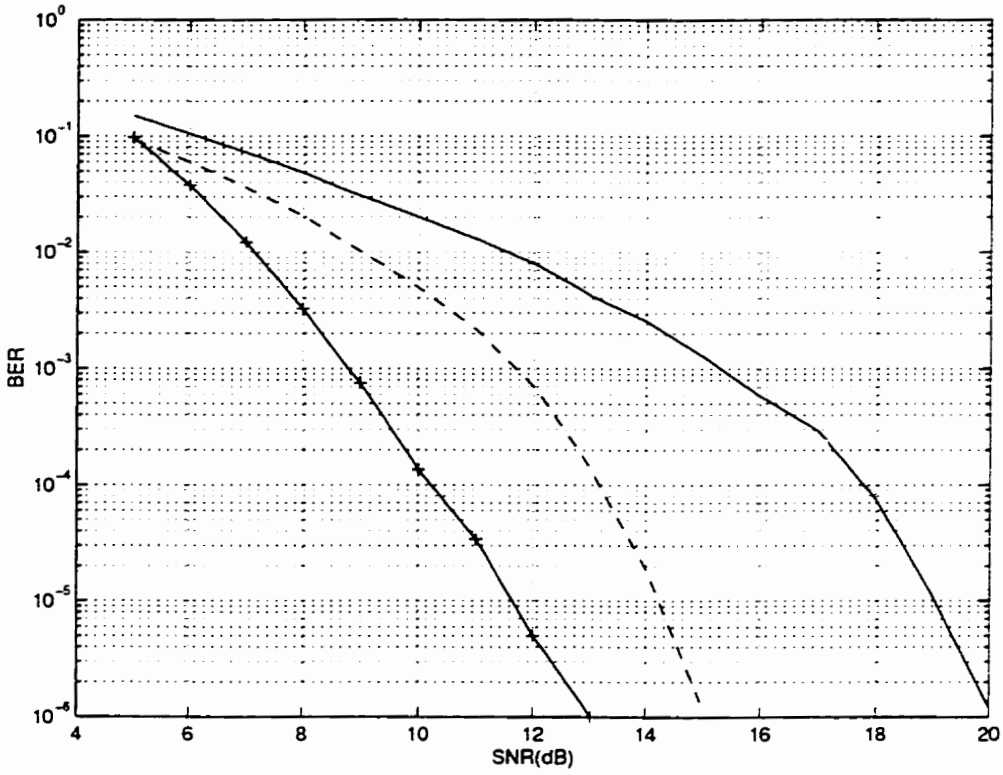


Figure 5.2: Comparison between the 16 4-chip groups/symbol chip interleaving, symbol block interleaving, and the ideal symbol block interleaving. Maximum Doppler shift of 60 Hz. (Hard decision decoding)

Legends: IS-95 symbol interleaving(solid line), 16 4-chip groups/symbol chip interleaving(dash line), and ideal symbol block interleaving('+').

Appendix A

IS-95 Symbol Block Interleaving Algorithm

The length of a speech frame in the forward link of IS-95 is 20 ms. Each speech frame has 192 information bits, and corresponds to 384 symbols in the forward link. The size of the interleaver table is designed to fill 384 symbols. There are four different vocoder rates: 1200 bps, 2400 bps, 4800 bps, and 9600 bps. For vocoder rates which are less than 9600 bps, symbols are repeated to fill up the interleaver table. For 1200 bps, the same symbol is repeated 7 times, for 2400 bps, the same symbol is repeated 3 times, and for 4800 bps, the same symbol is repeated 1 time. The IS-95 block interleaver is shown in Fig.A.1.

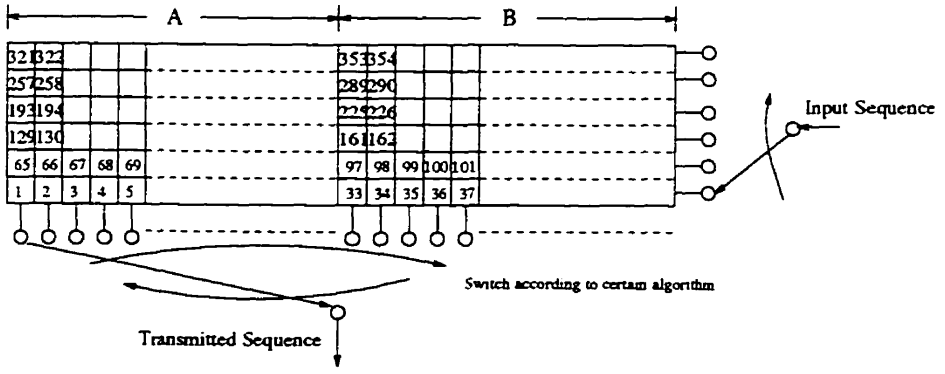


Figure A.1: CDMA Cellular Standard IS-95 Forward Link Block Interleaver

There are two main regions in this table; region A and region B. The read in process is straight forward; the symbols are read in row by row. After the interleaver is full, the read out process switches between region A and region B. For simplicity, column 1 is denoted as col-1. Region A and region B are denoted only as A and B. A-col-1 represents col-1 in region A. First, A-col-1 is read out. Then 32 columns is added to A-col-1, and the switch is pointed to B-col-33. After symbols are read out from B-col-33, B-col-33 subtracts 16 columns and becomes col-17 in A. At this point the read out process has gone through region A and region B, where we represent the process as A B. Next, symbols in A-col-17 are read out, and 32 columns are added to A-col-17, and the switch is in B-col-49. After the symbols are read out, B-col-49 subtracts 40 columns, and becomes A-col-9. At this point, the read out process has gone through A B A B A. The process repeats itself by adding 32 columns, subtracting 16 columns, adding 32 columns, followed by a repetition of the process A B A B. Then 52 columns are subtracted from the current column in B. For the read out process to go through the region A B A B, we call this process a section. The number of adding and subtracting columns are always the same for the first three letters in each section, which are denoted as A B A, as the following, $A+32 \rightarrow B-16 \rightarrow A+32 \rightarrow B-* \rightarrow A+32 \rightarrow B-16 \rightarrow A+32 \rightarrow B-* \rightarrow A...$ $*$ has a fix pattern for all the speech frames.

The order of the columns that the symbols are read out for each speech frame is as follows:(Read from left to right, row after row)

1, 33, 17, 49, 9, 41, 25, 57, 5, 37, 21, 53, 13, 45, 29, 61,

3, 35, 19, 51, 11, 43, 27, 59, 7, 39, 23, 55, 15, 47, 31, 63,

2, 34, 18, 50, 10, 42, 26, 58, 6, 38, 22, 54, 14, 46, 30, 62,

4, 36, 20, 52, 12, 44, 28, 60, 8, 40, 24, 56, 16, 48, 32, 64.

Symbol block interleaving read out algorithm summary:

1. Symbols are read out column by column. Initially, read out from column in region A, followed by region B, then region A, and region B again. The above process is denoted as A B A B, and this is called the first section. The number of columns to be added to or subtracted from the current column are as follows: from A to B add 32 columns to the current column, then from B to A subtract 16 columns form the current column. Again from A to B by adding 32 columns.

Now, the column is again second time at region B.

2. At the second B of the A B A B section, the current column subtracts 40 columns, and switch back to A again. Procedure (1) is repeated. At the second B again, go to procedure (3).

3. At the second B of second section, subtract 52 columns from the current column, and repeats (1). Go to (4).

4. There are a total of 15 (A B A B) sections. At the second B of each section, the current column subtracts the number of columns with respect to the section number, as shown in the following:
   (section number)number of columns:
   (1)40, (2)52, (3)40, (4)58, (5)40, (6)52, (7)40, (8)61, (9)40, (10)52, (11)40, (12)58, (13)40, (14)58, (15)40.

5. The whole procedure is repeated for each new speech frame.

Below shows the IS-95 transmitted symbols at the symbol block interleaver output, the data rate is 9600 bps. The transmitted symbols are read from left to right, top to bottom, column by column. (at the 9600 bps):

1	9	5	13	3	11	7	15	2	10	6	14	4	12	8	16
65	73	69	77	67	75	71	79	66	74	70	78	68	76	72	80
129	137	133	141	131	139	135	143	130	138	134	142	132	140	136	144
193	201	197	205	195	203	199	207	194	202	198	206	196	204	200	208
257	265	261	269	259	267	263	271	258	266	262	270	260	268	264	272
321	329	325	333	323	331	327	335	322	330	326	334	324	332	328	336
33	41	37	45	35	43	39	47	34	42	38	46	36	44	40	48
97	105	101	109	99	107	103	111	98	106	102	110	100	108	104	112
161	169	165	173	163	171	167	175	162	170	166	174	164	172	168	176
225	233	229	237	227	235	231	239	226	234	230	238	228	236	232	240
289	297	293	301	291	299	295	303	290	298	294	302	292	300	296	304
353	361	357	365	355	363	359	367	354	362	358	366	356	364	360	368
17	25	21	29	19	27	23	31	18	26	22	30	20	28	24	32
81	89	85	93	83	91	87	95	82	90	86	94	84	92	88	96
145	153	149	157	147	155	151	159	146	154	150	158	148	156	152	160
209	217	213	221	211	219	215	223	210	218	214	222	212	220	216	224
273	281	277	285	275	283	279	287	274	282	278	286	276	284	280	288
337	345	341	349	339	347	343	351	338	346	342	350	340	348	344	352
49	57	53	61	51	59	55	63	50	58	54	62	52	60	56	64
113	121	117	125	115	123	119	127	114	122	118	126	116	124	120	128
177	185	181	189	179	187	183	191	178	186	182	190	180	188	184	192
241	249	245	253	243	251	247	255	242	250	246	254	244	252	248	256
305	313	309	317	307	315	311	319	306	314	310	318	308	316	312	320
369	377	373	381	371	379	375	383	370	378	374	382	372	380	376	384

Appendix B

Chip Deinterleaving

This appendix shows an example of the chip deinterleaving process for a 4 16-chip groups, with the maximum separation configuration.

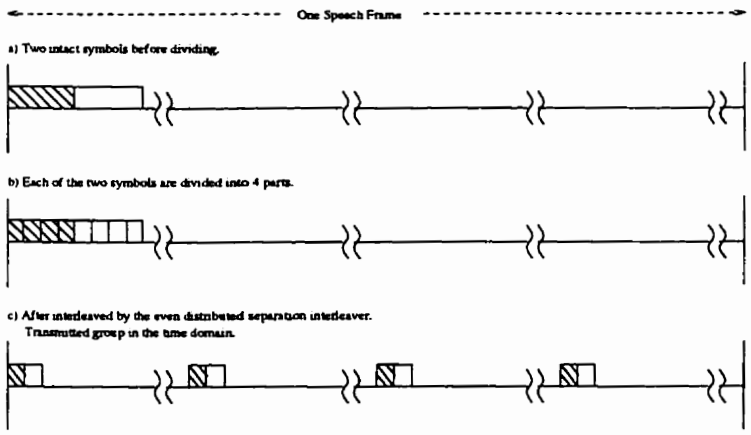


Figure B.1: A maximum separation for 4 16-chip group interleaving in the time scale.

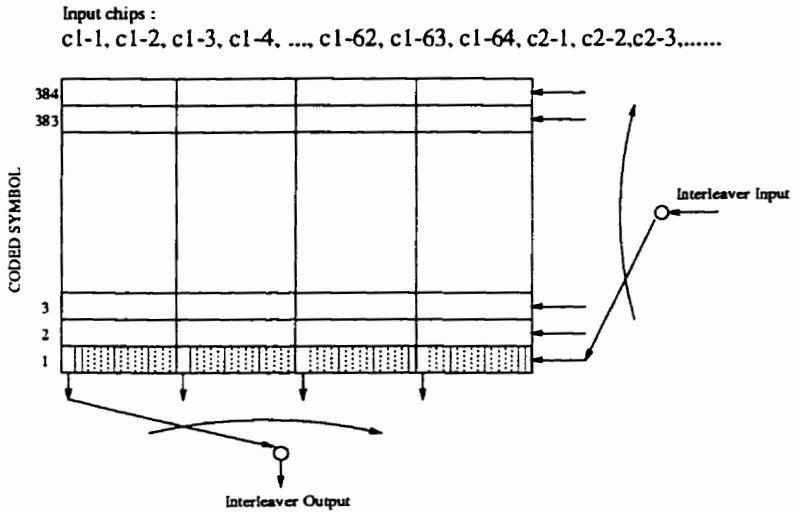


Figure B.2: A maximum separation for 4 16-chip groups chip interleaver.

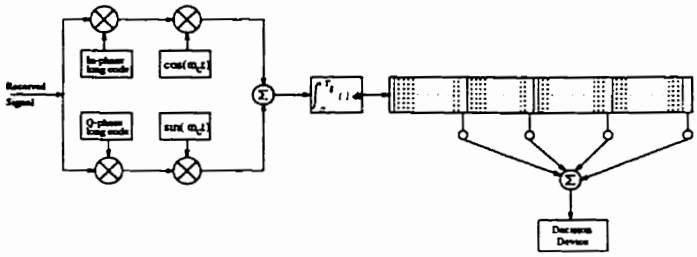


Figure B.3: A chip deinterleaving for 4 16-chip groups at the receiver.

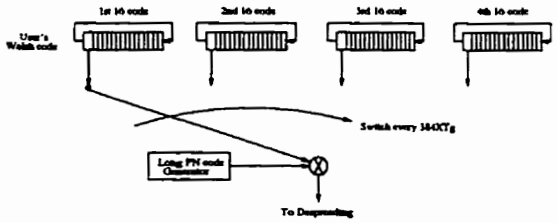


Figure B.4: Long code generation for the 4 16-chip groups maximum separation configuration.

References

[1] A. Mehrotra, *Cellular Radio: Analog and Digital Systems.* Norwood, MA.: Artech House, Inc., 1994.

[2] D. D. Falconer, F. Adachi, and B. Gudmundson, "Time division multiple access methods for wireless personal communications," *IEEE Communications Magazine*, pp. 50–57, Jan. 1995.

[3] W. C. Y. Lee, "Overview of cellular CDMA," in *IEEE Transactions On Vhicular Technology*, vol. 40, pp. 291–302, May 1991.

[4] TIA/EIA/IS-95, *Interim Standard, Telecommunications Industry Association.* July 1993.

[5] J. E. Padgett *et al.*, "Overview of wireless personal communication," *IEEE Communications Magazine*, pp. 28–41, Jan. 1995.

[6] G. L. Stuber and C. Kchao, "Analysis of a multiple cell DS/CDMA cellular mobile radio systems," *IEEE Journal On Selected Areas In Communications*, vol. 10, pp. 669–679, May 1992.

[7] G. L. Turin, "The effects of multipath and fading on the performance of DS/CDMA systems," *IEEE Journal On Selected Areas In Communications*, vol. 2, pp. 597–603, July 1984.

[8] M. B. Pursley *et al.*, "Error probability for DS spread-spectrum multiple-access communication-PartI: Upper and lower bounds," in *IEEE Transaction On Communcation Technology*, vol. 30, pp. 975–984, May 1982.

[9] A. Salmasi and K. S. Gillhousen, "On the system design aspects of code division multiple access (CDMA) applied to digital cellular personal communciations networks," in *IEEE Vehicular Technology Conference*, vol. 41, pp. 57–62, 1991.

[10] S. Ariyavisitakul and L. F. Chang, "Signal and interference statistics of a CDMA system with feedback power control," in *IEEE Transaction On Communcation Technology*, vol. 41, pp. 1626–1634, Nov. 1993.

[11] A. Jalali and P. Mermelstein, "Effects of diversity, power control, and bandwidth on the capacity of microcellular CDMA systems," *IEEE Journal On Selected Areas In Communications*, vol. 12, pp. 952–961, June 1994.

[12] G. E. Bottomley, "Optimizing the rake receiver for the CDMA downlink," in *IEEE Vehicular Technology Conference*, vol. 43, pp. 742–745, 1993.

[13] F. Ling and D. D. Falconer, "Combined orthogonal/convolutional coding for digital cellular CDMA system," in *IEEE Vehicular Technology Conference*, vol. 42, pp. 63–66, 1992.

[14] D. C. Cox, "Delay doppler characteristic of multipath propagation at 910 MHz in a suburban mobile radio environment," in *IEEE Transaction on Antenna and Propagation*, vol. AP-20, pp. 625–634, September 1972.

[15] W. D. Rummler, R. P. Coutts, and M. Liniger, "Multipath fading channel models for microwave digital radio," *IEEE Communications Magazine*, vol. 24, pp. 30–42, November 1986.

[16] E. Lutz, "Code and interleaver design for data transmission over fading channels," in *Proceeding Globecomm*, pp. 381–386, 1984.

[17] G. C. Hess, *Land-Mobile Radio System Engineering*. Boston: Artech House, Inc., 1993.

[18] G. D. Forney, Jr., "Burst correction codes for the classic bursty channel," in *IEEE Transaction On Communcation Technology*, vol. com-19, pp. 772–781, October 1971.

[19] J. L. Ramsey, "Realization of optimum interleavers," in *IEEE Transaction on Information Theory*, vol. IT-16, pp. 338–345, 1970.

[20] D. R. Martin and P. L. McAdam, "Convolutional code performance with optimal jamming," in *ICC*, pp. 4.3.1.–4.3.7, 1980.

[21] D. J. Torrieri, "Performance of direct-sequence with long pseudonoise sequence," *IEEE Journal On Selected Areas In Communications*, vol. 10, pp. 770–781, May 1992.

[22] E. G. Strom, S. Parkvall, S. L. Miller, and B. E. Ottersten, "DS-CDMA synchronization in time-varying fading channels," *IEEE Journal On Selected Areas In Communications*, vol. 14, pp. 1636–1642, October 1996.

[23] V. M. DaSilva and E. S. Sousa, "Effect of multipath propagation on the forward link of a CDMA cellular system," in *Wireless Personal Communications*, vol. 1, pp. 33–41, Kluwer Academic, 1994.

[24] S. B. Wicker, *Error Control Systems: for Digital Communication and Storage*. Englewood Cliffs, N. J.: Prentice Hall, 1995.

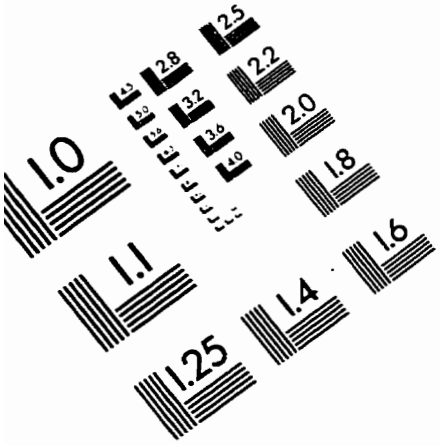
[25] S. Lin and D. J. Costello, Jr., *Error Control Coding:Fundamentals and Applications*. Englewood Cliffs, N. J.: Prentice-Hall, Inc., 1983.

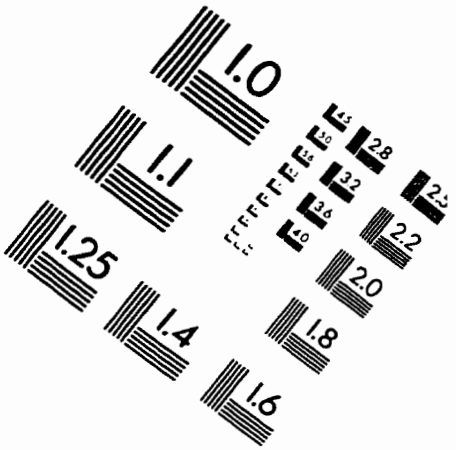
[26] J. A. Heller and I. M. Jacobs, "Viterbi decoding for satellite and space communication," in *IEEE Transaction On Communcation Technology*, vol. com-19, pp. 835–848, October 1971.

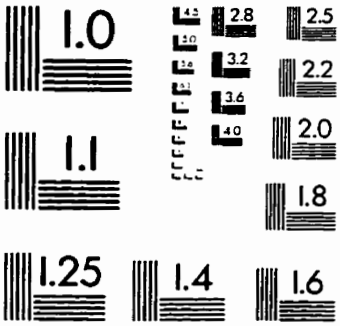
[27] W. C. J. Jr., *Microwave Mobile Communications*. New York: Wiley, Inc., 1974.

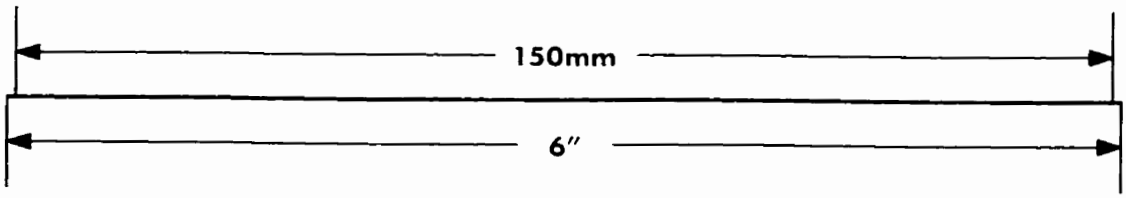
[28] S. A. Hanna, "Convolutional interleaving for digital radio communications," in *ICUPC*, pp. 443–447, 1993.

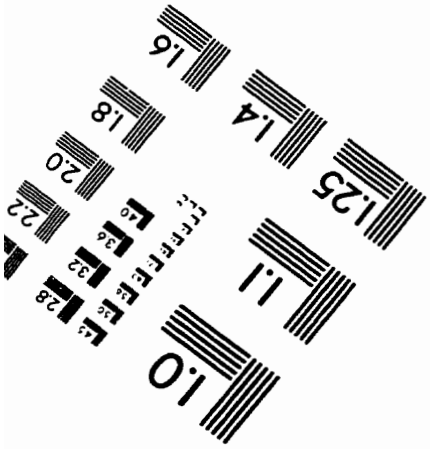
IMAGE EVALUATION TEST TARGET (QA-3)











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