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United States Patent [19]

Brey et al.

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[11]

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[54]	EXCESSIVE ERROR CORRECTION	ĺ
	CONTROL	

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[51] **U.S. Cl.** **371/40.1;** 371/13; [52]

371/21.6 Field of Search 371/13, 40.1, 40.2, 371/21.6; 395/575

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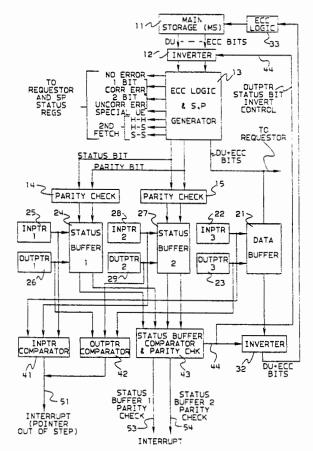
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Primary Examiner-Charles E. Atkinson Attorney, Agent, or Firm-Bernard M. Goldman

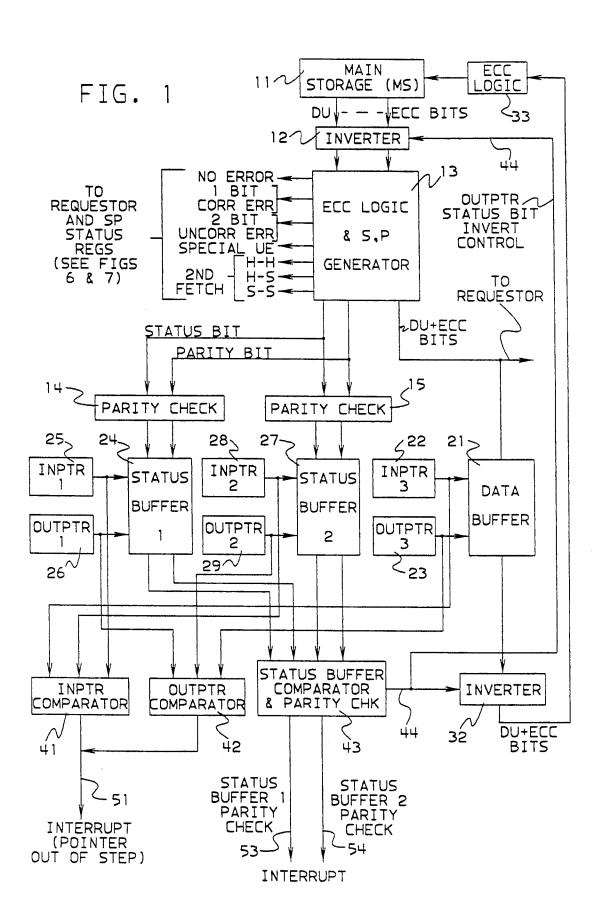
ABSTRACT [57]

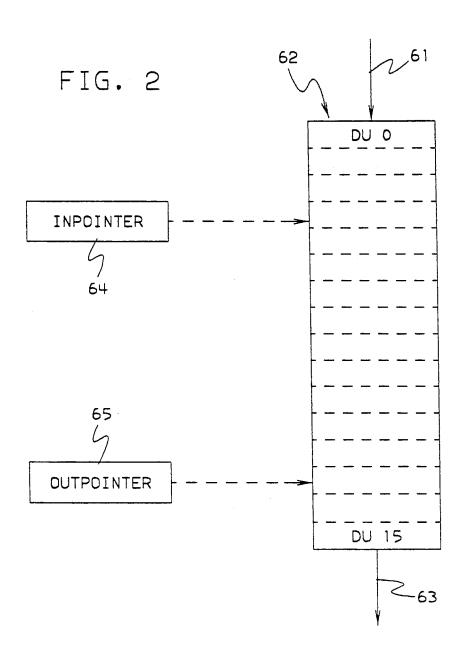
A method of automatically invoking a recoverable and fault tolerant implementation of the complemented/recomplemented (C/R) error correction method without the assistance of a service processor when an excessive error is detected in main storage (MS) by ECC logic circuits. An excessive error is not correctable by the ECC. These novel changes to the C/R method increase its effectiveness and protect the C/R hardware against random failure. Further, if an excessive error is corrected in a page in MS, an excessive error reporting process is provided for controlling the reporting using a storage map to determine if a previous correction in that page has been reported. If it has been reported, then no further reporting of soft excessive errors is made for that page. A service processor is signaled in parallel to update its persistent copy of the storage map so that on a next initializations of MS the memory map can be restored in the memory. The memory map is used to assist the repair of failing parts of MS, and is reset after MS is repaired.

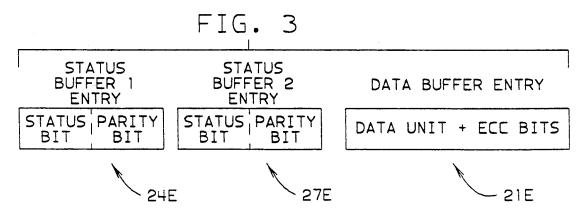
24 Claims, 7 Drawing Sheets













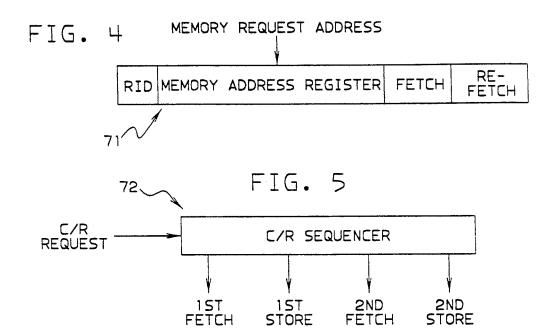
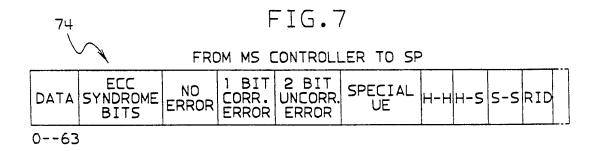


FIG. 6 FROM MS CONTROLLER TO REQUESTOR PROCESSOR OR I/O BIT SPECIAL NO EXCESS. CORR. ERROR H-HH-S|S-S|RID DATA **ERROR ERROR** UE 0---63. 1 1 1 1 1 1 1 1



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FIG. 8

1. REQUESTOR REQUESTS DATA LINE

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- 2. FETCH ALL DU+ECC GROUPS IN REQUESTED DATA LINE FROM MS
- 3. GENERATE STATUS INFORMATION FOR EACH DU+ECC GROUP (INDICATE ANY EXCESSIVE ERROR FOR ANY GROUP)
 - 4. SEND EACH FETCHED DU+ECC GROUP WITH ITS STATUS INFORMATION TO ITS REQUESTOR



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