Petitioner Bluehouse Global Ltd.

Ex. 1002

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	: 9,298,057 B2
APPLICATION NO.	: 13/939323
DATED	: March 29, 2016
INVENTOR(S)	: Yasuharu Hosaka et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the specification,

At column 26, lines 59-60, "terminal Note" should be --terminal. Note--;

At column 29, line 40, "1.5 μm-thick" should be --1.5-μm-thick--;

At column 30, line 5, "lam" should be --μm--;

In the claims,

In claim 12, column 32, line 36, "in the second insulating film" should be --in the second insulating film,--.

Signed and Sealed this
Twelfth Day of July, 2016

Michelle K. Lee

Michelle K. Lee
Director of the United States Patent and Trademark Office

Attorney Docket No. 0756-10194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 2340
Yasuharu HOSAKA et al.	)	Group Art Unit: 2871
U.S. Patent No. 9,298,057	)	Examiner: Richard H. Kim
Serial No. 13/939,323	)	
Filed: July 11, 2013	)	
For: DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	)	

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. § 1.322 FOR CORRECTION OF OFFICE MISTAKE

ATTN: Certificate of Correction Branch
Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

As provided in detail in the attached, the patentee respectfully requests that a Certificate of Correction be granted in the above-identified patent to correct a mistake in a patent, incurred through the fault of the Office.

Under 37 C.F.R. 1.322, "The Commissioner may issue a certificate of correction pursuant to 35 U.S.C. 254 to correct a mistake in a patent, incurred through the fault of the Office, which mistake is clearly disclosed in the records of the Office at the request of the patentee or the patentee's assignee."

The patentee furthermore requests Expedited Issuance of this Certificate of Correction in accordance with MPEP § 1480.01. Specifically, this section provides that:

> In an effort to reduce the overall time required in processing and granting Certificate of Correction requests, the Office will expedite processing and granting of patentee requests where such requests are

> accompanied by evidence to show that the error is attributable solely to the Office . . . . Where the correction requested was incurred through the fault of the Office, and the matter is clearly disclosed in the records of the Office, and is accompanied by documentation that unequivocally supports the patentee's assertion(s), a Certificate of Correction will be expeditiously issued. MPEP § 1480.01

The following errors appear to have occurred through the fault of the Office, and the patentee respectfully requests correction thereof.

At column 26, lines 59-60, "terminal Note" should be --terminal. Note--;

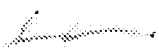
At column 29, line 40, "1.5 μm-thick" should be --1.5-μm-thick--;

At column 30, line 5, "lam" should be --μm--;

In claim 12, column 32, line 36, "in the second insulating film" should be --in the second insulating film,--.

The corrections in the specification and claim 12 (original claim 21) are directed to mistakes in the patent incurred through the fault of the Office, possibly resulting from the Office's document scanning processes. As the errors were incurred through the fault of the Office, a fee is not believed to be necessary. Should it be determined that a fee is necessary, any deficiencies or overages in any fees due in connection with this patent and the requested actions should be applied to Deposit Account No. 50-2280.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO : 9,298,057

DATED : March 29, 2016

INVENTOR(S) : Yasuharu HOSAKA et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At column 26, lines 59-60, "terminal Note" should be --terminal. Note--;

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At column 30, line 5, "lam" should be --μm--;

In claim 12, column 32, line 36, "in the second insulating film" should be --in the second insulating film,--.

MAILING ADDRESS OF SENDER:

Eric J. Robinson
Robinson Intellectual Property Law Office
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033

PATENT NO. 9,298,057

No. of additional copies

Electronic Acknowledgement Receipt

EFS ID:	25963489
Application Number:	13939323
International Application Number:	
Confirmation Number:	2340
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu HOSAKA
Customer Number:	31780
Filer:	Eric J. Robinson/Sulma Portillo
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10194
Receipt Date:	03-JUN-2016
Filing Date:	11-JUL-2013
Time Stamp:	14:22:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	COC_03JUNE2016.pdf	30083 d209c2a9b2b8607615fc66ce1f759c53f8e6edbb	no	3

Warnings:	
Information:	

Total Files Size (in bytes):	30083

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/939,323	03/29/2016	9298057	0756-10194	2340

31780 7590 03/09/2016

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 50 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Semiconductor Energy Laboratory Co., Ltd., Atsugi-shi, JAPAN;
Yasuharu HOSAKA, Tochigi, JAPAN;
Yukinori SHIMA, Tatebayashi, JAPAN;
Kenichi OKAZAKI, Tochigi, JAPAN;
Shunpei YAMAZAKI, Setagaya, JAPAN;

Document Description: Issue Fee Payment (PTO-85B)

Issue Fee Transmittal Form

Application Number	Filing Date	First Named Inventor	Atty. Docket No.	Confirmation No.
13939323	11-Jul-2013	Yasuharu HOSAKA	0756-10194	2340

TITLE OF INVENTION :

DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

Entity Status	Application Type	Art Unit	Class - Subclass	EXAMINER
Regular Undiscounted	Utility under 35 USC 111(a)	2871	043000	RICHARD KIM

Issue Fee Due	Publication Due	Total Fee(s) Due	Date Due	Prev. Paid Fee
$960	$0	$960	19-Feb-2016	$0

1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

Current Correspondence Address:	Current Indicated Fee Address :
31780 Robinson Intellectual Property Law Office, P.C. 3975 Fair Ridge Drive Suite 20 North Fairfax VA 22033 UNITED STATES 571-434-6789 erobinson@riplo.com	
☐ Change of correspondence address requested, system generated AIA/122-EFS form attached	☐ Fee Address indication requested, system generated SB/47-EFS form attached

2.Entity Status

Change in Entity Status

○ Applicant certifying micro entity status; system generated Micro Entity certification form attached. See 37 CFR 1.29.
Note: Absent a valid certification of micro entity status, issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. If this box is checked, you will be prompted to choose a micro entity status on the gross income basis (37 CFR 1.29(a)) or the institution of higher education basis (37 CFR 1.29(d)), and make the applicable certification online.

○ Applicant asserting small entity status. See 37 CFR 1.27.
Note: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

◉ Applicant changing to regular undiscounted fee status.
Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

Document Description: Issue Fee Payment (PTO-85B)

3.The Following Fee(s) Are Submitted:

☒ Issue Fee

☐ I authorize USPTO to apply my previously paid issue fee to the current fees due

☐ Publication Fee

☐ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number _____

☒ Advance Order - # of copies 2

☒ If **in addition to** the payment of the issue fee amount submitted with this form, there are any discrepancies in any amount(s) due, the Director is authorized to charge any deficiency or credit any overpayment, to Deposit Account Number 50-2280 . The **issue fee must be submitted** with this form. **If payment of the issue fee does not accompany this form, checking this box and providing a deposit account number will NOT be effective to satisfy full payment of the fee(s) due.**

4.Firm and/or Attorney Names To Be Printed

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

1. ROBINSON INTELLECTUAL PROPERTY LAW OFFICE
2. ERIC J. ROBINSON
3.

5.Assignee Name(s) and Residence Data To Be Printed

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

Name	City	State	Country	Category
Semiconductor Energy Laboratory Co., Ltd.	Kanagawa-ken		japan	corporation

6.Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

Signature	/Eric J. Robinson/	**Date**	02-19-2016
Name	Eric J. Robinson	**Registration Number**	38285

Electronic Patent Application Fee Transmittal

Application Number:	13939323
Filing Date:	11-Jul-2013
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu HOSAKA
Filer:	Eric J. Robinson/Sue Ann Carr
Attorney Docket Number:	0756-10194

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility Appl Issue Fee	1501	1	960	960
Publ. Fee- Early, Voluntary, or Normal	1504	1	0	0
Printed Copy of Patent - No Color	8001	2	3	6
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**966**

Electronic Acknowledgement Receipt

EFS ID:	24925623
Application Number:	13939323
International Application Number:	
Confirmation Number:	2340
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu HOSAKA
Customer Number:	31780
Filer:	Eric J. Robinson/Sue Ann Carr
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10194
Receipt Date:	19-FEB-2016
Filing Date:	11-JUL-2013
Time Stamp:	07:31:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$966
RAM confirmation Number	7440,7441
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Web85b.pdf	46334 29b1790973c1933ebcd9d8c4e219072ea24c1326	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	35568 edf12b5d6f7e688b42052f84b28312de14785e36	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	81902		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

31780 7590 11/19/2015

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

EXAMINER
KIM, RICHARD H

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/19/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/939,323	07/11/2013	Yasuharu HOSAKA	0756-10194	2340

TITLE OF INVENTION: DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/19/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31780 7590 11/19/2015
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/939,323	07/11/2013	Yasuharu HOSAKA	0756-10194	2340

TITLE OF INVENTION: DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/19/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
KIM, RICHARD H	2871	349-043000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/939,323	07/11/2013	Yasuharu HOSAKA	0756-10194	2340

31780 7590 11/19/2015

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

EXAMINER	
KIM, RICHARD H	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/19/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/939,323	Applicant(s) HOSAKA ET AL.	
	Examiner RICHARD KIM	Art Unit 2871	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/3/15*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-9 and 21-38*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/3/15 has been entered.

Allowable Subject Matter

3. Claims 1-9 and 21-38 allowed.

4. The following is an examiner's statement of reasons for allowance: the prior art of record, taken alone or in combination, fails to teach or disclose, in light of the specifications, **claim 1)** a display device wherein the third insulating film is in an opening provided in the second insulating film; **claim 21)** a display device wherein the third insulating film is in an opening provided in the second insulating film; and **claim 27)** a display device wherein an edge portion of the second insulating film overlaps with the third insulating film, and wherein the third insulating film is not provided in the driver circuit portion.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD KIM whose telephone number is (571)272-2294. The examiner can normally be reached on 9:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Caley can be reached on 571-272-2286. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RICHARD KIM/
Primary Examiner, Art Unit 2871

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 2340

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/939,323	07/11/2013	349	2871	0756-10194

APPLICANTS

Semiconductor Energy Laboratory Co., Ltd., Atsugi-shi, JAPAN;

INVENTORS

Yasuharu HOSAKA, Tochigi, JAPAN;
Yukinori SHIMA, Tatebayashi, JAPAN;
Kenichi OKAZAKI, Tochigi, JAPAN;
Shunpei YAMAZAKI, Setagaya, JAPAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

JAPAN 2012-161344 07/20/2012

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

07/26/2013

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /RICHARD H KIM/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	11	20	2

ADDRESS

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033
UNITED STATES

TITLE

DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

FILING FEE RECEIVED		
2160	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13939323	HOSAKA ET AL.
	Examiner	**Art Unit**
	RICHARD KIM	2871

CPC						
Symbol					**Type**	**Version**
G02F		1	/	1368	F	2013-01-01
G02F		1	/	133345	A	2013-01-01
H01L		27	/	1214	I	2013-01-01
H01L		27	/	1225	I	2013-01-01
H01L		27	/	1248	I	2013-01-01
G02F		1	/	13454	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	27	
/RICHARD KIM/ Primary Examiner.Art Unit 2871	11/15/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13939323	HOSAKA ET AL.
	Examiner	**Art Unit**
	RICHARD KIM	2871

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		G	0	2	F	1 / 1345 (2006.01.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	27	
/RICHARD KIM/ Primary Examiner.Art Unit 2871	11/15/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13939323	HOSAKA ET AL.
	Examiner	**Art Unit**
	RICHARD KIM	2871

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		17	10	33										
2	2		18	11	34										
3	3		19	18	35										
4	4		20	19	36										
5	5	12	21	26	37										
6	6	13	22	27	38										
7	7	14	23												
8	8	15	24												
9	9	16	25												
	10	17	26												
	11	20	27												
	12	21	28												
	13	22	29												
	14	23	30												
	15	24	31												
	16	25	32												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	27	
/RICHARD KIM/ Primary Examiner.Art Unit 2871	11/15/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S178	1602	((G02F1/133345).CPC. and ((thin adj film adj transistor) tft))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/12 17:19
S181	797	S180 and driv$5	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/12 17:20
S180	835	(349/151).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/12 17:20
S179	1423	((G02F1/134363).CPC. and ffs)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/12 17:20
S182	3053	((G02F1/13454).CPC.)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/12 17:22
S183	2863	((G02F1/13454).CPC. and @ad<"20130720")	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/12 17:23
S184	206	((G02F1/13454).CPC. and @ad<"20130720" and (third adj (passivat$5 insulat$5)))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/12 17:24
S185	164	((G02F1/133345).CPC. and S182)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/12 18:16
S186	8	("20110068334" | "20110095299" | "20130321726" | "20140078440" | "7142260" | "8189130" | "8592814" | "8791458").PN. OR ("9146429").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/12 18:17
S187	243	("3967882" | "4390245" | "4775225" | "4844597" | "5148301" | "5338240" | "5381255" | "5537235" | "5566013" | "5739888" | "5880803").PN. OR ("6163357").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/12 18:25
S188	120	("20010046027" | "20020056838" |	US-	OR	ON	2015/11/12

		"20020132454" | "20030137621" | "20030189401" | "20030218222" | "20040038446" | "20040127038" | "20050017302" | "20050088589" | "20050199959" | "20060012729" | "20060035452" | "20060043377" | "20060091793" | "20060108529" | "20060108636" | "20060110867" | "20060113536" | "20060113539" | "20060113549" | "20060113565" | "20060169973" | "20060170111" | "20060197092" | "20060208977" | "20060228974" | "20060231882" | "20060238135" | "20060244107" | "20060284171" | "20060284172" | "20060292777" | "20070024187" | "20070046191" | "20070052025" | "20070054507" | "20070072439" | "20070090365" | "20070108446" | "20070152217" | "20070172591" | "20070187678" | "20070187760" | "20070194379" | "20070252928" | "20070272922" | "20070287296" | "20080006877" | "20080038882" | "20080038929" | "20080050595" | "20080073653" | "20080083950" | "20080106191" | "20080128689" | "20080129195" | "20080166834" | "20080182358" | "20080224133" | "20080254569" | "20080258139" | "20080258140" | "20080258141" | "20080258143" | "20080296568" | "20080308796" | "20080308797" | "20080308804" | "20080308805" | "20080308806" | "20090008639" | "20090068773" | "20090073325" | "20090114910" | "20090134399" | "20090152506" | "20090152541" | "20090239335" | "20090278122" | "20090280600" | "20090305461" | "20100051937" | "20100065844" | "20100092800" | "20100109002" | "20100136743" | "20110102697" | "5731856" | "5744864" | "6294274" | "6489952" | "6563174" | "6635505" | "6727522").PN. OR ("6847422" | "7049190" | "7061014" | "7064346" | "7105868" | "7198967" | "7211825" | "7282782" | "7297977" | "7298437" | "7323356" | "7385224" | "7402506" | "7411209" | "7453065" | "7453087" | "7462862" | "7468304" | "7501293" | "7544981" | "7674650" | "7732819").PN. OR ("8592814").URPN.	PGPUB; USPAT; USOCR			18:37
S189	1	("20020084459").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/12 20:09
S190	566	((G02F1/13454).CPC. and @ad<"20130720" and (second adj insulat$5))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/12 21:03

S191	206	((G02F1/13454).CPC. and @ad<"20130720" and (third adj (passivat$5 insulat$5)))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/13 17:16
L1	20147	(g02f1/1368 h01l27/1214 h01l27/1225 h01l27/1248 g02f1/1354).cpc.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/15 20:56
L3	1903	((G02F1/1368 OR H01L27/1248 OR H01L27/1214 OR H01L27/1255).CPC.) and (third adj (insulat$5 passivat$5))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/15 20:58
L2	18653	((G02F1/1368 OR H01L27/1248 OR H01L27/1214 OR H01L27/1255).CPC.)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/15 20:58
L5	925	((G02F1/1368 OR H01L27/1248 OR H01L27/1214 OR H01L27/1255).CPC.) and (third adj (insulat$5 passivat$5)) and ((driv$5 peripher$5) near5 (TFT transistor)) and @ad<"20120720"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/15 20:59
L4	1192	((G02F1/1368 OR H01L27/1248 OR H01L27/1214 OR H01L27/1255).CPC.) and (third adj (insulat$5 passivat$5)) and ((driv$5 peripher$5) near5 (TFT transistor))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/15 20:59
L6	4714	((G02F1/1368 OR H01L27/1248 OR H01L27/1214 OR H01L27/1255).CPC.) and ((opening hole) near5 (insulat$5 passivat$5)) and ((driv$5 peripher$5) near5 (TFT transistor)) and @ad<"20120720"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/15 21:25
L7	2130	((G02F1/1368 OR H01L27/1248 OR H01L27/1214 OR H01L27/1255).CPC.) and ((opening hole) near5 (insulat$5 passivat$5) near5 (second third)) and ((driv$5 peripher$5) near5 (TFT transistor)) and @ad<"20120720"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/15 21:26
L9	2313	((G02F1/133345).CPC.)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/11/15 21:53

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	0	(third adj insulating adj film adj3 opening adj provided).clm.	US-PGPUB; USPAT	OR	ON	2015/11/15 21:53

11/ 15/ 2015 10:00:57 PM
C:\ Users\ rkim3\ Documents\ EAST\ Workspaces\ 13939323.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13939323	HOSAKA ET AL.
	Examiner	Art Unit
	RICHARD KIM	2871

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search attached	1/12/2015	RHK
EAST search attached	7/31/2015	RHK
EAST search attached	11/15/2015	RHK

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	PGPUB claim language search	11/15/2015	RHK

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	13/939,323	Filing Date	2013-07-11	Docket Number (if applicable)	0756-10194	Art Unit	2871
First Named Inventor	Yasuharu HOSAKA et al.			Examiner Name	Richard H. Kim		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 502280

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Signature of Registered U.S. Patent Practitioner			
Signature	/Eric J. Robinson/	Date (YYYY-MM-DD)	2015-11-03
Name	Eric J. Robinson	Registration Number	38285

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Attorney Docket No. 0756-10194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 2340
Yasuharu HOSAKA et al.	)	Group Art Unit: 2871
Serial No. 13/939,323	)	Examiner: Richard H. Kim
Filed: July 11, 2013	)	
For: DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	)	

AMENDMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action dated August 6, 2015, please consider the following amendments and remarks in connection with the above-identified application.

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks begin on page 9 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A display device comprising:

a pixel portion comprising:

a first transistor;

a first insulating film over the first transistor;

a second insulating film over the first insulating film;

a third insulating film covering the second insulating film; and

a first electrode over the third insulating film, the first electrode being electrically connected to the first transistor; and

a driver circuit portion comprising:

a second transistor;

the first insulating film over the second transistor; and

the second insulating film over the first insulating film,

wherein the third insulating film is in a opening provided in the second insulating film,

wherein the first insulating film comprises an inorganic insulating material,

wherein the second insulating film comprises an organic insulating material,

wherein the third insulating film comprises an inorganic insulating material, and

wherein an edge portion of the second insulating film overlaps with the third insulating film.

2. (Previously Presented) The display device according to claim 1 further comprising:

a second electrode over the first electrode;

a fourth insulating film over the second electrode;

a colored film over the fourth insulating film; and

a light-blocking film over the fourth insulating film.

3. (Original) The display device according to claim 1,

wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a Ga-Zn-based metal oxide film.

4. (Original) The display device according to claim 1,

wherein the second insulating film is any of an acrylic-based resin, a polyimide-based resin, a benzocyclobutene-based resin, a polyamide-based resin, and an epoxy-based resin.

5. (Original) The display device according to claim 1,

wherein the third insulating film is any of a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

6. (Original) The display device according to claim 1,

wherein the first transistor and the second transistor each comprises an oxide semiconductor layer.

7. (Original) The display device according to claim 6,

wherein the oxide semiconductor layer comprises any of indium and zinc.

8. (Original) The display device according to claim 6,

wherein the oxide semiconductor layer has a first oxide semiconductor film and a second oxide semiconductor film.

9. (Original) An electronic device comprising the display device according to claim 1.

10.-20. (Canceled)

21. (Currently Amended) A display device comprising:

a pixel portion comprising:

a first transistor;

a first insulating film over the first transistor;

a second insulating film over the first insulating film;

a third insulating film covering the second insulating film;

a first electrode over the third insulating film, the first electrode being electrically connected to the first transistor; and

a liquid crystal layer over the first electrode; and

a driver circuit portion comprising:

a second transistor;

the first insulating film over the second transistor; and

the second insulating film over the first insulating film,

wherein the third insulating film is in an opening provided in the second insulating film,

wherein the first insulating film comprises an inorganic insulating material,

wherein the second insulating film comprises an organic insulating material,

wherein the third insulating film comprises an inorganic insulating material, and

wherein an edge portion of the second insulating film overlaps with the third insulating film.

22. (Previously Presented) The display device according to claim 21, further comprising:

a first alignment film over the first electrode;

a second alignment film over the liquid crystal layer;

a second electrode over the second alignment film;

a fourth insulating film over the second electrode;

a colored film over the fourth insulating film; and

a light-blocking film over the fourth insulating film.

23. (Previously Presented) The display device according to claim 21,

wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a Ga-Zn-based metal oxide film.

24. (Previously Presented) The display device according to claim 21,

wherein the third insulating film is any of a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

25. (Previously Presented) The display device according to claim 21,

wherein the first transistor and the second transistor each comprises an oxide semiconductor layer.

26. (Previously Presented) An electronic device comprising the display device according to claim 21.

27. (Previously Presented) A display device comprising:

a pixel portion comprising:

a first transistor;

a first insulating film over the first transistor;

a second insulating film over the first insulating film;

a third insulating film covering the second insulating film;

a first electrode over the third insulating film, the first electrode being electrically connected to the first transistor; and

a liquid crystal layer over the first electrode; and

a driver circuit portion comprising:

a second transistor;

the first insulating film over the second transistor; and

the second insulating film over the first insulating film;

wherein the first insulating film comprises an inorganic insulating material,

wherein the second insulating film comprises an organic insulating material,

wherein the third insulating film comprises an inorganic insulating material,

wherein an edge portion of the second insulating film overlaps with the third insulating film, and

wherein the third insulating film is not provided in the driver circuit portion.

28. (Previously Presented) The display device according to claim 27, further comprising:

a first alignment film over the first electrode;

a second alignment film over the liquid crystal layer;

a second electrode over the second alignment film;

a fourth insulating film over the second electrode;

a colored film over the fourth insulating film; and

a light-blocking film over the fourth insulating film.

29. (Previously Presented) The display device according to claim 27,

wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a Ga-Zn-based metal oxide film.

30. (Previously Presented) The display device according to claim 27,

wherein the third insulating film is any of a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

31. (Previously Presented) The display device according to claim 27,

wherein the first transistor and the second transistor each comprises an oxide semiconductor layer.

32. (Previously Presented) An electronic device comprising the display device according to claim 27.

33. (Previously Presented) The display device according to claim 1,

wherein an edge portion of the first insulating film overlaps with the third insulating film.

34. (Previously Presented) The display device according to claim 1,

wherein the first transistor and the second transistor each comprises a gate insulating film, a source electrode, and a drain electrode, and

wherein bottom surfaces of the source electrode and the drain electrode are in contact with a top surface of the gate insulating film.

35. (Previously Presented) The display device according to claim 21,

wherein an edge portion of the first insulating film overlaps with the third insulating film.

36. (Previously Presented) The display device according to claim 21,

wherein the first transistor and the second transistor each comprises a gate insulating film, a source electrode, and a drain electrode, and

wherein bottom surfaces of the source electrode and the drain electrode are in contact with a top surface of the gate insulating film.

37. (Previously Presented) The display device according to claim 27,

wherein an edge portion of the first insulating film overlaps with the third insulating film.

38. (Previously Presented) The display device according to claim 27,

wherein the first transistor and the second transistor each comprises a gate insulating film, a source electrode, and a drain electrode, and

wherein bottom surfaces of the source electrode and the drain electrode are in contact with a top surface of the gate insulating film.

REMARKS

The Official Action mailed August 6, 2015, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Filed concurrently herewith is a *Request for Continued Examination*. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on July 11, 2013; September 19, 2013; November 12, 2013; December 2, 2014 and April 21, 2015.

Claims 1-9 and 21-38 are pending in the present application, of which claims 1, 21 and 27 are independent. The Applicant notes with appreciation the allowance of claims 27-32, 37 and 38. Claims 1 and 21 have been amended to better recite the features of the present invention. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

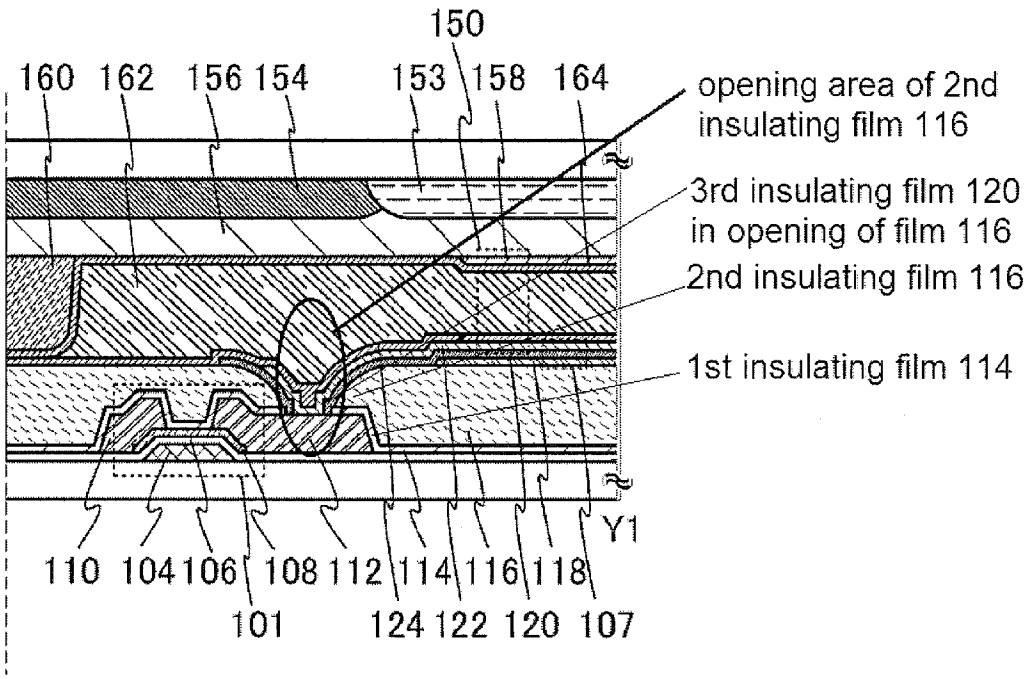
Paragraph 3 of the Official Action rejects claims 1-5, 9, 21-24, 26 and 33-36 as obvious based on U.S. Patent No. 8,988,623 to Koyama. Paragraph 12 of the Official Action rejects claims 6, 7 and 25 as obvious based on the combination of Koyama and U.S. Publication No. 2012/0013817 to Kim. Paragraph 16 of the Official Action rejects claim 8 as obvious based on the combination of Koyama, Kim and U.S. Publication No. 2011/0157252 to Yamazaki. The Applicant respectfully traverses the rejections because a *prima facie* case of obviousness cannot be maintained against the independent claims of the present application, as amended.

As stated in MPEP §§ 2142-2144.04, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some reason to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

With respect to independent claims 1 and 21, the prior art, either alone or in combination, does not teach or suggest all the features of the independent claims, as amended. Specifically, rejected independent claims 1 and 21 have been revised to add the limitation that "the third insulating film is in an opening provided in the second insulating film," as supported by at least Applicant's FIG. 2A, a portion of which is annotated below.

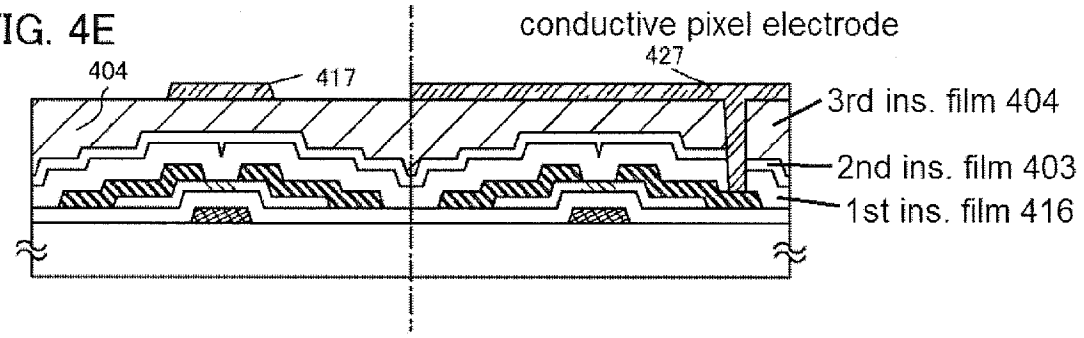
PORTION OF FIG. 2A



Koyama does not teach or suggest the added feature. The Patent Office relies on FIGS. 4A-4E and alleges that Koyama discloses a first insulating film 416, a second insulating film 403, and a third insulating film 404. However, as shown by asserted FIG. 4E of Koyama annotated below, to the extent that the alleged second insulating film 403 has an opening therein, the alleged third insulating film 404 is not "in" such an opening. Rather, it is conductive pixel electrode 427 that is provided into such an opening. For at least this reason, a *prima facie* case of obviousness cannot be maintained.

KOYAMA

FIG. 4E



Moreover, in the claimed invention, the second insulating film is formed using an organic insulating material with which the planarity is improved. However, when heating or the like is performed, the organic insulating material releases hydrogen, moisture or an organic component as a gas. Entry of such gas into a transistor could adversely impact and change the electrical characteristics of the display device and the reliability of the display device can be decreased. However, the claimed first insulating film and the third insulating film cover the second insulating film. The first insulating film and the third insulating film include inorganic insulating materials such as a silicon nitride film, a silicon nitride oxide film, or the like. These can prevent entry of the gas into the first transistor and suppress a change of electrical characteristics and decrease in the reliability of the display device (e.g., see Applicant's paragraphs [0156] to [0162]). Thus, the stacking order of the organic insulating film and the inorganic insulating film is critical and has a specific beneficial function.

On the other hand, while the cited references may disclose a display device including various organic and inorganic insulating films, they do not disclose the stacking order or appreciate the criticality to such in obtaining a functionality that can prevent entry of the gas from the second insulating film into the first transistor. As a result, one of ordinary skill in the art would not have been predictably led to the claimed invention. For this additional reason, a *prima facie* case of obviousness has not been met.

Because Koyama alone or in view of Kim and Yamazaki do not appear to teach or suggest all the claim limitations, or appreciate advantages thereof, a *prima facie* case of obviousness cannot be maintained with respect to independent claims 1 and 21. Therefore, Applicant believes the rejections of claims 1 and 21 and claims dependent therefrom are not proper. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

Electronic Patent Application Fee Transmittal

Application Number:	13939323
Filing Date:	11-Jul-2013
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu HOSAKA
Filer:	Eric J. Robinson
Attorney Docket Number:	0756-10194

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
		Total in USD ($)		**1200**

Electronic Acknowledgement Receipt

EFS ID:	23974637
Application Number:	13939323
International Application Number:	
Confirmation Number:	2340
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu HOSAKA
Customer Number:	31780
Filer:	Eric J. Robinson/Jennifer Rosenfeld
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10194
Receipt Date:	03-NOV-2015
Filing Date:	11-JUL-2013
Time Stamp:	15:53:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$1200
RAM confirmation Number	2158
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	RCE_03NOV2015.pdf	697481 947ec17b1bf46bc400b179963e7c331dbe06eea4	no	3
Warnings:					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	AMENDMENT_03NOV2015.pdf	1550890 59d270935a8dcc077e4a4bbcea2f0da79733380a	no	12
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30686 8962f62b9b268395a9b0bda0fab7257ca64bdee6	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2279057		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/939,323	Filing Date 07/11/2013	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **11/03/2015**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 27	Minus	** 27	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/JERMAINE MINOR/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/939,323	07/11/2013	Yasuharu HOSAKA	0756-10194	2340

31780 7590 08/06/2015

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

EXAMINER
KIM, RICHARD H

ART UNIT	PAPER NUMBER
2871	

MAIL DATE	DELIVERY MODE
08/06/2015	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/939,323	Applicant(s) HOSAKA ET AL.	
	Examiner RICHARD KIM	Art Unit 2871	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/21/15*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-9 and 21-38* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *27-32,37 and 38* is/are allowed.

7)☒ Claim(s) *1-9,21-26 and 33-36* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *4/21/15*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Rejections - 35 USC § 103

2. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 9, 21-24, 26 and 33-36 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Koyama et al. (US 8,988,623 B2).

4. Re claims 1, 9, 21, 26, Koyama et al. discloses an electronic device (Figs. 4a-4e) comprising a first transistor (420); a first insulating film (416) over the first transistor; a second insulating film (403) over the first insulating film; a third insulating film (404) covering the second insulating film; and a first electrode (427) over the third insulating film, the first electrode being electrically connected to the first transistor (see Fig. 4D, ref. 427); a liquid crystal layer (Fig. 10, ref. 650) over the first electrodes; and a driver circuit portion comprising: a second transistor (410); the first insulating film (416) over the second transistor; and the second insulating film (403) over the first insulating film, wherein the first insulating film comprises an inorganic insulating material (col. 25, lines 29, 30), wherein an edge portion of the second insulating film (403) overlaps with the third insulating film (404) (at the contact hole in Fig. 4e). Koyama et al. does not disclose the device wherein the second insulating film comprises an

organic insulating material, and wherein the third insulating film comprises an inorganic insulating material.

5. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the device wherein the second insulating film comprises an organic insulating material, wherein the third insulating film comprises an inorganic insulating material. Alternating layers of inorganic and organic insulating material is well known in the art to obtain excellent insulating properties. Additionally, the simple substitution of one known element for another to obtain predictable results requires routine skill in the art (*KSR*).

6. Re claims 2 and 22, Koyama et al. does not disclose the device comprising a first alignment film over the first electrode; a second alignment film over the liquid crystal layer; a second electrode over the second alignment film; a fourth insulating film over the second electrode; a colored film over the fourth insulating film; and a light blocking film over the fourth insulating film.

7. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the device comprising a first alignment film over the first electrode; a second alignment film over the liquid crystal layer; a second electrode over the second alignment film; a fourth insulating film over the second electrode; a colored film over the fourth insulating film; and a light blocking film over the fourth insulating film. Doing so is a well-known structure in the art to form a color filter substrate in order to obtain a color display.

8. Re claims 3-5, 23 and 24, Koyama et al. does not disclose the device wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, and aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a GA-Zn-based metal oxide film; wherein the

second insulating film is any of an acrylic-based resin, a polyimide-based resin, a benzocyclobutene-based resin, a polyamide-based resin, and an epoxy-based resin; wherein the third insulating film is any of a silicon nitride film, a silicon oxide film, and an aluminum oxide film.

9. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the device wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, and aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a GA-Zn-based metal oxide film; wherein the second insulating film is any of an acrylic-based resin, a polyimide-based resin, a benzocyclobutene-based resin, a polyamide-based resin, and an epoxy-based resin; wherein the third insulating film is any of a silicon nitride film, a silicon oxide film, and an aluminum oxide film. Employing the claimed materials as an insulating layer is well known in the art due to their high insulating properties. Furthermore, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin,* 125 USPQ 416.

10. Re claims 33 and 35, Koyama et al. discloses the device wherein an edge portion of the first insulating film (416) overlaps with the third insulating film (404) (at the contact hole in Fig. 4e).

11. Re claims 34 and 36, Koyama et al. discloses the device wherein the first transistor and the second transistor each comprises a gate insulating film (402), a source electrode (415a), and a drain electrode (415b), and wherein bottom surfaces of the source electrode and the drain electrode are in contact with a top surface of the gate insulating film.

12. Claims 6, 7 and 25 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Koyama et al. in view of Kim et al. (US 2012/0013817 A1).

13. Koyama et al. discloses the device previously recited, but does not disclose the device wherein the first and the second transistors each comprise an oxide semiconductor layer, wherein the oxide semiconductor layer comprises any of indium and zinc.

14. Kim et al. discloses a device wherein the transistor comprises an oxide semiconductor layer comprising indium or zinc (paragraph 0107).

15. It would have been obvious to one having ordinary skill in the art at the time the invention as made to employ the device wherein the transistor comprises an oxide semiconductor layer comprising indium or zinc since one would be motivated by superior semiconductor characteristics (paragraph 0107).

16. Claim 8 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Koyama et al. and Kim et al. in view of Yamazaki et al. (US 2011/0157252 A1).

17. Koyama et al. does not disclose the device wherein the oxide semiconductor layer has a first oxide semiconductor layer and a second oxide semiconductor layer.

18. Yamazaki et al. discloses a device wherein the oxide semiconductor layer has a first oxide semiconductor layer and a second oxide semiconductor layer (paragraph 0178).

19. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the device wherein the oxide semiconductor layer has a first

oxide semiconductor layer and a second oxide semiconductor layer since one would be motivated by obtaining an oxide semiconductor having a crystal region having a large thickness (paragraph 0178).

Allowable Subject Matter

20. Claims 27-32, 37 and 38 allowed.

Response to Arguments

21. Applicant's arguments with respect to the claims have been considered but are moot due to new grounds of rejection.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD KIM whose telephone number is (571)272-2294. The examiner can normally be reached on 9:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bumsuk Won can be reached on (571)272-2713. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RICHARD KIM/
Primary Examiner, Art Unit 2871

Notice of References Cited	Application/Control No. 13/939,323	Applicant(s)/Patent Under Reexamination HOSAKA ET AL.	
	Examiner RICHARD KIM	Art Unit 2871	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,988,623 B2	03-2015	Koyama et al.	349/43
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S72	4	("6498369" "20090046230").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 19:54
S73	7	yasuharu.in. and hosaka.in. and (edge adj portion)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 20:03
S76	234	S74 and S75	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 20:35
S75	3440	(349/43).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 20:35
S74	1463	(349/138).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 20:35
S78	75	S77 and ((align$5 adj film) near5 (contact adj hole))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 20:43
S77	60592	("349").CLAS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 20:43
S80	27	S79 and Richard.xa.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 20:51
S79	1463	(349/138).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 20:51
S82	3	S79 and Richard.xa. and superimpos$5	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 20:52
S81	2	S79 and Richard.xa. and superimpose	US-PGPUB; USPAT;	OR	ON	2015/07/29 20:52

			EPO; DERWENT			
S83	322	((G02F1/136227 and G02F1/133345).CPC.)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 20:53
S84	254	((G02F1/136227 and G02F1/133345).CPC. and @ad<"20130711")	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:01
S86	102	((G02F1/136227 and G02F1/133345).CPC. and @ad<"20120720") and (driv$5 near5 (transistor tft))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:04
S85	223	((G02F1/136227 and G02F1/133345).CPC. and @ad<"20120720")	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:04
S87	110	((G02F1/136227 and G02F1/133345).CPC. and @ad<"20130720") and (driv$5 near5 (transistor tft))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:05
S88	251	((G02F1/136227 and G02F1/13454).CPC.)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:06
S89	19	("4826297" | "5095304" | "5130829" | "5641974" | "5798534" | "5936698" | "5952588" | "5982462" | "5982469" | "6046479" | "6108055").PN. OR ("6246460").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/07/29 21:08
S91	278	S90 and (driv$5 near5 transistor)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:09
S90	835	(349/151).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 21:09
S94	147	S92 and S93	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:10
S93	1896	((G02F1/133345).CPC.)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:10
S92	2878	((G02F1/13454).CPC.)	US-PGPUB; USPAT; EPO;	OR	ON	2015/07/29 21:10

			DERWENT			
S95	64	("4408836" | "4832457" | "4874227" | "4906071" | "5032531" | "5055899" | "5106197" | "5121237" | "5148301" | "5164853" | "5200847" | "5250931" | "5453858" | "5525822" | "5608557" | "5644370" | "5650664" | "5710606" | "5739880" | "5780872" | "5796150" | "5815226" | "5818070" | "5821138" | "5821622" | "5859443" | "5864150" | "5929464").PN. OR ("6115094").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/07/29 21:11
S98	1443	S96 and (driv$5 near2 TFT) and ((contact adj hole) near5 (insulat$5))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:14
S97	4795	S96 and (driv$5 near2 TFT)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:14
S96	60592	("349").CLAS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 21:14
S99	1343	S96 and (driv$5 near2 TFT) and ((contact adj hole) near5 (insulat$5)) and @ad<"20120711"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:15
S100	6	("20060215102" | "20070279572" | "20080218838" | "20090051286" | "20110068334" | "20110080549").PN. OR ("8982306").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/07/29 21:17
S101	15	("20060256268" | "20070146591" | "20070222925" | "6727969" | "6798480" | "6914656" | "7088409" | "7362400" | "7486351" | "7502084").PN. OR ("7643115").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/07/29 21:48
S103	419	S102 and ((tft) near5 driv$5)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 21:54
S102	2740	(349/141).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 21:54
S104	15	("20060256268" | "20070146591" | "20070222925" | "6727969" | "6798480" | "6914656" | "7088409" | "7362400" | "7486351" | "7502084").PN. OR ("7643115").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/07/29 22:01
S107	137	S105 and S106	US-PGPUB; USPAT; EPO;	OR	ON	2015/07/29 22:02

			DERWENT			
S106	2740	(349/141).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 22:02
S105	1463	(349/138).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 22:02
S109	1325	((G02F1/133345).CPC. and ((thin adj film adj transistor) tft))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 22:09
S108	1896	((G02F1/133345).CPC.)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 22:09
S110	946	((G02F1/133345).CPC. and ((thin adj film adj transistor) tft) and @ad<"20120720")	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 22:10
S111	1	("8531637").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 22:21
S113	46	S112 and (bottom adj gate)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/29 22:28
S112	835	(349/151).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 22:28
S114	1	("6498369").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/29 22:42
S115	1	("8988623").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/30 15:11
S116	13	((G02F1/133345).CPC. and (inorganic near5 organic near5 alternat$5) and @ad<"20120720")	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/30 15:32
S118	60633	("349").CLAS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/30 15:34
S117	1	((G02F1/133345).CPC. and (inorganic near5 organic near5 alternating) and @ad<"20120720")	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/30 15:34

S120	10	(S118 and (inorganic near5 organic near5 alternate) and @ad<"20120720")	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/30 15:35
S119	18	(S118 and (inorganic near5 organic near5 alternating) and @ad<"20120720")	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/30 15:35
S121	64	(S118 and (inorganic near5 organic near5 gas) and @ad<"20120720")	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/30 15:36
S123	23	(S118 and (inorganic near5 organic near5 react$5) and @ad<"20120720")	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/30 15:37
S122	1	(S118 and (inorganic near5 organic near5 reactivity) and @ad<"20120720")	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/30 15:37
S124	1	("20120013817").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/30 16:48
S125	1	("20110157252").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/30 16:50
S126	1	("6498369").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/30 21:45
S127	1	("8,988,623").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/30 21:46
S129	129923	g02f1/$.cpc.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 00:21
S128	0	g02f1.cpc.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 00:21
S131	41	S129 and ((alternating alternate) near5 organic near5 inorganic)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 00:22
S130	242	S129 and ((alternating alternat$5) near5 organic near5 inorganic)	US-PGPUB; USPAT; EPO;	OR	ON	2015/07/31 00:22

			DERWENT			
S132	11	S129 and ((alternates) near5 organic near5 inorganic)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 00:24
S135	400	S134 and (organic near5 inorganic)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 00:26
S134	1463	(349/138).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/31 00:26
S133	11	S132 and (organic near5 inorganic)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 00:26
S137	310	S134 and S136	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 00:27
S136	4760	(349/42,43).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/31 00:27
S139	75	S137 and (organic near5 inorganic)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 00:28
S138	388489	"19" and (organic near5 inorganic)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 00:28
S146	34	S145 and ((organic near5 inorganic) near5 (alternating))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:29
S145	129923	g02f1/$.cpc.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:29
S144	0	S141 and ((organic near5 inorganic) near5 (alternating))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:29
S143	0	S142 and ((organic near5 inorganic) near5 (alternating))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:29

S142	310	S140 and S141	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:29
S141	4760	(349/42,43).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/31 13:29
S140	1463	(349/138).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/31 13:29
S147	171	S145 and ((organic near5 inorganic) near5 (barrier))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:32
S148	0	S145 and ((organic near5 inorganic) near5 (barrier) near5 tft)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:33
S149	6	S145 and ((organic near5 inorganic) near5 (stack) near5 tft)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:40
S152	56	S141 and ((organic near5 inorganic) near5 (stacked stack))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:41
S151	480	S145 and ((organic near5 inorganic) near5 (stacked stack))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:41
S150	4	S145 and ((organic near5 inorganic) near5 (stacked) near5 tft)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:41
S153	3	"8988623"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 13:48
S156	24	S154 and S155	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 14:08
S155	1463	(349/138).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/31 14:08
S154	835	(349/151).CCLS.	US-PGPUB; USPAT;	OR	OFF	2015/07/31 14:08

			USOCR			
S157	1205	S155 and (insulating)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 14:09
S161	2623	((G02F1/13454).CPC.) and @ad<"20120720"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 14:10
S160	2878	((G02F1/13454).CPC.)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 14:10
S159	287	S158 and (tft near5 driv$5)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 14:10
S158	835	(349/151).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/31 14:10
S162	141	((G02F1/13454).CPC.) and @ad<"20120720" and zhang.in.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/07/31 14:11
S163	23	("4457589" | "5148301" | "5300446" | "5523865" | "5777701" | "5888856" | "6011607" | "6055034" | "6072556" | "6075580").PN. OR ("6404479").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/07/31 14:12
L1	1	("8988623").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/03 14:41
L2	1	("20110157252").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/03 14:52
L4	23	("7,583,336" "7,696,529" "7,760,309" "8,115,893" "8,399,182" "8,704,962" "7,859,510" "20100117991").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/08/03 14:56
L3	21	("7,583,336" "7,696,529" "7,760,309" "8,115,893" "8,399,182" "8,704,962" "7,859,510" 2010/0117991).pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/08/03 14:56
L5	23	("7583336" "7696529" "7760309" "8115893" "8399182" "8704962" "7859510" "20100117991").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/08/03 14:58
L6	9	("20080129706" | "20080143906" |	US-	OR	ON	2015/08/03

		"20080239214" | "20080252618" | "20080266661" | "20090051842" | "20090075421" | "20100020029" | "20100194709").PN. OR ("8704962").URPN.	PGPUB; USPAT; USOCR			15:03
L9	59	7 and 8	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/08/03 15:05
L8	3214	(349/149-152).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/03 15:05
L7	2741	(349/141).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/03 15:05
L10	96	("3774989" | "3814501" | "3838909" | "3864905" | "4097128" | "4345249" | "4923286" | "5035490" | "5128782" | "5194976" | "5270846" | "5448385" | "5453858" | "5574292" | "5583678" | "5612799" | "5745203").PN. OR ("6160600").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/03 15:07
L11	1338	((G02F1/134363).CPC. and ffs)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/08/03 15:14
L14	11	((G02F1/13454).CPC.) and 11	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/08/03 15:15
L13	1184	((G02F1/13454).CPC. and ((align$5 orientat$5) adj3 (layer film)))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/08/03 15:15
L12	1915	((G02F1/133345).CPC.)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/08/03 15:15

EAST Search History (Interference)

<This search history is empty>

8/3/2015 3:17:04 PM
C:\Users\rkim3\Documents\EAST\Workspaces\13939323.wsp

PTO/SB/08A (07-06)
Approved for use through 03/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA
Art Unit	2871
Examiner Name	R. KIM
Attorney Docket Number	0756-10194

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-7,583,336	09-01-2009	AHN.B	
		US-7,696,529	04-13-2010	CHOO.K et al.	
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		US-2010/0117991	05-13-2010	KOYAMA.J et al.	

FOREIGN PATENT DOCUMENTS

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		JP-2007-123861A	05-17-2007			Abst.
		JP-2012-128159A	07-05-2012			Abst.
		JP-2009-271103A	11-19-2009			Abst.
		EP-2466365A	06-20-2012			Eng.
		KR-2012-0067288A	06-25-2012			Abst.
		CN-102540603A	07-04-2012			Abst.

Examiner Signature	/Richard Kim/	Date Considered	08/03/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.K./

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13939323	HOSAKA ET AL.
	Examiner	Art Unit
	RICHARD KIM	2871

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search attached	1/12/2015	RHK
EAST search attached	7/31/2015	RHK

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Attorney Docket No. 0756-10194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 2340
Yasuharu HOSAKA et al.	)	Group Art Unit: 2871
Serial No. 13/939,323	)	Examiner: Richard H. Kim
Filed: July 11, 2013	)	
For: DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	)	

AMENDMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action dated January 21, 2015, please consider the following amendments and remarks in connection with the above-identified application.

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks begin on page 9 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A display device comprising:

a pixel portion comprising:

a first transistor;

a first insulating film over the first transistor;

a second insulating film over the first insulating film;

a third insulating film [[over]] covering the second insulating film; and

a first electrode over the third insulating film, the first electrode being electrically connected to the first transistor;

~~a first alignment film over the first electrode; and~~

~~a liquid crystal layer over the first alignment film;~~ and

a driver circuit portion comprising:

a second transistor;

the first insulating film over the second transistor; and

the second insulating film over the first insulating film[[; and]]

~~the first alignment film over the second insulating film~~,

wherein the first insulating film comprises an inorganic insulating material,

wherein the second insulating film comprises an organic insulating material,

wherein the third insulating film comprises an inorganic insulating material, and

~~wherein the first alignment film is entirely in contact with the second insulating film in the driver circuit portion~~

wherein an edge portion of the second insulating film overlaps with the third insulating film.

2. (Currently Amended) The display device according to claim 1 further comprising:

~~a second alignment film over the liquid crystal layer;~~

a second electrode over the ~~second alignment film~~ first electrode;

a fourth insulating film over the second electrode;

a colored film over the fourth insulating film; and

a light-blocking film over the fourth insulating film.

3. (Original) The display device according to claim 1,

wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a Ga-Zn-based metal oxide film.

4. (Original) The display device according to claim 1,

wherein the second insulating film is any of an acrylic-based resin, a polyimide-based resin, a benzocyclobutene-based resin, a polyamide-based resin, and an epoxy-based resin.

5. (Original) The display device according to claim 1,

wherein the third insulating film is any of a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

6. (Original) The display device according to claim 1,

wherein the first transistor and the second transistor each comprises an oxide semiconductor layer.

7. (Original) The display device according to claim 6,

wherein the oxide semiconductor layer comprises any of indium and zinc.

8. (Original) The display device according to claim 6,

wherein the oxide semiconductor layer has a first oxide semiconductor film and a second oxide semiconductor film.

9. (Original) An electronic device comprising the display device according to claim 1.

10.-20. (Canceled)

21. (Currently Amended) A display device comprising:

a pixel portion comprising:

a first transistor;

a first insulating film over the first transistor;

a second insulating film over the first insulating film;

a third insulating film [[over]] covering the second insulating film;

a first electrode over the third insulating film, the first electrode being electrically connected to the first transistor; and

~~a first alignment film over the first electrode; and~~

a liquid crystal layer over the first ~~alignment film~~ electrode; and

a driver circuit portion comprising:

a second transistor;

the first insulating film over the second transistor; and

the second insulating film over the first insulating film[[; and]]

~~the first alignment film over the second insulating film~~,

wherein the first insulating film comprises an inorganic insulating material,

wherein the second insulating film comprises an organic insulating material,

wherein the third insulating film comprises an inorganic insulating material, and

~~wherein the first alignment film is in contact with the second insulating film over the driver circuit portion~~

wherein an edge portion of the second insulating film overlaps with the third insulating film.

22. (Currently Amended) The display device according to claim 21, further comprising:

a first alignment film over the first electrode;

a second alignment film over the liquid crystal layer;

a second electrode over the second alignment film;

a fourth insulating film over the second electrode;

a colored film over the fourth insulating film; and

a light-blocking film over the fourth insulating film.

23. (Previously Presented) The display device according to claim 21,

wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a Ga-Zn-based metal oxide film.

24. (Previously Presented) The display device according to claim 21,

wherein the third insulating film is any of a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

25. (Previously Presented) The display device according to claim 21,

wherein the first transistor and the second transistor each comprises an oxide semiconductor layer.

26. (Previously Presented) An electronic device comprising the display device according to claim 21.

27. (Currently Amended) A display device comprising:

a pixel portion comprising:

a first transistor;

a first insulating film over the first transistor;

a second insulating film over the first insulating film;

a third insulating film ~~over and in contact with~~ covering the second insulating film;

a first electrode over the third insulating film, the first electrode being electrically connected to the first transistor; and

~~a first alignment film over the first electrode; and~~

a liquid crystal layer over the first ~~alignment film~~ electrode; and

a driver circuit portion comprising:

a second transistor;

the first insulating film over the second transistor; and

the second insulating film over the first insulating film; [[and]]

~~the first alignment film over and in contact with the second insulating film,~~

wherein the first insulating film comprises an inorganic insulating material,

wherein the second insulating film comprises an organic insulating material,

wherein the third insulating film comprises an inorganic insulating material, [[and]]

~~wherein the first alignment film is in contact with the second insulating film over the driver circuit portion~~

wherein an edge portion of the second insulating film overlaps with the third insulating film, and

wherein the third insulating film is not provided in the driver circuit portion.

28. (Currently Amended) The display device according to claim 27, further comprising:

a first alignment film over the first electrode;

a second alignment film over the liquid crystal layer;

a second electrode over the second alignment film;

a fourth insulating film over the second electrode;

a colored film over the fourth insulating film; and

a light-blocking film over the fourth insulating film.

29. (Previously Presented) The display device according to claim 27,

wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a Ga-Zn-based metal oxide film.

30. (Previously Presented) The display device according to claim 27,

wherein the third insulating film is any of a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

31. (Previously Presented) The display device according to claim 27,

wherein the first transistor and the second transistor each comprises an oxide semiconductor layer.

32. (Previously Presented) An electronic device comprising the display device according to claim 27.

33. (New) The display device according to claim 1,

wherein an edge portion of the first insulating film overlaps with the third insulating film.

34. (New) The display device according to claim 1,

wherein the first transistor and the second transistor each comprises a gate insulating film, a source electrode, and a drain electrode, and

wherein bottom surfaces of the source electrode and the drain electrode are in contact with a top surface of the gate insulating film.

35. (New) The display device according to claim 21,

wherein an edge portion of the first insulating film overlaps with the third insulating film.

36. (New) The display device according to claim 21,

wherein the first transistor and the second transistor each comprises a gate insulating film, a source electrode, and a drain electrode, and

wherein bottom surfaces of the source electrode and the drain electrode are in contact with a top surface of the gate insulating film.

37. (New) The display device according to claim 27,

wherein an edge portion of the first insulating film overlaps with the third insulating film.

38. (New) The display device according to claim 27,

wherein the first transistor and the second transistor each comprises a gate insulating film, a source electrode, and a drain electrode, and

wherein bottom surfaces of the source electrode and the drain electrode are in contact with a top surface of the gate insulating film.

REMARKS

The Official Action mailed January 21, 2015, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on July 11, 2013; September 19, 2013; November 12, 2013 and December 2, 2014.

A further Information Disclosure Statement is submitted herewith and consideration of this Information Disclosure Statement is respectfully requested.

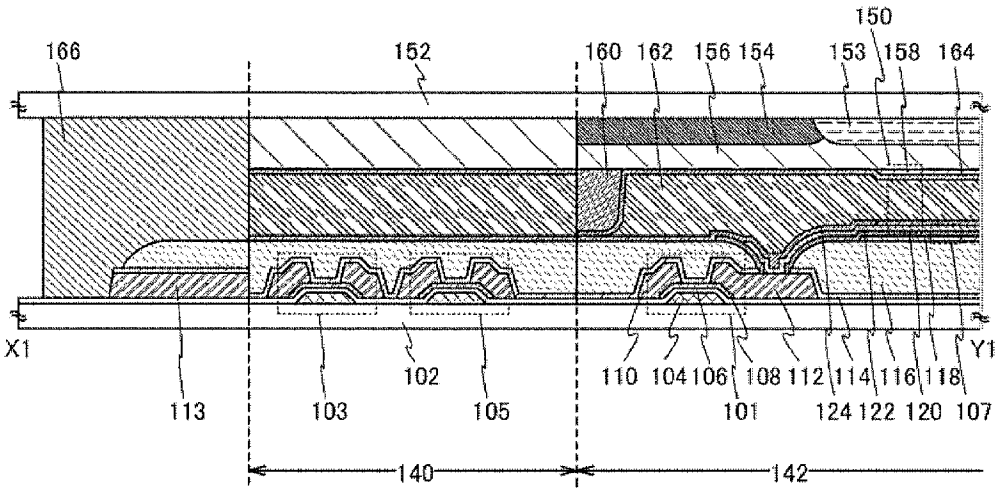
Claims 1-9 and 21-32 were pending in the present application prior to the above amendment. Claims 1-2, 21-22 and 27-28 have been amended to better recite the features of the present invention and new claims 33-38, which read on the elected species, have been added to recite additional protection to which the Applicant is entitled. Accordingly, claims 1-9 and 21-38 are now pending in the present application and elected, of which claims 1, 21 and 27 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 3 of the Official Action rejects claims 1-5, 9 and 21-32 as obvious based on the combination of U.S. Patent No. 6,498,369 to Yamazaki and U.S. Publication No. 2009/0046230 to Sakurai. Paragraph 15 of the Official Action rejects claims 6-7 as obvious based on the combination of Yamazaki '369, Sakurai and U.S. Publication No. 2012/0013817 to Kim. Paragraph 19 of the Official Action rejects claim 8 as obvious based on the combination of Sakurai and U.S. Publication No. 2011/0157252 to Yamazaki. The Applicant respectfully traverses the rejections because a *prima facie* case of obviousness cannot be maintained against the independent claims of the present application, as amended.

As stated in MPEP §§ 2142-2144.04, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some reason to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

With respect to independent claims 1, 21 and 27, the prior art, either alone or in combination, does not teach or suggest all the features of the independent claims, as amended. Specifically, rejected independent claims 1, 21 and 27 are revised to add that a third insulating film (an inorganic film) covers a second insulating film (an inorganic film) and an edge portion of the second insulating film overlaps the third insulating film. Independent claim 27 further adds that the third insulating film is not provided in the driver circuit portion. These features are supported by at least Applicant's FIG. 2 (below) and FIG. 5 as well as paragraph [0235] of Applicant's publication where there are shown and described first-third insulating films 114, 116 and 120, respectively oriented as claimed.

FIG. 2



In the present invention, the second insulating film is formed using an organic insulating material, with which planarity is improved. However, when heating or the like is performed, the organic insulating material may release hydrogen, moisture, or an organic component as a gas. Entry of such a gas into a transistor of the display device may adversely change the electrical characteristics of a display device, and decrease the reliability of the display device. However, covering the second insulating film with the third insulating film including an inorganic insulating material (such as a silicon nitride film, a silicon nitride oxide film, or the like) can prevent entry of such a gas into the first transistor. This acts to suppress a change of electrical characteristics and any adverse decrease in the reliability of the display device.

In rejecting the claims, the Official Action alleges that Yamazaki '369 discloses a second insulating film and a third insulating film over the second insulating film. However, Yamazaki does not necessarily teach or suggest that the third insulating film covers the second insulating film, and fails to teach that entry of gas from the second insulating film into the transistor should be reduced. The secondary references do not appear to overcome the above deficiencies of Yamazaki '369.

Because Yamazaki '369 and Sakurai do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained with respect to independent claims 1, 21 and 27. The secondary references to Kim and Yamazaki '252 do not cure the deficiencies of Yamazaki '369 and Sakurai. Therefore, Applicant believes the rejections of claims 1, 21 and 27 and claims dependent therefrom are not proper. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

New claims 33-38 have been added to recite additional protection to which the Applicant is entitled. The features of claims 33-38 are supported in the present specification, for example, by at least Applicant's FIGS. 2 and 5. New claims 33, 35, and 37 recite that an edge of a first insulating film and the third insulating film are overlapped with each other. Thus, the second insulating film is surrounded by the first insulating film and the third insulating film, which are inorganic insulating films that suppress entry of hydrogen, moisture, or an organic component into the transistor. Surrounding the second insulating film can prevent entry of gas into the transistor, and suppress a change of electrical characteristics or a decrease in the reliability of the display device. New claims 34, 36, and 38 recite that a first transistor and a second transistor each comprises a gate insulating film, a source electrode, and a drain electrode, and bottom surfaces of the source electrode and the drain electrode are in contact with a top surface of the gate insulating film. These features do not appear to be taught or suggested by Yamazaki '369 or the other cited references. For the reasons stated above, the Applicant respectfully submits that new claims 33-38 are in condition for allowance.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

Attorney Docket No. 0756-10194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 2340
Yasuharu HOSAKA et al.	)	Group Art Unit: 2871
Serial No. 13/939,323	)	Examiner: Richard H. Kim
Filed: July 11, 2013	)	
For: DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

JP 2012-128159; KR 20120067288 and CN 102540603 are in the family of EP 2 466 365.

A payment in the amount of $180 is being submitted to comply with the provisions of 37 C.F.R. § 1.97.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

PTO/SB/08A (07-06)
Approved for use through 03/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA
Art Unit	2871
Examiner Name	R. KIM
Attorney Docket Number	0756-10194

U. S. PATENT DOCUMENTS

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		US-8,115,893	02-14-2012	JUNG.T et al.	
		US-8,399,182	03-19-2013	LIM.J et al.	
		US-8,704,962	04-22-2014	OH.K et al.	
		US-7,859,510	12-28-2010	UMEZAKI.A	
		US-2010/0117991	05-13-2010	KOYAMA.J et al.	

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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] -Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
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		JP-2012-128159A	07-05-2012			Abst.
		JP-2009-271103A	11-19-2009			Abst.
		EP-2466365A	06-20-2012			Eng.
		KR-2012-0067288A	06-25-2012			Abst.
		CN-102540603A	07-04-2012			Abst.

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal

Application Number:	13939323
Filing Date:	11-Jul-2013
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu HOSAKA
Filer:	Eric J. Robinson/Adele Stamper
Attorney Docket Number:	0756-10194

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in Excess of 20	1202	6	80	480
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**660**

Electronic Acknowledgement Receipt

EFS ID:	22124387
Application Number:	13939323
International Application Number:	
Confirmation Number:	2340
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu HOSAKA
Customer Number:	31780
Filer:	Eric J. Robinson/Adele Stamper
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10194
Receipt Date:	21-APR-2015
Filing Date:	11-JUL-2013
Time Stamp:	16:07:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$660
RAM confirmation Number	2790
Deposit Account	
Authorized User	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	AMENDMENT_21APR2015_075610194.pdf	1683063 af69ddecf41b1823f996e23476530e37d860eed0	no	13
Warnings:					
Information:					
2		IDS_21APR2015_075610194.pdf	319421 dc9d8c5c4dca4192ea632d22a0be3f945fa5ab28	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Information Disclosure Statement (IDS) Form (SB08)	2	2

Warnings:					
Information:					
3	Foreign Reference	JP_2007123861.pdf	7792536 b3fc872c18b4380bcbb99155645ce03ae46850fc	no	48
Warnings:					
Information:					
4	Foreign Reference	JP2012128159.pdf	2372423 e4908e568eaa1a36a58ea819f47e2b5862ef93ba	no	16
Warnings:					
Information:					
5	Foreign Reference	JP_2009271103.pdf	1960570 ee7f277e088ae6f742b8ffef150e52a4fc1607c5	no	12
Warnings:					
Information:					
6	Foreign Reference	EP_2466365.pdf	747621 21942dcf3126ca143bca818c99644081a2b6ddb4	no	17
Warnings:					
Information:					

7	Foreign Reference	KR_20120067288.pdf	2002650 a19df5e1d38728bcd19d27e7766aa524b1ec7322	no	16
Warnings:					
Information:					
8	Foreign Reference	CN_102540603.pdf	2752561 b9704d2c3164e423fc1f8f09479d5a1a54113b63	no	19
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	32381 e5f155442be4a51f458cfd9049fab887acaa2cc3	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	19663226	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/939,323	Filing Date 07/11/2013	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **04/21/2015**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 22	Minus	** 21	= 1	X $80 =	80
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**80**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/JOSEPHINE DOUGLAS/

PTO/SB/06 (09-11)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/939,323	Filing Date 07/11/2013	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	04/21/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 27	Minus	** 21	= 6	X $80 =	480
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**480**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/JOSEPHINE DOUGLAS/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/939,323	07/11/2013	Yasuharu HOSAKA	0756-10194	2340

31780 7590 01/21/2015

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

EXAMINER
KIM, RICHARD H

ART UNIT	PAPER NUMBER
2871	

MAIL DATE	DELIVERY MODE
01/21/2015	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/939,323	Applicant(s) HOSAKA ET AL.	
	Examiner RICHARD KIM	Art Unit 2871	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/2/14*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-9 and 21-32* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-9 and 21-32* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *7/11/13* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☒ All b)☐ Some** c)☐ None of the:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *See Continuation Sheet*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Continuation of Attachment(s) 2). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :7/11/13, 9/19/13, 11/12/13, 12/2/14.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Rejections - 35 USC § 103

2. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 9, 21-32 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (US 6,498,369 B1) in view of Sakurai et al. (US 2009/0046230 A1).

4. Re claims 1, 9, 21, 26, 27 and 32, Yamazaki et al. discloses an electronic device comprising: a pixel portion comprising: a first transistor (304); a first insulating film (14) over the first transistor; a second insulating film (15) over the first insulating film; a third insulating film (135) over and in contact with the second insulating film (in fig. 6, the end portion of the insulating film 135 is in contact with the second insulating film 15); a first electrode (137) over the third insulating film, the first electrode being electrically connected to the first transistor; a first alignment film (601) over the first electrode; and a liquid crystal layer (605) over the first alignment film; and a driver circuit portion comprising: a second transistor (302); the first insulating film over the second transistor; the second insulating film over the first insulating film; and the first alignment film over the second insulating film, wherein the first alignment film is entirely in contact with the second insulating film in the driver portion (Fig. 6, ref. 601). Yamazaki does not disclose the device wherein the first insulating film comprises an inorganic

insulating material, wherein the second insulating film comprises an organic insulating material, wherein the third insulating film comprises an inorganic insulating material.

5. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the device wherein the first insulating film comprises an inorganic insulating material, wherein the second insulating film comprises an organic insulating material, wherein the third insulating film comprises an inorganic insulating material. Alternating layers of inorganic and organic insulating material is well known in the art to obtain excellent insulating properties.

6. Furthermore, in regard to the third insulating film, Sakurai et al. discloses employing an inorganic insulating layer (paragraph 0013).

7. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the device wherein the third insulating film comprises an inorganic insulating material since one would be motivated by superior capacitance properties (paragraph 0013).

8. Re claims 2, 22 and 28, Yamazaki et al. does not disclose the device comprising a second alignment film over the liquid crystal layer; a second electrode over the second electrode over the second alignment film; a fourth insulating layer over the second electrode; a colored film over the fourth insulating film; and a light blocking film over the fourth insulating film.

9. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the device comprising a second alignment film over the liquid crystal layer; a second electrode over the second alignment film; a fourth insulating layer over the second electrode; a colored film over the fourth insulating film; and a light blocking film

over the fourth insulating film. Doing so is a well-known structure in the art to form a color filter substrate in order to obtain a color display.

10. Re claims 3-5, 23-25, and 29-31, Yamazaki does not disclose the device wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, and aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a GA-Zn-based metal oxide film; wherein the second insulating film is any of an acrylic-based resin, a polyimide-based resin, a benzocyclobutene-based resin, a polyamide-based resin, and an epoxy-based resin; wherein the third insulating film is any of a silicon nitride film, a silicon oxide film, and an aluminum oxide film.

11. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the device wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, and aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a GA-Zn-based metal oxide film; wherein the second insulating film is any of an acrylic-based resin, a polyimide-based resin, a benzocyclobutene-based resin, a polyamide-based resin, and an epoxy-based resin; wherein the third insulating film is any of a silicon nitride film, a silicon oxide film, and an aluminum oxide film. Employing the claimed materials as an insulating layer is well known in the art due to their high insulating properties. Furthermore, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin,* 125 USPQ 416.

15. Claims 6 and 7 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. and Sakurai et al. in view of Kim et al. (US 2012/0013817 A1).

16. Yamazaki et al. discloses the device previously recited, but does not disclose the device wherein the first and the second transistor each comprise an oxide semiconductor layer, wherein the oxide semiconductor layer comprises any of indium and zinc.

17. Kim et al. discloses a device wherein the transistor comprises an oxide semiconductor layer comprising indium or zinc (paragraph 0107).

18. It would have been obvious to one having ordinary skill in the art at the time the invention as made to employ the device wherein the transistor comprises an oxide semiconductor layer comprising indium or zinc since one would be motivated by superior semiconductor characteristics (paragraph 0107).

19. Claim 8 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. and Sakurai et al. in view of Yamazaki et al. (US 2011/0157252 A1).

20. Yamazaki et al. does not disclose the device wherein the oxide semiconductor layer has a first oxide semiconductor layer and a second oxide semiconductor layer.

21. Yamazaki et al. (US 2011/0157252 A1) discloses a device wherein the oxide semiconductor layer has a first oxide semiconductor layer and a second oxide semiconductor layer (paragraph 0178).

22. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the device wherein the oxide semiconductor layer has a first oxide semiconductor layer and a second oxide semiconductor layer since one would be

motivated by obtaining an oxide semiconductor having a crystal region having a large thickness (paragraph 0178).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD KIM whose telephone number is (571)272-2294. The examiner can normally be reached on 9:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bumsuk Won can be reached on (571)272-2713. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RICHARD KIM/
Primary Examiner, Art Unit 2871

Notice of References Cited	Application/Control No. 13/939,323	Applicant(s)/Patent Under Reexamination HOSAKA ET AL.	
	Examiner RICHARD KIM	Art Unit 2871	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,498,369 b1	12-2002	Yamazaki et al.	257/347
*	B	US-2009/0046230 a1	02-2009	SAKURAI et al.	349/138
*	C	US-2012/0013817 a1	01-2012	KIM et al.	349/41
*	D	US-2011/0157252 a1	06-2011	Yamazaki et al.	345/690
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13939323	HOSAKA ET AL.
	Examiner	Art Unit
	RICHARD KIM	2871

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search attached	1/12/2015	RHK

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	1	("6115094").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 12:35
L6	1	("8643812").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 12:37
L7	3635	(349/106).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 12:47
L8	4	7 and (organic adj color adj filter)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 12:47
L9	490	7 and (organic near5 (color adj filter))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 12:47
L10	0	(64/989369).APP.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 12:50
L11	1	("6498369").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 12:50
L12	1390	(349/138).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 12:52
L13	397	12 and (second adj insulat$5)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 12:52
L14	3635	(349/106).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 12:55
L15	0	14 and (filer near5 (bottom near5 substrate))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 12:55
L16	79	14 and (filter near5 (bottom near5	US-	OR	ON	2015/01/12

		substrate))	PGPUB; USPAT; EPO; DERWENT			12:56
L17	1470	14 and (filter near5 (first near5 substrate))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 12:57
L18	815	(349/151).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 13:03
L19	252	18 and ((align$5 orient$5) adj2 (layer film))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:03
L20	1	("6498369").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 13:05
L21	58443	("349").CLAS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 13:18
L22	267	21 and ((metal adj oxide) near5 inorganic)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:18
L23	44	21 and (oxide near5 oxidizing near5 metal)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:20
L24	0	21 and (oxide near5 oxidizing near5 metal near5 inorganic)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:20
L25	0	21 and (oxidizing near5 metal near5 inorganic)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:20
L26	2	21 and (oxidizing near5 inorganic)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:20
L27	0	21 and (oixidizing near5 metal near5 organic)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:21
L28	3	21 and (oxidizing near5 metal near5 organic)	US-PGPUB; USPAT; EPO;	OR	ON	2015/01/12 13:21

			DERWENT			
L29	2264	21 and (organic near5 inorganic near5 insulat$5)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:29
L30	0	21 and (organic near5 inorganic near5 insulat$5 near5 alternate)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:32
L31	157	21 and (organic near5 inorganic near5 alternat$5)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:35
L32	4	21 and (organic near5 inorganic near5 alternat$5 near5 combination)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:36
L33	4271	(349/138,139).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 13:42
L34	32	33 and (capacit$5 near5 inorganic near5 insulat$5)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:42
L35	253	21 and (organic near5 inorganic near5 (silicon adj oxide))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:53
L36	1563	21 and (insulating near5 (acrylic))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 13:54
L37	174	21 and ((silicon adj nitride) near5 capacit$5)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 14:00
L38	58443	("349").CLAS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 14:00
L39	2231	38 and (semiconductor near5 oxide)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 14:00
L40	9	38 and (semiconductor near5 oxide nEAR5 SUPERIOR)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 14:01

L41	171	38 and (semiconductor near5 second near5 oxide near5 film)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 14:05
L42	42	38 and (second adj oxide adj semiconductor adj film)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 14:10
L43	1	("20090046230").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 14:21
L44	36	("7323356" "6294274" "7061014" 2008/0296568 "7282782" "7297977" "7462862" "20080254569" "20090073325" "20050199959" "7049190" "20070194379" "20090134399" "20060231882" "20060284171" "20060284172" "20060292777" "20070024187" "20070046191").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 14:44
L45	38	("20070052025" "20070090365" "20070172591" "20070187678" "20070187760" "20070252928" "20070287296" "20080038882" "20080038929" "20080050595" "20080073653" "20080083950" "20080106191" "20080128689" "20080129195" "20080166834" "20080182358" "20080224133" "20080258139").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 14:46
L46	52	("20080258140" "20080258141" "20080258143" "20090114910" "7105868" "7402506" "7411209" "7453065" "7453087" "7468304" "20060197092" "20080006877" "20060228974" "20020132454" "20090152541" "20070091793" "20010046027" "20060035452" "7501293").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 14:48
L47	38	("20060244107" "7211825" "20050017302" "5731856" "5744864" "20030218222" "7674650" "6563174" "7385224" "20070152217" "20090068773" "7732819" "20060043377" "20090278122" "20090280600" "20090152506" "20100092800" "20100109002" "20100065844").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 14:49
L48	3	("7796101" "8059067").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 14:51
S1	3161	(349/149-152).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/11 22:11
S2	815	(349/151).CCLS.	US-	OR	OFF	2015/01/11

			PGPUB; USPAT; USOCR			22:12
S3	3276	(349/43).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/11 22:12
S4	56	S2 and S3	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/11 22:12
S5	1129	((G02F1/13454).CPC. and ((align$5 orientat$5) adj3 (layer film)))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/11 22:16
S6	4	("20010052950" "6115097" "64983696115094").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/11 23:26
S7	0	("20010052950" "6115097" "64983696115094").pn. and orgainc	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/11 23:26
S8	1	("20010052950" "6115097" "64983696115094").pn. and organic	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/11 23:26
S9	4	("20010052950" "6115097" "64983696115094").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/11 23:29
S10	1	("6115094").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/11 23:30
S11	1390	(349/138).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 00:50
S12	1136	S11 and (peripheral driv$5)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 00:50
S13	113	S11 and ((peripheral driv$5) near5 (align$5 orientation))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 00:56
S14	7	("20030058376" | "20070242179" | "20090147188" | "6115097" | "6577372" | "7333160" | "8120742").PN. OR ("8643812").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/01/12 01:00

S15	1717	(349/123).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 01:28
S16	199	S15 and ((align$5 orientat$5) adj3 (layer film)) near5 (peripher$5 driv$5 non$5display)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 01:29
S17	9	("200610113536" "7791072" "201010295041" "8237166" "20110133181" "8269218" "20120319118").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 02:48
S18	38	("20020056838" "20030189401" "6727522" "20060169973" "20060208977" "20060238135" "7064346" "20070108446" "20060170111" "20070054507" "20070272922" "20040127038" "20040038446" "20060108636" "20060108529" "20060110867" "20060113565" "20060113539" "20060113549").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 02:50
S19	141144	("20030189210" "20030127651" "6861710" "7033848" "20090261337" "7671369" "7492012" "8008666" "20110204368" "8115206" "20120061666" "20120132919" "20120175625" "8405092" "8415669" "20130168670" "20130221361" "20080036705" "20110198598")".pn"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 02:52
S20	141144	("20030189210" "20030127651" "6861710" "7033848" "20090261337" "7671369" "7492012" "8008666" "20110204368" "8115206" "20120061666" "20120132919" "20120175625" "8405092" "8415669" "20130168670" "20130221361" "20080036705" "20110198598")".pn"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 02:52
S21	43	("20030189210" "20030127651" "6861710" "7033848" "20090261337" "7671369" "7492012" "8008666" "20110204368" "8115206" "20120061666" "20120132919" "20120175625" "8405092" "8415669" "20130168670" "20130221361" "20080036705" "20110198598").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 02:52
S22	19	("6,960,786" "7,554,116" "7,989,808" "8,207,537" "8,471,259" "20110084272" "20120153292" "20140022480").pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 02:54
S23	65	S11 and S15	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 03:13
S24	0	go2f.cpc. and (align$5 orientat$5) near5 (driv$5 peripheral periphery non$display)	US-PGPUB; USPAT;	OR	ON	2015/01/12 03:21

			EPO; DERWENT			
S25	58443	("349").CLAS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/12 03:22
S26	4252	S25 and (align$5 orientat$5) near5 (driv$5 peripheral periphery non$display)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 03:22
S27	1334	S25 and ((align$5 orientat$5) adj3 (film layer)) near5 (driv$5 peripheral periphery non$display)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2015/01/12 03:22

EAST Search History (Interference)

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1/12/2015 2:53:48 PM
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Sheet 1 of 6

Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA et al.
Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-2003/0189210	10-09-2003	YAMAZAKI.S et al.	
		US-2003/0127651	07-10-2003	MURAKAMI.S et al.	
		US-6861710	03-01-2005	MURAKAMI.S et al.	
		US-7033848	04-25-2006	MURAKAMI.S et al.	
		US-2009/0261337	10-22-2009	SAKAKURA.M et al.	
		US-7671369	03-02-2010	YAMAZAKI.S et al.	
		US-7492012	02-17-2009	MURAKAMI.S et al.	
		US-8008666	08-30-2011	YAMAZAKI.S et al.	
		US-2011/0204368	08-25-2011	TSUBUKU.M et al.	
		US-8115206	02-14-2012	SAKAKURA.M et al.	
		US-2012/0061666	03-15-2012	INOUE.S et al.	
		US-2012/0132919	05-31-2012	SAKAKURA.M et al.	
		US-2012/0175625	07-12-2012	YAMAZAKI.S	
		US-8405092	03-26-2013	INOUE.S et al.	
		US-8415669	04-09-2013	YAMAZAKI.S et al.	
		US-2013/0168670	07-04-2013	INOUE.S et al.	
		US-2013/0221361	08-29-2013	YAMAZAKI.S et al.	
		US-2008/0036705	02-14-2008	IWASHITA.T et al.	
		US-2011/0198598	08-18-2011	KIM.Y et al.	

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		JP-2003-197367A	07-11-2003			Abst.
		WO-2011/102203	08-25-2011			Eng.
		WO-2007/011061	01-25-2007			Eng.
		WO-2012/035984	03-22-2012			Eng.
		JP-2003-302917A	10-24-2003			Abst.
		JP-2012-084864A	04-26-2012			Abst.

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Sheet 2 of 6

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Attorney Docket Number	0756-10194

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		US-7796101	09-14-2010	IWASHITA.T et al.	
		US-8059067	11-15-2011	IWASHITA.T et al.	

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		JP-2011-192977A	09-29-2011			Abst.
		JP-2007-053355A	03-01-2007			Abst.
		JP-2007-250244A	09-27-2007			Abst.
		JP-2011-171300A	09-01-2011			Abst.
		TW-201230341	07-16-2012			Abst.
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		CN-102593185	07-18-2012			Abst.
		KR-2012-0090779A	08-17-2012			Abst.
		TW-201238056	09-16-2012			Abst.
		TW-201214711	04-01-2012			Abst.
		KR-2012-0138770A	12-26-2012			Abst.
		TW-I264822	10-21-2006			Abst.

Examiner Signature	/Richard Kim/	Date Considered	01/12/2015

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		KR-2007-0093830A	09-19-2007			Abst.
		CN-101038932	09-19-2007			Abst.

Examiner Signature	/Richard Kim/	Date Considered	01/12/2015

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Sheet 5 of 6

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Art Unit	2871
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		KR-2011-0094458A	08-24-2011			Abst.

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Sheet 6 of 6

Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA et al.
Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		INTERNATIONAL SEARCH REPORT (APPLICATION NO.PCT/JP2013/069456) DATED October 22, 2013.	Eng.
		WRITTEN OPINION (APPLICATION NO.PCT/JP2013/069456) DATED October 22, 2013.	Eng.

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Examiner Name	R. KIM
Attorney Docket Number	0756-10194

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Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

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Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA et al.
Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

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Examiner Signature	/Richard Kim/	Date Considered	01/12/2015

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Attorney Docket Number	0756-10194

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				First Named Inventor	Yasuharu HOSAKA et al.
(Use as many sheets as necessary)				Art Unit	2871
				Examiner Name	E. Glick
Sheet	8	of	12	Attorney Docket Number	0756-10194

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Examiner Signature	/Richard Kim/	Date Considered	01/12/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.K./

PTO/SB/08A (07-06)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	13/939,323
				Filing Date	July 11, 2013
				First Named Inventor	Yasuharu HOSAKA et al.
(Use as many sheets as necessary)				Art Unit	2871
				Examiner Name	E. Glick
Sheet	12	of	12	Attorney Docket Number	0756-10194

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		ORITA.M et al., "Amorphous transparent conductive oxide InGaO3(ZnO)m (m<4):a Zn4s conductor,", PHILOSOPHICAL MAGAZINE, 2001, Vol. 81, No. 5, pp. 501-515.	Eng.
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Examiner Signature	/Richard Kim/	Date Considered	01/12/2015

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	
				Filing Date	July 11, 2013
				First Named Inventor	Yasuharu HOSAKA et al.
(Use as many sheets as necessary)				Art Unit	
				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	0756-10194

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US2006/0113536	06-01-2006	KUMOMI et al.	
		US7791072	09-07-2010	KUMOMI et al.	
		US2010/0295041	11-25-2010	KUMOMI et al.	
		US8237166	08-07-2012	KUMOMI et al.	
		US2011/0133181	06-09-2011	YAMAZAKI	
		US8269218	09-18-2012	YAMAZAKI	
		US2012/0319118	12-20-2012	YAMAZAKI	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] -Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP2006-165528	06-22-2006			abst.
		JP2011-139047	07-14-2011			abst.

Examiner Signature	/Richard Kim/	Date Considered	01/12/2015

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.K./

Attorney Docket No. 0756-10194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 2340
Yasuharu HOSAKA et al.	)	Examiner: Richard H. Kim
Serial No. 13/939,323	)	Group Art Unit: 2871
Filed: July 11, 2013	)	
For: DISPLAY DEVICE AND	)	
ELECTRONIC DEVICE INCLUDING	)	
THE DISPLAY DEVICE	)	

AMENDMENT AND RESPONSE TO ELECTION REQUIREMENT

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Please consider the following amendments and remarks in connection with the above-identified application.

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A display device comprising:

a pixel portion comprising:

a first transistor;

a first insulating film over the first transistor;

a second insulating film over the first insulating film;

a third insulating film over the second insulating film;

a first electrode over the third insulating film, the first electrode being electrically connected to the first transistor;

a first alignment film over the first electrode; and

a liquid crystal layer over the first alignment film; and

a driver circuit portion comprising:

a second transistor;

the first insulating film over the second transistor;

the second insulating film over the first insulating film; and

the first alignment film over the second insulating film,

wherein the first insulating film comprises an inorganic insulating material,

wherein the second insulating film comprises an organic insulating material,

wherein the third insulating film comprises an inorganic insulating material, and

wherein the first alignment film is entirely in contact with the second insulating film in the driver circuit portion.

2. (Original) The display device according to claim 1 further comprising:

a second alignment film over the liquid crystal layer;

a second electrode over the second alignment film;

a fourth insulating film over the second electrode;

a colored film over the fourth insulating film; and

a light-blocking film over the fourth insulating film.

3. (Original) The display device according to claim 1,

wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a Ga-Zn-based metal oxide film.

4. (Original) The display device according to claim 1,

wherein the second insulating film is any of an acrylic-based resin, a polyimide-based resin, a benzocyclobutene-based resin, a polyamide-based resin, and an epoxy-based resin.

5. (Original) The display device according to claim 1,

wherein the third insulating film is any of a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

6. (Original) The display device according to claim 1,

wherein the first transistor and the second transistor each comprises an oxide semiconductor layer.

7. (Original) The display device according to claim 6,

wherein the oxide semiconductor layer comprises any of indium and zinc.

8. (Original) The display device according to claim 6,

wherein the oxide semiconductor layer has a first oxide semiconductor film and a second oxide semiconductor film.

9. (Original) An electronic device comprising the display device according to claim 1.

10.-20. (Canceled)

21. (New) A display device comprising:

a pixel portion comprising:

a first transistor;

a first insulating film over the first transistor;

a second insulating film over the first insulating film;

a third insulating film over the second insulating film;

a first electrode over the third insulating film, the first electrode being electrically connected to the first transistor;

a first alignment film over the first electrode; and

a liquid crystal layer over the first alignment film; and

a driver circuit portion comprising:

a second transistor;

the first insulating film over the second transistor;

the second insulating film over the first insulating film; and

the first alignment film over the second insulating film,

wherein the first insulating film comprises an inorganic insulating material,

wherein the second insulating film comprises an organic insulating material,

wherein the third insulating film comprises an inorganic insulating material, and

wherein the first alignment film is in contact with the second insulating film over the driver circuit portion.

22. (New) The display device according to claim 21, further comprising:

a second alignment film over the liquid crystal layer;

a second electrode over the second alignment film;

a fourth insulating film over the second electrode;

a colored film over the fourth insulating film; and

a light-blocking film over the fourth insulating film.

23. (New) The display device according to claim 21,

wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a Ga-Zn-based metal oxide film.

24. (New) The display device according to claim 21,

wherein the third insulating film is any of a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

25. (New) The display device according to claim 21,

wherein the first transistor and the second transistor each comprises an oxide semiconductor layer.

26. (New) An electronic device comprising the display device according to claim 21.

27. (New) A display device comprising:

a pixel portion comprising:

a first transistor;

a first insulating film over the first transistor;

a second insulating film over the first insulating film;

a third insulating film over and in contact with the second insulating film;

a first electrode over the third insulating film, the first electrode being electrically connected to the first transistor;

a first alignment film over the first electrode; and

a liquid crystal layer over the first alignment film; and

a driver circuit portion comprising:

a second transistor;

the first insulating film over the second transistor;

the second insulating film over the first insulating film; and

the first alignment film over and in contact with the second insulating film,

wherein the first insulating film comprises an inorganic insulating material,

wherein the second insulating film comprises an organic insulating material,

wherein the third insulating film comprises an inorganic insulating material, and

wherein the first alignment film is in contact with the second insulating film over the driver circuit portion.

28. (New) The display device according to claim 27, further comprising:

a second alignment film over the liquid crystal layer;

a second electrode over the second alignment film;

a fourth insulating film over the second electrode;

a colored film over the fourth insulating film; and

a light-blocking film over the fourth insulating film.

29. (New) The display device according to claim 27,

wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a Ga-Zn-based metal oxide film.

30. (New) The display device according to claim 27,

wherein the third insulating film is any of a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

31. (New) The display device according to claim 27,

wherein the first transistor and the second transistor each comprises an oxide semiconductor layer.

32. (New) An electronic device comprising the display device according to claim 27.

REMARKS

In response to the election requirement in the Office Action of October 31, 2014, Applicant hereby elects Species (1) "The specifics of the device comprising a liquid crystal display device comprising a liquid crystal layer (Fig. 2)." Claims 1-9 read on the elected species. New claims 21-32, which also read on Species (1), have been added. Specifically, newly added independent claims 21 and 27 are supported by, for example, Applicant's Figs.1A to 1C and Fig. 2 and associated disclosure while added dependent claims 22-26 and 28-32 correspond to dependent claims 2, 3, 5, 6, and 9. Non-elected claims 10-20 have been canceled without prejudice or disclaimer. Thus, claims 1-9 and 21-32 are pending and subject to examination at this time.

Examination on the merits is respectfully requested.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive,
Suite 20 North
Fairfax, Virginia 22033
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Attorney Docket No. 0756-10194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 2340
Yasuharu HOSAKA et al.	)	Examiner: Richard H. Kim
Serial No. 13/939,323	)	Group Art Unit: 2871
Filed: July 11, 2013	)	
For: DISPLAY DEVICE AND	)	
ELECTRONIC DEVICE INCLUDING	)	
THE DISPLAY DEVICE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

This Information Disclosure Statement is being submitted before the issuance of a first Office Action on the merits, therefore, no fee is required.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive,
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PTO/SB/08A (07-06)
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA
Art Unit	2871
Examiner Name	R. KIM
Attorney Docket Number	0756-10194

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-6,960,786	11-01-2005	YAMAZAKI.S et al.	
		US-7,554,116	06-30-2009	YAMAZAKI.S et al.	
		US-7,989,808	08-02-2011	YAMAZAKI.S et al.	
		US-8,207,537	06-26-2012	YAMAZAKI.S et al.	
		US-8,471,259	06-25-2013	YAMAZAKI.S et al.	
		US-2011/0084272	04-14-2011	MIYANAGA.A et al.	
		US-2012/0153292	06-21-2012	NAKAMURA.T et al.	
		US-2014/0022480	01-23-2014	YOKOYAMA.M et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] -Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP-2005-173106A	06-30-2005			Abst.

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Electronic Patent Application Fee Transmittal

Application Number:	13939323
Filing Date:	11-Jul-2013
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu HOSAKA
Filer:	Eric J. Robinson
Attorney Docket Number:	0756-10194

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in Excess of 20	1202	1	80	80
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**80**

Electronic Acknowledgement Receipt

EFS ID:	20841612
Application Number:	13939323
International Application Number:	
Confirmation Number:	2340
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu HOSAKA
Customer Number:	31780
Filer:	Eric J. Robinson/Adele Stamper
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10194
Receipt Date:	02-DEC-2014
Filing Date:	11-JUL-2013
Time Stamp:	15:52:22
Application Type:	Utility under 35 USC 111(a)

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Payment was successfully received in RAM	$80
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1	Response to Election / Restriction Filed	RER_02DEC2014_075610194.pdf	835725 44f028dbe41b9839e5c172bf47bf77661866a594	no	8
Warnings:					
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2		IDS_02DEC2014_075610194.pdf	314982 175db00c699f16c11663c821611da6a6ff2859cf	yes	2
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Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30402 7657bfed4bb63ec488af043980462ed683314ec9	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	4733217		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/939,323	Filing Date 07/11/2013	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
	12/02/2014	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 21	Minus	** 20	= 1	X $80 =	80
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**80**

		(Column 1)		(Column 2)	(Column 3)		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/LYNNELL JOHNSON/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/939,323	07/11/2013	Yasuharu HOSAKA	0756-10194	2340

31780 7590 10/31/2014

Robinson Intellectual Property Law Office, P.C.
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Fairfax, VA 22033

EXAMINER	
KIM, RICHARD H	

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2871	

MAIL DATE	DELIVERY MODE
10/31/2014	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/939,323	Applicant(s) HOSAKA ET AL.	
	Examiner RICHARD KIM	Art Unit 2871	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Election/Restrictions

2. This application contains claims directed to the following patentably distinct species:

3. (1) The specifics of the device comprising a liquid crystal display device comprising a liquid crystal layer (Fig. 2);

4. (2) The specifics of the device comprising an organic EL panel comprising a filler (Fig. 4).

5. The species are independent or distinct because they represent mutually exclusive embodiments distinguished by the type of display device. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable.

There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following reason(s) apply:

A search and/or examination of both species would require searches in different class/subclasses and/or require different fields of search (i.e. search queries). Additionally, a reference relevant to one species may not be relevant to the other species.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37

CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of patentably indistinct species**, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing them to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be corrected in compliance with 37 CFR 1.48(a) if one or more of the

currently named inventors is no longer an inventor of at least one claim remaining in the application. A request to correct inventorship under 37 CFR 1.48(a) must be accompanied by an application data sheet in accordance with 37 CFR 1.76 that identifies each inventor by his or her legal name and by the processing fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD KIM whose telephone number is (571)272-2294. The examiner can normally be reached on 9:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bumsuk Won can be reached on (571)272-2713. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RICHARD KIM/
Primary Examiner, Art Unit 2871

日　本　国　特　許　庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日 Date of Application:	２０１２年　７月２０日
出願番号 Application Number:	特願２０１２－１６１３４４
パリ条約による外国への出願に用いる優先権の主張の基礎となる出願の国コードと出願番号 The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is	ＪＰ２０１２－１６１３４４
出願人 Applicant(s):	株式会社半導体エネルギー研究所

２０１４年　２月２４日

特許庁長官
Commissioner,
Japan Patent Office　羽藤秀雄

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【整理番号】　P017384
【提出日】　平成24年 7月20日
【あて先】　特許庁長官　殿
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【手数料の表示】
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　【物件名】　明細書　1
　【物件名】　特許請求の範囲　1
　【物件名】　要約書　1
　【物件名】　図面　1

【書類名】明細書
【発明の名称】表示装置、及び該表示装置を有する電子機器
【技術分野】
【０００１】
液晶パネルを用いる表示装置、または有機ＥＬパネルを用いる表示装置に関する。また、該表示装置を有する電子機器に関する。
【背景技術】
【０００２】
近年、液晶パネルを用いる表示装置や有機ＥＬパネルを用いる表示装置の開発が盛んである。この表示装置には、大別して画素制御用のトランジスタ（画素トランジスタ）のみを基板上に形成して走査回路（駆動回路）は周辺ＩＣで行うものと、画素トランジスタとともに走査回路を同一基板上に形成するものに分類される。
【０００３】
表示装置の狭額縁化または周辺ＩＣのコスト低減のため、駆動回路一体型の表示装置の方が、有利である。しかしながら、駆動回路に用いるトランジスタとしては、画素トランジスタに用いられる電気特性（例えば、電界効果移動度（μＦＥ）またはしきい値等）よりも、高い電気特性が求められる。
【０００４】
トランジスタに適用可能な半導体薄膜としてシリコン系半導体材料が広く知られているが、その他の材料として酸化物半導体が注目されている。例えば、トランジスタに用いる半導体薄膜として、電子キャリア濃度が１０１８／ｃｍ３未満であるインジウム（Ｉｎ）、ガリウム（Ｇａ）、及び亜鉛（Ｚｎ）を含む非晶質酸化物を用いたトランジスタが開示されている（例えば、特許文献１参照）。
【０００５】
酸化物半導体を半導体層に用いるトランジスタは、シリコン系半導体材料である非晶質シリコンを半導体層に用いるトランジスタよりも電界効果移動度が大きいため、動作速度が速く、駆動回路一体型の表示装置には好適であり、且つ多結晶シリコンを半導体層に用いるトランジスタよりも製造工程が容易である。
【０００６】
しかし、酸化物半導体を半導体層に用いるトランジスタは、酸化物半導体に水素、水分等の不純物が入り込むことによってキャリアが形成され、該トランジスタの電気特性が変動するという問題がある。
【０００７】
上述した問題を解決するために、トランジスタのチャネル形成領域として用いる酸化物半導体膜中の水素原子の濃度を１×１０１６ｃｍ－３未満とすることで、信頼性を向上させたトランジスタが開示されている（例えば、特許文献２）。
【先行技術文献】
【特許文献】
【０００８】
【特許文献１】特開２００６－１６５５２８号公報
【特許文献２】特開２０１１－１３９０４７号公報
【発明の概要】
【発明が解決しようとする課題】
【０００９】
特許文献２にも記載されているように、酸化物半導体膜を半導体層に用いるトランジスタは、その電気特性を十分に維持するためには、水素、水分等を該酸化物半導体膜より極力排除することが重要である。
【００１０】
また、表示装置の画素領域及び駆動回路領域に双方にトランジスタを用いる場合、駆動方法にも依存するが、画素領域よりも駆動回路領域に用いるトランジスタの方が、電気的

負荷が大きいため、駆動回路領域に用いるトランジスタの電気特性が重要となる。
【００１１】
とくに、酸化物半導体膜を半導体層に用いるトランジスタを、画素領域及び駆動回路領域に用いた表示装置では、高温高湿環境下の信頼性試験において、駆動回路領域に用いるトランジスタの劣化が問題になっている。該トランジスタの劣化原因としては、トランジスタ上に形成された有機絶縁膜から、半導体層に用いる酸化物半導体膜へ水分等が入り込み、該酸化物半導体膜のキャリア密度が増加するためである。
【００１２】
そこで、本発明の一態様は、画素領域及び駆動回路領域にトランジスタを有する表示装置において、電気特性の変動を抑制すると共に、信頼性を向上させることを課題の一とする。とくに、トランジスタのチャネル形成領域に酸化物半導体膜を用いた表示装置において、該酸化物半導体膜への水素、水分の入り込みを抑制し、電気特性の変動を抑制すると共に、信頼性を向上させることを課題の一とする。
【課題を解決するための手段】
【００１３】
上述した課題に鑑み、本発明の一態様では、画素領域及び駆動回路領域に用いるトランジスタを有する表示装置において、トランジスタの電気特性の変動を抑制することができる構造を提供する。より具体的には、トランジスタのチャネル形成領域に酸化物半導体膜を用い、該トランジスタ上に設けられた有機絶縁材料により形成された平坦化膜の構造に特徴を持たせ、水素、水分が酸化物半導体膜、特に駆動回路領域に用いる酸化物半導体膜に入り込みづらい構造とする。より具体的には以下の通りである。
【００１４】
本発明の一態様は、画素電極と、該画素電極と電気的に接続される少なくとも一の第１のトランジスタを含む画素が複数個配列されている画素領域と、画素領域の外側に隣接し、該画素領域の各画素に含まれる第１のトランジスタに信号を供給する少なくとも一の第２のトランジスタを含む駆動回路領域と、が形成された第１の基板と、第１の基板と対向するように設けられた第２の基板と、第１の基板と第２の基板間に挟持された液晶層と、を有し、第１のトランジスタ及び第２のトランジスタ上に無機絶縁材料で形成された第１の層間絶縁膜と、第１の層間絶縁膜上に有機絶縁材料で形成された第２の層間絶縁膜と、第２の層間絶縁膜上に無機絶縁材料で形成された第３の層間絶縁膜と、を有し、第３の層間絶縁膜は、画素領域上の一部に設けられ、該第３の層間絶縁膜の端部が駆動回路領域よりも内側に形成されることを特徴とする表示装置である。
【００１５】
上記構成において、画素電極上に設けられた第１の配向膜と、第１の配向膜上に形成された液晶層と、液晶層上に設けられた第２の配向膜と、第２の配向膜上に設けられた対向電極と、対向電極上に設けられた有機保護絶縁膜と、有機保護絶縁膜上に設けられた有色膜及び遮光膜と、有色膜及び遮光膜上に設けられた第２の基板と、を有していてもよい。
【００１６】
また、本発明の他の一態様は、画素電極と、該画素電極と電気的に接続される少なくとも一の第１のトランジスタを含む画素が複数個配列されている画素領域と、画素領域の外側に隣接し、該画素領域の各画素に含まれる第１のトランジスタに信号を供給する少なくとも一の第２のトランジスタを含む駆動回路領域と、が形成された第１の基板と、第１の基板と対向するように設けられた第２の基板と、第１の基板と第２の基板間に挟持された発光層と、を有し、第１のトランジスタ及び第２のトランジスタ上に無機絶縁材料で形成された第１の層間絶縁膜と、第１の層間絶縁膜上に有機絶縁材料で形成された第２の層間絶縁膜と、第２の層間絶縁膜上に無機絶縁材料で形成された第３の層間絶縁膜と、を有し、第３の層間絶縁膜は、画素領域上の一部に設けられ、該第３の層間絶縁膜の端部が駆動回路領域よりも内側に形成されることを特徴とする表示装置である。
【００１７】
上記構成において、画素電極上に設けられた発光層と、発光層上に設けられた電極と、

を有していてもよい。
【００１８】
また、上記各構成において、第３の層間絶縁膜は、窒化シリコン膜、窒化酸化シリコン膜、酸化アルミニウム膜の中から選ばれたいずれか一であると好ましい。
【００１９】
また、上記各構成において、第１のトランジスタ及び第２のトランジスタは、チャネル形成領域を形成する半導体材料が酸化物半導体であると好ましい。また、第１のトランジスタ及び第２のトランジスタは、ゲート電極と、ゲート電極上に形成された酸化物半導体からなる半導体層と、半導体層上に形成されたソース電極及びドレイン電極と、を有する構成であると好ましい。
【００２０】
また、本発明の一態様は、上記各構成の表示装置を有する電子機器も範疇に含めるものである。
【発明の効果】
【００２１】
画素領域及び駆動回路領域にトランジスタを有する表示装置において、電気特性の変動を抑制すると共に、信頼性を向上させることができる。とくに、トランジスタのチャネル形成領域に酸化物半導体膜を用いた表示装置において、該酸化物半導体膜への水素、水分の入り込みを抑制し、電気特性の変動を抑制すると共に、信頼性を向上させることができる。
【図面の簡単な説明】
【００２２】
【図１】表示装置の一形態の上面を説明する図。
【図２】表示装置の一形態の断面を説明する図。
【図３】表示装置の一形態の上面を説明する図。
【図４】表示装置の一形態の断面を説明する図。
【図５】本発明の一態様に係るイメージセンサ付表示装置の一例を示す回路図および断面図。
【図６】本発明の一態様に係るタブレット型端末の一例を示す図。
【図７】本発明の一態様に係る電子機器の例を示す図。
【図８】各質量電荷比における放出ガスのイオン強度を示す図。
【図９】基板表面温度に対する各質量電荷比のイオン強度を示す図。
【図１０】試料の断面観察像。
【図１１】各試料の電気特性を示す図。
【発明を実施するための形態】
【００２３】
以下では、本発明の実施の形態について図面を用いて詳細に説明する。ただし、本発明は以下の説明に限定されず、その形態および詳細を様々に変更し得ることは、当業者であれば容易に理解される。また、本発明は以下に示す実施の形態の記載内容に限定して解釈されるものではない。
【００２４】
以下に説明する実施の形態において、同じものを指す符号は異なる図面間で共通して用いる。なお、図面において示す構成要素、すなわち層や領域等の厚さ幅、相対的な位置関係等は、実施の形態において説明する上で明確性のために誇張して示される。
【００２５】
また、本明細書等において「電極」や「配線」の用語は、これらの構成要素を機能的に限定するものではない。例えば、「電極」は「配線」の一部として用いられることがあり、その逆もまた同様である。さらに、「電極」や「配線」の用語は、複数の「電極」や「配線」が一体となって形成されている場合なども含む。
【００２６】

また、本明細書等において、窒化酸化シリコン膜とは、窒素と、酸素と、シリコンと、を成分として含有し、且つ、窒素の含有量が酸素の含有量よりも多い膜である。また、酸化窒化シリコン膜とは、酸素と、窒素と、シリコンと、を成分として含有し、且つ、酸素の含有量が窒素の含有量よりも多い膜である。

【００２７】

また、「ソース」や「ドレイン」の機能は、異なる極性のトランジスタを採用する場合や、回路動作において電流の方向が変化する場合などには入れ替わることがある。このため、本明細書等においては、「ソース」や「ドレイン」の用語は、入れ替えて用いることができるものとする。

【００２８】

（実施の形態１）

本実施の形態では、表示装置の一形態として、液晶パネルを用いた表示装置について図１及び図２を用いて説明する。

【００２９】

図１（Ａ）、（Ｂ）、（Ｃ）に表示装置の一形態として、表示装置の上面図を示す。なお、図１（Ａ）は、表示装置全体を、図１（Ｂ）は、表示装置の駆動回路部の一部分を、図１（Ｃ）は画素部の一部分の上面図を、それぞれ示す。また、図２は、図１（Ａ）におけるＸ１－Ｙ１の断面図に相当する。

【００３０】

図１（Ａ）に示す表示装置において、第１の基板１０２上に設けられた画素領域１４２と、画素領域１４２の外側に隣接し、該画素領域１４２に信号を供給する駆動回路領域であるゲートドライバ回路部１４０及びソースドライバ回路部１４４を囲むようにして、シール材１６６が設けられ、第２の基板１５２によって封止されている。また、画素領域１４２と、ゲートドライバ回路部１４０及びソースドライバ回路部１４４が設けられた第１の基板１０２と対向するように第２の基板１５２が設けられている。よって画素領域１４２と、ゲートドライバ回路部１４０と、ソースドライバ回路部１４４とは、第１の基板１０２とシール材１６６と第２の基板１５２によって、表示素子と共に封止されている。

【００３１】

また、図１（Ａ）においては、第１の基板１０２上のシール材１６６によって囲まれている領域とは異なる領域に、画素領域１４２、ゲートドライバ回路部１４０、ソースドライバ回路部１４４と電気的に接続されているＦＰＣ端子部１４６（ＦＰＣ：Ｆｌｅｘｉｂｌｅ　ｐｒｉｎｔｅｄ　ｃｉｒｃｕｉｔ）が設けられており、ＦＰＣ端子部１４６には、ＦＰＣ１４８が接続され、画素領域１４２、ゲートドライバ回路部１４０、及びソースドライバ回路部１４４に与えられる各種信号、及び電位は、ＦＰＣ１４８により供給されている。

【００３２】

また、図１（Ａ）においては、ゲートドライバ回路部１４０及びソースドライバ回路部１４４を画素領域１４２と同じ第１の基板１０２に形成している例を示しているが、この構成に限定されない。例えば、ゲートドライバ回路部１４０のみを第１の基板１０２に形成し、別途用意されたソースドライバ回路が形成された基板（例えば、単結晶半導体膜、多結晶半導体膜で形成された駆動回路基板）を、第１の基板１０２に実装する構成としても良い。

【００３３】

また、図１（Ａ）においては、ゲートドライバ回路部１４０は画素領域１４２の両側に２つ配置する構成について例示しているが、この構成に限定されない。例えば、画素領域１４２の片側にのみゲートドライバ回路部１４０を配置する構成としても良い。

【００３４】

なお、別途形成した駆動回路基板の接続方法は、特に限定されるものではなく、ＣＯＧ（Ｃｈｉｐ　Ｏｎ　Ｇｌａｓｓ）方法、ワイヤボンディング方法、或いはＴＡＢ（Ｔａｐｅ　Ａｕｔｏｍａｔｅｄ　Ｂｏｎｄｉｎｇ）方法などを用いることができる。また、表示

装置は、表示素子が封止された状態にあるパネルと、該パネルにコントローラを含むＩＣ等を実装した状態にあるモジュールとを含む。

【００３５】

このように、トランジスタを含む駆動回路の一部または全体を、画素領域１４２と同じ第１の基板１０２上に一体形成し、システムオンパネルを形成することができる。

【００３６】

また、図１（Ｃ）においては、画素領域１４２に、第１のトランジスタ１０１、容量素子１０７が形成されている。第１のトランジスタ１０１は、半導体層１０８に対して、ゲート電極１０４、ソース電極１１０、及びドレイン電極１１２が、それぞれ電気的に接続されている。また、図１（Ｃ）に示す平面図においては、図示しないが、第１のトランジスタ１０１上には、無機絶縁材料で形成された第１の層間絶縁膜と、第１の層間絶縁膜上に有機絶縁材料で形成された第２の層間絶縁膜と、第２の層間絶縁膜上に無機絶縁材料で形成された第３の層間絶縁膜が形成されている。また、容量素子１０７は、容量電極１１８と、容量電極１１８上に形成された第３の層間絶縁膜と、該第３の層間絶縁膜上に形成された画素電極１２２により構成されている。

【００３７】

また、図１（Ｂ）においては、駆動回路領域であるゲートドライバ回路部１４０に、第２のトランジスタ１０３、及び第３のトランジスタ１０５が形成されている。また、ゲートドライバ回路部１４０の各トランジスタは、半導体層１０８に対して、ゲート電極１０４、ソース電極１１０、及びドレイン電極１１２が、それぞれ電気的に接続されている。また、ゲートドライバ回路部１４０においては、ゲート電極１０４を含むゲート線が左右方向に延在し、ソース電極１１０を含むソース線が上下方向に延在し、ドレイン電極１１２を含むドレイン線がソース電極と離間して上下方向に延在している。

【００３８】

第２のトランジスタ１０３、及び第３のトランジスタ１０５を含むゲートドライバ回路部１４０は、画素領域１４２の各画素に含まれる第１のトランジスタ１０１に信号を供給することができる。

【００３９】

また、ゲートドライバ回路部１４０における第２のトランジスタ１０３、及び第３のトランジスタ１０５は、各種信号の制御、及び昇圧等を行うために、比較的高い電圧が必要となる。具体的には、１０Ｖ～３０Ｖ程度の電圧が必要となる。一方、画素領域１４２における第１のトランジスタ１０１は、画素のスイッチングのために用いるのみであるため、数Ｖ～２０Ｖ程度の電圧で駆動することができる。そのため、ゲートドライバ回路部１４０における第２のトランジスタ１０３、及び第３のトランジスタ１０５は、画素領域１４２における第１のトランジスタ１０１と比較し、与えられるストレスが非常に大きい構成となる。

【００４０】

図１（Ａ）、（Ｂ）、（Ｃ）に示す表示装置の構成をより具体的に説明するため、図１（Ａ）、（Ｂ）、（Ｃ）におけるＸ１－Ｙ１の断面図に相当する図２を用いて、ゲートドライバ回路部１４０、及び画素領域１４２の構成について、以下説明を行う。

【００４１】

画素領域１４２において、第１の基板１０２と、第１の基板１０２上に形成されたゲート電極１０４と、ゲート電極１０４上に形成されたゲート絶縁膜１０６と、ゲート絶縁膜１０６と接し、ゲート電極１０４と重畳する位置に設けられた半導体層１０８と、ゲート絶縁膜１０６、及び半導体層１０８上に形成されたソース電極１１０及びドレイン電極１１２と、により、第１のトランジスタ１０１が形成されている。

【００４２】

また、画素領域１４２において、第１のトランジスタ１０１上、より詳しくはゲート絶縁膜１０６、半導体層１０８、ソース電極１１０、及びドレイン電極１１２上に無機絶縁材料で形成された第１の層間絶縁膜１１４と、第１の層間絶縁膜１１４上に有機絶縁材料

で形成された第２の層間絶縁膜１１６と、第２の層間絶縁膜１１６上に形成された容量電極１１８と、第２の層間絶縁膜１１６及び容量電極１１８上に無機絶縁材料で形成された第３の層間絶縁膜１２０と、第３の層間絶縁膜１２０上に形成された画素電極１２２と、を有している。

【００４３】

なお、容量電極１１８と、第３の層間絶縁膜１２０と、画素電極１２２と、により容量素子１０７が形成されている。容量電極１１８、第３の層間絶縁膜１２０、及び画素電極１２２を、それぞれ、可視光において、透光性を有する材料により形成することで、画素部の開口率を損ねることなく大きな容量を確保することができるので、好適である。

【００４４】

また、画素電極１２２上には、第１の配向膜１２４と、第１の配向膜１２４上に設けられた液晶層１６２と、液晶層１６２上に設けられた第２の配向膜１６４と、第２の配向膜１６４上に設けられた対向電極１５８と、対向電極１５８上に設けられた有機保護絶縁膜１５６と、有機保護絶縁膜１５６上に設けられた有色膜１５３及び遮光膜１５４と、有色膜１５３及び遮光膜１５４上に設けられた第２の基板１５２と、を有する。

【００４５】

なお、画素電極１２２と、第１の配向膜１２４と、液晶層１６２と、第２の配向膜１６４と、対向電極１５８と、により表示素子である液晶素子１５０が形成されている。

【００４６】

ゲートドライバ回路部１４０において、第１の基板１０２と、第１の基板１０２上に形成されたゲート電極１０４と、ゲート電極１０４上に形成されたゲート絶縁膜１０６と、ゲート絶縁膜１０６と接し、ゲート電極１０４と重畳する位置に設けられた半導体層１０８と、ゲート絶縁膜１０６、及び半導体層１０８上に形成されたソース電極１１０及びドレイン電極１１２と、により、第２のトランジスタ１０３、及び第３のトランジスタ１０５が形成されている。

【００４７】

また、ゲートドライバ回路部１４０において、第２のトランジスタ１０３及び第３のトランジスタ１０５上、より詳しくはゲート絶縁膜１０６、及び半導体層１０８、ソース電極１１０、及びドレイン電極１１２上に形成された第１の層間絶縁膜１１４と、第１の層間絶縁膜１１４上に形成された第２の層間絶縁膜１１６が形成されている。

【００４８】

すなわち、第３の層間絶縁膜１２０は、画素領域１４２上の一部に設けられ、第３の層間絶縁膜１２０の端部が駆動回路領域であるゲートドライバ回路部１４０よりも内側に形成される。

【００４９】

このような構成とすることによって、外部から取り込まれる水分、または表示装置内部で生じた水分、水素等のガスをゲートドライバ回路部１４０の第２の層間絶縁膜１１６から上部へ放出することができる。したがって、第１のトランジスタ１０１、第２のトランジスタ１０３、及び第３のトランジスタ１０５内部に水分、水素等のガスが取り込まれるのを抑制することができる。

【００５０】

なお、有機絶縁材料により形成される第２の層間絶縁膜１１６は、表示装置を構成するトランジスタの凹凸等を低減するために、平坦性の高い有機絶縁材料が必要とされる。これは、トランジスタの凹凸等を低減することにより、表示装置の画質を向上させることができるためである。しかしながら、該有機絶縁材料は加熱等により、水素、水分、または有機成分をガスとして放出してしまう。

【００５１】

しかし、半導体層１０８に、例えば、シリコン系半導体材料であるシリコン膜を用いたトランジスタにおいては、上述の水素、水分、または有機成分のガスが大きな問題になる可能性が低い。しかし、本発明の一態様においては、半導体層１０８に酸化物半導体膜を

用いるため、有機絶縁材料により形成される第２の層間絶縁膜１１６からのガスを外部に好適に放出させる必要がある。なお、第３の層間絶縁膜１２０の端部が駆動回路領域であるゲートドライバ回路部１４０よりも内側に形成される構成は、半導体層１０８を酸化物半導体膜により形成した場合において、優れた効果を奏する。ただし、半導体層１０８に酸化物半導体以外の材料（例えば、シリコン系半導体材料である非晶質シリコン、結晶性シリコンなど）により形成したトランジスタにおいても、同様の効果が得られる。

【００５２】

また、有機絶縁材料で形成された第２の層間絶縁膜１１６上に形成される無機絶縁材料で形成された第３の層間絶縁膜１２０は、本実施の形態においては、容量素子１０７の誘電体として用いる。また、無機絶縁材料で形成された第３の層間絶縁膜１２０は、外部から第２の層間絶縁膜１１６に入り込む水素、水分等を抑制することができる。

【００５３】

しかしながら、第３の層間絶縁膜１２０をゲートドライバ回路部１４０に用いる第２のトランジスタ１０３及び第３のトランジスタ１０５上の第２の層間絶縁膜１１６上に形成すると、第２の層間絶縁膜１１６に用いる有機絶縁材料から放出されるガスを外部に拡散することができず、第２のトランジスタ１０３、及び第３のトランジスタ１０５内部に入り込む。

【００５４】

上述した有機絶縁材料から放出されるガスが、トランジスタの半導体層１０８に用いる酸化物半導体に入り込むと、酸化物半導体膜中で不純物として取り込まれ、該半導体層１０８を用いたトランジスタの特性が変動してしまう。

【００５５】

しかし、図１（Ｂ）に示すように、ゲートドライバ回路部１４０に用いる第２のトランジスタ１０３、及び第３のトランジスタ１０５上の第３の層間絶縁膜１２０が開口された構成、すなわち第３の層間絶縁膜１２０が、画素領域１４２の一部に設けられ、第３の層間絶縁膜１２０の端部がゲートドライバ回路部１４０よりも内側に形成される構成とすることによって、第２の層間絶縁膜１１６から放出されるガスを、外部へ拡散できる構造とすることができる。

【００５６】

なお、図１（Ｂ）に示すように、画素領域１４２に用いる第１のトランジスタ１０１においても、半導体層１０８の重畳する位置の無機絶縁材料で形成された第３の層間絶縁膜１２０が除去された構成が好ましい。このような構成とすることで、有機絶縁材料で形成された第２の層間絶縁膜１１６から放出されるガスが、第１のトランジスタ１０１への入り込むのを抑制することができる。

【００５７】

ここで、図１及び図２に示す表示装置の他の構成要素について、以下詳細な説明を行う。

【００５８】

第１の基板１０２及び第２の基板１５２としては、アルミノシリケートガラス、アルミノホウケイ酸ガラス、バリウムホウケイ酸ガラスなどのガラス材料を用いる。量産する上では、第１の基板１０２及び第２の基板１５２は、第８世代（２１６０ｍｍ×２４６０ｍｍ）、第９世代（２４００ｍｍ×２８００ｍｍ、または２４５０ｍｍ×３０５０ｍｍ）、第１０世代（２９５０ｍｍ×３４００ｍｍ）等のマザーガラスを用いることが好ましい。マザーガラスは、処理温度が高く、処理時間が長いと大幅に収縮するため、マザーガラスを使用して量産を行う場合、作製工程の加熱処理は、好ましくは６００℃以下、さらに好ましくは４５０℃以下、さらに好ましくは３５０℃以下とすることが望ましい。

【００５９】

なお、第１の基板１０２及びゲート電極１０４の間に下地絶縁膜を設けてもよい。下地絶縁膜としては、酸化シリコン膜、酸化窒化シリコン膜、窒化シリコン膜、窒化酸化シリコン膜、酸化ガリウム膜、酸化ハフニウム膜、酸化イットリウム膜、酸化アルミニウム膜

、酸化窒化アルミニウム膜等がある。なお、下地絶縁膜として、窒化シリコン膜、酸化ガリウム膜、酸化ハフニウム膜、酸化イットリウム膜、酸化アルミニウム膜等を用いることで、第１の基板１０２から不純物、代表的にはアルカリ金属、水、水素等の半導体層１０８へ入り込むのを抑制することができる。

【００６０】

ゲート電極１０４としては、アルミニウム、クロム、銅、タンタル、チタン、モリブデン、タングステンから選ばれた金属元素、または上述した金属元素を成分とする合金か、上述した金属元素を組み合わせた合金等を用いて形成することができる。また、マンガン、ジルコニウムのいずれか一または複数から選択された金属元素を用いてもよい。また、ゲート電極１０４は、単層構造でも、二層以上の積層構造としてもよい。例えば、シリコンを含むアルミニウム膜の単層構造、アルミニウム膜上にチタン膜を積層する二層構造、窒化チタン膜上にチタン膜を積層する二層構造、窒化チタン膜上にタングステン膜を積層する二層構造、窒化タンタル膜または窒化タングステン膜上にタングステン膜を積層する二層構造、チタン膜と、そのチタン膜上にアルミニウム膜を積層し、さらにその上にチタン膜を形成する三層構造等がある。また、アルミニウムに、チタン、タンタル、タングステン、モリブデン、クロム、ネオジム、スカンジウムから選ばれた元素の膜、または複数組み合わせた合金膜、もしくは窒化膜を用いてもよい。

【００６１】

また、ゲート電極１０４は、インジウム錫酸化物、酸化タングステンを含むインジウム酸化物、酸化タングステンを含むインジウム亜鉛酸化物、酸化チタンを含むインジウム酸化物、酸化チタンを含むインジウム錫酸化物、インジウム亜鉛酸化物、酸化シリコンを添加したインジウム錫酸化物等の透光性を有する導電性材料を適用することもできる。また、上記透光性を有する導電性材料と、上記金属元素の積層構造とすることもできる。

【００６２】

また、ゲート電極１０４とゲート絶縁膜１０６との間に、Ｉｎ－Ｇａ－Ｚｎ系酸窒化物半導体膜、Ｉｎ－Ｓｎ系酸窒化物半導体膜、Ｉｎ－Ｇａ系酸窒化物半導体膜、Ｉｎ－Ｚｎ系酸窒化物半導体膜、Ｓｎ系酸窒化物半導体膜、Ｉｎ系酸窒化物半導体膜、金属窒化膜（ＩｎＮ、ＺｎＮ等）等を設けてもよい。これらの膜は５ｅＶ、好ましくは５．５ｅＶ以上の仕事関数を有し、酸化物半導体の電子親和力よりも大きい値であるため、酸化物半導体を用いたトランジスタのしきい値電圧をプラスにシフトすることができ、所謂ノーマリーオフ特性のスイッチング素子を実現できる。例えば、Ｉｎ－Ｇａ－Ｚｎ系酸窒化物半導体膜を用いる場合、少なくとも半導体層１０８より高い窒素濃度、具体的には７原子％以上のＩｎ－Ｇａ－Ｚｎ系酸窒化物半導体膜を用いる。

【００６３】

ゲート絶縁膜１０６としては、例えば酸化シリコン膜、酸化窒化シリコン膜、窒化酸化シリコン膜、窒化シリコン膜、酸化アルミニウム膜、酸化ハフニウム膜、酸化ガリウム膜またはＧａ－Ｚｎ系金属酸化物、窒化シリコン膜、窒化酸化シリコン膜などを用いればよく、積層または単層で設ける。なお、半導体層１０８との界面特性を向上させるため、ゲート絶縁膜１０６において少なくとも半導体層１０８と接する領域は酸化絶縁膜で形成することが好ましい。

【００６４】

また、ゲート絶縁膜１０６に、酸素、水素、水等のブロッキング効果を有する絶縁膜を設けることで、半導体層１０８からの酸素の外部への拡散と、外部から半導体層１０８への水素、水等の入り込むのを防ぐことができる。酸素、水素、水等のブロッキング効果を有する絶縁膜としては、酸化アルミニウム、酸化窒化アルミニウム、酸化ガリウム、酸化窒化ガリウム、酸化イットリウム、酸化窒化イットリウム、酸化ハフニウム、酸化窒化ハフニウム等がある。

【００６５】

また、ゲート絶縁膜１０６を積層構造とし、第１の窒化シリコン膜として、欠陥が少ない窒化シリコン膜とし、第１の窒化シリコン膜上に、第２の窒化シリコン膜として、水素

放出量及びアンモニア放出量の少ない窒化シリコン膜を設け、第２の窒化シリコン膜上に酸化絶縁膜を設けることで、ゲート絶縁膜１０６として、欠陥が少なく、且つ水素及びアンモニアの放出量の少ないゲート絶縁膜１０６を形成することができる。この結果、ゲート絶縁膜１０６に含まれる水素及び窒素が、半導体層１０８への移動を抑制することが可能である。

【００６６】

また、ゲート絶縁膜１０６に窒化シリコン膜を用いることで、以下の効果を得ることができる。窒化シリコン膜は、酸化シリコン膜と比較して比誘電率が高く、同等の静電容量を得るのに必要な膜厚が大きいため、ゲート絶縁膜を物理的に厚膜化することができる。よって、第１のトランジスタ１０１、第２のトランジスタ１０３、及び第３のトランジスタ１０５の絶縁耐圧の低下を抑制、さらには絶縁耐圧を向上させて、表示装置に用いるトランジスタの静電破壊を抑制することができる。

【００６７】

また、ゲート電極１０４として銅を用い、ゲート電極１０４に接するゲート絶縁膜１０６に窒化シリコン膜を用いる場合、銅とアンモニア分子が反応することを抑制するために当該窒化シリコン膜は、加熱によるアンモニア分子放出量をできる限り低減することが好ましい。

【００６８】

酸化物半導体膜を半導体層１０８に用いるトランジスタにおいて、酸化物半導体膜及びゲート絶縁膜の界面またはゲート絶縁膜中に捕獲準位（界面準位ともいう。）があると、トランジスタのしきい値電圧の変動、代表的にはしきい値電圧のマイナスシフト、及びトランジスタがオン状態となるときにドレイン電流が一桁変化するのに必要なゲート電圧を示すサブスレッショルド係数（Ｓ値）の増大の原因となる。この結果、トランジスタごとに電気特性がばらつくという問題がある。このため、ゲート絶縁膜として、欠陥の少ない窒化シリコン膜を用いることで、しきい値電圧のマイナスシフト、及びトランジスタの電気特性のばらつきを低減することができる。

【００６９】

また、ゲート絶縁膜１０６として、ハフニウムシリケート（$HfSiO_x$）、窒素が添加されたハフニウムシリケート（$HfSi_xO_yN_z$）、窒素が添加されたハフニウムアルミネート（$HfAl_xO_yN_z$）、酸化ハフニウム、酸化イットリウムなどのｈｉｇｈ－ｋ材料を用いることでトランジスタのゲートリークを低減できる。

【００７０】

ゲート絶縁膜１０６の厚さは、５ｎｍ以上４００ｎｍ以下、より好ましくは１０ｎｍ以上３００ｎｍ以下、より好ましくは５０ｎｍ以上２５０ｎｍ以下とするとよい。

【００７１】

半導体層１０８は、酸化物半導体を用い、少なくともインジウム（Ｉｎ）若しくは亜鉛（Ｚｎ）を含むことが好ましい。または、ＩｎとＺｎの双方を含むことが好ましい。また、該酸化物半導体を用いたトランジスタの電気特性のばらつきを減らすため、それらと共に、スタビライザーの一または複数を有することが好ましい。

【００７２】

スタビライザーとしては、ガリウム（Ｇａ）、スズ（Ｓｎ）、ハフニウム（Ｈｆ）、アルミニウム（Ａｌ）、またはジルコニウム（Ｚｒ）等がある。また、他のスタビライザーとしては、ランタノイドである、ランタン（Ｌａ）、セリウム（Ｃｅ）、プラセオジム（Ｐｒ）、ネオジム（Ｎｄ）、サマリウム（Ｓｍ）、ユウロピウム（Ｅｕ）、ガドリニウム（Ｇｄ）、テルビウム（Ｔｂ）、ジスプロシウム（Ｄｙ）、ホルミウム（Ｈｏ）、エルビウム（Ｅｒ）、ツリウム（Ｔｍ）、イッテルビウム（Ｙｂ）、ルテチウム（Ｌｕ）等がある。

【００７３】

例えば、酸化物半導体として、酸化インジウム、酸化スズ、酸化亜鉛、二元系金属酸化物であるＩｎ－Ｚｎ系金属酸化物、Ｓｎ－Ｚｎ系金属酸化物、Ａｌ－Ｚｎ系金属酸化物、

Ｚｎ－Ｍｇ系金属酸化物、Ｓｎ－Ｍｇ系金属酸化物、Ｉｎ－Ｍｇ系金属酸化物、Ｉｎ－Ｇａ系金属酸化物、Ｉｎ－Ｗ系金属酸化物、三元系金属酸化物であるＩｎ－Ｇａ－Ｚｎ系金属酸化物（ＩＧＺＯとも表記する）、Ｉｎ－Ａｌ－Ｚｎ系金属酸化物、Ｉｎ－Ｓｎ－Ｚｎ系金属酸化物、Ｓｎ－Ｇａ－Ｚｎ系金属酸化物、Ａｌ－Ｇａ－Ｚｎ系金属酸化物、Ｓｎ－Ａｌ－Ｚｎ系金属酸化物、Ｉｎ－Ｈｆ－Ｚｎ系金属酸化物、Ｉｎ－Ｌａ－Ｚｎ系金属酸化物、Ｉｎ－Ｃｅ－Ｚｎ系金属酸化物、Ｉｎ－Ｐｒ－Ｚｎ系金属酸化物、Ｉｎ－Ｎｄ－Ｚｎ系金属酸化物、Ｉｎ－Ｓｍ－Ｚｎ系金属酸化物、Ｉｎ－Ｅｕ－Ｚｎ系金属酸化物、Ｉｎ－Ｇｄ－Ｚｎ系金属酸化物、Ｉｎ－Ｔｂ－Ｚｎ系金属酸化物、Ｉｎ－Ｄｙ－Ｚｎ系金属酸化物、Ｉｎ－Ｈｏ－Ｚｎ系金属酸化物、Ｉｎ－Ｅｒ－Ｚｎ系金属酸化物、Ｉｎ－Ｔｍ－Ｚｎ系金属酸化物、Ｉｎ－Ｙｂ－Ｚｎ系金属酸化物、Ｉｎ－Ｌｕ－Ｚｎ系金属酸化物、四元系金属酸化物であるＩｎ－Ｓｎ－Ｇａ－Ｚｎ系金属酸化物、Ｉｎ－Ｈｆ－Ｇａ－Ｚｎ系金属酸化物、Ｉｎ－Ａｌ－Ｇａ－Ｚｎ系金属酸化物、Ｉｎ－Ｓｎ－Ａｌ－Ｚｎ系金属酸化物、Ｉｎ－Ｓｎ－Ｈｆ－Ｚｎ系金属酸化物、Ｉｎ－Ｈｆ－Ａｌ－Ｚｎ系金属酸化物を用いることができる。

【００７４】

なお、ここで、例えば、Ｉｎ－Ｇａ－Ｚｎ系金属酸化物とは、ＩｎとＧａとＺｎを主成分として有する酸化物という意味であり、ＩｎとＧａとＺｎの比率は問わない。また、ＩｎとＧａとＺｎ以外の金属元素が入っていてもよい。

【００７５】

また、酸化物半導体として、$InMO_3(ZnO)_m$（ｍ＞０、且つ、ｍは整数でない）で表記される材料を用いてもよい。なお、Ｍは、Ｇａ、Ｆｅ、Ｍｎ及びＣｏから選ばれた一の金属元素または複数の金属元素を示す。また、酸化物半導体として、$In_2SnO_5(ZnO)_n$（ｎ＞０、且つ、ｎは整数）で表記される材料を用いてもよい。

【００７６】

例えば、Ｉｎ：Ｇａ：Ｚｎ＝１：１：１（＝１／３：１／３：１／３）、Ｉｎ：Ｇａ：Ｚｎ＝２：２：１（＝２／５：２／５：１／５）、あるいはＩｎ：Ｇａ：Ｚｎ＝３：１：２（＝１／２：１／６：１／３）の原子数比のＩｎ－Ｇａ－Ｚｎ系金属酸化物やその組成の近傍の酸化物を用いることができる。あるいは、Ｉｎ：Ｓｎ：Ｚｎ＝１：１：１（＝１／３：１／３：１／３）、Ｉｎ：Ｓｎ：Ｚｎ＝２：１：３（＝１／３：１／６：１／２）あるいはＩｎ：Ｓｎ：Ｚｎ＝２：１：５（＝１／４：１／８：５／８）の原子数比のＩｎ－Ｓｎ－Ｚｎ系金属酸化物を用いるとよい。なお、金属酸化物の原子数比は、誤差として上記の原子数比のプラスマイナス２０％の変動を含む。

【００７７】

しかし、これらに限られず、必要とする半導体特性及び電気特性（電界効果移動度、しきい値電圧、ばらつき等）に応じて適切な組成のものを用いればよい。また、必要とする半導体特性を得るために、キャリア密度や不純物濃度、欠陥密度、金属元素と酸素の原子数比、原子間距離、密度等を適切なものとすることが好ましい。

【００７８】

例えば、Ｉｎ－Ｓｎ－Ｚｎ系金属酸化物では比較的容易に高い移動度が得られる。しかしながら、Ｉｎ－Ｇａ－Ｚｎ系金属酸化物でも、バルク内欠陥密度を低くすることにより電界効果移動度を上げることができる。

【００７９】

また、半導体層１０８として用いることのできる酸化物半導体膜としては、エネルギーギャップが２ｅＶ以上、好ましくは２．５ｅＶ以上、より好ましくは３ｅＶ以上である。このように、エネルギーギャップの広い酸化物半導体膜を用いることで、トランジスタのオフ電流を低減することができる。

【００８０】

また、半導体層１０８として用いる酸化物半導体膜は、非晶質構造、単結晶構造、または多結晶構造であってもよい。

【００８１】

また、半導体層１０８として用いる酸化物半導体膜として、結晶化した部分を有するＣＡＡＣ－ＯＳ（Ｃ　Ａｘｉｓ　Ａｌｉｇｎｅｄ　Ｃｒｙｓｔａｌｌｉｎｅ　Ｏｘｉｄｅ　Ｓｅｍｉｃｏｎｄｕｃｔｏｒともいう。）膜を用いてもよい。

【００８２】

ＣＡＡＣ－ＯＳ膜は、完全な単結晶ではなく、完全な非晶質でもない。ＣＡＡＣ－ＯＳ膜は、非晶質相に結晶部及び非晶質部を有する結晶－非晶質混相構造の酸化物半導体膜である。なお、当該結晶部は、一辺が１００ｎｍ未満の立方体内に収まる大きさであることが多い。また、透過型電子顕微鏡（ＴＥＭ：Ｔｒａｎｓｍｉｓｓｉｏｎ　Ｅｌｅｃｔｒｏｎ　Ｍｉｃｒｏｓｃｏｐｅ）による観察像では、ＣＡＡＣ－ＯＳ膜に含まれる非晶質部と結晶部との境界は明確ではない。また、ＴＥＭによってＣＡＡＣ－ＯＳ膜には粒界（グレインバウンダリーともいう。）は確認できない。そのため、ＣＡＡＣ－ＯＳ膜は、粒界に起因する電子移動度の低下が抑制される。

【００８３】

ＣＡＡＣ－ＯＳ膜に含まれる結晶部は、ｃ軸がＣＡＡＣ－ＯＳ膜の被形成面の法線ベクトルまたは表面の法線ベクトルに平行な方向に揃い、かつａｂ面に垂直な方向から見て三角形状または六角形状の原子配列を有し、ｃ軸に垂直な方向から見て金属原子が層状または金属原子と酸素原子とが層状に配列している。なお、異なる結晶部間で、それぞれａ軸及びｂ軸の向きが異なっていてもよい。本明細書において、単に垂直と記載する場合、８５°以上９５°以下の範囲も含まれることとする。また、単に平行と記載する場合、－５°以上５°以下の範囲も含まれることとする。なお、酸化物半導体膜を構成する酸素の一部は窒素で置換されてもよい。

【００８４】

なお、ＣＡＡＣ－ＯＳ膜において、結晶部の分布が一様でなくてもよい。例えば、ＣＡＡＣ－ＯＳ膜の形成過程において、酸化物半導体膜の表面側から結晶成長させる場合、被形成面の近傍に対し表面の近傍では結晶部の占める割合が高くなることがある。また、ＣＡＡＣ－ＯＳ膜へ不純物を添加することにより、当該不純物添加領域において結晶部が非晶質化することもある。

【００８５】

ＣＡＡＣ－ＯＳ膜に含まれる結晶部のｃ軸は、ＣＡＡＣ－ＯＳ膜の被形成面の法線ベクトルまたは表面の法線ベクトルに平行な方向に揃うため、ＣＡＡＣ－ＯＳ膜の形状（被形成面の断面形状または表面の断面形状）によっては互いに異なる方向を向くことがある。なお、結晶部のｃ軸の方向は、ＣＡＡＣ－ＯＳ膜が形成されたときの被形成面の法線ベクトルまたは表面の法線ベクトルに平行な方向となる。結晶部は、成膜することにより、または成膜後に加熱処理などの結晶化処理を行うことにより形成される。

【００８６】

ＣＡＡＣ－ＯＳ膜を用いたトランジスタは、可視光や紫外光の照射による電気特性の変動を抑制することが可能である。よって、当該トランジスタは、信頼性が高い。

【００８７】

また、ＣＡＡＣ－ＯＳ膜は、例えば、多結晶である酸化物半導体スパッタリング用ターゲットを用い、スパッタリング法によって成膜する。当該スパッタリング用ターゲットにイオンが衝突すると、スパッタリング用ターゲットに含まれる結晶領域がａ－ｂ面から劈開し、ａ－ｂ面に平行な面を有する平板状またはペレット状のスパッタリング粒子として剥離することがある。この場合、当該平板状のスパッタリング粒子が、結晶状態を維持したまま基板に到達することで、ＣＡＡＣ－ＯＳ膜を成膜することができる。

【００８８】

また、ＣＡＡＣ－ＯＳ膜を成膜するために、以下の条件を適用することが好ましい。

【００８９】

成膜時の不純物混入を低減することで、不純物によって結晶状態が崩れることを抑制できる。例えば、成膜室内に存在する不純物濃度（水素、水、二酸化炭素および窒素など）を低減すればよい。また、成膜ガス中の不純物濃度を低減すればよい。具体的には、露点

が－８０℃以下、好ましくは－１００℃以下である成膜ガスを用いる。
【００９０】
また、成膜時の基板加熱温度を高めることで、基板到達後にスパッタリング粒子のマイグレーションが起こる。具体的には、基板加熱温度を１００℃以上７４０℃以下、好ましくは１５０℃以上５００℃以下として成膜する。成膜時の基板加熱温度を高めることで、平板状のスパッタリング粒子が基板に到達した場合、基板上でマイグレーションが起こり、スパッタリング粒子の平らな面が基板に付着する。
【００９１】
また、成膜ガス中の酸素割合を高め、電力を最適化することで成膜時のプラズマダメージを軽減すると好ましい。成膜ガス中の酸素割合は、３０体積％以上、好ましくは１００体積％とする。
【００９２】
また、半導体層１０８として用いる酸化物半導体膜は、複数の酸化物半導体膜が積層された構造でもよい。例えば、酸化物半導体膜を、第１の酸化物半導体膜と第２の酸化物半導体膜の積層として、第１の酸化物半導体膜と第２の酸化物半導体膜に、異なる組成の金属酸化物を用いてもよい。例えば、第１の酸化物半導体膜に二元系金属酸化物乃至四元系金属酸化物の一を用い、第２の酸化物半導体膜に第１の酸化物半導体膜と異なる二元系金属酸化物乃至四元系金属酸化物を用いてもよい。
【００９３】
また、第１の酸化物半導体膜と第２の酸化物半導体膜の構成元素を同一とし、両者の組成を異ならせてもよい。例えば、第１の酸化物半導体膜の原子数比をＩｎ：Ｇａ：Ｚｎ＝１：１：１とし、第２の酸化物半導体膜の原子数比をＩｎ：Ｇａ：Ｚｎ＝３：１：２としてもよい。また、第１の酸化物半導体膜の原子数比をＩｎ：Ｇａ：Ｚｎ＝１：３：２とし、第２の酸化物半導体膜の原子数比をＩｎ：Ｇａ：Ｚｎ＝２：１：３としてもよい。なお、各酸化物半導体膜の原子数比は、誤差として上記の原子数比のプラスマイナス２０％の変動を含む。
【００９４】
この時、第１の酸化物半導体膜と第２の酸化物半導体膜のうち、ゲート電極に近い側（チャネル側）の酸化物半導体膜のＩｎとＧａの含有率をＩｎ＞Ｇａとするとよい。またゲート電極から遠い側（バックチャネル側）の酸化物半導体膜のＩｎとＧａの含有率をＩｎ≦Ｇａとするとよい。
【００９５】
また、酸化物半導体膜を３層構造とし、第１の酸化物半導体膜～第３の酸化物半導体膜の構成元素を同一とし、且つそれぞれの組成を異ならせてもよい。例えば、第１の酸化物半導体膜の原子数比をＩｎ：Ｇａ：Ｚｎ＝１：３：２とし、第２の酸化物半導体膜の原子数比をＩｎ：Ｇａ：Ｚｎ＝３：１：２とし、第３の酸化物半導体膜の原子数比をＩｎ：Ｇａ：Ｚｎ＝１：１：１としてもよい。
【００９６】
Ｇａ及びＺｎよりＩｎの原子数比が小さい酸化物半導体膜、代表的には原子数比がＩｎ：Ｇａ：Ｚｎ＝１：３：２である第１の酸化物半導体膜は、Ｇａ及びＺｎよりＩｎの原子数比が大きい酸化物半導体膜、代表的には第２の酸化物半導体膜、並びにＧａ、Ｚｎ、及びＩｎの原子数比が同じ酸化物半導体膜、代表的には第３の酸化物半導体膜と比較して、酸素欠損が生じにくいため、キャリア密度が増加することを抑制することができる。また、原子数比がＩｎ：Ｇａ：Ｚｎ＝１：３：２である第１の酸化物半導体膜が非晶質構造であると、第２の酸化物半導体膜がＣＡＡＣ－ＯＳ膜となりやすい。
【００９７】
また、第１の酸化物半導体膜～第３の酸化物半導体膜の構成元素は同一であるため、第１の酸化物半導体膜は、第２の酸化物半導体膜との界面におけるトラップ準位が少ない。このため、酸化物半導体膜を上記構造とすることで、トランジスタの経時変化や光劣化によるしきい値電圧の変動量を低減することができる。

【００９８】
酸化物半導体では主として重金属のｓ軌道がキャリア伝導に寄与しており、Ｉｎの含有率を多くすることにより、より多くのｓ軌道が重なるため、Ｉｎ＞Ｇａの組成となる酸化物はＩｎ≦Ｇａの組成となる酸化物と比較して高いキャリア移動度を備える。また、ＧａはＩｎと比較して酸素欠損の形成エネルギーが大きく酸素欠損が生じにくいため、Ｉｎ≦Ｇａの組成となる酸化物はＩｎ＞Ｇａの組成となる酸化物と比較して安定した特性を備える。
【００９９】
チャネル側にＩｎ＞Ｇａの組成となる酸化物半導体を適用し、バックチャネル側にＩｎ≦Ｇａの組成となる酸化物半導体を適用することで、トランジスタの電界効果移動度及び信頼性をさらに高めることが可能となる。
【０１００】
また、第１の酸化物半導体膜乃至第３の酸化物半導体膜に、結晶性の異なる酸化物半導体を適用してもよい。すなわち、単結晶酸化物半導体、多結晶酸化物半導体、非晶質酸化物半導体、またはＣＡＡＣ－ＯＳを適宜組み合わせた構成としてもよい。また、第１の酸化物半導体膜乃至第２の酸化物半導体膜のいずれか一に非晶質酸化物半導体を適用すると、酸化物半導体膜の内部応力や外部からの応力を緩和し、トランジスタの特性ばらつきが低減され、また、トランジスタの信頼性をさらに高めることが可能となる。
【０１０１】
酸化物半導体膜の厚さは、１ｎｍ以上１００ｎｍ以下、更に好ましくは１ｎｍ以上３０ｎｍ以下、更に好ましくは１ｎｍ以上５０ｎｍ以下、更に好ましくは３ｎｍ以上２０ｎｍ以下とすることが好ましい。
【０１０２】
半導体層１０８に用いる酸化物半導体膜において、二次イオン質量分析法（ＳＩＭＳ：Ｓｅｃｏｎｄａｒｙ　Ｉｏｎ　Ｍａｓｓ　Ｓｐｅｃｔｒｏｍｅｔｒｙ）により得られるアルカリ金属またはアルカリ土類金属の濃度を、１×１０^{18}ａｔｏｍｓ／ｃｍ^{3}以下、さらに好ましくは２×１０^{16}ａｔｏｍｓ／ｃｍ^{3}以下であることが望ましい。アルカリ金属及びアルカリ土類金属は、酸化物半導体と結合するとキャリアを生成する場合があり、トランジスタのオフ電流の上昇の原因となるためである。
【０１０３】
また、半導体層１０８に用いる酸化物半導体膜において、二次イオン質量分析法により得られる水素濃度を、５×１０^{18}ａｔｏｍｓ／ｃｍ^{3}未満、好ましくは１×１０^{18}ａｔｏｍｓ／ｃｍ^{3}以下、より好ましくは５×１０^{17}ａｔｏｍｓ／ｃｍ^{3}以下、さらに好ましくは１×１０^{16}ａｔｏｍｓ／ｃｍ^{3}以下とすることが好ましい。
【０１０４】
酸化物半導体膜に含まれる水素は、金属原子と結合する酸素と反応して水となると共に、酸素が脱離した格子（あるいは酸素が脱理した部分）には欠損が形成されてしまう。また、水素の一部が酸素と結合することで、キャリアである電子が生じてしまう。これらのため、酸化物半導体膜の成膜工程において、水素を含む不純物を極めて減らすことにより、酸化物半導体膜の水素濃度を低減することが可能である。このため、水素をできるだけ除去された酸化物半導体膜をチャネル領域とすることにより、しきい値電圧のマイナスシフトを抑制することができると共に、電気特性のばらつきを低減することができる。また、トランジスタのソース及びドレインにおけるリーク電流を、代表的には、オフ電流を低減することが可能である。
【０１０５】
また、半導体層１０８に用いる酸化物半導体膜の窒素濃度を５×１０^{18}ａｔｏｍｓ／ｃｍ^{3}以下とすることで、トランジスタのしきい値電圧のマイナスシフトを抑制することができると共に、電気特性のばらつきを低減することができる。
【０１０６】
なお、水素をできるだけ除去することで高純度化された酸化物半導体膜をチャネル領域

に用いたトランジスタのオフ電流が低いことは、いろいろな実験により証明できる。例えば、チャネル幅が１×１０６μｍでチャネル長が１０μｍのトランジスタであっても、ソース電極とドレイン電極間の電圧（ドレイン電圧）が１Ｖから１０Ｖの範囲において、オフ電流が、半導体パラメータアナライザの測定限界以下、すなわち１×１０－１３Ａ以下という特性を得ることができる。この場合、オフ電流をトランジスタのチャネル幅で除した数値に相当するオフ電流は、１００ｚＡ／μｍ以下であることが分かる。また、容量素子とトランジスタとを接続して、容量素子に流入または容量素子から流出する電荷を当該トランジスタで制御する回路を用いて、オフ電流の測定を行った。当該測定では、上記トランジスタに高純度化された酸化物半導体膜をチャネル領域に用い、容量素子の単位時間あたりの電荷量の推移から当該トランジスタのオフ電流を測定した。その結果、トランジスタのソース電極とドレイン電極間の電圧が３Ｖの場合に、数十ｙＡ／μｍという、さらに低いオフ電流が得られることが分かった。従って、高純度化された酸化物半導体膜をチャネル領域に用いたトランジスタは、オフ電流が著しく小さい。

【０１０７】

ソース電極１１０及びドレイン電極１１２としては、導電材料として、アルミニウム、チタン、クロム、ニッケル、銅、イットリウム、ジルコニウム、モリブデン、銀、タンタル、またはタングステンからなる単体金属、またはこれを主成分とする合金を単層構造または積層構造として用いる。例えば、シリコンを含むアルミニウム膜の単層構造、アルミニウム膜上にチタン膜を積層する二層構造、タングステン膜上にチタン膜を積層する二層構造、銅―マグネシウム―アルミニウム合金膜上に銅膜を積層する二層構造、チタン膜または窒化チタン膜と、そのチタン膜または窒化チタン膜上に重ねてアルミニウム膜または銅膜を積層し、さらにその上にチタン膜または窒化チタン膜を形成する三層構造、モリブデン膜または窒化モリブデン膜と、そのモリブデン膜または窒化モリブデン膜上に重ねてアルミニウム膜または銅膜を積層し、さらにその上にモリブデン膜または窒化モリブデン膜を形成する三層構造等がある。なお、酸化インジウム、酸化錫または酸化亜鉛を含む透明導電材料を用いてもよい。

【０１０８】

なお、本実施の形態では、ソース電極１１０及びドレイン電極１１２を半導体層１０８上に設けたが、ゲート絶縁膜１０６と半導体層１０８の間に設けても良い。

【０１０９】

第１の層間絶縁膜１１４としては、半導体層１０８として用いる酸化物半導体膜との界面特性を向上させるため、酸化物絶縁膜を用いることが好ましい。第１の層間絶縁膜１１４としては、厚さ１５０ｎｍ以上４００ｎｍ以下の酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウム膜、酸化ハフニウム膜、酸化ガリウム膜、またはＧａ－Ｚｎ系金属酸化物等を用いることができる。また、第１の層間絶縁膜１１４としては、酸化物絶縁膜と窒化物絶縁膜との積層構造としてもよい。例えば、第１の層間絶縁膜１１４として、酸化窒化シリコン膜と、窒化シリコン膜との積層構造とすることができる。

【０１１０】

第２の層間絶縁膜１１６としては、アクリル系樹脂、ポリイミド系樹脂、ベンゾシクロブテン系樹脂、ポリアミド系樹脂、エポキシ系樹脂等の、耐熱性を有する有機絶縁材料を用いることができる。なお、これらの材料で形成される絶縁膜を複数積層させることで、第２の層間絶縁膜１１６を形成してもよい。第２の層間絶縁膜１１６を用いることにより、第１のトランジスタ１０１等の凹凸を平坦化させることが可能となる。

【０１１１】

容量電極１１８としては、酸化タングステンを含むインジウム酸化物、酸化タングステンを含むインジウム亜鉛酸化物、酸化チタンを含むインジウム酸化物、酸化チタンを含むインジウム錫酸化物、インジウム錫酸化物（以下、ＩＴＯと示す。）、インジウム亜鉛酸化物、酸化ケイ素を添加したインジウム錫酸化物などの透光性を有する導電性材料を用いることができる。

【０１１２】

第３の層間絶縁膜１２０としては、酸化シリコン膜、酸化窒化シリコン膜、窒化酸化シリコン膜、窒化シリコン膜、酸化アルミニウム膜などの無機絶縁材料を用いることができる。特に、第３の層間絶縁膜１２０としては、窒化シリコン膜、窒化酸化シリコン膜、酸化アルミニウム膜の中から選ばれたいずれか一であることが好ましい。窒化シリコン膜、窒化酸化シリコン膜、酸化アルミニウム膜の中から選ばれたいずれか一を第３の層間絶縁膜１２０として用いることにより、第２の層間絶縁膜１１６からの水素、水分の放出を抑制することができる。

【０１１３】

画素電極１２２としては、容量電極１１８に示す材料と同様の材料を用いることができる。容量電極１１８と画素電極１２２に用いる材料としては、同一の材料、または異なる材料を用いても良いが、同一の材料の方が、製造コストを低減できるため好ましい。

【０１１４】

第１の配向膜１２４及び第２の配向膜１６４としては、アクリル系樹脂、ポリイミド系樹脂、ベンゾシクロブテン系樹脂、ポリアミド系樹脂、エポキシ系樹脂等の、耐熱性を有する有機材料を用いることができる。

【０１１５】

液晶層１６２としては、サーモトロピック液晶、低分子液晶、高分子液晶、高分子分散型液晶、強誘電性液晶、反強誘電性液晶等の液晶材料を用いることができる。これらの液晶材料は、条件により、コレステリック相、スメクチック相、キュービック相、カイラルネマチック相、等方相等を示す。

【０１１６】

また、横電界方式を採用する場合、配向膜（第１の配向膜１２４及び第２の配向膜１６４）を用いないブルー相を示す液晶を用いてもよい。ブルー相は液晶相の一つであり、コレステリック液晶を昇温していくと、コレステリック相から等方相へ転移する直前に発現する相である。ブルー相は狭い温度範囲でしか発現しないため、温度範囲を改善するために数重量％以上のカイラル剤を混合させた液晶組成物を用いて液晶層に用いる。ブルー相を示す液晶とカイラル剤とを含む液晶組成物は、応答速度が短く、光学的等方性であるため配向処理が不要であり、視野角依存性が小さい。また配向膜を設けなくてもよいのでラビング処理も不要となるため、ラビング処理によって引き起こされる静電破壊を防止することができ、作製工程中の液晶表示装置の不良や破損を軽減することができる。よって液晶表示装置の生産性を向上させることが可能となる。酸化物半導体膜を用いるトランジスタは、静電気の影響によりトランジスタの電気的な特性が著しく変動して設計範囲を逸脱する恐れがある。よって酸化物半導体膜を用いるトランジスタを有する液晶表示装置にブルー相の液晶材料を用いることはより効果的である。

【０１１７】

また、液晶材料の固有抵抗は、１×１０^{9}Ω・ｃｍ以上であり、好ましくは１×１０^{11}Ω・ｃｍ以上であり、さらに好ましくは１×１０^{12}Ω・ｃｍ以上である。なお、本明細書における固有抵抗の値は、２０℃で測定した値とする。

【０１１８】

表示装置に設けられる保持容量の大きさは、画素部に配置されるトランジスタのリーク電流等を考慮して、所定の期間の間電荷を保持できるように設定される。保持容量の大きさは、トランジスタのオフ電流等を考慮して設定すればよい。高純度且つ酸素欠損の形成を抑制した酸化物半導体層を有するトランジスタを用いることにより、例えば表示素子として、液晶素子を用いた場合、各画素における液晶容量に対して１／３以下、好ましくは１／５以下の容量の大きさを有する保持容量を設ければ充分である。

【０１１９】

また、本実施の形態で用いる高純度化し、酸素欠損の形成を抑制した酸化物半導体を半導体層に用いるトランジスタは、オフ状態における電流値（オフ電流値）を低くすることができる。よって、画像信号等の電気信号の保持時間を長くすることができ、電源オン状態では書き込み間隔も長く設定できる。よって、リフレッシュ動作の頻度を少なくするこ

とができるため、消費電力を抑制する効果を奏する。

【０１２０】

また、図１及び図２に示す表示装置において、液晶素子１５０の駆動モードとしては、ＴＮ（Ｔｗｉｓｔｅｄ　Ｎｅｍａｔｉｃ）モード、ＩＰＳ（Ｉｎ－Ｐｌａｎｅ－Ｓｗｉｔｃｈｉｎｇ）モード、ＦＦＳ（Ｆｒｉｎｇｅ　Ｆｉｅｌｄ　Ｓｗｉｔｃｈｉｎｇ）モード、ＡＳＭ（Ａｘｉａｌｌｙ　Ｓｙｍｍｅｔｒｉｃ　ａｌｉｇｎｅｄ　Ｍｉｃｒｏ－ｃｅｌｌ）モード、ＯＣＢ（Ｏｐｔｉｃａｌ　Ｃｏｍｐｅｎｓａｔｅｄ　Ｂｉｒｅｆｒｉｎｇｅｎｃｅ）モード、ＦＬＣ（Ｆｅｒｒｏｅｌｅｃｔｒｉｃ　Ｌｉｑｕｉｄ　Ｃｒｙｓｔａｌ）モード、ＡＦＬＣ（ＡｎｔｉＦｅｒｒｏｅｌｅｃｔｒｉｃ　Ｌｉｑｕｉｄ　Ｃｒｙｓｔａｌ）モードなどを用いることができる。特に、高視野角を得るにはＦＦＳモードを用いると好ましい。

【０１２１】

また、ノーマリブラック型の液晶表示装置、例えば垂直配向（ＶＡ）モードを採用した透過型の液晶表示装置としてもよい。垂直配向モードとしては、いくつか挙げられるが、例えば、ＭＶＡ（Ｍｕｌｔｉ－Ｄｏｍａｉｎ　Ｖｅｒｔｉｃａｌ　Ａｌｉｇｎｍｅｎｔ）モード、ＰＶＡ（Ｐａｔｔｅｒｎｅｄ　Ｖｅｒｔｉｃａｌ　Ａｌｉｇｎｍｅｎｔ）モードなどを用いることができる。また、画素（ピクセル）をいくつかの領域（サブピクセル）に分け、それぞれ別の方向に分子を倒すよう工夫されているマルチドメイン化あるいはマルチドメイン設計といわれる方法を用いてもよい。

【０１２２】

また、図１及び図２においては、図示していないが、偏光部材、位相差部材、反射防止部材などの光学部材（光学基板）などを適宜設けても良い。例えば、偏光基板及び位相差基板による円偏光を用いてもよい。また、光源としてバックライト、サイドライトなどを用いてもよい。

【０１２３】

また、画素領域１４２における表示方式は、プログレッシブ方式やインターレース方式等を用いることができる。また、カラー表示する際に画素で制御する色要素としては、ＲＧＢ（Ｒは赤、Ｇは緑、Ｂは青を表す）の三色に限定されない。例えば、ＲＧＢＷ（Ｗは白を表す）、又はＲＧＢに、イエロー、シアン、マゼンタ等を一色以上追加したものがある。なお、色要素のドット毎にその表示領域の大きさが異なっていてもよい。ただし、開示する発明はカラー表示の表示装置に限定されるものではなく、モノクロ表示の表示装置に適用することもできる。

【０１２４】

また、第２の基板１５２上には、スペーサ１６０が形成されており、第１の基板１０２と第２の基板１５２との間隔（セルギャップともいう）を制御するために設けられている。なお、セルギャップにより、液晶層１６２の膜厚が決定される。なお、スペーサ１６０としては、絶縁膜を選択的にエッチングすることで得られる柱状のスペーサ、球状のスペーサ等の任意の形状のスペーサを用いればよい。

【０１２５】

また、有色膜１５３は、所謂カラーフィルタとして機能する。有色膜１５３としては、特定波長帯域の光に対して透過性を示す材料を用いればよく、染料や顔料を含有した有機樹脂膜等を用いることができる。

【０１２６】

また、遮光膜１５４は、所謂ブラックマトリクスとして機能する。遮光膜１５４としては、隣接する画素間の放射光を遮光できればよく、金属膜、及び黒色染料や黒色顔料を含有した有機樹脂膜等を用いることができる。なお、本実施の形態においては、黒色顔料を含有した有機樹脂膜による遮光膜１５４を例示している。

【０１２７】

また、有機保護絶縁膜１５６としては、有色膜１５３に含まれるイオン性物質が液晶層１６２中に拡散しないように設ける。ただし、有機保護絶縁膜１５６は、この構成に限定

されず、設けない構成としても良い。
【０１２８】
また、シール材１６６としては、熱硬化型樹脂、または紫外線硬化型の樹脂等を用いることができる。なお、図２に示すシール材１６６の封止領域においては、第１の基板１０２と第２の基板１５２間に、ゲート絶縁膜１０６、ソース電極１１０及びドレイン電極１１２と同一工程で形成される電極１１３、第１の層間絶縁膜１１４、及び第２の層間絶縁膜１１６を設ける構成を例示したがこれに限定されない。例えば、ゲート絶縁膜１０６と、第１の層間絶縁膜１１４のみの構成としても良い。なお、第２の層間絶縁膜１１６を除去したほうが、外部からの水分等の入り込みがないため、図２に示すように、第２の層間絶縁膜１１６の一部を除去または一部を後退させる構造が好ましい。
【０１２９】
以上のように本実施の形態に示す表示装置は、画素領域と駆動回路領域のそれぞれに形成されたトランジスタと、該トランジスタ上に形成された第１の層間絶縁膜と、第１の層間絶縁膜上に形成された第２の層間絶縁膜と、第２の層間絶縁膜上に形成された第３の層間絶縁膜と、を有し、第３の層間絶縁膜が画素領域上の一部に設けられ、第３の層間絶縁膜の端部が駆動回路領域よりも内側に形成される構成である。このような構成とすることで、第２の層間絶縁膜からの脱ガスをトランジスタ側へ入り込むのを抑制し、信頼性の高い表示装置とすることができる。また、さらに第１の層間絶縁膜により、第２の層間絶縁膜からの脱ガスをトランジスタ側へ入り込むのを抑制できる。
【０１３０】
本実施の形態に示す構成は、他の実施の形態または実施例に示す構成と適宜組み合わせて用いることができる。
【０１３１】
（実施の形態２）
本実施の形態では、表示装置の一形態として、有機ＥＬパネルを用いた表示装置について図３及び図４を用いて説明する。なお、実施の形態１で示す構成と同一の箇所には同一の符号を付し、その詳細な説明は省略する。
【０１３２】
表示装置の一形態として、表示装置の上面図を図３に、表示装置の断面図を図４にそれぞれ示す。なお、図４は、図３におけるＸ２－Ｙ２の断面図に相当する。
【０１３３】
図３に示す表示装置において、第１の基板１０２上に設けられた画素領域１４２と、画素領域１４２の外側に隣接し、該画素領域１４２に信号を供給する駆動回路領域であるゲートドライバ回路部１４０及びソースドライバ回路部１４４を囲むようにして、シール材１６６が設けられ、第２の基板１５２によって封止されている。また、画素領域１４２と、ゲートドライバ回路部１４０及びソースドライバ回路部１４４が設けられた第１の基板１０２と対向するように第２の基板１５２が設けられている。よって画素領域１４２と、ゲートドライバ回路部１４０と、ソースドライバ回路部１４４とは、第１の基板１０２とシール材１６６と第２の基板１５２によって、表示素子と共に封止されている。
【０１３４】
このように、トランジスタを含む駆動回路の一部または全体を、画素領域１４２と同じ第１の基板１０２上に一体形成し、システムオンパネルを形成することができる。
【０１３５】
次に、図３におけるＸ２－Ｙ２の断面図に相当する図４を用いて、画素領域１４２、及びゲートドライバ回路部１４０の構成について、以下詳細に説明を行う。
【０１３６】
画素領域１４２において、第１の基板１０２と、第１の基板１０２上に形成されたゲート電極１０４と、ゲート電極１０４上に形成されたゲート絶縁膜１０６と、ゲート絶縁膜１０６と接し、ゲート電極１０４と重畳する位置に設けられた半導体層１０８と、ゲート絶縁膜１０６、及び半導体層１０８上に形成されたソース電極１１０及びドレイン電極１

１２と、により、第１のトランジスタ１０１が形成されている。
【０１３７】
また、画素領域１４２において、第１のトランジスタ１０１上、より詳しくはゲート絶縁膜１０６、及び半導体層１０８、ソース電極１１０、及びドレイン電極１１２上に無機絶縁材料で形成された第１の層間絶縁膜１１４と、第１の層間絶縁膜１１４上に有機絶縁材料で形成された第２の層間絶縁膜１１６と、第２の層間絶縁膜１１６上に無機絶縁材料で形成された第３の層間絶縁膜１２０と、第２の層間絶縁膜１１６、及び第３の層間絶縁膜１２０上に形成された隔壁１２６と、第３の層間絶縁膜１２０、及び隔壁１２６上に形成された画素電極１２２と、画素電極１２２上に形成された発光層１２８と、発光層１２８上に形成された電極１３０が形成されている。
【０１３８】
なお、画素電極１２２と、発光層１２８と、電極１３０と、により発光素子１７０が形成されている。
【０１３９】
また、発光素子１７０上、より詳しくは電極１３０上には、充填材１７２が設けられ、充填材１７２上には、第２の基板１５２が設けられている。すなわち、第１の基板１０２と、第２の基板１５２との間に発光素子１７０、及び充填材１７２が挟持された構造である。
【０１４０】
また、ゲートドライバ回路部１４０において、第１の基板１０２と、第１の基板１０２上に形成されたゲート電極１０４と、ゲート電極１０４上に形成されたゲート絶縁膜１０６と、ゲート絶縁膜１０６と接し、ゲート電極１０４と重畳する位置に設けられた半導体層１０８と、ゲート絶縁膜１０６、及び半導体層１０８上に形成されたソース電極１１０及びドレイン電極１１２と、により、第２のトランジスタ１０３、及び第３のトランジスタ１０５が形成されている。
【０１４１】
また、ゲートドライバ回路部１４０において、第２のトランジスタ１０３及び第３のトランジスタ１０５上、より詳しくはゲート絶縁膜１０６、及び半導体層１０８、ソース電極１１０、及びドレイン電極１１２上に無機絶縁材料で形成された第１の層間絶縁膜１１４と、第１の層間絶縁膜１１４上に有機絶縁材料で形成された第２の層間絶縁膜１１６が形成されている。
【０１４２】
すなわち、第３の層間絶縁膜１２０は、画素領域１４２上の一部に設けられ、第３の層間絶縁膜１２０の端部が駆動回路領域であるゲートドライバ回路部１４０よりも内側に形成される。
【０１４３】
このような構成とすることによって、外部から取り込まれる水分、または表示装置内部で生じた水分、水素等のガスをゲートドライバ回路部１４０の第２の層間絶縁膜１１６から上部へ放出することができる。したがって、第１のトランジスタ１０１、第２のトランジスタ１０３、及び第３のトランジスタ１０５内部に水分、水素等のガスが取り込まれるのを抑制することができる。
【０１４４】
なお、有機絶縁材料により形成される第２の層間絶縁膜１１６は、表示装置を構成するトランジスタの凹凸等を低減するために、平坦性の高い有機絶縁材料が必要とされる。しかしながら、該有機絶縁材料は加熱等により、水素、水分、または有機成分をガスとして放出してしまう。
【０１４５】
しかし、半導体層１０８に、例えば、シリコン系半導体材料であるシリコン膜を用いたトランジスタにおいては、上述の水素、水分、または有機成分のガスが大きな問題になる可能性が低い。しかし、本発明の一態様においては、半導体層１０８に酸化物半導体膜を

用いるため、有機絶縁材料により形成される第２の層間絶縁膜１１６からのガスを外部に好適に放出させる必要がある。なお、第３の層間絶縁膜１２０の端部が駆動回路領域であるゲートドライバ回路部１４０よりも内側に形成される構成は、半導体層１０８を酸化物半導体膜により形成した場合において、優れた効果を奏する。ただし、半導体層１０８に酸化物半導体以外の材料（例えば、シリコン系半導体材料である非晶質シリコン、結晶性シリコンなど）により形成したトランジスタにおいても、同様の効果が得られる。

【０１４６】

また、第２の層間絶縁膜１１６上に形成される第３の層間絶縁膜１２０は、本実施の形態においては、第２の層間絶縁膜１１６からの放出するガスを発光素子１７０側へ入り込むのを抑制するため、及び／または画素電極１２２と、第２の層間絶縁膜１１６との密着性を向上させるために形成されている。このような構成とすることで発光素子１７０側へ第２の層間絶縁膜１１６からの水素、水分等のガスが入り込むのを抑制することができる。

【０１４７】

しかしながら、第３の層間絶縁膜１２０をゲートドライバ回路部１４０に用いる第２のトランジスタ１０３、及び第３のトランジスタ１０５上の第２の層間絶縁膜１１６上に形成すると、第２の層間絶縁膜１１６に用いる有機絶縁材料から放出されるガスを外部に拡散することができず、第２のトランジスタ１０３、及び第３のトランジスタ１０５内部に入り込んでしまう。

【０１４８】

上述したガスがトランジスタの半導体層１０８に用いる酸化物半導体に入り込むと、酸化物半導体膜中で不純物として取り込まれ、該半導体層１０８を用いたトランジスタの特性が変動してしまう。

【０１４９】

しかし、図４に示すように、ゲートドライバ回路部１４０に用いる第２のトランジスタ１０３、及び第３のトランジスタ１０５上の第３の層間絶縁膜１２０が開口された構成、すなわち第３の層間絶縁膜１２０が、画素領域１４２の一部に設けられ、第３の層間絶縁膜１２０の端部がゲートドライバ回路部１４０よりも内側に形成される構成とすることによって、第２の層間絶縁膜１１６から放出されるガスを、外部へ拡散できる構造とすることができる。

【０１５０】

なお、図４に示すように、画素領域１４２に用いる第１のトランジスタ１０１においても、半導体層１０８の重畳する位置の無機絶縁材料で形成された第３の層間絶縁膜１２０が除去された構成が好ましい。このような構成とすることで、有機絶縁材料で形成された第２の層間絶縁膜１１６から放出されるガスが、第１のトランジスタ１０１への入り込むのを抑制することができる。

【０１５１】

ここで、図３及び図４に示す表示装置の他の構成要素について、実施の形態１に示す表示装置と異なる構成について、以下詳細な説明を行う。

【０１５２】

隔壁１２６としては、有機絶縁材料、又は無機絶縁材料を用いて形成する。特に感光性の樹脂材料を用い、画素電極１２２上に開口部を形成し、その開口部の側壁が連続した曲率を持って形成される傾斜面となるように形成することが好ましい。

【０１５３】

充填材１７２としては、窒素やアルゴンなどの不活性な気体の他に、紫外線硬化樹脂または熱硬化樹脂を用いることができ、ＰＶＣ（ポリビニルクロライド）、アクリル系樹脂、ポリイミド系樹脂、エポキシ系樹脂、シリコーン系樹脂、ＰＶＢ（ポリビニルブチラル）またはＥＶＡ（エチレンビニルアセテート）を用いることができる。例えば充填材１７２として、窒素を用いればよい。

【０１５４】

発光素子１７０としては、エレクトロルミネッセンスを利用する発光素子を適用することができる。エレクトロルミネッセンスを利用する発光素子は、発光材料が有機化合物であるか、無機化合物であるかによって区別され、一般的に、前者は有機ＥＬ素子、後者は無機ＥＬ素子と呼ばれている。ここでは、有機ＥＬ素子を用いて説明する。

【０１５５】

有機ＥＬ素子は、発光素子に電圧を印加することにより、一対の電極（画素電極１２２及び電極１３０）から電子および正孔がそれぞれ発光性の有機化合物を含む層に注入され、電流が流れる。そして、それらキャリア（電子および正孔）が再結合することにより、発光性の有機化合物が励起状態を形成し、その励起状態が基底状態に戻る際に発光する。このようなメカニズムから、このような発光素子は、電流励起型の発光素子と呼ばれる。

【０１５６】

発光素子１７０は発光を取り出すために少なくとも一対の電極（画素電極１２２または電極１３０）の一方が透光性であればよい。そして、第１の基板１０２とは逆側の面から発光を取り出す上面射出や、第１の基板１０２側の面から発光を取り出す下面射出や、第１の基板１０２側及び第１の基板１０２とは反対側の面から発光を取り出す両面射出構造の発光素子があり、どの射出構造の発光素子も適用することができる。

【０１５７】

また、発光素子１７０に酸素、水素、水分、二酸化炭素等が入り込まないように、電極１３０、及び隔壁１２６上に保護膜を形成してもよい。保護膜としては、窒化シリコン膜、窒化酸化シリコン膜等を形成することができる。また、第１の基板１０２、第２の基板１５２、及びシール材１６６によって封止された空間には充填材１７２が設けられ密封されている。このように外気に曝されないように気密性が高く、脱ガスの少ない保護フィルム（貼り合わせフィルム、紫外線硬化樹脂フィルム等）やカバー材でパッケージング（封入）することが好ましい。

【０１５８】

また、必要であれば、発光素子１７０の射出面に偏光板、又は円偏光板（楕円偏光板を含む）、位相差板（λ／４板、λ／２板）、カラーフィルタなどの光学フィルムを適宜設けてもよい。また、偏光板又は円偏光板に反射防止膜を設けてもよい。例えば、表面の凹凸により反射光を拡散し、映り込みを低減できるアンチグレア処理を施すことができる。

【０１５９】

また、発光層１２８としては、三重項励起エネルギーを発光に変える発光性材料をゲスト材料と、該ゲスト材料よりも三重項励起エネルギーの準位（Ｔ１準位）が高いホスト材料と、を含む有機化合物を用いると好適である。なお、発光層１２８は、発光層が複数積層された構造（所謂タンデム構造）や、発光層以外の機能層（正孔注入層、正孔輸送層、電子輸送層、電子注入層、電荷発生層など）を含む構成としてもよい。

【０１６０】

また、シール材１６６としては、実施の形態１に示す材料に加えて、ガラス材料を含む材料、例えば粉末ガラス（フリットガラスともよぶ）を溶解、凝固させて形成されたガラス体を用いてもよい。このような材料は、水分やガスの透過を効果的に抑制することができるため、表示素子として、発光素子１７０を用いた場合、該発光素子１７０の劣化を抑制し、極めて信頼性の高い表示装置を実現できる。

【０１６１】

また、図４に示すシール材１６６の封止領域においては、第１の基板１０２と第２の基板１５２の間に、ゲート絶縁膜１０６のみを設ける構成を例示したが、これに限定されない。例えば、ゲート絶縁膜１０６と、第１の層間絶縁膜１１４を積層した構成としても良い。ただし、図４に示すように、第２の層間絶縁膜１１６が除去された領域において、シール材１６６が配置されるような構成が好ましい。

【０１６２】

以上のように本実施の形態に示す表示装置は、画素領域と駆動回路領域のそれぞれに形成されたトランジスタと、該トランジスタ上に形成された第１の層間絶縁膜と、第１の層

間絶縁膜上に形成された第２の層間絶縁膜と、第２の層間絶縁膜上に形成された第３の層間絶縁膜と、を有し、第３の層間絶縁膜が画素領域上の一部に設けられ、第３の層間絶縁膜の端部が駆動回路領域よりも内側に形成される構成である。このような構成とすることで、第２の層間絶縁膜からの脱ガスをトランジスタ側へ入り込むのを抑制し、信頼性の高い表示装置とすることができる。また、さらに第１の層間絶縁膜により、第２の層間絶縁膜からの脱ガスをトランジスタ側へ入り込むのを抑制できる。

【０１６３】

本実施の形態に示す構成は、他の実施の形態または実施例に示す構成と適宜組み合わせて用いることができる。

【０１６４】

（実施の形態３）

本実施の形態では、先の実施の形態で示した表示装置と組み合わせが可能な、イメージセンサについて説明する。

【０１６５】

図５（Ａ）に、イメージセンサ付の表示装置の一例を示す。図５（Ａ）はイメージセンサ付の表示装置の一画素を示す等価回路である。

【０１６６】

フォトダイオード素子４００２は、一方の電極がリセット信号線４０５８に、他方の電極がトランジスタ４０４０のゲート電極に電気的に接続されている。トランジスタ４０４０は、ソース電極またはドレイン電極の一方が電源電位（ＶＤＤ）に、ソース電極またはドレイン電極の他方がトランジスタ４０５６のソース電極またはドレイン電極の一方に電気的に接続されている。トランジスタ４０５６は、ゲート電極がゲート選択線４０５７に、ソース電極またはドレイン電極の他方が出力信号線４０７１に電気的に接続されている。

【０１６７】

また、第１のトランジスタ４０３０は、画素スイッチング用のトランジスタであり、ソース電極またはドレイン電極の一方が映像信号線４０５９に、ソース電極またはドレイン電極の他方が容量素子４０３２及び液晶素子４０３４に電気的に接続されている。また、第１のトランジスタ４０３０のゲート電極は、ゲート線４０３６に電気的に接続されている。

【０１６８】

なお、第１のトランジスタ４０３０、容量素子４０３２、液晶素子４０３４は、実施の形態１で示した表示装置と同様の構造を適用すればよい。

【０１６９】

図５（Ｂ）は、イメージセンサ付の表示装置の一画素の一部を示す断面図と、駆動回路部の断面図であり、画素領域５０４２においては、第１の基板４００１上に、フォトダイオード素子４００２および第１のトランジスタ４０３０が設けられている。また、駆動回路であるゲートドライバ回路部５０４０においては、第１の基板４００１上に、第２のトランジスタ４０６０、及び第３のトランジスタ４０６２が設けられている。

【０１７０】

なお、画素領域５０４２上のフォトダイオード素子４００２、及び第１のトランジスタ４０３０上には、第１の層間絶縁膜４０１４、第２の層間絶縁膜４０１６、及び第３の層間絶縁膜４０２０が形成されている。また、第２の層間絶縁膜４０１６上に第３の層間絶縁膜４０２０を誘電体として用いる容量素子４０３２が形成されている。

【０１７１】

すなわち、第３の層間絶縁膜４０２０が、画素領域５０４２の一部に設けられ、第３の層間絶縁膜４０２０の端部がゲートドライバ回路部５０４０よりも内側に形成される構成である。このような構成とすることによって、第２の層間絶縁膜４０１６から放出されるガスを、外部へ拡散できる構造とすることができる。したがって、第２の層間絶縁膜４０１６からの脱ガスをトランジスタ側へ入り込むのを抑制し、信頼性の高い表示装置とする

ことができる。
【０１７２】
なお、フォトダイオード素子４００２は、第１のトランジスタ４０３０のソース電極及びドレイン電極と同一の工程で形成される下部電極と、液晶素子４０３４の画素電極と同一工程で形成される上部電極と、を一対の電極とし、該一対の電極間にダイオードを有する構成である。
【０１７３】
フォトダイオード素子４００２に用いることのできるダイオードとしては、ｐ型半導体膜、ｎ型半導体膜の積層を含むｐｎ型ダイオード、ｐ型半導体膜、ｉ型半導体膜、ｎ型半導体膜の積層を含むｐｉｎ型ダイオード、ショットキー型ダイオードなどを用いればよい。
【０１７４】
また、フォトダイオード素子４００２上には、第１の配向膜４０２４、液晶層４０９６、第２の配向膜４０８４、対向電極４０８８、有機絶縁膜４０８６、有色膜４０８５、第２の基板４０５２等が設けられている。
【０１７５】
なお、ｐｉｎ型ダイオードはｐ型の半導体膜側を受光面とする方が高い光電変換特性を示す。これは、正孔移動度は電子移動度に比べて小さいためである。本実施の形態においては、第２の基板４０５２の面から、有色膜４０８５、液晶層４０９６等を介して、フォトダイオード素子４００２に入射する光を電気信号に変換する構成について例示しているが、これに限定されない。例えば、有色膜４０８５を設けない構成としてもよい。
【０１７６】
本実施の形態で示したフォトダイオード素子４００２は、フォトダイオード素子４００２に光が入射することで、一対の電極間に電流が流れることを利用する。フォトダイオード素子４００２が光を検出することによって、被検出物の情報を読み取ることができる。
【０１７７】
本実施の形態で示したイメージセンサ付の表示装置は、トランジスタの作製など、表示装置およびイメージセンサの工程を共通化させることで、生産性を高めることができる。ただし、先の実施の形態で示した表示装置と、本実施の形態で示したイメージセンサを異なる基板上に作製しても構わない。具体的には、先の実施の形態で示した表示装置において、第２の基板上にイメージセンサを作製しても構わない。
【０１７８】
本実施の形態は、他の実施の形態または他の実施例に記載した構成と適宜組み合わせて実施することが可能である。
【０１７９】
（実施の形態４）
本実施の形態では、本発明の一態様の表示装置を用いたタブレット型端末の一例を説明する。
【０１８０】
図６（Ａ）及び図６（Ｂ）は２つ折り可能なタブレット型端末である。図６（Ａ）は、タブレット型端末を開いた状態である。タブレット型端末は、筐体８６３０と、筐体８６３０に設けられた、表示部８６３１ａ、表示部８６３１ｂ、表示モード切り替えスイッチ８０３４、電源スイッチ８０３５、省電力モード切り替えスイッチ８０３６、留め具８０３３および操作スイッチ８０３８と、を有する。
【０１８１】
本発明の一態様である表示装置は、表示部８６３１ａ、表示部８６３１ｂに適用することができる。
【０１８２】
表示部８６３１ａは、一部または全部をタッチパネルとして機能させることができ、表示された操作キーに触れることで入力することができる。例えば、表示部８６３１ａの全

面にキーボードボタンを表示し、タッチパネルとして機能させ、表示部８６３１ｂを表示画面として用いても構わない。

【０１８３】

また、表示部８６３１ａと同様に、表示部８６３１ｂの一部または全部をタッチパネルとして機能させることができる。

【０１８４】

また、表示部８６３１ａのタッチパネルの領域と表示部８６３１ｂのタッチパネルの領域を同時にタッチ入力することもできる。

【０１８５】

また、表示モード切り替えスイッチ８０３４は、縦表示または横表示などの表示の向きの切り替え、白黒表示やカラー表示の切り替えなどを選択できる。省電力モード切り替えスイッチ８０３６は、タブレット型端末に内蔵している光センサで検出される外光に応じて表示の輝度を最適なものとすることができる。なお、タブレット型端末は、光センサだけでなく、傾きを検出可能なジャイロ、加速度センサなど、他の検出装置を有してもよい。

【０１８６】

また、図６（Ａ）では、表示部８６３１ｂと表示部８６３１ａの面積が同じ例を示しているが特に限定されない。表示部８６３１ｂと表示部８６３１ａの面積が異なっていてもよく、表示の品質が異なっていてもよい。例えば、一方が他方よりも高精細な表示を行える表示パネルとしてもよい。

【０１８７】

図６（Ｂ）は、タブレット型端末を閉じた状態である。タブレット型端末は、筐体８６３０と、筐体８６３０に設けられた、太陽電池８６３３および充放電制御回路８６３４と、を有する。なお、図６（Ｂ）では充放電制御回路８６３４の一例としてバッテリー８６３５、ＤＣＤＣコンバータ８６３６を有する構成について示している。

【０１８８】

なお、タブレット型端末は２つ折り可能なため、未使用時に筐体８６３０を閉じた状態にすることができる。従って、表示部８６３１ａ、表示部８６３１ｂを保護できるため、耐久性に優れ、長期使用の観点からも信頼性に優れる。

【０１８９】

また、この他にも図６（Ａ）及び図６（Ｂ）に示したタブレット型端末は、様々な情報（静止画、動画、テキスト画像など）を表示する機能、カレンダー、日付または時刻などを表示部に表示する機能、表示部に表示した情報をタッチ入力操作または編集するタッチ入力機能、様々なソフトウェア（プログラム）によって処理を制御する機能、などを有することができる。

【０１９０】

タブレット型端末は、太陽電池８６３３によって得られた電力を、タブレット型端末の動作に用いることができる。または、当該電力をバッテリー８６３５に蓄積することができる。なお、太陽電池８６３３は、筐体８６３０の二面に設ける構成とすることもできる。なおバッテリー８６３５としては、リチウムイオン電池を用いると、小型化を図れるなどの利点がある。

【０１９１】

また、図６（Ｂ）に示す充放電制御回路８６３４の構成、及び動作について図６（Ｃ）にブロック図を示し説明する。図６（Ｃ）には、太陽電池８６３３と、バッテリー８６３５と、ＤＣＤＣコンバータ８６３６と、コンバータ８６３７と、スイッチＳＷ１と、スイッチＳＷ２と、スイッチＳＷ３と、表示部８６３１と、を示している。図６（Ｃ）において、バッテリー８６３５、ＤＣＤＣコンバータ８６３６、コンバータ８６３７、スイッチＳＷ１、スイッチＳＷ２およびスイッチＳＷ３が、図６（Ｂ）に示す充放電制御回路８６３４に対応する。

【０１９２】

太陽電池８６３３により発電がされる場合、太陽電池で発電した電力は、バッテリー８６３５を充電するための電圧となるようＤＣＤＣコンバータ８６３６で昇圧または降圧される。次に、スイッチＳＷ１をオンし、コンバータ８６３７で表示部８６３１に最適な電圧に昇圧または降圧をする。また、表示部８６３１での表示を行わない際は、スイッチＳＷ１をオフし、スイッチＳＷ２をオンしてバッテリー８６３５の充電を行う。

【０１９３】

なお、発電手段の一例として太陽電池８６３３について示したが、特に限定されず、圧電素子（ピエゾ素子）や熱電変換素子（ペルティエ素子）などの他の発電手段で代替しても構わない。例えば、無線（非接触）で電力を送受信して充電する無接点電力電送モジュールなど、他の充電手段を組み合わせて行う構成としてもよい。

【０１９４】

本実施の形態は、他の実施の形態または他の実施例に記載した構成と適宜組み合わせて実施することが可能である。

【０１９５】

（実施の形態５）

本実施の形態では、先の実施の形態で示した表示装置などを搭載した電子機器の例について説明する。

【０１９６】

図７（Ａ）は携帯型情報端末である。図７（Ａ）に示す携帯型情報端末は、筐体９３００と、ボタン９３０１と、マイクロフォン９３０２と、表示部９３０３と、スピーカ９３０４と、カメラ９３０５と、を具備し、携帯型電話機としての機能を有する。表示部９３０３に先の実施の形態で示した表示装置または／およびイメージセンサ付の表示装置を適用することができる。

【０１９７】

図７（Ｂ）は、ディスプレイである。図７（Ｂ）に示すディスプレイは、筐体９３１０と、表示部９３１１と、を具備する。表示部９３１１に先の実施の形態で示した表示装置または／およびイメージセンサ付表示装置を適用することができる。

【０１９８】

図７（Ｃ）は、デジタルスチルカメラである。図７（Ｃ）に示すデジタルスチルカメラは、筐体９３２０と、ボタン９３２１と、マイクロフォン９３２２と、表示部９３２３と、を具備する。表示部９３２３に先の実施の形態で示した表示装置または／およびイメージセンサ付表示装置を適用することができる。

【０１９９】

本発明の一態様を用いることで、電子機器の信頼性を高めることができる。

【０２００】

本実施の形態は、他の実施の形態または他の実施例に記載した構成と適宜組み合わせて実施することが可能である。

【実施例１】

【０２０１】

本実施例においては、表示装置に用いることのできる代表的な有機樹脂であるアクリル樹脂の放出ガスについて調査した。

【０２０２】

試料は、ガラス基板上にアクリル樹脂を塗布し、窒素ガス雰囲気下、２５０℃にて１時間の加熱処理を行った。なお、アクリル樹脂は加熱処理後に厚さが１．５μｍとなるように形成した。

【０２０３】

作製した試料に対し、ＴＤＳ（Ｔｈｅｒｍａｌ　Ｄｅｓｏｒｐｔｉｏｎ　Ｓｐｅｃｔｒｏｓｃｏｐｙ：昇温脱離ガス分光法）による放出ガスの測定を行った。

【０２０４】

図８に、基板表面温度２５０℃のときの、各質量電荷比（Ｍ／ｚともいう。）における

放出ガスのイオン強度を示す。図８において、横軸は質量電荷比を、縦軸は強度（任意単位）を、それぞれ示す。図８より、試料からは、水起因と見られる質量電荷比が１８（H_2O）のガスと、炭化水素起因と見られる質量電荷比が２８（C_2H_4）、４４（C_3H_8）および５６（C_4H_8）のガスが検出された。なお、各質量電荷比の近傍には、それぞれのフラグメントイオンが検出された。

【０２０５】

同様に、図９に、基板表面温度に対する各質量電荷比（１８、２８、４４および５６）のイオン強度を示す。図９において、横軸は基板表面温度（℃）を、縦軸は強度（任意単位）を、それぞれ示す。基板表面温度を５５℃から２７０℃の範囲とした場合、水起因と見られる質量電荷比が１８のイオン強度は、５５℃以上１００℃以下および１５０℃以上２７０℃以下にピークを有することがわかった。一方、炭化水素起因と見られる質量電荷比が２８、４４および５６のイオン強度は、１５０℃以上２７０℃以下にピークを有することがわかった。

【０２０６】

以上に示したように、有機樹脂からの水、炭化水素などの酸化物半導体膜にとっての不純物が放出されることがわかった。特に、水は５５℃以上１００℃以下の比較的低温でも放出されることがわかった。即ち、有機樹脂に起因する不純物が酸化物半導体膜に到達した場合、トランジスタの電気特性を劣化させることが示唆された。

【０２０７】

また、有機樹脂を水、炭化水素などの放出ガスを透過しない膜（窒化シリコン膜、窒化酸化シリコン膜、酸化アルミニウム膜など）で覆った場合、有機樹脂からガスが放出されることで水、炭化水素などの放出ガスを透過しない膜への圧力が高まり、最終的に水、炭化水素などの放出ガスを透過しない膜が破壊され、トランジスタの形状不良となることが示唆された。

【実施例２】

【０２０８】

本実施例では、トランジスタを作製し、断面形状および電気特性を評価した。

【０２０９】

各試料には、ボトムゲート・トップコンタクト型のチャネルエッチ構造の酸化物半導体膜を用いたトランジスタが設けられている。当該トランジスタは、ガラス基板上に設けられたゲート電極と、ゲート電極上に設けられたゲート絶縁膜と、ゲート絶縁膜を介しゲート電極上に設けられた酸化物半導体膜と、酸化物半導体膜上にあり酸化物半導体膜と接して設けられた一対の電極と、を有する。ここで、ゲート電極はタングステン膜を、ゲート絶縁膜は窒化シリコン膜、および窒化シリコン膜上の酸化窒化シリコン膜を、酸化物半導体膜はＩｎ－Ｇａ－Ｚｎ酸化物膜を、一対の電極はタングステン膜、タングステン膜上のアルミニウム膜、およびアルミニウム膜上のチタン膜を、それぞれ用いた。

【０２１０】

一対の電極上には保護絶縁膜（４５０ｎｍの厚さの酸化窒化シリコン膜と、酸化窒化シリコン膜上に設けられた５０ｎｍの厚さの窒化シリコン膜）が設けられている。

【０２１１】

なお、実施例試料は、保護絶縁膜上に２μｍの厚さでアクリル樹脂が設けられており、アクリル樹脂上にはアクリル樹脂の側面の一部を露出するように２００ｎｍの厚さで窒化シリコン膜が設けられている。また、比較試料は、保護絶縁膜上に１．５μｍの厚さでアクリル樹脂が設けられており、アクリル樹脂上にはアクリル樹脂を覆うように２００ｎｍの厚さで窒化シリコン膜が設けられている。

【０２１２】

図１０に、比較例試料の一部を拡大した領域のＴＥＭによる透過電子像（Ｔｒａｎｓｍｉｔｔｅｄ　Ｅｌｅｃｔｒｏｎ：ＴＥ像ともいう。）断面形状を示す。断面形状の観察には、株式会社日立ハイテクノロジーズ製「日立超薄膜評価装置ＨＤ－２３００」を用いた。図１０において、一対の電極、および一対の電極を覆うように設けられた保護絶縁膜に

着目すると、一対の電極が形成する段差部から保護絶縁膜に亀裂が生じていることがわかった。なお、観察領域において、実施例試料と比較例試料は概略同様の構造であるため、実施例試料の断面形状は省略する。

【０２１３】

従って、実施例試料はアクリル樹脂からの放出ガスが実施例試料外部へ抜ける構造であり、比較例試料はアクリル樹脂からの放出ガスが比較試料外部へ抜けない構造である。即ち、比較例試料において、アクリル樹脂からの放出ガスは、外部へは抜けず、保護絶縁膜に生じた亀裂を介してトランジスタに到達することがわかった。

【０２１４】

次に、各試料のトランジスタの電気特性であるゲート電圧（Ｖｇ）－ドレイン電流（Ｉｄ）特性を測定した。Ｖｇ－Ｉｄ特性は、チャネル長が３μｍ、チャネル幅が３μｍのトランジスタを用いて測定した。電気特性は、ドレイン電圧（Ｖｄ）を１Ｖまたは１０Ｖとし、ゲート電圧（Ｖｇ）を－２０Ｖから１５Ｖへ掃引した。

【０２１５】

図１１に各試料のＶｇ－Ｉｄ特性を示す。なお、６００ｍｍ×７２０ｍｍのガラス基板において、なるべく均等に２０個のトランジスタのＶｇ－Ｉｄ特性を測定した。なお、図１１（Ａ）に実施例試料のトランジスタのＶｇ－Ｉｄ特性および電界効果移動度を示し、図１１（Ｂ）に比較例試料のトランジスタのＶｇ－Ｉｄ特性を示す。なお、図１１（Ａ）に示す電界効果移動度はドレイン電圧（Ｖｄ）が１０Ｖにおける値を示す。また、図１１（Ｂ）においては、電界効果移動度の算出が困難であったため省略する。

【０２１６】

図１１（Ａ）より、実施例試料のトランジスタでは、良好なスイッチング特性が得られることがわかった。また、図１１（Ｂ）より、比較例試料のトランジスタでは、スイッチング特性が得られず、常時オンであることがわかった。

【０２１７】

実施例試料との比較により、比較例試料のスイッチング特性不良は、アクリル樹脂からの放出ガスがトランジスタに影響を及ぼしたためとわかる。具体的には、アクリル樹脂からの放出ガスの影響で酸化物半導体膜のキャリア密度が高まり、ゲート電極からの電界によってトランジスタをオフすることができなかったためと推察される。

【０２１８】

本実施例より、有機樹脂を水、炭化水素などの放出ガスを透過しない膜（ここでは厚さが２００ｎｍの窒化シリコン膜）で覆うと、有機樹脂からの放出ガスによってトランジスタのスイッチング特性不良が引き起こされることがわかる。また、有機樹脂を覆う、水、炭化水素などの放出ガスを透過しない膜の一部に、放出ガスの試料外部への抜け道を設けることで、当該トランジスタのスイッチング特性不良を回避でき、良好なスイッチング特性を得られることがわかる。

【符号の説明】

【０２１９】

１０１　第１のトランジスタ
１０２　第１の基板
１０３　第２のトランジスタ
１０４　ゲート電極
１０５　第３のトランジスタ
１０６　ゲート絶縁膜
１０７　容量素子
１０８　半導体層
１１０　ソース電極
１１２　ドレイン電極
１１３　電極
１１４　第１の層間絶縁膜

１１６　第２の層間絶縁膜
１１８　容量電極
１２０　第３の層間絶縁膜
１２２　画素電極
１２４　第１の配向膜
１２６　隔壁
１２８　発光層
１３０　電極
１４０　ゲートドライバ回路部
１４２　画素領域
１４４　ソースドライバ回路部
１４６　ＦＰＣ端子部
１４８　ＦＰＣ
１５０　液晶素子
１５２　第２の基板
１５３　有色膜
１５４　遮光膜
１５６　有機保護絶縁膜
１５８　対向電極
１６０　スペーサ
１６２　液晶層
１６４　第２の配向膜
１６６　シール材
１７０　発光素子
１７２　充填材
４００１　第１の基板
４００２　フォトダイオード素子
４０１４　第１の層間絶縁膜
４０１６　第２の層間絶縁膜
４０２０　第３の層間絶縁膜
４０２４　第１の配向膜
４０３０　第１のトランジスタ
４０３２　容量素子
４０３４　液晶素子
４０３６　ゲート線
４０４０　トランジスタ
４０５２　第２の基板
４０５６　トランジスタ
４０５７　ゲート選択線
４０５８　リセット信号線
４０５９　映像信号線
４０６０　第２のトランジスタ
４０６２　第３のトランジスタ
４０７１　出力信号線
４０８４　第２の配向膜
４０８５　有色膜
４０８６　有機絶縁膜
４０８８　対向電極
４０９６　液晶層
５０４０　ゲートドライバ回路部

５０４２　画素領域
８０３３　留め具
８０３４　スイッチ
８０３５　電源スイッチ
８０３６　スイッチ
８０３８　操作スイッチ
８６３０　筐体
８６３１　表示部
８６３１ａ　表示部
８６３１ｂ　表示部
８６３３　太陽電池
８６３４　充放電制御回路
８６３５　バッテリー
８６３６　ＤＣＤＣコンバータ
８６３７　コンバータ
９３００　筐体
９３０１　ボタン
９３０２　マイクロフォン
９３０３　表示部
９３０４　スピーカ
９３０５　カメラ
９３１０　筐体
９３１１　表示部
９３２０　筐体
９３２１　ボタン
９３２２　マイクロフォン
９３２３　表示部

【書類名】特許請求の範囲
【請求項１】
画素電極と、該画素電極と電気的に接続される少なくとも一の第１のトランジスタを含む画素が複数個配列されている画素領域と、
前記画素領域の外側に隣接し、該画素領域の各画素に含まれる前記第１のトランジスタに信号を供給する少なくとも一の第２のトランジスタを含む駆動回路領域と、が形成された第１の基板と、
前記第１の基板と対向するように設けられた第２の基板と、前記第１の基板と前記第２の基板間に挟持された液晶層と、を有し、
前記第１のトランジスタ及び前記第２のトランジスタ上に無機絶縁材料で形成された第１の層間絶縁膜と、
前記第１の層間絶縁膜上に有機絶縁材料で形成された第２の層間絶縁膜と、
前記第２の層間絶縁膜上に無機絶縁材料で形成された第３の層間絶縁膜と、を有し、
前記第３の層間絶縁膜は、前記画素領域上の一部に設けられ、該第３の層間絶縁膜の端部が前記駆動回路領域よりも内側に形成される
ことを特徴とする表示装置。
【請求項２】
請求項１において、
前記画素電極上に設けられた第１の配向膜と、
前記第１の配向膜上に形成された前記液晶層と、
前記液晶層上に設けられた第２の配向膜と、
前記第２の配向膜上に設けられた対向電極と、
前記対向電極上に設けられた有機保護絶縁膜と、
前記有機保護絶縁膜上に設けられた有色膜及び遮光膜と、
前記有色膜及び前記遮光膜上に設けられた前記第２の基板と、を有する
ことを特徴とする表示装置。
【請求項３】
画素電極と、該画素電極と電気的に接続される少なくとも一の第１のトランジスタを含む画素が複数個配列されている画素領域と、
前記画素領域の外側に隣接し、該画素領域の各画素に含まれる前記第１のトランジスタに信号を供給する少なくとも一の第２のトランジスタを含む駆動回路領域と、が形成された第１の基板と、
前記第１の基板と対向するように設けられた第２の基板と、前記第１の基板と前記第２の基板間に挟持された発光層と、を有し、
前記第１のトランジスタ及び前記第２のトランジスタ上に無機絶縁材料で形成された第１の層間絶縁膜と、
前記第１の層間絶縁膜上に有機絶縁材料で形成された第２の層間絶縁膜と、
前記第２の層間絶縁膜上に無機絶縁材料で形成された第３の層間絶縁膜と、を有し、
前記第３の層間絶縁膜は、前記画素領域上の一部に設けられ、該第３の層間絶縁膜の端部が前記駆動回路領域よりも内側に形成される
ことを特徴とする表示装置。
【請求項４】
請求項３において、
前記画素電極上に設けられた前記発光層と、
前記発光層上に設けられた電極と、を有する
ことを特徴とする表示装置。
【請求項５】
請求項１または請求項３において、
前記第３の層間絶縁膜は、窒化シリコン膜、窒化酸化シリコン膜、酸化アルミニウム膜の中から選ばれたいずれか一である

ことを特徴とする表示装置。
【請求項６】
請求項１または請求項３において、
前記第１のトランジスタ及び前記第２のトランジスタは、チャネル形成領域を形成する半導体材料が酸化物半導体である
ことを特徴とする表示装置。
【請求項７】
請求項６において、
前記第１のトランジスタ及び前記第２のトランジスタは、
ゲート電極と、
前記ゲート電極上に形成された酸化物半導体からなる半導体層と、
前記半導体層上に形成されたソース電極及びドレイン電極と、を有する
ことを特徴とする表示装置。
【請求項８】
請求項１乃至請求項７のいずれか一に記載する表示装置を有する電子機器。

【書類名】要約書
【要約】
【課題】画素領域及び駆動回路領域にトランジスタを有する表示装置において、電気特性の変動を抑制すると共に、信頼性を向上させる。
【解決手段】画素領域の外側に隣接し、該画素領域の各画素に含まれる第１のトランジスタに信号を供給する少なくとも一の第２のトランジスタを含む駆動回路領域が形成された第１の基板と、第１の基板と対向するように設けられた第２の基板と、第１の基板と第２の基板間に挟持された液晶層と、を有し、第１のトランジスタ及び第２のトランジスタ上に無機絶縁材料で形成された第１の層間絶縁膜と、第１の層間絶縁膜上に有機絶縁材料で形成された第２の層間絶縁膜と、第２の層間絶縁膜上に無機絶縁材料で形成された第３の層間絶縁膜と、を有し、第３の層間絶縁膜は、画素領域上の一部に設けられ、該第３の層間絶縁膜の端部が駆動回路領域よりも内側に形成される。
【選択図】図１

【書類名】図面
【図１】

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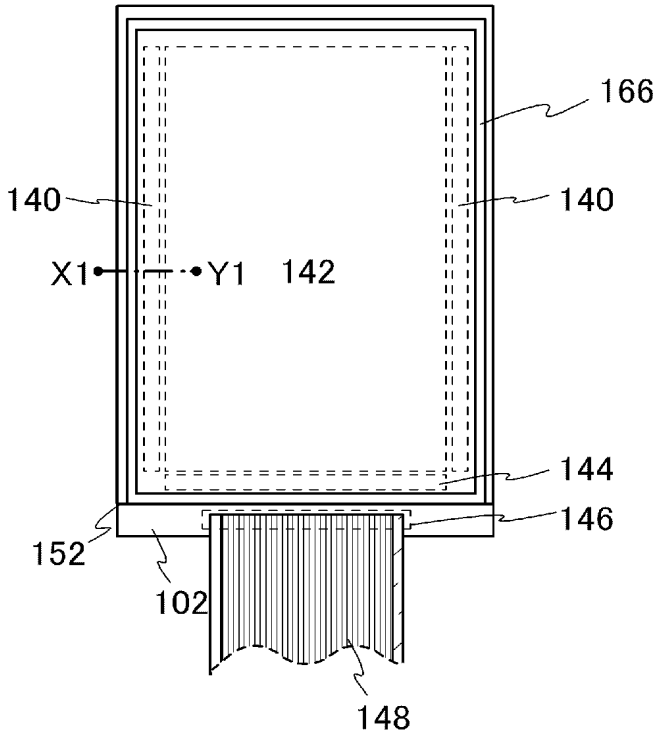

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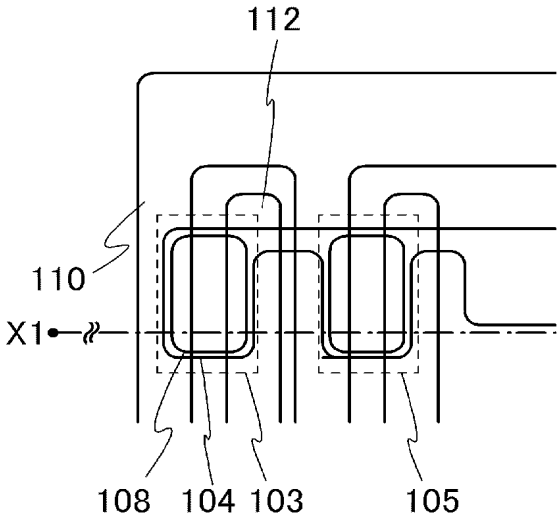
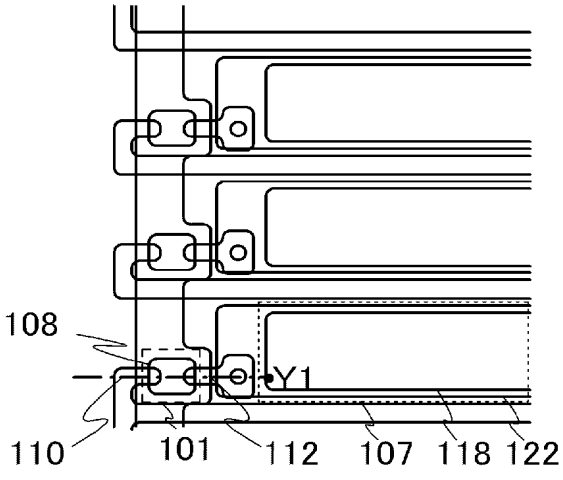


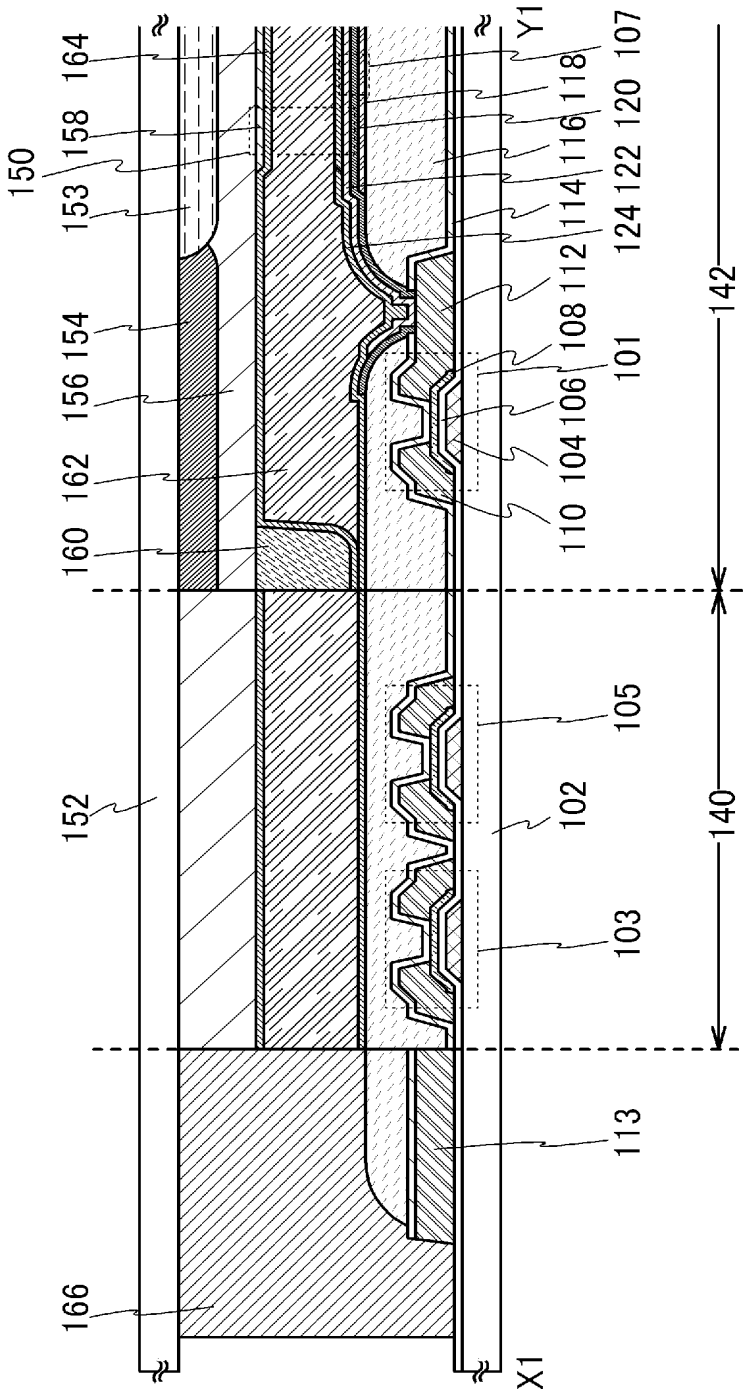
140

（C）



142

【図２】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152
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Y1
X1
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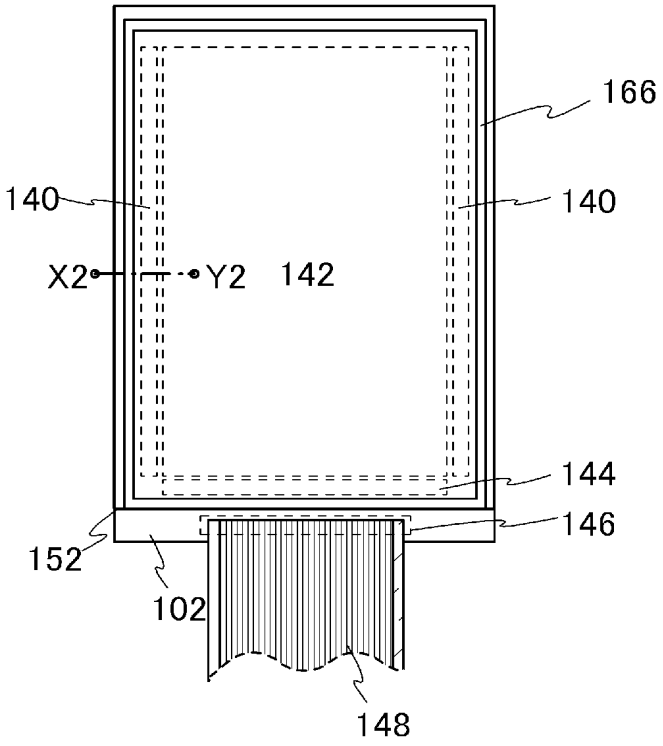
【図３】



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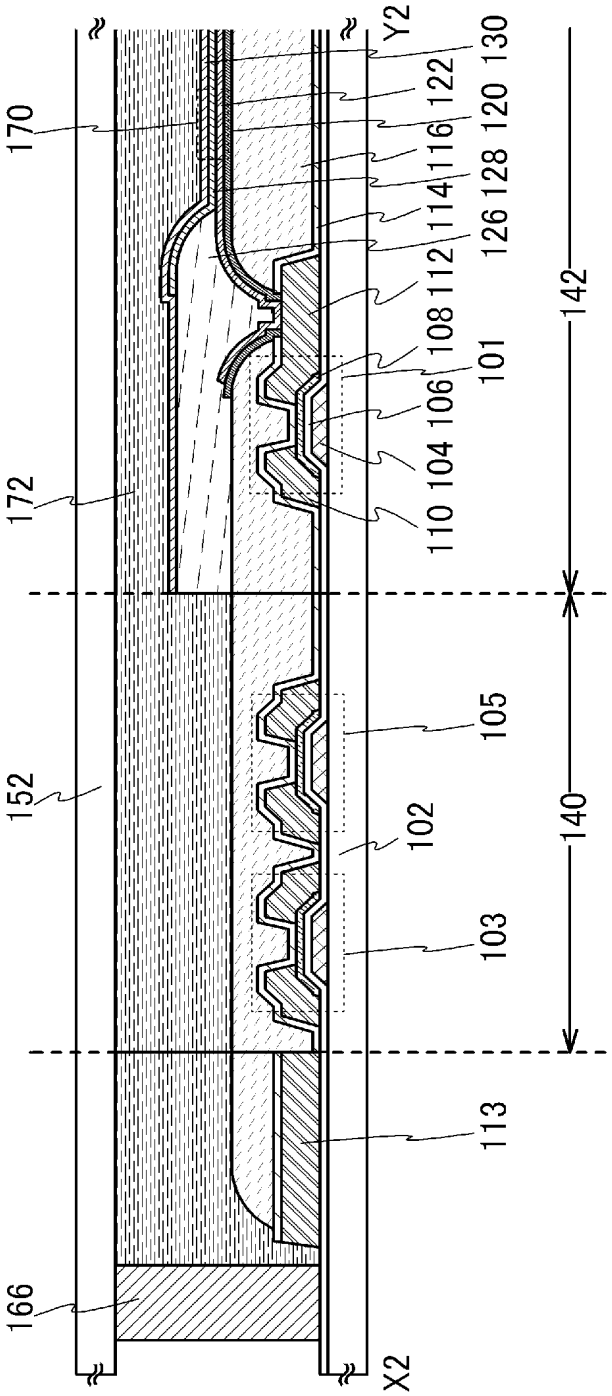
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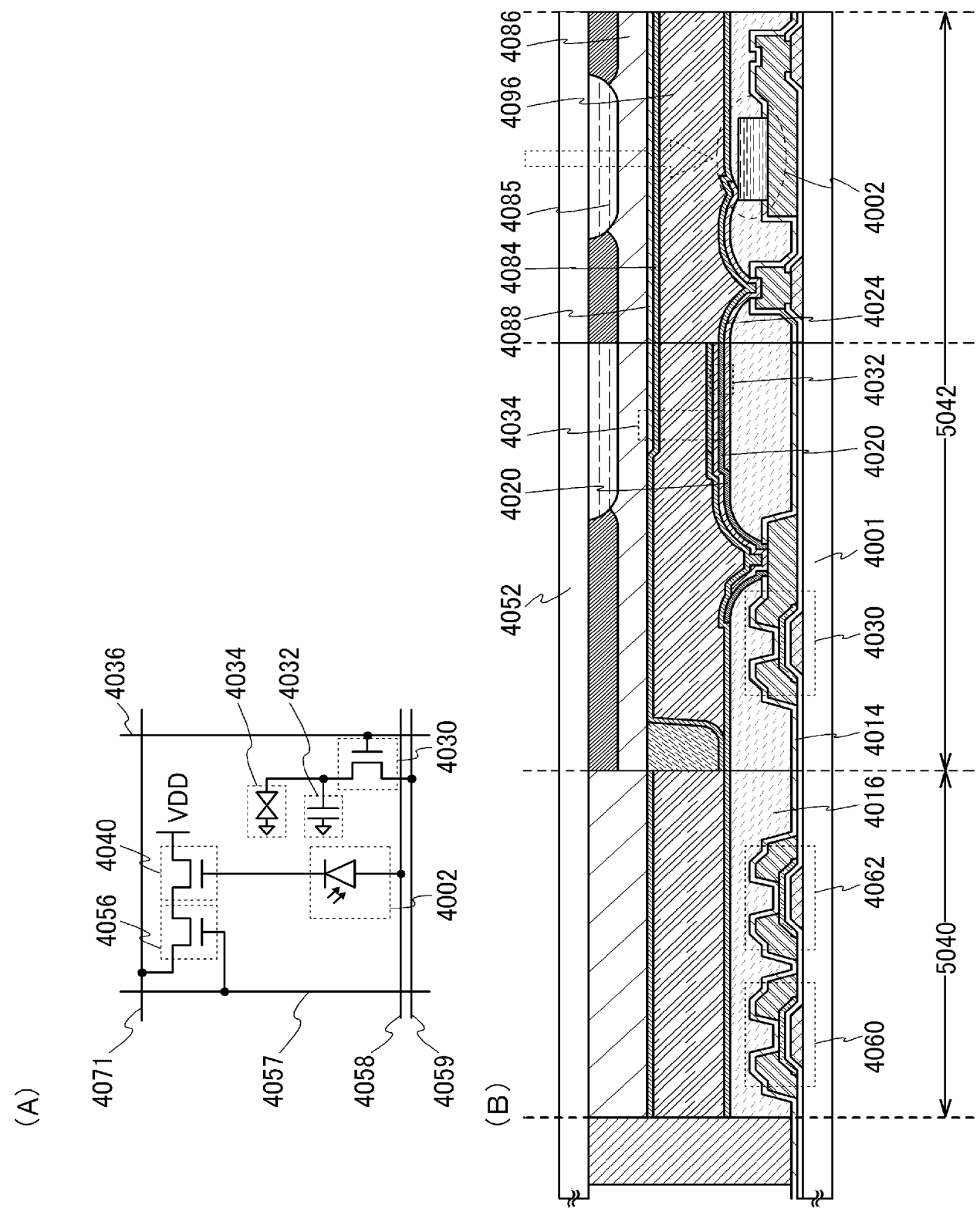
X2

【図５】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4059
(B)
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4096
4085
4084
4088
4002
4024
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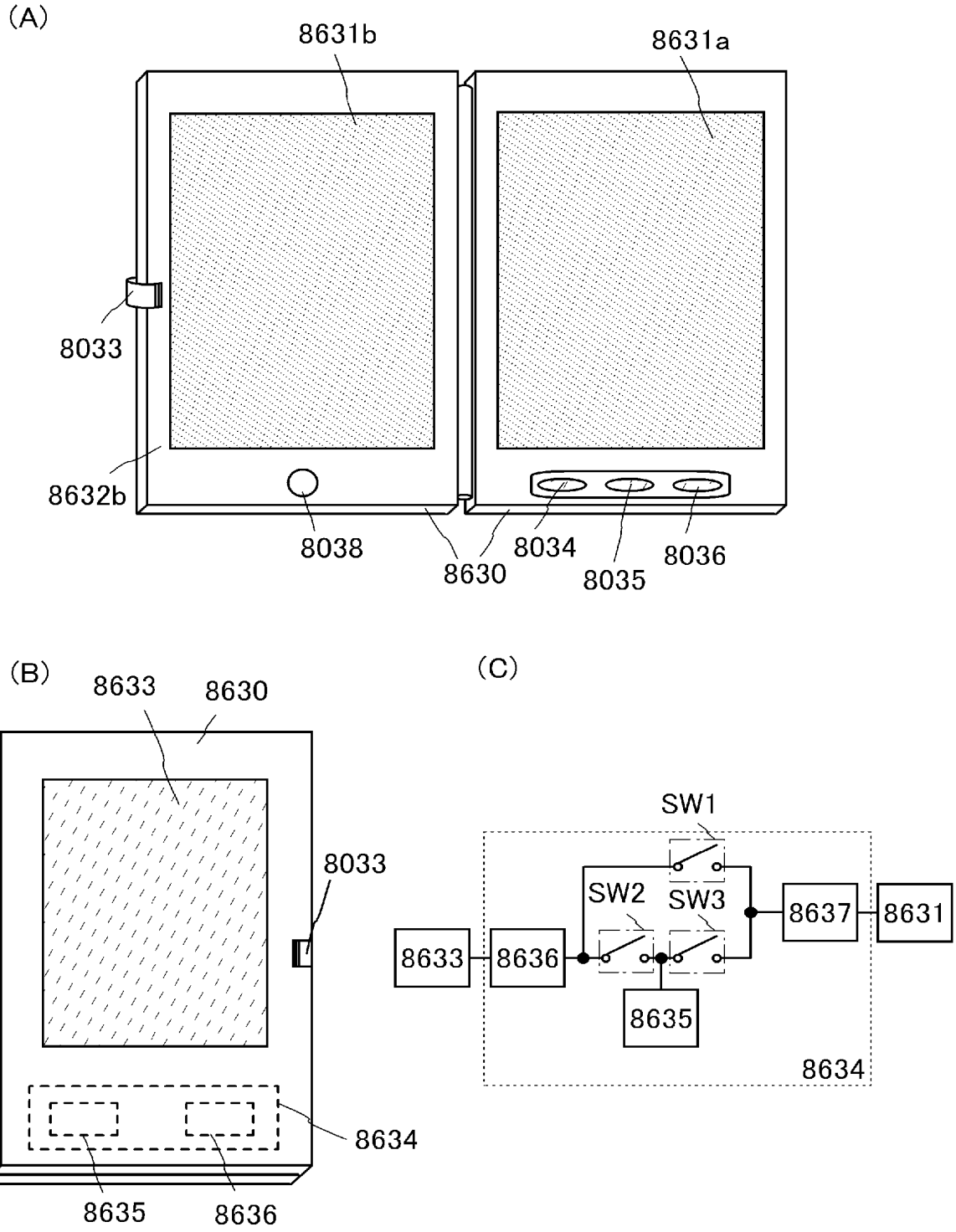
【図６】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(B)
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8033
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8635
8636
(C)
SW1
SW2
SW3
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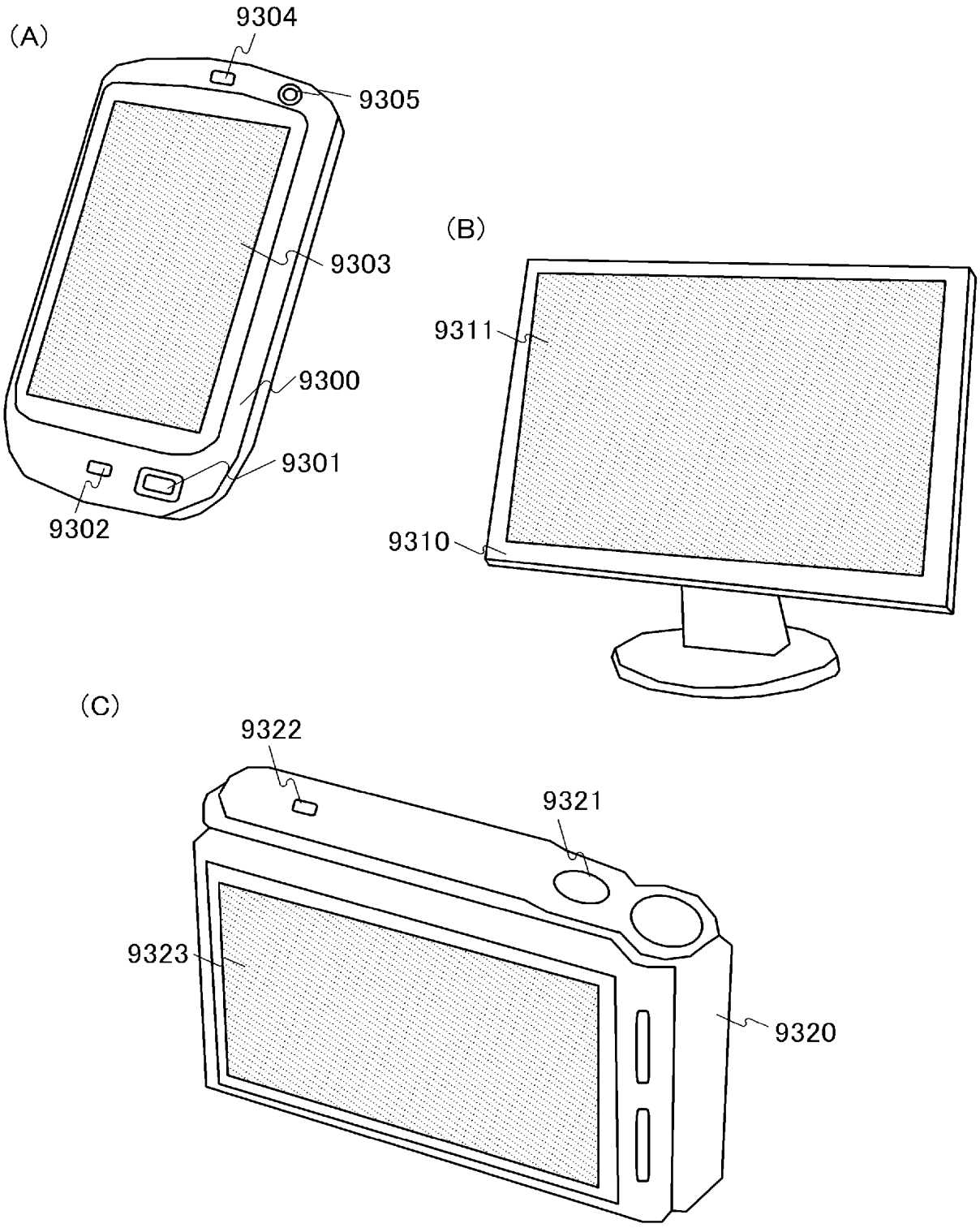
8637
8631
8635
8634

【図７】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(B)
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(C)
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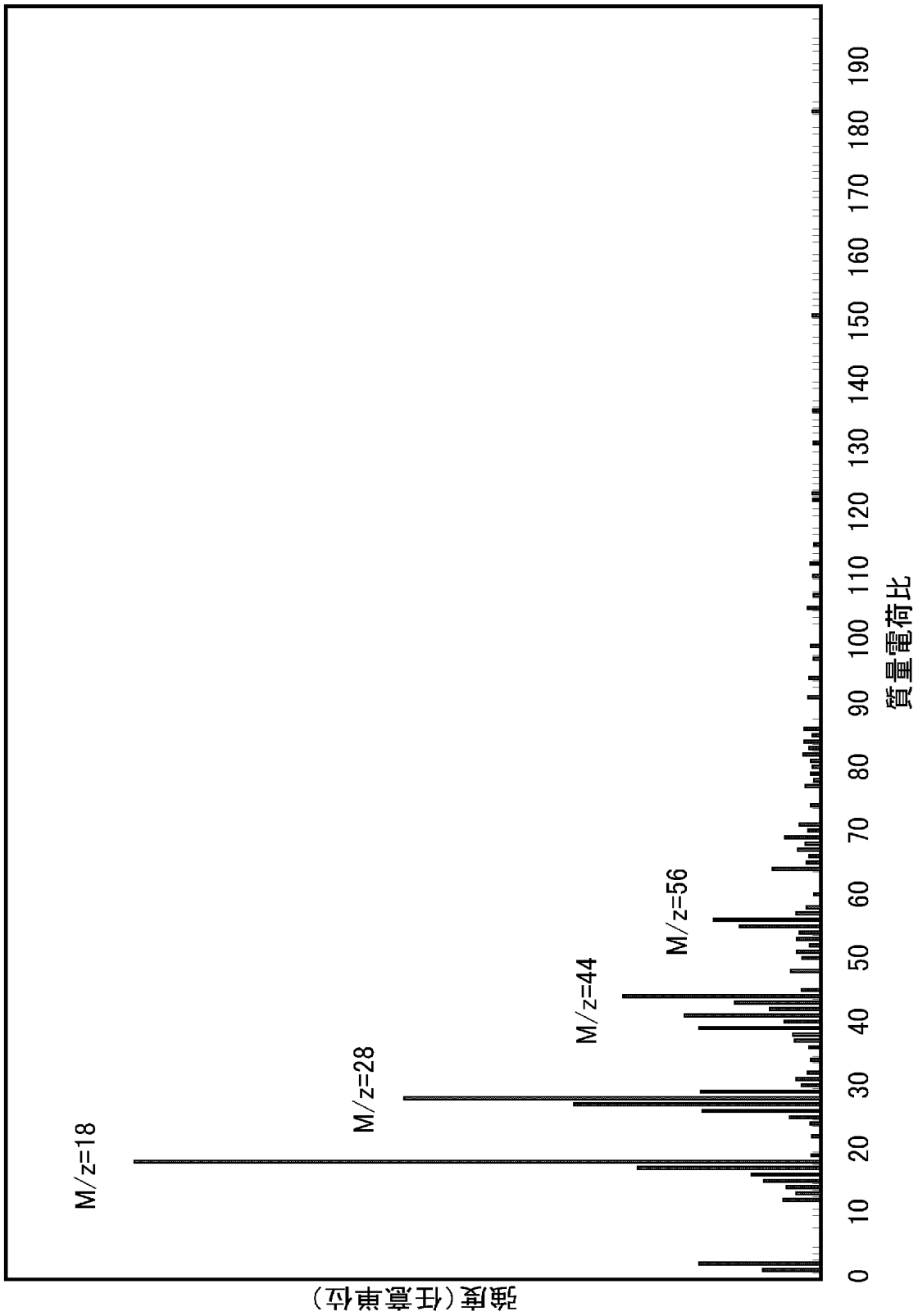
9320

【図８】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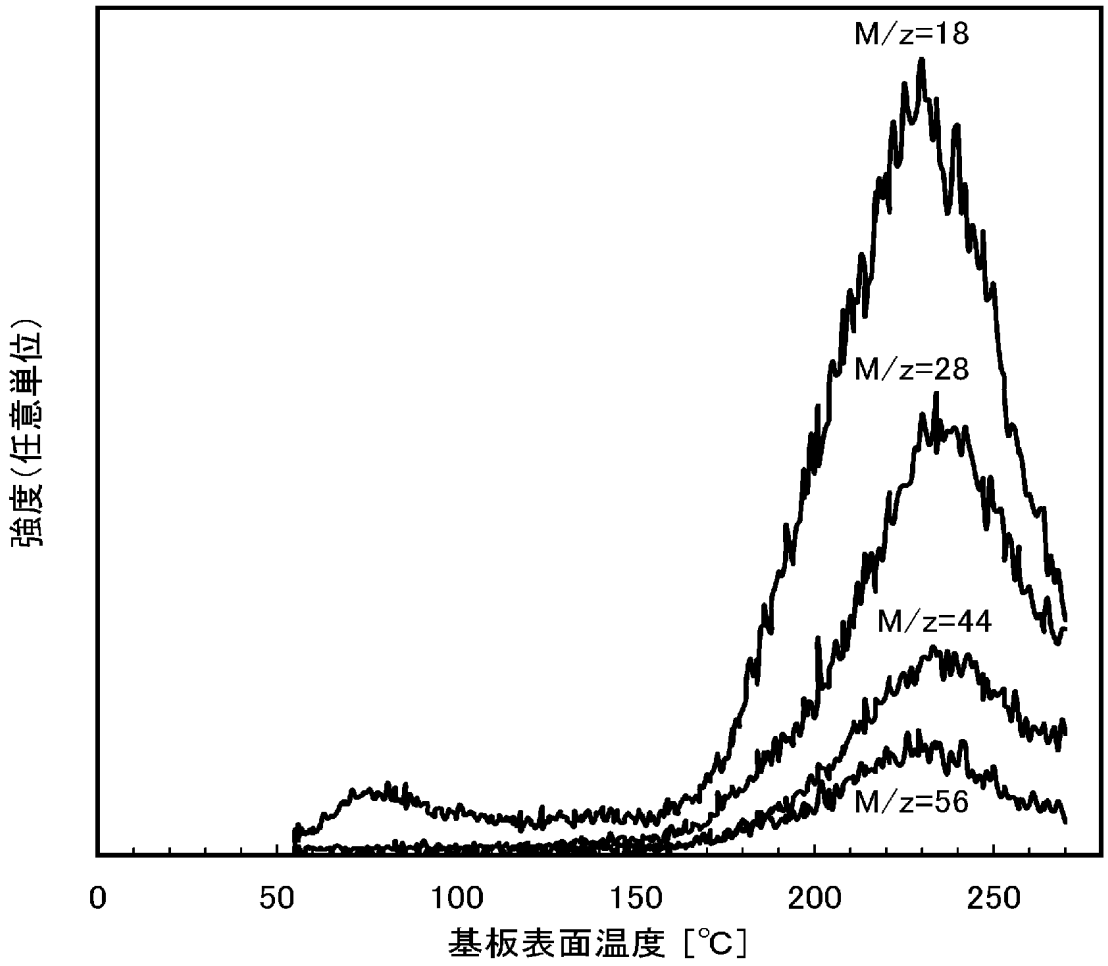
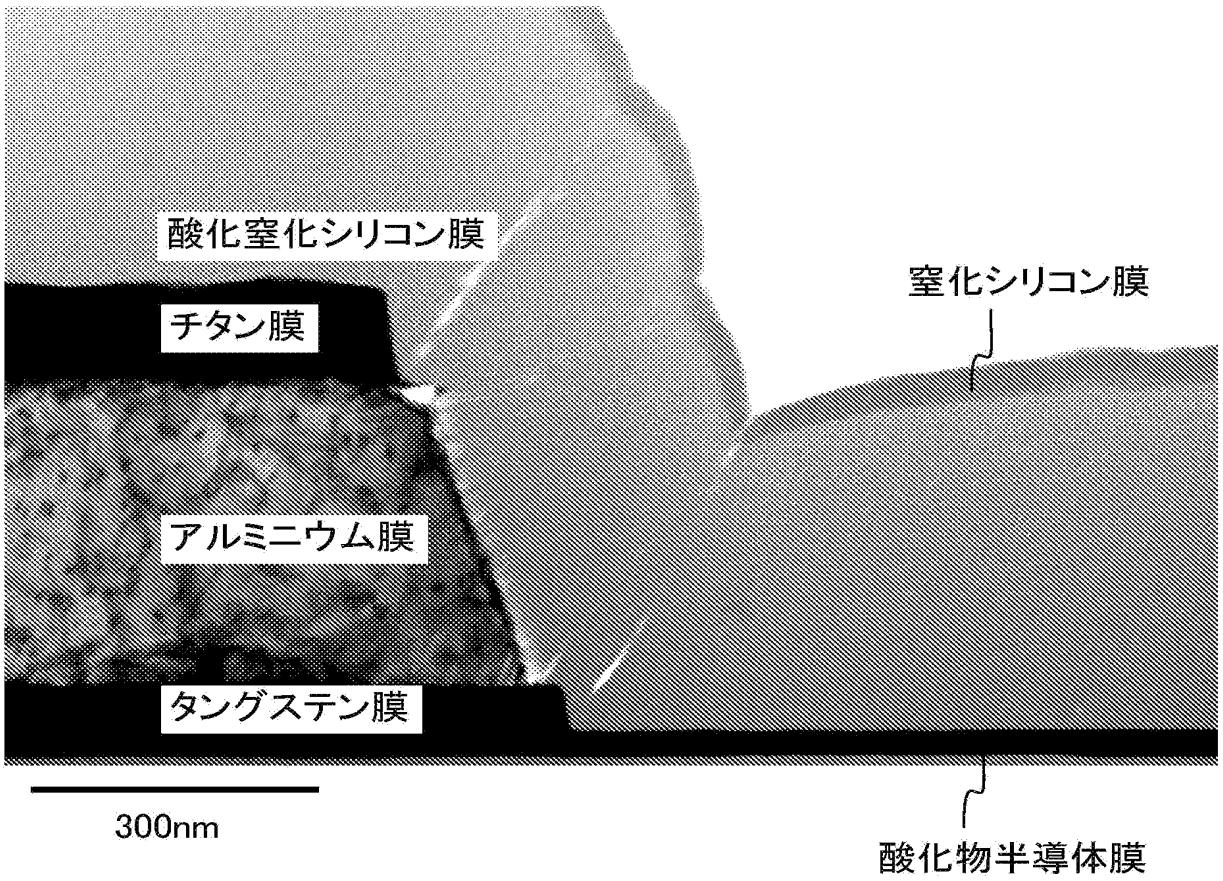
質量電荷比
強度（任意単位）

【図９】



【図１０】



【図１１】

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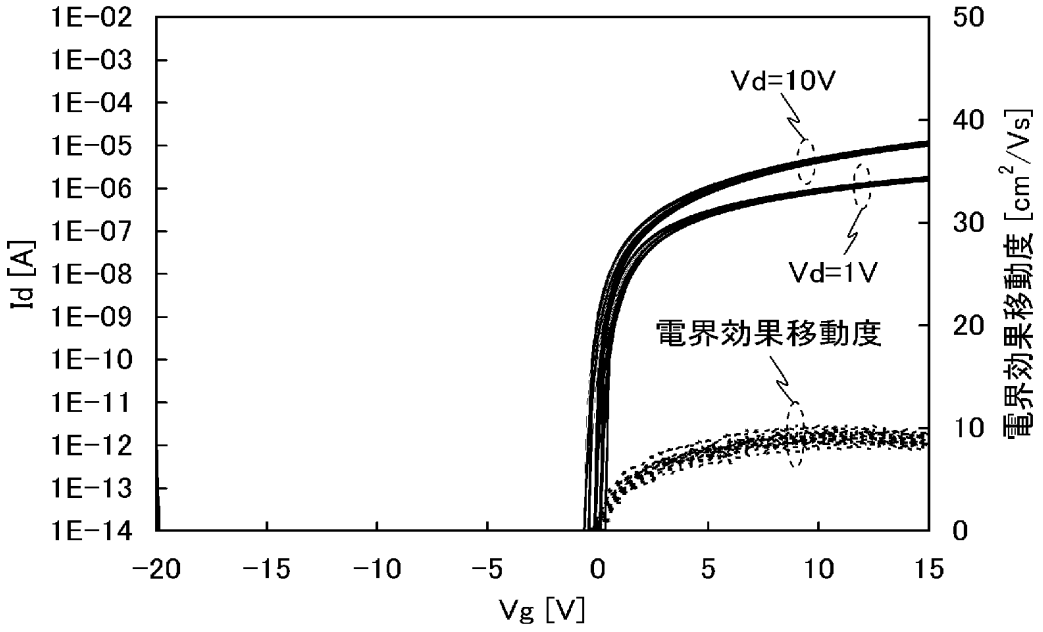
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1E-03
1E-04
1E-05
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0
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10
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Vg [V]
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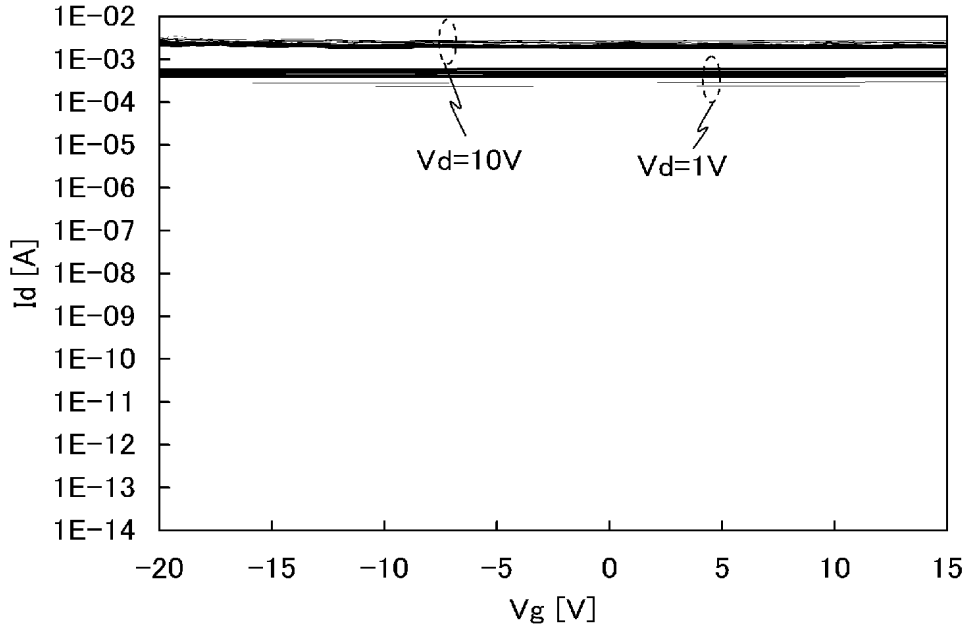
Vd=1V
電界効果移動度

(B)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0
5
10
15
Vg [V]
Vd=10V
Vd=1V

出願人履歴

０００１５３８７８

19900817

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/939,323	07/11/2013	Yasuharu HOSAKA	0756-10194

CONFIRMATION NO. 2340

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31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

OC00000066206134

Title:DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

Publication No.US-2014-0022479-A1
Publication Date:01/23/2014

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Sheet 1 of 6

Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA et al.
Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-2003/0189210	10-09-2003	YAMAZAKI.S et al.	
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		US-8115206	02-14-2012	SAKAKURA.M et al.	
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		US-2012/0175625	07-12-2012	YAMAZAKI.S	
		US-8405092	03-26-2013	INOUE.S et al.	
		US-8415669	04-09-2013	YAMAZAKI.S et al.	
		US-2013/0168670	07-04-2013	INOUE.S et al.	
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		US-2011/0198598	08-18-2011	KIM.Y et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] -Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP-2003-197367A	07-11-2003			Abst.
		WO-2011/102203	08-25-2011			Eng.
		WO-2007/011061	01-25-2007			Eng.
		WO-2012/035984	03-22-2012			Eng.
		JP-2003-302917A	10-24-2003			Abst.
		JP-2012-084864A	04-26-2012			Abst.

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 6

Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA et al.
Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-7796101	09-14-2010	IWASHITA.T et al.	
		US-8059067	11-15-2011	IWASHITA.T et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] -Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP-2011-192977A	09-29-2011			Abst.
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		JP-2011-171300A	09-01-2011			Abst.
		TW-201230341	07-16-2012			Abst.
		JP-2012-160715A	08-23-2012			Abst.

Examiner Signature		Date Considered	

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Sheet 3 of 6

Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA et al.
Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] -Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		CN-102593185	07-18-2012			Abst.
		KR-2012-0090779A	08-17-2012			Abst.
		TW-201238056	09-16-2012			Abst.
		TW-201214711	04-01-2012			Abst.
		KR-2012-0138770A	12-26-2012			Abst.
		TW-I264822	10-21-2006			Abst.

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 4 of 6

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Application Number	13/939,323
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		CN-001450665	10-22-2003			Abst.
		KR-2010-0061420A	06-07-2010			Abst.
		KR-2008-0035643A	04-23-2008			Abst.
		EP-1835540A	09-19-2007			Eng.
		KR-2007-0093830A	09-19-2007			Abst.
		CN-101038932	09-19-2007			Abst.

Examiner Signature		Date Considered	

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Sheet 5 of 6

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Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA et al.
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		KR-2011-0094458A	08-24-2011			Abst.

Examiner Signature		Date Considered	

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Sheet 6 of 6

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Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		INTERNATIONAL SEARCH REPORT (APPLICATION NO.PCT/JP2013/069456) DATED October 22, 2013.	Eng.
		WRITTEN OPINION (APPLICATION NO.PCT/JP2013/069456) DATED October 22, 2013.	Eng.

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Electronic Acknowledgement Receipt

EFS ID:	17373551
Application Number:	13939323
International Application Number:	
Confirmation Number:	2340
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu HOSAKA
Customer Number:	31780
Filer:	Eric J. Robinson/Doris Vasquez Soriano
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10194
Receipt Date:	12-NOV-2013
Filing Date:	11-JUL-2013
Time Stamp:	13:28:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS12NOV2013.pdf	1238200 f341170e63bd5fca9557c31b67e30490b07a11b3	yes	8

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	2	
	Information Disclosure Statement (IDS) Form (SB08)		3	8	
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Information:					
2	Foreign Reference	JP2003197367.pdf	4574958 7d1fada0099b6c96d548a9bb0a3ae278ef97ffb7	no	24
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3	Foreign Reference	WO2011102203.pdf	9995703 227a1e32ca66494302e941758e538de1984a6af4	no	81
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4	Foreign Reference	WO2007011061.pdf	13004151 fc4f1fb9849820bf4d15a018d14a30d83f4c8aa3	no	95
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8	Foreign Reference	JP2011192977.pdf	6747217 319fef76751c83dd8ec792aae0429da5ce282685	no	38
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18	Foreign Reference	KR20120138770.pdf	5633518 c6004065b7ded55bed2af9a95c14b7dcee552128	no	40
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21	Foreign Reference	KR20100061420.pdf	6817809 0dca36727c2c1d19da38885b730c866baffe4c2c	no	55
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24	Foreign Reference	KR20070093830.pdf	2701917 4ac9a15dbd9db1dc5611ba3850e468b66227e85c	no	22
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25	Foreign Reference	CN101038932.pdf	4567183 884ce71cc96719813fc392e74e3a8c5633974f36	no	29
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Information:					
26	Foreign Reference	KR20110094458.pdf	2655480 c0c25ddbb6001cad63568ebfcb8da144e4c5be97	no	19
Warnings:					
Information:					

27	Non Patent Literature	INTERNATIONALSEARCHREPORT.pdf	721536 c9c7a33e44001a12b97cc8e0e738eabfd44e064c	no	6
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Information:					
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Warnings:					
Information:					
			Total Files Size (in bytes):	188201023	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Attorney Docket No. 0756-10194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 2340
Yasuharu HOSAKA et al.	)	Group Art Unit: 2871
Serial No. 13/939,323	)	Examiner: E. Glick
Filed: July 11, 2013	)	
For: DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

Unless otherwise noted, the references submitted were cited in PCT Application No. PCT/JP2013/069456 in an International Search Report mailed October 22, 2013.

U.S. Patent No. 8,405,092 and U.S. Publication Nos. 2013/0168670 and 2012/0061666 and WO 2012/035984 and TW 201230341 are in the family JP 2012-084864. U.S. Patent No. 8,405,092 and U.S. Publication No. 2013/0168670 were not directly cited by the foreign patent office, but are submitted herewith for consideration by the Examiner.

U.S. Patent Nos. 6,861,710; 7,033,848 and 7,492,012 and U.S. Publication No. 2003/0127651 are in the family of JP 2003-197367. U.S. Patent Nos. 6,861,710; 7,033,848 and 7,492,012 were not directly cited by the foreign patent office, but are submitted herewith for consideration by the Examiner.

U.S. Publication No. 2012/0175625 is in the family of JP 2012-160715 and CN 102593185 and KR 2012-0090779 and TW 201238056.

U.S. Publication No. 2011/0204368 and WO 2011/102203 and TW 201214711 and KR 2012-0138770 are in the family of JP 2011-192977.

U.S. Patent Nos. 7,671,369; 8,008,666 and 8,415,669 and U.S. Publication Nos. 2013/0221361 and 2003/0189210 and TW I264822 and CN 001450665 and KR 2010-0061420 are in the family of JP 2003-302917. U.S. Patent Nos. 7,671,369; 8,008,666 and 8,415,669 and U.S. Publication No. 2013/0221361 were not directly cited by the foreign patent office, but are submitted herewith for consideration by the Examiner.

U.S. Patent No. 8,115,206 and U.S. Publication Nos. 2012/0132919 and 2009/0261337 and WO 2007/011061 and KR 2008-0035643 are in the family of JP 2007-053355. U.S. Patent No. 8,115,206 and U.S. Publication No. 2012/0132919 were not directly cited by the foreign patent office, but are submitted herewith for consideration by the Examiner.

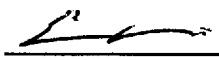
U.S. Patent Nos. 7,796,101 and 8,059,067 and U.S. Publication No. 2008/0036705 and EP 1 835 540 and KR 2007-0093830 and CN 101038932 are in the family of JP 2007-250244. U.S. Patent Nos. 7,796,101 and 8,059,067 were not directly cited by the foreign patent office, but are submitted herewith for consideration by the Examiner.

U.S. Publication No. 2011/0198598 and KR 2011-0094458 are in the JP 2011-171300.

This Information Disclosure Statement is being submitted before the issuance of a first Office Action on the merits, therefore, no fee is required.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



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(571) 434-6789

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Sheet 1 of 12

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		US-2002/0056838	05-16-2002	OGAWA.K	
		US-2003/0189401	10-09-2003	KIDO.J et al.	
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		US-2006/0108529	05-25-2006	SAITO.K et al.	
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		US-2006/0113565	06-01-2006	ABE.K et al.	
		US-2006/0113539	06-01-2006	SANO.M et al.	
		US-2006/0113549	06-01-2006	DEN.T et al.	

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		JP-2000-150900A	05-30-2000			Abst.
		JP-60-198861A	10-08-1985			Full
		JP-2004-103957A	04-02-2004			Abst.
		JP-11-505377	05-18-1999			Abst.
		JP-08-264794A	10-11-1996			Full
		JP-2000-044236A	02-15-2000			Full

Examiner Signature		Date Considered	

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		US-7323356	01-29-2008	HOSONO.H et al.	
		US-6294274	09-25-2001	KAWAZOE.H et al.	
		US-7061014	06-13-2006	HOSONO.H et al.	
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		US-2009/0073325	03-19-2009	KUWABARA.H et al.	
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		US-2007/0194379	08-23-2007	HOSONO.H et al.	
		US-2009/0134399	05-28-2009	SAKAKURA.M et al.	
		US-2006/0231882	10-19-2006	KIM.I et al.	
		US-2006/0284171	12-21-2006	LEVY.D et al.	
		US-2006/0284172	12-21-2006	ISHII.H	
		US-2006/0292777	12-28-2006	DUNBAR.T	
		US-2007/0024187	02-01-2007	SHIN.H et al.	
		US-2007/0046191	03-01-2007	SAITO.K	

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		JP-2002-289859A	10-04-2002			Full
		JP-05-251705A	09-28-1993			Full
		JP-2002-076356A	03-15-2002			Full
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Sheet 3 of 12

Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA et al.
Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Sheet 6 of 12

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Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

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Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA et al.
Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

NON PATENT LITERATURE DOCUMENTS

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(Use as many sheets as necessary)				Art Unit	2871
				Examiner Name	E. Glick
Sheet	8	of	12	Attorney Docket Number	0756-10194

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Sheet 10 of 12

Complete if Known	
Application Number	13/939,323
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA et al.
Art Unit	2871
Examiner Name	E. Glick
Attorney Docket Number	0756-10194

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	13/939,323
				Filing Date	July 11, 2013
				First Named Inventor	Yasuharu HOSAKA et al.
(Use as many sheets as necessary)				Art Unit	2871
				Examiner Name	E. Glick
Sheet	11	of	12	Attorney Docket Number	0756-10194

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	13/939,323
				Filing Date	July 11, 2013
				First Named Inventor	Yasuharu HOSAKA et al.
(Use as many sheets as necessary)				Art Unit	2871
				Examiner Name	E. Glick
Sheet	12	of	12	Attorney Docket Number	0756-10194

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EFS ID:	16833703
Application Number:	13939323
International Application Number:	
Confirmation Number:	2340
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu HOSAKA
Customer Number:	31780
Filer:	Eric J. Robinson/Doris Vasquez Soriano
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10194
Receipt Date:	19-SEP-2013
Filing Date:	11-JUL-2013
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Application Type:	Utility under 35 USC 111(a)

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Warnings:					
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47	Non Patent Literature	67_PARK_DRY.pdf	885984 c963f077e46f318469c1fdfe7da963ea5f4b31dc	no	4
Warnings:					
Information:					
48	Non Patent Literature	68_OH_IMPROVING_THE_GATE.pdf	1192533 ef22000cec95d5f376bfe5caf8f46bd8d1be01d9	no	6
Warnings:					
Information:					
49	Non Patent Literature	69_UENO_FIELD_EFFECT_TRANSISTOR.pdf	812168 7108ae13a91fa62f4cd400ad0b4850ac53f1fbd1	no	3
Warnings:					
Information:					
50		MASTERIDS19SEPT2013.pdf	3277313 df0a774216536fbc74c9b1711df5faf17ea12726	yes	13

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal Letter	1	1
Information Disclosure Statement (IDS) Form (SB08)	2	13

Warnings:	
Information:	
Total Files Size (in bytes):	43371000

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Attorney Docket No. 0756-10194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 2340
Yasuharu HOSAKA et al.	)	Group Art Unit: 2871
Serial No. 13/939,323	)	Examiner: E. Glick
Filed: July 11, 2013	)	
For: DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

U.S. Patent Nos. 6,727,522 and 7,064,346 are in the family of JP 2000-150900.

U.S. Patent No. 7,061,014 is in the family of JP 2004-103957.

U.S. Patent No. 5,744,864 is in the family of JP 11-505377.

U.S. Patent No. 6,563,174 is in the family of JP 2003-086808.

U.S. Publication No. 2006/0244107 is in the family of WO 2004/114391.

Although no fee is due for this Information Disclosure Statement, the Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/939,323

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/939,323	07/11/2013	2811	1600	0756-10194	20	2

CONFIRMATION NO. 2340

31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

FILING RECEIPT

OC000000062868614

Date Mailed: 08/01/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Yasuharu HOSAKA, Tochigi, JAPAN;
Yukinori SHIMA, Tatebayashi, JAPAN;
Kenichi OKAZAKI, Tochigi, JAPAN;
Shunpei YAMAZAKI, Setagaya, JAPAN;

Applicant(s)

Semiconductor Energy Laboratory Co., Ltd., Atsugi-shi, JAPAN

Non-Applicant Assignee(s)

Semiconductor Energy Laboratory Co., Ltd.

Power of Attorney: The patent practitioners associated with Customer Number 31780

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
JAPAN 2012-161344 07/20/2012

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to**

Retrieve Electronic Priority Application(s) (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 07/26/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/939,323**

Projected Publication Date: 01/23/2014

Non-Publication Request: No

Early Publication Request: No

Title

DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/939,323	07/11/2013	Yasuharu HOSAKA	0756-10194

CONFIRMATION NO. 2340

POA ACCEPTANCE LETTER

31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

OC000000062868622

Date Mailed: 08/01/2013

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/11/2013.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/ewondimu/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

DocCode – SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 13939323 Document Date: 07/11/2013

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawing

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

To access the documents in the SCORE database, refer to instructions developed by SIRA.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (http://es/ScoreAccessWeb/).
- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: February 8, 2006

PTO/AIA/15 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	0756-10194
First Named Inventor	Yasuharu HOSAKA et al.
Title	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. ☐ **Applicant asserts small entity status.** See 37 CFR 1.27
3. ☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. ☑ **Specification** [*Total Pages* 59] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. ☑ **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 11]
6. **Inventor's Oath or Declaration** [*Total Pages* 8] *(Including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. ☑ Newly executed (original or copy)
   b. ☐ A copy from a prior application (37 CFR 1.63(d))
7. ☑ **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   ☐ Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** *(if applicable, items a. – c. are required)*
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

ACCOMPANYING APPLICATION PAPERS

10. ☑ **Assignment Papers** (cover sheet & document(s)) Name of Assignee: Semiconductor Energy Laboratory Co., Ltd.
11. ☑ **37 CFR 3.73(c) Statement** *(when there is an assignee)* ☑ **Power of Attorney**
12. ☐ **English Translation Document** *(if applicable)*
13. ☑ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☑ Copies of citations attached
14. ☐ **Preliminary Amendment**
15. ☐ **Return Receipt Postcard** *(MPEP § 503) (Should be specifically itemized)*
16. ☐ **Certified Copy of Priority Document(s)** *(if foreign priority is claimed)*
17. ☐ **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. ☐ **Other:**

*Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 31780 **OR** ☐ Correspondence address below

Name	Eric J. Robinson, Robinson Intellectual Property Law Office, P.C.				
Address	3975 Fair Ridge Drive, Suite 20 North				
City	Fairfax	State	VA	Zip Code	22033
Country	US	Telephone	571-434-6789	Email	erobinson@riplo.com

Signature		Date	July 11, 2013
Name (Print/Type)	Stephen P. Catlin	Registration No. (Attorney/Agent)	36,101

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Semiconductor Energy Laboratory Co., Ltd.

Application No./Patent No.: _____ Filed/Issue Date: July 11, 2013

Titled: DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

Semiconductor Energy Laboratory Co., Ltd., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

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The document was recorded in the United States Patent and Trademark Office at

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature	July 11, 2013 Date
Stephen P. Catlin Printed or Typed Name	Reg. No. 36,101 Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Attorney Docket No. 0756-10194

ASSIGNMENT

Serial No. _____ Filed _____

WHEREAS, Yasuharu HOSAKA , Yukinori SHIMA , Kenichi OKAZAKI and Shunpei YAMAZAKI
(hereinafter designated as the undersigned) has (have) invented certain new and useful improvements in DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE for which an application for Letters Patent of the United States of America has been executed by the undersigned on , and;

WHEREAS, Semiconductor Energy Laboratory Co., Ltd. of 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036 Japan and its heirs, successors, legal representatives and assigns (hereinafter designated as the Assignee) is desirous of acquiring the entire right, title and interest in and to said invention and in and to any Letters Patent(s) that may be granted therefor in the United States of America;

NOW, THEREFORE, in consideration of the sum of One Dollar ($1.00) to the undersigned in hand paid, the receipt of which is hereby acknowledged, and other good and valuable consideration, the undersigned has (have) sold, assigned and transferred, and by these presents do sell, assign and transfer unto said Assignee the full and exclusive right to the said invention in the United States of America and its territories and for all foreign countries, dependencies and possessions and the entire right, title and interest in and to any and all Letters Patent(s) which may be granted therefor in the United States of America and its territories, dependencies and possessions, and in and to any and all divisions, reissues, continuations and extensions thereof for the full term or terms for which the same may be granted.

The undersigned agree(s) to execute all papers necessary in connection with this application and any continuing, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

The undersigned agree(s) to execute all papers necessary in connection with any interference which may be declared concerning this application or any continuation, division or reissue thereof or Letters Patent(s) or reissue patent issued thereon and to cooperate with the Assignee in every way possible in obtaining and producing evidence and proceeding with such interference.

The undersigned agree(s) to execute all papers and documents and to perform any act which may be necessary in connection with claims under or provisions of the International Convention for the Protection of Industrial Property or similar agreements.

The undersigned agree(s) to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent(s) to the Assignee and to vest all rights therein hereby conveyed to said Assignee as fully and entirely as the same would have been held by the undersigned if this Assignment and sale had not been made.

The undersigned hereby authorize(s) and request(s) the Commissioner of Patents and Trademarks to issue any and all Letters Patents of the United States of America resulting from

said application or any division or divisions or continuing or reissue applications thereof to the said Assignee, as Assignee of the entire interest, and hereby convenants that he has (they have) the full right to convey the entire interest herein assigned, and that he has (they have) not executed, and will not execute, any agreement in conflict herewith.

The undersigned hereby grant(s) the law firm of ROBINSON INTELLECTUAL PROPERTY LAW OFFICE the power to insert on this Assignment any further identification which may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office for recordation of this document.

In witness thereof, this Assignment has been executed by the undersigned on the date(s) opposite the undersigned name(s).

Date 07/02/2013 Signature Yasuharu HOSAKA
Name Yasuharu HOSAKA

Date 07/02/2013 Signature Yukinori Shima
Name Yukinori SHIMA

Date 07/02/2013 Signature Kenichi OKAZAKI
Name Kenichi OKAZAKI

Date _____ Signature _____
Name Shunpei YAMAZAKI

This assignment should preferably be acknowledged before a United States Consul or Notary Public. If not, then the execution by the Inventor(s) should be witnessed has (have) invented certain new and useful improvements in by at least two other persons who should sign here.

Witness _____ Signature _____

Witness _____ Signature _____

Witness _____ Signature _____

Attorney Docket No. _____

ASSIGNMENT

Serial No. _____ Filed _____

WHEREAS, Yasuharu HOSAKA , Yukinori SHIMA , Kenichi OKAZAKI and Shunpei YAMAZAKI
(hereinafter designated as the undersigned) has (have) invented certain new and useful improvements in DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE for which an application for Letters Patent of the United States of America has been executed by the undersigned on , and;

WHEREAS, Semiconductor Energy Laboratory Co., Ltd. of 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036 Japan and its heirs, successors, legal representatives and assigns (hereinafter designated as the Assignee) is desirous of acquiring the entire right, title and interest in and to said invention and in and to any Letters Patent(s) that may be granted therefor in the United States of America;

NOW, THEREFORE, in consideration of the sum of One Dollar ($1.00) to the undersigned in hand paid, the receipt of which is hereby acknowledged, and other good and valuable consideration, the undersigned has (have) sold, assigned and transferred, and by these presents do sell, assign and transfer unto said Assignee the full and exclusive right to the said invention in the United States of America and its territories and for all foreign countries, dependencies and possessions and the entire right, title and interest in and to any and all Letters Patent(s) which may be granted therefor in the United States of America and its territories, dependencies and possessions, and in and to any and all divisions, reissues, continuations and extensions thereof for the full term or terms for which the same may be granted.

The undersigned agree(s) to execute all papers necessary in connection with this application and any continuing, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

The undersigned agree(s) to execute all papers necessary in connection with any interference which may be declared concerning this application or any continuation, division or reissue thereof or Letters Patent(s) or reissue patent issued thereon and to cooperate with the Assignee in every way possible in obtaining and producing evidence and proceeding with such interference.

The undersigned agree(s) to execute all papers and documents and to perform any act which may be necessary in connection with claims under or provisions of the International Convention for the Protection of Industrial Property or similar agreements.

The undersigned agree(s) to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent(s) to the Assignee and to vest all rights therein hereby conveyed to said Assignee as fully and entirely as the same would have been held by the undersigned if this Assignment and sale had not been made.

The undersigned hereby authorize(s) and request(s) the Commissioner of Patents and Trademarks to issue any and all Letters Patents of the United States of America resulting from

said application or any division or divisions or continuing or reissue applications thereof to the said Assignee, as Assignee of the entire interest, and hereby convenants that he has (they have) the full right to convey the entire interest herein assigned, and that he has (they have) not executed, and will not execute, any agreement in conflict herewith.

The undersigned hereby grant(s) the law firm of ROBINSON INTELLECTUAL PROPERTY LAW OFFICE the power to insert on this Assignment any further identification which may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office for recordation of this document.

In witness thereof, this Assignment has been executed by the undersigned on the date(s) opposite the undersigned name(s).

Date_____ Signature_____
Name Yasuharu HOSAKA

Date_____ Signature_____
Name Yukinori SHIMA

Date_____ Signature_____
Name Kenichi OKAZAKI

Date 09/02/2013 Signature_____
Name Shunpei YAMAZAKI

This assignment should preferably be acknowledged before a United States Consul or Notary Public. If not, then the execution by the Inventor(s) should be witnessed has (have) invented certain new and useful improvements in by at least two other persons who should sign here.

Witness_____ Signature_____

Witness_____ Signature_____

Witness_____ Signature_____

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10194
	Application Number	
Title of Invention	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yasuharu		HOSAKA	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Tochigi	Country of Residence i	JP

Mailing Address of Inventor:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country** i	JP

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yukinori		SHIMA	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Tatebayashi	Country of Residence i	JP

Mailing Address of Inventor:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country** i	JP

Inventor 3 Remove

Legal Name

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10194
	Application Number	
Title of Invention	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kenichi		OKAZAKI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Tochigi	Country of Residence i	JP

Mailing Address of Inventor:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country** i	JP

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shunpei		YAMAZAKI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Setagaya	Country of Residence i	JP

Mailing Address of Inventor:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country** i	JP

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	31780		
Email Address	erobinson@riplo.com	Add Email	Remove Email

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10194
	Application Number	
Title of Invention	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	

Application Information:

Title of the Invention	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE		
Attorney Docket Number	0756-10194	**Small Entity Status Claimed** ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	11	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	31780		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10194
	Application Number	
Title of Invention	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [j] (if applicable)
2012-161344	JP	2012-07-20	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10194
	Application Number	
Title of Invention	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(●) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. [X]

Organization Name	Semiconductor Energy Laboratory Co., Ltd.		
Mailing Address Information:			
Address 1	398, Hase		
Address 2			
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Country [i]	JP	Postal Code	243-0036
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (03-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10194
	Application Number	
Title of Invention	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE	

Assignee 1

Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).

Remove

If the Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information:

Address 1	
Address 2	

City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Stephen P. Catlin/			Date (YYYY-MM-DD)	2013-07-11
First Name	Stephen P.	Last Name	Catlin	Registration Number	36101

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Attorney Docket No. 0756-10194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	
Yasuharu HOSAKA et al.	)	
Based on JP 2012-161344	)	New Application
Filed: July 20, 2012	)	
For: DISPLAY DEVICE AND ELECTRONIC	)	
DEVICE INCLUDING THE DISPLAY DEVICE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

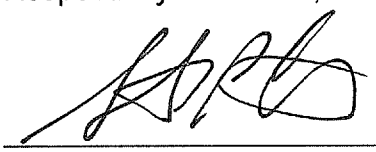
In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

U.S. Patent Nos. 7,791,072 and 8,237,166 and U.S. Publication Nos. 2006/0113536 and 2010/0295041 are in the family of JP 2006-165528.

U.S. Patent No. 8,269,218 and U.S. Publication Nos. 2011/0133181 and 2012/0319118 are in the family of JP 2011-139047.

Although no fee is due for this Information Disclosure Statement, the Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



Stephen P. Catlin
Reg. No. 36,101

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

PTO/AIA/80 (07-12)
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U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☑ Practitioners associated with Customer Number: 31780

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 31780

OR

☐	Firm or Individual Name		
	Address		
	City		
	Country		
	Telephone		Email

Assignee Name and Address: SEMICONDUCTOR ENERGY LABORATORY CO., LTD.
398, HASE, ATSUGI-SHI
KANAGAWA-KEN 243-0036
JAPAN

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Shunpei Yamazaki	Date	09/21/2012
Name	Dr. Shunpei Yamazaki	Telephone	81-46-270-1170
Title	President		

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	
Filing Date	July 11, 2013
First Named Inventor	Yasuharu HOSAKA et al.
Art Unit	
Examiner Name	
Attorney Docket Number	0756-10194

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US2006/0113536	06-01-2006	KUMOMI et al.	
		US7791072	09-07-2010	KUMOMI et al.	
		US2010/0295041	11-25-2010	KUMOMI et al.	
		US8237166	08-07-2012	KUMOMI et al.	
		US2011/0133181	06-09-2011	YAMAZAKI	
		US8269218	09-18-2012	YAMAZAKI	
		US2012/0319118	12-20-2012	YAMAZAKI	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] -Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP2006-165528	06-22-2006			abst.
		JP2011-139047	07-14-2011			abst.

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

PTO/AIA/01 (06-12)
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申請データシート(37 CFR 1.76)を使った実用及び意匠登録出願宣誓書(37 CFR 1.63)
DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

発明の名称 Title of Invention	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

下記発明者である私は、つぎのことがらを宣誓します。
As the below named inventor, I hereby declare that:

本宣誓は This declaration is directed to:

■ 添付されている、あるいは The attached application, or

☐ 米国出願、あるいは_____に出願されたPCT国際願番号_____として出願されているものに宛てられています。
United States application or PCT international application number _____filed on _____.

上記の出願は私自身、あるいは私が権限を授与したものによって行われたものです。
The above-identified application was made or authorized to be made by me.

私は本出願書中にあらわれるもともとの発明者、あるいはもともとの共同発明者です。
I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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発明者の正式氏名
LEGAL NAME OF INVENTOR

発明者: Inventor: Yasuharu HOSAKA　　日付(任意): Date (Optional): 07/02/2013

署名: Signature: Yasuharu HOSAKA

備考: 出願データシート(PTO/AIA/14 あるいはその同等用紙) は、発明の自主独立体全体の命名を含め、本用紙に添付すること。なお残余の発明者ごとにPTO/SB/AIA01 用紙を使用する。
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申請データシート(37 CFR 1.76)を使った実用及び意匠登録出願宣誓書(37 CFR 1.63)
DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

発明の名称 Title of Invention	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

下記発明者である私は、つぎのことがらを宣誓します。
As the below named inventor, I hereby declare that:

本宣誓は This declaration is directed to:

■ 添付されている、あるいは The attached application, or

☐ 米国出願、あるいは_____に出願されたPCT国際願番号_____として出願されているものに宛てられています。
United States application or PCT international application number _____filed on _____.

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The above-identified application was made or authorized to be made by me.

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I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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発明者の正式氏名
LEGAL NAME OF INVENTOR

発明者: Inventor: Yukinori SHIMA　　日付(任意): Date (Optional): 07/02/2013

署名: Signature: Yukinori Shima

備考: 出願データシート(PTO/AIA/14 あるいはその同等用紙) は、発明の自主独立体全体の命名を含め、本用紙に添付すること。なお残余の発明者ごとに PTO/SB/AIA01 用紙を使用する。
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

発明の名称 Title of Invention	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

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発明者の正式氏名
LEGAL NAME OF INVENTOR

発明者: Inventor: Kenichi OKAZAKI　　日付(任意): Date (Optional): 07/02/2013

署名: Signature: Kenichi OKAZAKI

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LEGAL NAME OF INVENTOR

発明者: Inventor: Shunpei YAMAZAKI　　日付(任意): Date (Optional): 07/02/2013

署名: Signature: Shunpei Yamazaki

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DESCRIPTION

DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

TECHNICAL FIELD

[0001]

The present invention relates to a display device using a liquid crystal panel or a display device using an organic EL panel. The present invention further relates to an electronic device including the display device.

BACKGROUND ART

[0002]

In recent years, display devices using liquid crystal panels and display devices using organic EL panels have been under active development. These display devices are broadly classified into display devices in which only a transistor for pixel control (pixel transistor) is formed over a substrate and a scanning circuit (driver circuit) is included in a peripheral IC and display devices in which a scanning circuit is formed over the same substrate as the pixel transistor.

[0003]

A display device in which a driver circuit is integrated with a pixel transistor is effective in reducing the frame width of the display device or cost of the peripheral IC. However, a transistor used in the driver circuit is required to have better electrical characteristics (e.g., field-effect mobility (μFE) or threshold) than the pixel transistor.

[0004]

A silicon-based semiconductor material is widely known as a material for a semiconductor thin film applicable to a transistor. As another material, an oxide semiconductor material has been attracting attention. For example, a transistor in which a semiconductor thin film is formed using an amorphous oxide that contains indium (In), gallium (Ga), and zinc (Zn) and has an electron carrier concentration lower than 10^{18} /cm^3 is disclosed (for example, see Patent Document 1).

[0005]

A transistor using an oxide semiconductor for a semiconductor layer has higher field-effect mobility than a transistor using amorphous silicon which is a silicon-based semiconductor material for a semiconductor layer. Hence, the transistor using an oxide semiconductor can operate at high speed and be suitably used for the display device in which a pixel transistor is integrated with a driver circuit. Besides, manufacturing steps of the transistor using an oxide semiconductor are easier than those of a transistor using polycrystalline silicon for a semiconductor layer.

[0006]

However, a problem of the transistor using an oxide semiconductor for a semiconductor layer is that entry of impurities such as hydrogen or moisture into the oxide semiconductor generates carriers and changes electrical characteristics of the transistor.

[0007]

To solve the above problem, a transistor whose reliability is improved by making the concentration of hydrogen atoms in an oxide semiconductor film used as a channel formation region of the transistor less than 1×10^{16} cm^{-3} is disclosed (e.g., Patent Document 2).

[References]

[0008]

Patent Document 1: Japanese Published Patent Application No. 2006-165528

Patent Document 2: Japanese Published Patent Application No. 2011-139047

DISCLOSURE OF INVENTION

[0009]

As also described in Patent Document 2, to sufficiently maintain the electrical characteristics of the transistor using an oxide semiconductor film for a semiconductor layer, it is important to remove hydrogen, moisture, and the like from the oxide semiconductor film as much as possible.

[0010]

Further, when transistors are used for both a pixel region and a driver circuit region in a display device, an electrical load on the transistor used for the driver circuit region is larger than that on the transistor used for the pixel region, although this

depends on the driving method. Thus, electrical characteristics of the transistor used for the driver circuit region is important.

[0011]

In particular, a problem with display devices in which transistors using an oxide semiconductor film for a semiconductor layer are used for the pixel region and the driver circuit region has been deterioration of the transistor used for the driver circuit region, which occurs in a reliability test in a high temperature and high humidity environment. The cause of the deterioration of the transistor is an increase in the carrier density of the oxide semiconductor film used as the semiconductor layer due to entry of moisture or the like into the oxide semiconductor film from an organic insulating film formed over the transistor.

[0012]

In view of the above, an object of one embodiment of the present invention is to suppress changes in the electrical characteristics of a display device including transistors in a pixel region and a driver circuit region and improve the reliability of the display device. An object of one embodiment of the present invention is, in particular, to suppress entry of hydrogen or moisture into the oxide semiconductor film in a display device using an oxide semiconductor film for a channel formation region of a transistor, suppress changes in the electrical characteristics of the display device, and improve its reliability.

[0013]

To achieve any of the above objects, one embodiment of the present invention provides a structure which can suppress changes in the electrical characteristics of transistors used for a pixel region and a driver circuit region in a display device. Specifically, one embodiment of the present invention provides a structure in which, an oxide semiconductor film is used for a channel formation region of a transistor, and a planarization film formed with an organic insulating material over the transistor has a characteristic structure so that hydrogen or moisture hardly enters the oxide semiconductor film, particularly the oxide semiconductor film used for the driver circuit region. The structure is more specifically described below.

[0014]

One embodiment of the present invention is a display device including a pixel

region where a plurality of pixels each including a pixel electrode and at least one first transistor electrically connected to the pixel electrode is arranged, a first substrate provided with a driver circuit region that is located outside and adjacent to the pixel region and includes at least one second transistor which supplies a signal to the first transistor included in each of the pixels in the pixel region, a second substrate provided to face the first substrate, a liquid crystal layer interposed between the first substrate and the second substrate, a first interlayer insulating film including an inorganic insulating material over the first transistor and the second transistor, a second interlayer insulating film including an organic insulating material over the first interlayer insulating film, and a third interlayer insulating film including an inorganic insulating material over the second interlayer insulating film. In the display device, the third interlayer insulating film is provided in part of an upper region of the pixel region, and an edge portion of the third interlayer insulating film is formed on an inner side than the driver circuit region.

[0015]

In the above structure, the following may be included: a first alignment film over the pixel electrode; the liquid crystal layer over the first alignment film; a second alignment film over the liquid crystal layer; a counter electrode over the second alignment film; an organic protective insulating film over the counter electrode; a colored film and a light-blocking film over the organic protective insulating film; and the second substrate over the colored film and the light-blocking film.

[0016]

Another embodiment of the present invention is a display device including a pixel region where a plurality of pixels each including a pixel electrode and at least one first transistor electrically connected to the pixel electrode is arranged, a first substrate provided with a driver circuit region that is located outside and adjacent to the pixel region and includes at least one second transistor which supplies a signal to the first transistor included in each of the pixels in the pixel region, a second substrate provided to face the first substrate, a light-emitting layer interposed between the first substrate and the second substrate, a first interlayer insulating film including an inorganic insulating material over the first transistor and the second transistor, a second interlayer insulating film including an organic insulating material over the first interlayer insulating film, and a third interlayer insulating film including an inorganic insulating

material over the second interlayer insulating film. In the display device, the third interlayer insulating film is provided in part of an upper region of the pixel region, and an edge portion of the third interlayer insulating film is formed on an inner side than the driver circuit region.

[0017]

In the above structure, the light-emitting layer over the pixel electrode and an electrode over the light-emitting layer may be included.

[0018]

Further, in any of the above structures, the third interlayer insulating film is preferably one selected from a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

[0019]

Further, in any of the above structures, a semiconductor material included in a channel formation region of each of the first transistor and the second transistor is preferably an oxide semiconductor. In addition, the first transistor and the second transistor each preferably include a gate electrode, a semiconductor layer including an oxide semiconductor over the gate electrode, and a source electrode and a drain electrode over the semiconductor layer.

[0020]

One embodiment of the present invention includes, in its category, an electronic device including a display device having any of the above structures.

[0021]

Changes in the electrical characteristics of a display device including transistors in a pixel region and a driver circuit region can be suppressed, and the reliability of the display device can be improved. In particular, entry of hydrogen or moisture into the oxide semiconductor film in a display device using an oxide semiconductor film for a channel formation region of a transistor can be suppressed, changes in the electrical characteristics of the display device can be suppressed, and its reliability can be improved.

BRIEF DESCRIPTION OF DRAWINGS

[0022]

In the accompanying drawings:

FIGS. 1A to 1C illustrate top views of one mode of a display device;

FIG. 2 illustrates a cross section of one mode of a display device;

FIG. 3 illustrates a top view of one mode of a display device;

FIG. 4 illustrates a cross section of one mode of a display device;

FIGS. 5A and 5B illustrate a circuit diagram and a cross-sectional view of an example of a display device with an image sensor according to one embodiment of the present invention;

FIGS. 6A to 6C illustrate an example of a tablet terminal according to one embodiment of the present invention;

FIGS. 7A to 7C each illustrate an example of an electronic device according to one embodiment of the present invention;

FIG. 8 shows the ion intensity of released gas versus mass-to-charge ratio;

FIG. 9 shows the ion intensity versus substrate surface temperature for each mass-to-charge ratio;

FIG. 10 illustrates a cross-sectional image of an observed sample; and

FIGS. 11A and 11B illustrate electrical characteristics of samples.

BEST MODE FOR CARRYING OUT THE INVENTION

[0023]

Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the description below, and it is easily understood by those skilled in the art that modes and details disclosed herein can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention is not construed as being limited to description of the embodiments.

[0024]

In embodiments hereinafter described, the same components may be denoted by the same reference numerals throughout the drawings. Note that the thickness, the width, a relative position, and the like of components, namely, layers, regions, and the like illustrated in the drawings are exaggerated in some cases for clarification in the description of the embodiment.

[0025]

In this specification and the like, the term such as "electrode" or "wiring" does not limit a function of a component. For example, an "electrode" is sometimes used as part of a "wiring", and vice versa. Furthermore, the term “electrode” or “wiring” can include the case where a plurality of “electrodes” or “wirings” is formed in an integrated manner.

[0026]

Further, in this specification or the like, a silicon nitride oxide film is a film containing nitrogen, oxygen, and silicon as its components and containing more nitrogen than oxygen. Further, a silicon oxynitride film is a film containing oxygen, nitrogen, and silicon as its components and containing more oxygen than nitrogen.

[0027]

Functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flowing is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be used to denote the drain and the source, respectively, in this specification and the like.

[0028]

(Embodiment 1)

In this embodiment, a display device using a liquid crystal panel is described as one mode of a display device with reference to FIGS. 1A to 1C and FIG. 2.

[0029]

FIGS. 1A to 1C illustrate top views of the display device as one mode of a display device. Note that FIG. 1A, FIG. 1B, and FIG. 1C illustrate top views of the whole display device, part of a driver circuit portion of the display device, and part of a pixel region, respectively. In addition, FIG. 2 corresponds to a cross-sectional view taken along the line X1-Y1 in FIG. 1A.

[0030]

In the display device illustrated in FIG. 1A, a sealant 166 is provided so as to surround a pixel region 142, and gate driver circuit portions 140 and a source driver circuit portion 144, which are driver circuit regions that are located outside and adjacent to the pixel region 142 and supply signals to the pixel region 142, which are provided

over a first substrate 102; sealing is performed with a second substrate 152. The second substrate 152 is provided so as to face the first substrate 102 where the pixel region 142, the gate driver circuit portions 140, and the source driver circuit portion 144 are provided. Thus, the pixel region 142, the gate driver circuit portions 140, and the source driver circuit portion 144 are sealed together with a display element by the first substrate 102, the sealant 166, and the second substrate 152.

[0031]

In FIG. 1A, a flexible printed circuit (FPC) terminal portion 146 which is electrically connected to the pixel region 142, the gate driver circuit portions 140, and the source driver circuit portion 144 is provided in a region that is different from the region surrounded by the sealant 166, over the first substrate 102. An FPC 148 is connected to the FPC terminal portion 146. Signals and potentials applied to the pixel region 142, the gate driver circuit portions 140, and the source driver circuit portion 144 are supplied through the FPC 148.

[0032]

Although an example in which the gate driver circuit portions 140 and the source driver circuit portion 144 are formed over the first substrate 102 where the pixel region 142 is formed is shown in FIG. 1A, this structure does not limit the present invention. For example, only the gate driver circuit portions 140 may be formed over the first substrate 102 so that an additionally provided substrate where a source driver circuit is formed (e.g., a driver circuit substrate formed using a single crystal semiconductor film or a polycrystalline semiconductor film) is mounted on the first substrate 102.

[0033]

Although a structure in which the two gate driver circuit portions 140 are placed on both sides of the pixel region 142 is exemplified in FIG. 1A, this structure does not limit the present invention. For example, a gate driver circuit portion 140 may be placed on only one side of the pixel region 142.

[0034]

There is no particular limitation on a method of connecting the additionally provided driver circuit substrate; a chip on glass (COG) method, a wire bonding method, a tape automated bonding (TAB) method, or the like can be used. In addition, the

display device includes a panel in which a display element is sealed and a module in which an IC and the like including a controller are mounted on the panel.

[0035]

As described above, some or all of the driver circuits which include transistors can be formed over the first substrate 102 where the pixel region 142 is formed, so that a system-on-panel can be obtained.

[0036]

In FIG. 1C, a first transistor 101 and a capacitor 107 are formed in the pixel region 142. In the first transistor 101, a gate electrode 104, a source electrode 110, and a drain electrode 112 are electrically connected to a semiconductor layer 108. Although not illustrated in the plan view in FIG. 1C, over the first transistor 101, a first interlayer insulating film formed using an inorganic insulating material, a second interlayer insulating film formed using an organic insulating material over the first interlayer insulating film, and a third interlayer insulating film formed using an inorganic insulating material over the second interlayer insulating film are formed. The capacitor 107 includes a capacitor electrode 118, the third interlayer insulating film formed over the capacitor electrode 118, and a pixel electrode 122 formed over the third interlayer insulating film.

[0037]

In FIG. 1B, a second transistor 103 and a third transistor 105 are formed in the gate driver circuit portion 140 which is a driver circuit region. In each of the transistors in the gate driver circuit portion 140, the gate electrode 104, the source electrode 110, and the drain electrode 112 are electrically connected to the semiconductor layer 108. In the gate driver circuit portion 140, a gate line including the gate electrode 104 extends in the horizontal direction, a source line including the source electrode 110 extends in the vertical direction, and a drain line including the drain electrode 112 extends in the vertical direction with a distance from the source electrode.

[0038]

The gate driver circuit portion 140 including the second transistor 103 and the third transistor 105 can supply a signal to the first transistor 101 included in each pixel of the pixel region 142.

[0039]

To control various signals, raise a voltage, and the like, the second transistor 103 and the third transistor 105 in the gate driver circuit portion 140 require a relatively high voltage, specifically a voltage of about 10 V to 30 V. In contrast, the first transistor 101 in the pixel region 142 is used only for switching of a pixel and therefore can be driven at a voltage of about several volts to 20 volts. Thus, a stress applied to the second transistor 103 and the third transistor 105 in the gate driver circuit portion 140 is much larger than a stress applied to the first transistor 101 in the pixel region 142.

[0040]

To specifically describe a structure of the display device illustrated in FIGS. 1A to 1C, structures of the gate driver circuit portion 140 and the pixel region 142 are described below using FIG. 2 corresponding to a cross-sectional view along the line X1-Y1 in FIGS. 1A to 1C.

[0041]

In the pixel region 142, the first transistor 101 is formed with the first substrate 102, the gate electrode 104 formed over the first substrate 102, a gate insulating film 106 formed over the gate electrode 104, the semiconductor layer 108 which is in contact with the gate insulating film 106 and provided to overlap with the gate electrode 104, the source electrode 110 and the drain electrode 112 formed over the gate insulating film 106 and the semiconductor layer 108.

[0042]

In addition, the pixel region 142 includes a first interlayer insulating film 114 formed using an inorganic insulating material over the first transistor 101, specifically over the gate insulating film 106, the semiconductor layer 108, the source electrode 110, and the drain electrode 112, a second interlayer insulating film 116 formed using an organic insulating material over the first interlayer insulating film 114, the capacitor electrode 118 formed over the second interlayer insulating film 116, a third interlayer insulating film 120 formed using an inorganic insulating material over the second interlayer insulating film 116 and the capacitor electrode 118, and the pixel electrode 122 formed over the third interlayer insulating film 120.

[0043]

Note that the capacitor 107 is formed with the capacitor electrode 118, the third

interlayer insulating film 120, and the pixel electrode 122. The capacitor electrode 118, the third interlayer insulating film 120, and the pixel electrode 122 are preferably formed using a material having the property of transmitting visible light, in which case large capacitance can be ensured without reducing the aperture ratio of the pixel region.

[0044]

The pixel region 142 includes, over the pixel electrode 122, a first alignment film 124, a liquid crystal layer 162 provided over the first alignment film 124, a second alignment film 164 provided over the liquid crystal layer 162, a counter electrode 158 provided over the second alignment film 164, an organic protective insulating film 156 provided over the counter electrode 158, a colored film 153 and a light-blocking film 154 which are provided over the organic protective insulating film 156, and the second substrate 152 provided over the colored film 153 and the light-blocking film 154.

[0045]

Note that a liquid crystal element 150 which is a display element is formed with the pixel electrode 122, the first alignment film 124, the liquid crystal layer 162, the second alignment film 164, and the counter electrode 158.

[0046]

In the gate driver circuit portion 140, the second transistor 103 and the third transistor 105 are formed with the first substrate 102, the gate electrode 104 formed over the first substrate 102, the gate insulating film 106 formed over the gate electrode 104, the semiconductor layer 108 which is in contact with the gate insulating film 106 and provided to overlap with the gate electrode 104, the source electrode 110 and the drain electrode 112 formed over the gate insulating film 106 and the semiconductor layer 108.

[0047]

In addition, the gate driver circuit portion 140 includes the first interlayer insulating film 114 formed over the second transistor 103 and the third transistor 105, specifically over the gate insulating film 106, the semiconductor layer 108, the source electrode 110, and the drain electrode 112, and the second interlayer insulating film 116 formed over the first interlayer insulating film 114.

[0048]

Thus, the third interlayer insulating film 120 is provided in part of an upper

region of the pixel region 142, and an edge portion of the third interlayer insulating film 120 is formed on an inner side than the gate driver circuit portion 140 which is a driver circuit region.

[0049]

The above-described structure allows moisture taken in from the outside or a gas of moisture, hydrogen, or the like generated in the display device to be released to a portion above the second interlayer insulating film 116 of the gate driver circuit portion 140. Accordingly, it is possible to suppress incorporation of a gas of moisture, hydrogen, or the like into the first transistor 101, the second transistor 103, and the third transistor 105.

[0050]

For the second interlayer insulating film 116 formed using an organic insulating material, an organic insulating material with which the planarity is improved is needed so that unevenness of the transistors included in the display device or the like is reduced. This is because the reduction in the unevenness of the transistors or the like leads to an improvement of the display quality of the display device. However, when heating or the like is performed, the organic insulating material releases hydrogen, moisture, or an organic component as a gas.

[0051]

The above-mentioned gas of hydrogen, moisture, or an organic component is unlikely to be a great problem for a transistor using a silicon film, which is a silicon-based semiconductor material, in the semiconductor layer 108, for example. However, in one embodiment of the present invention, the semiconductor layer 108 is formed using an oxide semiconductor film, and hence the gas from the second interlayer insulating film 116 formed using an organic insulating material needs to be suitably released. Note that, when the semiconductor layer 108 is formed using an oxide semiconductor film, the structure in which an edge portion of the third interlayer insulating film 120 is formed on an inner side than the gate driver circuit portion 140 which is a driver circuit region has an excellent effect. Further, a similar effect can also be obtained in a transistor with the semiconductor layer 108 formed using a material (e.g., amorphous silicon or crystalline silicon which is a silicon-based semiconductor material) other than an oxide semiconductor.

[0052]

In this embodiment, the third interlayer insulating film 120 formed using an inorganic insulating material over the second interlayer insulating film 116 formed using an organic insulating material is used as a dielectric of the capacitor 107. Further, the third interlayer insulating film 120 formed using an inorganic insulating material can suppress entry of hydrogen, moisture, or the like into the second interlayer insulating film 116 from the outside.

[0053]

However, if the third interlayer insulating film 120 is formed over the second interlayer insulating film 116 over the second transistor 103 and the third transistor 105 which are used for the gate driver circuit portion 140, the gas released from the organic insulating material in the second interlayer insulating film 116 cannot be dispersed into the outside and enters the second transistor 103 and the third transistor 105.

[0054]

When the above-described gas released from the organic insulating material enters the oxide semiconductor used in the semiconductor layer 108 of the transistors, the gas is taken in as an impurity into the oxide semiconductor film. This changes characteristics of the transistors using the semiconductor layer 108.

[0055]

In contrast, in the structure as illustrated in FIG. 2 where the third interlayer insulating film 120 is holed over the second transistor 103 and the third transistor 105 which are used for the gate driver circuit portion 140, that is, the third interlayer insulating film 120 is provided in part of the pixel region 142 and an edge portion of the third interlayer insulating film 120 is formed on an inner side than the gate driver circuit portion 140, the gas released from the second interlayer insulating film 116 can be dispersed into the outside.

[0056]

Also in the first transistor 101 used for the pixel region 142, as illustrated in FIG. 2, it is preferable to remove a portion of the third interlayer insulating film 120 formed using an inorganic insulating material, which overlaps with the semiconductor layer 108. Such a structure can suppress entry of the gas released from the second interlayer insulating film 116 formed using an organic insulating material into the first

transistor 101.

[0057]

Here, other components of the display device illustrated in FIGS. 1A to 1C and FIG. 2 are detailed below.

[0058]

For the first substrate 102 and the second substrate 152, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used. In the mass production, for the first substrate 102 and the second substrate 152, a mother glass with any of the following sizes is preferably used: the 8-th generation (2160 mm × 2460 mm), the 9-th generation (2400 mm × 2800 mm, or 2450 mm × 3050 mm), the 10-th generation (2950 mm × 3400 mm), and the like. High process temperature and a long period of process time drastically shrink the mother glass. Hence, in the case where mass production is performed with the use of the mother glass, it is preferable that the heat process in the manufacturing process be preferably performed at a temperature lower than or equal to 600 °C, further preferably lower than or equal to 450 °C, still further preferably lower than or equal to 350 °C.

[0059]

Note that a base insulating film may be provided between the first substrate 102 and the gate electrode 104. As the base insulating film, a silicon oxide film, a silicon oxynitride film, a silicon nitride film, a silicon nitride oxide film, a gallium oxide film, a hafnium oxide film, an yttrium oxide film, an aluminum oxide film, an aluminum oxynitride film, and the like can be given as examples. Note that when a silicon nitride film, a gallium oxide film, a hafnium oxide film, an yttrium oxide film, an aluminum oxide film, or the like is used as the base insulating film, it is possible to suppress entry of impurities such as an alkali metal, water, and hydrogen from the first substrate 102 into the oxide semiconductor layer 108.

[0060]

For the gate electrode 104, a metal element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten, an alloy containing any of these metal elements as a component, an alloy containing these metal elements in combination, or the like can be used. One or both of the metal elements of manganese

and zirconium may be used. Further, the gate electrode 104 may have a single-layer structure or a stacked-layer structure of two or more layers. A single-layer structure of an aluminum film containing silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a two-layer structure in which a titanium film is stacked over a titanium nitride film, a two-layer structure in which a tungsten film is stacked over a titanium nitride film, a two-layer structure in which a tungsten film is stacked over a tantalum nitride film or a tungsten nitride film, a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order, and the like can be given as examples. Alternatively, a film, an alloy film, or a nitride film which contains aluminum and one or more elements selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium may be used.

[0061]

The gate electrode 104 can also be formed using a light-transmitting conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added. It is also possible to use a stacked-layer structure formed using the above light-transmitting conductive material and the above metal element.

[0062]

Further, between the gate electrode 104 and the gate insulating film 106, an In-Ga-Zn-based oxynitride semiconductor film, an In-Sn-based oxynitride semiconductor film, an In-Ga-based oxynitride semiconductor film, an In-Zn-based oxynitride semiconductor film, a Sn-based oxynitride semiconductor film, an In-based oxynitride semiconductor film, a film of a metal nitride (such as InN or ZnN), or the like may be provided. These films each have a work function higher than or equal to 5 eV, preferably higher than or equal to 5.5 eV, which is higher than the electron affinity of the oxide semiconductor. Hence, the threshold voltage of the transistor using the oxide semiconductor can be shifted in the positive direction, and a so-called normally-off switching element can be achieved. For example, as an In-Ga-Zn-based oxynitride semiconductor film, an In-Ga-Zn-based oxynitride semiconductor film having a higher nitrogen concentration than at least the semiconductor layer 108, specifically an In-Ga-Zn-based oxynitride semiconductor film having a nitrogen

concentration higher than or equal to 7 at.%, is used.

[0063]

As the gate insulating film 106, a single layer or a stacked layer of, for example, a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, a Ga-Zn-based metal oxide film, or the like can be provided. To improve the properties of the interface with the semiconductor layer 108, at least a region of the gate insulating film 106, which is in contact with the semiconductor layer 108, is preferably formed with an oxide insulating film.

[0064]

Further, by providing an insulating film having a blocking effect against oxygen, hydrogen, water, and the like over the gate insulating film 106, it is possible to prevent outward diffusion of oxygen from the semiconductor layer 108 and entry of hydrogen, water, or the like into the semiconductor layer 108 from the outside. For the insulating film having a blocking effect against oxygen, hydrogen, water, and the like, an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, a gallium oxynitride film, an yttrium oxide film, an yttrium oxynitride film, a hafnium oxide film, and a hafnium oxynitride film can be given as examples.

[0065]

The gate insulating film 106 can be formed as a gate insulating film which has few defects and releases less hydrogen and less ammonia, when formed to have a stacked structure in which a silicon nitride film having few defects is used as a first silicon nitride film, a silicon nitride film which releases less hydrogen and less ammonia is provided as a second silicon nitride film over the first silicon nitride film, and an oxide insulating film is provided over the second silicon nitride film. Thus, transfer of hydrogen and nitrogen, which are contained in the gate insulating film 106, to the semiconductor layer 108 can be suppressed.

[0066]

The use of a silicon nitride film as the gate insulating film 106 has the following effect. As compared with a silicon oxide film, a silicon nitride film has a high dielectric constant and needs a large thickness to obtain an equivalent capacitance. Thus, the physical thickness of the gate insulating film can be increased. Accordingly,

a reduction in the withstand voltages of the first transistor 101, the second transistor 103, and the third transistor 105 is suppressed and the withstand voltages are improved, so that an electrostatic breakdown of the transistors used for the display device can be suppressed.

[0067]

Further, in the case where copper is used for the gate electrode 104 and a silicon nitride film is used as the gate insulating film 106 in contact with the gate electrode 104, the number of the ammonia molecules released from the silicon nitride film by heating is preferably reduced as much as possible so that reaction between copper and the ammonia molecules can be suppressed.

[0068]

In the transistor using an oxide semiconductor film for the semiconductor layer 108, the trap level (also referred to as interface level) at the interface between the oxide semiconductor film and the gate insulating film or in the gate insulating film shifts the threshold voltage of the transistor typically in the negative direction, and increases the subthreshold swing (S value), which refers to a gate voltage needed for changing the drain current by an order of magnitude when the transistor is turned on. This results in the problem of variation in the electrical characteristics among transistors. Therefore, with the use of a silicon nitride film having few defects as the gate insulating film, the shift of the threshold voltage in the negative direction and the variation in the electrical characteristics among transistors can be reduced.

[0069]

The gate insulating film 106 may be formed using a high-k material such as hafnium silicate ($HfSiO_x$), hafnium silicate to which nitrogen is added ($HfSi_xO_yN_z$), hafnium aluminate to which nitrogen is added ($HfAl_xO_yN_z$), hafnium oxide, or yttrium oxide, so that gate leakage of the transistor can be reduced.

[0070]

The thickness of the gate insulating film 106 is preferably greater than or equal to 5 nm and less than or equal to 400 nm, more preferably greater than or equal to 10 nm and less than or equal to 300 nm, still more preferably greater than or equal to 50 nm and less than or equal to 250 nm.

[0071]

An oxide semiconductor is used for the semiconductor layer 108, which preferably contains at least indium (In) or zinc (Zn) or both In and Zn. In order to reduce variation in the electrical characteristics among the transistors using the oxide semiconductor, the oxide semiconductor preferably contains one or more of stabilizers in addition to In or Zn.

[0072]

Examples of the stabilizer are gallium (Ga), tin (Sn), hafnium (Hf), aluminum (Al), zirconium (Zr), and the like. Another examples of the stabilizer are lanthanoids such as lanthanum (La), cerium (Ce), praseodymium (Pr), neodymium (Nd), samarium (Sm), europium (Eu), gadolinium (Gd), terbium (Tb), dysprosium (Dy), holmium (Ho), erbium (Er), thulium (Tm), ytterbium (Yb), and lutetium (Lu).

[0073]

As the oxide semiconductor, for example, any of the following can be used: indium oxide, tin oxide, zinc oxide, an In-Zn-based metal oxide, a Sn-Zn-based metal oxide, an Al-Zn-based metal oxide, a Zn-Mg-based metal oxide, a Sn-Mg-based metal oxide, an In-Mg-based metal oxide, an In-Ga-based metal oxide, an In-W-based metal oxide, an In-Ga-Zn-based metal oxide (also referred to as IGZO), an In-Al-Zn-based metal oxide, an In-Sn-Zn-based metal oxide, a Sn-Ga-Zn-based metal oxide, an Al-Ga-Zn-based metal oxide, a Sn-Al-Zn-based metal oxide, an In-Hf-Zn-based metal oxide, an In-La-Zn-based metal oxide, an In-Ce-Zn-based metal oxide, an In-Pr-Zn-based metal oxide, an In-Nd-Zn-based metal oxide, an In-Sm-Zn-based metal oxide, an In-Eu-Zn-based metal oxide, an In-Gd-Zn-based metal oxide, an In-Tb-Zn-based metal oxide, an In-Dy-Zn-based metal oxide, an In-Ho-Zn-based metal oxide, an In-Er-Zn-based metal oxide, an In-Tm-Zn-based metal oxide, an In-Yb-Zn-based metal oxide, an In-Lu-Zn-based metal oxide, an In-Sn-Ga-Zn-based metal oxide, an In-Hf-Ga-Zn-based metal oxide, an In-Al-Ga-Zn-based metal oxide, an In-Sn-Al-Zn-based metal oxide, an In-Sn-Hf-Zn-based metal oxide, and an In-Hf-Al-Zn-based metal oxide.

[0074]

Note that, for example, an In-Ga-Zn-based metal oxide means an oxide containing In, Ga, and Zn as its main components and there is no particular limitation on the ratio of In to Ga and Zn. The In-Ga-Zn-based metal oxide may contain a metal

element other than In, Ga, and Zn.

[0075]

Alternatively, a material represented by $InMO_3(ZnO)_m$ (m is larger than 0 and not an integer) may be used as the oxide semiconductor. Note that M represents one or more metal elements selected from Ga, Fe, Mn, and Co. Alternatively, as the oxide semiconductor, a material represented by $In_2SnO_5(ZnO)_n$ (n is an integer greater than 0) may be used.

[0076]

For example, it is possible to use an In-Ga-Zn-based metal oxide containing In, Ga, and Zn at an atomic ratio of 1:1:1 (= 1/3:1/3:1/3), 2:2:1 (= 2/5:2/5:1/5), or 3:1:2 (= 1/2:1/6:1/3), or any of oxides whose composition is in the neighborhood of the above compositions. Alternatively, an In-Sn-Zn-based metal oxide containing In, Sn, and Zn at an atomic ratio of 1:1:1 (= 1/3:1/3:1/3), 2:1:3 (= 1/3:1/6:1/2), or 2:1:5 (= 1/4:1/8:5/8) may be used. Note that the proportion of each atom in the atomic ratio of the oxide semiconductor film may vary within a range of ±20 % as an error.

[0077]

However, the composition is not limited to those described above, and a material having the appropriate composition may be used depending on required semiconductor characteristics and electrical characteristics (e.g., field-effect mobility, threshold voltage, and variation). In order to obtain required semiconductor characteristics, it is preferable that the carrier density, the impurity concentration, the defect density, the atomic ratio of a metal element to oxygen, the interatomic distance, the density, and the like be set appropriate.

[0078]

For example, high mobility can be obtained relatively easily in the case where an In-Sn-Zn-based metal oxide is used. Also in the case where an In-Ga-Zn-based metal oxide is used, the field-effect mobility can be increased by reducing the defect density in a bulk.

[0079]

Further, the energy gap of a metal oxide that can be used for the semiconductor layer 108 is greater than or equal to 2 eV, preferably greater than or equal to 2.5 eV,

more preferably greater than or equal to 3 eV. With the oxide semiconductor film having such a wide energy gap, the off-state current of the transistor can be reduced.

[0080]

Next, a structure of the oxide semiconductor film that can be used as the semiconductor layer 108 is described below.

[0081]

An oxide semiconductor film is roughly classified into a non-single-crystal oxide semiconductor film and a single-crystal oxide semiconductor film. The non-single-crystal oxide semiconductor film includes any of a c-axis aligned crystalline oxide semiconductor (CAAC-OS) film, a polycrystalline oxide semiconductor film, a microcrystalline oxide semiconductor film, an amorphous oxide semiconductor film, and the like.

[0082]

Here, the CAAC-OS film is described.

[0083]

The CAAC-OS film is one of oxide semiconductor films including a plurality of crystal parts, and most of each crystal part fits inside a cube whose one side is less than 100 nm. Thus, there is a case where a crystal part included in the CAAC-OS film fits a cube whose one side is less than 10 nm, less than 5 nm, or less than 3 nm.

[0084]

In a transmission electron microscope (TEM) image of the CAAC-OS film, a boundary between crystal parts, that is, a grain boundary is not clearly confirmed. Thus, in the CAAC-OS film, a reduction in electron mobility due to the grain boundary is less likely to occur.

[0085]

According to the TEM image of the CAAC-OS film observed in a direction substantially parallel to a sample surface (cross-sectional TEM image), metal atoms are arranged in a layered manner in the crystal parts. Each metal atom layer has a morphology reflected by a surface over which the CAAC-OS film is formed (hereinafter, a surface over which the CAAC-OS film is formed is referred to as a formation surface) or a top surface of the CAAC-OS film, and is arranged in parallel to the formation surface or the top surface of the CAAC-OS film.

[0086]

On the other hand, according to the TEM image of the CAAC-OS film observed in a direction substantially perpendicular to the sample surface (plan TEM image), metal atoms are arranged in a triangular or hexagonal configuration in the crystal parts. However, there is no regularity of arrangement of metal atoms between different crystal parts.

[0087]

In this specification, a term "parallel" indicates that the angle formed between two straight lines is greater than or equal to −10° and less than or equal to 10°, and accordingly also includes the case where the angle is greater than or equal to −5° and less than or equal to 5°. In addition, a term "perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100°, and accordingly includes the case where the angle is greater than or equal to 85° and less than or equal to 95°.

[0088]

From the results of the cross-sectional TEM image and the plan TEM image, alignment is found in the crystal parts in the CAAC-OS film.

[0089]

A CAAC-OS film is subjected to structural analysis with an X-ray diffraction (XRD) apparatus. For example, when the CAAC-OS film including an $InGaZnO_4$ crystal is analyzed by an out-of-plane method, a peak appears frequently when the diffraction angle (2θ) is around 31°. This peak is derived from the (009) plane of the $InGaZnO_4$ crystal, which indicates that crystals in the CAAC-OS film have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS film.

[0090]

On the other hand, when the CAAC-OS film is analyzed by an in-plane method in which an X-ray enters a sample in a direction perpendicular to the c-axis, a peak appears frequently when 2θ is around 56°. This peak is derived from the (110) plane of the $InGaZnO_4$ crystal. Here, analysis (ϕ scan) is performed under conditions where the sample is rotated around a normal vector of a sample surface as an axis (ϕ axis) with

2θ fixed at around 56°. In the case where the sample is a single-crystal oxide semiconductor film of $InGaZnO_4$, six peaks appear. The six peaks are derived from crystal planes equivalent to the (110) plane. On the other hand, in the case of a CAAC-OS film, a peak is not clearly observed even when ϕ scan is performed with 2θ fixed at around 56°.

[0091]

According to the above results, in the CAAC-OS film having c-axis alignment, while the directions of a-axes and b-axes are different between crystal parts, the c-axes are aligned in a direction parallel to a normal vector of a formation surface or a normal vector of a top surface. Thus, each metal atom layer arranged in a layered manner observed in the cross-sectional TEM image corresponds to a plane parallel to the a-b plane of the crystal.

[0092]

Note that the crystal part is formed concurrently with deposition of the CAAC-OS film or is formed through crystallization treatment such as heat treatment. As described above, the c-axis of the crystal is aligned in a direction parallel to a normal vector of a formation surface or a normal vector of a top surface of the CAAC-OS film. Thus, for example, in the case where a shape of the CAAC-OS film is changed by etching or the like, the c-axis might not be necessarily parallel to a normal vector of a formation surface or a normal vector of a top surface of the CAAC-OS film.

[0093]

Further, the degree of crystallinity in the CAAC-OS film is not necessarily uniform. For example, in the case where crystal growth leading to the CAAC-OS film occurs from the vicinity of the top surface of the film, the degree of the crystallinity in the vicinity of the top surface is higher than that in the vicinity of the formation surface in some cases. Further, when an impurity is added to the CAAC-OS film, the crystallinity in a region to which the impurity is added is changed, and the degree of crystallinity in the CAAC-OS film varies depends on regions.

[0094]

Note that when the CAAC-OS film with an $InGaZnO_4$ crystal is analyzed by an out-of-plane method, a peak of 2θ may also be observed at around 36°, in addition to

the peak of 2θ at around 31°. The peak of 2θ at around 36° is derived from the (311) plane of a $ZnGa_2O_4$ crystal; such a peak indicates that a $ZnGa_2O_4$ crystal is included in part of the CAAC-OS film including the $InGaZnO_4$ crystal. It is preferable that in the CAAC-OS film, a peak of 2θ appear at around 31° and a peak of 2θ do not appear at around 36°.

[0095]

The CAAC-OS film is an oxide semiconductor film having a low impurity concentration. The impurity is any of elements which are not the main components of the oxide semiconductor film and includes hydrogen, carbon, silicon, a transition metal element, and the like. In particular, an element (e.g., silicon) which has higher bonding strength with oxygen than a metal element included in the oxide semiconductor film causes disorder of atomic arrangement in the oxide semiconductor film because the element deprives the oxide semiconductor film of oxygen, thereby reducing crystallinity. Further, a heavy metal such as iron or nickel, argon, carbon dioxide, and the like have a large atomic radius (or molecular radius); therefore, when any of such elements is contained in the oxide semiconductor film, the element causes disorder of the atomic arrangement of the oxide semiconductor film, thereby reducing crystallinity. Note that the impurity contained in the oxide semiconductor film might become a carrier trap or a source of carriers.

[0096]

The CAAC-OS film is an oxide semiconductor film having a low density of defect states. For example, oxygen vacancies in the oxide semiconductor film serve as carrier traps or serve as carrier generation sources when hydrogen is captured therein.

[0097]

The state in which impurity concentration is low and density of defect states is low (few oxygen vacancies) is referred to as "highly purified intrinsic" or "substantially highly purified intrinsic". A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has few carrier generation sources, and thus has a low carrier density. Thus, a transistor using the oxide semiconductor film rarely has a negative threshold voltage (rarely has normally-on characteristics). A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has few

carrier traps. Accordingly, the transistor using the oxide semiconductor film little changes in electrical characteristics and high reliability. Note that charges trapped by the carrier traps in the oxide semiconductor film takes a long time to be released and may behave like fixed charges. Thus, the transistor using the oxide semiconductor film with a high impurity concentration and a high density of defect states has unstable electrical characteristics in some cases.

[0098]

In a transistor using the CAAC-OS film, change in electrical characteristics due to irradiation with visible light or ultraviolet light is small.

[0099]

For example, the CAAC-OS film is formed with a polycrystalline oxide semiconductor sputtering target by a sputtering method. When ions collide with the sputtering target, a crystal region included in the sputtering target may be separated from the target along an a-b plane, and a sputtered particle having a plane parallel to the a-b plane (a flat-plate-like sputtered particle or a pellet-like sputtered particle) may be separated from the target. In that case, the flat-plate-like sputtered particle reaches a substrate while keeping its crystal state, so that the CAAC-OS film can be formed over the substrate.

[0100]

For the formation of the CAAC-OS film, the following conditions are preferably used.

[0101]

By reducing the amount of impurities entering the CAAC-OS film during the deposition, the crystal state can be prevented from being broken by the impurities. For example, the concentration of impurities (e.g., hydrogen, water, carbon dioxide, or nitrogen) which exist in the deposition chamber may be reduced. Furthermore, the concentration of impurities in a deposition gas may be reduced. Specifically, a deposition gas whose dew point is –80 °C or lower, preferably –100 °C or lower is used.

[0102]

By increasing the substrate heating temperature during the deposition, migration of a sputtered particle occurs after the sputtered particle reaches the substrate.

Specifically, the substrate heating temperature during the deposition is 100 °C to 740 °C, preferably 150 °C to 500 °C. By increasing the substrate heating temperature during the deposition, when the flat-plate-like sputtered particle reaches the substrate, migration occurs on the substrate, so that a flat plane of the sputtered particle is attached to the substrate.

[0103]

Furthermore, it is preferable to reduce plasma damage during the deposition by increasing the proportion of oxygen in the deposition gas and optimizing power. The proportion of oxygen in the deposition gas is 30 vol% or higher, preferably 100 vol%.

[0104]

Alternatively, the oxide semiconductor film used as the semiconductor layer 108 may have a stacked-layer structure of a plurality of oxide semiconductor films. For example, the oxide semiconductor film may have a stacked-layer structure of a first oxide semiconductor film and a second oxide semiconductor film which are formed using metal oxides with different compositions. For example, the first oxide semiconductor film may be formed using any of a two-component metal oxide, a three-component metal oxide, and a four-component metal oxide, while the second oxide semiconductor film is formed using any of these which is different from the oxide for the first oxide semiconductor film.

[0105]

Further, the constituent elements of the first oxide semiconductor film and the second oxide semiconductor film may be made the same while the composition of the constituent elements of the first oxide semiconductor film and the second oxide semiconductor film is made different. For example, the first oxide semiconductor film may contain In, Ga, and Zn at an atomic ratio of 1:1:1, while the second oxide semiconductor film contains In, Ga, and Zn at an atomic ratio of 3:1:2. Alternatively, the first oxide semiconductor film may contain In, Ga, and Zn at an atomic ratio of 1:3:2, while the second oxide semiconductor film contains In, Ga, and Zn at an atomic ratio of 2:1:3. Note that the proportion of each atom in the atomic ratio of the oxide semiconductor film varies within a range of ±20 % as an error.

[0106]

At this time, one of the first oxide semiconductor film and the second oxide semiconductor film, which is closer to the gate electrode (on the channel side), preferably contains In and Ga such that In > Ga. The other oxide semiconductor film, which is farther from the gate electrode (on the back channel side), preferably contains In and Ga such that In ≤ Ga.

[0107]

Further, the oxide semiconductor film may have a three-layer structure of a first oxide semiconductor film, a second oxide semiconductor film, and a third oxide semiconductor film, in which the constituent elements thereof may be made the same, while the composition of the constituent elements of the first oxide semiconductor film, the second oxide semiconductor film, and the third oxide semiconductor film is made different. For example, the first oxide semiconductor film may contain In, Ga, and Zn at an atomic ratio of 1:3:2, the second oxide semiconductor film may contain In, Ga, and Zn at an atomic ratio of 3:1:2, and the third oxide semiconductor film may contain In, Ga, and Zn at an atomic ratio of 1:1:1.

[0108]

In an oxide semiconductor film which contains less In than Ga and Zn at an atomic ratio, typically, the first oxide semiconductor film containing In, Ga, and Zn at an atomic ratio of 1:3:2, generation of oxygen vacancies can be more inhibited than in an oxide semiconductor film containing more In than Ga and Zn at an atomic ratio, typically, the second oxide semiconductor film, and an oxide semiconductor film containing Ga, Zn, and In at the same atomic ratio, typically, the third oxide semiconductor film, and accordingly, an increase in carrier density can be suppressed. Further, when the first oxide semiconductor film containing In, Ga, and Zn at an atomic ratio of 1:3:2 has an amorphous structure, the second oxide semiconductor film is likely to be a CAAC-OS film.

[0109]

Since the constituent elements of the first oxide semiconductor film, the second oxide semiconductor film, and the third oxide semiconductor film are the same, the first oxide semiconductor film has fewer trap levels at the interface with the second oxide semiconductor film. Therefore, when the oxide semiconductor film has the above

structure, the amount of change in the threshold voltage of the transistor due to a change over time or photodegradation can be reduced.

[0110]

In an oxide semiconductor, the *s* orbital of heavy metal mainly contributes to carrier transfer, and when the In content in the oxide semiconductor is increased, overlap of the *s* orbitals is likely to be increased. Therefore, an oxide containing In and Ga such that In > Ga has higher carrier mobility than an oxide containing In and Ga such that In ≤ Ga. Further, in Ga, the formation energy of an oxygen vacancy is larger and thus an oxygen vacancy is less likely to occur, than in In; therefore, the oxide containing In and Ga such that In ≤ Ga has more stable characteristics than the oxide containing In and Ga such that In > Ga.

[0111]

By the use of an oxide semiconductor containing In and Ga such that In > Ga for the oxide semiconductor film on the channel side and an oxide semiconductor containing In and Ga such that In ≤ Ga for the oxide semiconductor film on the back channel side, the field-effect mobility and reliability of the transistor can be further improved.

[0112]

Further, the first oxide semiconductor film, the second oxide semiconductor film, and the third oxide semiconductor film may be formed using oxide semiconductors having different crystallinity. In other words, the oxide semiconductor films may be formed using appropriate combination of a single crystal oxide semiconductor, a polycrystalline oxide semiconductor, a microcrystalline oxide semiconductor, an amorphous oxide semiconductor, and a CAAC-OS. When an amorphous oxide semiconductor is applied to the first oxide semiconductor film or the second oxide semiconductor film, internal stress of the oxide semiconductor film or external stress is reduced, change in characteristics of the transistor is reduced, and reliability of the transistor can be further improved.

[0113]

The thickness of the oxide semiconductor film is preferably greater than or equal to 1 nm and less than or equal to 100 nm, more preferably greater than or equal to

1 nm and less than or equal to 30 nm, still more preferably greater than or equal to 1 nm and less than or equal to 50 nm, further preferably greater than or equal to 3 nm and less than or equal to 20 nm.

[0114]

The concentration of an alkali metal or an alkaline earth metal in the oxide semiconductor film used for the semiconductor layer 108, which is obtained by secondary ion mass spectrometry (SIMS), is preferably less than or equal to 1×10^{18} atoms/cm^3, more preferably less than or equal to 2×10^{16} atoms/cm^3. This is because, when alkali metals or alkaline earth metals are bonded to an oxide semiconductor, some of the alkali metals or the alkaline earth metals generate carriers to increase the off-state current of the transistor.

[0115]

Further, the hydrogen concentration in the oxide semiconductor film used for the semiconductor layer 108, which is obtained by secondary ion mass spectrometry, is lower than 5×10^{18} atoms/cm^3, preferably less than or equal to 1×10^{18} atoms/cm^3, more preferably less than or equal to 5×10^{17} atoms/cm^3, still more preferably less than or equal to 1×10^{16} atoms/cm^3.

[0116]

Hydrogen contained in the oxide semiconductor film reacts with oxygen bonded to a metal atom to produce water, and a defect is formed in a lattice from which oxygen is released (or a portion from which oxygen is removed). In addition, when part of hydrogen is bonded to oxygen, electrons serving as carriers are generated. Thus, by reducing impurities including hydrogen as much as possible in the step of forming the oxide semiconductor film, the hydrogen concentration in the oxide semiconductor film can be reduced. Hence, by using an oxide semiconductor film in which hydrogen is removed as much as possible in the channel region, a shift of the threshold voltage in the negative direction can be suppressed and variation in electrical characteristics can be reduced. Further, leakage current between a source and a drain of the transistor, typically off-state current, can be reduced.

[0117]

Furthermore, the nitrogen concentration in the oxide semiconductor film used

for the semiconductor layer 108 is set to be less than or equal to 5×10^{18} atoms/cm^3, which can suppress a shift of the threshold voltage in the negative direction and reduce variation in electrical characteristics.

[0118]

Note that various experiments can prove the low off-state current of a transistor using an oxide semiconductor film which is highly purified by removing hydrogen as much as possible for a channel region. For example, even a transistor with a channel width of 1×10^6 μm and a channel length of 10 μm can have an off-state current less than or equal to the measurement limit of a semiconductor parameter analyzer, that is, less than or equal to 1×10^{-13} A when the voltage (drain voltage) between a source electrode and a drain electrode ranges between 1 V and 10 V. In this case, it can be seen that the off-state current corresponding to a value obtained by dividing the off-state current by the channel width of the transistor is 100 zA/mm or less. In addition, a capacitor and a transistor were connected to each other and the off-state current was measured with a circuit in which charge flowing into or from the capacitor was controlled by the transistor. In the measurements, a highly purified oxide semiconductor film was used for a channel region of the transistor, and the off-state current of the transistor was measured from a change in the amount of charge of the capacitor per unit time. As a result, it was found that in the case where the voltage between the source electrode and the drain electrode of the transistor was 3 V, a lower off-state current of several tens of yoctoamperes per micrometer (yA/μm) was able to be obtained. Thus, the transistor whose channel region is formed using a highly purified oxide semiconductor film has a very low off-state current.

[0119]

The source electrode 110 and the drain electrode 112 are formed to have a single-layer structure or a stacked-layer structure including, as a conductive material, any of metals such as aluminum, titanium, chromium, nickel, copper, yttrium, zirconium, molybdenum, silver, tantalum, and tungsten or an alloy containing any of these metals as its main component. The following structures can be given as examples: a single-layer structure of an aluminum film containing silicon; a two-layer structure in which a titanium film is stacked over an aluminum film; a two-layer structure in which

a titanium film is stacked over a tungsten film; a two-layer structure in which a copper film is formed over a copper-magnesium-aluminum alloy film; a three-layer structure in which a titanium film or a titanium nitride film, an aluminum film or a copper film, and a titanium film or a titanium nitride film are stacked in this order; and a three-layer structure in which a molybdenum film or a molybdenum nitride film, an aluminum film or a copper film, and a molybdenum film or a molybdenum nitride film are stacked in this order; and the like. Note that a transparent conductive material containing indium oxide, tin oxide, or zinc oxide may be used.

[0120]

The source electrode 110 and the drain electrode 112 are provided over the semiconductor layer 108 in this embodiment but may be provided between the gate insulating film 106 and the semiconductor layer 108.

[0121]

As the first interlayer insulating film 114, an oxide insulating film is preferably used so as to improve characteristics of the interface with the oxide semiconductor film used for the semiconductor layer 108. As the first interlayer insulating film 114, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, a Ga-Zn-based metal oxide film, or the like having a thickness greater than or equal to 150 nm and less than or equal to 400 nm can be used. The first interlayer insulating film 114 may have a stacked-layer structure of an oxide insulating film and a nitride insulating film. For example, the first interlayer insulating film 114 can have a stacked-layer structure of a silicon oxynitride film and a silicon nitride film.

[0122]

For the second interlayer insulating film 116, an organic insulating material having heat resistance such as an acrylic-based resin, a polyimide-based resin, a benzocyclobutene-based resin, a polyamide-based resin, or an epoxy-based resin can be used. Note that the second interlayer insulating film 116 may be formed by stacking a plurality of insulating films formed using any of these materials. With the use of the second interlayer insulating film 116, the unevenness of the first transistor 101 and the like can be reduced.

[0123]

The capacitor electrode 118 can be formed using a light-transmitting conductive material such as indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium tin oxide (hereinafter referred to as ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added.

[0124]

As the third interlayer insulating film 120, an inorganic insulating material such as a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, or an aluminum oxide film can be used. In particular, one selected from a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film is preferably used as the third interlayer insulating film 120. By use of one selected from a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film as the third interlayer insulating film 120, release of hydrogen or moisture from the second interlayer insulating film 116 can be suppressed.

[0125]

As the pixel electrode 122, a material similar to that of the capacitor electrode 118 can be used. Although materials of the capacitor electrode 118 and the pixel electrode 122 may be the same or different, the use of the same materials is preferred, in which case manufacturing cost can be reduced.

[0126]

For the first alignment film 124 and the second alignment film 164, an organic material having heat resistance such as an acrylic-based resin, a polyimide-based resin, a benzocyclobutene-based resin, a polyamide-based resin, or an epoxy-based resin can be used.

[0127]

For the liquid crystal layer 162, a liquid crystal material such as thermotropic liquid crystal, low-molecular liquid crystal, high-molecular liquid crystal, polymer dispersed liquid crystal, ferroelectric liquid crystal, or anti-ferroelectric liquid crystal can be used. Such a liquid crystal material exhibits a cholesteric phase, a smectic phase, a cubic phase, a chiral nematic phase, an isotropic phase, or the like depending on conditions.

[0128]

Alternatively, in the case of employing a horizontal electric field mode, liquid crystal exhibiting a blue phase for which an alignment film (the first alignment film 124 or the second alignment film 164) is unnecessary may be used. A blue phase is one of liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase while temperature of cholesteric liquid crystal is increased. Since the blue phase appears only in a narrow temperature range, a liquid crystal composition in which several weight percent or more of a chiral material is mixed is used for the liquid crystal layer in order to improve the temperature range. The liquid crystal composition which includes liquid crystal exhibiting a blue phase and a chiral material has a short response time, and has optical isotropy, which makes the alignment process unneeded and the viewing angle dependence small. In addition, since an alignment film does not need to be provided and rubbing treatment is unnecessary, electrostatic discharge damage caused by the rubbing treatment can be prevented and defects and damage of the liquid crystal display device can be reduced in the manufacturing process. Thus, the liquid crystal display device can be manufactured with improved productivity. A transistor using an oxide semiconductor film has a possibility that the electrical characteristics of the transistor may be significantly changed by the influence of static electricity and deviate from the designed range. Therefore, it is more effective to use a liquid crystal material exhibiting a blue phase for a liquid crystal display device including a transistor using an oxide semiconductor film.

[0129]

The specific resistivity of the liquid crystal material is higher than or equal to 1×10^9 Ω·cm, preferably higher than or equal to 1×10^{11} Ω·cm, further preferably higher than or equal to 1×10^{12} Ω·cm. Note that the specific resistivity in this specification is measured at a temperature of 20 °C.

[0130]

The size of a storage capacitor formed in the display device is set considering the leakage current of the transistor provided in the pixel region or the like so that charge can be held for a predetermined period. The size of the storage capacitor can be set considering the off-state current of the transistor or the like. In the case where a transistor including an oxide semiconductor layer which is highly purified and in which

formation of an oxygen vacancy is inhibited is used and, for example, a liquid crystal element is used as the display element, a storage capacitor having a capacitance that is 1/3 or less, preferably 1/5 or less of the liquid crystal capacitance of each pixel is sufficient.

[0131]

It is possible to reduce the current in an off state (off-state current) of the transistor in this embodiment using the oxide semiconductor which is highly purified and in which formation of an oxygen vacancy is inhibited for the semiconductor layer. Accordingly, an electric signal such as an image signal can be held for a longer period, and a writing interval can be set longer in an on state. Thus, the frequency of refresh operation can be reduced, which leads to the effect of suppressing power consumption.

[0132]

As a driving mode of the liquid crystal element 150 in the display device illustrated in FIGS. 1A to 1C and FIG. 2, a twisted nematic (TN) mode, an in-plane-switching (IPS) mode, a fringe field switching (FFS) mode, an axially symmetric aligned micro-cell (ASM) mode, an optical compensated birefringence (OCB) mode, a ferroelectric liquid crystal (FLC) mode, an antiferroelectric liquid crystal (AFLC) mode, or the like can be used. In particular, an FFS mode is preferably used to achieve a wide viewing angle.

[0133]

The display device may be a normally black liquid crystal display device such as a transmissive liquid crystal display device utilizing a vertical alignment (VA) mode. Some examples are given as the vertical alignment mode. For example, a multi-domain vertical alignment (MVA) mode, a patterned vertical alignment (PVA) mode, and the like can be used. Moreover, it is possible to use a method called domain multiplication or multi-domain design, in which a pixel is divided into some regions (subpixels) and molecules are aligned in different directions in their respective regions.

[0134]

Although not illustrated in FIGS. 1A to 1C and FIG. 2, an optical member (optical substrate) such as a polarizing member, a retardation member, or an anti-reflection member, and the like may be provided as appropriate. For example, circular polarization may be obtained by using a polarizing substrate and a retardation

substrate. In addition, a backlight, a side light, or the like may be used as a light source.

[0135]

As a method for display in the pixel region 142, a progressive method, an interlace method, or the like can be employed. Further, color components controlled in a pixel at the time of color display are not limited to three colors: R, G, and B (R, G, and B correspond to red, green, and blue, respectively). For example, R, G, B, and W (W corresponds to white) or R, G, B, and one or more of yellow, cyan, magenta, and the like can be used. Note that the sizes of display regions may be different between respective dots of color components. Note that the disclosed invention is not limited to the application to a display device for color display; the disclosed invention can also be applied to a display device for monochrome display.

[0136]

Further, a spacer 160 is provided below the second substrate 152 so as to control the distance (cell gap) between the first substrate 102 and the second substrate 152. Note that the cell gap determines the thickness of the liquid crystal layer 162. The spacer 160 may have any shape, like a columnar spacer or a spherical spacer obtained by selective etching of an insulating film, or the like.

[0137]

The colored film 153 functions as a so-called color filter. For the colored film 153, a material having the property of transmitting light in a specific wavelength band is used, and an organic resin film including a dye or a pigment, or the like can be used.

[0138]

The light-blocking film 154 functions as a so-called black matrix. As the light-blocking film 154, as long as it can block light emitted from adjacent pixels, any film such as a metal film or an organic resin film including a black dye or a black pigment can be used. In this embodiment, the light-blocking film 154 formed of an organic resin film including a black pigment is exemplified.

[0139]

The organic protective insulating film 156 is provided so that an ionic substance included in the colored film 153 is not dispersed into the liquid crystal layer 162. However, the organic protective insulating film 156 is not limited to this

structure and not necessarily provided.

[0140]

As the sealant 166, a thermosetting resin, an ultraviolet curable resin, or the like can be used. A region sealed by the sealant 166 illustrated in FIG. 2 has a structure in which the gate insulating film 106, an electrode 113 formed in the same step as the source electrode 110 and the drain electrode 112, the first interlayer insulating film 114, and the second interlayer insulating film 116 are provided between the first substrate 102 and the second substrate 152; however, this structure is an example and does not limit the present invention. For example, the structure may be a structure in which only the gate insulating film 106 and the first interlayer insulating film 114 are provided. Entry of moisture or the like from the outside is more prevented when the second interlayer insulating film 116 is removed, and therefore, part of the second interlayer insulating film 116 is preferably removed or recessed as illustrated in FIG. 2.

[0141]

As described above, the display device described in this embodiment includes the transistors formed in the pixel region and the driver circuit region, the first interlayer insulating film formed over the transistors, the second interlayer insulating film formed over the first interlayer insulating film, and the third interlayer insulating film formed over the second interlayer insulating film. In this structure, the third interlayer insulating film is provided in part of an upper region of the pixel region, and an edge portion of the third interlayer insulating film is formed on an inner side than the driver circuit region. This structure can suppress entry of the gas released from the second interlayer insulating film into the transistor side, which can increase the reliability of the display device. Further, the first interlayer insulating film can suppress entry of the gas released from the second interlayer insulating film into the transistor side.

[0142]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments and examples.

[0143]

(Embodiment 2)

In this embodiment, a display device using an organic EL panel is described as one mode of a display device with reference to FIG. 3 and FIG. 4. Note that portions

that are similar to the portions in Embodiment 1 are denoted by the same reference numerals, and detailed description thereof is omitted.

[0144]

FIG. 3 and FIG. 4 illustrate a top view and a cross-sectional view, respectively, of the display device as one mode of a display device. Note that FIG. 4 corresponds to a cross-sectional view along the line X2-Y2 in FIG. 3.

[0145]

In the display device illustrated in FIG. 3, a sealant 166 is provided so as to surround a pixel region 142, and gate driver circuit portions 140 and a source driver circuit portion 144, which are driver circuit regions that are located outside and adjacent to the pixel region 142 and supply signals to the pixel region 142, which are provided over a first substrate 102; sealing is performed with a second substrate 152. The second substrate 152 is provided so as to face the first substrate 102 where the pixel region 142, the gate driver circuit portions 140, and the source driver circuit portion 144 are provided. Thus, the pixel region 142, the gate driver circuit portions 140, and the source driver circuit portion 144 are sealed together with a display element by the first substrate 102, the sealant 166, and the second substrate 152.

[0146]

As described above, some or all of the driver circuits which include transistors can be formed over the first substrate 102 where the pixel region 142 is formed, so that a system-on-panel can be obtained. Further, the whole or part of a driver circuit including a thin film transistor can be formed over the same substrate as a pixel region, so that a system-on-panel can be obtained.

[0147]

Next, structures of the pixel region 142 and the gate driver circuit portion 140 are detailed below using FIG. 4 corresponding to a cross-sectional view along the line X2-Y2 in FIG. 3.

[0148]

In the pixel region 142, the first transistor 101 is formed with the first substrate 102, the gate electrode 104 formed over the first substrate 102, a gate insulating film 106 formed over the gate electrode 104, the semiconductor layer 108 which is in contact with the gate insulating film 106 and provided to overlap with the gate electrode 104,

the source electrode 110 and the drain electrode 112 formed over the gate insulating film 106 and the semiconductor layer 108.

[0149]

In addition, the pixel region 142 includes the following: the first interlayer insulating film 114 formed using an inorganic insulating material over the first transistor 101, specifically over the gate insulating film 106, the semiconductor layer 108, the source electrode 110, and the drain electrode 112; the second interlayer insulating film 116 formed using an organic insulating material over the first interlayer insulating film 114; the third interlayer insulating film 120 formed using an inorganic insulating material over the second interlayer insulating film 116; a partition 126 formed over the second interlayer insulating film 116 and the third interlayer insulating film 120; the pixel electrode 122 formed over the third interlayer insulating film 120 and the partition 126; a light-emitting layer 128 formed over the pixel electrode 122; and an electrode 130 formed over the light-emitting layer 128.

[0150]

Note that the pixel electrode 122, the light-emitting layer 128, and the electrode 130 form a light-emitting element 170.

[0151]

In addition, a filler 172 is provided over the light-emitting element 170, specifically over the electrode 130. Over the filler 172, the second substrate 152 is provided. In other words, the light-emitting element 170 and the filler 172 are interposed between the first substrate 102 and the second substrate 152.

[0152]

In the gate driver circuit portion 140, the second transistor 103 and the third transistor 105 are formed with the first substrate 102, the gate electrode 104 formed over the first substrate 102, the gate insulating film 106 formed over the gate electrode 104, the semiconductor layer 108 which is in contact with the gate insulating film 106 and provided to overlap with the gate electrode 104, the source electrode 110 and the drain electrode 112 formed over the gate insulating film 106 and the semiconductor layer 108.

[0153]

In addition, the gate driver circuit portion 140 includes the first interlayer

insulating film 114 formed using an inorganic insulating material over the second transistor 103 and the third transistor 105, specifically over the gate insulating film 106, the semiconductor layer 108, the source electrode 110, and the drain electrode 112, and the second interlayer insulating film 116 formed using an organic insulating material over the first interlayer insulating film 114.

[0154]

Thus, the third interlayer insulating film 120 is provided in part of an upper region of the pixel region 142, and an edge portion of the third interlayer insulating film 120 is formed on an inner side than the gate driver circuit portion 140 which is a driver circuit region.

[0155]

The above-described structure allows moisture taken in from the outside or a gas of moisture, hydrogen, or the like generated in the display device to be released to a portion above the second interlayer insulating film 116 of the gate driver circuit portion 140. Accordingly, it is possible to suppress incorporation of a gas of moisture, hydrogen, or the like into the first transistor 101, the second transistor 103, and the third transistor 105.

[0156]

For the second interlayer insulating film 116 formed using an organic insulating material, an organic insulating material with which the planarity is improved is needed so that unevenness of the transistors included in the display device or the like is reduced. This is because the reduction in the unevenness of the transistors or the like leads to an improvement of the display quality of the display device. However, when heating or the like is performed, the organic insulating material releases hydrogen, moisture, or an organic component as a gas.

[0157]

The above-mentioned gas of hydrogen, moisture, or an organic component is unlikely to be a great problem for a transistor using a silicon film, which is a silicon-based semiconductor material, in the semiconductor layer 108, for example. However, in one embodiment of the present invention, the semiconductor layer 108 is formed using an oxide semiconductor film, and hence the gas from the second interlayer insulating film 116 formed using an organic insulating material needs to be suitably

released. Note that, when the semiconductor layer 108 is formed using an oxide semiconductor film, the structure in which an edge portion of the third interlayer insulating film 120 is formed on an inner side than the gate driver circuit portion 140 which is a driver circuit region has an excellent effect. Further, a similar effect can also be obtained in a transistor with the semiconductor layer 108 formed using a material (e.g., amorphous silicon or crystalline silicon which is a silicon-based semiconductor material) other than an oxide semiconductor.

[0158]

In this embodiment, the third interlayer insulating film 120 over the second interlayer insulating film 116 is formed in order to suppress entry of the gas released from the second interlayer insulating film 116 into the light-emitting element 170 side and/or to improve adhesion between the pixel electrode 122 and the second interlayer insulating film 116. Such a structure can suppress entry of the gas of hydrogen, moisture, or the like from the second interlayer insulating film 116 into the light-emitting element 170 side.

[0159]

However, if the third interlayer insulating film 120 is formed over the second interlayer insulating film 116 over the second transistor 103 and the third transistor 105 which are used for the gate driver circuit portion 140, the gas released from the organic insulating material in the second interlayer insulating film 116 cannot be dispersed into the outside and enters the second transistor 103 and the third transistor 105.

[0160]

When the above-described gas enters the oxide semiconductor used in the semiconductor layer 108 of the transistors, the gas is taken in as an impurity into the oxide semiconductor film. This changes characteristics of the transistors using the semiconductor layer 108.

[0161]

In contrast, in the structure as illustrated in FIG. 4 where the third interlayer insulating film 120 is holed over the second transistor 103 and the third transistor 105 which are used for the gate driver circuit portion 140, that is, the third interlayer insulating film 120 is provided in part of the pixel region 142 and an edge portion of the third interlayer insulating film 120 is formed on an inner side than the gate driver circuit

portion 140, the gas released from the second interlayer insulating film 116 can be dispersed into the outside.

[0162]

Also in the first transistor 101 used for the pixel region 142, as illustrated in FIG. 4, it is preferable to remove a portion of the third interlayer insulating film 120 formed using an inorganic insulating material, which overlaps with the semiconductor layer 108. Such a structure can suppress entry of the gas released from the second interlayer insulating film 116 formed using an organic insulating material into the first transistor 101.

[0163]

Here, other components of the display device illustrated in FIG. 3 and FIG. 4 which differ in structure from those in the display device described in Embodiment 1 are detailed below.

[0164]

The partition 126 is formed using an organic insulating material or an inorganic insulating material. It is particularly preferable that the partition 126 be formed using a photosensitive resin material to have an opening over the pixel electrode 122 so that a sidewall of the opening is formed as a tilted surface with continuous curvature.

[0165]

As the filler 172, an ultraviolet curable resin or a thermosetting resin can be used as well as an inert gas such as nitrogen or argon. For example, polyvinyl chloride (PVC), an acrylic-based resin, a polyimide-based resin, an epoxy-based resin, a silicone-based resin, polyvinyl butyral (PVB), or ethylene vinyl acetate (EVA) can be used. For example, nitrogen is used as the filler 172.

[0166]

As the light-emitting element 170, a light-emitting element utilizing electroluminescence can be used. Light-emitting elements utilizing electroluminescence are classified according to whether a light-emitting material is an organic compound or an inorganic compound. In general, the former is referred to as an organic EL element, and the latter is referred to as an inorganic EL element. Here, an organic EL element is used.

[0167]

In an organic EL element, by application of a voltage to a light-emitting element, electrons and holes are separately injected from a pair of electrodes (the pixel electrode 122 and the electrode 130) into a layer containing a light-emitting organic compound, and current flows. The carriers (electrons and holes) are recombined, and thus, the light-emitting organic compound is excited. The light-emitting organic compound returns to a ground state from the excited state, thereby emitting light. Owing to such a mechanism, this light-emitting element is referred to as a current-excitation light-emitting element.

[0168]

To extract light from the light-emitting element 170, at least one of the electrodes (the pixel electrode 122 or the electrode 130) has a light-transmitting property. The light-emitting element can employ any of the following emission structures: a top emission structure in which light emission is extracted through the surface opposite to the first substrate 102; a bottom emission structure in which light emission is extracted through the surface on the first substrate 102 side; or a dual emission structure in which light emission is extracted through the surface opposite to the first substrate 102 and the surface on the first substrate 102 side.

[0169]

A protective film may be formed over the electrode 130 and the partition 126 in order to prevent oxygen, hydrogen, moisture, carbon dioxide, or the like from entering the light-emitting element 170. As the protective film, a silicon nitride film, a silicon nitride oxide film, or the like can be formed. In addition, in a space which is formed with the first substrate 102, the second substrate 152, and the sealant 166, the filler 172 is provided for sealing. It is preferable that a panel be packaged (sealed) with a protective film (such as a laminate film or an ultraviolet curable resin film) or a cover material with high air-tightness and little degasification so that the panel is not exposed to the outside air, in this manner.

[0170]

In addition, if needed, an optical film, such as a polarizing plate, a circularly polarizing plate (including an elliptically polarizing plate), a retardation plate (a quarter-wave plate or a half-wave plate), or a color filter, may be provided as appropriate on a light-emitting surface of the light-emitting element 170. Further, the

polarizing plate or the circularly polarizing plate may be provided with an anti-reflection film. For example, anti-glare treatment by which reflected light can be diffused by projections and depressions on the surface so as to reduce the glare can be performed.

[0171]

For the light-emitting layer 128, it is preferable to use organic compounds including a guest material which is a light-emitting material converting triplet excitation energy to light emission and a host material the triplet excitation energy level (T_1 level) of which is higher than that of the guest material. Note that the light-emitting layer 128 may have a structure in which a plurality of light-emitting layers is stacked (so-called tandem structure) or a structure including a functional layer (e.g., a hole-injection layer, a hole-transport layer, an electron-transport layer, an electron-injection layer, or a charge generation layer) other than a light-emitting layer.

[0172]

For the sealant 166, a material containing a glass material, such as a glass body formed by melting and solidifying powder glass (also called frit glass), may be used in addition to any of the materials described in Embodiment 1. Such a material can effectively suppress permeation of moisture and gas. Hence, when the light-emitting element 170 is used as the display element, deterioration of the light-emitting element 170 can be suppressed, so that the display device can have very high reliability.

[0173]

A region sealed by the sealant 166 illustrated in FIG. 4 has a structure in which only the gate insulating film 106 is provided between the first substrate 102 and the second substrate 152; however, this structure is an example and does not limit the present invention. For example, the structure may be a structure in which the gate insulating film 106 and the first interlayer insulating film 114 are stacked. Note that in a preferred structure, the sealant 166 is placed in a region where the second interlayer insulating film 116 is removed, as illustrated in FIG. 4.

[0174]

As described above, the display device described in this embodiment includes the transistors formed in the pixel region and the driver circuit region, the first interlayer insulating film formed over the transistors, the second interlayer insulating film formed

over the first interlayer insulating film, and the third interlayer insulating film formed over the second interlayer insulating film. In this structure, the third interlayer insulating film is provided in part of an upper region of the pixel region, and an edge portion of the third interlayer insulating film is formed on an inner side than the driver circuit region. This structure can suppress entry of the gas released from the second interlayer insulating film into the transistor side, which can increase the reliability of the display device. Further, the first interlayer insulating film can suppress entry of the gas released from the second interlayer insulating film into the transistor side.

[0175]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments and examples.

[0176]

(Embodiment 3)

In this embodiment, an image sensor that can be used in combination with any of the display devices described in the above embodiments is described.

[0177]

An example of a display device with an image sensor is illustrated in FIG. 5A. FIG. 5A illustrates an equivalent circuit of a pixel of the display device with an image sensor.

[0178]

One electrode of a photodiode element 4002 is electrically connected to a reset signal line 4058, and the other electrode of the photodiode element 4002 is electrically connected to a gate electrode of a transistor 4040. One of a source electrode and a drain electrode of the transistor 4040 is electrically connected to a power supply potential (VDD), and the other of the source electrode and the drain electrode of the transistor 4040 is electrically connected to one of a source electrode and a drain electrode of a transistor 4056. A gate electrode of the transistor 4056 is electrically connected to a gate selection line 4057, and the other of the source electrode and the drain electrode of the transistor 4056 is electrically connected to an output signal line 4071.

[0179]

A first transistor 4030 is a transistor for pixel switching. One of a source

electrode and a drain electrode of the first transistor 4030 is electrically connected to a video signal line 4059, and the other of the source electrode and the drain electrode of the first transistor 4030 is electrically connected to a capacitor 4032 and a liquid crystal element 4034. A gate electrode of the first transistor 4030 is electrically connected to a gate line 4036.

[0180]

Note that structures of the first transistor 4030, the capacitor 4032, and the liquid crystal element 4034 can be similar to those in the display device described in Embodiment 1.

[0181]

FIG. 5B illustrates a cross section of part of a pixel of the display device with an image sensor and a cross section of a driver circuit portion. In a pixel region 5042, the photodiode element 4002 and the first transistor 4030 are provided over a first substrate 4001. In a gate driver circuit portion 5040 which is a driver circuit, a second transistor 4060 and a third transistor 4062 are provided over the first substrate 4001.

[0182]

Over the photodiode element 4002 and the first transistor 4030 in the pixel region 5042, a first interlayer insulating film 4014, a second interlayer insulating film 4016, and a third interlayer insulating film 4020 are formed. Over the second interlayer insulating film 4016, the capacitor 4032 using the third interlayer insulating film 4020 as a dielectric is formed.

[0183]

Thus, the third interlayer insulating film 4020 is provided in part of the pixel region 5042, and an edge portion of the third interlayer insulating film 4020 is formed on an inner side than the gate driver circuit portion 5040. By this structure, a gas released from the second interlayer insulating film 4016 can be dispersed into the outside. Thus, this structure can suppress entry of the gas released from the second interlayer insulating film 4016 into the transistor side, which can increase the reliability of the display device.

[0184]

In the photodiode element 4002, a lower electrode formed in the same step as the source electrode and the drain electrode of the first transistor 4030 and an upper

electrode formed in the same step as a pixel electrode of the liquid crystal element 4034 are included as a pair of electrodes, and a diode is present between the pair of electrodes.

[0185]

As a diode that can be used as the photodiode element 4002, a pn-type diode including a stack of a p-type semiconductor film and an n-type semiconductor film, a pin-type diode including a stack of a p-type semiconductor film, an i-type semiconductor film, and an n-type semiconductor film, a Schottky diode, or the like can be used.

[0186]

Over the photodiode element 4002, a first alignment film 4024, a liquid crystal layer 4096, a second alignment film 4084, a counter electrode 4088, an organic insulating film 4086, a colored film 4085, a second substrate 4052, and the like are provided.

[0187]

Note that a pin-type diode has better photoelectric conversion characteristics when the p-type semiconductor film side is used as a light-receiving plane. This is because the hole mobility is lower than the electron mobility. This embodiment shows an example in which light which enters the photodiode element 4002 from a surface of the second substrate 4052 through the colored film 4085, the liquid crystal layer 4096, and the like is converted into an electric signal, but this example does not limit the present invention. For example, the colored film 4085 may be omitted.

[0188]

The photodiode element 4002 described in this embodiment utilizes flow of current between the pair of electrodes which is caused by entry of light into the photodiode element 4002. When the photodiode element 4002 detects light, information of an object to be detected can be read.

[0189]

By performing, for example, a step of forming the transistor for the display device and a step for the image sensor at the same time, the productivity of the display device with the image sensor described in this embodiment can be increased. However, any of the display devices described in the above embodiments and the image sensor

described in this embodiment may be fabricated over different substrates. Specifically, the image sensor may be fabricated over the second substrate in any of the display devices described in the above embodiments.

[0190]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments and examples.

[0191]

(Embodiment 4)

In this embodiment, an example of a tablet terminal using a display device of one embodiment of the present invention is described.

[0192]

FIGS. 6A to 6C illustrate a foldable tablet terminal. FIG. 6A illustrates the tablet terminal which is unfolded. The tablet terminal includes a housing 8630, and a display portion 8631a, a display portion 8631b, a display mode switch 8034, a power switch 8035, a power-saving mode switch 8036, a clasp 8033, and an operation switch 8038 which are provided on the housing 8630.

[0193]

A display device of one embodiment of the present invention can be applied to the display portion 8631a and the display portion 8631b.

[0194]

The whole or part of the display portion 8631a can function as a touch panel and data can be input when a displayed operation key is touched. For example, the display portion 8631a can display keyboard buttons in the whole region to function as a touch panel, and the display portion 8631b may be used as a display screen.

[0195]

Like the display portion 8631a, the whole or part of the display portion 8631b can function as a touch panel.

[0196]

Further, a touch panel region of the display portion 8631a and a touch panel region of the display portion 8631b can be touched for input at the same time.

[0197]

With the display mode switch 8034, the display can be switched between a

portrait mode, a landscape mode, and the like, and between monochrome display and color display, for example. With the power-saving mode switch 8036, display luminance can be controlled in accordance with external light detected by an optical sensor incorporated in the tablet terminal. Note that in addition to the optical sensor, another detection device including a sensor such as a gyroscope or an acceleration sensor which is capable of detecting inclination may be included in the tablet terminal.

[0198]

Note that FIG. 6A shows an example in which the areas of the display portion 8631a and the display portion 8631b are the same; however, this example does not limit the present invention. The display portion 8631a and the display portion 8631b may differ in area or display quality. For example, one display panel may be capable of higher-definition display than the other display panel.

[0199]

The tablet terminal is closed in FIG. 6B. The tablet terminal includes the housing 8630, and a solar cell 8633 and a charge and discharge control circuit 8634 with which the housing 8630 is provided. In FIG. 6B, a structure including a battery 8635 and a DCDC converter 8636 is illustrated as an example of the charge and discharge control circuit 8634.

[0200]

Since the tablet terminal is foldable, the housing 8630 can be closed when the tablet terminal is not used. Thus, the display portion 8631a and the display portion 8631b can be protected, which leads to excellent durability and excellent reliability in terms of long-term use.

[0201]

The tablet terminal illustrated in FIGS. 6A to 6C can also have a function of displaying various kinds of data (e.g., a still image, a moving image, and a text image), a function of displaying a calendar, the date, the time, or the like on the display portion, a touch-input function of operating or editing data displayed on the display portion by touch input, a function of controlling processing by various kinds of software (programs), and the like.

[0202]

Electric power obtained with the solar cell 8633 can be used for the operation

of the tablet terminal or can be stored in the battery 8635. Note that the solar cell 8633 can be provided on both surfaces of the housing 8630. When a lithium ion battery is used as the battery 8635, there is an advantage of downsizing or the like.

[0203]

The structure and the operation of the charge and discharge control circuit 8634 illustrated in FIG. 6B are described with reference to a block diagram in FIG. 6C. In FIG. 6C, the solar cell 8633, the battery 8635, the DCDC converter 8636, a converter 8637, a switch SW1, a switch SW2, a switch SW3, and a display portion 8631 are illustrated. The battery 8635, the DCDC converter 8636, the converter 8637, and the switches SW1 to SW3 in FIG. 6C correspond to the charge and discharge control circuit 8634 illustrated in FIG. 6B.

[0204]

In the case where power is generated by the solar cell 8633, the voltage of the power generated by the solar cell is raised or lowered by the DCDC converter 8636 so that the power has a voltage for charging the battery 8635. Then, the switch SW1 is turned on and the voltage of the power is stepped up or down by the converter 8637 so as to be the most suitable voltage for the display portion 8631. In addition, when display on the display portion 8631 is not performed, the switch SW1 is turned off and the switch SW2 is turned on so that the battery 8635 is charged.

[0205]

Note that the solar cell 8633 is described as an example of a power generation means, but this does not limit the present invention. Another power generation means such as a piezoelectric element or a thermoelectric conversion element (Peltier element) may be used instead. For example, the battery may be charged with another charging means, such as a non-contact power transmission module which is capable of charging by transmitting and receiving power wirelessly (without contact), used in combination.

[0206]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments and examples.

[0207]

(Embodiment 5)

In this embodiment, examples of an electronic device including any of the

display devices described in the above embodiments or the like are described.

[0208]

FIG. 7A illustrates a portable information terminal. The portable information terminal illustrated in FIG. 7A includes a housing 9300, a button 9301, a microphone 9302, a display portion 9303, a speaker 9304, and a camera 9305, and has a function as a mobile phone. Any of the display devices and the display device with an image sensor described in the above embodiments can be applied to the display portion 9303.

[0209]

FIG. 7B illustrates a display. The display illustrated in FIG. 7B includes a housing 9310 and a display portion 9311. Any of the display devices and the display device with an image sensor which are described in the above embodiments can be applied to the display portion 9311.

[0210]

FIG. 7C illustrates a digital still camera. The digital still camera illustrated in FIG. 7C includes a housing 9320, a button 9321, a microphone 9322, and a display portion 9323. Any of the display devices and the display device with an image sensor described in the above embodiments can be applied to the display portion 9323.

[0211]

By application of one embodiment of the present invention, the reliability of the electronic devices can be increased.

[0212]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments and examples.

[Example 1]

[0213]

In this example, a released gas from an acrylic resin which is a typical example of the organic resin that can be used for a display device was examined.

[0214]

For a sample, an acrylic resin was applied onto a glass substrate, and heat treatment was performed in a nitrogen gas atmosphere at 250 °C for one hour. Note that the acrylic resin was formed so as to have a thickness of 1.5 μm after the heat

treatment.

[0215]

The released gas from the fabricated sample was measured by thermal desorption spectroscopy (TDS).

[0216]

FIG. 8 shows the ion intensity of the released gas versus mass-to-charge ratio (also referred to as M/z) at a substrate surface temperature of 250 °C. In FIG. 8, the horizontal axis represents mass-to-charge ratio and the vertical axis represents intensity (arbitrary unit). As shown in FIG. 8, a gas of an ion having a mass-to-charge ratio of 18 (an H_2O gas) which seems to be due to water, a gas of an ion having a mass-to-charge ratio of 28 (a C_2H_4 gas), a gas of an ion having a mass-to-charge ratio of 44 (a C_3H_8 gas), and a gas of an ion having a mass-to-charge ratio of 56 (a C_4H_8 gas), which seem to be due to hydrocarbon, were detected. Note that in the vicinities of the respective mass-to-charge ratios, fragment ions of gases were detected.

[0217]

FIG. 9 also shows the ion intensity versus substrate surface temperature for each mass-to-charge ratio (18, 28, 44, and 56). In FIG. 9, the horizontal axis represents substrate surface temperature (°C) and the vertical axis represents intensity (arbitrary unit). It was found that, in the case where the substrate surface temperature was in the range from 55 °C to 270 °C, the intensity of an ion having a mass-to-charge ratio of 18 which seems to be due to water had a peak in the range of greater than or equal to 55 °C and less than or equal to 100 °C and a peak in the range of greater than or equal to 150 °C and less than or equal to 270 °C. In contrast, it was found that the intensities of ions having mass-to-charge ratio of 28, 44, and 56 which seem to be due to hydrocarbon each had a peak in the range of greater than or equal to 150 °C and less than or equal to 270 °C.

[0218]

The above showed that water, hydrocarbon, and the like, which serve as impurities in the oxide semiconductor film, were released from the organic resin. In particular, water was found to be also released at a relatively low temperature greater than or equal to 55 °C and less than or equal to 100 °C. In other words, this indicated

that, when an impurity due to the organic resin reached the oxide semiconductor film, electrical characteristics of the transistor might deteriorate.

[0219]

The above also indicated that, when the organic resin was covered with a film that does not transmit a released gas of water, hydrocarbon, or the like (e.g. a silicon nitride film, a silicon nitride oxide film, or an aluminum oxide film), release of the gas from the organic resin increased pressure on the film that does not transmit a released gas of water, hydrocarbon, or the like, which might finally destroy the film that does not transmit a released gas of water, hydrocarbon, or the like and cause a shape defect of the transistor.

[Example 2]

[0220]

In this example, a transistor was fabricated and a cross-sectional shape and electrical characteristics thereof were estimated.

[0221]

In each sample, a bottom-gate top-contact transistor having a channel-etched structure in which an oxide semiconductor film is used is provided. The transistor includes a gate electrode provided over a glass substrate, a gate insulating film provided over the gate electrode, an oxide semiconductor film provided over the gate electrode with the gate insulating film interposed therebetween, and a pair of electrodes over and in contact with the oxide semiconductor film. Here, a tungsten film was used for the gate electrode, a silicon nitride film and a silicon oxynitride film thereover were used for the gate insulating film, and an In-Ga-Zn oxide film was used for the oxide semiconductor film. For each of the electrodes, a tungsten film, an aluminum film over the tungsten film, and a titanium film over the aluminum film were used.

[0222]

The protective insulating films (a 450-nm-thick silicon oxynitride film and a 50-nm-thick silicon nitride film thereover) are provided over each of the electrodes.

[0223]

In a sample of this example, a 2-μm-thick acrylic resin is provided over the protective insulating films, and a 200-nm-thick silicon nitride film is provided over the acrylic resin so as to expose part of a side surface of the acrylic resin. In a sample of a

comparison example, a 1.5-μm-thick acrylic resin is provided over the protective insulating films, and a 200-nm-thick silicon nitride film is provided over the acrylic resin so as to cover the acrylic resin.

[0224]

FIG. 10 shows a transmitted electron image (also referred to as a TE image) of a cross-sectional shape of an enlarged part of the sample of the comparison example, which was obtained by TEM. For the observation of the cross-sectional shape, an Ultra-thin Film Evaluation System HD-2300 manufactured by Hitachi High-Technologies Corporation was used. Note that in FIG. 10, only one of the electrodes is illustrated. It is found from the electrode and the protective insulating films provided so as to cover the electrode in FIG. 10 that in the protective films, cracks are generated from a step portion formed by the electrode. Since structures of the observed regions in the sample of this example and the sample of the comparison example are substantially the same, a cross-sectional shape of the sample of this example is not shown.

[0225]

Thus, the sample of this example has a structure in which a gas released from the acrylic resin is extracted to the outside of the sample, and the sample of the comparison example has a structure in which a gas released from the acrylic resin is not extracted to the outside of the sample. In other words, in the sample of the comparison example, the gas released from the acrylic resin is not extracted to the outside and enters the transistor through the crack generated in the protective insulating films.

[0226]

Next, gate voltage (Vg)-drain current (Id) characteristics which are electrical characteristics of the transistors of the samples were measured. The Vg-Id characteristics were measured using the transistors each having a channel length of 3 μm and a channel width of 3 μm. Note that in the measurements of the Vg-Id characteristics, the drain voltage (Vd) was set to 1 V or 10 V and the gate voltage (Vg) was swept from –20 V to 15 V.

[0227]

FIGS. 11A and 11B show the Vg-Id characteristics of the samples. The Vg-Id

characteristics of 20 transistors over a 600 mm by 720 mm glass substrate were measured as uniformly as possible. FIG. 11A shows the Vg-Id characteristics and field-effect mobility of the transistors of the sample of this example, and FIG. 11B shows the Vg-Id characteristics of the transistors of the sample of the comparison example. Note that the field-effect mobility shown in FIG. 11A was obtained at a drain voltage (Vd) of 10 V. The field-effect mobility is not shown in FIG. 11B because it was difficult to calculate.

[0228]

FIG. 11A demonstrates that the transistors of the sample of this example exhibited excellent switching characteristics. FIG. 11B shows that the transistors of the sample of the comparison example did not exhibit switching characteristics and were normally on.

[0229]

Comparison with the sample of this example reveals that the deficiency of the switching characteristics of the sample of the comparison example was caused because the gas released from the acrylic resin affected the transistors. Specifically, this was probably because the gas released from the acrylic resin increased the carrier density in the oxide semiconductor film, and an electric field from the gate electrode prevented the transistors from being turned off.

[0230]

This example shows that, when an organic resin is covered with a film (a 200-nm-thick silicon nitride film, here) that does not transmit released gas of water, a hydrocarbon, or the like, the gas released from the organic resin causes a deficiency of the switching characteristics of a transistor. This example also shows that, by providing a path through which the released gas is extracted to the outside of the sample in part of the film that covers the organic resin and does not transmit the released gas of water, a hydrocarbon, or the like, a deficiency of the switching characteristics of a transistor can be avoided and excellent switching characteristics can be obtained.

REFERENCE NUMERALS

[0231]

101: first transistor, 102: first substrate, 103: second transistor, 104: gate electrode, 105:

third transistor, 106: gate insulating film, 107: capacitor, 108: semiconductor layer, 110: source electrode, 112: drain electrode, 113: electrode, 114: first interlayer insulating film, 116: second interlayer insulating film, 118: capacitor electrode, 120: third interlayer insulating film, 122: pixel electrode, 124: first alignment film, 126: partition, 128: light-emitting layer, 130: electrode, 140: gate driver circuit portion, 142: pixel region, 144: source driver circuit portion, 146: FPC terminal portion, 148: FPC, 150: liquid crystal element, 152: second substrate, 153: colored film, 154: light-blocking film, 156: organic protective insulating film, 158: counter electrode, 160: spacer, 162: liquid crystal layer, 164: second alignment film, 166: sealant, 170: light-emitting element, 172: filler, 4001: first substrate, 4002: photodiode element, 4014: first interlayer insulating film, 4016: second interlayer insulating film, 4020: third interlayer insulating film, 4024: first alignment film, 4030: first transistor, 4032: capacitor, 4034: liquid crystal element, 4036: gate line, 4040: transistor, 4052: second substrate, 4056: transistor, 4057: gate selection line, 4058: reset signal line, 4059: video signal line, 4060: second transistor, 4062: third transistor, 4071: output signal line, 4084: second alignment film, 4085: colored film, 4086: organic insulating film, 4088: counter electrode, 4096: liquid crystal layer, 5040: gate driver circuit portion, 5042: pixel region, 8033: clasp, 8034: switch, 8035: power supply switch, 8036: switch, 8038: operation switch, 8630: housing, 8631: display portion, 8631a: display portion, 8631b: display portion, 8633: solar cell, 8634: charge and discharge control circuit, 8635: battery, 8636: DCDC converter, 8637: converter, 9300: housing, 9301: button, 9302: microphone, 9303: display portion, 9304: speaker, 9305: camera, 9310: housing, 9311: display portion, 9320: housing, 9321: button, 9322: microphone, 9323: display portion.

This application is based on Japanese Patent Application serial no. 2012-161344 filed with the Japan Patent Office on July 20, 2012, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A display device comprising:

a pixel portion comprising:

a first transistor;

a first insulating film over the first transistor;

a second insulating film over the first insulating film;

a third insulating film over the second insulating film;

a first electrode over the third insulating film, the first electrode being electrically connected to the first transistor;

a first alignment film over the first electrode; and

a liquid crystal layer over the first alignment film; and

a driver circuit portion comprising:

a second transistor;

the first insulating film over the second transistor;

the second insulating film over the first insulating film; and

the first alignment film over the second insulating film,

wherein the first insulating film comprises an inorganic insulating material,

wherein the second insulating film comprises an organic insulating material,

wherein the third insulating film comprises an inorganic insulating material, and

wherein the first alignment film is entirely in contact with the second insulating film in the driver circuit portion.

2. The display device according to claim 1 further comprising:

a second alignment film over the liquid crystal layer;

a second electrode over the second alignment film;

a fourth insulating film over the second electrode;

a colored film over the fourth insulating film; and

a light-blocking film over the fourth insulating film.

3. The display device according to claim 1,

wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a Ga-Zn-based metal oxide film.

4. The display device according to claim 1,

wherein the second insulating film is any of an acrylic-based resin, a polyimide-based resin, a benzocyclobutene-based resin, a polyamide-based resin, and an epoxy-based resin.

5. The display device according to claim 1,

wherein the third insulating film is any of a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

6. The display device according to claim 1,

wherein the first transistor and the second transistor each comprises an oxide semiconductor layer.

7. The display device according to claim 6,

wherein the oxide semiconductor layer comprises any of indium and zinc.

8. The display device according to claim 6,

wherein the oxide semiconductor layer has a first oxide semiconductor film and a second oxide semiconductor film.

9. An electronic device comprising the display device according to claim 1.

10. A display device comprising:

a pixel portion comprising:

a first transistor;

a first insulating film over the first transistor;

a second insulating film over the first insulating film;

a third insulating film over the second insulating film;

a first electrode over the third insulating film, the first electrode being electrically connected to the first transistor;

a fourth insulating film over the first electrode;

a light-emitting layer over the first electrode;

a second electrode over the light-emitting layer; and

a filler over the second electrode; and

a driver circuit portion comprising:

a second transistor;

the first insulating film over the second transistor;

the second insulating film over the first insulating film; and

the filler over the second insulating film,

wherein the first insulating film comprises an inorganic insulating material,

wherein the second insulating film comprises an organic insulating material,

wherein the third insulating film comprises an inorganic insulating material, and

wherein the filler is entirely in contact with the second insulating film in the driver circuit portion.

11. The display device according to claim 10,

wherein the first insulating film is any of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, and a Ga-Zn-based metal oxide film.

12. The display device according to claim 10,

wherein the second insulating film is any of an acrylic-based resin, a polyimide-based resin, a benzocyclobutene-based resin, a polyamide-based resin, and an epoxy-based resin.

13. The display device according to claim 10,

wherein the third insulating film is any of a silicon nitride film, a silicon nitride oxide film, and an aluminum oxide film.

14. The display device according to claim 10,

wherein the first transistor and the second transistor each comprises an oxide semiconductor layer.

15. The display device according to claim 14,

wherein the oxide semiconductor layer comprises any of indium and zinc.

16. The display device according to claim 14,

wherein the oxide semiconductor layer has a first oxide semiconductor film and a second oxide semiconductor film.

17. An electronic device comprising the display device according to claim 10.

18. The display device according to claim 10,

wherein the filler is any of an inert gas, an ultraviolet curable resin, and a thermosetting resin.

19. The display device according to claim 10,

wherein the filler is an insulating film.

20. The display device according to claim 10,

wherein the filler is any of polyvinyl chloride, an acrylic-based resin, a polyimide-based resin, an epoxy-based resin, a silicone-based resin, polyvinyl butyral, and ethylene vinyl acetate.

ABSTRACT

The display device includes a first substrate provided with a driver circuit region that is located outside and adjacent to a pixel region and includes at least one second transistor which supplies a signal to the first transistor in each of the pixels in the pixel region, a second substrate facing the first substrate, a liquid crystal layer between the first substrate and the second substrate, a first interlayer insulating film including an inorganic insulating material over the first transistor and the second transistor, a second interlayer insulating film including an organic insulating material over the first interlayer insulating film, and a third interlayer insulating film including an inorganic insulating material over the second interlayer insulating film. The third interlayer insulating film is provided in part of an upper region of the pixel region, and has an edge portion on an inner side than the driver circuit region.

FIG. 1A

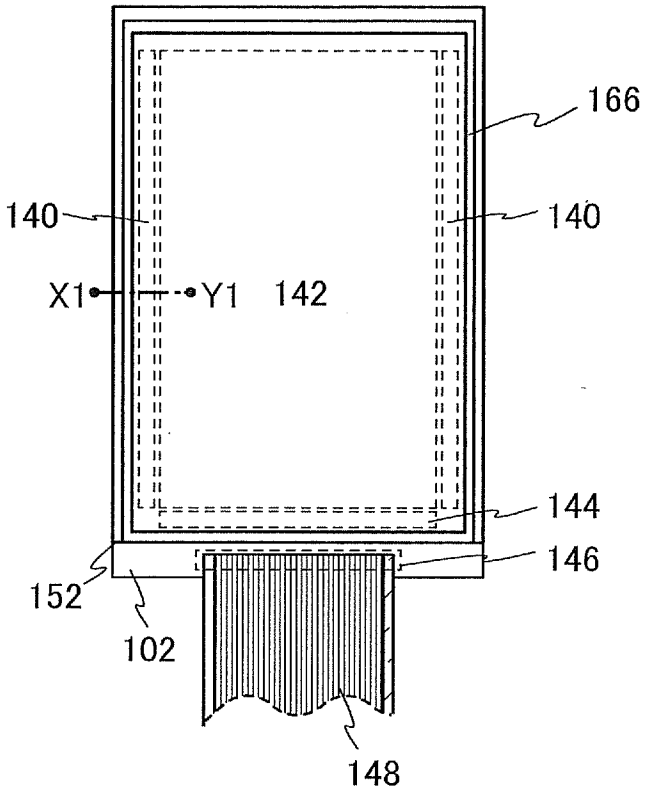
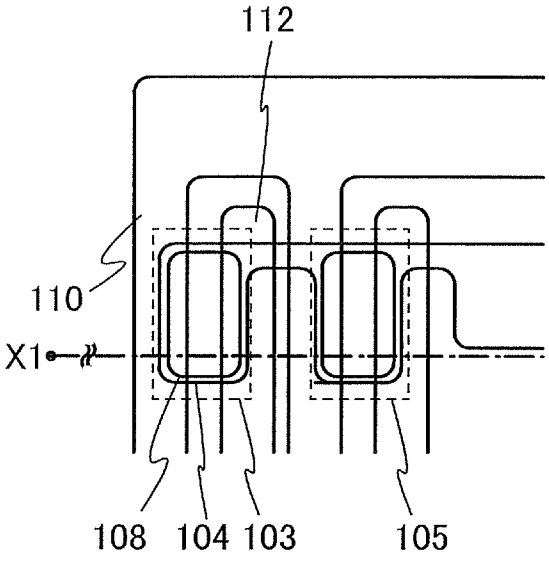
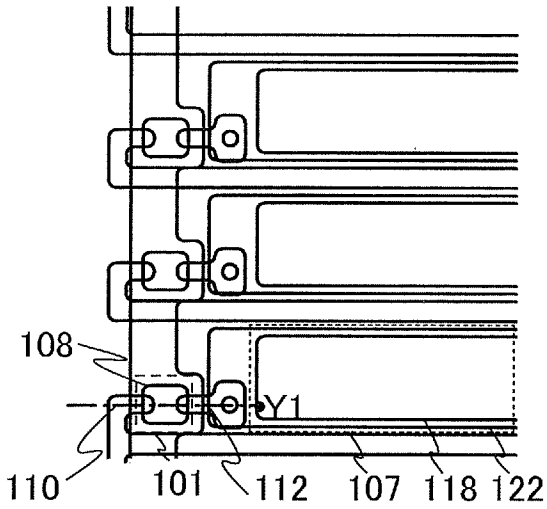


FIG. 1B



140

FIG. 1C



142

FIG. 2

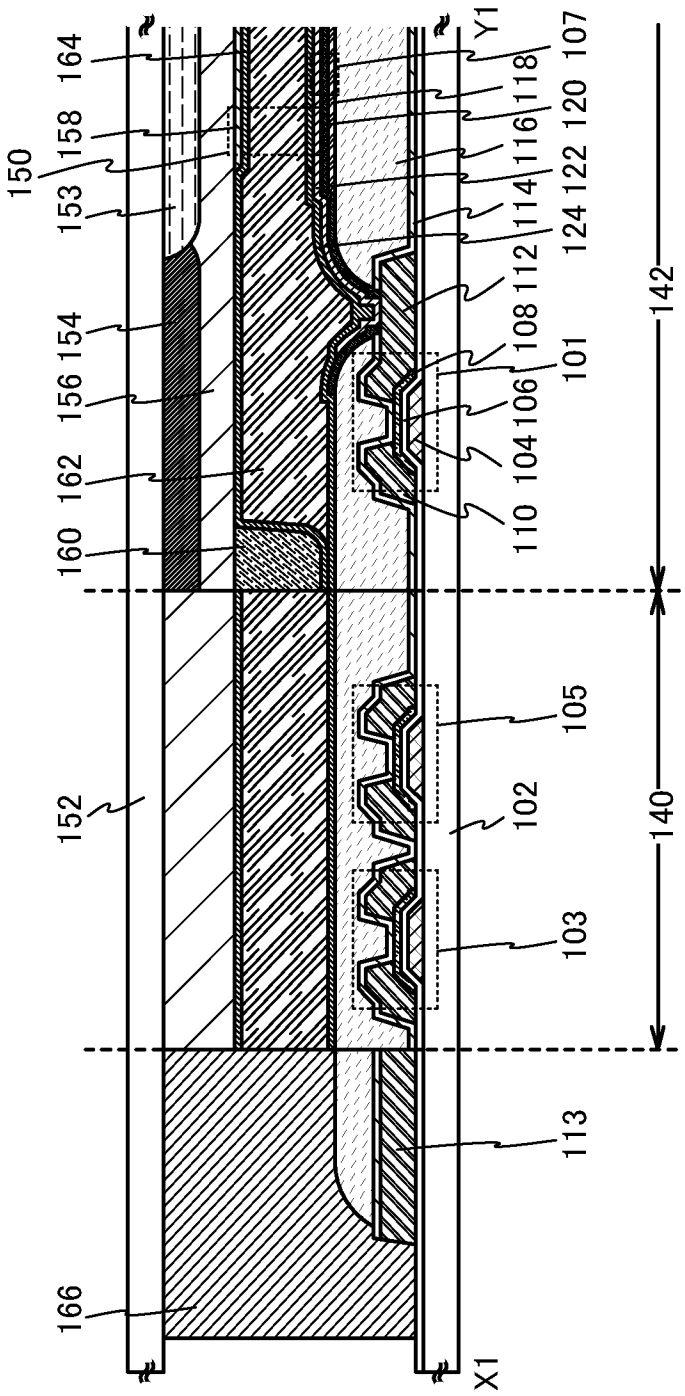

150
153
154
156
158
160
162
164
166
152
Y1
X1
107
118
120
116
122
114
124
112
108
101
106
104
110
105
102
103
113
142
140

FIG. 3

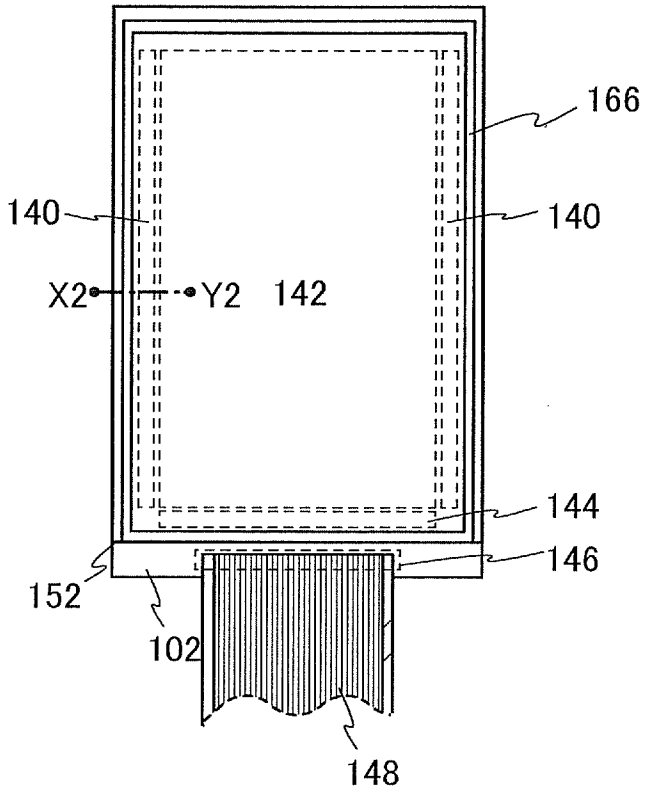
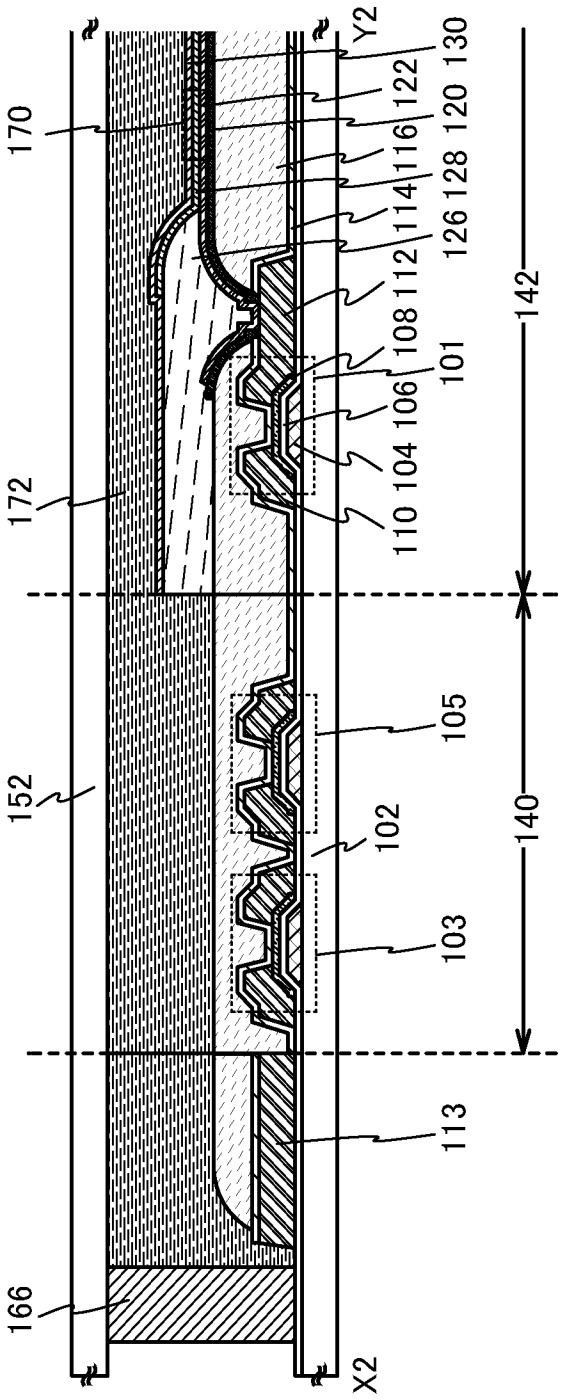


FIG. 4


Y2
X2
170
172
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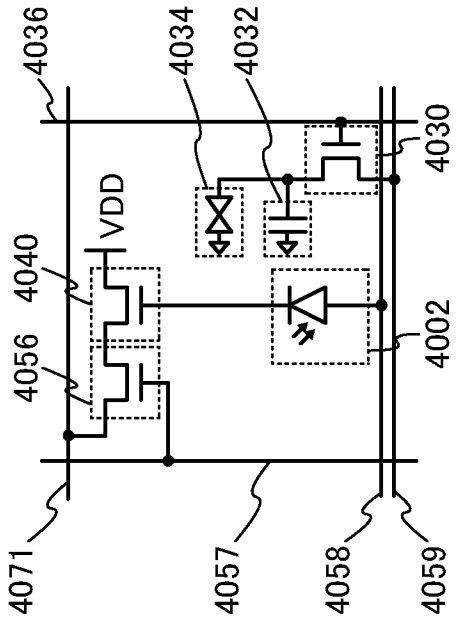
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VDD
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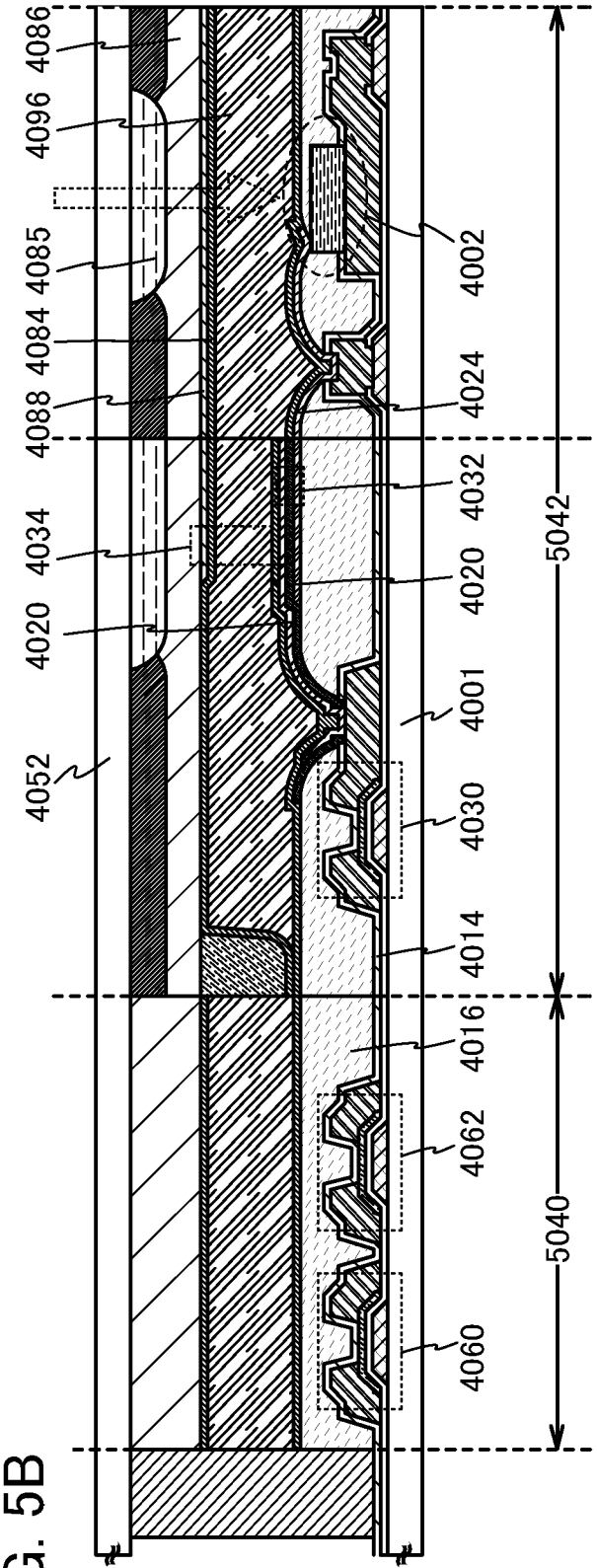
4056
4002
4071
4057
4058
4059

FIG. 5A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4002
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4001
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4014
4016
4062
4060
5042
5040

FIG. 5B

FIG. 6A

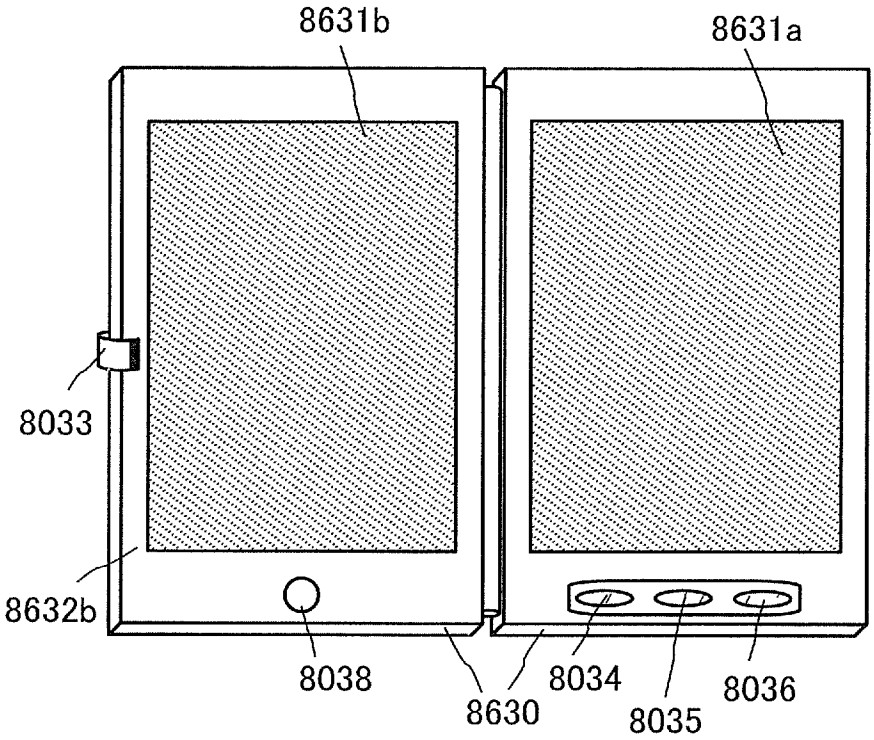


FIG. 6B

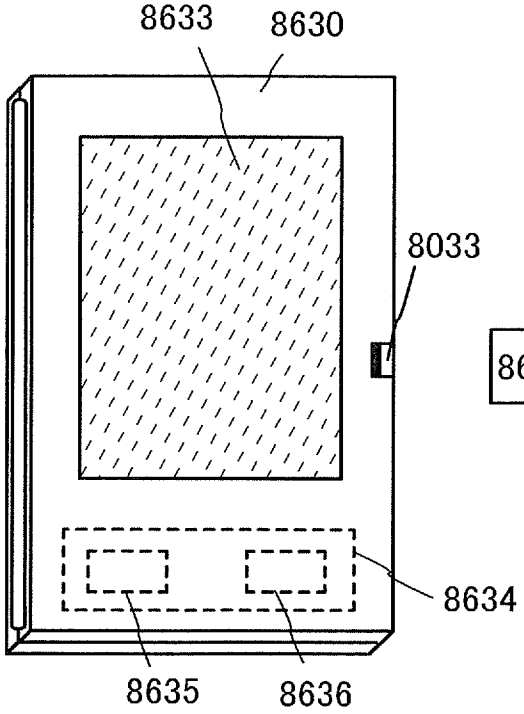


FIG. 6C

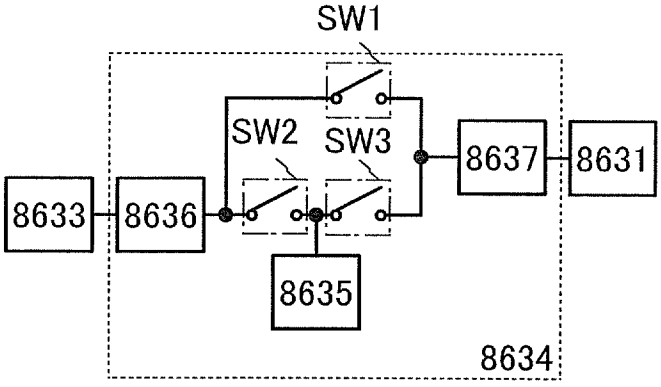


FIG. 7A

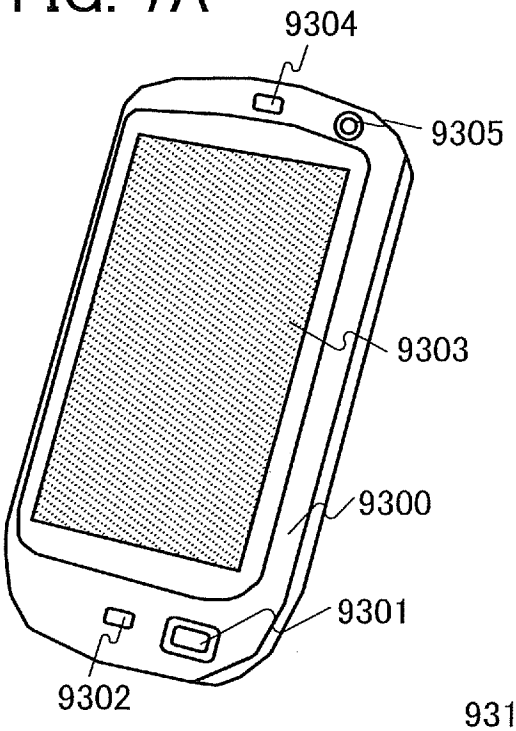


FIG. 7B

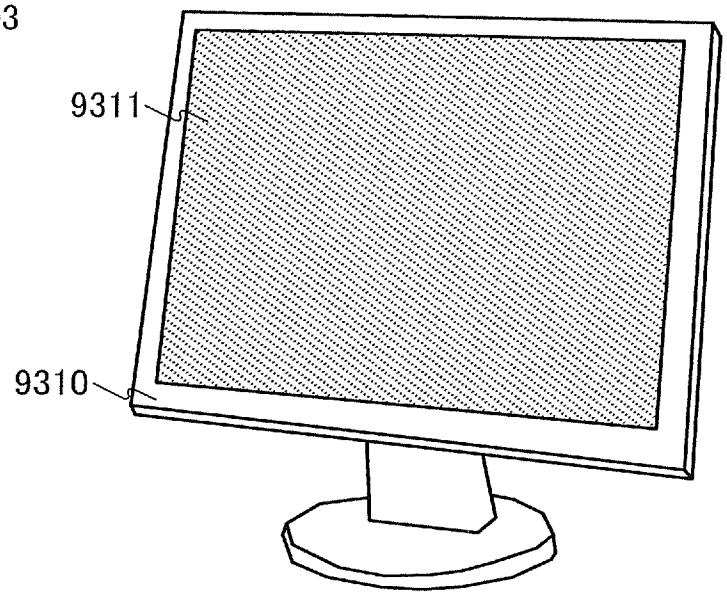


FIG. 7C

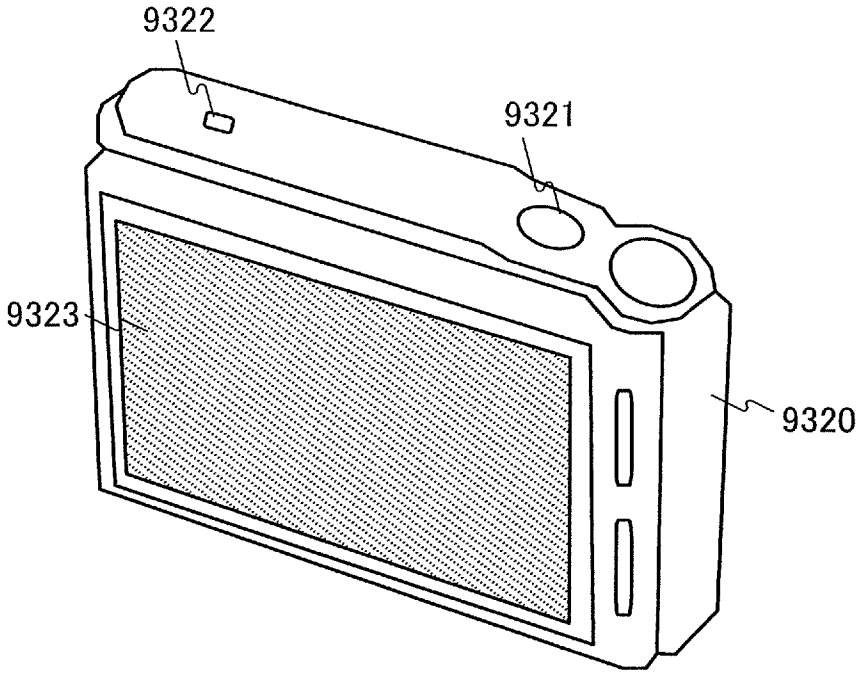


FIG. 8

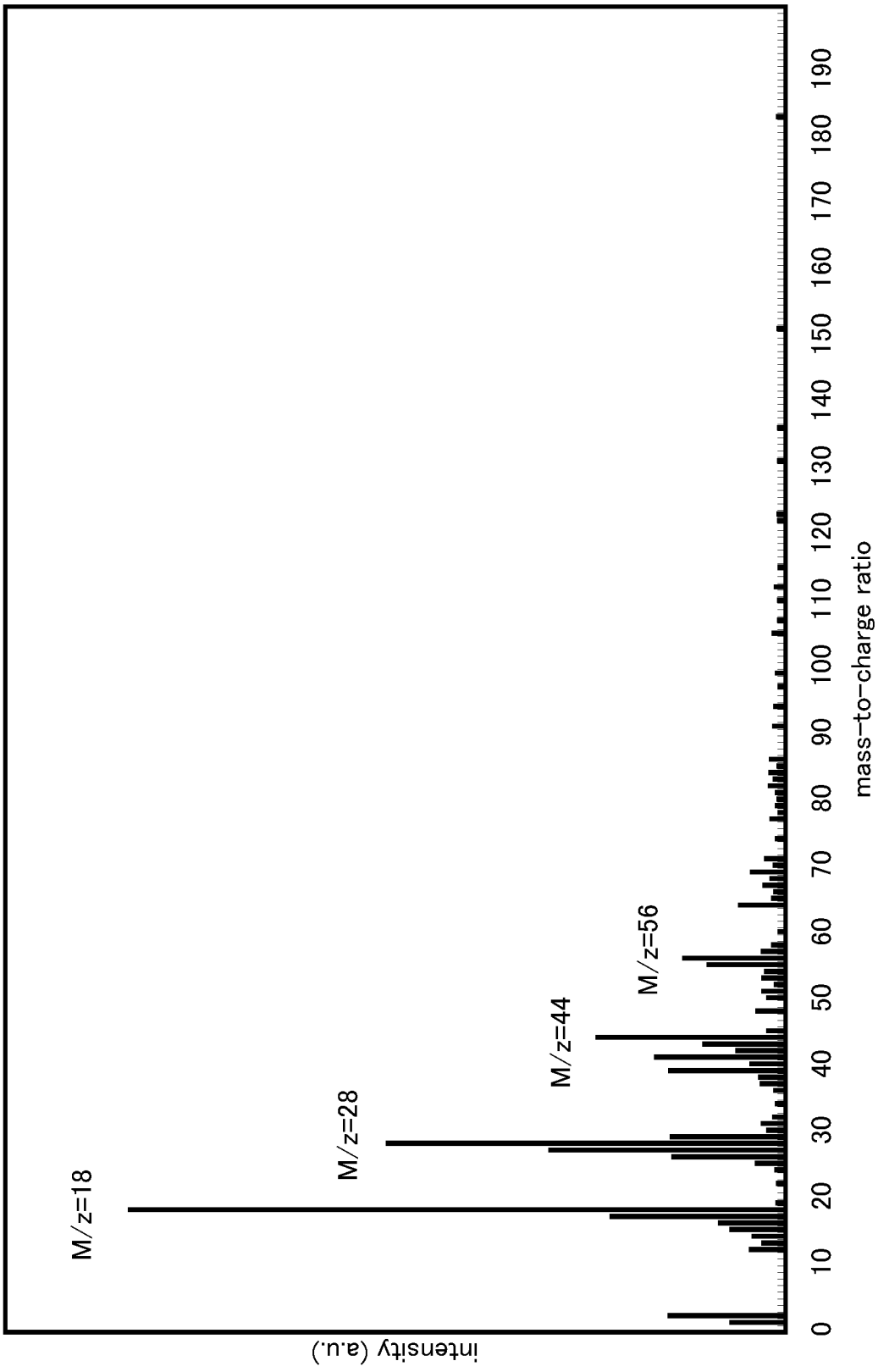

M/z=18
M/z=28
M/z=44
M/z=56
intensity (a.u.)
0
10
20
30
40
50
60
70
80
90
100
110
120
130
140
150
160
170
180
190
mass-to-charge ratio

FIG. 9

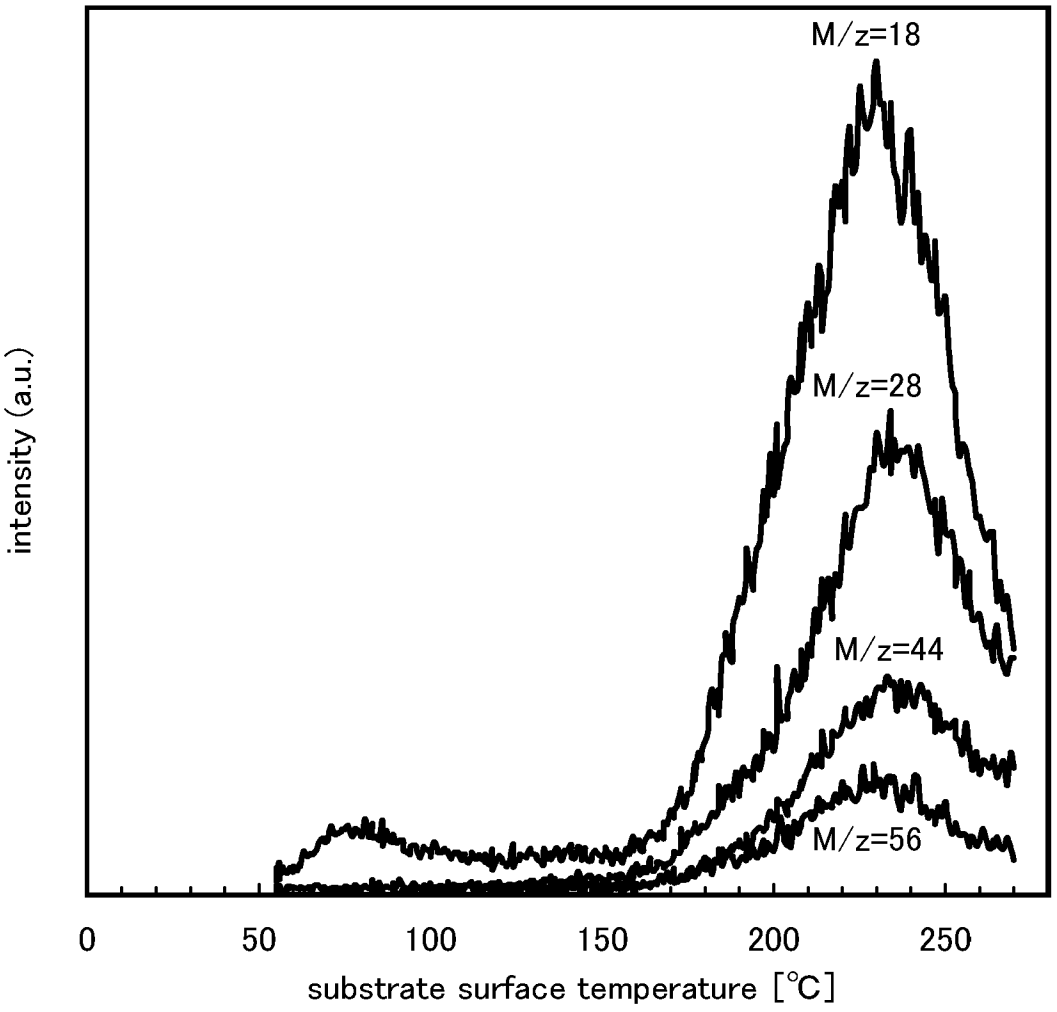

M/z=18
M/z=28
M/z=44
M/z=56
intensity (a.u.)
0
50
100
150
200
250
substrate surface temperature [℃]

FIG. 10

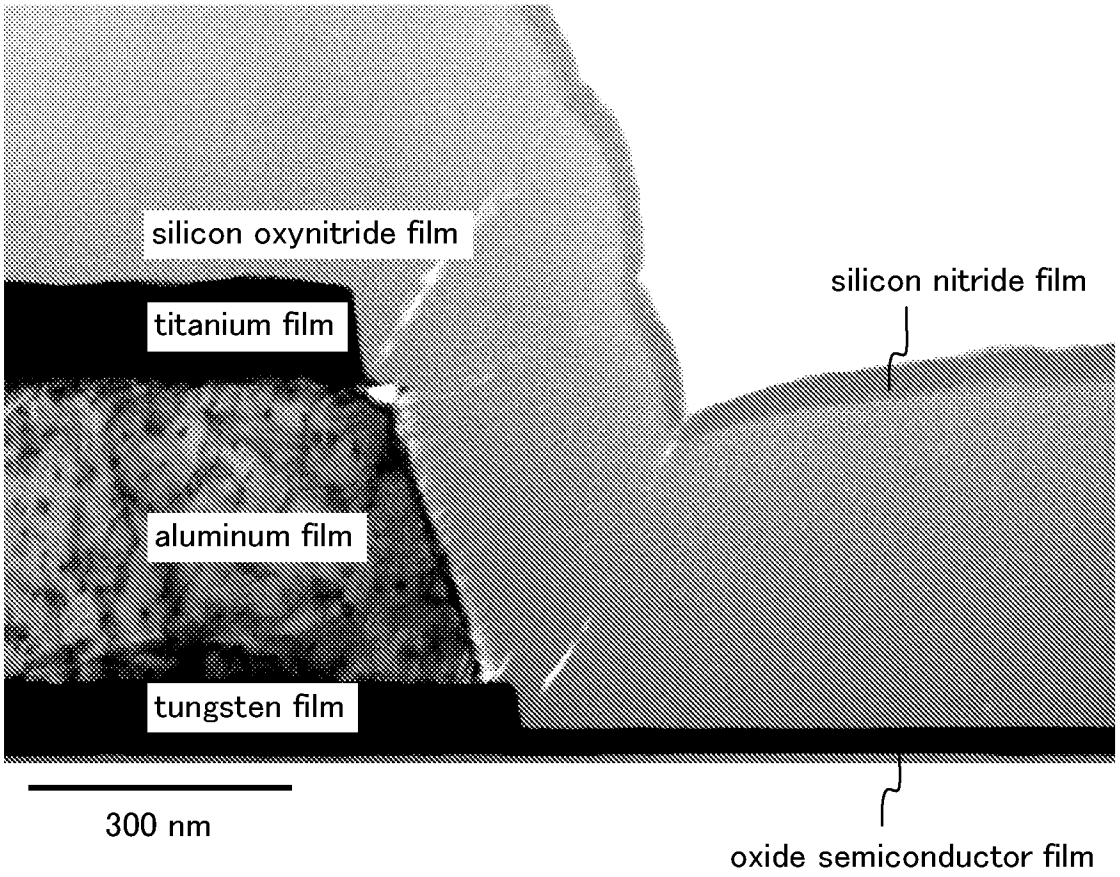

silicon oxynitride film
titanium film
aluminum film
tungsten film
silicon nitride film
300 nm
oxide semiconductor film

FIG. 11A

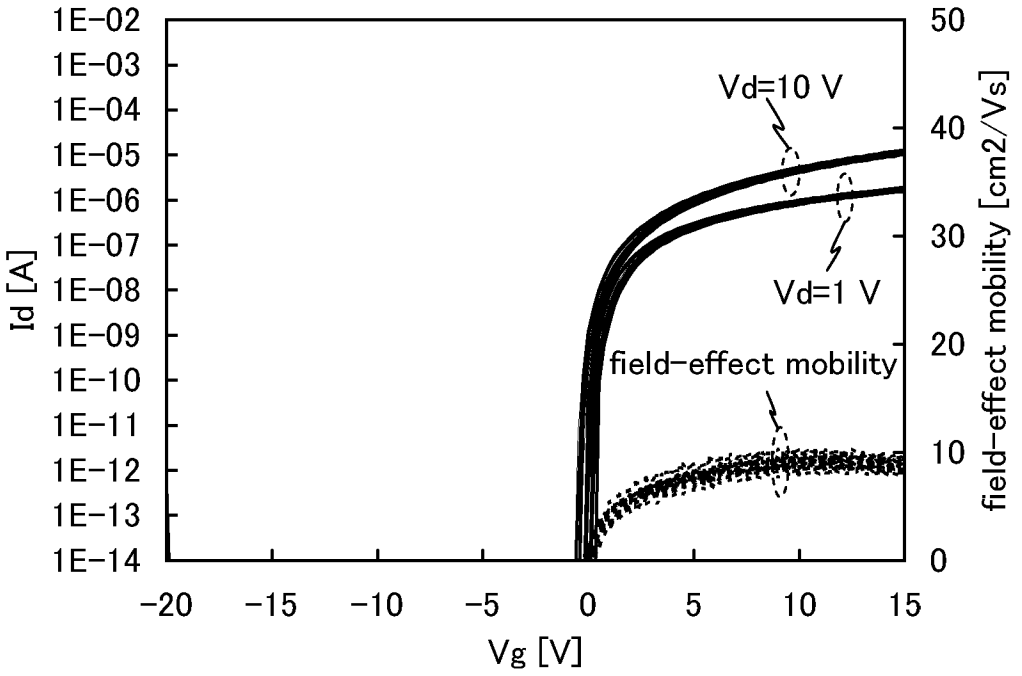
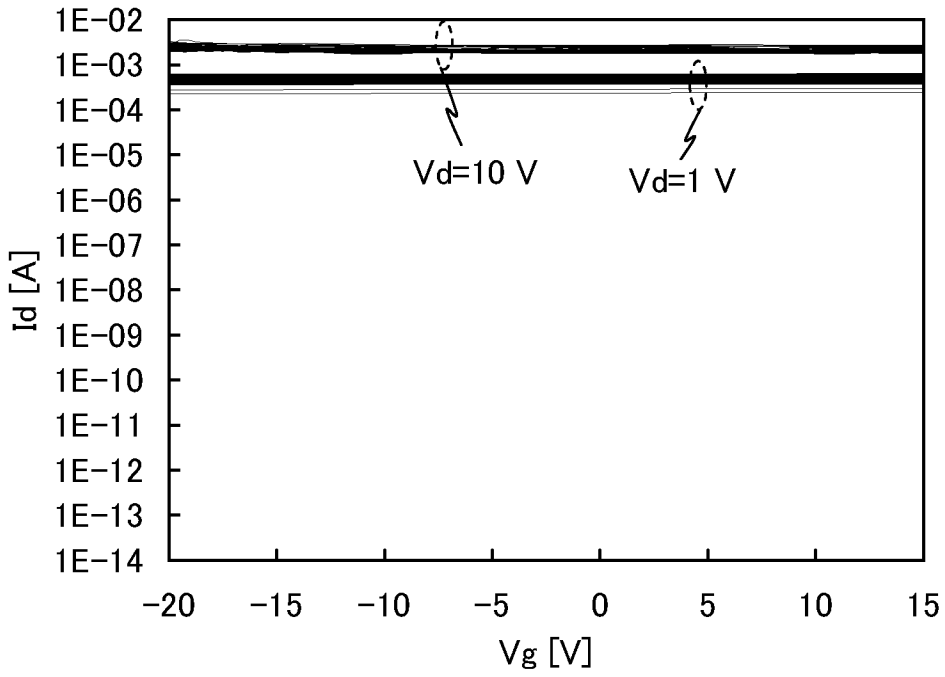


FIG. 11B



Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu Hosaka
Filer:	Eric J. Robinson/Sue Ann Carr
Attorney Docket Number:	0756-10194

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1600**

Electronic Acknowledgement Receipt

EFS ID:	16263511
Application Number:	13939323
International Application Number:	
Confirmation Number:	2340
Title of Invention:	DISPLAY DEVICE AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE
First Named Inventor/Applicant Name:	Yasuharu Hosaka
Customer Number:	31780
Filer:	Eric J. Robinson/Sue Ann Carr
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10194
Receipt Date:	11-JUL-2013
Filing Date:	
Time Stamp:	11:12:19
Application Type:	Utility under 35 USC 111(a)

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Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$1600
RAM confirmation Number	9801
Deposit Account	
Authorized User	

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

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Information:					
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Multipart Description/PDF files in .zip description

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Transmittal Letter	1	1
Information Disclosure Statement (IDS) Form (SB08)	2	2

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	Claims	55	58
	Abstract	59	59
	Drawings-other than black and white line drawings	60	70

Warnings:					
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.