PTO/AIA/15 (07-12)
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U.S. Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	0756-10065
First Inventor	Shunpei YAMAZAKI et al.
Title	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ **Fee Transmittal Form.** (PTO/SB/17 or equivalent)
2. ☐ **Applicant claims small entity status.** See 37 CFR 1.27.
3. ☒ **Specification.** [*Total Pages* 78] Both the claims and abstract must start on a new page *(For information on the preferred arrangement, see MPEP § 608.01(a))*
4. ☒ **Drawing(s).** *(35 U.S.C. 113)* [*Total Sheets* 37]
5. **Inventor's Oath or Declaration.** [*Total Sheets* ____] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. ☐ Newly executed (original or copy)
   b. ☐ A copy from a prior application (37 CFR 1.63(d))
6. ☒ **Application Data Sheet.** *See Note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
7. ☐ **CD-ROM or CD-R.** in duplicate, large table or Computer Program *(Appendix)*
   ☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission.** *(if applicable, items a. – c. are required)*
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO:

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

ACCOMPANYING APPLICATION PARTS

9. ☐ **Assignment Papers.** (cover sheet & document(s))
   Name of Assignee ____
10. ■ **37 CFR 3.73(c) Statement.** ■ **Power of Attorney.** *(when there is an assignee)*
11. ☐ **English Translation Document.** *(if applicable)*
12. ■ **Information Disclosure Statement.** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations attached
13. ☐ **Preliminary Amendment.**
14. ☐ **Return Receipt Postcard.** *(MPEP § 503) (Should be specifically itemized)*
15. ☐ **Certified Copy of Priority Document(s).** *(if foreign priority is claimed)*
16. ☐ **Nonpublication Request.** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
17. ☐ **Other:** ____

19. CORRESPONDENCE ADDRESS

■ The address associated with Customer Number: 31780 **OR** ☐ Correspondence address below

Name	Eric J. Robinson, Robinson Intellectual Property Law Office, P.C.				
Address	3975 Fair Ridge Drive, Suite 20 North				
City	Fairfax	State	VA	Zip Code	22033
Country	US	Telephone	571-434-6789	Email	erobinson@riplo.com

Signature		Date	February 11, 2013
Name (Print/Type)	Eric J. Robinson	Registration No. (Attorney/Agent)	38,285

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Semiconductor Energy Laboratory Co., Ltd.

Application No./Patent No.: _____ Filed/Issue Date: February 11, 2013

Titled: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

Semiconductor Energy Laboratory Co., Ltd., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 023662, Frame 0270, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature	February 11, 2013 Date
Eric J. Robinson Printed or Typed Name	Reg. No. 38,285 Title or Registration Number

[Page 2 of 2]

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/80 (07-12)
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U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☑ Practitioners associated with Customer Number: 31780

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications a ssigned only to the undersigned according to the USPTO assignment records or assignments docu ments attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 31780

OR

☐	Firm or Individual Name		
	Address		
	City		
	Country		
	Telephone		Email

Assignee Name and Address: SEMICONDUCTOR ENERGY LABORATORY CO., LTD.
398, HASE, ATSUGI-SHI
KANAGAWA-KEN 243-0036
JAPAN

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Shunpei Yamazaki	Date	09/21/2012
Name	Dr. Shunpei Yamazaki	Telephone	81-46-270-1170
Title	President		

Privacy Act Statement

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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PTO/AIA/14 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10065
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shunpei		YAMAZAKI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Setagaya	Country of Residence	JP

Mailing Address of Inventor:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country**	JP

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kengo		AKIMOTO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Atsugi	Country of Residence	JP

Mailing Address of Inventor:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country**	JP

Inventor 3 Remove

Legal Name

PTO/AIA/14 (08-12)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10065
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Daisuke		KAWAE	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Yamato	Country of Residence i	JP

Mailing Address of Inventor:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country** i	JP

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	31780		
Email Address	erobinson@riplo.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF		
Attorney Docket Number	0756-10065	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	37	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

PTO/AIA/14 (08-12)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10065
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF	

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for thr Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	31780		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	12613769	2009-11-06
Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12613769	Continuation of	12606262	2009-10-27

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country i	Filing Date (YYYY-MM-DD)	Priority Claimed
2008-287187	JP	2008-11-07	◉ Yes ○ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10065
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF	

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Remove

◉	Assignee	○	Legal Representative under 35 U.S.C. 117
○	Person to whom the inventor is obligated to assign.	○	Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :	

If the Assignee is an Organization check here. ☒

Organization Name	Semiconductor Energy Laboratory Co., Ltd.

Mailing Address Information:

Address 1	398, Hase		
Address 2			
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Country [i]	JP	Postal Code	243-0036
Phone Number		Fax Number	

PTO/AIA/14 (08-12)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10065
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF	

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Signature	/Eric J. Robinson/			Date (YYYY-MM-DD)	2013-02-11
First Name	Eric J.	Last Name	Robinson	Registration Number	38285

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Attorney Docket No. 0756-10065

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re CONTINUATION Patent Application of:	)	
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2896
Based on Serial No. 12/613,769	)	Examiner: Jeremy J. Joy
Filed: November 6, 2009	)	
For: SEMICONDUCTOR DEVICE AND	)	
MANUFACTURING METHOD	)	
THEREOF	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application.

U.S. Publication No. 2007/0072439 is in the family of JP 2007-123861.

U.S. Patent No. 6,727,522 is in the family of JP 2000-150900.

U.S. Patent No. 7,061,014 is in the family of JP 2004-103957.

U.S. Patent No. 5,744,864 is in the family of JP 11-505377.

U.S. Patent No. 6,563,174 is in the family of JP 2003-086808.

U.S. Publication No. 2006/0244107 is in the family of WO 2004/114391.

The references listed on the attached Form PTO-1449 were cited in parent Application Serial No. 12/613,769 and/or predecessor Application Serial No. 12/606,262

and copies of the references can be found in these applications (37 C.F.R. § 1.98(d)(1)-(2)).

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

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Sheet 1 of 14

Complete if Known	
Application Number	Based on 12/613,769
Filing Date	November 6, 2009
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2896
Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10065

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7,323,368		Takayama et al.	01/29/2008	
		2007/0272922		Kim et al.	11/29/2007	
		2007/0158652		Lee et al.	07/12/2007	
		2008/0128689		Lee et al.	06/05/2008	
		7,298,084		Baude et al.	11/20/2007	
		6,532,045		Chung et al.	03/11/2003	
		2007/0108446		Akimoto	05/17/2007	
		2007/0072439		Akimoto et al.	03/29/2007	
		5,847,410		Nakajima	12/08/1998	
		6,586,346		Yamazaki et al.	07/01/2003	
		2003/0189401		Kido et al.	10/09/2003	
		6,960,812		Yamazaki et al.	11/01/2005	
		6,727,522		Kawasaki et al.	04/27/2004	
		7,061,014		Hosono et al.	06/13/2006	
		2008/0296568		Ryu et al.	12/04/2008	
		2008/0308806		Akimoto et al.	12/18/2008	
		2008/0308805		Akimoto et al.	12/18/2008	
		2008/0308804		Akimoto et al.	12/18/2008	
		2008/0308797		Akimoto et al.	12/18/2008	
		2008/0308796		Akimoto et al.	12/18/2008	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP	2007-123861			05/17/2007		Abst.
		JP	2007-096055			04/12/2007		Full

Examiner Signature		Date Considered	

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Sheet 2 of 14

Complete if Known	
Application Number	Based on 12/613,769
Filing Date	November 6, 2009
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2896
Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10065

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2009/0008639		Akimoto et al.	01/08/2009	
		2007/0172591		Seo et al.	07/26/2007	
		2007/0187760		Furuta et al.	08/16/2007	
		2008/0203387		Kang et al.	08/28/2008	
		2009/0065771		Iwasaki et al.	03/12/2009	
		7,301,211		Yamazaki et al.	11/27/2007	
		2006/0244107		Sugihara et al.	11/02/2006	
		5,744,864		Cillessen et al.	04/28/1998	
		2010/0025678		Yamazaki et al.	02/04/2010	
		7,674,650		Akimoto et al.	03/09/2010	
		6,563,174		Kawasaki et al.	05/13/2003	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP	03-231472	A		10/15/1991		Abst.
		JP	2000-150900	A		05/30/2000		Abst.
		JP	2004-103957	A		04/02/2004		Abst.
		JP	11-505377			05/18/1999		Abst.
		JP	08-264794	A		10/11/1996		Full
		JP	2007-250983	A		09/27/2007		Abst.
		WO	2007/119386			10/25/2007		Eng.
		JP	05-251705	A		09/28/1993		Full
		WO	2004/114391			12/29/2004		Abst.
		JP	2003-086000	A		03/20/2003		Full
		JP	2003-086808	A		03/20/2003		Abst.

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Dembo et al., "RFCPUS on Glass and Plastic Substrates Fabricated by TFT Transfer Technology," IEDM 05: TECHNICAL DIGEST OF INTERNATIONAL ELECTRON DEVICES MEETING, December 5, 2005, pp. 1067-1069.	Eng.

Examiner Signature		Date Considered	

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Complete if Known	
Application Number	Based on 12/613,769
Filing Date	November 6, 2009
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2896
Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10065

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		Ikeda et al., "Full-Functional System Liquid Crystal Display Using CG-Silicon Technology," SID DIGEST '04: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, 2004, Vol. 35, pp. 860-863.	Eng.
		Nomura et al., "Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Amorphous Oxide Semiconductors," NATURE, November 25, 2004, Vol. 432, pp. 488-492.	Eng.
		Takahashi et al., "Theoretical Analysis of IGZO Transparent Amorphous Oxide Semiconductor," IDW '08: PROCEEDINGS OF THE 15th INTERNATIONAL DISPLAY WORKSHOPS, December 3, 2008, pp. 1637-1640.	Eng.
		Prins et al., "A Ferroelectric Transparent Thin-Film Transistor," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), June 17, 1996, Vol. 68, No. 25, pp. 3650-3652.	Eng.
		Nakamura et al., "The Phase Relations In the In_2O_3-Ga_2ZnO_4-ZnO System at 1350°C," JOURNAL OF SOLID STATE CHEMISTRY, August 1, 1991, Vol. 93, No. 2, pp. 298-315.	Eng.
		Kimizuka et al., "Syntheses and Single-Crystal Data of Homologous Compounds, $In_2O_3(ZnO)_m$ (m = 3, 4, and 5), $InGaO_3(ZnO)_3$, and $Ga_2O_3(ZnO)_m$ (m = 7, 8, 9, and 16) in the In_2O_3-$ZnGa_2O_4$-ZnO System," JOURNAL OF SOLID STATE CHEMISTRY, April 1, 1995, Vol. 116, No. 1, pp. 170-178.	Eng.
		Nomura et al., "Thin-Film Transistor Fabricated in Single-Crystalline Transparent Oxide Semiconductor," SCIENCE, May 23, 2003, Vol. 300, No. 5623, pp. 1269-1272.	Eng.
		Osada et al., "15.2: Development of Driver-Integrated Panel using Amorphous In-Ga-Zn-Oxide TFT," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 184-187.	Eng.
		Li et al., "Modulated Structures of Homologous Compounds $InMO_3(ZnO)_m$ (M=In,Ga; m=Integer) Described by Four-Dimensional Superspace Group," JOURNAL OF SOLID STATE CHEMISTRY, 1998, Vol. 139, pp. 347-355.	Eng.

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Complete if Known	
Application Number	Based on 12/613,769
Filing Date	November 6, 2009
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2896
Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10065

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

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		Lee et al., "World's Largest (15-inch) XGA AMLCD Panel Using IGZO Oxide TFT," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, pp. 625-628.	Eng.
		Nowatari et al., "60.2: Intermediate Connector with Suppressed Voltage Loss for White Tandem OLEDs," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, Vol. 40, pp. 899-902.	Eng.
		Kanno et al., "White Stacked Electrophosphorecent Organic Light-Emitting Devices Employing MoO_3 as a Charge-Generation Layer," ADV. MATER. (ADVANCED MATERIALS), 2006, Vol. 18, No. 3, pp. 339-342.	Eng.
		Tsuda et al., "Ultra Low Power Consumption Technologies for Mobile TFT-LCDs," IDW '02: PROCEEDINGS OF THE 9th INTERNATIONAL DISPLAY WORKSHOPS, December 4, 2002, pp. 295-298.	Eng.
		Jeong et al., "3.1: Distinguished Paper: 12.1-Inch WXGA AMOLED Display Driven by Indium-Gallium-Zinc Oxide TFTs Array," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, No. 1, pp. 1-4.	Eng.
		Kurokawa et al., "UHF RFCPUs on Flexible and Glass Substrates for Secure RFID Systems," JOURNAL OF SOLID-STATE CIRCUITS, 2008, Vol. 43, No. 1, pp. 292-299.	Eng.
		Ohara et al., "Amorphous In-Ga-Zn-Oxide TFTs with Suppressed Variation for 4.0 inch QVGA AMOLED Display," AM-FPD '09 DIGEST OF TECHNICAL PAPERS, July 1, 2009, pp. 227-230, THE JAPAN SOCIETY OF APPLIED PHYSICS.	Eng.
		Coates et al., "OPTICAL STUDIES OF THE AMORPHOUS LIQUID-CHOLESTERIC LIQUID CRYSTAL TRANSITION: THE "BLUE PHASE"," PHYSICS LETTERS, September 10, 1973, Vol. 45A, No. 2, pp. 115-116.	Eng.
		Cho et al., "21.2: Al and Sn-doped Zinc Indium Oxide Thin Film Transistors For AMOLED Back-Plane," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 280-283.	Eng.

Examiner Signature		Date Considered	

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Substitute for form 1449A/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				**Application Number**	Based on 12/613,769
				Filing Date	November 6, 2009
				First Named Inventor	Shunpei YAMAZAKI et al.
				Group Art Unit	2896
				Examiner Name	Jeremy J. Joy
Sheet	5	of	14	**Attorney Docket Number**	0756-10065

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Lee et al., "15.4: Excellent Performance of Indium-Oxide-Based Thin-Film Transistors by DC Sputtering," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 191-193.	Eng.
		Jin et al., "65.2: Distinguished Paper: World-Largest (6.5") Flexible Full Color Top Emission AMOLED Display on Plastic Film and Its Bending Properties," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 983-985.	Eng.
		Sakata et al., "Development of 4.0-In. AMOLED Display with Driver Circuit Using Amorphous In-Ga-Zn-Oxide TFTs," IDW '09: PROCEEDINGS OF THE 16th INTERNATIONAL DISPLAY WORKSHOPS, 2009, pp. 689-692.	Eng.
		Park et al., "Amorphous Indium-Gallium-Zinc Oxide TFTs and their Application for Large Size AMOLED," AM-FPD '08 DIGEST OF TECHNICAL PAPERS, July 2, 2008, pp. 275-278.	Eng.
		Park et al., "Challenge to Future Displays: Transparent AM-OLED Driven by PEALD Grown ZnO TFT," IMID '07 DIGEST, 2007, pp. 1249-1252.	Eng.
		Godo et al., "Temperature Dependence of Characteristics and Electronic Structure for Amorphous In-Ga-Zn-Oxide TFT," AM-FPD '09 DIGEST OF TECHNICAL PAPERS, July 1, 2009, pp. 41-44.	Eng.
		Osada et al., "Development of Driver-Integrated Panel using Amorphous In-Ga-Zn-Oxide TFT," AM-FPD '09 DIGEST OF TECHNICAL PAPERS, July 1, 2009, pp. 33-36.	Eng.
		Hirao et al., "Novel Top-Gate Zinc Oxide Thin-Film Transistors (ZnO TFTs) for AMLCDs," JOURNAL OF THE SID, 2007, Vol. 15, No. 1, pp. 17-22.	Eng.
		Hosono, "68.3: INVITED PAPER: TRANSPARENT AMORPHOUS OXIDE SEMICONDUCTORS FOR HIGH PERFORMANCE TFT," SID DIGEST '07: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, 2007, Vol. 38, pp. 1830-1833.	Eng.
		Godo et al., "P-9: Numerical Analysis on Temperature Dependence of Characteristics of Amorphous In-Ga-Zn-Oxide TFT," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 1110-1112.	Eng.

Examiner Signature		Date Considered	

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Sheet 6 of 14

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Application Number	Based on 12/613,769
Filing Date	November 6, 2009
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2896
Examiner Name	Jeremy J. Joy
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		Ohara et al., "21.3: 4.0 IN. QVGA AMOLED Display Using In-Ga-Zn-Oxide TFTs with a Novel Passivation Layer," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 284-287.	Eng.
		Miyasaka, "58.2: Invited Paper: Suftla Flexible Microelectronics on their Way to Business," SID DIGEST '07: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, 2007, Vol. 38, pp. 1673-1676.	Eng.
		Chern et al., "An Analytical Model for the Above-Threshold Characteristics of Polysilicon Thin-Film Transistors," IEEE TRANSACTIONS ON ELECTRON DEVICES, July 1, 1995, Vol. 42, No. 7, pp. 1240-1246.	Eng.
		Kikuchi et al., "39.1: INVITED PAPER: OPTICALLY ISOTROPIC NANO-STRUCTURED LIQUID CRYSTAL COMPOSITES FOR DISPLAY APPLICATIONS," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 578-581.	Eng.
		Asaoka et al., "29.1: POLARIZER-FREE REFLECTIVE LCD COMBINED WITH ULTRA LOW-POWER DRIVING TECHNOLOGY," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 395-398.	Eng.
		Lee et al., "Current Status of, Challenges to, and Perspective View of AM-OLED," IDW '06: PROCEEDINGS OF THE 13th INTERNATIONAL DISPLAY WORKSHOPS, December 7, 2006, pp. 663-666.	Eng.
		Kikuchi et al., "62.2: Invited Paper: Fast Electro-Optical Switching in Polymer-Stabilized Liquid Crystalline Blue Phases for Display Application," SID DIGEST '07: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, 2007, Vol. 38, pp. 1737-1740.	Eng.
		Kikuchi et al., "Polymer-Stabilized Liquid Crystal Blue Phases," NATURE MATERIALS, September 2, 2002, Vol. 1, pp. 64-68.	Eng.

Examiner Signature		Date Considered	

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Sheet 7 of 14

Complete if Known	
Application Number	Based on 12/613,769
Filing Date	November 6, 2009
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2896
Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10065

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2002/0056838		Ogawa	05/16/2002	
		2006/0169973		Isa et al.	08/03/2006	
		2006/0208977		Kimura	09/21/2006	
		2006/0238135		Kimura	10/26/2006	
		7,064,346		Kawasaki et al.	06/20/2006	
		2006/0170111		Isa et al.	08/03/2006	
		2007/0054507		Kaji et al.	03/08/2007	
		2004/0127038		Carcia et al.	07/01/2004	
		2004/0038446		Takeda et al.	02/26/2004	
		2006/0108636		Sano et al.	05/25/2006	
		2006/0108529		Saito et al.	05/25/2006	
		2006/0110867		Yabuta et al.	05/25/2006	
		2006/0113536		Kumomi et al.	06/01/2006	
		2006/0113565		Abe et al.	06/01/2006	
		2006/0113539		Sano et al.	06/01/2006	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

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		Kimizuka et al., "Spinel, $YbFe_2O_4$, and $Yb_2Fe_3O_7$ Types of Structures for Compounds in the In_2O_3 and Sc_2O_3-A_2O_3-BO Systems [A: Fe, Ga, Or Al; B: Mg, Mn, Fe, Ni, Cu, or Zn] at Temperatures Over 1000°C," JOURNAL OF SOLID STATE CHEMISTRY, 1985, Vol. 60, pp. 382-384.	Eng.
		Kitzerow et al., "Observation of Blue Phases in Chiral Networks," Liquid Crystals, 1993, Vol. 14, No. 3, pp. 911-916.	Eng.
		Costello et al., "Electron Microscopy of a Cholesteric Liquid Crystal and its Blue Phase," PHYS. REV. A (PHYSICAL REVIEW A), May 1, 1984, Vol. 29, No. 5, pp. 2957-2959.	Eng.
		Meiboom et al., "Theory of the Blue Phase of Cholesteric Liquid Crystals," PHYS. REV. LETT. (PHYSICAL REVIEW LETTERS), May 4, 1981, Vol. 46, No. 18, pp. 1216-1219.	Eng.

Examiner Signature		Date Considered	

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U.S. PATENT DOCUMENTS

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		2006/0113549		Den et al.	06/01/2006	
		7,323,356		Hosono et al.	01/29/2008	
		6,294,274		Kawazoe et al.	09/25/2001	
		7,282,782		Hoffman et al.	10/16/2007	
		7,297,977		Hoffman et al.	11/20/2007	
		7,462,862		Hoffman et al.	12/09/2008	
		2008/0254569		Hoffman et al.	10/16/2008	
		2009/0073325		Kuwabara et al.	03/19/2009	
		2005/0199959		Chiang et al.	09/15/2005	
		7,049,190		Takeda et al.	05/23/2006	
		2007/0194379		Hosono et al.	08/23/2007	
		2009/0134399		Sakakura et al.	05/28/2009	
		2006/0231882		Kim et al.	10/19/2006	
		2006/0284171		Levy et al.	12/21/2006	
		2006/0284172		Ishii	12/21/2006	
		2006/0292777		Dunbar	12/28/2006	
		2007/0024187		Shin et al.	02/01/2007	
		2007/0046191		Saito	03/01/2007	
		2007/0052025		Yabuta	03/08/2007	
		2007/0090365		Hayashi et al.	04/26/2007	
		2007/0187678		Hirao et al.	08/16/2007	
		2007/0252928		Ito et al.	11/01/2007	
		2007/0287296		Chang	12/13/2007	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP	60-198861	A		10/08/1985		Full
		JP	2000-044236	A		02/15/2000		Full
		JP	2002-289859	A		10/04/2002		Full
		JP	2002-076356	A		03/15/2002		Full
		JP	2004-273732	A		09/30/2004		Full
		JP	2004-273614	A		09/30/2004		Full

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		2008/0038882		Takechi et al.	02/14/2008	
		2008/0038929		Chang	02/14/2008	
		2008/0050595		Nakagawara et al.	02/28/2008	
		2008/0073653		Iwasaki	03/27/2008	
		2008/0083950		Pan et al.	04/10/2008	
		2008/0106191		Kawase	05/08/2008	
		2008/0129195		Ishizaki et al.	06/05/2008	
		2008/0166834		Kim et al.	07/10/2008	
		2008/0182358		Cowdery-Corvan et al.	07/31/2008	
		2008/0224133		Park et al.	09/18/2008	
		2008/0258139		Ito et al.	10/23/2008	
		2008/0258140		Lee et al.	10/23/2008	
		2008/0258141		Park et al.	10/23/2008	
		2008/0258143		Kim et al.	10/23/2008	
		2009/0114910		Chang	05/07/2009	
		7,105,868		Nause et al.	09/12/2006	
		7,402,506		Levy et al.	07/22/2008	
		7,411,209		Endo et al.	08/12/2008	
		7,453,065		Saito et al.	11/18/2008	
		7,453,087		Iwasaki	11/18/2008	
		7,468,304		Kaji et al.	12/23/2008	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP	63-210022	A		08/31/1988		Full
		JP	63-210023	A		08/31/1988		Full
		JP	63-210024	A		08/31/1988		Full
		JP	63-215519	A		09/08/1988		Full
		JP	63-239117	A		10/05/1988		Full
		JP	63-265818	A		11/02/1988		Full
		EP	1 737 044	A		12/27/2006		Eng.
		EP	2 226 847	A		09/08/2010		Eng.

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		2006/0197092		Hoffman et al.	09/07/2006	
		2008/0006877		Mardilovich et al.	01/10/2008	
		2006/0228974		Thelss et al.	10/12/2006	
		2002/0132454		Ohtsu et al.	09/19/2002	
		2009/0152541		Maekawa et al.	06/18/2009	
		2001/0046027		Tai et al.	11/29/2001	
		2006/0035452		Carcia et al.	02/16/2006	
		7,501,293		Ito et al.	03/10/2009	
		7,211,825		Shih et al.	05/01/2007	
		2005/0017302		Hoffman	01/27/2005	
		5,731,856		Kim et al.	03/24/1998	
		2003/0218222		Wager et al.	11/27/2003	
		7,385,224		Ishii et al.	06/10/2008	
		2007/0152217		Lai et al.	07/05/2007	
		2009/0068773		Lai et al.	03/12/2009	
		7,732,819		Akimoto et al.	06/08/2010	
		2006/0043377		Hoffman et al.	03/02/2006	
		2009/0278122		Hosono et al.	11/12/2009	
		2009/0280600		Hosono et al.	11/12/2009	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Fortunato et al., "WIDE-BANDGAP HIGH-MOBILITY ZNO THIN-FILM TRANSISTORS PRODUCED AT ROOM TEMPERATURE," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), September 27, 2004, Vol. 85, No. 13, pp. 2541-2543.	Eng.
		Park et al., "Improvements in the Device Characteristics of Amorphous Indium Gallium Zinc Oxide Thin-Film Transistors by Ar Plasma Treatment," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), June 26, 2007, Vol. 90, No. 26, pp. 262106-1-262106-3.	Eng.

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		Hayashi et al., "42.1: Invited Paper: Improved Amorphous In-Ga-Zn-O TFTs," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, pp. 621-624.	Eng.
		Masuda et al., "Transparent thin film transistors using ZnO as an active channel layer and their electrical properties," J. APPL. PHYS. (JOURNAL OF APPLIED PHYSICS), February 1, 2003, Vol. 93, No. 3, pp. 1624-1630.	Eng.
		Asakuma et al., "Crystallization and Reduction of Sol-Gel-Derived Zinc Oxide Films by Irradiation with Ultraviolet Lamp," JOURNAL OF SOL-GEL SCIENCE AND TECHNOLOGY, 2003, Vol. 26, pp. 181-184.	Eng.
		Nomura et al., "Carrier transport in transparent oxide semiconductor with intrinsic structural randomness probed using single-crystalline $InGaO_3(ZnO)_5$ films," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), September 13, 2004, Vol. 85, No. 11, pp. 1993-1995.	Eng.
		Son et al., "42.4L: Late-News Paper: 4 Inch QVGA AMOLED Driven by the Threshold Voltage Controlled Amorphous GIZO (Ga_2O_3-In_2O_3-ZnO) TFT," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, pp. 633-636.	Eng.
		Van de Walle, "Hydrogen as a Cause of Doping in Zinc Oxide," PHYS. REV. LETT. (PHYSICAL REVIEW LETTERS), July 31, 2000, Vol. 85, No. 5, pp. 1012-1015.	Eng.
		Fung et al., "2-D Numerical Simulation of High Performance Amorphous In-Ga-Zn-O TFTs for Flat Panel Displays," AM-FPD '08 DIGEST OF TECHNICAL PAPERS, July 2, 2008, pp. 251-252, THE JAPAN SOCIETY OF APPLIED PHYSICS.	Eng.
		Park et al., "High performance amorphous oxide thin film transistors with self-aligned top-gate structure," IEDM 09: TECHNICAL DIGEST OF INTERNATIONAL ELECTRON DEVICES MEETING, December 7, 2009, pp. 191-194.	Eng.

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		Nakamura, "Synthesis of Homologous Compound with New Long-Period Structure," NIRIM NEWSLETTER, March 1, 1995, Vol. 150, pp. 1-4.	Full
		Park et al., "42.3: Transparent ZnO Thin Film Transistor for the Application of High Aperture Ratio Bottom Emission AM-OLED Display," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, pp. 629-632.	Eng.
		Orita et al., "Mechanism of Electrical Conductivity of Transparent $InGaZnO_4$," PHYS. REV. B (PHYSICAL REVIEW B), January 15, 2000, Vol. 61, No. 3, pp. 1811-1816.	Eng.
		Nomura et al., "Amorphous Oxide Semiconductors for High-Performance Flexible Thin-Film Transistors," JPN. J. APPL. PHYS. (JAPANESE JOURNAL OF APPLIED PHYSICS), 2006, Vol. 45, No. 5B, pp. 4303-4308.	Eng.
		Janotti et al., "Native Point Defects in ZnO," PHYS. REV. B (PHYSICAL REVIEW. B), October 4, 2007, Vol. 76, No. 16, pp. 165202-1–165202-22.	Eng.
		Park et al., "Electronic Transport Properties of Amorphous Indium-Gallium-Zinc Oxide Semiconductor Upon Exposure to Water," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), 2008, Vol. 92, pp. 072104-1-072104-3.	Eng.
		Hsieh et al., "P-29: Modeling of Amorphous Oxide Semiconductor Thin Film Transistors and Subgap Density of States," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, 2008, Vol. 39, pp. 1277-1280.	Eng.
		Janotti et al., "Oxygen Vacancies in ZnO," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), 2005, Vol. 87, pp. 122102-1-122102-3.	Eng.
		Oba et al., "Defect energetics in ZnO: A hybrid Hartree-Fock density functional study," PHYS. REV. B (PHYSICAL REVIEW B), 2008, Vol. 77, pp. 245202-1-245202-6.	Eng.

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		Orita et al., "Amorphous transparent conductive oxide $InGaO_3(ZnO)_m$ ($m<4$): a Zn 4s conductor," PHILOSOPHICAL MAGAZINE, 2001, Vol. 81, No. 5, pp. 501-515.	Eng.
		Hosono et al., "Working hypothesis to explore novel wide band gap electrically conducting amorphous oxides and examples," J. NON-CRYST. SOLIDS (JOURNAL OF NON-CRYSTALLINE SOLIDS), 1996, Vol. 198-200, pp. 165-169.	Eng.
		Mo et al., "Amorphous Oxide TFT Backplanes for Large Size AMOLED Displays," IDW '08: PROCEEDINGS OF THE 6th INTERNATIONAL DISPLAY WORKSHOPS, December 3, 2008, pp. 581-584.	Eng.
		Kim et al., "High-Performance oxide thin film transistors passivated by various gas plasmas," 214th ECS MEETING, 2008, No. 2317.	Eng.
		Clark et al., "First Principles Methods Using CASTEP," Zeitschrift fur Kristallographie, 2005, Vol. 220, pp. 567-570.	Eng.
		Lany et al., "Dopability, Intrinsic Conductivity, and Nonstoichiometry of Transparent Conducting Oxides," PHYS. REV. LETT. (PHYSICAL REVIEW LETTERS), January 26, 2007, Vol. 98, pp. 045501-1-045501-4.	Eng.
		Park et al., "Dry etching of ZnO films and plasma-induced damage to optical properties," J. VAC. SCI. TECHNOL. B (JOURNAL OF VACUUM SCIENCE & TECHNOLOGY B), March 1, 2003, Vol. 21, No. 2, pp. 800-803.	Eng.
		Oh et al., "Improving the Gate Stability of ZnO Thin-Film Transistors with Aluminum Oxide Dielectric Layers," J. ELECTROCHEM. SOC. (JOURNAL OF THE ELECTROCHEMICAL SOCIETY), 2008, Vol. 155, No. 12, pp. H1009-H1014.	Eng.
		Ueno et al., "Field-Effect Transistor on $SrTiO_3$ with Sputtered Al_2O_3 Gate Insulator," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), September 1, 2003, Vol. 83, No. 9, pp. 1755-1757.	Eng.

Examiner Signature		Date Considered	

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] *(if known)*	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2009/0152506		Umeda et al.	06/18/2009	
		2010/0092800		Itagaki et al.	04/15/2010	
		2010/0109002		Itagaki et al.	05/06/2010	
		2010/0065844		Tokunaga	03/18/2010	
		8,021,917		Akimoto et al.	09/20/2011	
		2011/0318916		Akimoto et al.	12/29/2011	
		8,030,663		Yamazaki et al.	10/04/2011	
		2012/0058599		Yamazaki et al.	03/08/2012	
		8,115,201		Yamazaki et al.	02/14/2012	
		2012/0132910		Yamazaki et al.	05/31/2012	
		2005/0056897		Kawasaki et al.	03/17/2005	
		2006/0027804		Yamazaki et al.	02/09/2006	
		2010/0117086		Akimoto et al.	05/13/2010	
		2009/0114917		Yamazaki et al.	05/07/2009	
		2010/0044711		Imai	02/25/2010	
		2005/0050897		Lewis	03/10/2005	
		2006/0292726		Akimoto et al.	12/28/2006	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] *(if known)*	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001]

The present invention relates to a display device using an oxide semiconductor and a method for manufacturing the same.

2. Description of the Related Art

[0002]

As typically seen in liquid crystal display devices, a thin film transistor formed over a flat plate such as a glass substrate is manufactured using amorphous silicon or polycrystalline silicon. A thin film transistor manufactured using amorphous silicon has low field effect mobility, but can be formed over a larger glass substrate. In contrast, a thin film transistor manufactured using crystalline silicon has high field effect mobility, but due to the necessity of a crystallization step such as laser annealing, such a transistor is not always suitable for being formed over a larger glass substrate.

[0003]

In view of the foregoing, attention has been drawn to a technique in which a thin film transistor is manufactured using an oxide semiconductor and applied to electronic appliances or optical devices. For example, Patent Document 1 and Patent Document 2 disclose a technique in which a thin film transistor is manufactured using zinc oxide or an In-Ga-Zn-O-based oxide semiconductor for forming an oxide semiconductor film and such a transistor is used as a switching element or the like of an image display device.

[0004]

Patent Document 1: Japanese Published Patent Application No. 2007-123861

Patent Document 2: Japanese Published Patent Application No. 2007-096055

SUMMARY OF THE INVENTION

[0005]

It is one object of the present invention to provide a structure by which

electric-field concentration which might occur between a source electrode and a drain electrode in a bottom-gate thin film transistor is relaxed and deterioration of the switching characteristics is suppressed, and a manufacturing method thereof.

[0006]

Further, it is one object of the present invention to provide a structure by which coverage by an oxide semiconductor layer is improved and a manufacturing method thereof.

[0007]

In accordance with the present invention, a bottom-gate thin film transistor in which an oxide semiconductor layer is provided over a source and drain electrodes is manufactured, and angle $\theta 1$ of the side surface of the source electrode which is in contact with the oxide semiconductor layer and angle $\theta 2$ of the side surface of the drain electrode which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the distance from the top edge to the bottom edge in the side surface of each electrode is increased.

[0008]

One embodiment of the present invention disclosed in this specification is a semiconductor device wherein a gate electrode is formed over a substrate having an insulating surface, an insulating layer is formed over the gate electrode, a source and drain electrodes are formed over the insulating layer, an oxide semiconductor layer is formed between their respective side surfaces of the source and drain electrodes, which face each other, so as to overlap with the gate electrode with the insulating layer interposed therebetween, and the angle formed between the surface of the substrate and the side surface of the source electrode and the angle formed between the surface of the substrate and the side surface of the drain electrode are each greater than or equal to 20° and less than 90°.

[0009]

With the above embodiment, at least one of the objects can be achieved.

[0010]

A native oxide film is formed at least on the side surfaces of the source and drain electrodes, which depends on a metal material of the source and drain electrodes.

This native oxide film is formed by exposure to an atmosphere containing oxygen, such as the air, after etching for forming the source and drain electrodes. The native oxide film is also formed with oxygen contained in the atmosphere for deposition of the oxide semiconductor layer after etching for forming the source and drain electrodes.

[0011]

In order to prevent formation of the native oxide film on the electrodes, it is preferable that a buffer layer (also called an n^+ layer) is formed successively without exposure to the air on and in contact with a metal film formed by a sputtering method. This buffer layer is an oxide semiconductor layer which has lower resistance than the oxide semiconductor layer which is formed thereover, and functions as a source and drain regions.

[0012]

In the above-described embodiment, the buffer layer is provided on the top surfaces of the source and drain electrodes and the oxide semiconductor layer is provided on the buffer layer. The buffer layer (also called the n^+ layer) is formed successively without exposure to the air, which prevents a native oxide film from being formed on the top surfaces of the source and drain electrodes.

[0013]

Further, in the bottom-gate thin film transistor, the pathway of a drain current (current pathway in the channel length direction) when the transistor is turned on by applying a voltage which is sufficiently higher than the threshold voltage to the gate electrode starts from the drain electrode and leads to the source electrode through the oxide semiconductor layer in the vicinity of the interface with the gate insulating film.

[0014]

Note that here the channel length of the bottom-gate thin film transistor in which the oxide semiconductor layer is provided over the source and drain electrodes corresponds to the shortest distance between the source and drain electrodes, and is the distance of the part of the oxide semiconductor layer in the vicinity of the interface with the gate insulating film, positioned between the source and drain electrodes.

[0015]

In the case where the n^+ layer is formed on and in contact with the top surface of each of the drain and source electrodes, when the conductivity of the native oxide

film formed on the side surface of each electrode is low, a main pathway of a drain current starts from the drain electrode and leads through the n^+ layer, a part of the oxide semiconductor layer in the vicinity of the interface with the side surface of the drain electrode, a part of the oxide semiconductor layer in the vicinity of the interface with the gate insulating film, a part of the oxide semiconductor layer in the vicinity of the interface with the side surface of the source electrode, and the n^+ layer to the source electrode. As for the oxide semiconductor layer formed by a sputtering method, the film quality in the vicinity of the interface with a surface on which the film is formed tends to be affected by the material of the surface on which the film is formed. The oxide semiconductor layer here has at least three interfaces with different materials: the interface with the n^+ layer, the interface with the side surface of each of the source and drain electrodes, and the interface with the gate insulating film. Therefore, in the oxide semiconductor layer, the interfacial state with the native oxide film on the side surface of the drain electrode is different from the interfacial state with the gate insulating film, so that a part of the oxide semiconductor layer, which is in the vicinity of the interface with the side surface of the drain electrode functions as a first electric-field relaxation region. Similarly, in the oxide semiconductor layer, the interfacial state with the native oxide film on the side surface of the source electrode is different from the interfacial state with the gate insulating film, so that a part of the oxide semiconductor layer, which is in the vicinity of the interface with the side surface of the source electrode functions as a second electric-field relaxation region.

[0016]

As described above, the regions of the oxide semiconductor layer, which overlap with the side surfaces of the source electrode and the drain electrode function as electric-field relaxation regions.

[0017]

With an oxide semiconductor used in this specification, a thin film of a material described as $InMO_3(ZnO)_m$ ($m > 0$) is formed, and a thin film transistor in which the thin film is used as a semiconductor layer is manufactured. Note that M denotes a single metal element or a plurality of metal elements selected from Ga, Fe, Ni, Mn, and Co. For example, M is Ga in some cases, and M includes another metal element in addition to Ga, such as either Ga and Ni or Ga and Fe, in some cases. Moreover, in the

oxide semiconductor, in some cases, a transition metal element such as Fe or Ni or an oxide of the transition metal is contained as an impurity element in addition to the metal element contained as M. In this specification, this thin film is also referred to as an In-Ga-Zn-O-based non-single-crystal film.

[0018]

An amorphous structure is observed by X-ray diffraction (XRD), as the crystal structure of the In-Ga-Zn-O-based non-single-crystal film. Note that heat treatment is performed on the In-Ga-Zn-O non-single-crystal film to be observed at 200 to 500 °C, typically 300 to 400 °C, for 10 minutes to 100 minutes after the film deposition by a sputtering method.

[0019]

The angle θ1 of the side surface of the source electrode which is in contact with the oxide semiconductor layer and the angle θ2 of the side surface of the drain electrode which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the distance from the top edge to the bottom edge of the electrode in the side surface of each electrode is increased, thereby increasing the lengths of the first and second electric-field relaxation regions to relax the electric-field concentration. Moreover, the distance from the top edge to the bottom edge of the electrode in the side surface of each electrode can also be increased by increasing the thickness of the electrode.

[0020]

Further, in the case where the oxide semiconductor layer is formed by a sputtering method, if the side surface of the electrode is vertical to the substrate surface, the thickness of a part of the oxide semiconductor layer, which is formed on the side surface of the electrode might be smaller than that of a part of the same, which is formed on the top surface of the electrode. Therefore, the angle θ1 of the side surface of the source electrode which is in contact with the oxide semiconductor layer and the angle θ2 of the side surface of the drain electrode which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the thickness uniformity of the oxide semiconductor layer can be improved even over the side surface of each electrode and electric-field concentration can be relaxed.

[0021]

Further, in the case where the straight line which connects the top edge of the side surface of the source electrode to the bottom edge of the side surface of the source electrode substantially coincides with the slope of the side surface of the source electrode as shown in FIG. 1, it can be said that the source electrode has a tapered shape, and the angle θ1 of the side surface of the source electrode with respect to the surface of the substrate can also be called a first taper angle. Similarly, in the case where the straight line which connects the top edge of the side surface of the drain electrode to the bottom edge of the side surface of the drain electrode substantially coincides with the slope of the slope of the side surface of the drain electrode, it can be said that the drain electrode has a tapered shape, and the angle θ2 of the side surface of the drain electrode with respect to the surface of the substrate can also be called a second taper angle.

[0022]

Further, the present invention is not limited to the shape in which the side surface of the electrode has only one angle, the side surface of the electrode may have a step as long as the angle θ1 of the side surface of the bottom edge of the source electrode and the angle θ2 of the side surface of the bottom edge of the drain electrode each are greater than or equal to 20° and less than 90°.

[0023]

Another embodiment of the present invention is a semiconductor device wherein a gate electrode is formed over a substrate having an insulating surface, an insulating layer is formed over the gate electrode, a source and drain electrodes are formed over the insulating layer, an oxide semiconductor layer is formed between their respective side surfaces of the source and drain electrodes, which face each other, so as to overlap with the gate electrode with the insulating layer interposed therebetween, and the angle formed between the surface of the substrate and the side surface of a bottom edge of the source electrode and the angle formed between the surface of the substrate and the side surface of a bottom edge of the drain electrode each are greater than or equal to 20° and less than 90°.

[0024]

In the above embodiment, the angle formed between the surface of the

substrate and the side surface of the bottom edge of the source electrode is made to be different from the angle formed between the surface of the substrate and the side surface at a top edge of the source electrode. In addition, the angle formed between the surface of the substrate and the side surface of the bottom edge of the drain electrode is made to be different from the angle formed between the surface of the substrate and the side surface at a top edge of the drain electrode. The cross section of the side surface of the source electrode and that of the side surface of the drain electrode, which face each other with the oxide semiconductor layer interposed therebetween, have substantially the same shape as each other because the same etching step is performed thereon.

[0025]

For example, their respective angles of the side surfaces of the top edges of the source electrode and the drain electrode may be set to 90° so that their respective angles of the side surfaces of the bottom edges of the source electrode and the drain electrode are different from their respective angles of the side surfaces of the top edges of the source electrode and the drain electrode. By increasing their respective angles of the side surfaces of the top edges of the source electrode and the drain electrode to be greater than their respective angles of the side surfaces of the bottom edges of the source electrode and the drain electrodes, the interval between masks for forming the source and drain electrodes can be designed to be small, which can result in shorter design of the channel length, for example, a channel length of 1 to 10 μm.

[0026]

The side surface of each of the source and drain electrodes may have a curved surface; for example, in the cross-sectional shape of each of the source and drain electrodes, the bottom edge portion of the electrode may have one curved surface at least partly which originates from a center of a curvature radius, which is positioned outside the electrode. The side surface of each of the source and drain electrodes may have a cross-sectional shape which spreads toward the substrate from the top surface of each electrode.

[0027]

The electrodes, which can have various cross-sectional shapes as described

above, are formed by dry etching or wet etching. As an etching apparatus used for the dry etching, an etching apparatus using a reactive ion etching method (an RIE method), or a dry etching apparatus using a high-density plasma source such as ECR (electron cyclotron resonance) or ICP (inductively coupled plasma) can be used. As a dry etching apparatus by which uniform electric discharge can be obtained over a wider area as compared to an ICP etching apparatus, there is an ECCP (enhanced capacitively coupled plasma) mode apparatus in which an upper electrode is grounded, a high-frequency power source at 13.56 MHz is connected to a lower electrode, and further a low-frequency power source at 3.2 MHz is connected to the lower electrode. This ECCP mode etching apparatus can be applied even when, as the substrate, a substrate, the size of which exceeds 3 m of the tenth generation, is used, for example.

[0028]

Each of the source and drain electrodes may be a single layer or a stacked layer of at least two layers formed using two different materials.

[0029]

Another embodiment of the present invention, which relates to the manufacturing method to realize the above structure, is a method for manufacturing a semiconductor device, wherein a gate electrode is formed over a substrate having an insulating surface, a gate insulating layer is formed to cover the gate electrode, a conductive layer and a buffer layer are formed to be stacked over the gate insulating layer without exposure to the air, the conductive layer and the buffer layer are selectively etched to form a source and drain electrodes each having a side surface which forms an angle greater than or equal to 20° and less than 90° with respect to the surface of the substrate, and an oxide semiconductor layer is formed over the gate insulating layer, the source electrode, and the drain electrode.

[0030]

In the above-described embodiment which relates to the manufacturing method, the buffer layer contains indium, gallium, and zinc, and can be used using the same target as a target used for the oxide semiconductor layer formed over the buffer layer. The buffer layer and the oxide semiconductor layer can be separately formed by changing the film deposition atmosphere, and the manufacturing cost can be decreased by using the same target.

[0031]

According to the above-described embodiment which relates to the manufacturing method, the conductive layer and the buffer layer are formed to be stacked over the gate insulating layer without exposure to the air, that is, successive film deposition is performed.

[0032]

In the above-described embodiment which relates to the manufacturing method, the conductive layer, which forms the source and drain electrodes, is formed using a metal material such as aluminum, tungsten, chromium, tantalum, titanium, or molybdenum, or an alloy material thereof. The conductive layer may be a stacked layer of at least two layers; for example, a stacked layer in which an aluminum layer as a bottom layer and a titanium layer as an upper layer are stacked, a stacked layer in which a tungsten layer as a bottom layer and a molybdenum layer as an upper layer are stacked, a stacked layer in which an aluminum layer as a bottom layer and a molybdenum layer as an upper layer are stacked, or the like can be used.

[0033]

Successive film deposition in this specification means that a series of steps from a first film deposition step by a sputtering method to a second film deposition step by a sputtering method are performed by controlling an atmosphere in which a process substrate is disposed so that it is constantly in vacuum or an inert gas atmosphere (a nitrogen atmosphere or a rare gas atmosphere) without being exposed to a contaminated atmosphere such as the air. By the successive film deposition, film deposition can be performed on the process substrate which has been cleaned, without further adhesion of moisture or the like.

[0034]

Performing the series of steps from the first deposition step to the second deposition step in the same chamber is within the scope of the successive film deposition in this specification.

[0035]

In addition, the following is also within the scope of the successive film deposition in this specification: in the case of performing the series of steps from the first film deposition step to the second film deposition step in different chambers, the

process substrate is transferred to another chamber without being exposed to the air after the first film deposition step and subjected to the second film deposition.

[0036]

Further, the following is also within the scope of the successive film deposition in this specification: a substrate transfer step, an alignment step, a slow-cooling step, a step of heating or cooling the substrate to a temperature which is necessary for the second film deposition step, or the like is provided between the first film deposition step and the second film deposition step.

[0037]

However, the case in which a step in which liquid is used, such as a cleaning step, wet etching, or resist formation, is provided between the first film deposition step and the second film deposition step is not within the scope of the successive film deposition in this specification.

[0038]

In this specification, a word which expresses a direction, such as "over", "below", "side", "horizontal", or "vertical", indicates a direction based on the substrate surface in the case where a device is provided over the surface of the substrate.

[0039]

Note that the ordinal numerals such as "first" and "second" in this specification are used for convenience and do not denote the order of steps or the stacking order of layers. In addition, the ordinal numbers in this specification do not denote particular names which specify the present invention.

[0040]

The angle formed by the surface of the substrate and the side surface of the source electrode and the angle formed by the surface of the substrate and the side surface of the drain electrode are adjusted, so that the coverage by the oxide semiconductor layer provided over the source and drain electrodes is improved.

[0041]

An electric-field relaxation region is provided, so that electric-field concentration which might occur between the source and drain electrodes is relaxed and degradation of the switching characteristics of the thin film transistor is suppressed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0042]

FIG. 1 is a cross-sectional view showing one example of a semiconductor device.

FIG. 2 is a cross-sectional view showing one example of a semiconductor device.

FIGS. 3A and 3B are cross-sectional views showing one example of a method for manufacturing a semiconductor device.

FIGS. 4A to 4C are cross-sectional views showing one example of a method for manufacturing a semiconductor device.

FIG. 5 is a top view showing one example of a method for manufacturing a semiconductor device.

FIG. 6 is a top view showing one example of a method for manufacturing a semiconductor device.

FIG. 7 is a top view showing one example of a method for manufacturing a semiconductor device.

FIG. 8 is a top view showing one example of a method for manufacturing a semiconductor device.

FIGS. 9A1 and 9B1 are views showing one example of a cross-sectional view of a terminal portion and FIGS. 9A2 and 9B2 are views showing one example of a top view of the terminal portion.

FIG. 10 is a top view showing one example of a method for manufacturing a semiconductor device.

FIG. 11 is a cross-sectional view showing one example of a semiconductor device.

FIGS. 12 A and 12B are views showing examples of a block diagram of semiconductor device.

FIG. 13 is a diagram showing one example of a structure of a signal line driver circuit.

FIG. 14 is a timing chart showing an operation of a signal line driver circuit.

FIG. 15 is a timing chart showing one example of an operation of a signal line driver circuit.

FIG. 16 is a diagram showing one example of a structure of a shift register.

FIG. 17 is a diagram showing a connection structure of the flip-flop shown in FIG. 16.

FIG. 18 is a diagram showing one example of a pixel equivalent circuit of a semiconductor device.

FIGS. 19A to 19C are cross-sectional views showing examples of a semiconductor device.

FIG. 20A1 and 20A2 are top views showing examples of a semiconductor device, and FIG. 20B is a cross-sectional view showing one example of a semiconductor device.

FIG. 21 is a cross-sectional view showing one example of a semiconductor device.

FIGS. 22A and 22B are a top view and a cross-sectional view showing one example of a semiconductor device.

FIGS. 23A and 23B are views showing examples of a usage pattern of electronic paper.

FIG. 24 is an external view of one example of an electronic book reader.

FIGS. 25A and 25B are external views showing respective examples of a television device and a digital photo frame.

FIGS. 26A and 26B are external views showing examples of an amusement machine.

FIG. 27 is an external view showing one example of a mobile phone.

FIG. 28 is a graph showing one example of electrical characteristics of a thin film transistor.

FIG. 29 is a top view of a thin film transistor manufactured to measure the electrical characteristics.

FIGS. 30A to 30C are cross-sectional views showing a process for manufacturing a sample.

FIGS. 31A and 31B are a photograph and a cross-sectional view showing a part of the cross-section of a sample.

FIG. 32A is a view showing one example of a cross-sectional structure of a semiconductor device, FIG. 32B is an equivalent circuit diagram thereof, and FIG. 32C

is a top view thereof.

FIGS. 33A to 33C are cross-sectional views showing structures of a calculation model.

FIG. 34 is a graph showing calculation results.

FIG. 35 is a graph showing calculation results.

FIG. 36 is a graph showing calculation results.

FIGS. 37A and 37B are graphs showing calculation results (comparative examples).

DETAILED DESCRIPTION OF THE INVENTION

[0043]

Embodiments and examples of the present invention will be hereinafter described.

[Embodiment 1]

[0044]

The case in which a thin film transistor 170 is provided over a substrate is illustrated in FIG. 1. FIG. 1 is one example of a cross-sectional view of a thin film transistor.

[0045]

A gate electrode 101 provided over a substrate 100 having an insulating surface is covered with a gate insulating layer 102, and a first wiring and a second wiring are provided over the gate insulating layer 102 which overlaps with the gate electrode 101. A buffer layer is provided over each of the first wiring and the second wiring which function as a source electrode layer 105a and a drain electrode layer 105b. A first buffer layer 104a is provided over the source electrode layer 105a, and a second buffer layer 104b is provided over the drain electrode layer 105b. An oxide semiconductor layer 103 is provided over the first buffer layer 104a and the second buffer layer 104b.

[0046]

In FIG. 1, as the substrate 100 having a light-transmitting property, a glass substrate of barium borosilicate glass, aluminoborosilicate glass, or the like typified by 7059 glass, 1737 glass, or the like manufactured by Corning, Inc. can be used.

[0047]

The gate electrode 101 is a single layer or a stacked layer made of different metal materials. As a material of the gate electrode 101, a metal material (an element selected from aluminum (Al), copper (Cu), titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc), or an alloy including the element as a component) is used. The angle of the side surface of the gate electrode 101 is set to be greater than or equal to 20° and less than 90°. The gate electrode 101 is formed by etching so as to have a tapered shape at least in the edge portion thereof.

[0048]

The gate insulating layer 102 may be formed to have a single-layer structure or a stacked-layer structure using an insulating film obtained by a sputtering method or a plasma CVD method, such as a silicon oxide film, a silicon oxynitride film, a silicon nitride film, an aluminum oxide film, or a tantalum oxide film. It is preferable to select a material which can provide an etching selectivity which is high enough for the etching for forming the source electrode layer 105a and the drain electrode layer 105b which are formed over the gate insulating layer 102. In etching the source electrode layer 105a and the drain electrode layer 105b, the surface of the gate insulating layer 102 may be etched off by about 20 nm at a maximum; and it is preferable to etch off the superficial layer of the gate insulating layer 102 by a small thickness in order to remove an etching residue of the metal material.

[0049]

The source electrode layer 105a and the drain electrode layer 105b each are a single layer or a stacked layer made of different metal materials. As a material of each of the source electrode layer 105a and the drain electrode layer 105b, a metal material (an element selected from aluminum (Al), copper (Cu), titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc), or an alloy including the element as a component) is used.

[0050]

With respect to the cross-sectional shape of the source electrode layer 105a, as shown in FIG. 1, angle θ1 formed between the surface of the substrate and the side surface of the source electrode layer 105a is set to be greater than or equal to 20° and

less than 90°. Similarly, with respect to the cross-sectional shape of the drain electrode layer 105b, as shown in FIG. 1, angle θ2 formed between the surface of the substrate and the side surface of the drain electrode layer 105b is set to be greater than or equal to 20° and less than 90°. The angle θ1 and the angle θ2 are substantially the same as each other because the same etching step (dry etching or wet etching) is performed thereon. The angle θ1 of the side surface of the source electrode layer 105a which is in contact with the oxide semiconductor layer and the angle θ2 of the side surface of the drain electrode layer 105b which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the distance from the top edge to the bottom edge in the side surface of each of the source electrode layer 105a and the drain electrode layer 105b is increased.

[0051]

Although the angles θ1 and θ2 are described when it is assumed that the plane of the back surface of the substrate is the substrate surface in FIG. 1, the present invention is not limited thereto, and the angles θ1 and θ2 are not changed even when it is assumed that the plane of the front surface of the substrate is the substrate surface because the plane of the back surface of the substrate is in parallel to the plane of the front surface of the substrate.

[0052]

The oxide semiconductor layer 103 is formed over the source electrode layer 105a and the drain electrode layer 105b having the above-described shapes. The oxide semiconductor layer 103 is formed as follows: film deposition is performed using an oxide semiconductor target including In, Ga, and Zn (In_2O_3:Ga_2O_3:ZnO = 1:1:1), under a condition in which the distance between the substrate and the target is 170 mm, the pressure is 0.4 Pa, and the direct-current (DC) power source is 0.5 kW, in an argon atmosphere containing oxygen, and a resist mask is formed and the deposited film is selectively etched off to remove the unnecessary portion thereof. Note that it is preferable to use a pulsed direct-current (DC) power source with which dust can be reduced and thickness distribution can be evened. The thickness of the oxide semiconductor film is set to be 5 to 200 nm. In this embodiment, the thickness of the oxide semiconductor film is 100 nm.

[0053]

It is preferable to provide the first buffer layer 104a between the source electrode layer 105a and the oxide semiconductor layer 103. It is preferable to provide the second buffer layer 104b between the drain electrode layer 105b and the oxide semiconductor layer 103.

[0054]

The first buffer layer 104a and the second buffer layer 104b each are an oxide semiconductor layer (n^+ layer) which have lower resistance than the oxide semiconductor layer 103, and function as a source and drain regions.

[0055]

In this embodiment, the n^+ layers are each formed as follows: film deposition is performed by a sputtering method using a target in which In_2O_3:Ga_2O_3:ZnO = 1:1:1, under a condition in which the pressure is 0.4 Pa, the power is 500 W, the deposition temperature is room temperature, and the argon-gas flow rate is 40 sccm. Despite the use of the target in which In_2O_3:Ga_2O_3:ZnO = 1:1:1, an In-Ga-Zn-O-based non-single-crystal film including crystal grains with a size of 1 to 10 nm may be formed immediately after the start of the film deposition. Note that it can be said that the presence or absence of crystal grains or the density of crystal grains can be adjusted and the diameter size can be adjusted within the range of 1 to 10 nm by appropriate adjustment of the composition ratio in the target, the film deposition pressure (0.1 to 2.0 Pa), the power (250 to 3000 W: 8 inches ø), the temperature (room temperature to 100 °C), the reactive sputtering deposition conditions, and/or the like. The second In-Ga-Zn-O-based non-single-crystal film has a thickness of 5 to 20 nm. Needless to say, when the film includes crystal grains, the size of each crystal grain does not exceed the thickness of the film. In this embodiment, the thickness of the second In-Ga-Zn-O-based non-single-crystal film is 5 nm.

[0056]

By forming and stacking the conductive film which forms the source electrode layer 105a and the drain electrode layer 105b and the oxide semiconductor film which forms the n^+ layers without exposing to the air, by a sputtering method, the source and drain electrode layers can be prevented from being exposed to the air during the manufacturing process, so that dust can be prevented from attaching thereto.

[0057]

As for the oxide semiconductor layer 103 formed by a sputtering method, the film quality in the vicinity of the interface with a surface on which the film is formed tends to be affected by the material of the surface on which the film is formed. The oxide semiconductor layer here has at least three interfaces with different materials: the interface with the n^+ layer, the interface with the side surface of each of the source and drain electrodes, and the interface with the gate insulating film. Therefore, in the oxide semiconductor layer 103, the interfacial state with the native oxide film on the side surface of the drain electrode layer is different from the interfacial state with the gate insulating film, so that a part of the oxide semiconductor layer, which is in the vicinity of the interface with the side surface of the drain electrode layer functions as the first electric-field relaxation region 106a. Similarly, in the oxide semiconductor layer, the interfacial state with the native oxide film on the side surface of the source electrode is different from the interfacial state with the gate insulating film, so that a part of the oxide semiconductor layer, which is in the interface vicinity with the side surface of the source electrode functions as the second electric-field relaxation region 106b. The angle θ1 of the side surface of the source electrode which is in contact with the oxide semiconductor layer and the angle θ2 of the side surface of the drain electrode which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the distance from the top edge to the bottom edge of the electrode in the side surface of each electrode is increased, thereby increasing length L1 of the first electric-field relaxation region 106a and length L2 of the second electric-field relaxation region 106b to relax the electric-field concentration. The distance from the top edge to the bottom edge of the electrode in the side surface of each electrode can also be increased by increasing the thickness of the electrode.

[0058]

Further, in the case where the oxide semiconductor layer 103 is formed by a sputtering method, if the side surface of the electrode is vertical to the substrate surface, the thickness of a part of the oxide semiconductor layer 103, which is formed on the side surface of the electrode might be smaller than that of a part of the same, which is formed on the top surface of the electrode. Therefore, the angle θ1 of the side surface

of the source electrode which is in contact with the oxide semiconductor layer and the angle θ2 of the side surface of the drain electrode which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the thickness uniformity of the oxide semiconductor layer can be improved even over the side surface of each electrode, a partial reduction in the thickness of the oxide semiconductor layer 103 can be suppressed, and electric-field concentration can be relaxed.

[Embodiment 2]

[0059]

The case where the straight line which connects the top edge of the side surface of the source electrode layer (or the drain electrode layer) to the bottom edge of the side surface of the source electrode layer (or the drain electrode layer) substantially coincides with the slope of the side surface of the source electrode layer (or the drain electrode layer) is illustrated in FIG. 1. In Embodiment 2, the case where the side surface of a source electrode layer (or a drain electrode layer) has a step will be described using FIG. 2. The side surface of the electrode may have a step as long as angle θ1 of the side surface of the bottom edge of the source electrode layer and angle θ2 of the side surface of the bottom edge of the drain electrode layer each are greater than or equal to 20° and less than 90°. Note that, in FIG. 2, the same reference numerals are used for the portions that are common to those in FIG. 1.

[0060]

A gate electrode 101 provided over a substrate 100 having an insulating surface is covered with a gate insulating layer 102, and a first wiring and a second wiring are provided over the gate insulating layer 102 which overlaps with the gate electrode 101. A buffer layer is provided over each of the first wiring and the second wiring which function as a source electrode layer 405a and a drain electrode layer 405b. A first buffer layer 404a is provided over the source electrode 405a, and a second buffer layer 404b is provided over the drain electrode layer 405b. An oxide semiconductor layer 403 is provided over the first buffer layer 404a and the second buffer layer 404b.

[0061]

The substrate 100 having an insulating surface, the gate electrode 101, and the

gate insulating layer 102 are the same as in Embodiment 1, and specific description thereof is omitted in this embodiment.

[0062]

The source electrode layer 405a and the drain electrode layer 405b each are a single layer or a stacked layer made of different metal materials. As a material of each of the source electrode layer 405a and the drain electrode layer 405b, a metal material (an element selected from aluminum (Al), copper (Cu), titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc), or an alloy including the element as a component) is used.

[0063]

Described in this embodiment is the case where a single layer of a tungsten film with a thickness of 100 nm is used as the source electrode layer 405a and the drain electrode layer 405b, and the side surface shapes of the source electrode layer 405a and the drain electrode layer 405b shown in FIG. 2 are formed by using an ICP etching apparatus using a coiled antenna.

[0064]

In this embodiment, etching is performed by generating plasma under the following condition: the gas flow rate of CF_4 is 25 sccm, the gas flow rate of Cl_3 is 25 sccm, the gas flow rate of O_2 is 10 sccm, and an RF (13.56 MHz) power of 500 W is applied to a coiled electrode at a pressure of 1.5 Pa. An RF (13.56 MHz) power of 10 W is applied to the substrate side (sample stage), which means that a negative self-bias voltage is substantially applied thereto. This etching is stopped when at least the gate insulating film 102 is exposed to some extent, thereby forming the side surface of the electrode, which has a step.

[0065]

By the above etching condition, with respect to the cross-sectional shape of the source electrode layer 405a, the angle θ1 formed between the surface of the substrate and the bottom edge of the side surface of the source electrode layer 405a can be made to be greater than or equal to 20° and less than 90°; and as shown in FIG. 2, θ1 is about 40°. Further, the angle formed between the surface of the substrate and the top edge of the side surface of the source electrode layer 405a is about 90°. The cross section of

the side surface of the source electrode layer 405a and that of the side surface of the drain electrode layer 405b, which face each other with the oxide semiconductor layer 403 interposed therebetween, have substantially the same shape as each other because the same etching step is performed thereon.

[0066]

By increasing their respective angles of the side surfaces of the top edges of the source electrode layer 405a and the drain electrode layer 405b to be greater than their respective angles of the side surfaces of the bottom edges of the source electrode layer 405a and the drain electrode layer 405b, the interval between masks for forming the source and drain electrode layers 405a and 405b can be designed to be small, which can result in shorter design of the channel length, for example, a channel length of 1 to 10 μm.

[0067]

The present invention is not limited to the above-described method, and a step can also be formed in the side surface of each electrode by the following: materials having different etching rates of an etching gas, which form the source electrode layer 405a and the drain electrode layer 405b, are stacked such that a material layer having a low etching rate and a material layer having a high etching rate are stacked as a lower layer and an upper layer respectively, and etching is performed thereon.

[0068]

The two side surfaces of the electrodes which face each other with the oxide semiconductor layer 403 interposed therebetween each have a step, so that the distance from the top edge to the bottom edge of the electrode in the side surface of each electrode is increased, thereby increasing length L3 of a first electric-field relaxation region 406a and length L4 of a second electric-field relaxation region to relax the electric-field concentration.

[0069]

In order to further increase the distance from the top edge to the bottom edge of the electrode in the side surface of each of the source electrode layer and the drain electrode layer, wet etching may be performed after the above-described dry etching to provide a curved surface partly for the side surfaces of the electrodes which face each other with the oxide semiconductor layer 403 interposed therebetween.

[0070]

Alternatively, instead of the above-described dry etching, the source electrode layer and the drain electrode layer may be formed by wet etching so that the angle θ1 of the side surface of the bottom edge of the source electrode layer and the angle θ2 of the side surface of the bottom edge of the drain electrode layer each are greater than or equal to 20° and less than 90°. The side surface of each of the source and drain electrode layers may have a cross-sectional shape which spreads toward the substrate from the top surface of each electrode layer.

[0071]

This embodiment can be combined with Embodiment 1, as appropriate.

[Embodiment 3]

[0072]

In this embodiment, a thin film transistor and a manufacturing process thereof are described with reference to FIGS. 3A and 3B, 4A to 4C, 5 to 8, and FIGS. 9A1 and 9A2 and 9B1 and 9B2.

[0073]

In FIG. 3A, as a substrate 100 having a light-transmitting property, a glass substrate of barium borosilicate glass, aluminoborosilicate glass, or the like can be used.

[0074]

Then, a conductive layer is formed over the entire surface of the substrate 100, a first photolithography step is performed to form a resist mask, and an unnecessary portion is removed by etching to form wirings and an electrode (a gate wiring including a gate electrode 101, a capacitor wiring 108, and a first terminal 121). At this time, the etching is performed so that at least the edge portion of the gate electrode 101 is tapered. FIG. 3A is a cross-sectional view at this stage. A top view at this stage corresponds to FIG. 5.

[0075]

The gate wiring including the gate electrode 101, the capacitor wiring 108, and the first terminal 121 in a terminal portion are each formed using an element selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), aluminum (Al), and copper (Cu), or an alloy including the element as

a component, an alloy film in which the elements are combined, or a nitride including the element as a component. Among these, it is preferable to use a low-resistance conductive material such as aluminum (Al) or copper (Cu), but however, since aluminum itself has disadvantages such as low heat resistance and a tendency to be corroded, the following is used to form them: an element selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), and neodymium (Nd), aluminum (Al), and copper (Cu), an alloy film including a combination of any or all of these elements, or a nitride including the element as a component.

[0076]

Then, a gate insulating layer 102 is formed entirely over the gate electrode 101. The gate insulating layer 102 is formed with a thickness of 50 to 250 nm by a sputtering method or the like.

[0077]

For example, as the gate insulating layer 102, a 100-nm-thick silicon oxide film is formed by a sputtering method. The gate insulating layer 102 is not limited to such a silicon oxide film and may be a single layer or a stacked layer using another insulating film such as a silicon oxynitride film, a silicon nitride film, an aluminum oxide film, or a tantalum oxide film.

[0078]

Next, a conductive film is formed using a metal material over the gate insulating layer 102 by a sputtering method or a vacuum evaporation method. As the material of the conductive film, there are an element selected from Al, Cr, Ta, Ti, Mo, and W, an alloy including any of these elements as a component, an alloy film including a combination of any or all of these elements, and the like. In this embodiment, the conductive film is formed by stacking an aluminum (Al) film and a titanium (Ti) film in this order. Alternatively, the conductive film may have a three-layer structure in which a titanium film is stacked over a tungsten film. Further alternatively, the conductive film may have a single-layer structure of a titanium film or an aluminum film including silicon.

[0079]

Next, a first oxide semiconductor film (a first In-Ga-Zn-O-based non-single-crystal film) is formed over the conductive film by a sputtering method. In

this embodiment, the first oxide semiconductor film is formed as follows: film deposition is performed by a sputtering method using a target in which In_2O_3:Ga_2O_3:ZnO = 1:1:1, under a condition in which the pressure is 0.4 Pa, the power is 500 W, the deposition temperature is room temperature, and the argon-gas flow rate is 40 sccm. Despite the use of the target in which In_2O_3:Ga_2O_3:ZnO = 1:1:1, an In-Ga-Zn-O-based non-single-crystal film including crystal grains with a size of 1 to 10 nm may be formed immediately after the start of the film deposition. Note that it can be said that the presence or absence of crystal grains or the density of crystal grains can be adjusted and the diameter size can be adjusted within the range of 1 to 10 nm by appropriate adjustment of the composition ratio in the target, the film deposition pressure (0.1 to 2.0 Pa), the power (250 to 3000 W: 8 inches ø), the temperature (room temperature to 100 °C), the reactive sputtering deposition conditions, and/or the like. The first In-Ga-Zn-O-based non-single-crystal film has a thickness of 5 to 20 nm. Needless to say, when the film includes crystal grains, the size of the crystal grains does not exceed the thickness of the film. In this embodiment, the thickness of the first In-Ga-Zn-O-based non-single-crystal film is 5 nm.

[0080]

Next, a second photolithography step is performed to form a resist mask, and the first In-Ga-Zn-O-based non-single-crystal film is etched. In this embodiment, wet etching using ITO07N (manufactured by Kanto Chemical Co., Inc.) is performed to remove an unnecessary portion in a pixel portion, so that first In-Ga-Zn-O-based non-single-crystal films 111a and 111b are formed. The etching here is not limited to wet etching and may be dry etching.

[0081]

Next, with use of the same resist mask as used for the etching of the first In-Ga-Zn-O-based non-single-crystal film, an unnecessary portion is removed by etching to form a source electrode layer 105a and a drain electrode layer 105b. Wet etching or dry etching is used as the etching method at this time. Here, dry etching using a mixed gas of $SiCl_4$, Cl_2, and BCl_3 is performed to etch the conductive film in which the Al film and the Ti film are stacked, so that a source electrode layer 105a and a drain electrode layer 105b are formed. The cross-section at this stage is illustrated in FIG. 3B. FIG. 6 is a top view at this stage.

[0082]

By this etching, angle θ1 of the side surface of the source electrode layer 105a and angle θ2 of the side surface of the drain electrode layer 105b which are in contact with an oxide semiconductor layer formed later are made to be greater than or equal to 20° and less than 90°. Tapered shapes of the side surfaces of the electrodes which face each other with the oxide semiconductor layer interposed therebetween enable respective regions of the oxide semiconductor layer, which overlap with the side surfaces of the source electrode layer and the drain electrode layer to function as electric-field relaxation regions.

[0083]

In the second photolithography process, a second terminal 122 formed using the same material as the material of the source electrode layer 105a and the drain electrode layer 105b remains in a terminal portion. Note that the second terminal 122 is electrically connected to a source wiring (a source wiring including the source electrode layer 105a). In the terminal portion, a first In-Ga-Zn-O-based non-single-crystal film 123 remains over the second terminal 122 to overlap with the second terminal 122.

[0084]

In a capacitor portion, a capacitor electrode layer 124 which is made from the same material as the material of the source electrode layer 105a and the drain electrode layer 105b remains. In addition, in the capacitor portion, a first In-Ga-Zn-O-based non-single-crystal film 111c remains over the capacitor electrode layer 124 to overlap with capacitor electrode layer 124.

[0085]

Next, the resist mask is removed, and then, a second oxide semiconductor film (a second In-Ga-Zn-O-based non-single-crystal film in this embodiment) formed without exposure to the air. Formation of the second In-Ga-Zn-O-based non-single-crystal film without exposure to the air after the plasma treatment is effective in preventing dust and the like from attaching to the interface between the gate insulating layer and the semiconductor film. In this embodiment, the second In-Ga-Zn-O-based non-single-crystal film is formed in an argon or oxygen atmosphere

using an oxide semiconductor target having a diameter of 8 inches and containing In, Ga, and Zn (In_2O_3:Ga_2O_3:ZnO = 1:1:1), with the distance between the substrate and the target set to 170 mm, under a pressure of 0.4 Pa, and with a direct-current (DC) power source of 0.5 kW. Note that it is preferable to use a pulsed direct-current (DC) power source with which dust can be reduced and thickness distribution can be evened. The second In-Ga-Zn-O-based non-single-crystal film is formed to have a thickness of 5 to 200 nm. In this embodiment, the thickness of the second In-Ga-Zn-O-based non-single-crystal film is 100 nm.

[0086]

The film deposition condition of the second In-Ga-Zn-O-based non-single-crystal film is different from that of the first In-Ga-Zn-O-based non-single-crystal film, thereby forming the second In-Ga-Zn-O-based non-single-crystal film to have a higher electrical resistance than the first In-Ga-Zn-O-based non-single-crystal film. For example, the second In-Ga-Zn-O-based non-single-crystal film is formed under a condition where the ratio of an oxygen gas flow rate to argon gas flow rate is higher than the ratio of an oxygen gas flow rate to an argon gas flow rate under the deposition condition of the first In-Ga-Zn-O-based non-single-crystal film. Specifically, the first In-Ga-Zn-O-based non-single-crystal film is formed in a rare gas (e.g., argon or helium) atmosphere (or an atmosphere, less than or equal to 10 % of which is an oxygen gas and greater than or equal to 90 % of which is an argon gas), and the second In-Ga-Zn-O-based non-single-crystal film is formed in an oxygen atmosphere (or an atmosphere in which the ratio of an oxygen gas flow rate to an argon gas flow rate is 1:1 or higher).

[0087]

Then, heat treatment is preferably performed at 200 to 600 °C, typically, 300 to 500 °C. In this embodiment, heat treatment is performed under a nitrogen atmosphere or the air in a furnace at 350 °C for 1 hour. Through this heat treatment, rearrangement at the atomic level occurs in the In-Ga-Zn-O-based non-single-crystal film. Because strain energy which inhibits carrier movement is released by the heat treatment, the heat treatment (including optical annealing) is important. There is no particular limitation on the timing of heat treatment as long as it is performed after formation of the second

In-Ga-Zn-O-based non-single-crystal film, and for example, heat treatment may be performed after formation of a pixel electrode.

[0088]

Next, a third photolithography process is performed to form a resist mask, and an unnecessary portion is removed by etching, so that a semiconductor layer 103 is formed. In this embodiment, wet etching using ITO07N (manufactured by Kanto Chemical Co., Inc.) is performed to remove the second In-Ga-Zn-O-based non-single-crystal film, so that the semiconductor layer 103 is formed. In the case of the removal by wet etching, an oxide semiconductor can be reproduced using a waste solution of the etching to use for manufacturing a target again.

[0089]

Indium or gallium contained in an oxide semiconductor, which is known as a rare metal, can achieve resource saving and cost reduction of a product formed using an oxide semiconductor by recycle of it.

[0090]

The same etchant is used for the first In-Ga-Zn-O-based non-single-crystal film and the second In-Ga-Zn-O-based non-single-crystal film, and therefore, the first In-Ga-Zn-O-based non-single-crystal film is removed by this etching. Therefore, a side surface of the first In-Ga-Zn-O-based non-single-crystal film, which is covered with the second In-Ga-Zn-O-based non-single-crystal film is protected whereas parts of the first In-Ga-Zn-O-based non-single-crystal films 111a and 111b, which are exposed to the outside are etched, so that a first buffer layer 104a and a second buffer layer 104b are formed. The etching of the semiconductor layer 103 is not limited to wet etching and may be dry etching. Through the above steps, a thin film transistor 170 including the semiconductor layer 103 as a channel formation region can be manufactured. A cross-sectional view at this stage is FIG. 4A. A top view at this stage is FIG. 7.

[0091]

Next, the resist mask is removed, and a protective insulating film 107 is formed to cover the semiconductor layer. The protective insulating film 107 can be formed using a silicon nitride film, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, a tantalum oxide film, or the like by a sputtering method or the like.

[0092]

Then, a fourth photolithography step is performed to form a resist mask, so that the protective insulating film 107 is etched to form a contact hole 125 reaching the drain electrode layer 105b. In addition, a contact hole 127 reaching the second terminal 122 is also formed in the same etching step. In addition, a contact hole 109 reaching the capacitor electrode layer 124 is also formed in the same etching step. In order to reduce the number of masks, the gate insulating layer is preferably etched using the same resist mask so that a contact hole 126 reaching the gate electrode is formed using the same resist mask. A cross-sectional view at this stage is FIG. 4B.

[0093]

Then, the resist mask is removed, and a transparent conductive film is formed. The transparent conductive film is formed using indium oxide (In_2O_3), an alloy of indium oxide and tin oxide (In_2O_3-SnO_2, abbreviated as ITO), or the like by a sputtering method, a vacuum evaporation method, or the like. Etching treatment of such a material is performed with a hydrochloric acid based solution. Instead, because a residue tends to be generated particularly in etching of ITO, an alloy of indium oxide and zinc oxide (In_2O_3-ZnO) may be used in order to improve etching processability.

[0094]

Next, a fifth photolithography step is performed to form a resist mask, so that an unnecessary portion is removed by etching to form a pixel electrode 110.

[0095]

In the fifth photolithography step, a storage capacitor is formed by the capacitor electrode layer 124 and the pixel electrode layer 110 with the gate insulating layer 102 in the capacitor portion, used as a dielectric. The capacitor wiring 108 is electrically connected to the capacitor electrode layer 124 through the contact hole 109.

[0096]

Furthermore, in the fifth photolithography step, the first terminal and the second terminal are covered with the resist mask so that transparent conductive films 128 and 129 remain in the terminal portion. The transparent conductive films 128 and 129 serve as electrodes or wirings that are used for connection with an FPC. The transparent conductive film 129 formed over the second terminal 122 serves as a terminal electrode for connection which functions as an input terminal for the source

wiring.

[0097]

Then, the resist mask is removed, and a cross-sectional view at this stage is FIG. 4C. A top view at this stage is FIG. 8A.

[0098]

FIGS. 9A1 and 9A2 are a cross-sectional view and a top view of a gate wiring terminal portion at this stage, respectively. FIG. 9A1 is a cross-sectional view along line C1-C2 in FIG. 9A2. In FIG. 9A1, a transparent conductive film 155 formed over a protective insulating film 154 is a connecting terminal electrode which functions as an input terminal. Furthermore, in a terminal portion of FIG. 9A1, a first terminal 151 formed using the same material as the material of a gate wiring and a connection electrode 153 formed using the same material as the material of a source wiring overlap each other with a gate insulating layer 152 interposed therebetween, and are electrically connected to each other through the transparent conductive film 155. Note that a portion where the transparent conductive film 128 and the first terminal 121 shown in FIG. 4C are in contact with each other corresponds to a portion where the transparent conductive film 155 and the first terminal 151 are in contact with each other in FIG. 9A1.

[0099]

FIGS. 9B1 and 9B2 are a cross-sectional view and a top view of a source wiring terminal portion which is different from the source wiring terminal portion shown in FIG. 4C, respectively. FIG. 9B1 is a cross-sectional view along line D1-D2 in FIG. 9B2. In FIG. 9B1, a transparent conductive film 155 formed over a protective insulating film 154 is a connection terminal electrode which functions as an input terminal. In a terminal portion in FIG. 9B1, an electrode 156 formed using the same material as the material of a gate wiring is located under and overlaps with a second terminal 150 electrically connected to a source wiring with a gate insulating layer 102 interposed therebetween. The electrode 156 is not electrically connected to the second terminal 150. When the electrode 156 is set to, for example, floating, GND, or 0 V such that the potential the electrode 156 is different from the potential of the second terminal 150, a capacitor for preventing noise or static electricity can be formed. In addition, the second terminal 150 is electrically connected to the transparent conductive

film 155 with the protective insulating film 154 interposed therebetween.

[0100]

A plurality of gate wirings, source wirings, and capacitor wirings are provided depending on the pixel density. Also in the terminal portion, the first terminal at the same potential as the gate wiring, the second terminal at the same potential as the source wiring, the third terminal at the same potential as the capacitor wiring, and the like are each arranged in plurality. There is no particular limitation on the number of each of the terminals, and the number of the terminals may be determined, as appropriate.

[0101]

Through these five photolithography steps, a pixel thin film transistor portion including the thin film transistor 170 which is a bottom-gate n-channel thin film transistor, and the storage capacitor can be completed using the five photomasks. When these pixel thin film transistor portion and storage capacitor are arranged in a matrix corresponding to respective pixels, a pixel portion can be formed and one of the substrates for manufacturing an active matrix display device can be obtained. In this specification, such a substrate is referred to as an active matrix substrate for convenience.

[0102]

When an active matrix liquid crystal display device is manufactured, an active matrix substrate and a counter substrate provided with a counter electrode are bonded to each other with a liquid crystal layer interposed therebetween. Note that a common electrode electrically connected to the counter electrode on the counter substrate is provided over the active matrix substrate, and a fourth terminal electrically connected to the common electrode is provided in the terminal portion. This fourth terminal is provided so that the common electrode is fixed to a predetermined potential such as GND or 0 V.

[0103]

One embodiment of the present invention is not limited to the pixel structure of FIG. 8, and an example of a top view different from FIG. 8 is illustrated in FIG. 10. FIG. 10 illustrates the example in which a capacitor wiring is not provided and a pixel electrode overlaps with a gate wiring of an adjacent pixel with a protective insulating film and a gate insulating layer interposed therebetween to form a storage capacitor. In

that case, the capacitor wiring and a third terminal connected to the capacitor wiring can be omitted. Note that in FIG. 10, the same portions as those in FIG. 8 are denoted by the same reference numerals.

[0104]

In an active matrix liquid crystal display device, display patterns are formed on a screen by driving pixel electrodes arranged in a matrix. Specifically, when voltage is applied between a selected pixel electrode and a counter electrode that corresponds to the selected pixel electrode, a liquid crystal layer provided between the pixel electrode and the counter electrode is optically modulated, and this optical modulation is recognized as a display pattern.

[0105]

In displaying moving images, a liquid crystal display device has a problem that a long response time of liquid crystal molecules themselves causes afterimages or blurring of moving images. In order to improve the moving-image characteristics of a liquid crystal display device, a driving method called black insertion is employed in which black is displayed on the whole screen every other frame period.

[0106]

Alternatively, a driving method called double-frame rate driving may be employed in which the vertical cycle is 1.5 or 2 times as long as usual to improve the moving-image characteristics.

[0107]

Further alternatively, in order to improve the moving-image characteristics of a liquid crystal display device, a driving method may be employed in which a plurality of LEDs (light-emitting diodes) or a plurality of EL light sources are used to form a surface light source as a backlight, and each light source of the surface light source is independently driven in a pulsed manner in one frame period. As the surface light source, three or more kinds of LEDs may be used and an LED emitting white light may be used. Since a plurality of LEDs can be controlled independently, the light emission timing of LEDs can be synchronized with the timing at which a liquid crystal layer is optically modulated. According to this driving method, LEDs can be partly turned off; therefore, an effect of reducing power consumption can be obtained particularly in the case of displaying an image having a large part on which black is displayed.

[0108]

By combining these driving methods, the display characteristics of a liquid crystal display device, such as moving-image characteristics, can be improved as compared to those of conventional liquid crystal display devices.

[0109]

The n-channel transistor obtained in Embodiment 3 includes an In-Ga-Zn-O-based non-single-crystal semiconductor film in a channel formation region and has good dynamic characteristics. Thus, these driving methods can be applied in combination to the n-channel transistor of this embodiment.

[0110]

When a light-emitting display device is manufactured, one electrode (also referred to as a cathode) of an organic light-emitting element is set to a low power supply potential such as GND or 0 V; therefore, a terminal portion is provided with a fourth terminal for setting the cathode to a low power supply potential such as GND or 0 V. In addition, when a light-emitting display device is manufactured, a power supply line is provided in addition to a source wiring and a gate wiring. Therefore, a terminal portion is provided with a fifth terminal electrically connected to the power supply line.

[0111]

According to this embodiment, the thin film transistor has a stacked-layer structure in which a gate electrode layer, a gate insulating layer, a source and drain electrode layers, a source and drain regions (an oxide semiconductor layer containing In, Ga, and Zn), and a semiconductor layer (an oxide semiconductor layer containing In, Ga, and Zn), and the quality of the surface of the gate insulating layer is changed by plasma treatment, so that the semiconductor film is kept to be thin and parasitic capacitance can be suppressed. Note that the parasitic capacitance is sufficiently suppressed even when the semiconductor layer is thin, because the thickness is sufficient with respect to that of the gate insulating layer.

[0112]

According to this embodiment, a thin film transistor with high on-off ratio can be obtained, so that a thin film transistor having high dynamic characteristics can be manufactured. Thus, a semiconductor device including a thin film transistor with high electrical characteristics and high reliability can be provided.

[Embodiment 4]

[0113]

In this embodiment, an example of electronic paper will be described as a semiconductor device.

[0114]

FIG. 11 illustrates active-matrix electronic paper as an example of a semiconductor device, which is different from a liquid crystal display device. A thin film transistor 581 used in a pixel portion of the semiconductor device can be manufactured in a manner similar to the manner of the thin film transistor in the pixel portion described in Embodiment 3 and is a thin film transistor including an In-Ga-Zn-O-based non-single-crystal film as a semiconductor layer. Further, as described in Embodiment 1, tapered shapes of side surfaces of two electrodes which face each other with an oxide semiconductor layer interposed therebetween enables electronic paper including a highly reliable thin film transistor provided with an electric-field relaxation region to be manufactured.

[0115]

The electronic paper in FIG. 11 is an example of a display device using a twisting ball display system. A twisting ball display method employs a method in which display is performed by arranging spherical particles each of which is colored separately in black and white between the first electrode layer and the second electrode layer which are electrode layers used for display elements, and generating a potential difference between the first electrode layer and the second electrode layer so as to control the directions of the spherical particles.

[0116]

The thin film transistor 581 is a bottom-gate thin film transistor, and a source or drain electrode layer thereof is in contact with a first electrode layer 587 through an opening formed in an insulating layer 585, whereby the thin film transistor 581 is electrically connected to the first electrode layer 587. Between the first electrode layer 587 and a second electrode layer 588, spherical particles 589 each having a black region 590a, a white region 590b, and a cavity 594 around the regions which is filled with liquid are provided. A space around the spherical particles 589 is filled with a filler 595 such as a resin (see FIG. 11).

[0117]

Instead of the twisting ball, an electrophoretic element can also be used. A microcapsule having a diameter of approximately 10 μm to 200 μm, in which a transparent liquid and positively charged white microparticles and negatively charged black microparticles are encapsulated, is used. In the microcapsule that is provided between the first electrode layer and the second electrode layer, when an electric field is applied by the first electrode layer and the second electrode layer, the white microparticles and the black microparticles migrate to opposite sides to each other, so that white or black can be displayed. A display element using this principle is an electrophoretic display element, and is generally called an electronic paper. The electrophoretic display element has higher reflectivity than a liquid crystal display element; thus, an auxiliary light is unnecessary, less power is consumed, and a display portion can be recognized even in a dusky place. In addition, even when power is not supplied to the display portion, an image which has been displayed once can be maintained; accordingly, a displayed image can be stored even if a semiconductor device having a display function (which may simply be referred to as a display device or a semiconductor device provided with a display device) is distanced from an electric wave source.

[0118]

Through the above process, electronic paper as a semiconductor device can be manufactured at reduced cost.

[0119]

This embodiment can be implemented in appropriate combination with any of the structures described in Embodiments 1 to 3.

[Embodiment 5]

[0120]

In this embodiment, an example will be described below, in which at least part of a driver circuit and a thin film transistor arranged in a pixel portion are formed over one substrate in a display device which is one example of a semiconductor device.

[0121]

The thin film transistor arranged in the pixel portion is formed according to Embodiment 1 or 2. Further, the thin film transistor described in Embodiment 1 or 2 is

an n-channel TFT, and thus a part of a driver circuit that can include an n-channel TFT among driver circuits is formed over the same substrate as the substrate of the thin film transistor of the pixel portion.

[0122]

FIG. 12A illustrates an example of a block diagram of an active-matrix liquid crystal display device which is an example of a semiconductor device. The display device illustrated in FIG. 12A includes, over a substrate 5300, a pixel portion 5301 including a plurality of pixels that are each provided with a display element; a scan line driver circuit 5302 that selects a pixel; and a signal line driver circuit 5303 that controls a video signal input to the selected pixel.

[0123]

The pixel portion 5301 is connected to the signal line driver circuit 5303 by a plurality of signal lines S1 to Sm (not shown) which extend in a column direction from the signal line driver circuit 5303, and to the scan line driver circuit 5302 by a plurality of scan lines G1 to Gn (not shown) that extend in a row direction from the scan line driver circuit 5302. The pixel portion 5301 includes a plurality of pixels (not shown) arranged in matrix so as to correspond to the signal lines S1 to Sm and the scan lines G1 to Gn. Each pixel is connected to a signal line Sj (one of the signal lines S1 to Sm) and a scan line Gj (one of the scan lines G1 to Gn).

[0124]

The thin film transistor described in Embodiment 1 or 2 is an n-channel TFT, and a signal line driver circuit including the n-channel TFT is described with reference to FIG. 13.

[0125]

The signal line driver circuit illustrated in FIG. 13 includes a driver IC 5601, switch groups 5602_1 to 5602_M, a first wiring 5611, a second wiring 5612, a third wiring 5613, and wirings 5621_1 to 5621_M. Each of the switch groups 5602_1 to 5602_M includes a first thin film transistor 5603a, a second thin film transistor 5603b, and a third thin film transistor 5603c.

[0126]

The driver IC 5601 is connected to the first wiring 5611, the second wiring 5612, the third wiring 5613, and the wirings 5621_1 to 5621_M. Each of the switch

groups 5602_1 to 5602_M is connected to the first wiring 5611, the second wiring 5612, the third wiring 5613, and the wirings 5621_1 to 5621_M corresponding to the switch groups 5602_1 to 5602_M, respectively. Each of the wirings 5621_1 to 5621_M is connected to three signal lines via the first thin film transistor 5603a, the second thin film transistor 5603b, and the third thin film transistor 5603c. For example, the wiring 5621_J of the J-th column (one of the wirings 5621_1 to 5621_M) is connected to a signal line Sj−1, a signal line Sj, and a signal line Sj+1 via the first thin film transistor 5603a, the second thin film transistor 5603b, and the third thin film transistor 5603c which are included in the switch group 5602_J.

[0127]

A signal is input to each of the first wiring 5611, the second wiring 5612, and the third wiring 5613.

[0128]

Note that the driver IC 5601 is preferably formed over a single crystalline semiconductor substrate. Further, the switch groups 5602_1 to 5602_M are preferably formed over the same substrate as the substrate of the pixel portion. Therefore, the driver IC 5601 and the switch groups 5602_1 to 5602_M are preferably connected through an FPC or the like.

[0129]

Next, operation of the signal line driver circuit illustrated in FIG. 13 is described with reference to a timing chart in FIG. 14. The timing chart in FIG. 14 illustrates the case where the scan line Gi of the i-th row is selected. A selection period of the scan line Gi of the i-th row is divided into a first sub-selection period T1, a second sub-selection period T2, and a third sub-selection period T3. The signal line driver circuit in FIG. 13 operates similarly to that in FIG. 14 even when a scan line of another row is selected.

[0130]

Note that the timing chart in FIG. 14 shows the case where the wiring 5621_J of the J-th column is connected to the signal line Sj−1, the signal line Sj, and the signal line Sj+1 via the first thin film transistor 5603a, the second thin film transistor 5603b, and the third thin film transistor 5603c.

[0131]

The timing chart in FIG. 14 shows timing at which the scan line Gi of the i-th row is selected, timing 5703a of on/off of the first thin film transistor 5603a, timing 5703b of on/off of the second thin film transistor 5603b, timing 5703c of on/off of the third thin film transistor 5603c, and a signal 5721_J input to the wiring 5621_J of the J-th column.

[0132]

In the first sub-selection period T1, the second sub-selection period T2, and the third sub-selection period T3, different video signals are input to the wirings 5621_1 to 5621_M. For example, a video signal input to the wiring 5621_J in the first sub-selection period T1 is input to the signal line Sj−1, a video signal input to the wiring 5621_J in the second sub-selection period T2 is input to the signal line Sj, and a video signal input to the wiring 5621_J in the third sub-selection period T3 is input to the signal line Sj+1. The video signals input to the wiring 5621_J in the first sub-selection period T1, the second sub-selection period T2, and the third sub-selection period T3 are denoted by Data_j−1, Data_j, and Data_j+1, respectively.

[0133]

As shown in FIG. 14, in the first sub-selection period T1, the first thin film transistor 5603a is turned on, and the second thin film transistor 5603b and the third thin film transistor 5603c are turned off. At this time, Data_j−1 input to the wiring 5621_J is input to the signal line Sj−1 via the first thin film transistor 5603a. In the second sub-selection period T2, the second thin film transistor 5603b is turned on, and the first thin film transistor 5603a and the third thin film transistor 5603c are turned off. At this time, Data_j input to the wiring 5621_J is input to the signal line Sj via the second thin film transistor 5603b. In the third sub-selection period T3, the third thin film transistor 5603c is turned on, and the first thin film transistor 5603a and the second thin film transistor 5603b are turned off. At this time, Data_j+1 input to the wiring 5621_J is input to the signal line Sj+1 via the third thin film transistor 5603c.

[0134]

As described above, in the signal line driver circuit in FIG. 13, by dividing one gate selection period into three, video signals can be input to three signal lines from one

wiring 5621 in one gate selection period. Therefore, in the signal line driver circuit in FIG. 13, the number of connections between the substrate provided with the driver IC 5601 and the substrate provided with the pixel portion can be about 1/3 of the number of signal lines. The number of connections is reduced to about 1/3 of the number of the signal lines, so that reliability, yield, etc., of the signal line driver circuit in FIG. 13 can be improved.

[0135]

Note that there are no particular limitations on the arrangement, the number, a driving method, and the like of the thin film transistors, as long as one gate selection period is divided into a plurality of sub-selection periods and video signals are input to a plurality of signal lines from one wiring in the respective sub-selection periods as shown in FIG. 13.

[0136]

For example, when video signals are input to three or more signal lines from one wiring in each of three or more sub-selection periods, it is necessary to add a thin film transistor and a wiring for controlling the thin film transistor. Note that when one selection period is divided into four or more sub-selection periods, one sub-selection period becomes short. Therefore, one selection period is preferably divided into two or three sub-selection periods.

[0137]

As another example, one gate selection period may be divided into a precharge period Tp, the first sub-selection period T1, the second sub-selection period T2, and the third sub-selection period T3 as illustrated in a timing chart in FIG. 15. The timing chart in FIG. 15 illustrates timing at which the scan line Gi of the i-th row is selected, timing 5803a of on/off of the first thin film transistor 5603a, timing 5803b of on/off of the second thin film transistor 5603b, timing 5803c of on/off of the third thin film transistor 5603c, and a signal 5821_J input to the wiring 5621_J of the J-th column. As shown in FIG. 15, the first thin film transistor 5603a, the second thin film transistor 5603b, and the third thin film transistor 5603c are tuned on in the precharge period Tp. At this time, precharge voltage Vp input to the wiring 5621_J is input to each of the signal line Sj−1, the signal line Sj, and the signal line Sj+1 via the first thin film

transistor 5603a, the second thin film transistor 5603b, and the third thin film transistor 5603c. In the first sub-selection period T1, the first thin film transistor 5603a is turned on, and the second thin film transistor 5603b and the third thin film transistor 5603c are turned off. At this time, Data_j–1 input to the wiring 5621_J is input to the signal line Sj–1 via the first thin film transistor 5603a. In the second sub-selection period T2, the second thin film transistor 5603b is turned on, and the first thin film transistor 5603a and the third thin film transistor 5603c are turned off. At this time, Data_j input to the wiring 5621_J is input to the signal line Sj via the second thin film transistor 5603b. In the third sub-selection period T3, the third thin film transistor 5603c is turned on, and the first thin film transistor 5603a and the second thin film transistor 5603b are turned off. At this time, Data_j+1 input to the wiring 5621_J is input to the signal line Sj+1 via the third thin film transistor 5603c.

[0138]

As described above, in the signal line driver circuit in FIG. 13 to which the timing chart in FIG. 15 is applied, the video signal can be written to the pixel at high speed because the signal line can be precharged by providing a precharge selection period before a sub-selection period. Note that portions in FIG. 15 which are similar to those of FIG. 14 are denoted by common reference numerals and detailed description of the same portions and portions which have similar functions is omitted.

[0139]

Further, a structure of a scan line driver circuit is described. The scan line driver circuit includes a shift register and a buffer. Also, a level shifter may be included in some cases. In the scan line driver circuit, when the clock signal (CLK) and the start pulse signal (SP) are input to the shift register, a selection signal is generated. The generated selection signal is buffered and amplified by the buffer, and the resulting signal is supplied to a corresponding scan line. Gate electrodes of transistors in pixels of one line are connected to the scan line. Since the transistors in the pixels of one line have to be turned on all at once, a buffer which can supply a large current is used.

[0140]

One mode of a shift register which is used in a part of a scan line driver circuit

is described with reference to FIGS. 16 and 17.

[0141]

FIG. 16 illustrates a circuit configuration of the shift register. The shift register illustrated in FIG. 16 includes a plurality of flip-flops 5701-i (one of flip-flops 5701-1 to 5701-n). Further, the shift register operates by inputting a first clock signal, a second clock signal, a start pulse signal, and a reset signal.

[0142]

The connection relation of the shift register in FIG. 16 is described below. In the i-th stage flip-flop 5701_i (one of the flip-flops 5701_1 to 5701_n) in the shift register of FIG. 16, a first wiring 5501 illustrated in FIG. 17 is connected to a seventh wiring 5717_i–1; a second wiring 5502 illustrated in FIG. 17 is connected to a seventh wiring 5717_i+1; a third wiring 5503 illustrated in FIG. 17 is connected to a seventh wiring 5717_i; and a sixth wiring 5506 illustrated in FIG. 17 is connected to a fifth wiring 5715.

[0143]

Further, a fourth wiring 5504 shown in FIG. 17 is connected to a second wiring 5712 in flip-flops of odd-numbered stages, and is connected to a third wiring 5713 in flip-flops of even-numbered stages. A fifth wiring 5505 shown in FIG. 17 is connected to a fourth wiring 5714.

[0144]

Note that the first wiring 5501 of the first stage flip-flop 5701_1 shown in FIG. 17 is connected to a first wiring 5711, and the second wiring 5502 of the n-th stage flip-flop 5701_n shown in FIG. 17 is connected to a sixth wiring 5716.

[0145]

Note that the first wiring 5711, the second wiring 5712, the third wiring 5713, and the sixth wiring 5716 may be referred to as a first signal line, a second signal line, a third signal line, and a fourth signal line, respectively. The fourth wiring 5714 and the fifth wiring 5715 may be referred to as a first power supply line and a second power supply line, respectively.

[0146]

Next, FIG. 17 illustrates details of the flip-flop shown in FIG. 16. A flip-flop

illustrated in FIG. 17 includes a first thin film transistor 5571, a second thin film transistor 5572, a third thin film transistor 5573, a fourth thin film transistor 5574, a fifth thin film transistor 5575, a sixth thin film transistor 5576, a seventh thin film transistor 5577, and an eighth thin film transistor 5578. Each of the first thin film transistor 5571, the second thin film transistor 5572, the third thin film transistor 5573, the fourth thin film transistor 5574, the fifth thin film transistor 5575, the sixth thin film transistor 5576, the seventh thin film transistor 5577, and the eighth thin film transistor 5578 is an n-channel transistor and is turned on when the gate-source voltage (V_{gs}) exceeds the threshold voltage (V_{th}).

[0147]

Next, the connection structure of the flip-flop illustrated in FIG. 16 is described below.

[0148]

A first electrode (one of a source electrode and a drain electrode) of the first thin film transistor 5571 is connected to the fourth wiring 5504. A second electrode (the other of the source electrode and the drain electrode) of the first thin film transistor 5571 is connected to the third wiring 5503.

[0149]

A first electrode of the second thin film transistor 5572 is connected to the sixth wiring 5506, and a second electrode of the second thin film transistor 5572 is connected to the third wiring 5503.

[0150]

A first electrode of the third thin film transistor 5573 is connected to the fifth wiring 5505; a second electrode of the third thin film transistor 5573 is connected to a gate electrode of the second thin film transistor 5572; and a gate electrode of the third thin film transistor 5573 is connected to the fifth wiring 5505.

[0151]

A first electrode of the fourth thin film transistor 5574 is connected to the sixth wiring 5506; a second electrode of the fourth thin film transistor 5574 is connected to a gate electrode of the second thin film transistor 5572; and a gate electrode of the fourth thin film transistor 5574 is connected to a gate electrode of the first thin film transistor 5571.

[0152]

A first electrode of the fifth thin film transistor 5575 is connected to the fifth wiring 5505; a second electrode of the fifth thin film transistor 5575 is connected to the gate electrode of the first thin film transistor 5571; and a gate electrode of the fifth thin film transistor 5575 is connected to the first wiring 5501.

[0153]

A first electrode of the sixth thin film transistor 5576 is connected to the sixth wiring 5506; a second electrode of the sixth thin film transistor 5576 is connected to the gate electrode of the first thin film transistor 5571; and a gate electrode of the sixth thin film transistor 5576 is connected to the gate electrode of the second thin film transistor 5572.

[0154]

A first electrode of the seventh thin film transistor 5577 is connected to the sixth wiring 5506; a second electrode of the seventh thin film transistor 5577 is connected to the gate electrode of the first thin film transistor 5571; and a gate electrode of the seventh thin film transistor 5577 is connected to the second wiring 5502. A first electrode of the eighth thin film transistor 5578 is connected to the sixth wiring 5506; a second electrode of the eighth thin film transistor 5578 is connected to the gate electrode of the second thin film transistor 5572; and a gate electrode of the eighth thin film transistor 5578 is connected to the first wiring 5501.

[0155]

Note that the points at which the gate electrode of the first thin film transistor 5571, the gate electrode of the fourth thin film transistor 5574, the second electrode of the fifth thin film transistor 5575, the second electrode of the sixth thin film transistor 5576, and the second electrode of the seventh thin film transistor 5577 are connected are each referred to as a node 5543. The points at which the gate electrode of the second thin film transistor 5572, the second electrode of the third thin film transistor 5573, the second electrode of the fourth thin film transistor 5574, the gate electrode of the sixth thin film transistor 5576, and the second electrode of the eighth thin film transistor 5578 are connected are each referred to as a node 5544.

[0156]

Note that the first wiring 5501, the second wiring 5502, the third wiring 5503,

and the fourth wiring 5504 may be referred to as a first signal line, a second signal line, a third signal line, and a fourth signal line, respectively. The fifth wiring 5505 and the sixth wiring 5506 may be referred to as a first power supply line and a second power supply line, respectively.

[0157]

The signal line driver circuit and the scan line driver circuit can be formed using only the n-channel TFTs described in Embodiment 1 or 2. In that case, the drive frequency of the driver circuit can be increased because the mobility of a transistor using an oxide semiconductor layer is high. Further, since the parasitic capacitance is reduced by the source and drain regions in each of the n-channel TFTs described in Embodiment 1 or 2, the frequency characteristic (also called f characteristic) is high. For example, a scan line driver circuit using the n-channel TFT described in Embodiment 1 or 2 can operate at high speed, and thus a frame frequency can be increased and insertion of black images can be realized.

[0158]

In addition, by increasing the channel width of the transistor in the scan line driver circuit or providing a plurality of scan line driver circuits, for example, higher frame frequency can be realized. When a plurality of scan line driver circuits are provided, a scan line driver circuit for driving even-numbered scan lines is provided on one side and a scan line driver circuit for driving odd-numbered scan lines is provided on the opposite side; thus, increase in frame frequency can be realized.

[0159]

Further, when an active-matrix light-emitting display device which is an example of a semiconductor device is manufactured, a plurality of thin film transistors are arranged in at least one pixel, and thus a plurality of scan line driver circuits are preferably arranged. FIG. 12B is a block diagram illustrating an example of an active-matrix light-emitting display device.

[0160]

The light-emitting display device illustrated in FIG. 12B includes, over a substrate 5400, a pixel portion 5401 having a plurality of pixels each provided with a display element, a first scan line driver circuit 5402 and a second scan line driver circuit 5404 that select a pixel, and a signal line driver circuit 5403 that controls input of a

video signal to the selected pixel.

[0161]

When the video signal input to a pixel of the light-emitting display device illustrated in FIG. 12B is a digital signal, a pixel is in a light-emitting state or in a non-light-emitting state by switching of ON/OFF of a transistor. Thus, grayscale can be displayed using an area ratio grayscale method or a time ratio grayscale method. An area ratio grayscale method refers to a driving method by which one pixel is divided into a plurality of subpixels and the respective subpixels are driven separately based on video signals so that grayscale is displayed. Further, a time ratio grayscale method refers to a driving method by which a period during which a pixel is in a light-emitting state is controlled so that grayscale is displayed.

[0162]

Since the response speed of light-emitting elements is faster than that of liquid crystal elements or the like, the light-emitting elements are suitable for a time ratio grayscale method. Specifically, in the case of performing display with a time ratio grayscale method, one frame period is divided into a plurality of subframe periods. Then, in accordance with video signals, the light-emitting element in the pixel is set in a light-emitting state or a non-light-emitting state in each subframe period. By dividing one frame period into a plurality of subframe periods, the total length of time, in which a pixel actually emits light in one frame period, can be controlled by video signals so that grayscale can be displayed.

[0163]

In the example of the light-emitting display device illustrated in FIG. 12B, in the case where two TFTs, a switching TFT and a current control TFT, are arranged in one pixel, the first scan line driver circuit 5402 generates a signal which is input to a first scan line serving as a gate wiring of the switching TFT, and the second scan line driver circuit 5404 generates a signal which is input to a second scan line serving as a gate wiring of the current control TFT; however, one scan line driver circuit may generate both the signal which is input to the first scan line and the signal which is input to the second scan line. In addition, for example, there is a possibility that a plurality of first scan lines used for controlling the operation of the switching element be provided in each pixel depending on the number of transistors included in the switching

element. In that case, signals which are input to the plurality of first scan lines may be all generated by one scan line driver circuit or by an individual plurality of scan line driver circuits.

[0164]

Also in the light-emitting display device, a part of a driver circuit that can include n-channel TFTs among driver circuits can be formed over the same substrate as the substrate of the thin film transistors of the pixel portion. The signal line driver circuit and the scan line driver circuit can be formed using only the n-channel TFTs described in Embodiment 1 or 2.

[0165]

Through the above process, a highly reliable display device can be manufactured as a semiconductor device.

[0166]

This embodiment can be implemented in appropriate combination with any of the structures disclosed in the other embodiments.

[Embodiment 6]

[0167]

In this embodiment, an example of a light-emitting display device will be described as a semiconductor device. As a display element included in a display device, a light-emitting element utilizing electro luminescence is described in this embodiment. Light-emitting elements utilizing electroluminescence are classified according to the type of a light emitting material, that is, an organic compound or an inorganic compound. In general, the former is referred to as an organic EL element, the latter as an inorganic EL element.

[0168]

In an organic EL element, voltage is applied to the light-emitting element, so that electrons are injected from an electrode into a layer including a light-emitting organic compound, and holes are injected from the other electrode into the layer including the light-emitting organic compound, and there flows electric current. Then, by recombination of these carriers (electrons and holes), the organic compound having a light-emitting property gets in an excited state, and light is emitted when the excited state returns to a ground state. From such a mechanism, such a light emitting element

is referred to as a current-excitation-type light-emitting element.

[0169]

Inorganic EL elements are classified in a dispersive inorganic EL element and a thin-film inorganic EL element. A dispersive inorganic EL element includes a light-emitting layer in which particles of a light-emitting material are dispersed in a binder, and light emission mechanism thereof is donor-acceptor recombination light emission, in which a donor level and an acceptor level are utilized. In a thin film inorganic EL element, a light-emitting layer is sandwiched between dielectric layers, and the dielectric layers are sandwiched between electrodes. Light emission mechanism of the thin film inorganic EL element is local light emission, in which inner-shell electron transition of a metal ion is utilized. In this embodiment, description will be made using an organic EL element as a light-emitting element.

[0170]

FIG. 18 illustrates an example of a pixel structure to which digital time grayscale driving can be applied, as an example of a semiconductor device.

[0171]

A structure and an operation of the pixel to which digital time grayscale driving can be applied are described below. An example is described in this embodiment in which one pixel includes two n-channel transistors using an oxide semiconductor layer (an In-Ga-Zn-O-based non-single-crystal film) in a channel formation region.

[0172]

A pixel 6400 includes a switching transistor 6401, a driving transistor 6402, a light-emitting element 6404, and a capacitor 6403. A gate of the switching transistor 6401 is connected to a scan line 6406, a first electrode (one of a source electrode and a drain electrode) of the switching transistor 6401 is connected to a signal line 6405, and a second electrode (the other of the source electrode and the drain electrode) of the switching transistor 6401 is connected to a gate of the driving transistor 6402. The gate of the driving transistor 6402 is connected to a power supply line 6407 through the capacitor 6403, a first electrode of the driving transistor 6402 is connected to the power supply line 6407, and a second electrode of the driving transistor 6402 is connected to a first electrode (pixel electrode) of the light-emitting element 6404. A second electrode of the light-emitting element 6404 corresponds to a common electrode 6408.

[0173]

The second electrode of the light-emitting element 6404 (the common electrode 6408) is set to a low power supply potential. The low power supply potential is a potential satisfying the low power supply potential < a high power supply potential with the high power supply potential set to the power supply line 6407 as a reference. As the low power supply potential, GND, 0 V, or the like may be employed, for example. A potential difference between the high power supply potential and the low power supply potential is applied to the light-emitting element 6404, and a current is supplied to the light-emitting element 6404. Here, in order to make the light-emitting element 6404 emit light, each potential is set so that the potential difference between the high power supply potential and the low power supply potential is a forward threshold voltage or higher.

[0174]

Gate capacitance of the driving transistor 6402 may be used as a substitute for the capacitor 6403, so that the capacitor 6403 can be omitted. The gate capacitance of the driving transistor 6402 may be formed between a channel region and a gate electrode.

[0175]

In the case of voltage-input voltage-driving method, a video signal is input to the gate of the driving transistor 6402 so that the driving transistor 6402 is in either of two states of being sufficiently turned on and turned off. That is, the driving transistor 6402 operates in a linear region. Since the driving transistor 6402 operates in a linear region, a voltage higher than the voltage of the power supply line 6407 is applied to the gate of the driving transistor 6402. Note that a voltage greater than or equal to the sum voltage of the power supply line voltage and V_{th} of the driving transistor 6402 is applied to the signal line 6405.

[0176]

In the case of performing analog grayscale driving instead of digital time grayscale driving, the same pixel structure as that in FIG. 18 can be used by changing signal input.

[0177]

In the case of performing the analog grayscale driving, a voltage greater than or

equal to the sum of the forward voltage of the light-emitting element 6404 and V_{th} of the driving transistor 6402 is applied to the gate of the driving transistor 6402. The forward voltage of the light-emitting element 6404 refers to a voltage to obtain a desired luminance, and includes at least a forward threshold voltage. The video signal such that the driving transistor 6402 operates in a saturation region is input, so that a current can be supplied to the light-emitting element 6404. In order that the driving transistor 6402 can operate in the saturation region, the potential of the power supply line 6407 is higher than the gate potential of the driving transistor 6402. Since the video signal is an analog signal, a current in accordance with the video signal flows in the light-emitting element 6404, and the analog grayscale driving can be performed.

[0178]

Note that the pixel structure illustrated in FIG. 18 is not limited thereto. For example, a switch, a resistor, a capacitor, a transistor, a logic circuit, or the like may be added to the pixel illustrated in FIG. 18.

[0179]

Next, structures of a light-emitting element will be described using FIGS. 19A to 19C. In this embodiment, cross-sectional structures of pixels are described taking the case where a driving TFT is the thin film transistor 170, as an example. Driving TFTs 7001, 7011, and 7021 used in semiconductor devices illustrated in FIGS. 19A to 19C can be manufactured in a manner similar to that of the thin film transistor 170 described in Embodiment 1 and are thin film transistors having high electrical characteristics, each including an In-Ga-Zn-O-based non-single-crystal film as a semiconductor layer.

[0180]

In order to extract light emission from the light-emitting element, at least one of the anode and the cathode of the light-emitting element is required to be transparent. The thin film transistors and the light-emitting element are formed over the substrate. A light-emitting element can have a top emission structure in which light is extracted through the surface opposite to the substrate; a bottom emission structure in which light is extracted through the surface on the substrate side; or a dual emission structure in which light is extracted through the surface opposite to the substrate and the surface on the substrate side. The pixel structure illustrated in FIG. 18 can be applied to a

light-emitting element having any of these emission structures.

[0181]

A light-emitting element having a top emission structure is described with reference to FIG. 19A.

[0182]

FIG. 19A is a cross-sectional view of a pixel in the case where a driving TFT 7001 is the thin film transistor 170 shown in FIG. 1B and light emission from a light-emitting element 7002 passes to an anode 7005 side. In FIG. 19A, a cathode 7003 of the light-emitting element 7002 is electrically connected to the driving TFT 7001, and a light-emitting layer 7004 and the anode 7005 are stacked in this order over the cathode 7003. The cathode 7003 can be formed using various conductive materials as long as they have a low work function and reflect light. For example, Ca, Al, CaF, MgAg, AlLi, or the like is preferably used. The light-emitting layer 7004 may be formed using either a single layer or a stacked layer of a plurality of layers. If the light-emitting layer 7004 is formed using a plurality of layers, the light-emitting layer 7004 is formed by stacking an electron-injecting layer, an electron-transporting layer, a light-emitting layer, a hole-transporting layer, and a hole-injecting layer in this order over the cathode 7003. It is not necessary to form all of these layers. The anode 7005 is formed using a light-transmitting conductive film such as a film of indium oxide including tungsten oxide, indium zinc oxide including tungsten oxide, indium oxide including titanium oxide, indium tin oxide including titanium oxide, indium tin oxide (hereinafter, referred to as ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added.

[0183]

A region where the light-emitting layer 7004 is sandwiched between the cathode 7003 and the anode 7005 corresponds to the light-emitting element 7002. In the case of the pixel illustrated in FIG. 19A, light emitted from the light-emitting element 7002 is ejected to the anode 7005 side as indicated by an arrow.

[0184]

A light-emitting element having a bottom emission structure is described next with reference to FIG. 19B. FIG. 19B is a cross-sectional view of a pixel in the case where a driving TFT 7011 is the thin film transistor 170 shown in FIG. 1A and light

emission from a light-emitting element 7012 passes to a cathode 7013 side. In FIG. 19B, the cathode 7013 of the light-emitting element 7012 is formed over a light-transmitting conductive film 7017 that is electrically connected to the driving TFT 7011, and a light-emitting layer 7014 and an anode 7015 are stacked in this order over the cathode 7013. A blocking film 7016 for reflecting or blocking light may be formed so as to cover the anode 7015 when the anode 7015 has a light-transmitting property. For the cathode 7013, a variety of materials can be used as in the case of FIG. 19A as long as they are conductive materials having a low work function. The cathode 7013 has a thickness that can transmit light (preferably, about 5 to 30 nm). For example, an aluminum film with a thickness of 20 nm can be used as the cathode 7013. In a manner similar to that of FIG. 19A, the light-emitting layer 7014 may be formed using either a single-layer structure or a layered structure of a plurality of layers. Although the anode 7015 does not need to transmit light, the anode 7015 can be formed using a light-transmitting conductive material in a manner similar to that of FIG. 19A. For the blocking film 7016, a metal or the like that reflects light can be used; however, it is not limited to a metal film. For example, a resin or the like to which black pigments are added can be used.

[0185]

A region where the light-emitting layer 7014 is sandwiched between the cathode 7013 and the anode 7015 corresponds to the light-emitting element 7012. In the case of the pixel illustrated in FIG. 19B, light emitted from the light-emitting element 7012 is ejected to the cathode 7013 side as indicated by an arrow.

[0186]

Next, a light-emitting element having a dual emission structure is described with reference to FIG. 19C. In FIG. 19C, a cathode 7023 of a light-emitting element 7022 is formed over a light-transmitting conductive film 7027 which is electrically connected to the driving TFT 7021, and a light-emitting layer 7024 and an anode 7025 are stacked in this order over the cathode 7023. As in the case of FIG. 19A, the cathode 7023 can be formed using a variety of conductive materials as long as they have a low work function. The cathode 7023 has a thickness that can transmit light. For example, an Al film having a thickness of 20 nm can be used as the cathode 7023. In a manner similar to that of FIG. 19A, the light-emitting layer 7024 may be formed using

either a single-layer structure or a layered structure of a plurality of layers. In a manner similar to that of FIG. 19A, the anode 7025 can be formed using a light-transmitting conductive material.

[0187]

A region where the cathode 7023, the light-emitting layer 7024, and the anode 7025 overlap with each other corresponds to the light-emitting element 7022. In the case of the pixel illustrated in FIG. 19C, light emitted from the light-emitting element 7022 is ejected to both an anode 7025 side and a cathode 7023 side as indicated by arrows.

[0188]

Although an organic EL element is described as a light-emitting element in this embodiment, an inorganic EL element may be provided as a light-emitting element.

[0189]

This embodiment describes the example in which a thin film transistor for controlling the drive of a light-emitting element (the driving TFT) is electrically connected to the light-emitting element. However, a current control TFT may be connected between the driving TFT and the light-emitting element.

[0190]

A semiconductor device described in this embodiment is not limited to the structures illustrated in FIGS. 19A to 19C and can be modified in various ways based on the spirit of techniques according to the present invention disclosed in this specification.

[0191]

Next, a top surface and a cross section of a light-emitting display panel (also referred to as a light-emitting panel), which is one embodiment of the semiconductor device will be described with reference to FIGS. 22A and 22B. FIG. 22A is a top view of a panel in which a thin film transistor and a light-emitting element are sealed between a first substrate and a second substrate with a sealant. FIG. 22B is a cross-sectional view taken along line H-I of FIG. 22A.

[0192]

A sealant 4505 is provided to surround a pixel portion 4502, signal line driver circuits 4503a and 4503b, and scan line driver circuits 4504a and 4504b, which are provided over a first substrate 4501. In addition, a second substrate 4506 is provided

over the pixel portion 4502, the signal line driver circuits 4503a and 4503b, and the scan line driver circuits 4504a and 4504b. Accordingly, the pixel portion 4502, the signal line driver circuits 4503a and 4503b, and the scan line driver circuits 4504a and 4504b are sealed together with a filler 4507, by the first substrate 4501, the sealant 4505, and the second substrate 4506. It is preferable that a display device be thus packaged (sealed) with a protective film (such as a bonding film or an ultraviolet curable resin film) or a cover material with high air-tightness and little degasification so that the display device is not exposed to the outside air.

[0193]

The pixel portion 4502, the signal line driver circuits 4503a and 4503b, and the scan line driver circuits 4504a and 4504b formed over the first substrate 4501 each include a plurality of thin film transistors, and a thin film transistor 4510 included in the pixel portion 4502 and a thin film transistor 4509 included in the signal line driver circuit 4503a are illustrated as an example in FIG. 20B.

[0194]

As the thin film transistors 4509 and 4510, the highly reliable thin film transistors described in Embodiment 1, each including an In-Ga-Zn-O-based non-single-crystal film as a semiconductor layer can be used.

[0195]

Moreover, reference numeral 4511 denotes a light-emitting element. A first electrode layer 4517 that is a pixel electrode included in the light-emitting element 4511 is electrically connected to a source electrode layer or a drain electrode layer of the thin film transistor 4510. Note that a structure of the light-emitting element 4511 which includes the first electrode layer 4517, an electroluminescent layer 4512, and the second electrode layer 4513 is not limited to the structure described in Embodiment 6. The structure of the light-emitting element 4511 can be changed as appropriate depending on the direction in which light is extracted from the light-emitting element 4511, or the like.

[0196]

A bank 4520 is formed using an organic resin film, an inorganic insulating film, or organic polysiloxane. It is particularly preferable that the bank 4520 be formed using a photosensitive material to have an opening over the first electrode layer 4517 so

that a sidewall of the opening is formed as an inclined surface with continuous curvature.

[0197]

The electroluminescent layer 4512 may be formed as a single layer or a plurality of layers stacked.

[0198]

A protective film may be formed over the second electrode layer 4513 and the bank 4520 in order to prevent oxygen, hydrogen, moisture, carbon dioxide, or the like from entering into the light-emitting element 4511. As the protective film, a silicon nitride film, a silicon nitride oxide film, a DLC film, or the like can be formed.

[0199]

A variety of signals and potentials are supplied to the signal line driver circuits 4503a and 4503b, the scan line driver circuits 4504a and 4504b, or the pixel portion 4502 from FPCs 4518a and 4518b.

[0200]

In Embodiment 6, a connection terminal electrode 4515 is formed from the same conductive film as the first electrode layer 4517 included in the light-emitting element 4511, and a terminal electrode 4516 is formed from the same conductive film as the source and drain electrode layers included in the thin film transistors 4509 and 4510.

[0201]

The connection terminal electrode 4515 is electrically connected to a terminal of the FPC 4518a through an anisotropic conductive film 4519.

[0202]

As the second substrate located in the direction in which light is extracted from the light-emitting element 4511 needs to have a light-transmitting property. In that case, a material with a light-transmitting property, such as a glass plate, a plastic sheet, a polyester film, or an acrylic film is used.

[0203]

As the filler 4507, an ultraviolet curable resin or a thermosetting resin can be used, in addition to an inert gas such as nitrogen or argon. For example, PVC (polyvinyl chloride), acrylic, polyimide, an epoxy resin, a silicone resin, PVB (polyvinyl butyral), or EVA (ethylene vinyl acetate) can be used.

[0204]

If necessary, an optical film such as a polarizing plate, a circularly polarizing plate (including an elliptically polarizing plate), a retardation plate (a quarter-wave plate or a half-wave plate), or a color filter may be provided as appropriate for a light-emitting surface of the light-emitting element. Further, the polarizing plate or the circularly polarizing plate may be provided with an anti-reflection film. For example, anti-glare treatment may be carried out by which reflected light can be diffused by projections and depressions on the surface so as to reduce the glare.

[0205]

The signal line driver circuits 4503a and 4503b and the scan line driver circuits 4504a and 4504b may be mounted as driver circuits formed using a single crystal semiconductor film or polycrystalline semiconductor film over a single crystal semiconductor substrate or an insulating substrate separately prepared. Alternatively, only the signal line driver circuits or part thereof, or the scan line driver circuits or part thereof may be separately formed and mounted. This embodiment is not limited to the structure illustrated in FIGS. 22A and 22B.

[0206]

Through the above process, a light-emitting display device (display panel) can be manufactured at low cost.

[0207]

This embodiment can be implemented in appropriate combination with any of the structures described in Embodiments 1 to 3.

[Embodiment 7]

[0208]

In this embodiment, top surfaces and a cross section each of a liquid crystal display panel which corresponds to one example of the semiconductor device will be described using FIGS. 20A1, 20A2, and 20B. FIGS. 20A1 and 20A2 are each a top view of a panel in which thin film transistors 4010 and 4011 formed over a first substrate 4001 and a liquid crystal element 4013 are sealed between the first substrate 4001 and a second substrate 4006 with a sealant 4005. The thin film transistors 4010 and 4011 are according to Embodiment 1 and each includes an In-Ga-Zn-O-based non-single-crystal film as a semiconductor layer. FIG. 20B is a cross-sectional view

along line M-N of each of FIGS. 20A1 and 20A2.

[0209]

The sealant 4005 is provided so as to surround a pixel portion 4002 and a scan line driver circuit 4004 that are provided over the first substrate 4001. The second substrate 4006 is provided over the pixel portion 4002 and the scan line driver circuit 4004. Therefore, the pixel portion 4002 and the scan line driver circuit 4004 are sealed together with a liquid crystal layer 4008, by the first substrate 4001, the sealant 4005, and the second substrate 4006. A signal line driver circuit 4003 that is formed using a single crystal semiconductor film or a polycrystalline semiconductor film over a substrate separately prepared is mounted in a region different from the region surrounded by the sealant 4005 over the first substrate 4001.

[0210]

Note that there is no particular limitation on the connection method of a driver circuit which is separately formed, and a COG method, a wire bonding method, a TAB method, or the like can be used. FIG. 20A1 illustrates an example of mounting the signal line driver circuit 4003 by a COG method, and FIG. 20A2 illustrates an example of mounting the signal line driver circuit 4003 by a TAB method.

[0211]

The pixel portion 4002 and the scan line driver circuit 4004 provided over the first substrate 4001 each include a plurality of thin film transistors. FIG. 20B illustrates the thin film transistor 4010 included in the pixel portion 4002 and the thin film transistor 4011 included in the scanning line driver circuit 4004. Insulating layers 4020 and 4021 are provided over the thin film transistors 4010 and 4011.

[0212]

As each of the thin film transistors 4010 and 4011, the thin film transistor including an In-Ga-Zn-O-based non-single-crystal film as a semiconductor layer, which is described in Embodiment 1 can be employed. The thin film transistor 4011 corresponds to the thin film transistor 170 shown in FIG. 1 of Embodiment 1.

[0213]

A pixel electrode layer 4030 included in the liquid crystal element 4013 is electrically connected to the thin film transistor 4010. A counter electrode layer 4031 of the liquid crystal element 4013 is formed over the second substrate 4006. A portion

where the pixel electrode layer 4030, the counter electrode layer 4031, and the liquid crystal layer 4008 overlap with one another corresponds to the liquid crystal element 4013. Note that the pixel electrode layer 4030 and the counter electrode layer 4031 are provided with an insulating layer 4032 and an insulating layer 4033, respectively, each of which functions as an alignment film. The liquid crystal layer 4008 is sandwiched between the pixel electrode layer 4030 and the counter electrode layer 4031 with the insulating layers 4032 and 4033 interposed therebetween.

[0214]

The first substrate 4001 and the second substrate 4006 can be formed using glass, metal (typically, stainless steel), ceramic, or plastic. As for plastic, an FRP (fiberglass-reinforced plastics) plate, a PVF (polyvinyl fluoride) film, a polyester film, or an acrylic resin film can be used. Further, sheet in which aluminum foil is sandwiched by PVF films or polyester films can also be used.

[0215]

A columnar spacer denoted by reference numeral 4035 is obtained by selective etching of an insulating film and is provided in order to control the distance (a cell gap) between the pixel electrode layer 4030 and the counter electrode layer 4031. Note that a spherical spacer may be used. The counter electrode layer 4031 is electrically connected to a common potential line provided over the same substrate as the substrate of the thin film transistor 4010. With the use of the common connection portion, the counter electrode layer 4031 can be electrically connected to the common potential line through conductive particles provided between the pair of substrates. Note that the conductive particles are contained in the sealant 4005.

[0216]

Alternatively, a liquid crystal showing a blue phase for which an alignment film is unnecessary may be used. A blue phase is one of the liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase while temperature of cholesteric liquid crystal is increased. Since the blue phase is only generated within a narrow range of temperatures, a liquid crystal composition containing a chiral agent at 5 wt% or more is used for the liquid crystal layer 4008 in order to improve the temperature range. The liquid crystal composition which includes a liquid crystal showing a blue phase and a chiral agent has a small response

time of 10 to 100 μs, has optical isotropy, which makes the alignment process unneeded, and has a small viewing angle dependence.

[0217]

Although an example of a transmissive liquid crystal display device is described in this embodiment, the present invention can also be applied to a reflective liquid crystal display device or a transflective liquid crystal display device.

[0218]

In Embodiment 7, an example of the liquid crystal display device is described in which a polarizing plate is provided on the outer surface of the substrate (on the viewer side) and a coloring layer and an electrode layer used for a display element are provided on the inner surface of the substrate in this order; however, the polarizing plate may be provided on the inner surface of the substrate. The stack structure of the polarizing plate and the coloring layer is not limited to that described in Embodiment 7 and may be set as appropriate depending on materials of the polarizing plate and the coloring layer or conditions of manufacturing steps. Furthermore, a light-blocking film serving as a black matrix may be provided.

[0219]

In this embodiment, in order to reduce surface roughness of the thin film transistor and to improve reliability of the thin film transistor, the thin film transistor obtained by Embodiment 1 is covered with the insulating layers (the insulating layer 4020 and the insulating layer 4021) each functioning as a protective film or a planarizing insulating film. The protective film is provided to prevent entry of impurities floating in air, such as an organic substance, a metal substance, or moisture, and is preferably a dense film. The protective film may be formed by a sputtering method to be a single-layer film or a stack of a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, and/or an aluminum nitride oxide film. Although an example in which the protective film is formed by a sputtering method is described in this embodiment, the present invention is not limited to this example, and the protective film may be formed by a variety of methods such as a PCVD method.

[0220]

In this embodiment, the insulating layer 4020 having a stack structure is formed as the protective film. As a first layer of the insulating layer 4020, a silicon oxide film is formed by a sputtering method. The use of the silicon oxide film as the protective film has the effect of preventing a hillock of an aluminum film used for the source and drain electrode layers.

[0221]

In addition, an insulating layer is formed as a second layer of the protective film. In this embodiment, as the second layer of the insulating layer 4020, a silicon nitride film is formed by a sputtering method. The use of the silicon nitride film as the protective film can prevent the entry of mobile ions of sodium or the like to a semiconductor region so that variation in electrical characteristics of the TFT can be suppressed.

[0222]

After the protective film is formed, the semiconductor layer may be subjected to annealing (at 300 to 400 °C).

[0223]

Then, the insulating layer 4021 is formed as the planarizing insulating film. The insulating layer 4021 can be formed using an organic material having heat resistance, such as polyimide, acrylic, benzocyclobutene, polyamide, or epoxy. Other than such organic materials, it is also possible to use a low-dielectric constant material (a low-k material), a siloxane-based resin, PSG (phosphosilicate glass), BPSG (borophosphosilicate glass), or the like. Note that the insulating layer 4021 may be formed by stacking a plurality of insulating films formed using any of these materials.

[0224]

Note that a siloxane resin is a resin formed from a siloxane material as a starting material and having the bond of Si-O-Si. A siloxane-based resin may use, as a substituent, an organic group (e.g., an alkyl group, and an aryl group) or a fluoro group. The organic group may have a fluoro group.

[0225]

There is no particular limitation on the method for forming the insulating layer 4021, and the insulating layer 4021 can be formed, depending on the material, by a sputtering method, an SOG method, a spin coating method, a dipping method, a spray

coating method, a droplet discharge method (e.g., an inkjet method, screen printing, offset printing, or the like), a doctor knife, a roll coater, a curtain coater, a knife coater, or the like. In the case where the insulating layer 4021 is formed using a material solution, the semiconductor layer may be annealed (at 300 to 400 °C) at the same time as a baking step. The baking step of the insulating layer 4021 also serves as the annealing step of the semiconductor layer, whereby a semiconductor device can be manufactured efficiently.

[0226]

The pixel electrode layer 4030 and the counter electrode layer 4031 can be made of a light-transmitting conductive material such as indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium tin oxide (hereinafter referred to as ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added..

[0227]

A conductive composition containing a conductive high molecule (also referred to as a conductive polymer) can be used for forming the pixel electrode layer 4030 and the counter electrode layer 4031.It is preferable that the pixel electrode formed using a conductive composition have sheet resistance of 10000 Ω/square or less, and light transmittance of greater than or equal to 70 % at a wavelength of 550 nm. Further, it is preferable that the conductive high molecule contained in the conductive composition have resistance of less than or equal to 0.1 Ω·cm.

[0228]

As the conductive high molecule, a so-called π electron conjugated conductive high molecule can be used. For example, polyaniline and/or a derivative thereof, polypyrrole and/or a derivative thereof, polythiophene and/or a derivative thereof, and a copolymer of two or more kinds of those materials can be given.

[0229]

The variety of signals and potentials are supplied to the signal line driver circuit 4003 that is formed separately, and the scan line driver circuit 4004 or the pixel portion 4002 from an FPC 4018.

[0230]

In Embodiment 7, a connection terminal electrode 4015 is formed from the same conductive film as the pixel electrode layer 4030 included in the liquid crystal element 4013, and a terminal electrode 4016 is formed from the same conductive film as source and drain electrode layers of the thin film transistors 4010 and 4011.

[0231]

The connection terminal electrode 4015 is electrically connected to a terminal included in the FPC 4018 through an anisotropic conductive film 4019.

[0232]

Although FIGS. 20A1 and 20A2 illustrate an example in which the signal line driver circuit 4003 is formed separately and mounted on the first substrate 4001, this embodiment is not limited to this structure. The scan line driver circuit may be formed separately and then mounted, or only a part of the signal line driver circuit or a part of the scan line driver circuit may be formed separately and then mounted.

[0233]

FIG. 21 illustrates an example of a liquid crystal display module which is formed as a semiconductor device by using a TFT substrate 2600.

[0234]

FIG. 21 shows an example of a liquid crystal display module, in which the TFT substrate 2600 and a counter substrate 2601 are fixed to each other with a sealant 2602, and a pixel portion 2603 including a TFT and the like, a display element 2604 including a liquid crystal layer, a coloring layer 2605, and a polarizing plate 2606 are provided between the substrates to form a display region. A coloring layer 2605 is necessary to perform color display. In the case of the RGB system, respective coloring layers for red, green, and blue colors are provided for respective pixels. Polarizing plates 2606 and 2607 and a diffuser plate 2613 are provided outside the TFT substrate 2600 and the counter substrate 2601. A light source includes a cold cathode tube 2610 and a reflective plate 2611, and a circuit substrate 2612 is connected to a wiring circuit portion 2608 of the TFT substrate 2600 through a flexible wiring board 2609 and includes an external circuit such as a control circuit and a power source circuit. The polarizing plate and the liquid crystal layer may be stacked with a retardation film interposed therebetween.

[0235]

The liquid crystal display module can use any of the following modes: a TN (Twisted Nematic) mode, an IPS (In-Plane-Switching) mode, an FFS (Fringe Field Switching) mode, an MVA (Multi-domain Vertical Alignment) mode, a PVA (Patterned Vertical Alignment) mode, an ASM (Axially Symmetric aligned Micro-cell) mode, an OCB (Optical Compensated Birefringence) mode, an FLC (Ferroelectric Liquid Crystal) mode, an AFLC (AntiFerroelectric Liquid Crystal) mode, and the like.

[0236]

Through the above process, a liquid crystal display panel as a semiconductor device can be manufactured at reduced cost.

[0237]

This embodiment can be implemented in appropriate combination with any of the structures described in Embodiments 1 to 3.

[Embodiment 8]

[0238]

Electronic paper can be used for electronic devices of a variety of fields as long as they display data. For example, an electronic paper can be applied to an e-book reader (electronic book), a poster, an advertisement in a vehicle such as a train, or displays of various cards such as a credit card. Examples of the electronic devices are illustrated in FIGS. 23A and 23B and FIG. 24.

[0239]

FIG. 23A illustrates a poster 2631 formed using electronic paper. In the case where an advertising medium is printed paper, the advertisements are replaced by hands; however, by using electronic paper to which Embodiment 3 is applied, the advertisements can be changed in a short period of time. Further, stable images can be obtained without display defects. The poster may have a configuration capable of wirelessly transmitting and receiving data.

[0240]

FIG. 23B illustrates an advertisement 2632 in a vehicle such as a train. In the case where an advertising medium is printed paper, the advertisement is replaced by hands; however, by using electronic paper to which Embodiment 3 is applied, the advertising display can be changed in a short period of time with less manpower.

Furthermore, stable images can be obtained without display defects. The poster may have a configuration capable of wirelessly transmitting and receiving data.

[0241]

FIG. 24 illustrates an example of an e-book reader 2700. For example, the e-book reader 2700 includes two housings, a housing 2701 and a housing 2703. The housing 2701 and the housing 2703 are combined with a hinge 2711 so that the e-book reader 2700 can be opened and closed with the hinge 2711 as an axis. With such a structure, the e-book reader 2700 can operate like a paper book.

[0242]

A display portion 2705 and a display portion 2707 are incorporated in the housing 2701 and the housing 2703, respectively. The display portion 2705 and the display portion 2707 may display one image or different images. In the case where the display portion 2705 and the display portion 2707 display different images, for example, a display portion on the right side (the display portion 2705 in FIG. 24) can display text and a display portion on the left side (the display portion 2707 in FIG. 24) can display graphics.

[0243]

FIG. 24 illustrates an example in which the housing 2701 is provided with an operation portion and the like. For example, the housing 2701 is provided with a power switch 2721, an operation key 2723, a speaker 2725, and the like. With the operation key 2723, pages can be turned. Note that a keyboard, a pointing device, and the like may be provided on the same surface as the display portion of the housing. Furthermore, an external connection terminal (an earphone terminal, a USB terminal, a terminal that can be connected to various cables such as an AC adapter and a USB cable, or the like), a recording medium insertion portion, and the like may be provided on the back surface or the side surface of the housing. Moreover, the e-book reader 2700 may have a function of an electronic dictionary.

[0244]

The e-book reader 2700 may have a configuration capable of wirelessly transmitting and receiving data. Through wireless communication, desired book data or the like can be purchased and downloaded from an electronic book server.

[Embodiment 9]

[0245]

A semiconductor device according to one embodiment of the present invention can be applied to a variety of electronic devices (including an amusement machine). Examples of electronic devices include: television sets (also referred to as televisions or television receivers), monitor of computers or the like, cameras such as digital cameras or digital video cameras, digital photo frames, cellular phones (also referred to as mobile phones or mobile phone sets), portable game consoles, portable information terminals, audio reproducing devices, large-sized game machines such as pachinko machines, and the like.

[0246]

FIG. 25A illustrates an example of a television set 9600. In the television set 9600, a display portion 9603 is incorporated in a housing 9601. The display portion 9603 can display images. In FIG. 25A, the housing 9601 is supported by a stand 9605.

[0247]

The television set 9600 can be operated with an operation switch of the housing 9601 or a separate remote controller 9610. Channels and volume can be controlled with an operation key 9609 of the remote controller 9610 so that an image displayed on the display portion 9603 can be controlled. Furthermore, the remote controller 9610 may be provided with a display portion 9607 for displaying data output from the remote controller 9610.

[0248]

Note that the television set 9600 is provided with a receiver, a modem, and the like. With the use of the receiver, general television broadcasting can be received. Moreover, when the display device is connected to a communication network with or without wires via the modem, one-way (from a sender to a receiver) or two-way (between a sender and a receiver or between receivers) information communication can be performed.

[0249]

FIG. 25B illustrates an example of a digital photo frame 9700. For example, in the digital photo frame 9700, a display portion 9703 is incorporated in a housing 9701. Various images can be displayed on the display portion 9703.For example, the display portion 9703 can display data of an image shot by a digital camera or the like to

function as a normal photo frame.

[0250]

Note that the digital photo frame 9700 is provided with an operation portion, an external connection portion (a USB terminal, a terminal that can be connected to various cables such as a USB cable, or the like), a recording medium insertion portion, and the like. Although they may be provided on the same surface as the display portion, it is preferable to provide them on the side surface or the back surface for the design of the digital photo frame 9700. For example, a memory storing data of an image shot by a digital camera is inserted in the recording medium insertion portion of the digital photo frame, whereby the image data can be downloaded and displayed on the display portion 9703.

[0251]

The digital photo frame 9700 may transmit and receive data wirelessly. Through wireless communication, desired image data can be downloaded to be displayed.

[0252]

FIG. 26A is a portable game machine and includes two housings, a housing 9881 and a housing 9891, which are connected with a joint portion 9893 so that the portable game machine can be opened or folded. A display portion 9882 and a display portion 9883 are incorporated in the housing 9881 and the housing 9891, respectively. In addition, the portable game machine illustrated in FIG. 26A is provided with a speaker portion 9884, a recording medium insert portion 9886, an LED lamp 9890, input means (operation keys 9885, a connection terminal 9887, a sensor 9888 (having a function of measuring force, displacement, position, speed, acceleration, angular velocity, rotation number, distance, light, liquid, magnetism, temperature, chemical substance, sound, time, hardness, electric field, current, voltage, electric power, radial ray, flow rate, humidity, gradient, vibration, odor, or infrared ray), and a microphone 9889), and the like. It is needless to say that the structure of the portable amusement machine is not limited to the above as long as the structure is provided with at least a semiconductor device including the thin film transistor described in Embodiment 1 or 2. The portable amusement machine may include other accessory equipment as appropriate. The portable game machine illustrated in FIG. 26A has a function of

reading a program or data stored in a recording medium to display it on the display portion, and a function of sharing information with another portable game machine by wireless communication. Note that the function of the portable game machine illustrated in FIG. 26A is not limited to those described above, and the portable game machine can have a variety of functions.

[0253]

FIG. 26B illustrates an example of a slot machine 9900 which is a large-sized amusement machine. In the slot machine 9900, a display portion 9903 is incorporated in a housing 9901. In addition, the slot machine 9900 includes an operation means such as a start lever or a stop switch, a coin slot, a speaker, and the like. It is needless to say that the structure of the slot machine 9900 is not limited to the above as long as the structure is provided with at least a semiconductor device including the thin film transistor described in Embodiment 1 or 2. The slot machine 9900 may include other accessory equipment as appropriate.

[0254]

FIG. 27 illustrates an example of a mobile phone 1000. The mobile phone 1000 is provided with a display portion 1002 incorporated in a housing 1001, operation buttons 1003, an external connection port 1004, a speaker 1005, a microphone 1006, and the like.

[0255]

When the display portion 1002 of the mobile phone 1000 illustrated in FIG. 27 is touched with a finger or the like, data can be input into the mobile phone 1000. Furthermore, operations such as making calls and composing mails can be performed by touching the display portion 1002 with a finger or the like.

[0256]

There are mainly three screen modes of the display portion 1002. The first mode is a display mode mainly for displaying an image. The second mode is an input mode mainly for inputting information such as text. The third mode is a display-and-input mode in which two modes of the display mode and the input mode are mixed.

[0257]

For example, in the case of making a call or composing a mail, a text input

mode mainly for inputting text is selected for the display portion 1002 so that text displayed on a screen can be input. In that case, it is preferable to display a keyboard or number buttons on almost all the area of the screen of the display portion 1002.

[0258]

When a detection device including a sensor for detecting inclination, such as a gyroscope or an acceleration sensor, is provided inside the mobile phone 1000, display on the screen of the display portion 1002 can be automatically switched by determining the direction of the mobile phone 1000 (whether the mobile phone 1000 is placed horizontally or vertically for a landscape mode or a portrait mode).

[0259]

The screen mode is switched by touching the display portion 1002 or operating the operation buttons 1003 of the housing 1001. Alternatively, the screen modes can be switched depending on kinds of images displayed in the display portion 1002. For example, when a signal for an image displayed in the display portion is data of moving images, the screen mode is switched to the display mode, and whereas when the signal is text data, the screen mode is switched to the input mode.

[0260]

Moreover, in the input mode, when input by touching the display portion 1002 is not performed within a specified period while a signal detected by the optical sensor in the display portion 1002 is detected, the screen mode may be controlled so as to be switched from the input mode to the display mode.

[0261]

The display portion 1002 can also function as an image sensor. For example, an image of a palm print, a fingerprint, or the like is taken by touching the display portion 1002 with the palm or the finger, whereby personal authentication can be performed. Furthermore, by providing a backlight or a sensing light source emitting a near-infrared light for the display portion, an image of a finger vein, a palm vein, or the like can also be taken.

[Embodiment 10]

[0262]

The examples in which a buffer layer is provided are described in Embodiments 1 and 2. In this embodiment, an example in which a buffer layer is not

provided will be described. Further, an example in which an inverter circuit is formed using two n-channel thin film transistors will be described below.

[0263]

A driver circuit for driving a pixel portion is formed using an inverter circuit, a capacitor, a resistor, and the like. When two n-channel TFTs are combined to form an inverter circuit, there are two types of combinations: a combination of an enhancement type transistor and a depression type transistor (hereinafter, a circuit formed by such a combination is referred to as an "EDMOS circuit") and a combination of enhancement type TFTs (hereinafter, a circuit formed by such a combination is referred to as an "EEMOS circuit"). Note that when the threshold voltage of the n-channel TFT is positive, the n-channel TFT is defined as an enhancement type transistor, while when the threshold voltage of the n-channel TFT is negative, the n-channel TFT is defined as a depression type transistor, and this specification follows the above definitions.

[0264]

The pixel portion and the driver circuit are formed over the same substrate. In the pixel portion, ON/OFF of voltage application to a pixel electrode is switched using enhancement type transistors arranged in a matrix. An oxide semiconductor is used for these enhancement type transistors arranged in the pixel portion. Since the enhancement type transistor has electric characteristics such as an on/off ratio of greater than or equal to 10^9 at a gate voltage of $\pm$ 20 V, leakage current is small and low power consumption drive can be realized.

[0265]

FIG. 32A illustrates a cross-sectional structure of the inverter circuit of the driver circuit. In FIG. 32A, a first gate electrode 1401 and a second gate electrode 1402 are provided over a substrate 1400. The first gate electrode 1401 and the second gate electrode 1402 each can be formed to have a single-layer structure or a stacked-layer structure using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material containing any of these materials as its main component.

[0266]

For example, as a two-layer structure of each of the first gate electrode 1401 and the second gate electrode 1402, the following structures are preferable: a two-layer

structure of an aluminum layer and a molybdenum layer stacked thereover, a two-layer structure of a copper layer and a molybdenum layer stacked thereover, a two-layer structure of a copper layer and a titanium nitride layer or a tantalum nitride layer stacked thereover, and a two-layer structure of a titanium nitride layer and a molybdenum layer. As a three-layer structure, a stack of a tungsten layer or a tungsten nitride layer, a layer of an alloy of aluminum and silicon or an alloy of aluminum and titanium, and a titanium nitride layer or a titanium layer is preferable.

[0267]

Further, a first wiring 1409, a second wiring 1410, and a third wiring 1411 are provided over a gate insulating layer 1403 that covers the first gate electrode 1401 and the second gate electrode 1402. The second wiring 1410 is directly connected to the second gate electrode 1402 through a contact hole 1404 formed in the gate insulating layer 1403.

[0268]

Further, a first oxide semiconductor layer 1405 which is on and in contact with the first wiring 1409 and the second wiring 1410 is provided at a position overlapping with the first gate electrode 1401, and a second oxide semiconductor layer 1407 which is on and in contact with the second wiring 1410 and the third wiring 1411 is provided at a position overlapping with the second gate electrode 1402.

[0269]

A first thin film transistor 1430 includes the first gate electrode 1401 and the first oxide semiconductor layer 1405 that overlaps with the first gate electrode 1401 with the gate insulating layer 1403 interposed therebetween, and the first wiring 1409 is a power supply line at a ground potential (a ground power supply line). This power supply line at a ground potential may be a power supply line to which a negative voltage VDL is applied (a negative power supply line).

[0270]

In addition, the second thin film transistor 1431 includes the second gate electrode 1402 and the second oxide semiconductor layer 1407 overlapped with the second gate electrode 1402 with the gate insulating layer 1403 interposed therebetween, and the third wiring 1411 is a power supply line to which a positive voltage VDD is applied (a positive power supply line).

[0271]

Tapered shapes of the side surfaces of the first wiring 1409 and the second wiring 1410 which face each other with the first oxide semiconductor layer 1405 interposed therebetween enable respective regions of the oxide semiconductor layer, which overlap with the side surfaces of the source electrode layer and the drain electrode layer to function as electric-field relaxation regions.

[0272]

Further, tapered shapes of the side surfaces of the second wiring 1410 and the third wiring 1411 which face each other with the second oxide semiconductor layer 1407 interposed therebetween enable respective regions of the oxide semiconductor layer, which overlap with the side surfaces of the source electrode layer and the drain electrode layer to function as electric-field relaxation regions.

[0273]

As illustrated in FIG. 32A, the second wiring 1410 which is electrically connected to both the first oxide semiconductor layer 1405 and the second oxide semiconductor layer 1407 is directly connected to the second gate electrode 1402 of the second thin film transistor 1431 through the contact hole 1404 formed in the gate insulating layer 1403. The second wiring 1410 and the second gate electrode 1402 are directly connected to each other, whereby favorable contact can be obtained, which leads to reduction in contact resistance. In comparison with the case where the second gate electrode 1402 and the second wiring 1410 are connected to each other with another conductive film, e.g., a transparent conductive film interposed therebetween, a reduction in the number of contact holes and a reduction in an area occupied by the driver circuit by the reduction in the number of contact holes can be achieved.

[0274]

Further, FIG. 32C is a top view of the inverter circuit of the driver circuit. A cross section taken along chain line Z1-Z2 of FIG. 32C corresponds to FIG. 32A.

[0275]

Further, FIG. 32B illustrates an equivalent circuit of the EDMOS circuit. The circuit connection illustrated in FIGS. 32A and 32C corresponds to that illustrated in FIG. 32B. Illustrated is an example in which the first thin film transistor 1430 is an enhancement-type n-channel transistor and the second thin film transistor 1431 is a

depression-type n-channel transistor.

[0276]

Although the example of an EDMOS circuit is described in this embodiment, the driver circuit may be formed using an EEMOS circuit in which enhancement-type n-channel transistors are used.

[0277]

Further, although the example in which a buffer layer is not provided is described in this embodiment, the present invention is not limited thereto and a buffer layer may be provided over the first wiring 1409, the second wiring 1410, and the third wiring 1411 like in Embodiment 1.

[0278]

This embodiment can be freely combined with any one of Embodiments 1 to 9.

[Embodiment 11]

[0279]

In Embodiment 11, the degradation of electrical characteristics of thin film transistors having model structures shown in FIGS. 33A to 33C when stress is applied was calculated.

[0280]

In a structure shown in FIG. 33A, a gate electrode layer 302 and a gate insulating layer 303 are stacked over a glass substrate 301 in this order, and a source electrode layer 304 and a drain electrode layer 305 are formed thereover. An oxide layer 307 and an oxide layer 308 are provided on the side surface of the source electrode layer 304 and the side surface of the drain electrode layer 305 respectively. The oxide layers 307 and 308 here are respective native oxide films of the source electrode layer 304 and the drain electrode layer 305. An oxide semiconductor layer 306 is formed to cover the source electrode layer 304, the drain electrode layer 305, and the oxide layers 307 and 308.

[0281]

In this embodiment, the gate electrode layer 302 was formed using molybdenum, and the source electrode layer 304 and the drain electrode layer 305 were formed using the same material as the gate electrode layer 302. The gate insulating layer 303 was a silicon oxide film, and thickness thereof was 100 nm and relative

permittivity εr thereof was 4.1. The thickness of the oxide semiconductor layer 306 was 50 nm and a material thereof was an In-Ga-Zn-O-based non-single-crystal film. Channel length L of the thin film transistor was 10 μm and channel width W thereof was 10 μm.

[0282]

As for the stress which was applied to the thin film transistor, gate voltage Vgs was set to 2 V and source-drain voltage Vds was set to 20 V. The period of time during which the stress is applied was 1000 seconds, and the electrical characteristics before and after the stress application were compared to each other.

[0283]

Device simulator "Atlas" made by Silvaco was used for the calculation.

[0284]

Further, the calculation was performed in the respective cases where the taper angles θ1 of the source electrode layer 304 are 27°, 45°, and 63°. The taper angle θ1 of the source electrode layer 304 was set to be the same angle as the taper angle θ2 of the drain electrode layer 305.

[0285]

Calculation results in the case where the taper angle θ1 of the source electrode layer 304 is 27° are shown in FIG. 34.

[0286]

Calculation results in the case where the taper angle θ1 of the source electrode layer 304 is 45° are shown in FIG. 35.

[0287]

Calculation results in the case where the taper angle θ1 of the source electrode layer 304 is 63° are shown in FIG. 36.

[0288]

From these results of FIGS. 34 to 36, such result that the degradation becomes smaller as the taper angle θ1 of the source electrode layer 304 is smaller can be obtained.

[0289]

For comparison, the result of the calculation which was performed in the

similar manner on a structure shown in FIG. 33B where taper angle θ1 is 90° is shown in FIG. 37A. The structure shown in FIG. 33B is the same as the structure shown in FIG. 33A except that the taper angle θ1 is different from that in FIG. 33A.

[0290]

Furthermore, for comparison, the result of the calculation which was performed in the similar manner on a structure shown in FIG. 33C where taper angle θ1 is 27° and no oxide layer is formed on the side surface of each of a source electrode layer 304 and a drain electrode layer 305 is shown in FIG. 37B. Changing of the taper angle θ1 made no difference in the results as long as there is no oxide layer on the side surface of each electrode layer. In the case where there is no oxide layer on the side surface of each electrode layer, the interface between the gate insulating layer 303 and the oxide semiconductor layer 306 corresponds to a current path, and therefore, the taper angle of the side surface of the source electrode layer 304 does not affect the current path.

[0291]

From these results, it can be said that degradation of the electrical characteristics of the thin film transistor can be suppressed by providing the oxide layer 307 and the oxide layer 308 on the respective side surfaces of the source electrode layer 304 and the drain electrode layer 305 and setting the taper angle θ1 to be smaller than 90°.

[0292]

The embodiments described above will be described in more detail in examples below.

[Example 1]

[0293]

In this example, characteristics of a thin film transistor manufactured using an oxide semiconductor layer will be described.

[0294]

The method for manufacturing a transistor used in this example will be described below.

[0295]

First, a first conductive film was formed over a substrate and patterned by a

photolithography method to form a gate electrode 502. Then, a gate insulating layer 503 was formed over the gate electrode 502. Then, a second conductive film and a buffer layer were formed over the gate insulating layer 503. The second conductive film and the buffer layer were formed successively without exposing the substrate to the air. Then, the second conductive film and the buffer layer were patterned by a photolithography method, so that a source electrode layer 506a and a drain electrode layer 506b respective parts of which overlap with the gate electrode were formed. Then, an oxide semiconductor layer was formed over the gate insulating layer, the source electrode layer, and the drain electrode layer and patterned by a photolithography method to form an island-shaped oxide semiconductor layer 510 which functions as a channel formation region. Then, thermal treatment at 350 °C for 1 hour was performed under a nitrogen atmosphere.

[0296]

As the substrate, a glass substrate manufactured by ASAHI GLASS CO., LTD. (product name: AN 100) was used.

[0297]

As the first conductive film for forming the gate electrode 502, a tungsten film with a thickness of 100 nm was formed by a sputtering method.

[0298]

As the gate insulating layer 503, a silicon oxynitride film with a thickness of 100 nm was formed by a plasma CVD method.

[0299]

As the second conductive film for forming the source electrode layer 506a and the drain electrode layer 506b, a tungsten film with a thickness of 100 nm was formed by a sputtering method.

[0300]

As the buffer layer, an In-Ga-Zn-O-based non-single-crystal film with a thickness of 5 to 10 nm was formed by a sputtering method. As for the film deposition condition, only an argon gas was used and a target in which In_2O_3:Ga_2O_3:ZnO = 1:1:1 was used.

[0301]

As the oxide semiconductor layer, an In-Ga-Zn-O-based non-single-crystal film

with a thickness of 150 nm was formed by a sputtering method. The film deposition condition was as follows: the pressure was 0.4 Pa, the power was 500 W, the film deposition temperature was 25 °C, the argon gas flow rate was 10 sccm, the oxygen flow rate was 5 sccm, the distance between the glass substrate and the target was 170 mm, and a direct-current (DC) power source was used. As the target, a target in which In_2O_3:Ga_2O_3:ZnO = 1:1:1 (In:Ga:Zn = 1:1:0.5) was used. After a plasma treatment was performed, the oxide semiconductor layer was formed successively without exposing a substrate 500 to the air. From the measurement with inductively coupled plasma mass spectrometry (ICP-MS), the composition of the oxide semiconductor layer obtained by this film deposition condition was $InGa_{0.94}Zn_{0.40}O_{3.31}$.

[0302]

FIG. 28 is a graph showing a V_g-I_d curve of a thin film transistor. In this example, the drain voltage (a voltage which is applied to the drain with respect to a voltage which is applied to the source) was set to 1 V for the measurement.

[0303]

In this example also, the structure of the transistor was as follows, which is shown in FIG. 29. In specific, channel length L of the transistor was set to 100 μm, channel width W of the transistor was set to 100 μm, length Ls where the source electrode layer 506a and the gate electrode 502 overlap with each other was set to 5 μm, length Ld where the drain electrode layer 506b and the gate electrode 502 overlap with each other was set to 5 μm, and each length A where the oxide semiconductor layer 510 does not overlap with either the source electrode layer 506a or the drain electrode layer 506b in the direction which is parallel to the channel width was set to 5 μm.

[0304]

Through the above, it was found that the successive formation of the second conductive film and the buffer layer without exposing the substrate to the air enables the on/off ratio of the transistor to be increased and the electron field-effect mobility to be increased.

[Example 2]

[0305]

In this example, one example of the electrode shape after etching will be

described. First, the process for manufacturing a sample will be described using FIGS. 30A to 30C. The sample is different from the thin film transistor described in Example 1 only in the cross-sectional shape of each of a source electrode layer and a drain electrode layer and in that a buffer layer is not formed, and will be described using the same reference numerals for the same portions as those of the thin film transistor described in Example 1.

[0306]

First, a first conductive film was formed over a substrate and patterned by a photolithography method to form a gate electrode 502. Then, a gate insulating layer 503 was formed over the gate electrode 502 (see FIG. 30A). Then, a second conductive film was formed over the gate insulating layer 503. Then, the second conductive film was patterned by a photolithography method, so that a source electrode layer 606a and a drain electrode layer 606b respective parts of which overlap with the gate electrode were formed (see FIG. 30B). Then, an oxide semiconductor layer was formed over the gate insulating layer, the source electrode layer, and the drain electrode layer and patterned by a photolithography method to form an island-shaped oxide semiconductor layer 610 which functions as a channel formation region was formed (see FIG. 30C).

[0307]

As the substrate, a glass substrate manufactured by ASAHI GLASS CO., LTD. (product name: AN 100) was used.

[0308]

As the first conductive film for forming the gate electrode 502, a tungsten film with a thickness of 100 nm was formed by a sputtering method.

[0309]

As the gate insulating layer 503, a silicon oxynitride film with a thickness of 100 nm was formed by a plasma CVD method.

[0310]

As the second conductive film for forming the source electrode layer 606a and the drain electrode layer 606b, a tungsten film with a thickness of 100 nm was formed by a sputtering method.

[0311]

As the oxide semiconductor layer, an In-Ga-Zn-O-based non-single-crystal film with a thickness of 150 nm was formed by a sputtering method. The film deposition condition thereof was the same as that in Example 1.

[0312]

The source electrode layer 606a and the drain electrode layer 606b were etched by using an ICP etching apparatus using a coiled antenna. The etching was performed by generating plasma under the following condition: the gas flow rate of CF_4 was set to 25 sccm, the gas flow rate of Cl_3 was set to 25 sccm, the gas flow rate of O_2 was set to 10 sccm, and an RF (13.56 MHz) power of 500 W was applied to a coiled electrode at a pressure of 1.5 Pa. An RF (13.56 MHz) power of 10 W was applied to the substrate side (sample stage), which means that a negative self-bias voltage was substantially applied thereto. This etching was stopped when at least the gate insulating film 503 is exposed to some extent, thereby forming the side surface of the electrode, which has a step.

[0313]

By the above etching condition, with respect to the cross-sectional shape of the source electrode layer 606a, the angle θ1 formed between the surface of the substrate and the bottom edge of the side surface of the source electrode layer 606a can be made to be greater than or equal to 20° and less than 90°. The cross-sectional photograph of the portion surrounded by a dotted line in FIG. 30C is FIG. 31A. FIG. 31B is a pattern diagram of FIG. 31A. As shown in FIG. 31A, θ1 was about 40°. Further, as shown in FIG. 31A, the angle formed between the surface of the substrate and the top edge of the side surface of the source electrode layer 606a was about 90°. The cross section of the side surface of the source electrode layer 606a and that of the side surface of the drain electrode layer 606b, which face each other with the oxide semiconductor layer 610 interposed therebetween have substantially the same shape as each other because the same etching step is performed thereon.

[0314]

From this example, it can be said that it can be suggested that the cross-sectional shape of each of the source electrode layer and the drain electrode layer described in Embodiment 2 is manufactured.

This application is based on Japanese Patent Application serial no. 2008-287187 filed with Japan Patent Office on November 7, 2008, the entire contents of which are hereby incorporated by reference.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a gate electrode formed over a substrate having an insulating surface;

an insulating layer formed over the gate electrode;

a source and drain electrodes formed over the insulating layer; and

an oxide semiconductor layer formed between a side surface of the source electrode and a side surface of the drain electrode, which face each other, so as to overlap with the gate electrode with the insulating layer interposed therebetween,

wherein the oxide semiconductor layer is in contact with at least the respective side surfaces of the source and drain electrodes, and

wherein a first angle formed between a surface of the substrate and the side surface of the source electrode and a second angle formed between the surface of the substrate and the side surface of the drain electrode are each greater than or equal to 20° and less than 90°.

ABSTRACT OF THE DISCLOSURE

A structure by which electric-field concentration which might occur between a source electrode and a drain electrode in a bottom-gate thin film transistor is relaxed and deterioration of the switching characteristics is suppressed, and a manufacturing method thereof. A bottom-gate thin film transistor in which an oxide semiconductor layer is provided over a source and drain electrodes is manufactured, and angle θ1 of the side surface of the source electrode which is in contact with the oxide semiconductor layer and angle θ2 of the side surface of the drain electrode which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the distance from the top edge to the bottom edge in the side surface of each electrode is increased.

FIG. 1

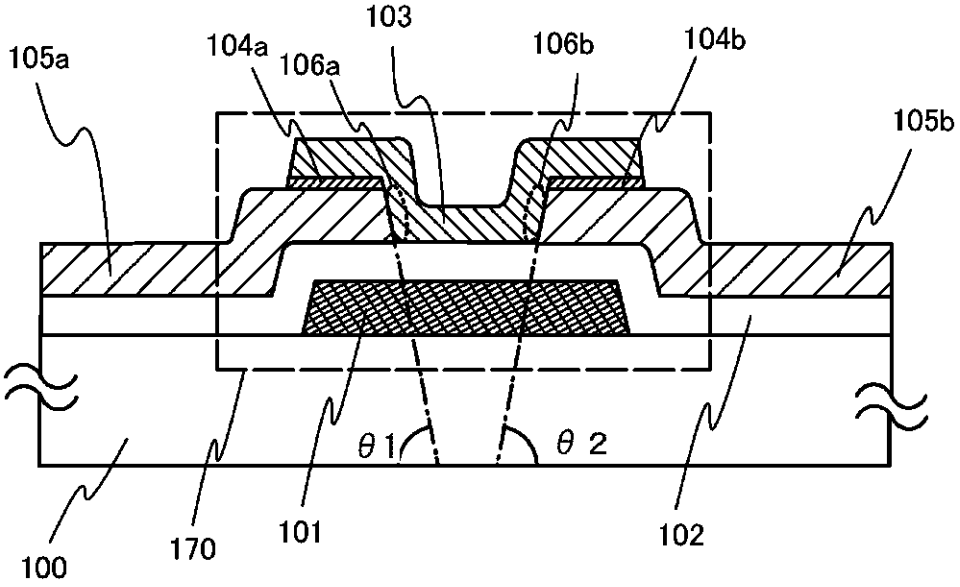
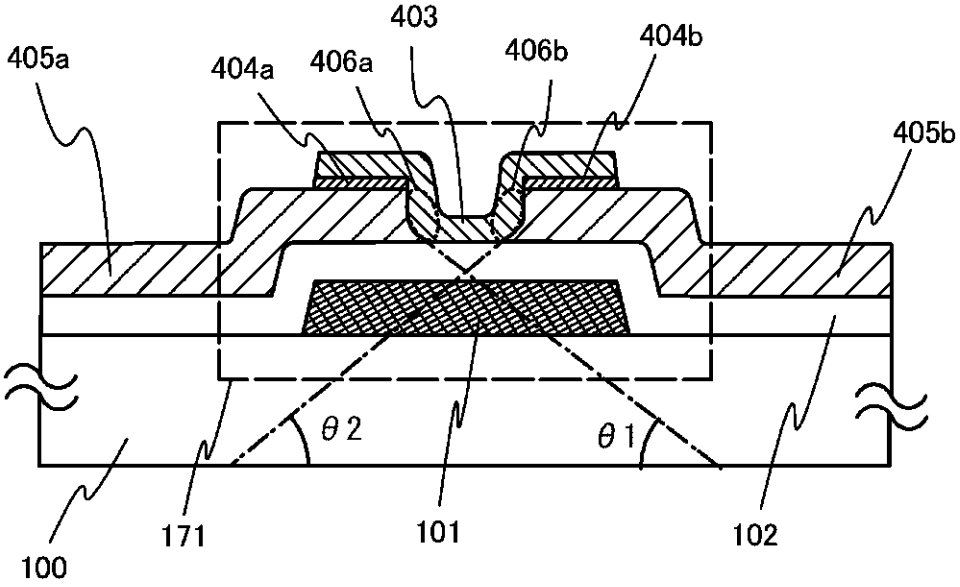


FIG. 2



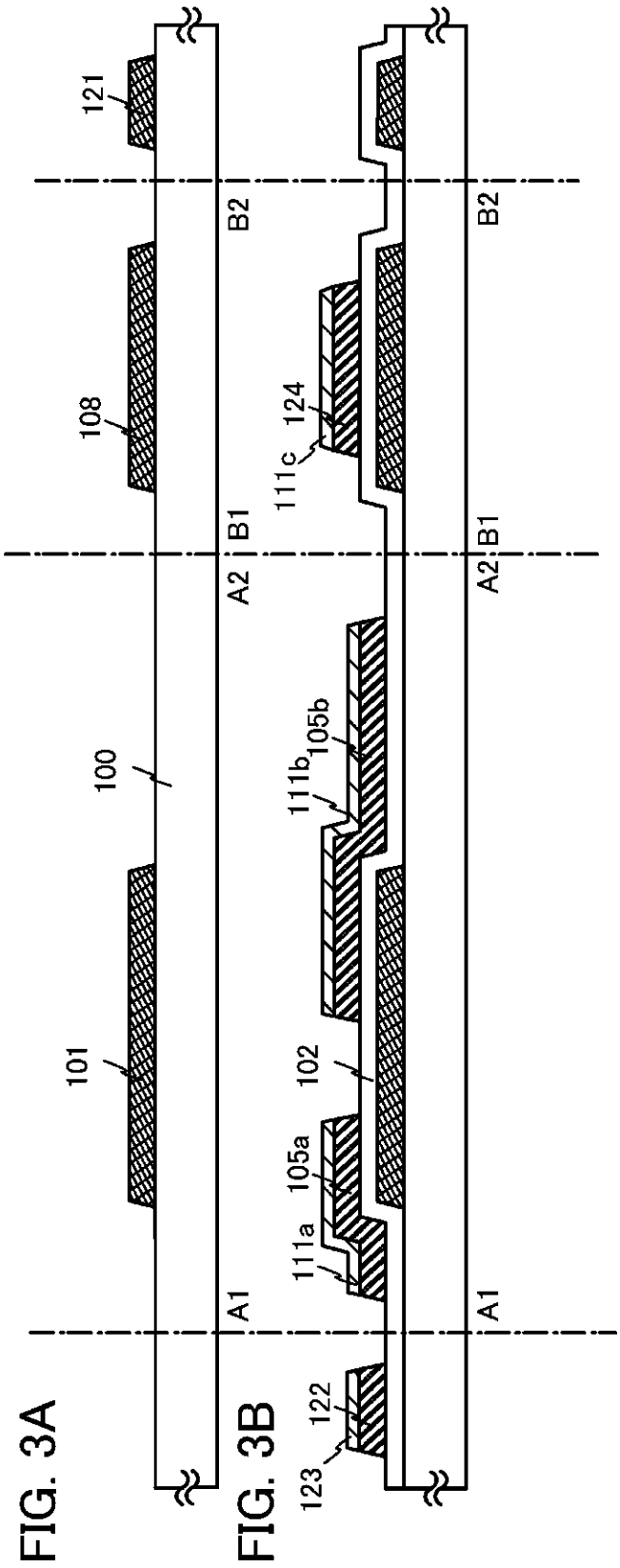

121
108
124
111c
105b
111b
100
101
102
105a
111a
122
123
A1
A2
B1
B2

FIG. 3A

FIG. 3B

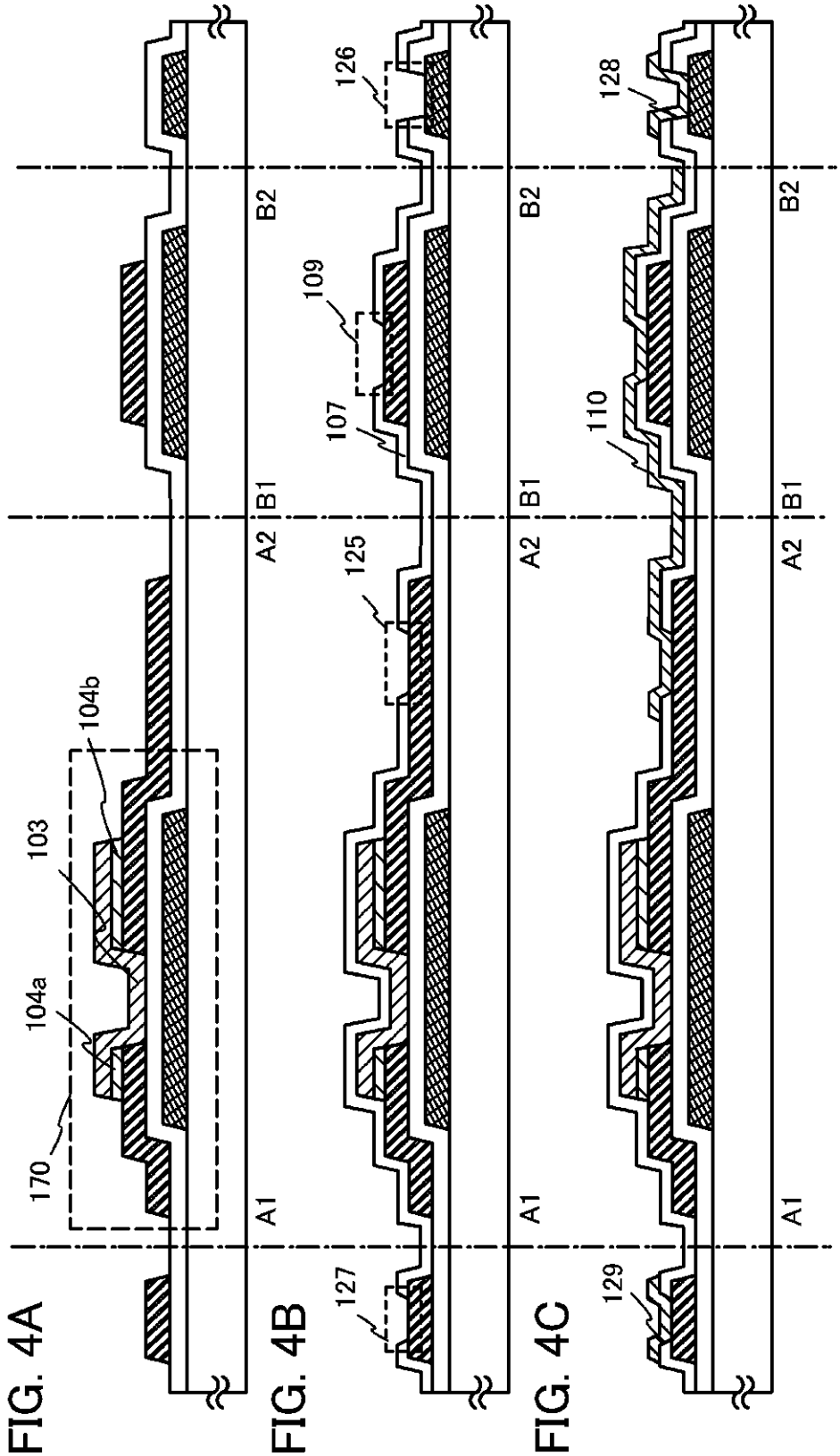

170
104a
103
104b
A1
A2
B1
B2
FIG. 4A
127
125
109
107
126
A1
A2
B1
B2
FIG. 4B
129
110
128
A1
A2
B1
B2
FIG. 4C

FIG. 5

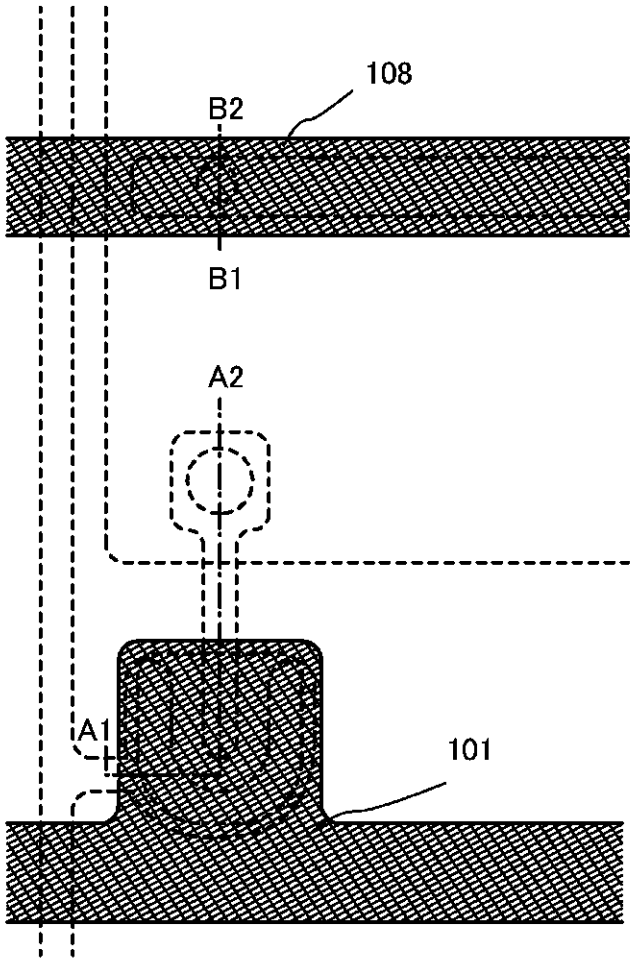


FIG. 6

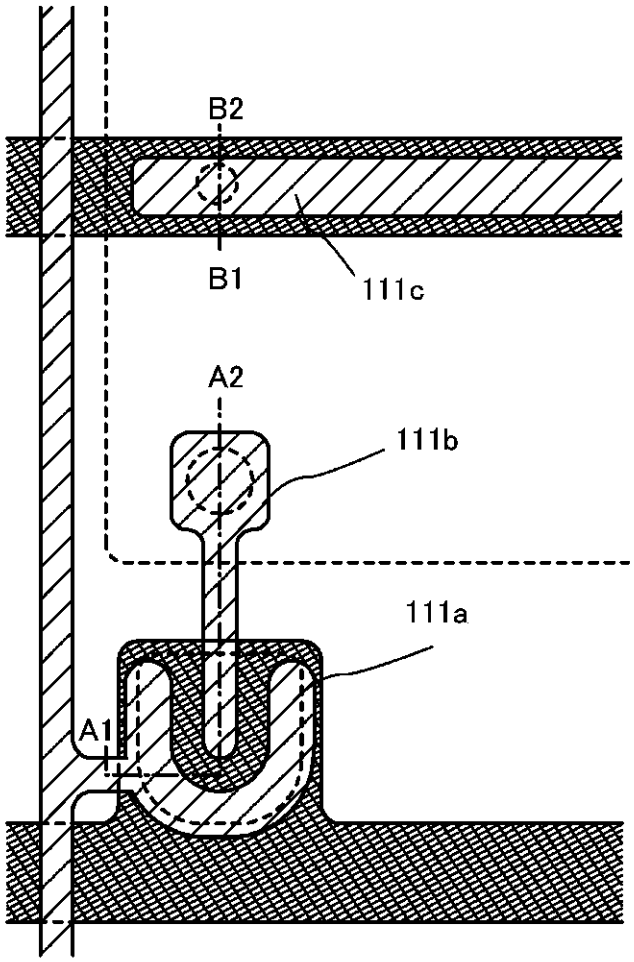


FIG. 7

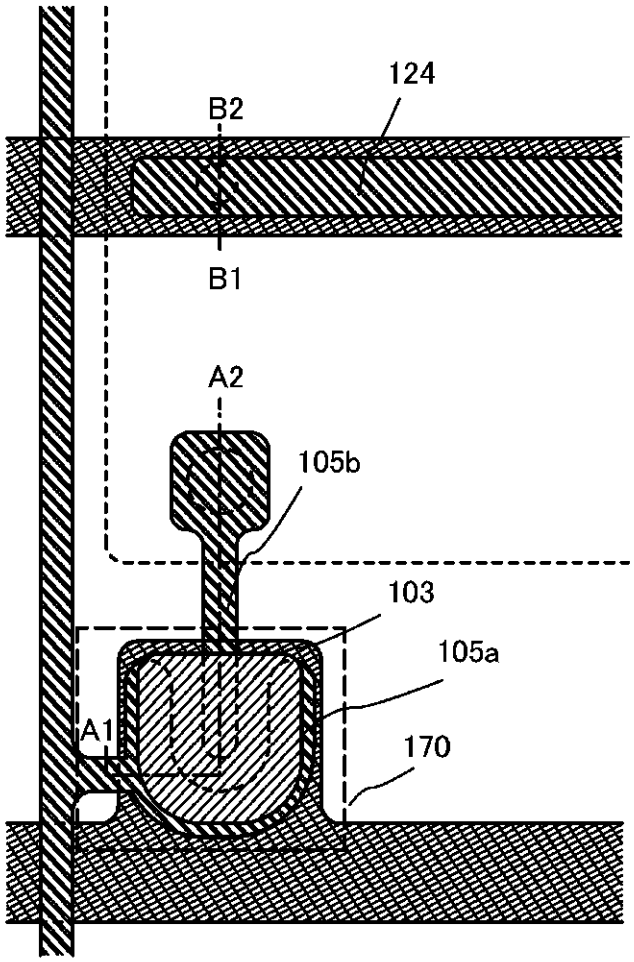


FIG. 8

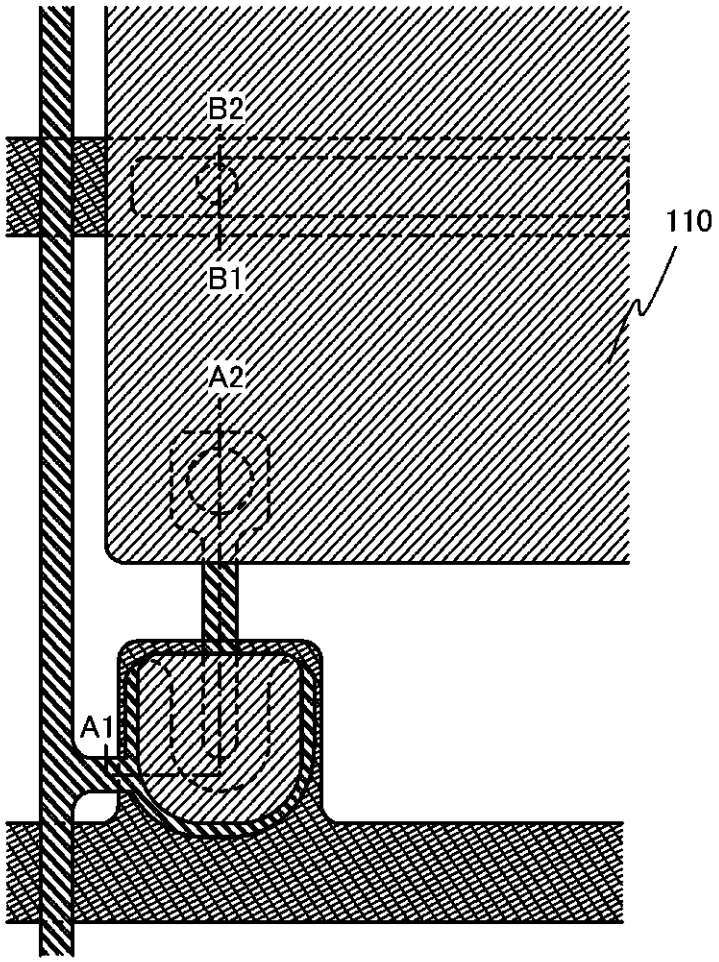


FIG. 9A1

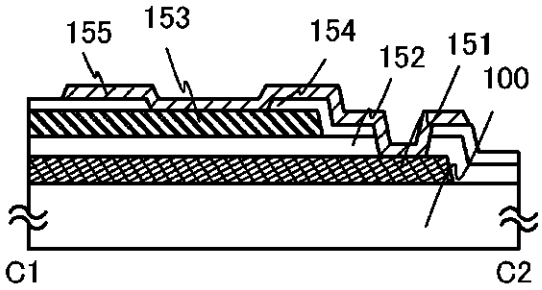


FIG. 9A2

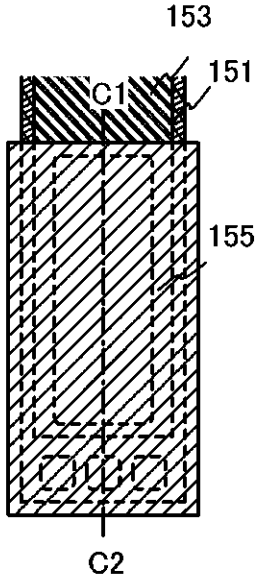


FIG. 9B1

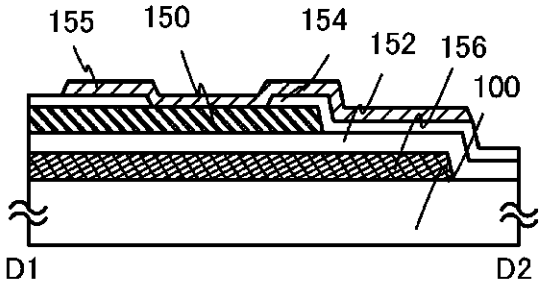


FIG. 9B2

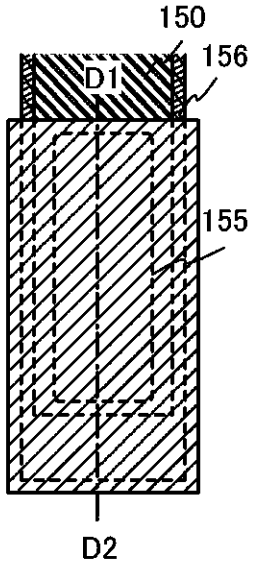


FIG. 10

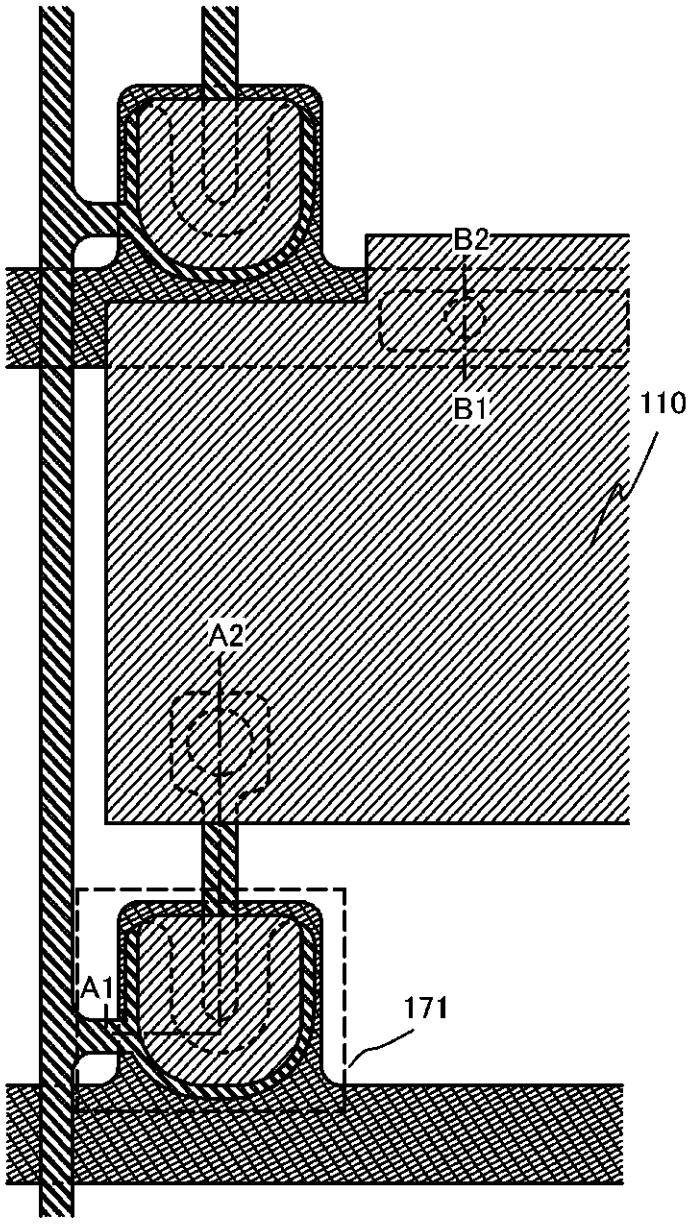


FIG. 11

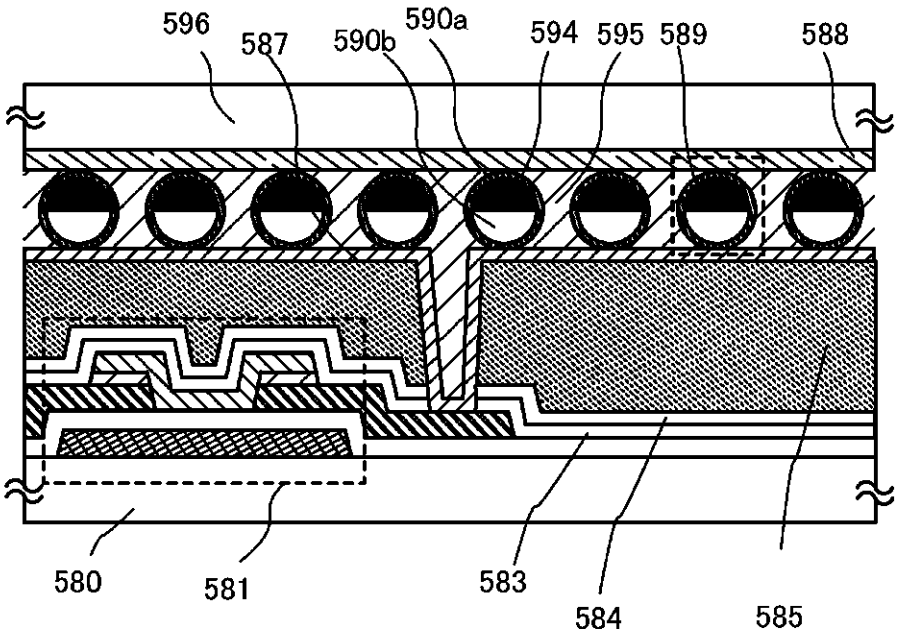


FIG. 12A

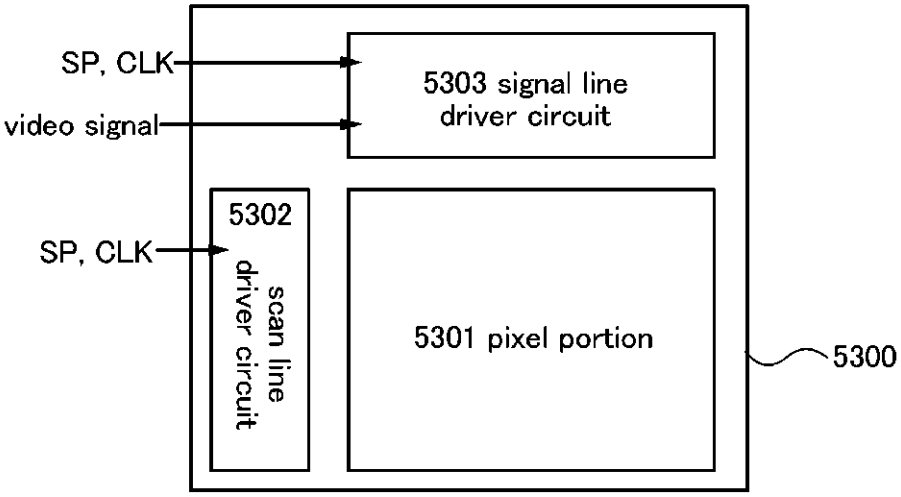


FIG. 12B

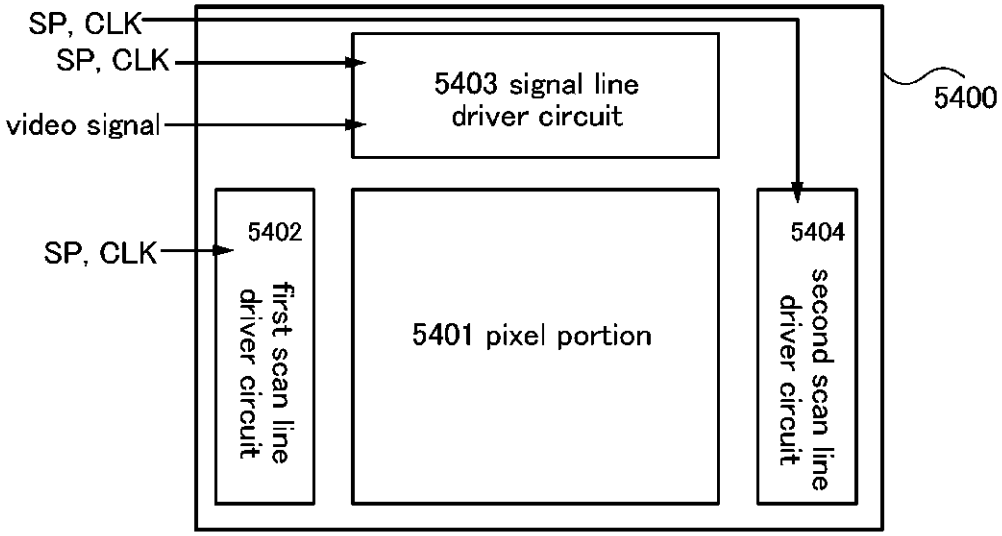


FIG. 13

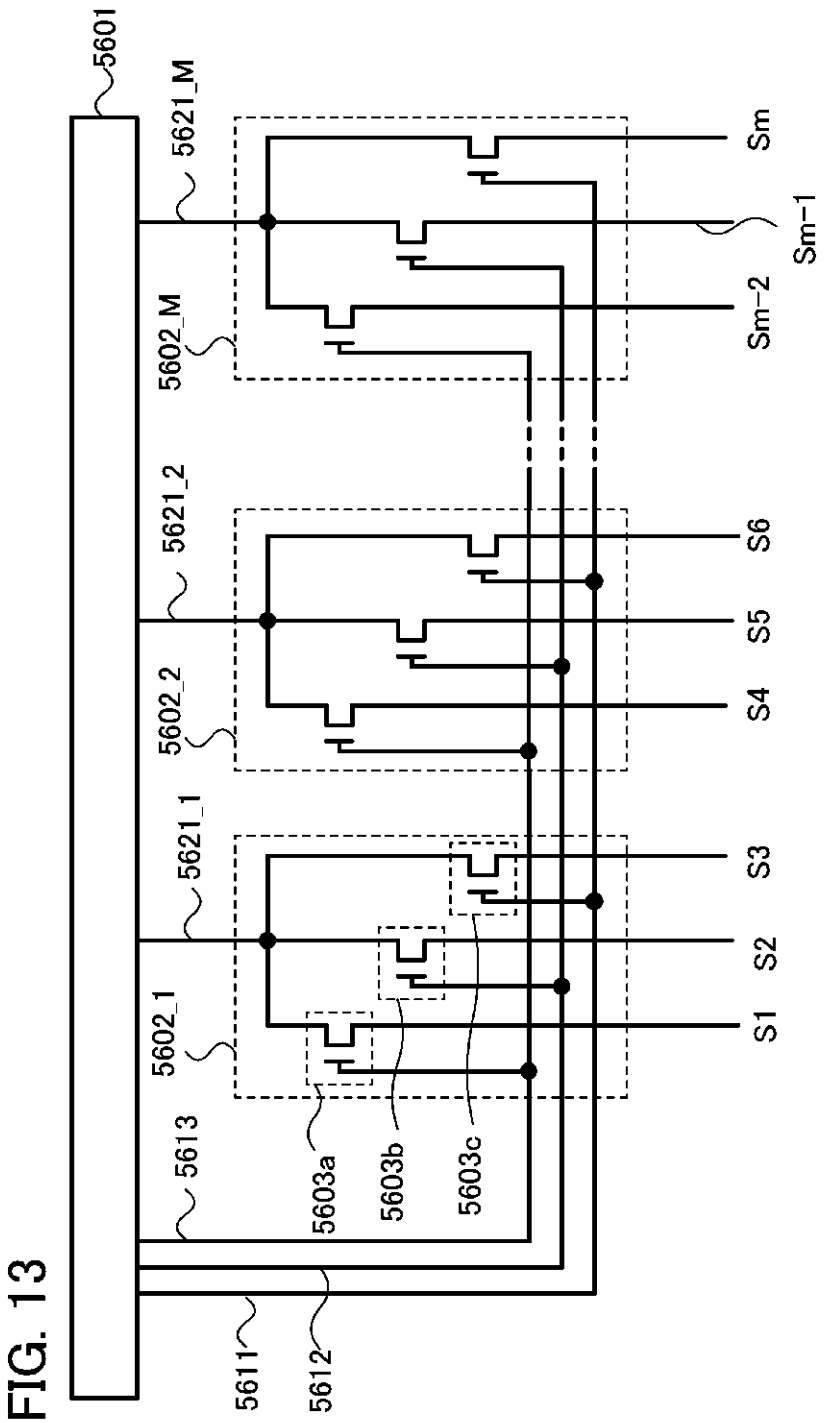

5601
5621_M
5602_M
5621_2
5602_2
5621_1
5602_1
5613
5611
5612
5603a
5603b
5603c
Sm
Sm−1
Sm−2
S6
S5
S4
S3
S2
S1

FIG. 14

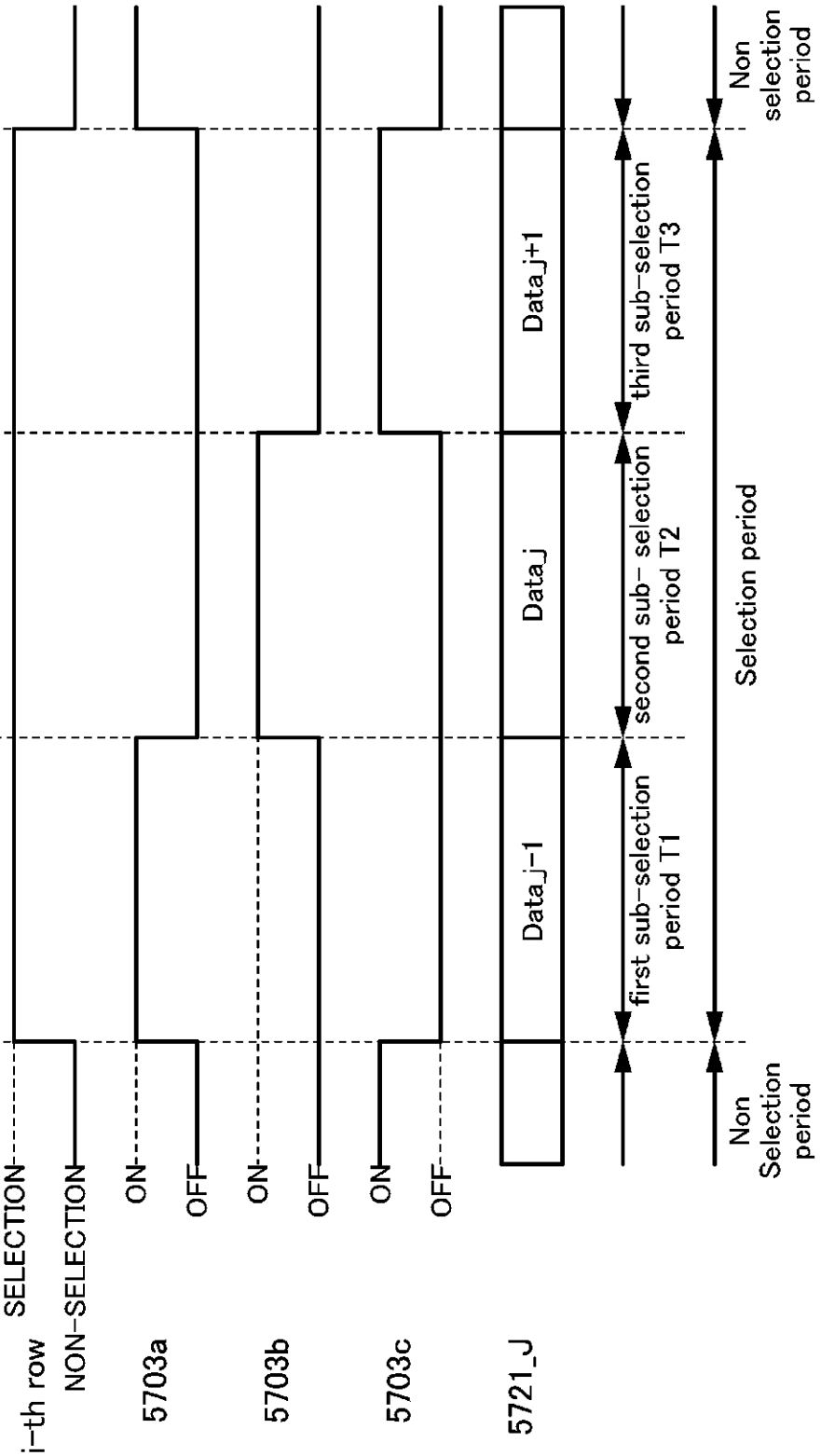

SELECTION
i-th row
NON-SELECTION
5703a
ON
OFF
5703b
ON
OFF
5703c
ON
OFF
5721_J
Data_j-1
Data_j
Data_j+1
first sub-selection period T1
second sub- selection period T2
third sub-selection period T3
Selection period
Non Selection period
Non selection period

FIG. 15

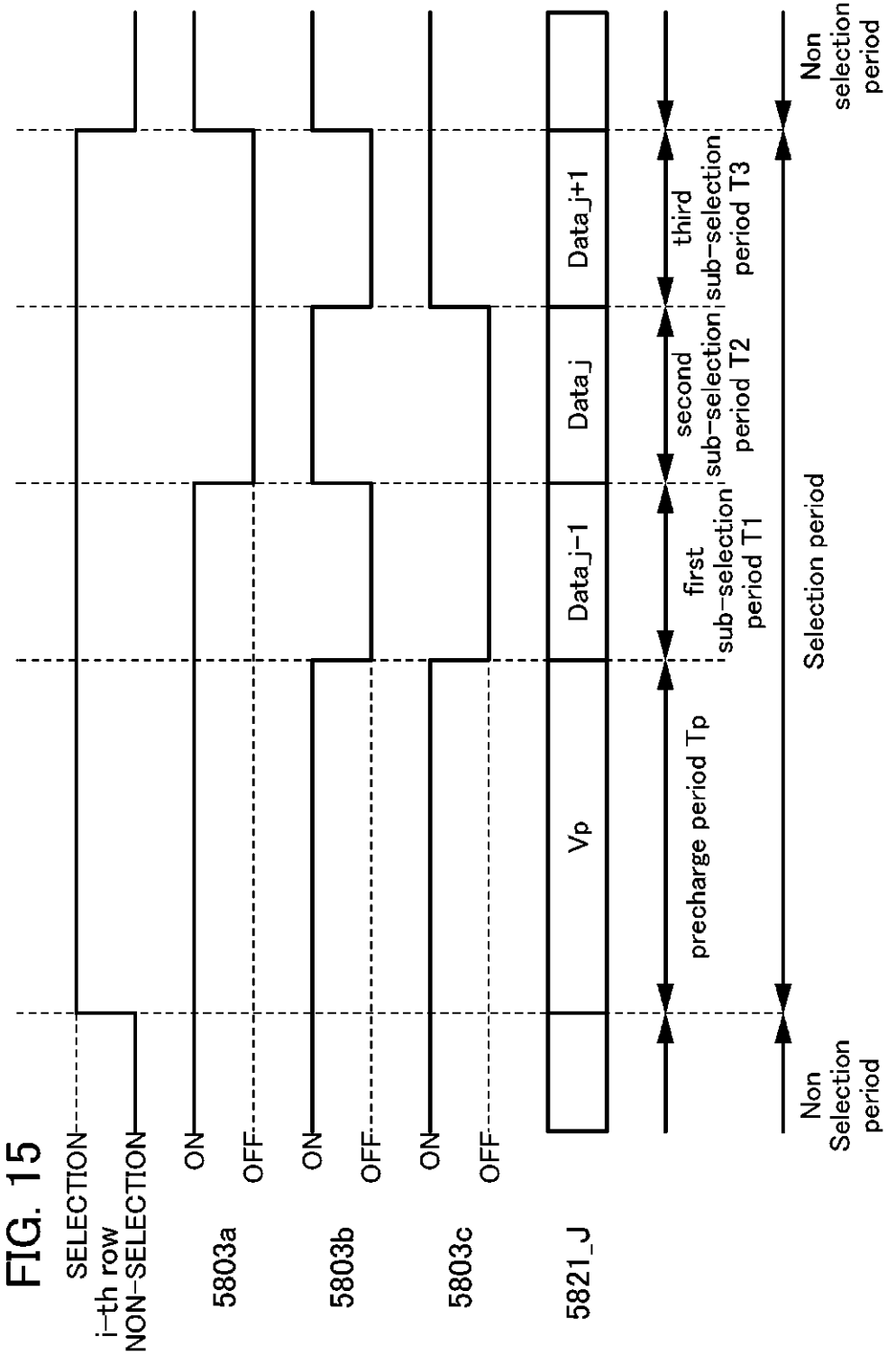

SELECTION
i-th row
NON-SELECTION
ON
OFF
5803a
ON
OFF
5803b
ON
OFF
5803c
Vp
Data_j-1
Data_j
Data_j+1
5821_J
precharge period Tp
first sub-selection period T1
second sub-selection period T2
third sub-selection period T3
Selection period
Non Selection period
Non selection period

FIG. 16

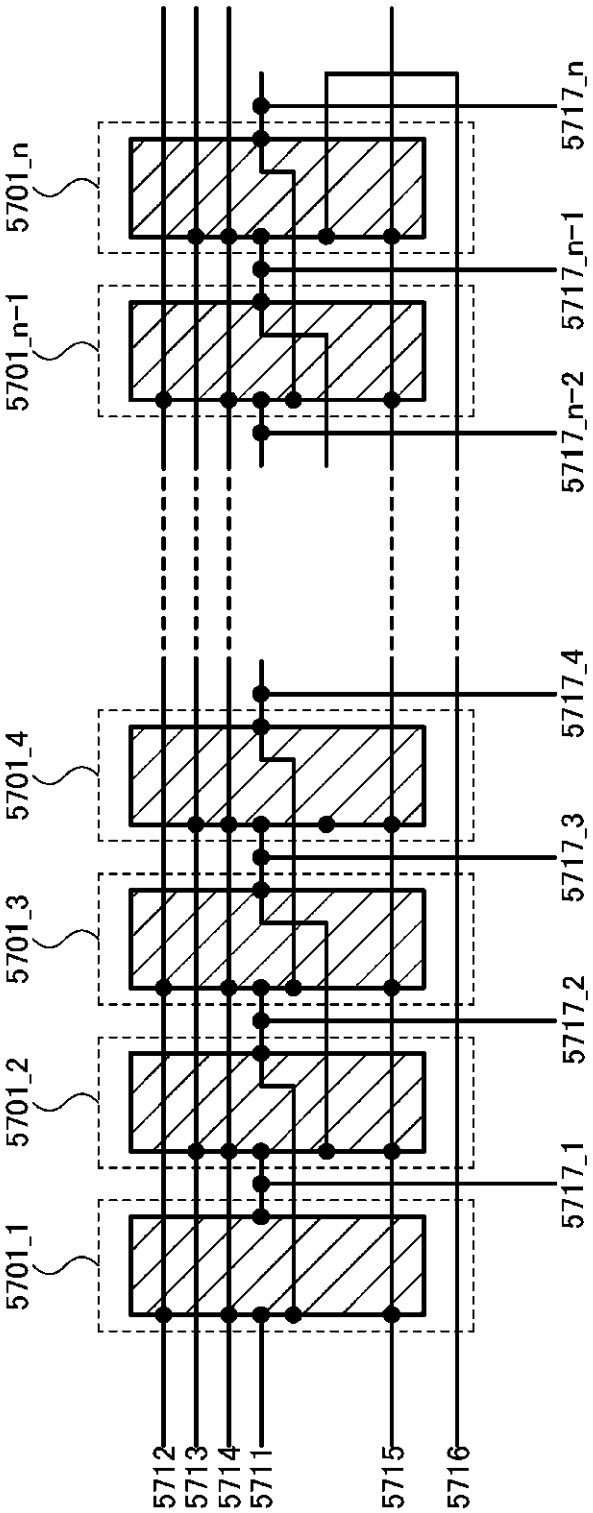

5701_1
5701_2
5701_3
5701_4
5701_n-1
5701_n
5711
5712
5713
5714
5715
5716
5717_1
5717_2
5717_3
5717_4
5717_n-2
5717_n-1
5717_n

FIG. 17

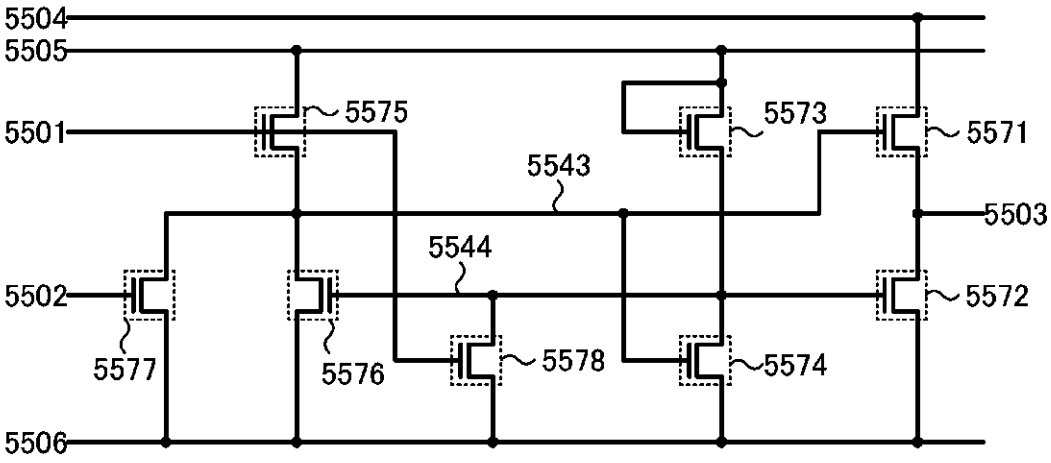

5504
5505
5501
5575
5573
5571
5543
5503
5544
5502
5572
5577
5576
5578
5574
5506

FIG. 18

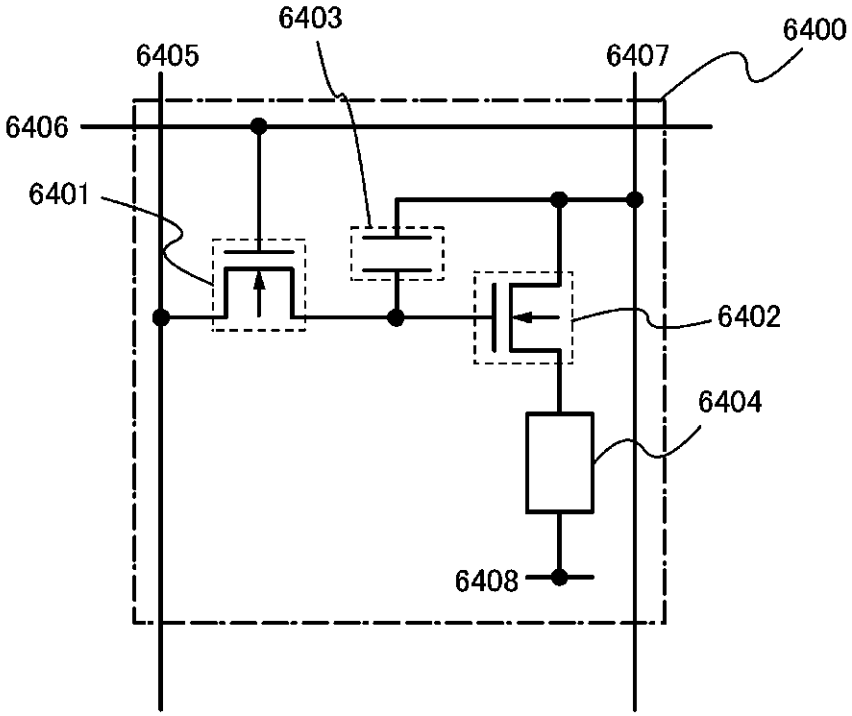


FIG. 19A

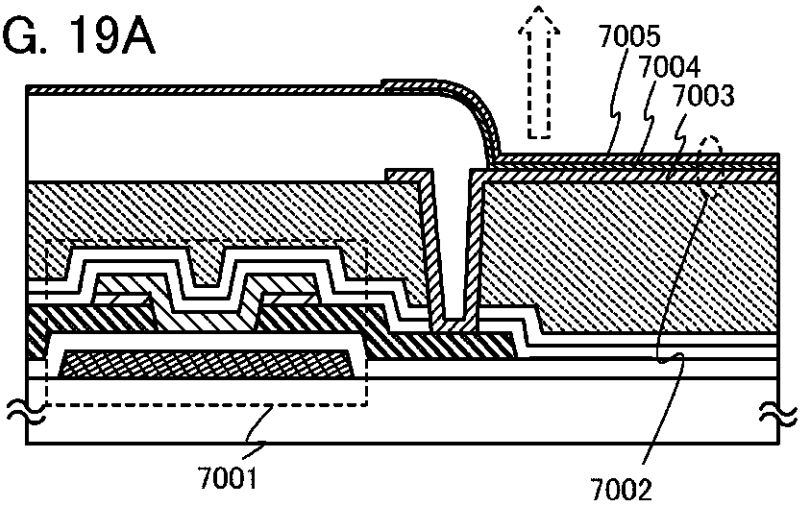


FIG. 19B

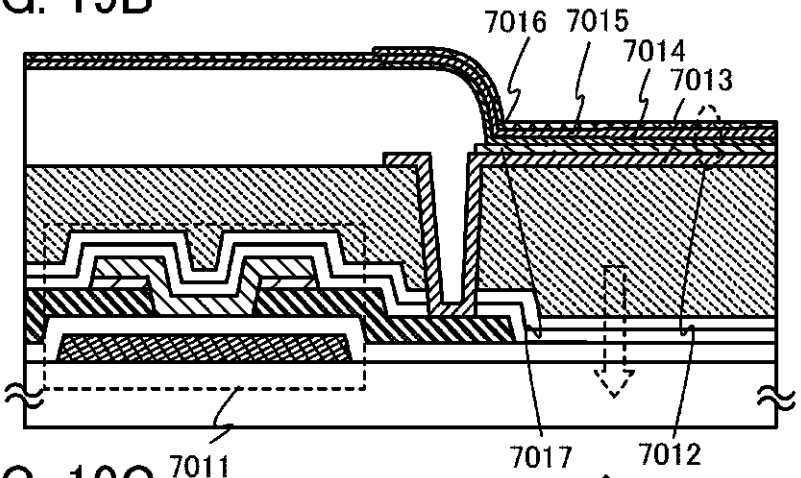


FIG. 19C

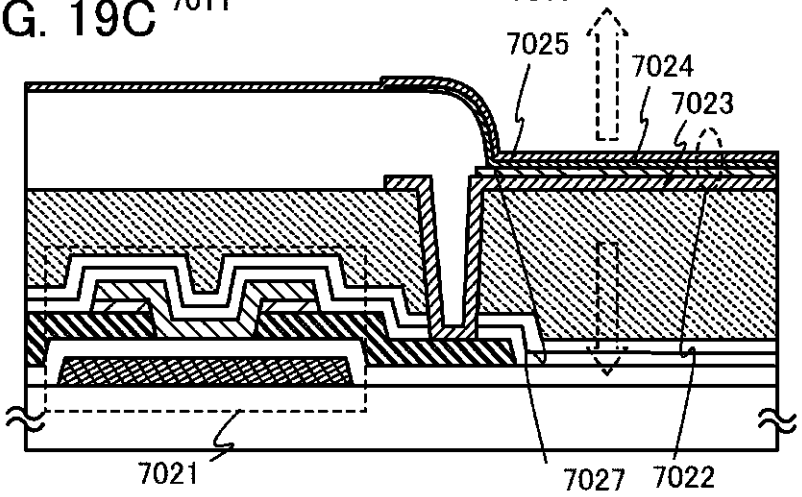


FIG. 20A1

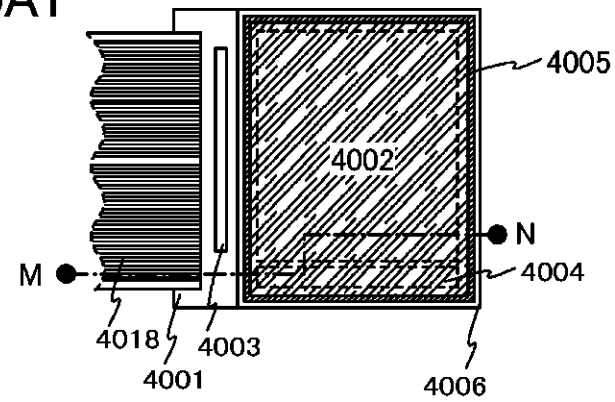


FIG. 20A2

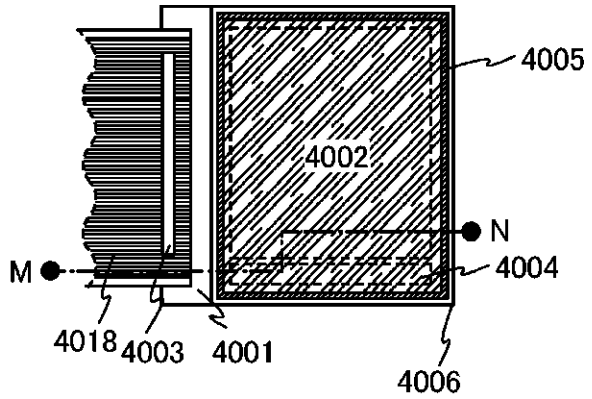


FIG. 20B

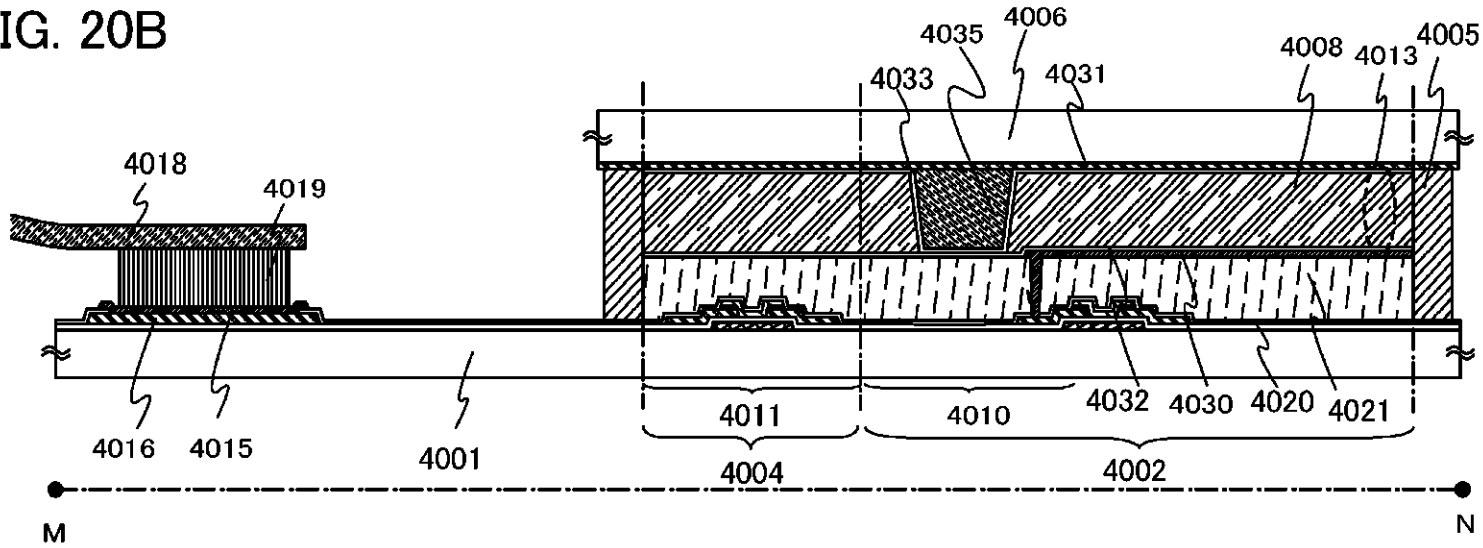


FIG. 21

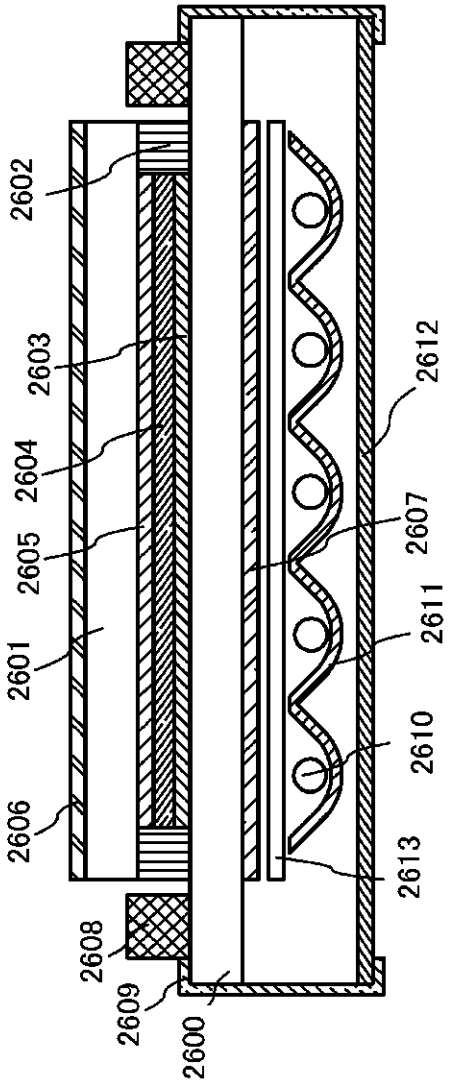

2602
2603
2604
2605
2601
2606
2608
2609
2600
2612
2607
2611
2610
2613

FIG. 22A

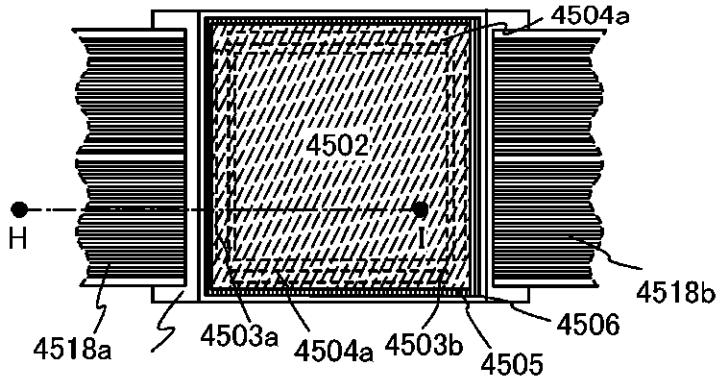


FIG. 22B

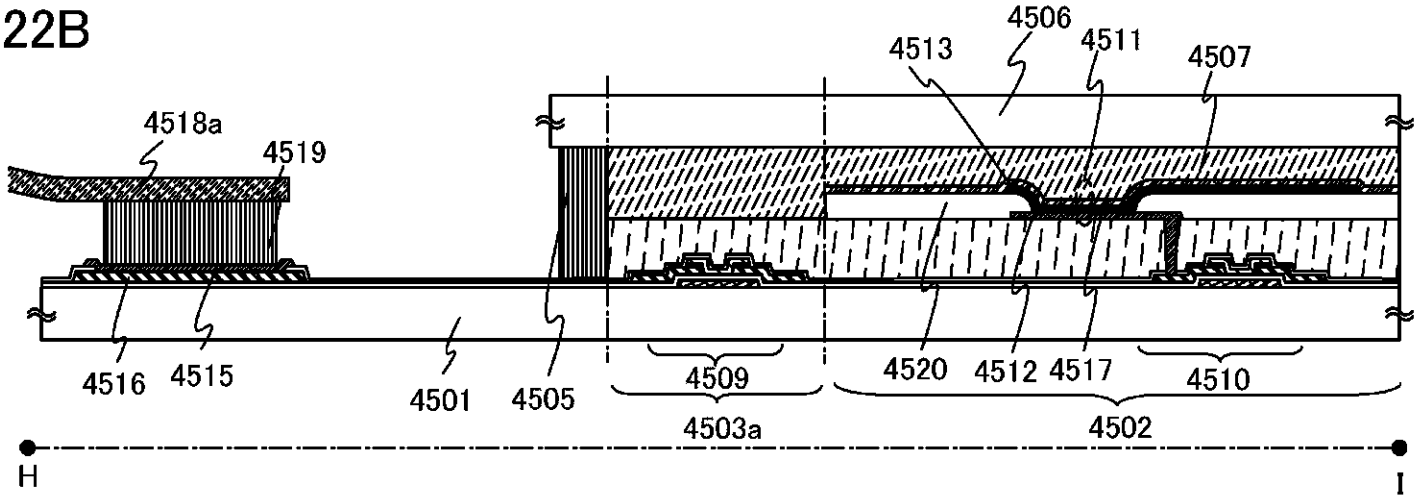


FIG. 23A

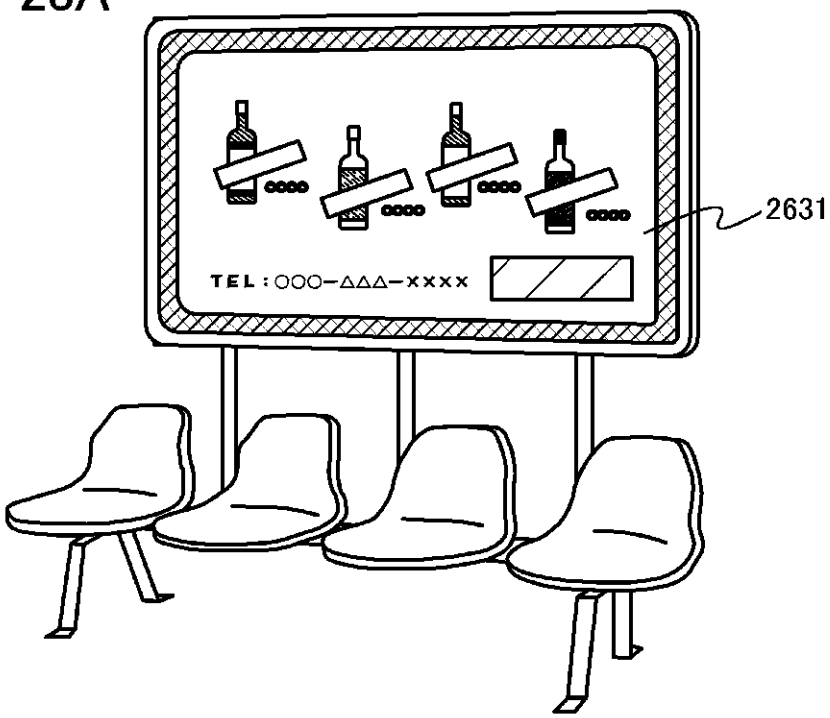


FIG. 23B

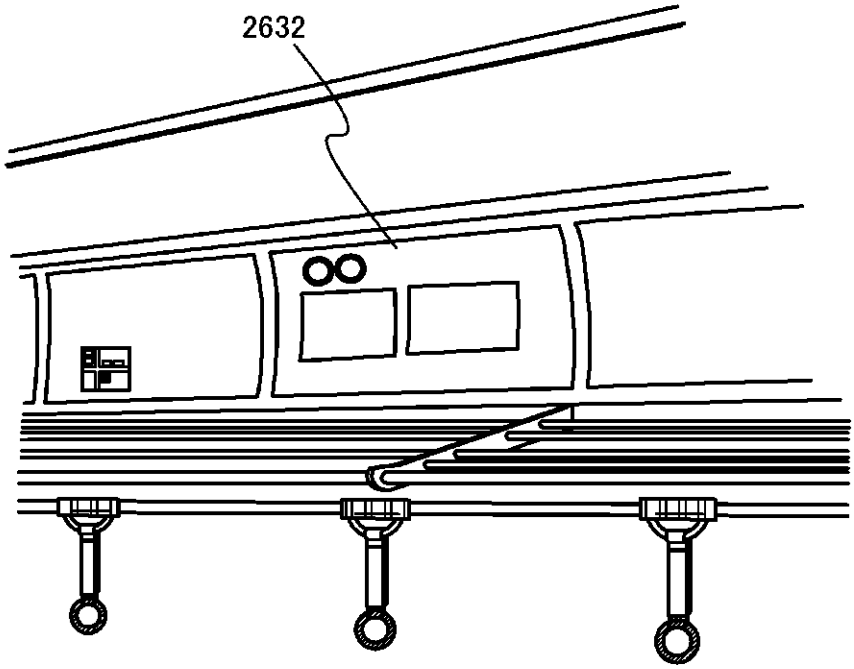


FIG. 24

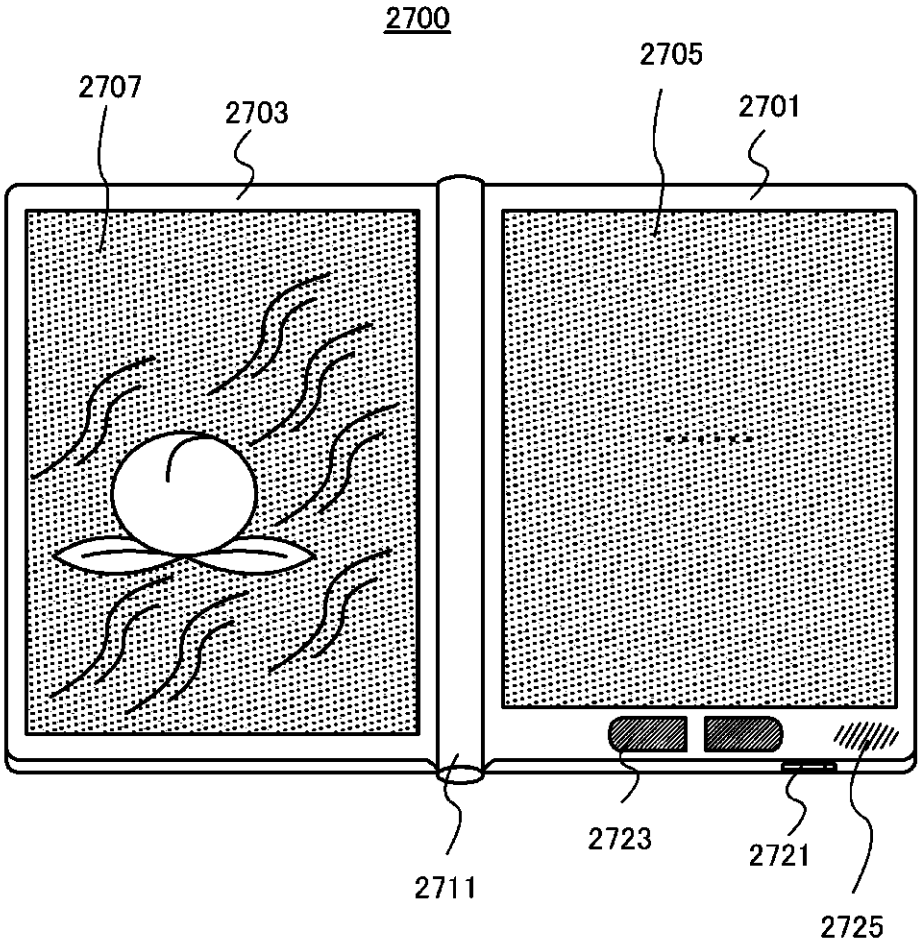


FIG. 25A

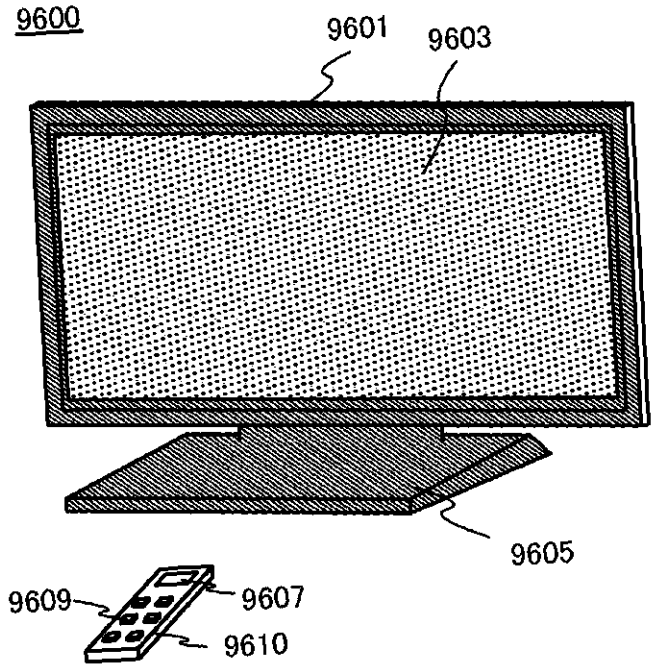


FIG. 25B

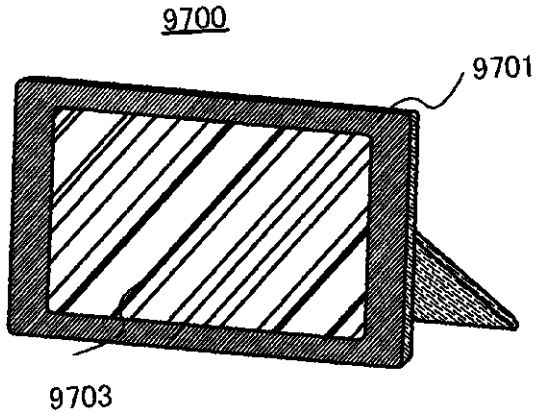


FIG. 26A

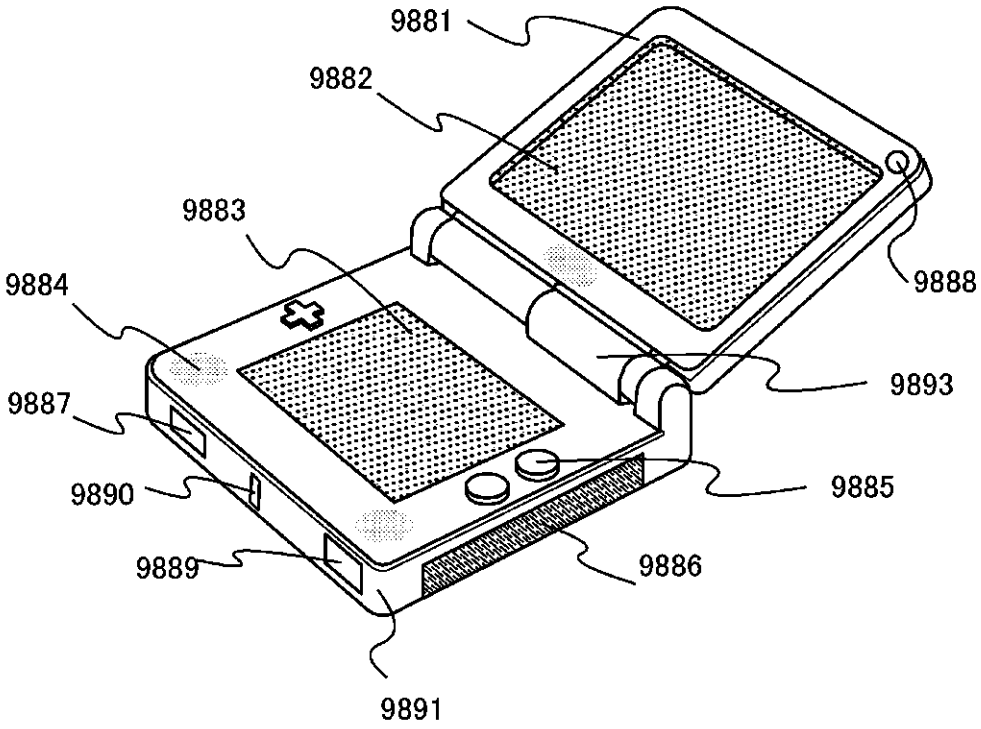


FIG. 26B

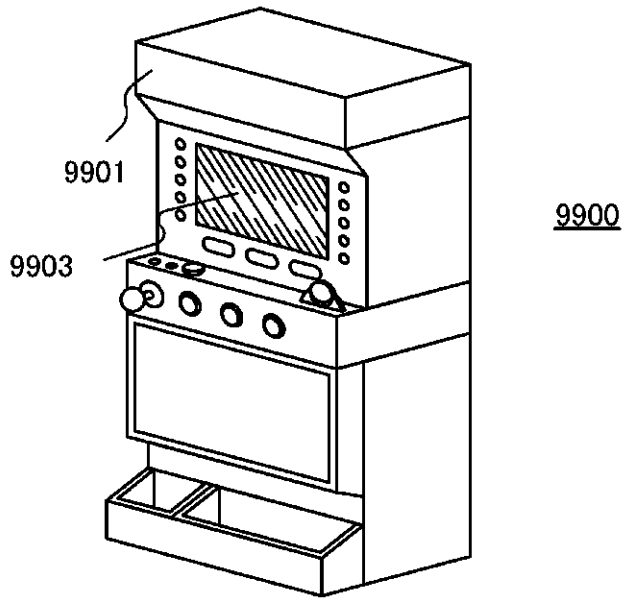


FIG. 27

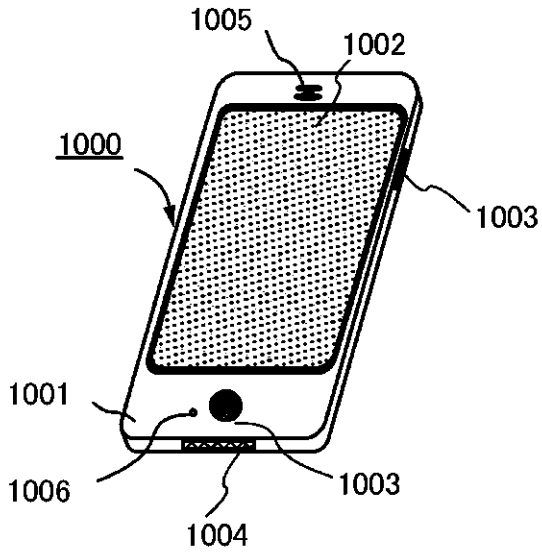


FIG. 28

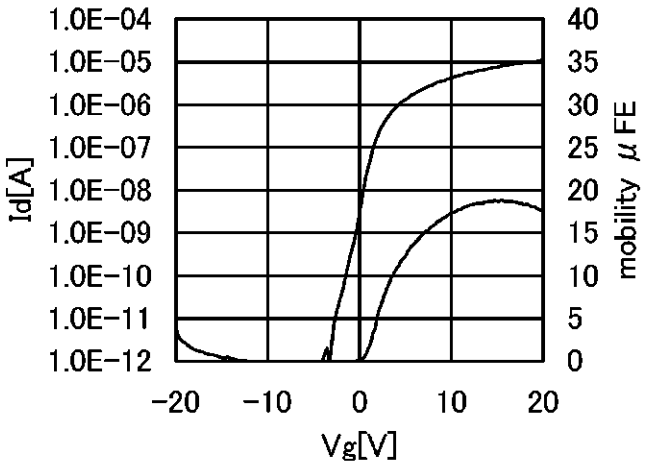

1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
1.0E-12
Id[A]
40
35
30
25
20
15
10
5
0
mobility μFE
-20
-10
0
10
20
Vg[V]

FIG. 29

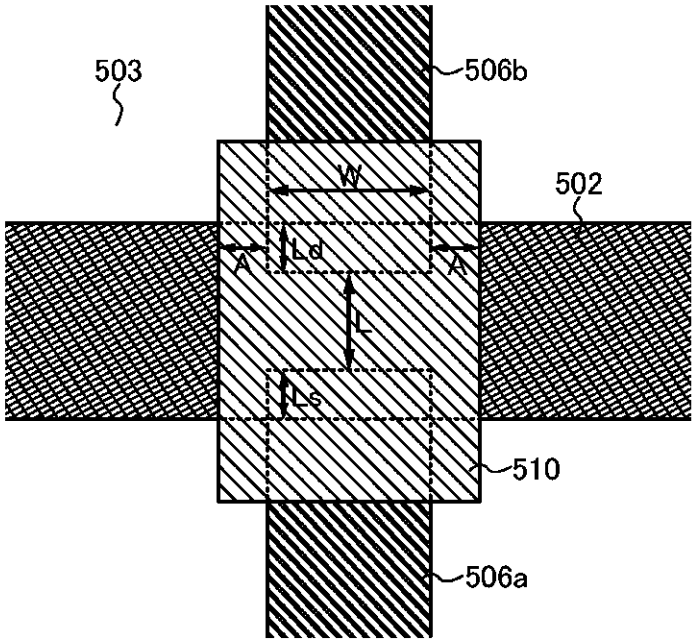


FIG. 30A

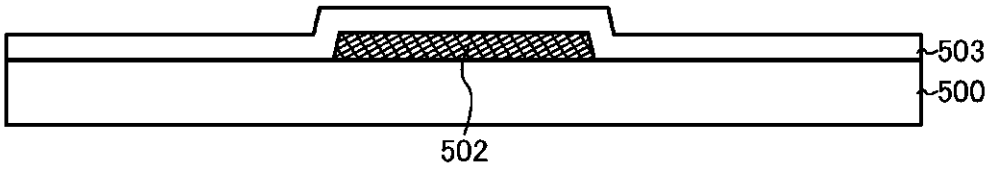


FIG. 30B

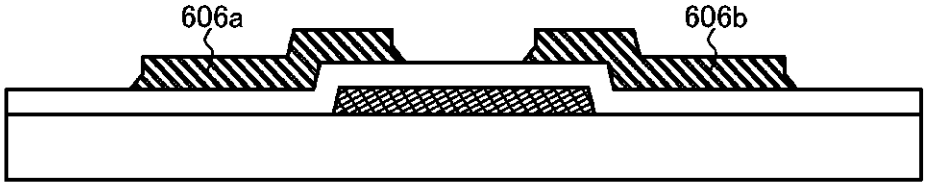


FIG. 30C

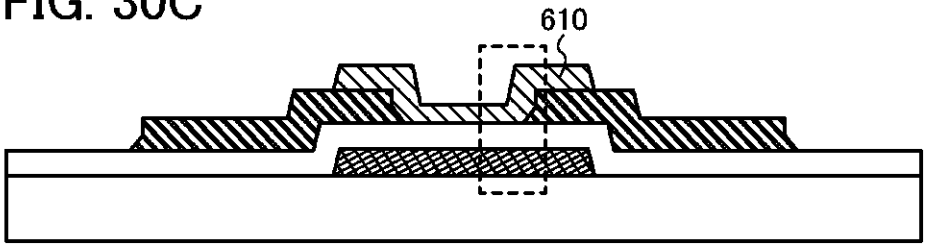


FIG. 31A

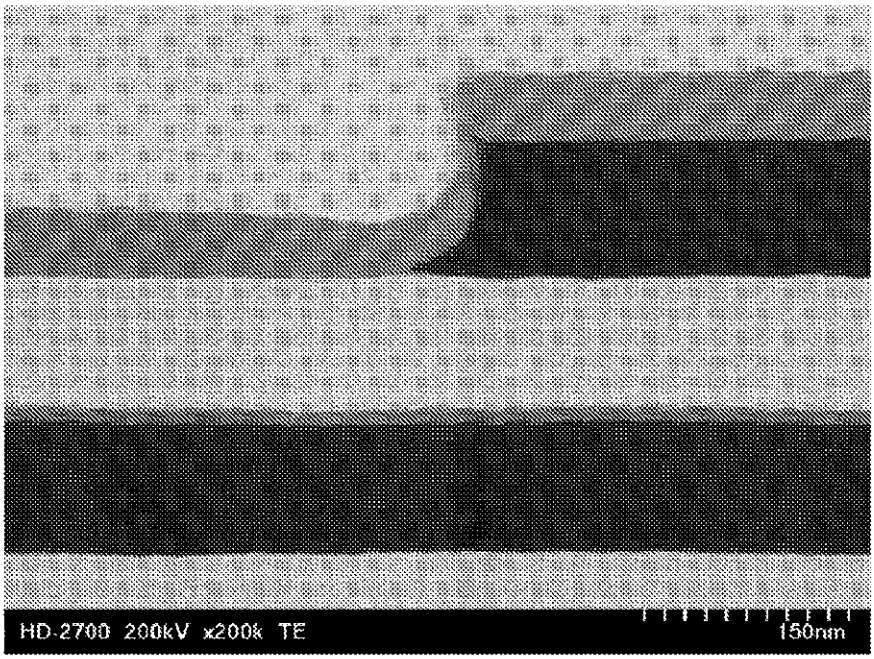


FIG. 31B

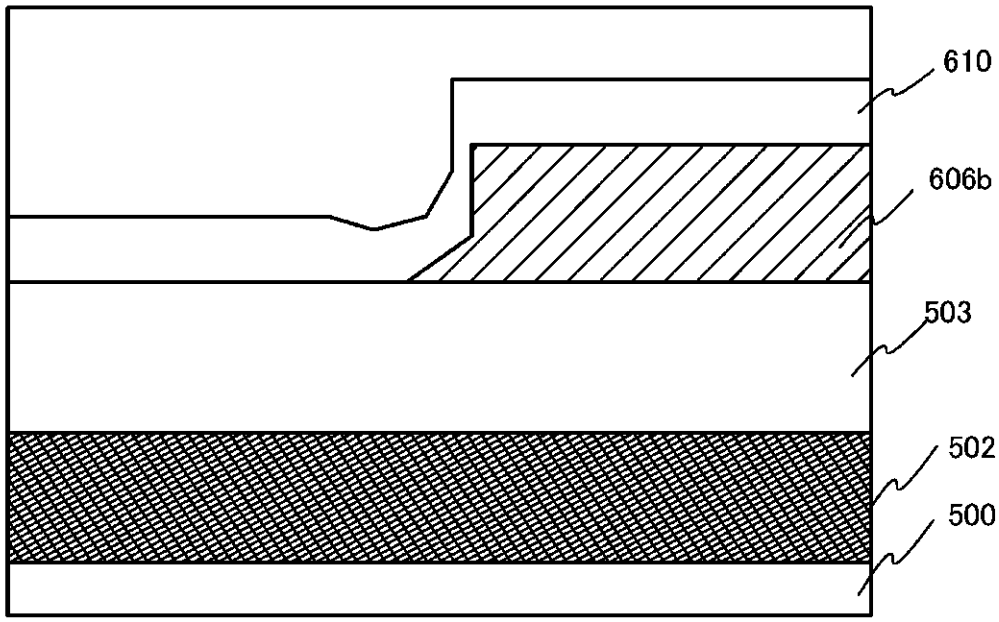


FIG. 32A

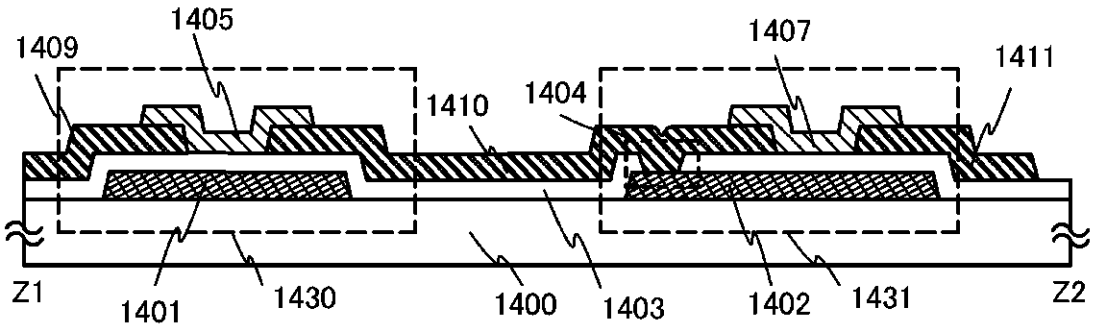


FIG. 32B

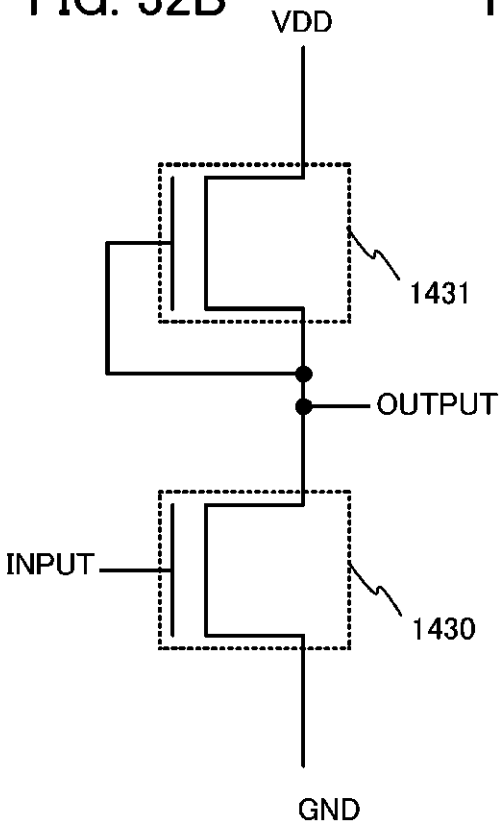


FIG. 32C

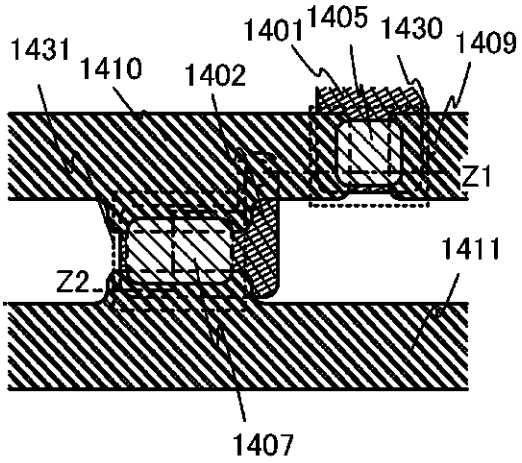


FIG. 33A

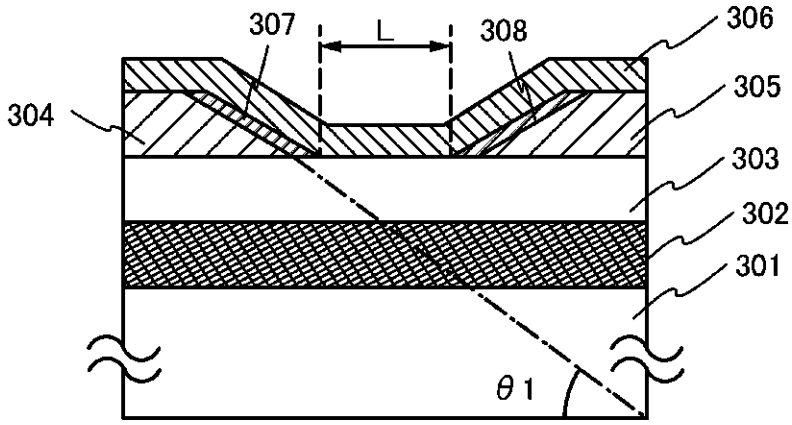


FIG. 33B

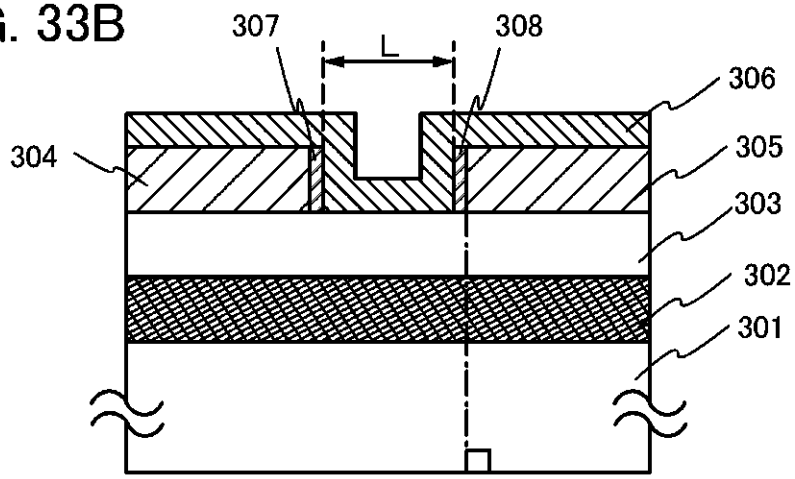


FIG. 33C

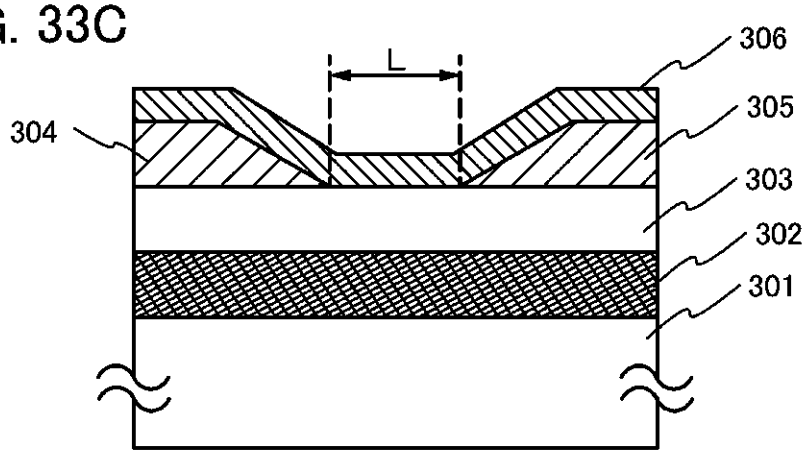


FIG. 34

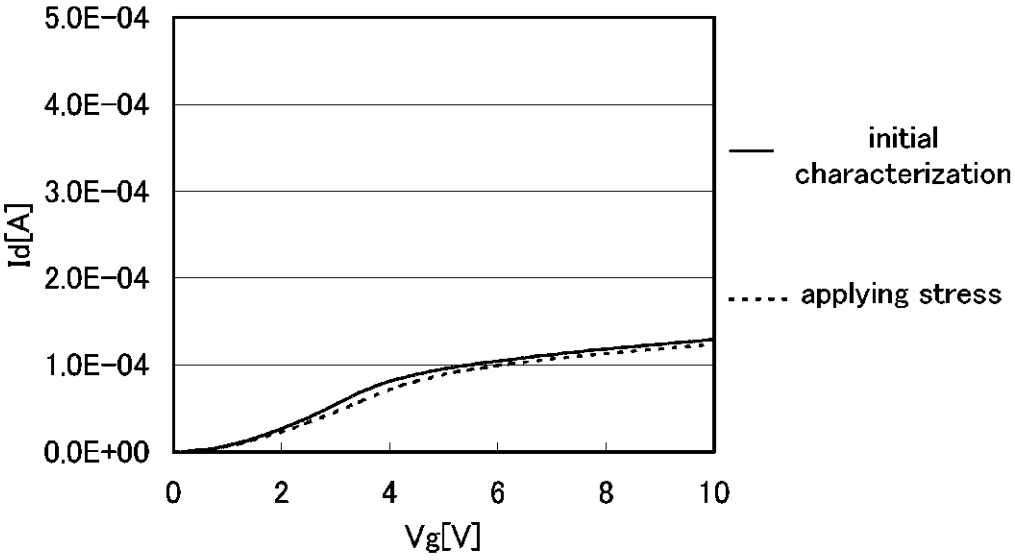

5.0E-04
4.0E-04
3.0E-04
2.0E-04
1.0E-04
0.0E+00
Id[A]
0
2
4
6
8
10
Vg[V]
initial characterization
applying stress

FIG. 35

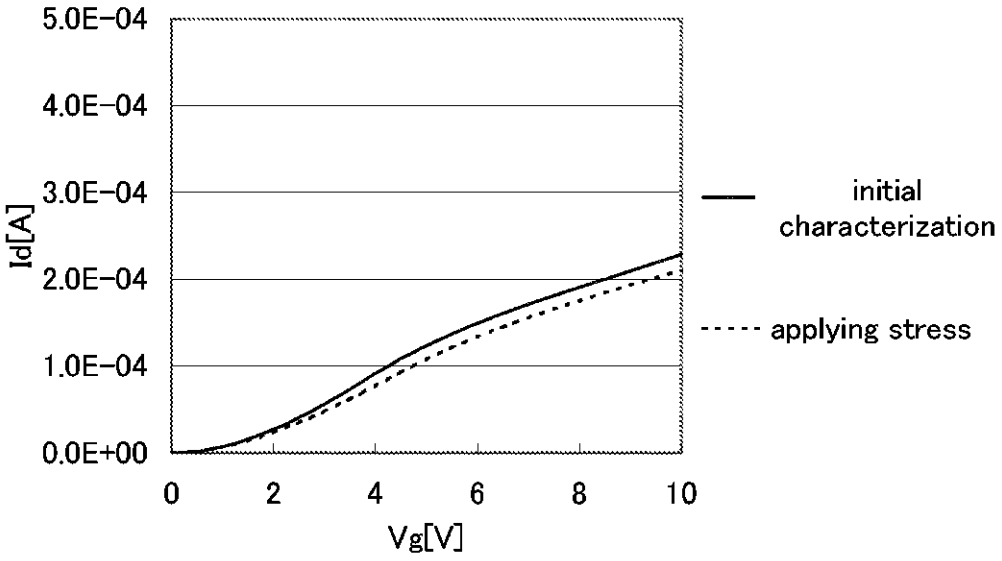

5.0E-04
4.0E-04
3.0E-04
2.0E-04
1.0E-04
0.0E+00
Id[A]
0
2
4
6
8
10
Vg[V]
initial characterization
applying stress

FIG. 36

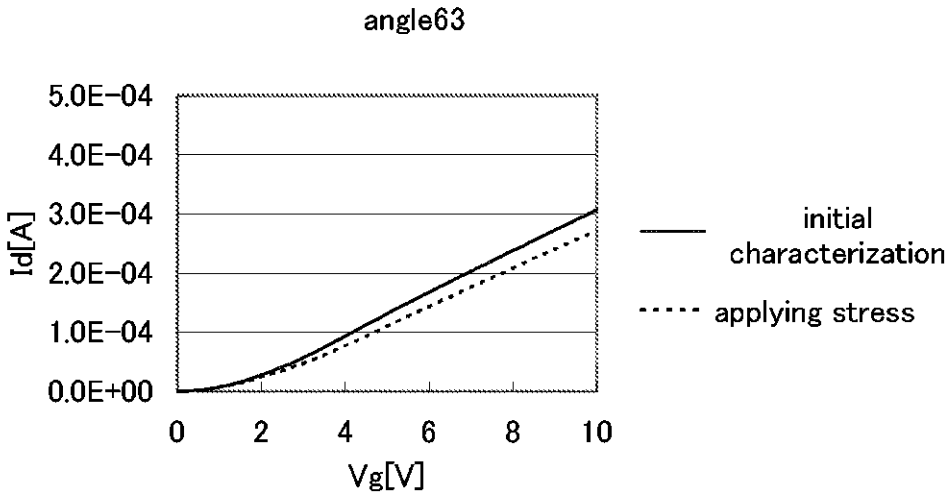

angle63
5.0E-04
4.0E-04
3.0E-04
2.0E-04
1.0E-04
0.0E+00
Id[A]
0
2
4
6
8
10
Vg[V]
initial characterization
applying stress

FIG. 37A

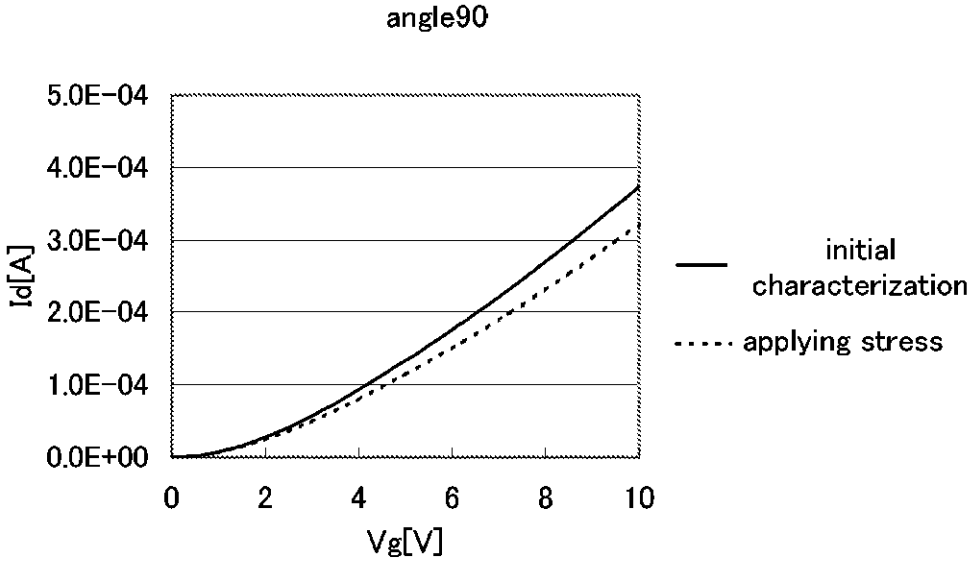
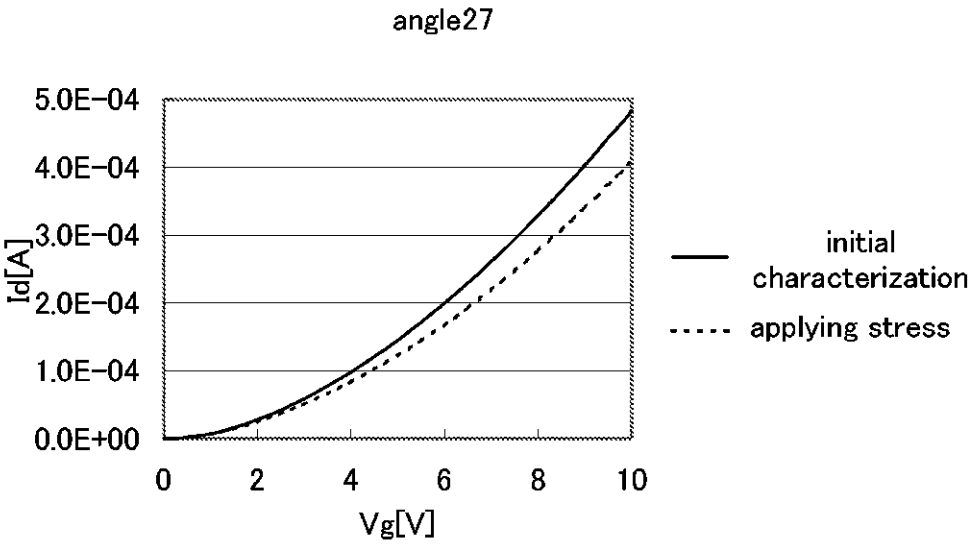


FIG. 37B



Electronic Acknowledgement Receipt	
EFS ID:	14924381
Application Number:	13763874
International Application Number:	
Confirmation Number:	7085
Title of Invention:	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Shunpei Yamazaki
Customer Number:	31780
Filer:	Eric J. Robinson/Sue Carr
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10065
Receipt Date:	11-FEB-2013
Filing Date:	
Time Stamp:	13:10:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	TRNA.pdf	440004 64a0eba80494e6f545140692bef003e2dbb4351e	no	2
Warnings:					
Information:					

2	Assignee showing of ownership per 37 CFR 3.73.	373c_STATEMENT.pdf	563530 d7dd627b9583a933e4468be3d761978104 71cd11	no	3
Warnings:					
Information:					
3	Power of Attorney	POA.pdf	196278 45ffba535bb2bc9ba5112ae39715d358079 619cb	no	2
Warnings:					
Information:					
4	Application Data Sheet	ADSPTOAIA14.pdf	1882524 7808faf4982a2e13a9168b1c8604809bd6c9 9e8b	no	6
Warnings:					
Information:					
5		IDS.pdf	339497 daa139debfd95c722ea1cbdc357c6c0b530 993f5	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	2
	Information Disclosure Statement (IDS) Form (SB08)	3	16

Warnings:					
Information:					
6		SPEC.pdf	1256776 74d373775b17fb93c9aab83b070c244ade7 da40c	yes	115

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	76
	Claims	77	77
	Abstract	78	78
	Drawings-only black and white line drawings	79	115

Warnings:	
Information:	
Total Files Size (in bytes):	4678609

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SCORE Placeholder Sheet for IFW Content

Application Number: 13763874 Document Date: 02/11/2013

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

To access the documents in the SCORE database, refer to instructions developed by SIRA.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (http://es/ScoreAccessWeb/).
- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: February 8, 2006

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/763,874

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	390
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 62 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1260

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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United States Patent and Trademark Office
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/763,874	02/11/2013	2812	0.00	0756-10065	1	1

CONFIRMATION NO. 7085

31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

FILING RECEIPT

OC000000059658089

Date Mailed: 03/08/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Shunpei YAMAZAKI, Setagaya, JAPAN;
Kengo AKIMOTO, Atsugi, JAPAN;
Daisuke KAWAE, Yamato, JAPAN;

Applicant(s)

Semiconductor Energy Laboratory Co., Ltd., Atsugi-shi, JAPAN

Assignment For Published Patent Application

SEMICONDUCTOR ENERGY LABORATORY CO., LTD., Atsugi-shi, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 31780

Domestic Priority data as claimed by applicant

This application is a CON of 12/613,769 11/06/2009 PAT 8373164 *
which is a CON of 12/606,262 10/27/2009 ABN
(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
JAPAN 2008-287187 11/07/2008

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 03/04/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/763,874**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

Preliminary Class

438

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/763,874	02/11/2013	Shunpei YAMAZAKI	0756-10065

CONFIRMATION NO. 7085

31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

FORMALITIES LETTER

OC000000059658090

Date Mailed: 03/08/2013

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  *Applicant must submit $**390** to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- A surcharge (for late submission of the basic filing fee, search fee, examination fee or inventor's oath or declaration) as set forth in 37 CFR 1.16(f) of $ **130** for a non-small entity, must be submitted.

SUMMARY OF FEES DUE:

Total fee(s) required within **TWO MONTHS** from the date of this Notice is $ **1390** for a non-small entity
- $ **390** Statutory basic filing fee.
- $ **130** Surcharge.
- The application search fee has not been paid. Applicant must submit $ **620** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit $ **250** to complete the examination fee for a non-small entity.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):

All

Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/tnegash/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/763,874	02/11/2013	Shunpei YAMAZAKI	0756-10065

CONFIRMATION NO. 7085

POA ACCEPTANCE LETTER

31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

OC000000059658209

Date Mailed: 03/08/2013

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/11/2013.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/tpnguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/08A (07-06)
Approved for use through 03/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	13/763,874
Filing Date	February 11, 2013
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2812
Examiner Name	Unknown
Attorney Docket Number	0756-10065

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-2009/0186445	07-23-2009	AKIMOTO.K	
		US-2009/0189156	07-30-2009	AKIMOTO.K	
		US-2009/0189155	07-30-2009	AKIMOTO.K	
		US-2010/0003783	01-07-2010	AKIMOTO.K	
		US-8134156	03-13-2012	AKIMOTO.K	
		US-8158464	04-17-2012	AKIMOTO.K	
		US-8368079	02-05-2013	AKIMOTO.K	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] -Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		WO-2007/058329	05-24-2007			Eng.
		CN-101283444	10-08-2008			Abst.

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/SB/08A (07-06)
Approved for use through 03/31/2007. OMB 0651-0031
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	13/763,874
Filing Date	February 11, 2013
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2812
Examiner Name	Unknown
Attorney Docket Number	0756-10065

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		CHINESE OFFICE ACTION (APPLICATION NO.200910206768.3) DATED March 15, 2013.	Full

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt	
EFS ID:	15591316
Application Number:	13763874
International Application Number:	
Confirmation Number:	7085
Title of Invention:	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Doris Vasquez Soriano
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10065
Receipt Date:	23-APR-2013
Filing Date:	11-FEB-2013
Time Stamp:	15:57:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	WO2007058329.pdf	8891176 9c032aa5b544c300082f7cc7cf5cde30a8d166d1	no	67

Warnings:
Information:

2	Foreign Reference	CN101283444.pdf	8925957 6fb5a45cbeb41b3693546f8df2c8d5d5edec a4f8	no	53
Warnings:					
Information:					
3	Non Patent Literature	CHINESEOFFICEACTION.pdf	3199719 0e2f99c1f085f625dd2f6ff73899fd46eb8d5 ba5	no	20
Warnings:					
Information:					
4		IDS23APR2013.pdf	428025 29d024d52d35fb2a0c85e1ea6a2f81d3f32f 1f86	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Information Disclosure Statement (IDS) Form (SB08)	2	3

Warnings:	
Information:	
Total Files Size (in bytes):	21444877

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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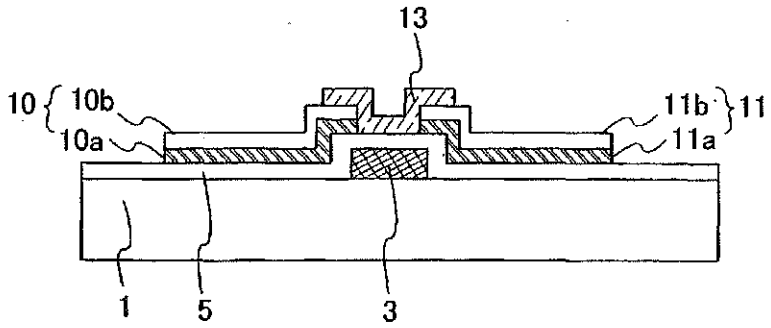

(57) Abstract: To provide a semiconductor device in which a defect or fault is not generated and a manufacturing method thereof even if a ZnO semiconductor film is used and a ZnO film to which an n-type or p-type impurity is added is used for a source electrode and a drain electrode. The semiconductor device includes a gate insulating film formed by using a silicon oxide film or a silicon oxynitride film over a gate electrode, an Al film or an Al alloy film over the gate insulating film, a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film, and a ZnO semiconductor film over the ZnO film to which an n-type or p-type impurity is added and the gate insulating film.

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DESCRIPTION

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device using ZnO (Zinc Oxide) and a manufacturing method thereof.

BACKGROUND ART

[0002]

A semiconductor device used for a display panel of a liquid crystal display device or an EL (Electroluminescent) display device, for example, a semiconductor portion of a TFT (Thin Film Transistor), is generally formed by using a-Si (amorphous silicon) or poly-Si (polycrystalline silicon).

[0003]

Si (silicon) does not have a large band gap (for example, single-crystalline Si is 1.1 eV), and absorbs visible light. By irradiation with the light, electrons and holes (carriers) are formed in Si. If a Si film is used for a channel formation region of a TFT, a carrier is generated in the channel formation region by irradiation with the light even in an OFF state. Then, current flows between a source region and a drain region. The current which flows in an OFF state is called "OFF-leak current". If the current value is high, a display panel does not operate normally. Consequently, a light shielding film is formed so as not to irradiate the Si film with light. However, a process becomes complex when the light shielding film is formed, because a deposition step, a photolithography step, and an etching step are required.

[0004]

To solve the problem, an attention is paid to a transparent transistor using zinc oxide (ZnO) which is a semiconductor having a larger band gap of 3.4 eV than that of Si. Concerning such a transparent transistor, the band gap is larger than light energy in a visible light band and the visible light is not absorbed. Consequently, it has an advantage that the OFF-leak current

does not increase if irradiated with light.

[0005]

A semiconductor device using ZnO for the channel formation region is disclosed in Reference 1, for example. The structure of the semiconductor device using ZnO is described referring to FIG. 7A.

[0006]

A semiconductor device in FIG. 7A has a source electrode 1001 and a drain electrode 1002, a ZnO layer 1003 arranged so as to be contacted with the source electrode 1001 and the drain electrode 1002, and a gate insulating layer 1004 stacked over the ZnO layer 1003 and a gate electrode 1005 over an insulating substrate 1000 such as a glass substrate.

[0007]

For the source electrode 1001 and the drain electrode 1002, a conductive ZnO is used. The conductive ZnO is doped with one of the following: B(boron), Al (aluminum), Ga (gallium), In (indium), or Tl (thallium), which are III group elements; F(fluorine), Cl (chlorine), Br (bromine), or I (iodine), which are VII group elements; Li (lithium), Na (sodium), K (potassium), Rb (rubidium), or Cs (caesium), which are I group elements; and N (nitrogen), P (phosphorus), As (arsenic), Sb (antimony), or Bi (bismuth), which are V group elements.

[Reference 1] Japanese Published Patent Application No. 2000-150900

DISCLOSURE OF INVENTION

[0008]

According to the examination by the present inventor, it was revealed that the substrate 1000 is etched in some cases when the source electrode 1001 and the drain electrode 1002 of the top gate semiconductor device shown in FIG. 7A is formed by etching. Even in the case of forming a base film 1006 formed by using a silicon oxide film or a silicon oxynitride film on the substrate 1000, the surface of the substrate 1000 is exposed in some cases when the base film is etched. In addition, in the case of a bottom gate semiconductor device shown in FIG. 7B, it is revealed that a gate insulating film 1004 formed by using a silicon oxide film or a silicon oxynitride film is etched when a source electrode 1001 and a drain electrode 1002 are formed by etching.

[0009]

It the case of the top gate semiconductor device, when the glass substrate 1000 or the base film 1006 formed by using a silicon oxide film or a silicon oxynitride film is etched, an impurity such as sodium is diffused into a semiconductor film 1003 from the substrate 1000, so that characteristics are deteriorated.

[0010]

In the case of the bottom gate semiconductor device (FIG. 7B), if the gate insulating film 1004 is etched when the source electrode 1001 and the drain electrode 1002 are formed by etching, the characteristics are not stable and causes a fault.

[0011]

In consideration of the above situation, it is an object of the present invention to provide a semiconductor device in which a defect or a fault is not generated and a manufacturing method thereof even if a ZnO semiconductor film is used for the channel formation region, and a ZnO film to which an n-type or p-type impurity is added is used for the source electrode and the drain electrode.

[0012]

An aspect of a semiconductor device of this invention has an Al film or an Al alloy film over a silicon oxide film or a silicon oxynitride film, and a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film. "A silicon oxide film", "a silicon oxynitride film", "an Al film", "an Al alloy film" and "a ZnO film" in this specification means a film containing silicon oxide, a film containing silion oxynitride, a film containing Al, a film containing Al alloy, a film containing ZnO, respectively.

[0013]

An aspect of a semiconductor device of this invention has a gate insulating film formed by using a silicon oxide film or a silicon oxynitride film over a gate electrode, an Al film or an Al alloy film over the gate insulating film, a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film, and a ZnO semiconductor film over the ZnO film to which an n-type or p-type impurity is added and the gate insulating film.

[0014]

An aspect of a semiconductor device of this invention has an Al film or an Al alloy film over a silicon oxide film or a silicon oxynitride film, a ZnO film to which an n-type or p-type

impurity is added over the Al film or the Al alloy film, a ZnO semiconductor film over the silicon oxide film or the silicon oxynitride film and the ZnO film to which an n-type or p-type impurity is added, a gate insulating film over the ZnO semiconductor film, and a gate electrode over the gate insulating film.

[0015]

An aspect of a manufacturing method of a semiconductor device of this invention has the steps of: forming a silicon oxide film or a silicon oxynitride film; forming an Al film or an Al alloy film over the silicon oxide film or the silicon oxynitride film; forming a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film, wherein the ZnO film to which an n-type or p-type impurity is added is etched to have an island-like shape by a first etching, and the Al film or the Al alloy film is etched to have an island-like shape by a second etching.

[0016]

An aspect of a manufacturing method of a semiconductor device of this invention, wherein a ZnO semiconductor film is formed over the ZnO film to which an n-type or p-type impurity is added, and the silicon oxide film or the silicon oxynitride film after the second etching.

[0017]

In the case of the bottom gate semiconductor device, a gate insulating film formed by using the silicon oxide film or the silicon oxynitride film is formed over the gate electrode after forming a gate electrode.

[0018]

In the case of the top gate semiconductor device, a gate insulating film is formed and a gate electrode is formed after the ZnO semiconductor film is formed.

[0019]

A first etching of this invention may be wet etching.

[0020]

A first etching of this invention may be wet etching using buffered fluoric acid.

[0021]

A first etching of this invention may be dry etching.

[0022]

A first etching of this invention may be dry etching using CH_4 (methane) gas.

[0023]

A second etching of this invention may be wet etching.

[0024]

A second etching of this invention may be wet etching using developing solution for a photoresist.

[0025]

A second etching of this invention may be wet etching using an organic alkaline solution.

[0026]

A second etching of this invention may be wet etching using TMAH (tetramethylammonium hydroxide).

[0027]

An aspect of a semiconductor device of this invention has a gate electrode, a gate insulating film over the gate electrode, a first film comprising metal material over the gate insulating film, a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the first film, and a third film comprising the transparent semiconductor material over the second film and the gate insulating film.

[0028]

An aspect of a semiconductor device of this invention has an insulating film over a substrate, a first film comprising a metal material over the insulating film, a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the metal film, a third film comprising the transparent semiconductor material over the insulating film and the second film, a gate insulating film over the third film, and a gate electrode over the gate insulating film.

[0029]

An aspect of a manufacturing method of a semiconductor device of this invention has the steps of: forming an insulating film over a substrate, forming a first film comprising a metal material over the insulating film, forming a second film comprising a transparent semiconductor

material and an n-type or p-type impurity over the first film, etching the second film, and etching the first film.

[0030]

An aspect of a manufacturing method of a semiconductor device of this invention has the steps of: forming a gate electrode over a substrate, forming a gate insulating film over the gate electrode, forming a first film comprising a metal material over the gate insulating film, forming a second film comprising a transparent semiconductor material and an n-type or p-type impurity over second film, etching the second film, and etching the first film.

[0031]

In the top gate semiconductor device, a base film formed by using a glass substrate, a silicon oxide film or a silicon oxynitride film is not etched, and an impurity such as sodium is not diffused from a substrate into a semiconductor film so that its characteristics are not deteriorated.

[0032]

In the bottom gate semiconductor device, the gate insulating film is not etched and its characteristics do not become unstable.

[0033]

Since Al is used for a part of the source electrode and drain electrode, low resistance of a wire can be obtained.

BRIEF DESCRIPTION OF DRAWINGS

[0034]

In the accompanying drawings:

FIGS. 1A and 1B show semiconductor devices of this invention;

FIGS. 2A to 2D show manufacturing steps of a semiconductor device of this invention;

FIGS. 3A to 3D show manufacturing steps of a semiconductor device of this invention;

FIGS. 4A and 4B show manufacturing steps of a semiconductor device of this invention;

FIGS. 5A to 5D show manufacturing steps of a semiconductor device of this invention;

FIGS. 6A to 6C show manufacturing steps of a semiconductor device of this invention;

FIGS. 7A and 7B show conventional examples;

FIGS. 8A and 8B show a manufacturing step of a liquid crystal display device;

FIGS. 9A and 9B show manufacturing steps of a liquid crystal display device;

FIGS. 10A and 10B show manufacturing steps of a light-emitting device;

FIGS. 11A and 11B show manufacturing steps of a light-emitting device;

FIGS. 12A to 12F each show an equivalent circuit of a light-emitting device;

FIG. 13 shows an equivalent circuit of a light-emitting device;

FIG. 14A illustrates a top front view of a pixel portion and FIG. 14B illustrates an equivalent circuit of a light-emitting device;

FIGS. 15A to 15E each show an example of an electronic apparatus to which this invention is applied; and

FIG. 16 shows an example of electronic apparatuses to which this invention is applied.

[0035]

The embodiments of this invention will be described hereinafter referring to the accompanying drawings. Note that this invention is not limited to the description below, and it is easily understood by those skilled in the art that the embodiments and details herein disclosed can be modified in various ways without departing from the purpose and the scope of the invention. Therefore, this invention should not be interpreted as being limited to the description of the embodiments to be given below.

BEST MODE FOR CARRYING OUT THE INVENTION

[0036]

[Embodiment 1]

Here, a bottom gate semiconductor device is described.

[0037]

FIG. 1A is a cross-sectional view in which one example of the embodiment of this invention is shown. In FIG. 1A, numeral reference 1 denotes a substrate, 3 denotes a gate electrode, 5 denotes a gate insulating film, 10 denotes a source electrode, 10a denotes a first conductive film, 10b denotes a second conductive film, 11 denotes a drain electrode, 11a denotes a first conductive film, 11b denotes a second conductive film, and 13 denotes a semiconductor

film. An insulating film for passivation or planarization may be formed over the semiconductor film 13.

[0038]

The gate electrode 3 is formed over the substrate 1, the gate insulating film 5 is formed over the gate electrode 3, and the source electrode 10 and the drain electrode 11 are formed over the gate insulating film 5. The source electrode 10 is formed of a layered film having the first conductive film 10a and the second conductive film 10b, and the drain electrode 11 is formed of a layered film having the first conductive film 11a and the second conductive film 11b. A third conductive film may be formed between the first conductive film 10a and the second conductive film 10b, or between the first conductive film 11a and the second conductive film 11b. The source electrode 10 and the drain electrode 11 may be each formed so as to overlap partially with the gate electrode 3 through the gate insulating film 5. The semiconductor film 13 is formed over the source electrode 10 and the drain electrode 11 over the gate insulating film 5.

[0039]

Hereinafter, each structure is described.

(1) substrate

The following can be used for forming a substrate: a substrate formed by using a glass substrate; an insulating material such as alumina; and a plastic substrate which can resist a processing temperature in post-steps; and the like. In the case of using a plastic substrate for the substrate 1, the following can be used: PC (polycarbonate); PES (polyethersulfone); PET (polyethylene terephthalate); PEN (polyethylene naphthalate); or the like. In the case of the plastic substrate, an inorganic layer or an organic layer may be provided as a gas barrier layer over the surface. In the case where a prominence due to dust or the like which is generated on the substrate in the manufacturing process of the plastic substrate, the substrate may be used after polishing it with CMP or the like to make its surface planarized. An insulating film such as silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy) (X>Y), and silicon nitride oxide (SiNxOy) (X>Y) may be formed over the substrate 1 for preventing an impurity or the like from diffusing from the substrate side.

[0040]

(2) gate electrode

A gate electrode can be formed by using an Al (aluminum) film, a W (tungsten) film, a Mo (molybdenum) film, a Ta (tantalum) film, a Cu (copper) film, a Ti (titanium) film, an alloy material containing the elements as a main component (for example, an Al alloy film, a MoW (molybdenum tungsten) alloy film), or the like. A semiconductor film represented by a polycrystalline silicon film doped with an impurity element such as P (phosphourus) may be used. The gate electrode 3 may be a single layer or a layered film in which two or more layers are stacked.

[0041]

(3) gate insulating film

The gate insulating film 5 is formed by using an insulating film containing silicon as a main component, for example, silicon oxide film, and silicon oxynitride film. In addition, it may be a single layer or a layered film.

[0042]

(4) source electrode and drain electrode

The source electrode 10 is formed with a layered film of the first conductive film 10a and the second conductive film 10b, and the drain electrode 11 is formed with a layered film of the first conductive film 11a and the second conductive film 11b.

[0043]

As the first conductive film, an Al film, an Al alloy film such as an AlNi (aluminum nickel) film, and an AlNd (neodymium aluminum) film can be used. As the second conductive film, ZnO (zinc oxide) to which a p-type or n-type impurity of B (boron), Al (aluminum), Ga (gallium), P (phosphorus), or As (arsenic) is added can be used. A metal film such as a Ti film may be provided as a third conductive film between the first conductive film and the second conductive film.

[0044]

(5) semiconductor film

A ZnO film is used as a semiconductor film. Since the source electrode and the drain electrode contacted with the semiconductor film have the ZnO film to which a p-type or n-type impurity is added, they can be easily connected with the semiconductor film.

[0045]

(6) insulating film

An insulating film such as a passivation film and a planarization film may be formed over the semiconductor film 13, although not shown. Silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy) (x>y), silicon nitride oxide (SiNxOy) (x>y), a SOG (spin-on-glass) film, or an organic resin film of acryl, or a layered film of those can be used.

[0046]

In the bottom gate semiconductor device, a gate insulating film is not etched in manufacturing process, and characteristics do not become unstable. Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

[0047]

[Embodiment 2]

Here, a top gate semiconductor device is described.

[0048]

FIG. 1B is a cross-sectional view showing one example of an embodiment of this invention. In FIG. 1B, numeral reference 1 denotes a substrate, 20 denotes an insulating film, 25 denotes a source electrode, 25a denotes a first conductive film, 25b denotes a second conductive film, 26 denotes a drain electrode, 26a denotes a first conductive film, 26b denotes a second conductive film, 27 denotes a semiconductor film, 28 denotes a gate insulating film, and 29 denotes a gate electrode. An insulating film for passivation or planarization may be formed over the gate electrode.

[0049]

The insulating film 20 is formed on the substrate 1, and the source electrode 25 and the drain electrode 26 are formed over the insulating film 20. The source electrode 25 is formed with a layered film of the first conductive film 25a and the second conductive film 25b, and the drain electrode 26 is formed with a layered film of the first conductive film 26a and the second conductive film 26b. A third conductive film may be formed between the first conductive film 25a and the second conductive film 25b, or between the first conductive film 26a and the second conductive film 26b. The semiconductor film 27 is formed over the source electrode 25 and the drain electrode 26 over the insulating film 20, the gate insulating film 28 is formed over the semiconductor film 27, and the gate electrode 29 is formed over the gate insulating film 28.

The gate electrode 29 may be formed so as to partially overlap with the source electrode and the drain electrode with the gate insulating film 28 and the semiconductor film 27 interposed therebetween.

[0050]

Here, each structure is described.

[0051]

For the substrate, the source electrode, the drain electrode, the semiconductor film, and the gate electrode, the same ones described in Embodiment 1 can be used.

(1) *insulating film over substrate*

An silicon oxide film or a silicon oxynitride film is formed as the insulating film 20 for preventing an impurity or the like from diffusing from the substrate side over the substrate 1. In addition, it may be a single layer or a layered film.

[0052]

(2) gate insulating film

The gate insulating film 28 is formed by using an insulating film containing silicon as a main component, for example, a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, and a silicon nitride film. In addition, it may be a single layer or a layered film.

[0053]

(3) *insulating film over gate electrode*

An interlayer insulating film such as a passivation film and a planarization film may be formed over the gate electrode 29, although not shown. A SiO_x film, a SiNx film, a SiON film, SiNO film, an SOG (spin-on-glass) film, and an organic resin film of acrylic or a layered film of those can be used.

[0054]

In the top gate semiconductor device, the substrate or the base film formed by using a silicon oxide film or a silicon oxynitride film is not etched, so that an impurity such as sodium is not diffused into the semiconductor film from the substrate and the characteristics are not deteriorated. Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

[0055]

[Embodiment 3]

A manufacturing method of the bottom gate semiconductor device is described, in which a silicon oxide film or a silicon oxynitride film is formed as a gate insulating film over the gate electrode, an Al film or an Al alloy film is formed as a first conductive film, and a ZnO film to which an n-type or p-type impurity is added is formed as a second conductive film, and then, the second conductive film is etched to have an island-like shape by a first etching and the first conductive film is etched to have an island-like shape by a second etching to form source and drain electrodes, and a ZnO semiconductor film is formed.

[0056]

As shown in FIG. 2A, a gate electrode 3 is formed. The thickness of the gate electrode may be 10 to 200 nm over a substrate 1. The substrate 1 may be formed by using the material shown in Embodiment 1. Here, a glass substrate is used.

[0057]

An insulating film 2 containing silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy) (x>y), silicon nitride oxide (SiNxOy) (x>y), or the like may be formed with a thickness of 10 to 200 nm by CVD or sputtering so as to prevent impurity or the like from diffusing from the substrate side (FIG. 2B).

[0058]

The insulating film 2 may be formed by processing the surface of the substrate 1 with high density plasma. For example, the high density plasma can be generated using a microwave of 2.45 GHz, and it is only required that electron density ranges from 1×10^{11} to $1\times10^{13}/cm^3$, and electron temperature is 2 eV or less. Such high density plasma has a low kinetic energy of active species and a film with fewer defects can be formed with less damage caused by plasma compared to a conventional plasma treatment.

[0059]

The surface of the substrate 1 can be nitrided by the high density plasma treatment under a nitriding atmosphere such as an atmosphere containing nitrogen and a noble gas, an atmosphere containing nitrogen, hydrogen and a noble gas, and an atmosphere containing ammonia and a noble gas. In the case where a glass substrate is used as the substrate 1 subjected to a nitriding treatment by the high density plasma, as a nitride film formed over the

surface of the substrate 1, the insulating film 2 containing silicon nitride as a main component can be formed. The insulating film 2 may be formed by using a plurality of layers in which a silicon oxide film or a silicon oxynitride film is formed by plasma CVD over the nitride film.

[0060]

In addition, a nitride film can be formed by nitriding over the surface of the insulating film 2 with high density plasma similarly.

[0061]

The nitride film formed by nitriding with high density plasma can suppress diffusion of impurity from the substrate 1.

[0062]

The gate electrode 3 can be formed by using materials shown in Embodiment 1. Here, an AlNd (aluminum neodymium) film is formed by sputtering using an AlNd target and processed into an island-like shape. A photolithography method is used for processing the film into an island-like shape, and dry etching or wet etching is used.

[0063]

After cleaning the surface of the gate electrode 3 and the surface of the substrate 1 or the insulating film 2, a gate insulating film 5 is formed with a thickness of 10 to 200 nm using a known CVD or sputtering over the gate electrode 3 (FIG. 2A and 2B). The surface cleaning step and the formation step of the gate insulating film 5 may be carried out continuously without being exposed to air. In the case where an Al film is used for the gate electrode 3, when the gate insulating film 5 is formed at a high temperature, a hillock is generated in some cases. Thus, it is preferable to form the film at a low temperature of 500°C or less, preferably 350 °C or less.

[0064]

The gate insulating film 5 can be formed by using the material shown in Embodiment 1. Here, a silicon oxide film is formed. Note that the insulating film 2 is omitted in the drawings below.

[0065]

A first conductive film 6 for source and drain electrodes is formed with a thickness of 10 to 200 nm on the gate insulating film 5. The first conductive film 6 can be formed by using

the material shown in Embodiment 1. Here, an AlNi (aluminum nickel) film or an AlNd film is used. The first conductive film 6 can be formed by sputtering using an AlNi target or an AlNd target. After forming the gate insulating film 5, the first conductive film 6 may be formed continuously without being exposed to the air.

[0066]

A second conductive film 7 is formed with a thickness of 10 to 200 nm on the first conductive film 6 (FIG. 2C). The second conductive film 7 can be formed by using the material shown in Embodiment 1. Here, ZnO (zinc oxide) to which an impurity such as Al or Ga is added is used. Consequently, an ohmic contact can be easily created between the second conductive film 7 and a ZnO film which is formed as a semiconductor layer later. The second conductive film 7 can be formed by sputtering. For example, the following methods can be used for adding Al or Ga: sputtering using a ZnO target to which 1 to 10 weight % of Al or Ga is added; or sputtering in which an Al or Ga chip is mounted on a ZnO target at 200 to 300°C.

[0067]

After forming the first conductive film 6, the second conductive film 7 may be formed continuously without being exposed to the air. Therefore, formation from the gate insulating film 5 to the second conductive film 7 may be continuously carried out without being exposed to air.

[0068]

A third conductive film 8 may be formed with a thickness of 10 to 200 nm between the first conductive film 6 and the second conductive film 7 (FIG. 2D). A contact resistance is occasionally increased between the first conductive film 6 and the second conductive film 7 depending on a heat treatment temperature in a manufacturing process. However, the contact resistance can be reduced between the first conductive film 6 and the second conductive film 7 by forming the third conductive film 8. The third conductive film 8 can be formed by using a metal film such as a Ti film which is formed by sputtering or the like.

[0069]

A resist mask 9 is formed over the second conductive film 7, and the second conductive film 7 is etched (FIGS. 3A and 3B). In the case of using wet etching, buffered fluoric acid (in which HF (hydrofluoric acid) and NH_4F (ammonium fluoride) are mixed), for example, solution

with a ratio of HF:NH_4F (weight ratio)=1: 100 to 1: 10 is used.

[0070]

In the case of using dry etching, anisotropic plasma etching using CH_4 gas can be used.

[0071]

Under the second conductive film 7, the first conductive film 6 is formed. Thus, the first conductive film 6 serves as an etching stopper when the second conductive film 7 is etched. Consequently, source and drain electrodes can be formed without damaging the gate insulating film 5 in etching.

[0072]

A part of the first conductive film 6 may be etched when the second conductive film 7 is etched. However, attention is required to be paid so as not to totally etch the first conductive film 6 because the gate insulating film is damaged if the first conductive film 6 is totally etched.

[0073]

Next, a source electrode 10 and a drain electrode 11 are formed by etching the first conductive film 6 using the resist mask 9 (FIG. 3C). In this invention, the first conductive film 6 is etched using an organic alkaline solution represented by TMAH (tetramethylammonium hydroxide), which is a developer for a photoresist.

[0074]

In the case of using an AlNi film for the first conductive film 6 and TMAH for etching solution, the etching ratio is approximately 300 nm/min at 30°C. On the other hand, the second conductive film 7 or the gate insulating film 5 to which the above-mentioned material is used is not etched with TMAH. Consequently, the source electrode 10 and the drain electrode 11 can be formed without damaging the gate insulating film 5. Further, the island-like shaped second conductive films 10b and 11b are not reduced in size. In this invention, the first conductive film 6 can be etched using a developer which is used when a resist mask is formed without using a special etching solution. Consequently, cost is reduced and efficiency is increased.

[0075]

The resist mask 9 is removed after forming the source electrode 10 and the drain electrode 11.

[0076]

A ZnO film is formed as a semiconductor film 12 with a thickness of 20 to 200 nm by sputtering over the source electrode 10, the drain electrode 11, and the gate insulating film 5 (FIG. 3D). For example, the film can be formed by sputtering using a ZnO target with a flow ratio of oxygen/argon ranging from 30 to 20, at 200 to 300°C.

[0077]

The semiconductor film 12 is etched by a photolithography method to form an island-like shaped semiconductor film 13 (FIG. 4A). A wet etching method using a buffered fluoric acid or anisotropic dry etching method using CH_4 gas can be used.

[0078]

Zno is commonly used in the semiconductor film 12 and the second conductive films 10b and 11b, and it is difficult to obtain a sufficient etching selectivity. However, since the second conductive film 7 is required to be formed in a portion in contact with the semiconductor film 12, the second conductive film 7 may be etched in a portion out of contact with the semiconductor film 12, for example, a wire portion. In the above-mentioned etching method, the second conductive films 10b and 11b may be etched, but the first conductive films 10a and 11a are not etched. Consequently, the first conductive films 10a and 11a serve as wires, and the electrical connection with the semiconductor device is ensured.

[0079]

An insulating film 14 is formed with a thickness of 50 nm to 1 μm over a semiconductor film 13 by CVD or sputtering (FIG. 4B). An insulating film containing silicon as a main component can be formed as the insulating film 14. An organic resin film or the like may be stacked over the insulating film containing silicon. The insulating film 14 functions as a planarization film or a passivation film. Since Al is included in the source electrode 10 and the drain electrode 11, a hillock is occasionally generated when the insulating film 14 is formed at high temperature. Thus, it is preferably formed at low temperature, 500°C or less, preferably 350°C or less.

[0080]

Contact holes are formed in the insulating film 14, and conductive films in contact with the gate electrode 3, the source electrode 10, and the drain electrode 11 are provided if necessary.

[0081]

According to this invention, a semiconductor device can be formed without damaging the gate insulating film. An Al alloy film such as an AlNi film is used as the first conductive film, thereby achieving lower resistance of the wire.

[0082]

[Embodiment 4]

Here, a manufacturing method of a top gate semiconductor device is described, in which an Al film or an Al alloy film is formed as a first conductive film on a silicon oxide film or a silicon oxynitride film, and a ZnO film to which an n-type or p-type impurity is added is formed as a second conductive film, and then, the second conductive film is formed to have an island-like shape by a first etching, the first conductive film is formed to have an island-like shape by a second etching to form source and drain electrodes, a ZnO semiconductor film is formed, a gate insulating film is formed, and a gate electrode is formed. Note that it is needless to say that materials and methods for manufacture described in Embodiments 1 to 3 can be applied to those used for the present embodiment.

[0083]

As shown in FIG. 5A, a silicon oxide (SiOx) film is formed as an insulating film 20 over a substrate 1 with a thickness of 10 to 200 nm by CVD or sputtering. The insulating film 20 prevents impurity or the like from diffusing from the substrate 1 side.

[0084]

A first conductive film 21 for the source and drain electrodes is formed with a thickness of 10 to 200 nm by sputtering or evaporation over the insulating film 20. An Al alloy film such as AlNi (aluminum nickel) film which is shown in Embodiment 1 can be used as the first conductive film 21. After forming the insulating film 20, the first conductive film 21 may be formed continuously without being exposed to the air.

[0085]

A second conductive film 22 is formed with a thickness of 10 to 200 nm by sputtering on the first conductive film 21 (FIG. 5A). As the second conductive film 22, ZnO (zinc oxide) to which a p-type or n-type impurity such as B (boron), Al (aluminum), Ga (gallium), P (phosphourus), or As (arsenic) is added can be used. After forming the first conductive film 21, the second conductive film 22 may be formed continuously without being exposed to the air.

Therefore, the steps of forming the insulating film 20 to the second conductive film 22 may be carried out continuously without being exposed to the air.

[0086]

A metal film such as a Ti film may be formed as a third conductive film 23 with a thickness of 10 to 200 nm by sputtering between the first conductive film 21 and the second conductive film 22 in order to reduce the contact resistance between the first conductive film 21 and the second conductive film 22 (FIG. 5B).

[0087]

A resist mask 24 is formed over the second conductive film 22, and the second conductive film 22 is etched (FIG. 5C). Wet etching using buffered fluoric acid or dry etching using CH_4 gas can be used as an etching method.

[0088]

The first conductive film 21 is formed under the second conductive film 22. Therefore, the first conductive film 21 serves as an etching stopper when the second conductive film 22 is etched. Thus, the source and drain electrodes can be formed without exposing the substrate 1 by etching the insulating film 20.

[0089]

When the second conductive film 22 is etched, a part of the first conductive film 21 may be etched. Note that if all of the first conductive film 21 is etched, the insulating film 20 is etched and the substrate 1 is exposed, which would cause diffusion of impurity included in the substrate 1.

[0090]

The first conductive film 21 is etched to form the source electrode 25 and the drain electrode 26 (FIG. 5D). Wet etching using a developer for a photoresist, TMAH is used as an etching method. Thus, the source electrode 25 and the drain electrode 26 can be formed without etching the insulating film 20. Further, the sizes of the island-like shaped second conductive films 25b and 26b are not reduced because the ZnO film is not etched by TMAH. Etching can be performed with a developer which is used in formation of a resist mask without a special etching solution for the first conductive film 21, which leads to cost reduction and improvement in efficiency.

[0091]

After forming the source electrode 25 and the drain electrode 26, the resist mask 24 is removed.

[0092]

A ZnO film is formed with a thickness of 20 to 200 nm by sputtering as the semiconductor film 27 over the source electrode 25, the drain electrode 26, and the insulating film 20 (FIG. 6A).

[0093]

The semiconductor film 27 is etched by a photolithography method to make an island-like shaped semiconductor film 27. Wet etching using buffered fluoric acid or dry etching using CH_4 gas can be used as an etching method.

[0094]

ZnO is commonly used for the semiconductor film 27 and the second conductive films 25b and 26b, and it is difficult to obtain a high etching selectivity. However, the second conductive film may be etched in the portion out of contact with the semiconductor film 27, specially the wire portion, because the second conductive film 22 may be formed in the source and drain electrode portions, which is the same as Embodiment 3.

[0095]

A gate insulating film 28 is formed with a thickness of 10 to 200 nm by CVD or sputtering over the semiconductor film 27 (FIG. 6B). The semiconductor film 27 may be subjected to a high density plasma treatment shown in the above-mentioned Embodiment to form a gate insulating film. The surface of the semiconductor film 27 can be nitrided by the high density plasma treatment under a nitriding atmosphere such as an atmosphere containing nitrogen and a noble gas; an atmosphere containing nitrogen, hydrogen, and a noble gas; and an atmosphere containing ammonia and a noble gas.

[0096]

The gate insulating film 28 may be formed by using an insulating film containing silicon as a main component, for example, a silicon oxide film, a silicon oxynitride film, a silicon nitride film, and a silicon nitride oxide film. In addition, it may be a single layer or a layered film.

[0097]

A gate electrode 29 is formed over the gate insulating film 28 (FIG. 6B). The gate electrode 29 can be formed by using the material shown in the above-mentioned embodiment, and may be a single layer or a layered film including two or more layers. A known CVD sputtering, evaporation, or the like can be employed as a method for film formation. Dry etching or wet etching method can be used for processing the gate electrode 29 into an island-like shape with a photolithography method.

[0098]

An insulating film 30 is formed with a thickness of 50 nm to 1 μm by CVD or sputtering over the gate electrode 29 and the gate insulating film 28 (FIG. 6C). The insulating film 30 can be formed by using an insulating film containing silicon. An organic resin film or the like may be stacked over the insulating film containing silicon. The insulating film 30 functions as a planarization film or a passivation film. Since Al is included in the source electrode 25 and the drain electrode 26, a hillock is occasionally generated when the gate insulating film 28, the gate electrode 29, and the insulating film 30 are formed at a high temperature. Thus, they are preferably formed at a low temperature, at 500°C or less, preferably 350°C or less.

[0099]

As described above, this invention can prevent an impurity from diffusing due to an exposure of the substrate 1. An Al alloy film such as an AlNi film is used as the first conductive film, thereby achieving lower resistance of a wire.

[0100]

[Embodiment 5]

Here, a description is made of a method of manufacturing a liquid crystal display device using a bottom gate semiconductor device which is shown in Embodiments 1 and 3 referring to FIGS. 8A and 8B and 9A and 9B. Note that it is needless to say that the top gate semiconductor device which is shown in Embodiments 2 and 4 can be applied. FIGS. 8A and 9A show cross-sectional views taken along line X-Y in FIG. 8B.

[0101]

A gate wire 40 and an auxiliary capacitor wire 41 are formed over a glass substrate or a

plastic substrate 1. An AlNd film is formed by sputtering, and then, formed by known photolithography method and etching.

[0102]

A gate insulating film 42 formed by using a silicon oxide film or a silicon oxynitride film is formed by CVD or sputtering.

[0103]

An AlNi film is formed as a first conductive film by sputtering over the gate insulating film 42. The first conductive film forms a source electrode 45a, a drain electrode 46a and a source wire 47 later.

[0104]

A ZnO (zinc oxide) film to which Al is added is formed as a second conductive film by sputtering over the first conductive film. The second conductive film forms a source electrode 45b, a drain electrode 46b, and a source wire 47 later.

[0105]

A resist mask is formed in a region which is to be a source electrode portion, a drain electrode portion, and a source wire portion, over the second conductive film (not shown in the figure). Then, the second conductive film is etched. Here, etching is performed using buffered fluoric acid and a solution of $HF:NH_4F=1:100$ (weight ratio).

[0106]

Next, the first conductive film is etched using TMAH solution to form the source electrode 45a, the drain electrode 46a, and the source wire 47. After that, the resist mask is removed. Then, the source electrode 45, the drain electrode 46, and the source wire 47 can be formed without damaging the gate insulating film 42. In addition, since the ZnO film is not etched by TMAH, the size of the island-like shaped second conductive film is not reduced. Further, since an AlNi film is used for the first conductive film, the resistance of the source wire can be reduced.

[0107]

Next, a semiconductor film 48 is formed. A ZnO film is formed by sputtering, and then, the semiconductor film 48 is formed from the ZnO film by a photolithography method and etching. Wet etching using buffered fluoric acid is used as etching. The portion of the second

conductive film out of contact with the semiconductor film 48 may be partially removed here, because the first conductive film is formed in a portion to be a wire.

[0108]

An insulating film 49 is formed by CVD, sputtering, coating, or the like over the semiconductor film 48. The insulating film 49 can be formed by using a layered film having an insulating film containing silicon, an organic resin film, or the like. The insulating film 49 may be a film which makes the unevenness of the surface planarized.

[0109]

A contact hole leading to the drain electrode 46 and a contact hole for the auxiliary capacitor are formed in the insulating film 49 using a photolithography method and an etching method.

[0110]

A transparent conductive film is formed by sputtering, and then, a pixel electrode 50 is formed using a photolithography method and etching. For example, ITO (Indium Tin Oxide), ITSO (Indium Tin Oxide containing silicon oxide), or IZO (Indium Zinc Oxide) may be used.

[0111]

In the case of a reflective liquid crystal display device, a light reflective metal material such as Ag (silver), Au (gold), Cu (copper), W (tungsten), or Al (aluminum) is formed instead of a transparent electrode.

[0112]

The portion where the pixel electrode 50 and the auxiliary capacitor wire 41 are overlapped forms an auxiliary capacitor 100 which is formed of the pixel electrode 50, the gate insulating film 42, and the auxiliary capacitor wire 41 (FIGS. 8A and 8B).

[0113]

A corner of a bent portion or a portion where width changes may be smoothed and rounded in a wire and an electrode. A shape of a chamfered corner can be realized by using a photomask pattern manufactured using a pattern of photomask. This will have advantages described below. When dry etching using plasma is performed, generation of fine particles due to abnormal discharge can be suppressed by chamfering a projecting portion. Even though the fine particles are generated, the fine particles can be prevented from accumulating at the corner

at the time of cleaning, and the fine particles can be washed away by chamfering a concave portion. Thus, a problem of fine particles or dust in the manufacturing process can be solved and the yield can be improved.

[0114]

An alignment film 51 is formed so as to cover the pixel electrode 50. The alignment film is formed by a droplet discharge method, printing, or the like. After forming the alignment film, rubbing is conducted.

[0115]

A color filter 55 is formed by using a colored layer and a light-shielding layer (black matrix), and a protective insulating film 54 is formed on an opposing substrate 56. A transparent electrode 57 is formed, and an alignment film 53 is formed on the protective insulating film 54 (FIG. 9A). The alignment film is subjected to a rubbing process.

[0116]

Next, a closed pattern 75 of a sealant is formed by a droplet discharge method (FIG. 9B). A region surrounded by the sealant is filled with liquid crystal composition 52 (FIG. 9A).

[0117]

After dropping the liquid crystal composition 52 in the closed pattern 75, the opposing substrate 56 and a substrate 1 in which a semiconductor device is formed are attached to each other. When the liquid crystal composition 52 is filled, thefollowing alternative may be adopted: a seal pattern having an opening portion is provided on the substrate 1; the opposing substrate 56 and the substrate 1 are attached to each other; then, liquid crystal is injected using capillary action.

[0118]

As an alignment mode of the liquid crystal composition 52, TN mode in which the alignment of liquid crystal molecules is twisted at 90° from the side of light incidence to the side of light emission, FLC mode, IPS mode, or the like can be used. Note that an electrode pattern is different from one shown in FIG. 8B and is a comb-like shape in the case of the IPS mode.

[0119]

Polarizing plates are attached to both of the opposing substrate 56 and the substrate 1 on which the semiconductor device is formed. In addition, an optical film can be attached if

required.

[0120]

The distance between the opposing substrate 56 and the substrate 1 on which the semiconductor device is formed may be kept by dispersing spherical spacers or forming a columnar spacer formed of a resin, or by mixing fillers in the sealant. The aforementioned columnar spacer is formed of an organic resin material containing at least one of acrylic, polyimide, polyimide amide, or epoxy as a main component, or an inorganic material having one of silicon oxide, silicon nitride and silicon oxide containing nitrogen, or a layered film thereof.

[0121]

Then, an FPC (Flexible Printed Circuit) is attached to the the substrate 1 with an anisotropic conductive layer interposed therebetween using a known technique.

[0122]

A peripheral driver circuit may be formed over the substrate. A plane exemplary diagram is shown in FIG. 9B.

[0123]

A gate wire driver circuit 62, a source wire driver circuit 63, and an active matrix portion 64 are formed over a substrate 61 formed of glass or the like. The gate wire driver circuit 62 is constituted from at least a shift register 62a and a buffer 62b. The source wire driver circuit 63 is constituted from at least a shift register 63a, a buffer 63b, and an analog switch 69 which samples video signals transmitted via video lines 68. A plurality of gate wires 72 extended from the gate wire driver circuit 62 is arranged in parallel with each other in the active matrix portion 64. A plurality of source wires 71 extended from the source wire driver circuit 63 is arranged orthogonally to the gate wires 72. In addition, an auxiliary capacitor wire 73 is arranged in parallel with the gate wires 72. In addition, a semiconductor device 65, a liquid crystal portion 66, and an auxiliary capacitor 67 are provided in a region surrounded by the gate wire 72, the source wires 71, and the auxiliary capacitor wire 73.

[0124]

The gate wire driver circuit 62, the source wire driver circuit 63, and the analog switch 69 are provided with a semiconductor device manufactured by the same manufacturing method as the semiconductor device 65 to have a similar structure.

[0125]

In the semiconductor device 65, a gate electrode is connected to the gate wire 72, and the source electrode is connected to the source wire 71. A liquid crystal portion 66 is formed by introducing a liquid crystal to be sealed between a pixel electrode connected to the drain electrode of the semiconductor device 65 and an opposing electrode over the opposing substrate. The auxiliary capacitor wire 73 is connected to an electrode having the same potential as the opposing electrode.

[0126]

In the aforementioned liquid crystal display device, the gate insulating film is not etched and the characteristics do not become unstable, and thus, high reliability is realized. In the case of using a top gate semiconductor device, a glass substrate or a base film formed by using, a silicon oxide film or a silicon oxynitride film is not etched, so that impurity such as sodium is not diffused into a semiconductor film from the substrate and the characteristics are not deteriorated, and thus, high reliability can be realized.

[0127]

Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

[0128]

[Embodiment 6]

Here, a description is made of a method for manufacturing a light-emitting device with using the bottom gate semiconductor device shown in Embodiments 1 and 3 referring to FIGS. 10A and 10B and 11A and 11B. Note that it is needless to say that the semiconductor device of Embodiments 2 and 4 can be applied.

[0129]

The semiconductor device is manufactured based on the description of the aforementioned embodiment, and formation to the stage shown in FIG. 10A is carried out. Note that the same parts as those of the above embodiments are denoted by the same reference numerals.

[0130]

In the EL display device, the pixel electrode 50 functions as an anode or a cathode. As

the material for the pixel electrode 50, the following can be employed: a conductive metal such as aluminum (Al), silver (Ag), gold (Au), platinum (Pt), nickel (Ni), tungsten (W), chromium (Cr), molybdenum (Mo), iron (Fe), cobalt (Co), copper (Cu), palladium (Pd), lithium (Li), caesium (Cs), magnesium (Mg), calcium (Ca), strontium (Sr), or titanium (Ti); an alloy such as aluminum-silicon (Al-Si), aluminum-titanium (Al-Ti), or aluminum-silicon-copper (Al-Si-Cu); nitride of a metal material such as titanium nitride (TiN); a metal compound such as ITO, ITO containing silicon, or IZO.

[0131]

An electrode from which light emitted from an EL layer is extracted is only required to be formed by using a light-transmitting conductive film, and a very thin film of metal such as Al or Ag may be used as well as a metal compound such as ITO, ITO containing silicon, or IZO.

[0132]

When light-emission is extracted from an electrode which is opposed to the pixel electrode 50, a highly reflective material (Al, Ag, or the like) can be used for the pixel electrode 50. In this embodiment, ITSO, which means ITO containing silicon, is used as the pixel electrode 50 (FIG. 10A).

[0133]

Next, an insulating film formed by using an organic material or an inorganic material is formed so as to cover the insulating film 49 and the pixel electrode 50. Then, the insulating film is processed to expose the pixel electrode 50 partially, thereby forming partition walls 81. As the material of the partition walls 81, a photosensitive organic material (such as acrylic or polyimide) is preferable. Alternatively, a non-photosensitive organic material or inorganic material may also be used. Further, the partition walls 81 may be used as a black matrix by coloring the partition walls 81 black in such a way that a black pigment or dye such as titanium black or carbon nitride is dispersed into the material of the partition wall 81 with the use of a dispersant. It is desirable that the partitions wall 81 have a tapered shape and those end surfaces 81a toward the pixel electrode have curvatures changing continuously (FIG. 10B).

[0134]

Next, a layer 82 including a light-emitting substance is formed, and an opposing electrode 83 which covers the layer 82 including a light-emitting substance is formed. Then, a

light-emitting element with the layer 82 including a light-emitting substance interposed between the pixel electrode 50 and the opposing electrode 83 can be manufactured, and light-emission can be obtained by applying a voltage between the opposing electrode 83 and the pixel electrode 50.

[0135]

As an electrode material used for forming the opposing electrode 83, a material similar to one which can be used for the pixel electrode can be used. In this embodiment, aluminum is used for a second electrode.

[0136]

The layer 82 including a light-emitting substance is formed by evaporation, ink-jet, spin coating, dip coating, roll-to-roll method, sputtering, or the like.

[0137]

In the case of an organic electroluminescent display device, the layer 82 including a light-emitting substance may be a layered film of layers having functions of hole transportation, hole injection, electron transportation, electron injection, or light-emission, respectively, or a single layer of a light-emitting layer. As a layer including a light-emitting substance, a single layer or a layered film of an organic compound may be used.

[0138]

A hole injecting layer is provided between an anode and a hole transporting layer. As the hole injecting layer, a mixed layer of an organic compound and a metal oxide can be used. This prevents short circuit between the pixel electrode 50 and the opposing electrode 83 due to unevenness which is formed on the surface of the pixel electrode 50 or a foreign substance which is left on the surface of the electrode. The thickness of the mixed layer is preferably 60 nm or more, more preferably 120 nm or more. Since increase in thickness of a film does not cause increase in driving voltage, the thickness of the film can be selected such that the influence of the unevenness or foreign substance can be covered sufficiently. Thus, a dark spot is not generated, and driving voltage or power consumption is not increased in the light-emitting device manufactured by this invention.

[0139]

An oxide or a nitride of transition metal is preferable as a metal oxide, concretely,

zirconium oxide, hafnium oxide, vanadium oxide, niobium oxide, tantalum oxide, chromium oxide, molybdenum oxide, tungsten oxide, titanium oxide, manganese oxide, and rhenium oxide.

[0140]

As an organic compound, the following can be employed: an organic material having an arylamino group such as 4,4'-bis[N-(1-napthyl)-N-phenylamino]biphenyl (NPB), 4,4'-bis[N-(3-methylphenyl]-N-phenylamino]biphenyl (TPD), 4,4',4''-tris(N,N-diphenylamino)triphenylamine (TDATA), 4,4',4''-tris[N-(3-methylphenyl)-N-phenylamino]triphenylamine (MTDATA), 4,4'-bis{N-[4-(N,N-di-m-tolylamino)phenyl]-N-phenylamino}biphenyl (DNTPD), 1,3,5-tris[N,N-di(m-tolyl)amino] benzene (m-MTDAB), and 4,4',4''-tris(N-carbazolyl) triphenylamine (TCTA); phthalocyanine (H_2Pc); copper phthalocyanine (CuPc); vanadyl phthalocyanine (VOPc); or the like.

[0141]

The hole transporting layer is provided between the anode and a light-emitting layer, or between the hole injecting layer and the light-emitting layer when the hole injecting layer is provided. The hole transporting layer is formed by using a layer which has an excellent property of transporting a hole, for example, a layer formed by using a compound of aromatic amine (that is, having a benzene ring-nitrogen bond) such as NPB, TPD, TDATA, MTDATA, and BSPB. The substances mentioned here have the hole mobility of 1×10^{-6} to 10 cm^2/Vs mainly. Note that a substance having higher transporting property of holes than electrons may be used as well as the materials. Note that the hole transporting layer may be formed by not only a single layer but also a layered film in which two or more layers formed from the above mentioned substances are stacked.

[0142]

The light-emitting layer is provided between the anode and the cathode, or between the hole transporting layer and the electron transporting layer when the hole transporting layer and the electron transporting layer are provided. There is no particular limitation on the light-emitting layer; however, a layer serving as the light-emitting layer has two modes roughly. One is a host-guest type layer which includes a dispersed light-emitting substance in a layer formed of a material (host material) having a larger energy gap than an energy gap of a

light-emitting substance (dopant material) which becomes a luminescent center, while the other is a layer in which a light-emitting layer is made of a light-emitting substance only. The former is preferable, because concentration quenching hardly occurs. As the light-emitting substance to be a luminescent center, the following can be employed: 4-dicyanomethylene-2-methyl-6-(1,1,7,7-tetramethyljulolidyl-9-enyl)-4H-pyran (DCJT); 4-dicyanomethylene-2-t-butyl-6-(1,1,7,7-tetramethyljulolidine-9-enyl)-4H-pyran; periflanthene; 2,5-dicyano-1, 4-bis(10-methoxy-1,1,7,7-tetramethyljulolidine-9-enyl)benzene; N,N'-dimethylquinacridone (DMQd); coumarin 6; coumarin 545T; tris (8-quinolinolato)aluminum (Alq_3); 9,9'-bianthryl; 9,10-diphenylanthracene (DPA); 9,10-bis(2-naphthyl)anthracene (DNA); 2,5,8,11-tetra-t-butylperylene (TBP); PtOEP; $Ir(ppy)_3$; $Btp_2Ir(acac)$; FIrpic; or the like. As the base material to be a host material in the case of forming the layer in which the light-emitting substance is diffused, the following can be used: an anthracene derivative such as 9,10-di(2-naphtyl)-2-tert-butylanthracene (t-BuDNA); a carbazole derivative such as 4,4'-bis(N-carbazolyl)biphenyl (CBP); or a metal complex such as tris(8-quinolinolato)aluminum (Alq_3), tris(4-methyl-8-quinolinolato)aluminum ($Almq_3$); bis(10-hydroxybenzo[h]-quinolinato)beryllium ($BeBq_2$); bis(2-methyl-8-quinolinolato)-4-phenylphenolato-aluminum (BAlq); bis[2-(2-hydroxyphenyl)pyridinato]zinc ($Znpp_2$); or bis[2-(2-hydroxyphenyl)benzoxazolate]zinc (ZnBOX). As the material which can constitute the light-emitting layer only with a light-emitting substance, tris(8-quinolinolato)aluminum (Alq_3), 9,10-bis(2-naphtyl)anthracene (DNA), bis(2-methyl-8-quinolinolato)-4-phenylphenolato-aluminum (BAlq), or the like can be used.

[0143]

An electron transporting layer is provided between the light-emitting layer and the cathode, or between the light-emitting layer and an electron injecting layer when the electron injecting layer is provided. The electron transporting layer is a layer having an excellent electron transporting property, and for example, a layer formed using a metal complex having a quinoline skeleton or a benzoquinoline skeleton such as tris(8-quinolinolato)aluminum (Alq_3), tris(5-methyl-8-quinolinolato)aluminum ($Almq_3$), bis(10-hydroxybenzo[h]-quinolinato)beryllium ($BeBq_2$), and bis(2-methyl-8-quinolinolato)-4-phenylphenolato-aluminum (BAlq). In addition,

a metal complex having an oxazole ligand or a thiazole ligand such as bis[2-(2-hydroxyphenyl)-benzoxazolato]zinc ($Zn(BOX)_2$), bis[2-(2-hydroxyphenyl)-benzothiazolato]zinc ($Zn(BTZ)_2$), or the like can be used. In addition to the metal complexes, 2-(4-biphenylyl)-5-(4-tert-butylphenyl)-1,3,4-oxadiazole (PBD); 1,3-bis[5-(p-tert-butylphenyl)-1,3,4-oxadiazole-2-yl]benzene (OXD-7); 3-(4-tert-butylphenyl)-4-phenyl-5-(4-biphenylyl)-1,2,4-triazole (TAZ); 3-(4-tert-butylphenyl)-4-(4-ethylphenyl)-5-(4-biphenylyl)-1,2,4-triazole (p-EtTAZ); bathophenanthroline (BPhen); bathocuproine (BCP); or the like can be used. These substances mentioned here mainly have the electron mobility of 1×10^{-6} to 10 cm^2/Vs. Note that other substance may be used for the electron transporting layer so long as it has a higher electron transporting property than a hole transporting property. Further, the electron transporting layer may be formed by not only a single layer but also a layered film in which two or more layers made from the above mentioned substances are stacked.

[0144]

The electron injecting layer is provided between the cathode and the electron transporting layer. As the electron injecting layer, a compound of alkali metal or alkaline earth metal such as lithium fluoride (LiF), cesium fluoride (CsF), or calcium fluoride (CaF_2) can be employed. In addition to that, a layer formed by using an electron transporting substance which contains alkali metal or alkaline earth metal, for example, Alq_3 containing magnesium (Mg) or the like can be used.

[0145]

In the case of an inorganic electroluminescent display device, one in which a fluorescent substance particles are diffused in dispersing agent for the layer 82 including a light-emitting substance can be used.

[0146]

A fluorescent substance in which a donor impurity such as Cl (chlorine), I (iodine), or Al (aluminum) is added with Cu (copper) in ZnS can be used.

[0147]

As the dispersing agent, the following can be employed: a polymer having a relatively high dielectric constant such as cyanoethyl cellulose based resin, polyethylene based resin,

polypropylene based resin, polystyrene based resin, silicone resin, epoxy resin, vinylidene fluoride resin, or the like. The dielectric constant can be adjusted by mixing the resin and minute particles having high dielectric constant such as $BaTiO_3$ (barium titanate) or $SrTiO_3$ (strontium titanate). As a diffusing means, an ultrasonic diffusing machine or the like can be used.

[0148]

A dielectric layer may be provided between the layer 82 including a light-emitting substance and one of the electrodes. For the dielectric layer, a highly dielectric and insulating material which has a high dielectric breakdown voltage is employed. One is selected from a metal oxide or nitride, for example, TiO_2, $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $KNbO_3$, $PbNbO_3$, Ta_2O_3, $BaTa_2O_6$, $LiTaO_3$, Y_2O_3, Al_2O_3, ZrO_2, AlON, ZnS, or the like. Those may be disposed as a uniform film or a film having a particle structure.

[0149]

In the case of an inorganic electroluminescent display device, a double-insulating structure in which a light-emitting layer is interposed between insulating layers may be employed. The light-emitting layer can be formed by using a II-VI compound such as Mn (manganese) or ZnO (zinc sulfide) containing a rare earth element, and the insulating layer can be formed by using oxide or nitride such as Si_3N_4, SiO_2, Al_2O_3, or TiO_2.

[0150]

A silicon oxide film containing nitrogen is formed as a passivation film over the opposing electrode 83 by plasma CVD (not shown). In the case of using a silicon oxide film containing nitrogen, the following can be used: a silicon oxynitride film formed by using SiH_4, N_2O, and NH_3 by plasma CVD; a silicon oxynitride film formed by using SiH_4, and N_2O; or a silicon oxynitride film formed by using a gas in which SiH_4 and N_2O is diluted with Ar.

[0151]

A silicon oxide nitride hydride film manufactured from SiH_4, N_2O, and H_2 may be employed as a passivation film. Note that a passivation film is not limited to the aforementioned substance. Another insulating film containing silicon as a main component can be also used. In addition, a layered film structure may be employed as well as a single layer structure. Further, a multilayer film of a carbon nitride film and a silicon nitride film or a

multilayer film of a styrene polymer can be used. A silicon nitride film or a diamond-like carbon film may be formed.

[0152]

Then, a display portion is sealed to protect a light-emitting element from a material such as water which promotes deterioration. In the case of using an opposing substrate for sealing, the opposing substrate is attached by using an insulating sealant so as to expose an external connection portion. A space between the opposing substrate and an element substrate may be filled with an inert gas such as dry nitrogen, or the opposing substrate may be attached by applying a sealant to the pixel portion entirely. It is preferable to use an ultraviolet curing resin or the like as the sealant. A drying agent or particles for keeping the gap between the substrates constant may be mixed in the sealant. Then, the light-emitting device is completed by attaching a flexible wire board to the external connection portion.

[0153]

One example of a structure of the light-emitting device manufactured as described above is shown referring to FIGS. 11A and 11B. Note that portions having the same functions are sometimes denoted by the same reference numerals even though they have different shapes, and the explanations are occasionally omitted.

[0154]

FIG. 11A shows a structure in which the pixel electrode 50 is formed using a light transmitting conductive film, and light generated in the layer 82 including a light-emitting substance is emitted toward a substrate 1. Further, reference numeral 86 denotes an opposing substrate. This opposing substrate is firmly attached to the substrate 1 using a sealant or the like after forming a light emitting element. A space between the opposing substrate 86 and the element is filled with resin 85 having a light-transmitting property or the like to seal the light emitting element. Accordingly, the light emitting element can be prevented from being deteriorated by moisture or the like. Preferably, the resin 85 has a hygroscopic property. More preferably, a drying agent 84 with a high light-transmitting property is dispersed in the resin 85 to prevent the adverse influence of moisture.

[0155]

FIG. 11B shows a structure in which both the pixel electrode 50 and an opposing

substrate 83 are formed by using conductive films having light-transmitting property. Accordingly, light can be emitted toward both the substrate 1 and the opposing substrate 86 as shown by an arrow of dotted lines. In this structure, by providing polarizing plates 88 outside of the substrate 1 and the opposing substrate 86, a screen can be prevented from being transparent, thereby improving visibility. Protection films 87 are preferably provided outside of the polarizing plates 88.

[0156]

The light-emitting device of this invention having a display function may employ either an analog video signal or a digital video signal. If a digital video signal is used, the video signal may use either a voltage or a current.

[0157]

When the light-emitting element emits light, a video signal to be inputted to a pixel may have either a constant voltage or a constant current. When a video signal has a constant voltage, a constant voltage is applied to a light-emitting element or a constant current flows through the light-emitting element.

[0158]

Also, when a video signal has a constant current, a constant voltage is applied to a light-emitting element or a constant current flows through the light-emitting element. A driving method where a constant voltage is applied to a light-emitting element is called a constant voltage drive. Meanwhile, a driving method where a constant current flows through a light-emitting element is called a constant current drive. In the constant current drive, constant current flows regardless of change in resistance of a light emitting element. The light emitting display device according to this invention and the driving method thereof may use any one of the aforementioned methods.

[0159]

In the light-emitting device, a gate insulating film is not etched, and the characteristics of the light-emitting element is not unstable so that its reliability is high. In the case of using a top gate semiconductor device, since a glass substrate or a base film formed by using, a silicon oxide film or a silicon oxynitride film is not etched, impurity such as sodium which deteriorates characteristics is not diffused from the substrate into the semiconductor film so that high

reliability is obtained.

[0160]

Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

[0161]

A pixel circuit and a protective circuit included in a panel and module, and operation thereof are shown referring to FIGS. 12A to 12F and 13 or the like. FIGS. 10A and 10B and 11A and 11B each show a cross-sectional view of a driving TFT 1403 of the semiconductor device. A switching TFT 1401, a current control TFT 1404, and an eraser TFT 1406 may be manufactured at the same time of the driving TFT 1403, and may have the same structure as the driving TFT 1403.

[0162]

A pixel shown in FIG. 12A includes a signal line 1410 and power source lines 1411 and 1412 arranged in a column direction and a scan line 1414 arranged in a row direction. The pixel further includes a switching TFT 1401, the driving TFT 1403, the current control TFT 1404, an auxiliary capacitor 1402, and a light-emitting element 1405.

[0163]

A pixel shown in FIG. 12C has the same structure as one in FIG. 12A except for that the gate electrode of the driving TFT 1403 is connected to the power source line 1412 provided in the row direction. In other words, the pixels shown in FIGS. 12A and 12C have the same equivalent circuit diagram. However, a power source line formed in the case of arranging the power source line 1412 in the column direction (FIG. 12A) is formed by using a conductive layer in a different layer from a layer in which a power source line is formed by using a conductive layer in the case of arranging the power source line 1412 in the row direction (FIG. 12C). Here, attention is paid to a wire connected to the gate electrode of the driving TFT 1403, and the structure is shown separately in FIGS. 12A and 12C in order to show that these wires are manufactured with different layers.

[0164]

As a feature of the pixels shown in FIGS. 12A and 12C, the driving TFT 1403 and the current control TFT 1404 are connected serially within the pixel, and it is preferable to set the

channel length L (1403) and the channel width W (1403) of the driving TFT 1403, and the channel length L (1404) and the channel width W (1404) of the current control TFT 1404 so as to satisfy L (1403)/W (1403):L (1404)/W (1404)=5 to 6000:1.

[0165]

The driving TFT 1403 operates in a saturation region and serves to control the current value of the current flowing into the light-emitting element 1405. The current control TFT 1404 operates in a linear region and serves to control the current supplied to the light-emitting element 1405. Both the TFTs preferably have the same conductivity type in the manufacturing process, and the TFTs are n-channel type TFTs in this embodiment. The driving TFT 1403 may be either an enhancement mode TFT or a depletion mode TFT. Since the current control TFT 1404 operates in the linear region in the light-emitting device having the above structure, slight fluctuation of Vgs of the current control TFT 1404 does not affect the current value of the light-emitting element 1405. That is to say, the current value of the light-emitting element 1405 can be determined by the driving TFT 1403 operating in the saturation region. With the above structure, the variation of the luminance of the light-emitting element due to the variation of the characteristics of the TFT can be remedied, thereby providing a light-emitting device having improved image quality.

[0166]

In each pixel shown in FIGS. 12A to 12D, the switching TFT 1401 is to control the input of the video signal to the pixel, and the video signal is inputted into the pixel when the switching TFT 1401 is turned on. Then, the voltage of the video signal is held in the auxiliary capacitor 1402. Although FIGS. 12A and 12C show the structure in which the auxiliary capacitor 1402 is provided, this invention is not limited thereto. When the gate capacitance and the like can serve as a capacitor holding the video signal, the auxiliary capacitor 1402 is not necessarily provided.

[0167]

A pixel shown in FIG. 12B has the same pixel structure as that in FIG. 12A except for that a TFT 1406 and a scan line 1415 are added. In the same way, a pixel shown in FIG. 12D has the same pixel structure as that in FIG. 12C expect for that the TFT 1406 and the scan line 1415 are added.

[0168]

ON and OFF of the TFT 1406 is controlled by the additionally provided scan line 1415. When the TFT 1406 is turned on, the charge held in the auxiliary capacitor 1402 is discharged, thereby turning off the current control TFT 1404. In other words, by the provision of the TFT 1406, a state can be produced compellingly in which the current does not flow into the light-emitting element 1405. For this reason, the TFT 1406 can be referred to as an eraser TFT. Consequently, in the structures shown in FIGS. 12B and 12D, a lighting period can be started at the same time as or just after the start of a writing period before the writing of the signal into all the pixels; therefore the duty ratio can be increased.

[0169]

In a pixel shown in FIG. 12E, the signal line 1410 and the power source line 1411 are arranged in the column direction, and the scan line 1414 is arranged in the row direction. Further, the pixel includes the switching TFT 1401, the driving TFT 1403, the auxiliary capacitor 1402, and the light-emitting element 1405. A pixel shown in FIG. 12F has the same pixel structure as that shown in FIG. 12E except for that the TFT 1406 and the scan line 1415 are added. In the structure shown in FIG. 12F, the duty ratio can also be increased by the provision of the TFT 1406.

[0170]

Such an active matrix light-emitting device can be driven at low voltage when the pixel density increases, because the TFTs are provided in respective pixels. Therefore, it is considered that the active matrix light-emitting device is advantageous.

[0171]

Although this embodiment described the active matrix light-emitting device in which the respective TFTs are provided in respective pixels, a passive matrix light-emitting device can also be formed. Since the TFTs are not provided in respective pixels in the passive matrix light-emitting device, high aperture ratio can be obtained. In the case of a light-emitting device in which light is emitted to both sides of the light emission stack, the transmissivity of the passive matrix light-emitting device is increased.

[0172]

Subsequently, a case will be described in which a diode is provided as a protective

circuit on the scan line and the signal line with the use of an equivalent circuit shown in FIG. 12E.

[0173]

In FIG. 13, the switching TFT 1401, the driving TFT 1403, the auxiliary capacitor 1402, and the light-emitting element 1405 are provided in a pixel area 1500. Diodes 1561 and 1562 are provided on the signal line 1410. In the similar way to the switching TFT 1401 and the driving TFT 1403, the diodes 1561 and 1562 are manufactured based on the above embodiments, and have a gate electrode, a semiconductor layer, a source electrode, a drain electrode, and the like. The diodes 1561 and 1562 are operated as diodes by connecting the gate electrode with the drain electrode or the source electrode.

[0174]

Common potential lines 1554 and 1555 connecting to the diodes 1561 and 1562 are formed by using the same layer as the gate electrode. Therefore, in order to connect the common potential lines 1554 and 1555 with the source electrode or the drain electrode of the diode, it is necessary to form a contact hole in the gate insulating layer.

[0175]

Diodes 1563 and 1564 provided on the scan line 1414 have a similar structure. Further, common potential lines 1565 and 1566 has the similar structure.

[0176]

In this manner, protection diodes can be simultaneously formed in an input stage according to this invention. Further, the positions of the protection diodes are not limited to this, and they can be provided between a driver circuit and a pixel.

[0177]

A top view of a pixel portion in the case of using an equivalent circuit shown in FIG. 12E is described in FIG. 14A. In addition, the same equivalent circuit as that in FIG. 12E is shown in FIG. 14B. Each semiconductor device shown in FIGS. 10A, 10B, 11A, and 11B is corresponds to each driving TFT 1403. FIGS. 10A, 10B, 11A and 11B show cross-sectional views taken along line X-Y in FIG. 14A and 14B. The power source line 1411, the signal line 1410, and the source electrode and the drain electrode of the switching TFT 1401 are formed by using the first conductive film, and the source electrode and the drain electrode of the driving

TFT 1403 are formed by using the second conductive film.

[0178]

The switching TFT 1401 is manufactured by the same method as the driving TFT 1403. The drain electrode of the switching TFT 1401 and a gate electrode 40 of the driving TFT 1403 are connected electrically with each other through a contact hole formed in an insulating film in the same layer as the gate insulating film 42.

[0179]

The auxiliary capacitor 1402 is formed by using a portion where the gate electrode of the driving TFT 1403 is extended, the power source line 1411, and an insulating film in the same layer as the gate insulating film 42.

[0180]

A light-emitting region 1420 is formed in an opening portion of a partition wall 81. The partition wall 81 is formed in the vicinity of the light-emitting region 1420, although it is not shown. The corner portion of the light-emitting region 1420 may be rounded. By making the corner portion of the opening portion of the partition wall 81 rounded, the corner portion of the light-emitting region 1420 can be rounded. When dry etching using plasma is performed to process the partition wall 81, generation of fine particles due to abnormal discharge can be suppressed by making the corner portion rounded.

[0181]

This embodiment can be combined with a suitable structure of the above embodiments as appropriate.

[0182]

[Embodiment 7]

As an electronic device having semiconductor devices according to this invention mounted with modules shown as examples in the above embodiments, a camera such as a video camera or a digital camera; a goggle type display (a head mounted display); a navigation system; an audio reproducing device (e.g., a car audio component); a computer; a game machine; a portable information terminal (e.g., a mobile computer, a cellular phone, a portable game machine, an electronic book, or the like); an image reproducing device equipped with a recording medium (specifically, a device which can reproduce the content of a recording medium

such as a digital versatile disc (DVD) and which has a display for displaying an image stored therein); and the like can be given. Specific examples of these electronic appliances are shown in FIGS. 15A to 15E, and FIG. 16.

[0183]

FIG. 15A shows a monitor for a television receiver or a personal computer, or the like, including a housing 3001, a display area 3003, speakers 3004, and the like. An active matrix display device is provided in the display area 3003. Each pixel of the display area 3003 includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a television with less characteristic deterioration can be obtained.

[0184]

FIG. 15B shows a cellular phone, including a main body 3101, a housing 3102, a display area 3103, an audio input portion 3104, an audio output portion 3105, operation keys 3106, an antenna 3108, and the like. An active matrix display device is provided in the display area 3103. Each pixel of the display area 3103 includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a cellular phone with less characteristic deterioration can be obtained.

[0185]

FIG. 15C shows a computer, including a main body 3201, a housing 3202, a display area 3203, a keyboard 3204, an external connection port 3205, a pointing mouse 3206, and the like. An active matrix display device is provided in the display area 3203. Each pixel of the display area 3203 includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a computer with less characteristic deterioration can be obtained.

[0186]

FIG. 15D shows a mobile computer, including a main body 3301, a display area 3302, a switch 3303, operation keys 3304, an infrared port 3305, and the like. An active matrix display device is provided in the display area 3302. Each pixel of the display area 3302 includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a mobile computer with less

characteristic deterioration can be obtained.

[0187]

FIG. 15E shows a portable game machine, including a housing 3401, a display area 3402, speakers 3403, operation keys 3404, a recording medium insert portion 3405, and the like. An active matrix display device is provided in the display area 3402. Each pixel of the display area 3402 includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a portable game machine with less characteristic deterioration can be obtained.

[0188]

FIG. 16 shows a flexible display, including a main body 3110, a pixel area 3111, a driver IC 3112, a receiving device 3113, a film buttery 3114, and the like. The receiving device can receive a signal from an infrared communication port 3107 of the above described cellular phone. An active matrix display device is provided in the pixel area 3111. Each pixel of the pixel area 3111 includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a flexible display with less characteristic deterioration can be obtained.

[0189]

As set forth above, the application range of this invention is extremely wide, and this invention can be applied to electronic devices in all fields.

[0190]

The present application is based on Japanese Patent Application serial No. 2005-329806 filed on November 15, 2005 in Japanese Patent Office, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

a gate electrode;

a gate insulating film over the gate electrode;

a first film comprising metal material over the gate insulating film;

a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the first film; and

a third film comprising the transparent semiconductor material over the second film and the gate insulating film.

2. A semiconductor device according to claim 1, wherein the gate insulating film comprises silicon oxide or silicon oxynitride.

3. A semiconductor device according to claim 1, wherein the metal material is aluminum or aluminum alloy.

4. A semiconductor device according to claim 1, wherein the transparent semiconductor material is zinc oxide.

5. A semiconductor device comprising:

an insulating film over a substrate;

a first film comprising a metal material over the insulating film;

a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the metal film;

a third film comprising the transparent semiconductor material over the insulating film and the second film;

a gate insulating film over the third film; and

a gate electrode over the gate insulating film.

6. A semiconductor device according to claim 5, wherein the insulating film comprises silicon oxide or silicon oxynitride.

7. A semiconductor device according to claim 5, wherein the metal material is aluminum or aluminum alloy.

8. A semiconductor device according to claim 5, wherein the transparent semiconductor material is zinc oxide.

9. A manufacturing method of a semiconductor device, comprising:

forming an insulating film over a substrate;

forming a first film comprising a metal material over the insulating film;

forming a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the first film,

etching the second film, and

etching the first film.

10. A manufacturing method of a semiconductor device according to Claim 9, further comprising forming a third film comprising the transparent semiconductor material over the second film and the insulating film after the step of etching the first film.

11. A manufacturing method of a semiconductor device according to claim 9, wherein the insulating film comprises silicon oxide or silicon oxynitride.

12. A manufacturing method of a semiconductor device according to claim 9, wherein the metal material is aluminum or aluminum alloy.

13. A manufacturing method of a semiconductor device according to claim 9, wherein the transparent semiconductor material is zinc oxide.

14. A manufacturing method of the semiconductor device according to claim 9, wherein the substrate is a glass substrate.

15. A manufacturing method of the semiconductor device according to claim 10, wherein the transparent semiconductor material is zinc oxide.

16. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the second film is wet etching.

17. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the second film is wet etching using a buffered fluoric acid.

18. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the second film is performed by dry etching.

19. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the second film is performed by dry etching using CH_4 gas.

20. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the first film is performed by wet etching.

21. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the first film is performed by wet etching using a developer for a photoresist.

22. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the first film is performed by wet etching using an organic alkali solution.

23. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the first film is performed by wet etching using TMAH (tetramethylammonium hydroxide).

24. A manufacturing method of a semiconductor device, comprising:

forming a gate electrode over a substrate;

forming a gate insulating film over the gate electrode;

forming a first film comprising a metal material over the gate insulating film;

forming a second film comprising a transparent semiconductor material and an n-type or p-type impurity over second film,

etching the second film, and

etching the first film.

25. A manufacturing method of the semiconductor device according to Claim 24, further comprising forming a third film comprising the transparent semiconductor material over the second film and the gate insulating film after the step of etching the first film.

26. A manufacturing method of the semiconductor device according to claim 24, wherein the gate insulating film comprises silicon oxide or silicon oxynitride.

27. A manufacturing method of the semiconductor device according to claim 24, wherein the metal material is aluminum or aluminum alloy.

28. A manufacturing method of the semiconductor device according to claim 24, wherein the transparent semiconductor material is zinc oxide.

29. A manufacturing method of the semiconductor device according to claim 24, wherein the substrate is a glass substrate.

30. A manufacturing method of the semiconductor device according to claim 25, wherein the transparent semiconductor material is zinc oxide.

31. A manufacturing method of the semiconductor device according to Claim 25, further

comprising:

forming a gate insulating film over the third film, and

forming a gate electrode over the gate insulating film.

32. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the second film is performed by wet etching.

33. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the second film is performed by wet etching using a buffered fluoric acid.

34. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the second film is performed by dry etching using CH_4 gas.

35. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the first film is performed by wet etching.

36. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the first film is performed by wet etching using a developer for a photoresist.

37. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the first film is performed by wet etching using an organic alkali solution.

38. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the first film is performed by wet etching using TMAH (tetramethylammonium hydroxide).

FIG. 1A

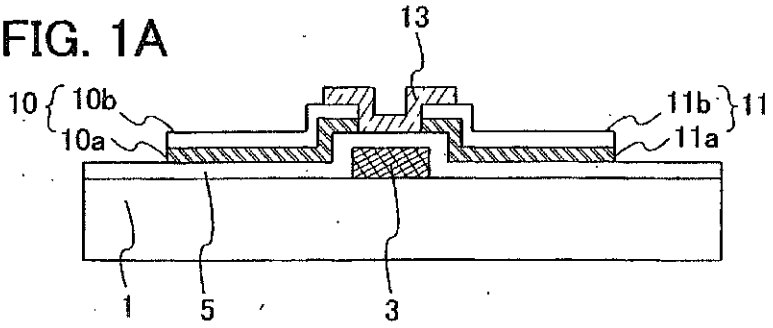

FIG. 1B

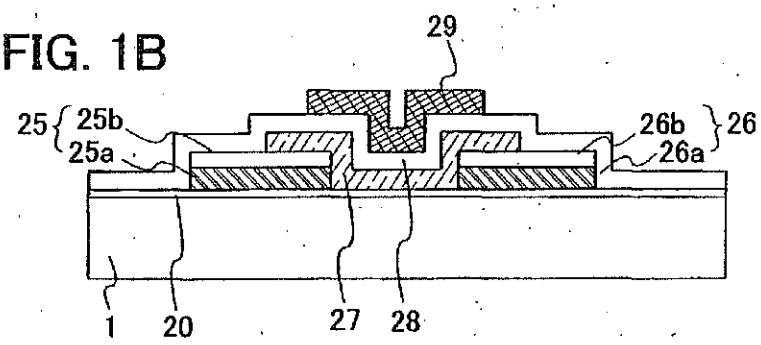

FIG. 2A

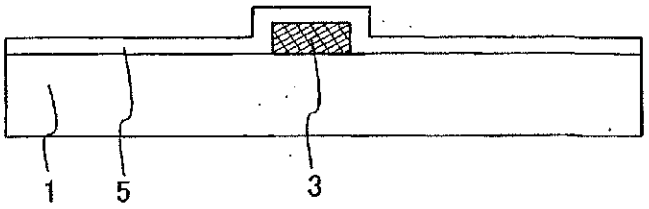

FIG. 2B

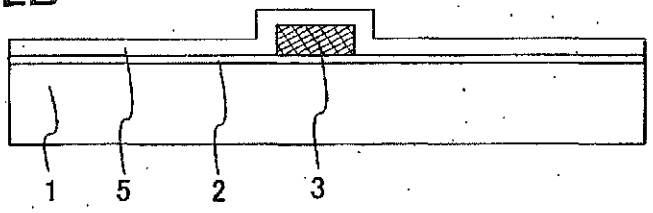

FIG. 2C

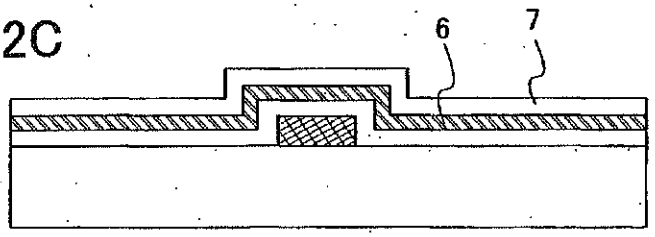

FIG. 2D

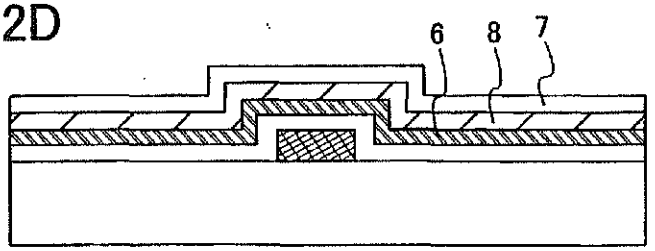

FIG. 3A

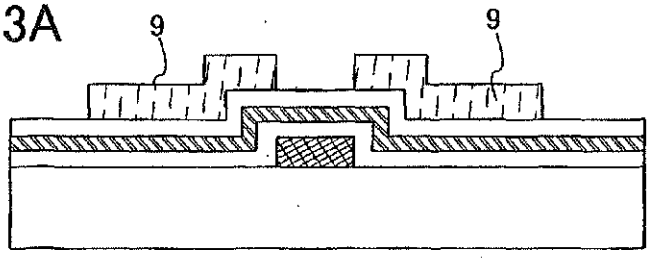

FIG. 3B

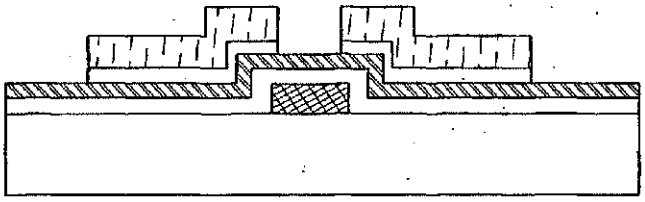

FIG. 3C

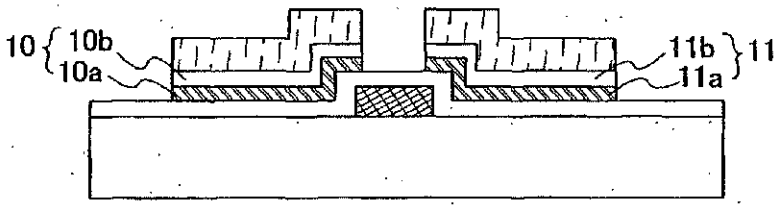

FIG. 3D

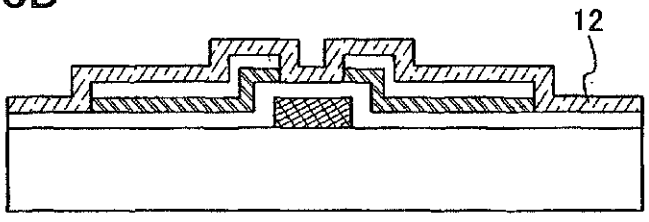

FIG. 4A

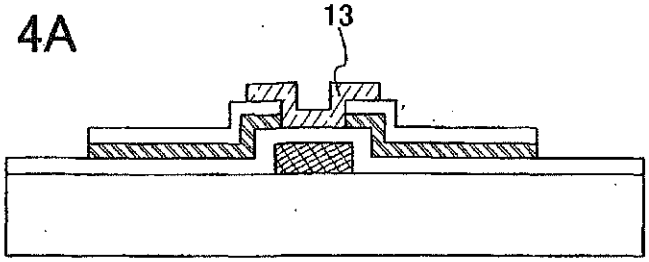

FIG. 4B

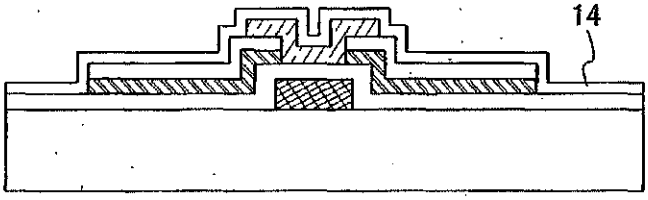

FIG. 5A

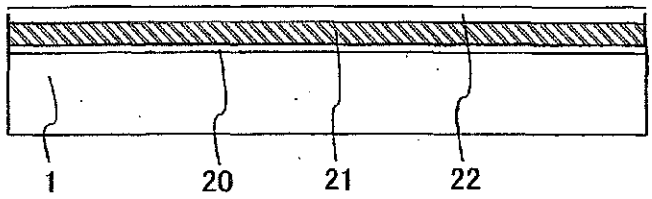

FIG. 5B

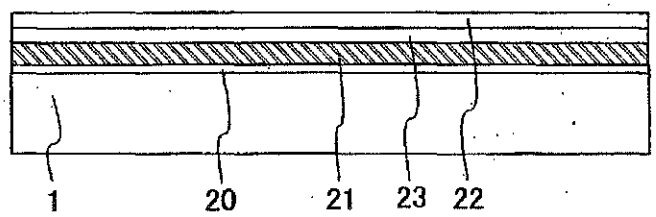

FIG. 5C

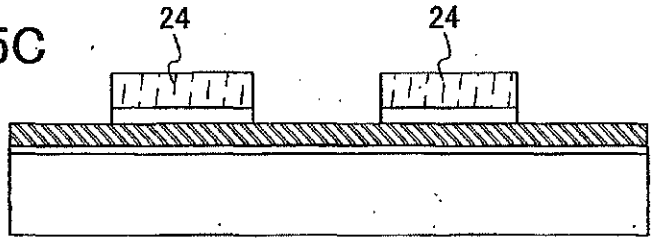

FIG. 5D

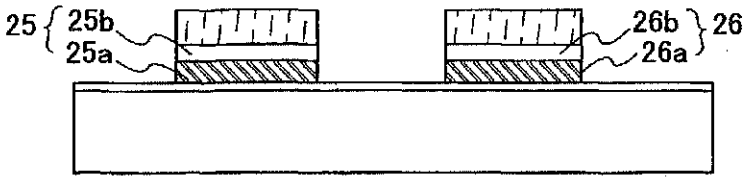

FIG. 6A

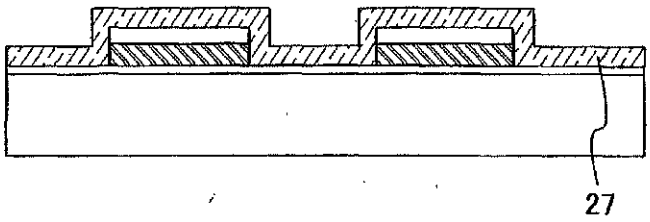

FIG. 6B

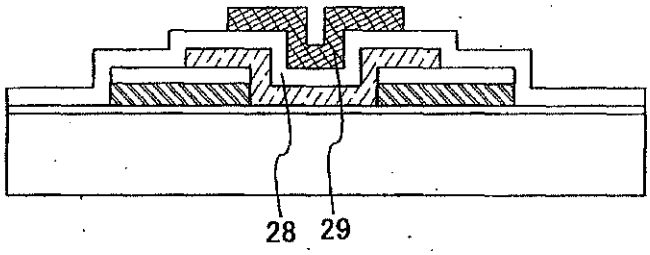

FIG. 6C

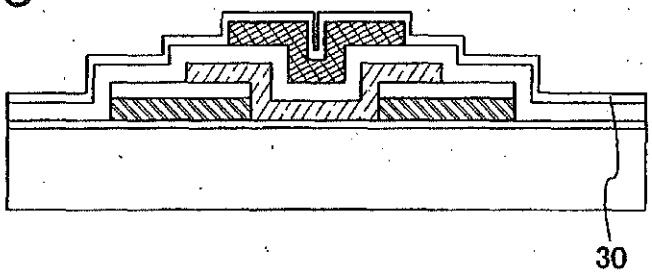

FIG. 7A

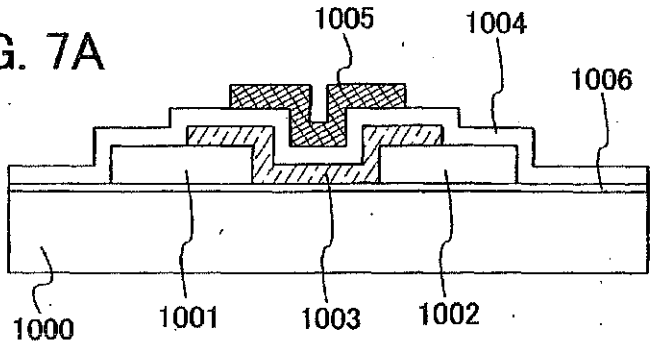
1005
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FIG. 7B

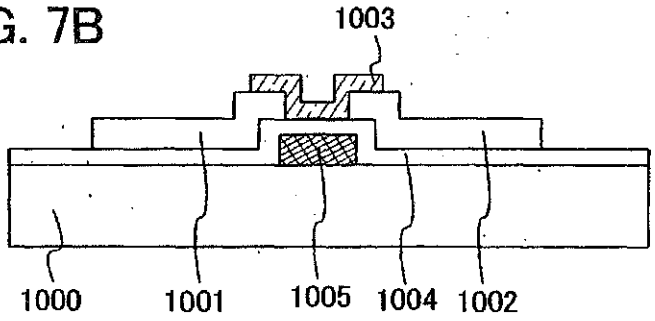
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FIG. 8A

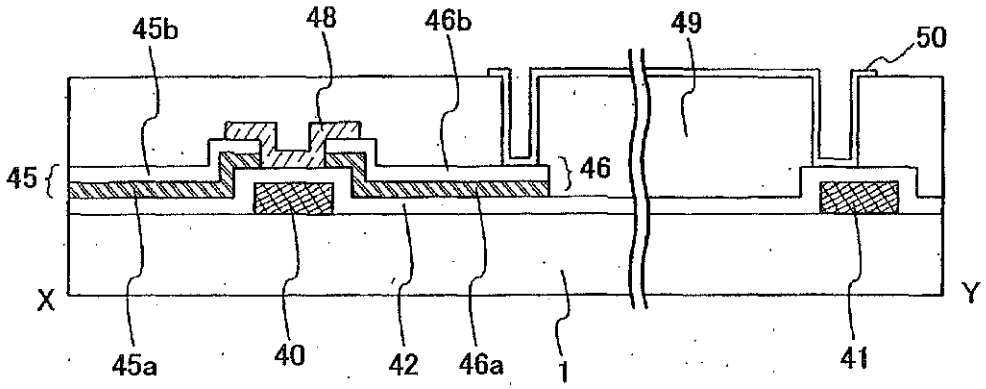


FIG. 8B

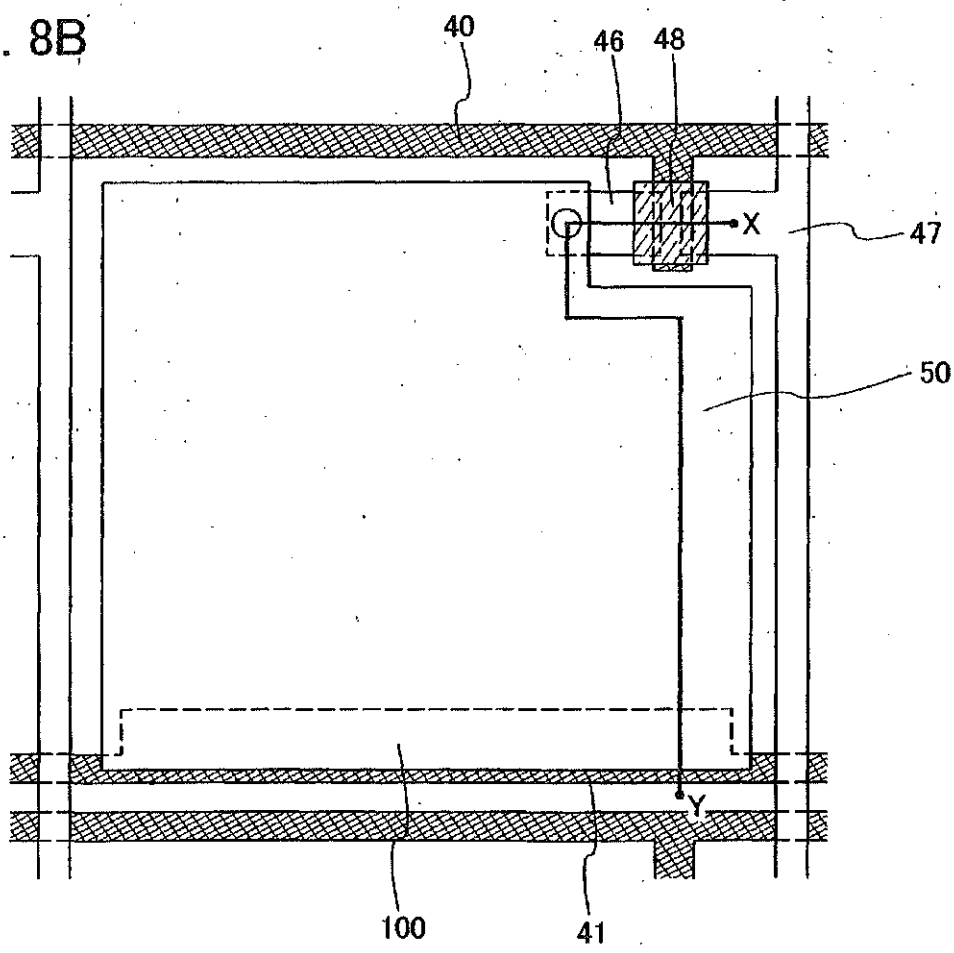
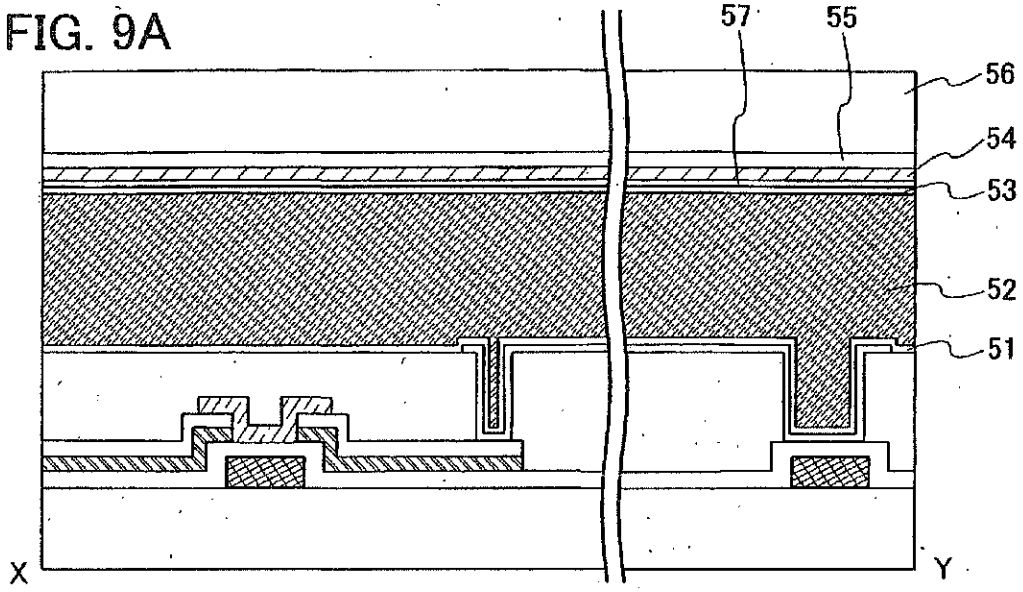


FIG. 9A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X
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FIG. 9B

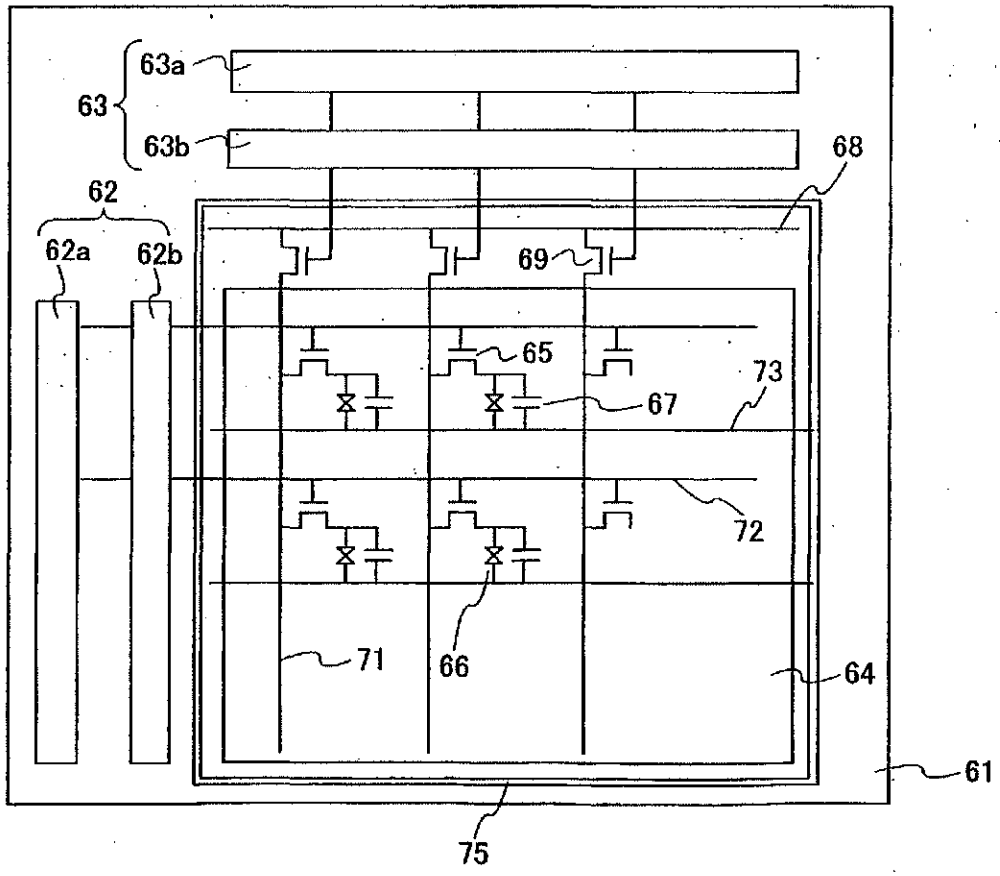
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FIG. 10A

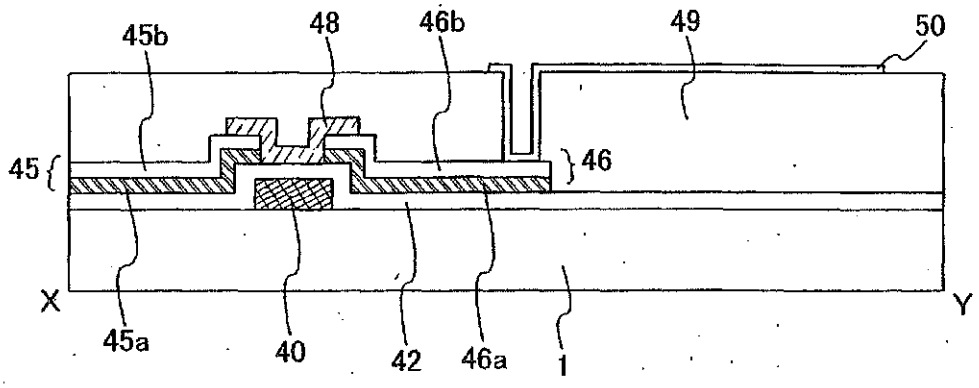

FIG. 10B

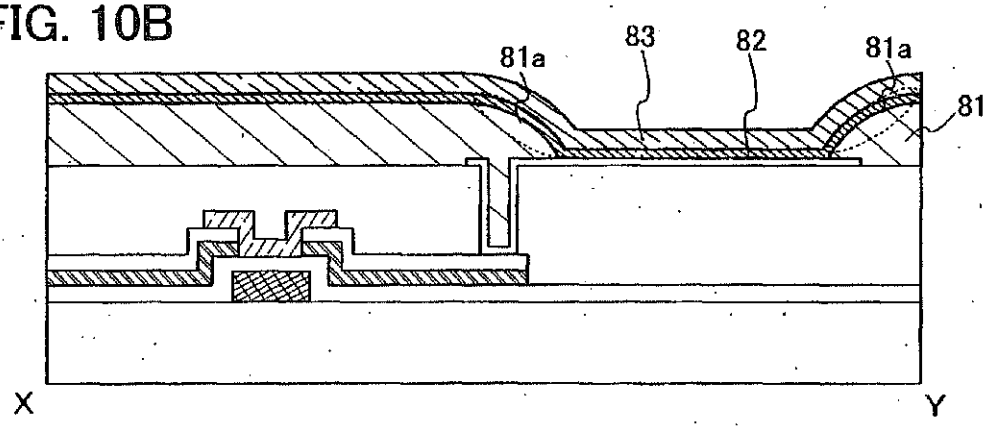

FIG. 11A

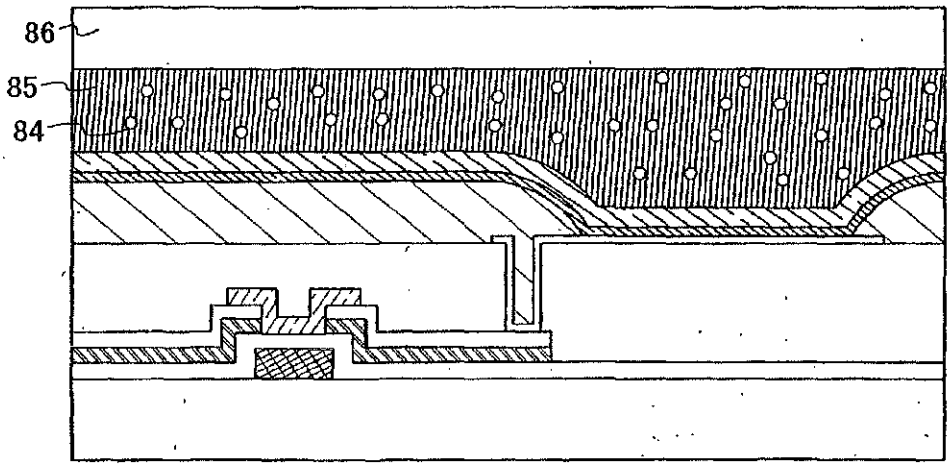

FIG. 11B

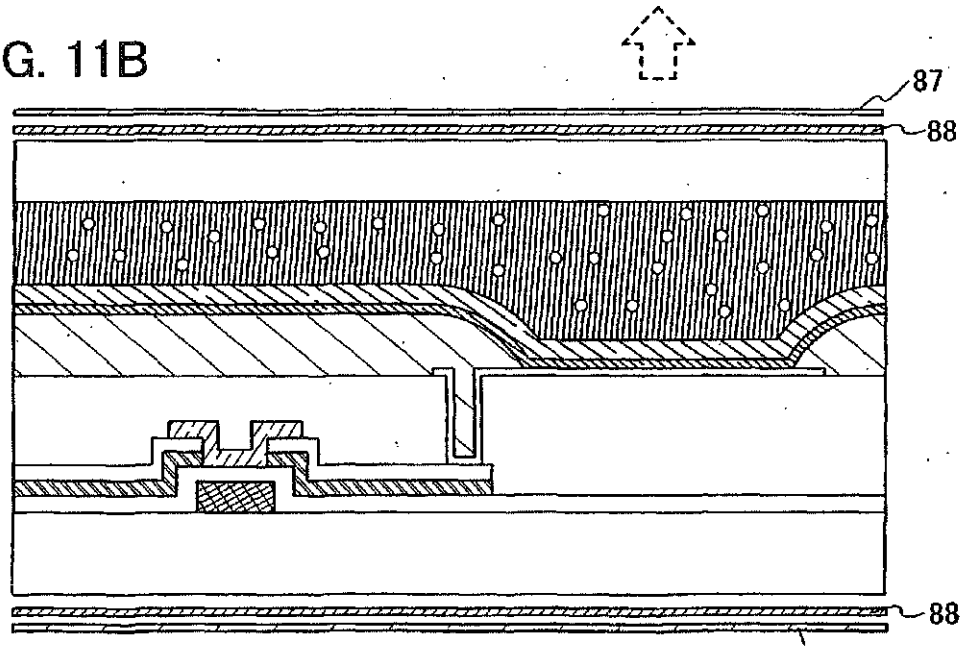

FIG. 12A

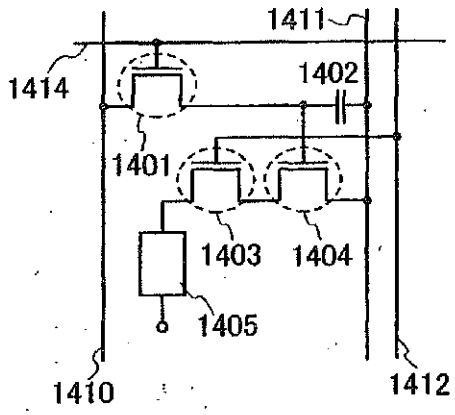

FIG. 12B

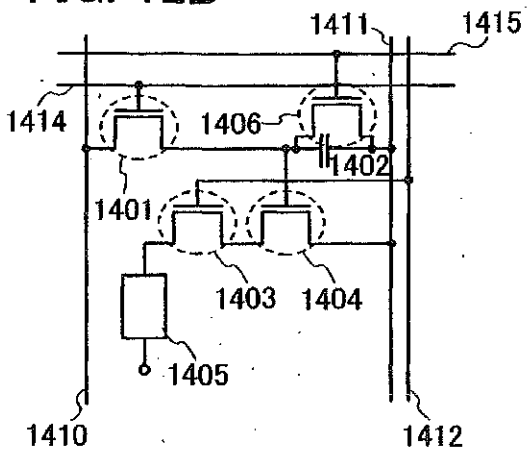

FIG. 12C

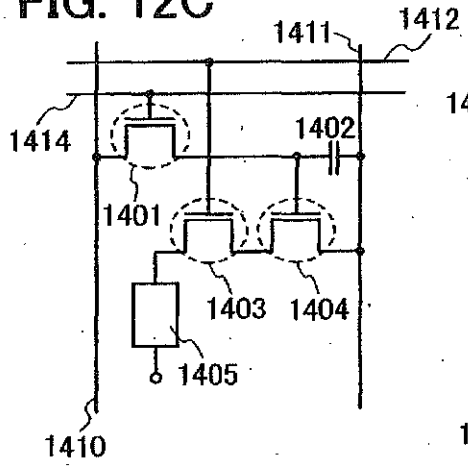

FIG. 12D

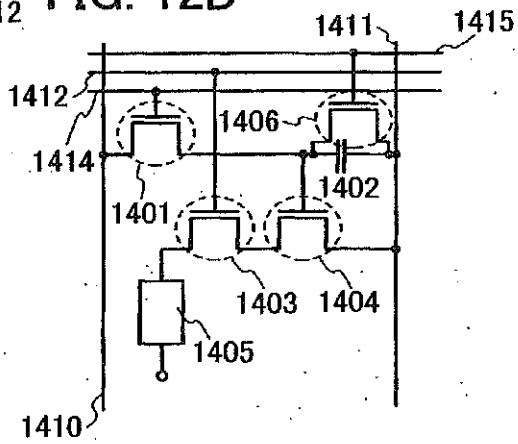

FIG. 12E

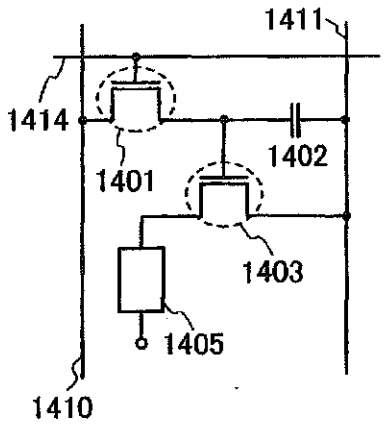

FIG. 12F

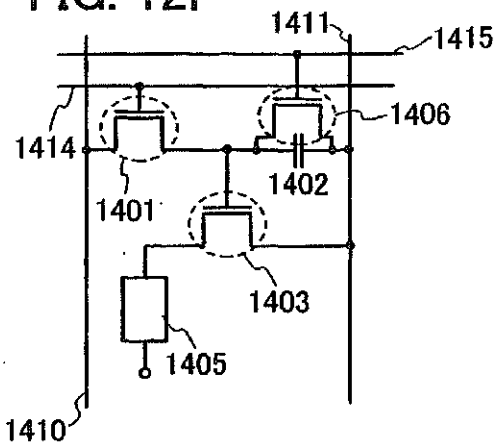

FIG. 13

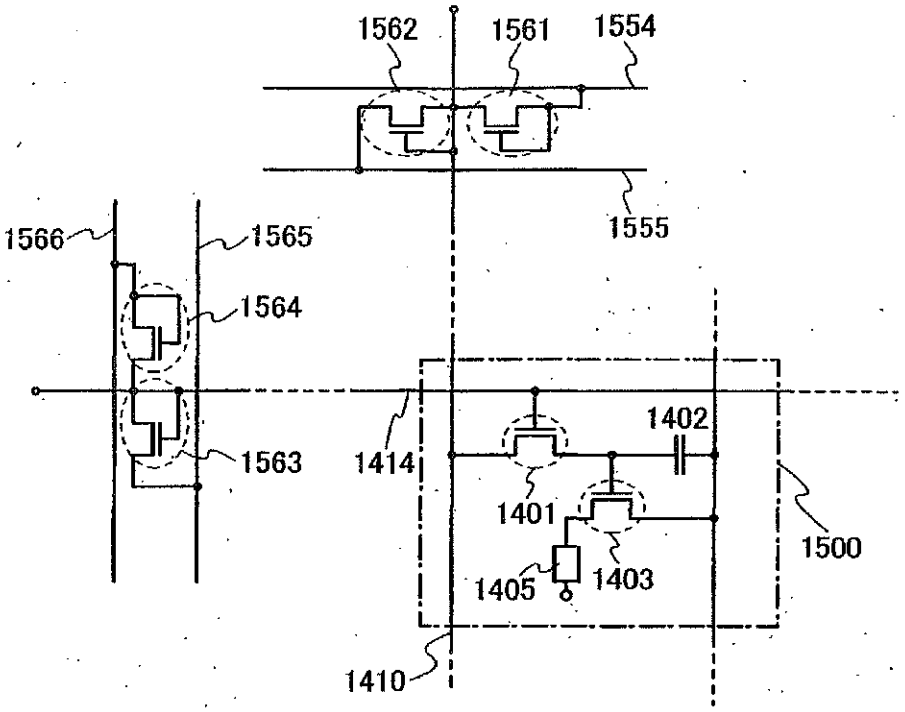
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FIG. 14A

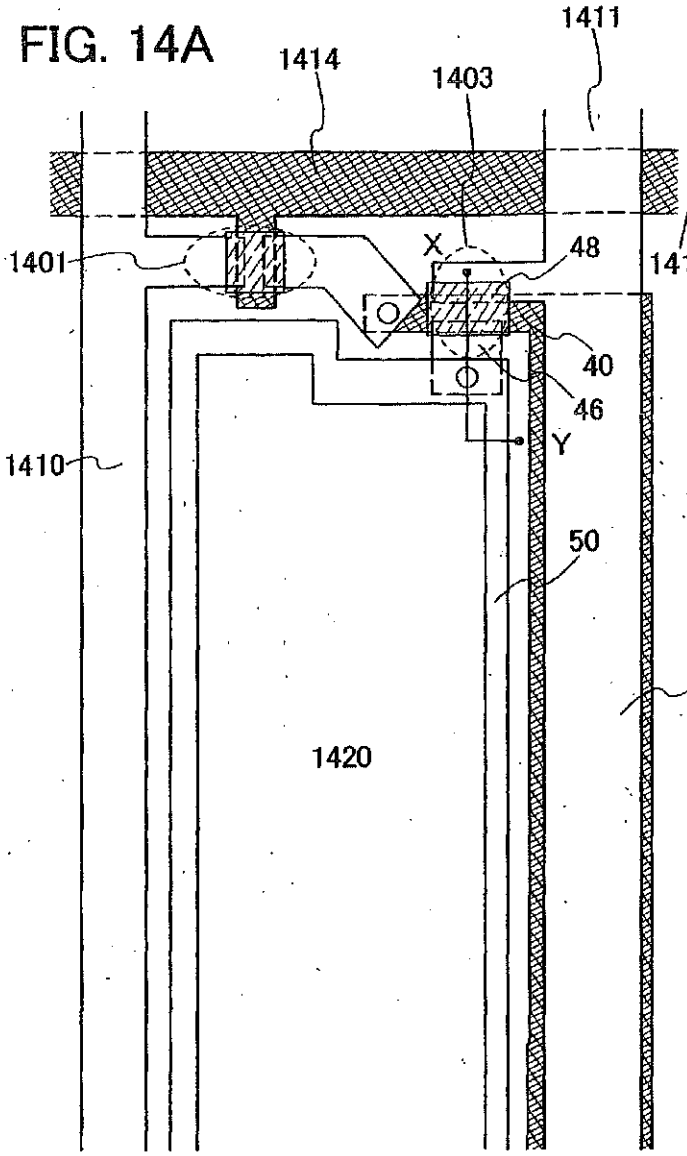


FIG. 14B

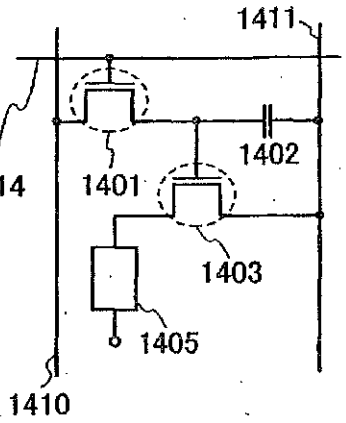


FIG. 15A

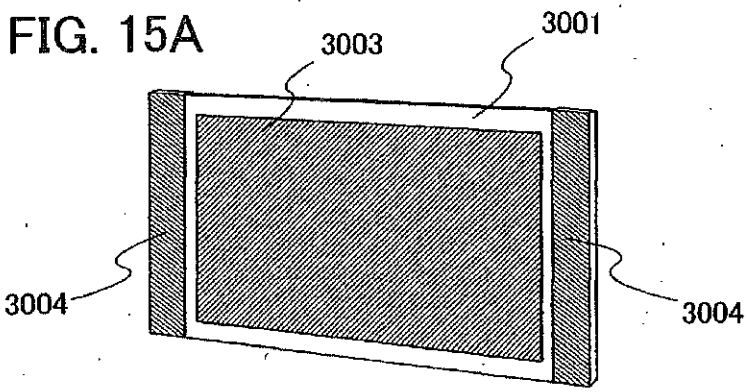


FIG. 15B

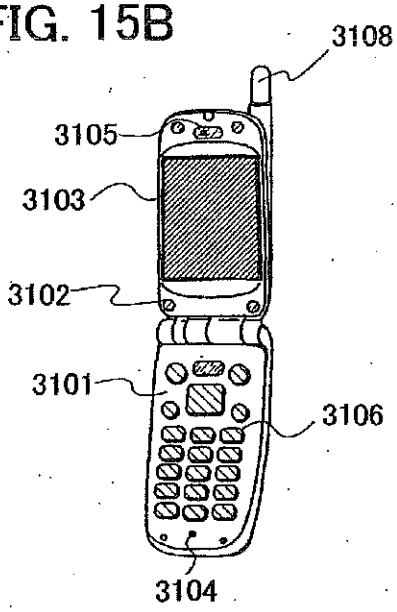


FIG. 15C

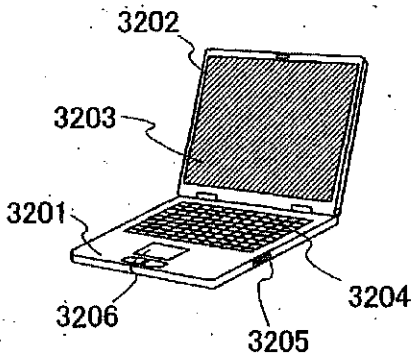


FIG. 15D

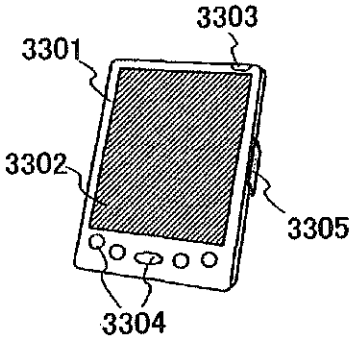


FIG. 15E

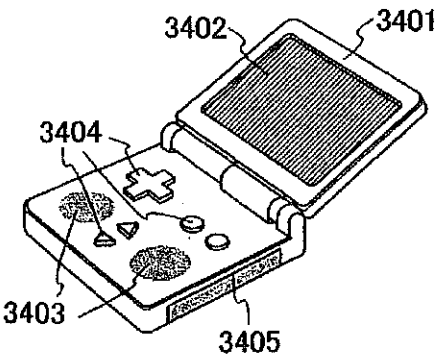
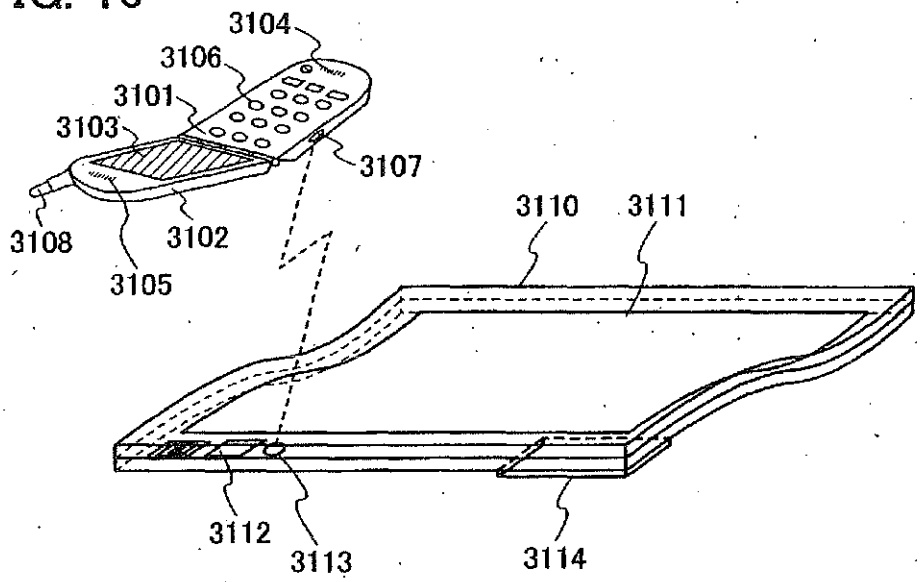


FIG. 16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EXPLANATION OF REFERENCE

1: substrate, 2: insulating film, 3: gate electrode, 5: gate insulating film, 6: first conductive film, 7: second conductive film, 8: third conductive film, 9: resist mask, 10: source electrode, 10a: source electrode, first conductive film, 10b: source electrode, second conductive film, 11: drain electrode, 11a: drain electrode, first conductive film, 11b: drain electrode, second conductive film, 12: semiconductor film, 13: island-like shaped semiconductor film, 14: insulating film, 20: insulating film, 21: first conductive film, 22: second conductive film, 23: third conductive film, 24: resist mask, 25: source electrode, 25a: source electrode, first conductive film, 25b: source electrode, second conductive film, 26: drain electrode, 26a: drain electrode, first conductive film, 26b: drain electrode, second conductive film, 27: semiconductor film, 28: gate insulating film, 29: gate electrode, 30: insulting film, 40: gate electrode, gate wire, 41: auxiliary capacitor wire, 42: gate insulating film, 45: source electrode, 45a: source electrode, 45b: source electrode, 46: drain electrode, 46a: drain electrode, 46b: drain electrode, 47: source wire, 48: semiconductor film, 49: insulating film, 50: pixel electrode, 51: alignment wire, 52: liquid crystal composition, 53: alignment film, 54: protective insulating film, 55: color filter, 56: opposing substrate, 61: substrate, 62: gate wire driver circuit, 62a: shift register, 62b: buffer, 63: source wire driver circuit, 63a: shift register, 63b: buffer, 64: active matrix portion, 65: semiconductor device, 66: liquid crystal portion, 67: auxiliary capacitor, 68: video line, 69: analog switch, 71: source wire, 72: gate wire, 73: auxiliary capacitor wire, 75: sealant, 81: partition wall, 81a: end surface, 82: layer including light-emitting substance, 83: opposing electrode, 84: drying agent, 85: resin, 86: opposing substrate, 87: protective film, 88: polarizing plate, 100: auxiliary capacitor, 1000: substrate, 1001: source electrode, 1002: drain electrode, 1003: semiconductor film, 1004: gate insulating film, 1005: gate electrode, 1006: base film, 1401: switching TFT, 1402: auxiliary capacitor, 1403: driving TFT, 1404: current control TFT, 1405: light-emitting element, 1406: TFT, 1410: signal line, 1411: power source line, 1412: power source line, 1414: scan line, 1415: scan line, 1420: light-emitting region, 1500: pixel portion, 1554: common potential line, 1555: common potential line, 1561: diode, 1562: diode, 1563: diode, 1564: diode, 1565: common potential line, 1566: common potential line, 3001: housing, 3003: display area, 3004: speaker,

3101: main body, 3102: housing, 3102: housing, 3103: display area, 3104: audio input portion, 3105: audio output portion, 3106: operation keys, 3107: infrared communication port, 3108: antenna, 3110: main body, 3111: pixel portion, 3112: driver IC, 3113: receiving device, 3114: film buttery, 3201: main body, 3202: housing, 3203: display area, 3204: keyboard, 3205: external connection port, 3206: pointing mouse, 3301: main body, 3302: display area, 3303: switch, 3304: operation keys, 3305: infrared port, 3401: housing, 3402: display area, 3403: speakers, 3404: operation keys, 3405: recording medium insert portion

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2006/323042

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L21/336(2006.01)i, G02F1/1368(2006.01)i, H01L21/28(2006.01)i, H01L29/786(2006.01)i, H01L51/50(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L21/336, G02F1/1368, H01L21/28, H01L29/786, H01L51/50

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2007
Registered utility model specifications of Japan 1996-2007
Published registered utility model applications of Japan 1994-2007

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 02-226729 A (SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.) 1990.09.10, Fig.4 (Family: none)	1-2

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13.02.2007	27.02.2007

Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	KAZUNARI TANADA 4L 9361 Telephone No. +81-3-3581-1101 Ext. 3498

Form PCT/ISA/210 (second sheet) (April 2005)

The "special technical feature" of claims 1-38 relates to "a gate electrode; a gate insulating film over the gate electrode; a first film comprising metal material over the gate insulating film; a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the first film; and a third film comprising the transparent semiconductor material over the second film and the gate insulating film". However, this feature is disclosed in a prior art document JP 02-226729 A(SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.), 1990.09.10., Fig.4. So the feature cannot be a special technical feature. And there exists no special technical feature linking the inventions of claims 1-38 as to form a single general inventive concept among the inventions.

Therefore there is no technical relationship which is considered as "special technical feature"(PCT rule 13.2) among the claims 1-38. So this application contains the following groups of invention which are not so linked as to form a single inventive concept under PCT rule 13.2.

Group 1:Claims 1-2
Group 2:Claim 3
Group 3:Claim 4
Group 4:Claims 5-6
Group 5:Claim 7
Group 6:Claim 8
Group 7:Claims 9-10,15
Group 8:Claim 11
Group 9:Claim 12
Group 10:Claim 13
Group 11:Claim 14
Group 12:Claim 16
Group 13:Claim 17
Group 14:Claim 18
Group 15:Claim 19
Group 16:Claim 20
Group 17:Claim 21
Group 18:Claim 22
Group 19:Claim 23
Group 20:Claims 24-25,30
Group 21:Claim 26
Group 22:Claim 27
Group 23:Claim 28
Group 24:Claim 29
Group 25:Claim 31
Group 26:Claim 32
Group 27:Claim 33
Group 28:Claim 34
Group 29:Claim 35
Group 30:Claim 36
Group 31:Claim 37
Group 32:Claim 38

INTERNATIONALSEARCHREPORT

International application No.
PCT/JP2006/323042

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
Refer to extra sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☑ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-2

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☐ No protest accompanied the payment of additional search fees.

No documents available for this priority number.

Espacenet

Bibliographic data: CN101283444 (A) — 2008-10-08

Semiconductor device and method of manufacturing the same

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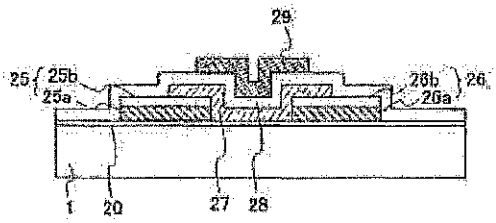
Abstract of CN101283444 (A)



To provide a semiconductor device in which a defect or fault is not generated and a manufacturing method thereof even if a ZnO semiconductor film is used and a ZnO film to which an n-type or p-type impurity is added is used for a source electrode and a drain electrode. The semiconductor device includes a gate insulating film formed by using a silicon oxide film or a silicon oxynitride film over a gate electrode, an Al film or an Al alloy film over the gate insulating film, a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film, and a ZnO semiconductor film over the ZnO film to which an n-type or p-type impurity is added and the gate insulating film.

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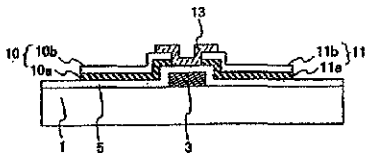
权利要求书 4 页 说明书 29 页 附图 18 页

[54] 发明名称

半导体器件及其制造方法

[57] 摘要

本发明提供一种半导体器件及其制造方法，即使使用 ZnO 半导体膜，并且对于源电极和漏电极使用其中添加 n 型或 p 型杂质的 ZnO 膜也不会产生缺陷或故障。该半导体器件包含：通过使用氧化硅膜或氧氮化硅膜在栅电极之上形成的栅绝缘膜、在栅绝缘膜之上的 Al 膜或 Al 合金膜、在 Al 膜或 Al 合金膜之上的其中添加 n 型或 p 型杂质的 ZnO 膜、以及在其中添加 n 型或 p 型杂质的 ZnO 膜和栅绝缘膜之上的 ZnO 半导体膜。



1. 一种半导体器件，包括:

栅电极;

在所述栅电极之上的栅绝缘膜;

在所述栅绝缘膜之上的包含金属材料的第一膜;

在所述第一膜之上的包含透明半导体材料和n型或p型杂质的第二膜; 和

在所述第二膜和所述栅绝缘膜之上的包含所述透明半导体材料的第三膜。

2. 根据权利要求1的半导体器件，其中，所述栅绝缘膜包含氧化硅或氧氮化硅。

3. 根据权利要求1的半导体器件，其中，所述金属材料是铝或铝合金。

4. 根据权利要求1的半导体器件，其中，所述透明半导体材料是氧化锌。

5. 一种半导体器件，包括:

在衬底之上的绝缘膜;

在所述绝缘膜之上的包含金属材料的第一膜;

在所述金属膜之上的包含透明半导体材料和n型或p型杂质的第二膜;

在所述绝缘膜和所述第二膜之上的包含所述透明半导体材料的第三膜;

在所述第三膜之上的栅绝缘膜; 和

在所述栅绝缘膜之上的栅电极。

6. 根据权利要求5的半导体器件，其中，所述绝缘膜包含氧化硅或氧氮化硅。

7. 根据权利要求5的半导体器件，其中，所述金属材料是铝或铝合金。

8. 根据权利要求5的半导体器件，其中，所述透明半导体材料是氧化锌。

9. 一种半导体器件的制造方法，包括以下步骤：

在衬底之上形成绝缘膜；

在所述绝缘膜之上形成包含金属材料的第一膜；

在所述第一膜之上形成包含透明半导体材料和n型或p型杂质的第二膜；

蚀刻所述第二膜；和

蚀刻所述第一膜。

10. 根据权利要求9的半导体器件的制造方法，还包括在蚀刻所述第一膜的步骤之后在所述第二膜和所述绝缘膜之上形成包含所述透明半导体材料的第三膜。

11. 根据权利要求9的半导体器件的制造方法，其中，所述绝缘膜包含氧化硅或氧氮化硅。

12. 根据权利要求9的半导体器件的制造方法，其中，所述金属材料是铝或铝合金。

13. 根据权利要求9的半导体器件的制造方法，其中，所述透明半导体材料是氧化锌。

14. 根据权利要求9的半导体器件的制造方法，其中，所述衬底是玻璃衬底。

15. 根据权利要求10的半导体器件的制造方法，其中，所述透明半导体材料是氧化锌。

16. 根据权利要求9的半导体器件的制造方法，其中，所述第二膜的所述蚀刻是湿蚀刻。

17. 根据权利要求9的半导体器件的制造方法，其中，所述第二膜的所述蚀刻是使用缓冲的氢氟酸的湿蚀刻。

18. 根据权利要求9的半导体器件的制造方法，其中，通过干蚀刻进行所述第二膜的所述蚀刻。

19. 根据权利要求9的半导体器件的制造方法，其中，通过使用

CH_4气体的干蚀刻进行所述第二膜的所述蚀刻。

20. 根据权利要求9的半导体器件的制造方法，其中，通过湿蚀刻进行所述第一膜的所述蚀刻。

21. 根据权利要求9的半导体器件的制造方法，其中，通过使用用于光刻胶的显影剂的湿蚀刻进行所述第一膜的所述蚀刻。

22. 根据权利要求9的半导体器件的制造方法，其中，通过使用有机碱溶液的湿蚀刻进行所述第一膜的所述蚀刻。

23. 根据权利要求9的半导体器件的制造方法，其中，通过使用TMAH（四甲基氢氧化铵）的湿蚀刻进行所述第一膜的所述蚀刻。

24. 一种半导体器件的制造方法，包括以下步骤：

在衬底之上形成栅电极；

在所述栅电极之上形成栅绝缘膜；

在所述栅绝缘膜之上形成包含金属材料的第一膜；

在所述第二膜之上形成包含透明半导体材料和n型或p型杂质的第二膜；

蚀刻所述第二膜；和

蚀刻所述第一膜。

25. 根据权利要求24的半导体器件的制造方法，还包括在蚀刻所述第一膜的步骤之后在所述第二膜和所述栅绝缘膜之上形成包含所述透明半导体材料的第三膜。

26. 根据权利要求24的半导体器件的制造方法，其中，所述栅绝缘膜包含氧化硅或氧氮化硅。

27. 根据权利要求24的半导体器件的制造方法，其中，所述金属材料是铝或铝合金。

28. 根据权利要求24的半导体器件的制造方法，其中，所述透明半导体材料是氧化锌。

29. 根据权利要求24的半导体器件的制造方法，其中，所述衬底是玻璃衬底。

30. 根据权利要求25的半导体器件的制造方法，其中，所述透明

半导体材料是氧化锌。

31. 根据权利要求25的半导体器件的制造方法，还包括以下步骤：

在所述第三膜之上形成栅绝缘膜；和

在所述栅绝缘膜之上形成栅电极。

32. 根据权利要求24的半导体器件的制造方法，其中，通过湿蚀刻进行所述第二膜的所述蚀刻。

33. 根据权利要求24的半导体器件的制造方法，其中，通过使用缓冲的氢氟酸的湿蚀刻进行所述第二膜的所述蚀刻。

34. 根据权利要求24的半导体器件的制造方法，其中，通过使用CH_4气体的干蚀刻进行所述第二膜的所述蚀刻。

35. 根据权利要求24的半导体器件的制造方法，其中，通过湿蚀刻进行所述第一膜的所述蚀刻。

36. 根据权利要求24的半导体器件的制造方法，其中，通过使用用于光刻胶的显影剂的湿蚀刻进行所述第一膜的所述蚀刻。

37. 根据权利要求24的半导体器件的制造方法，其中，通过使用有机碱溶液的湿蚀刻进行所述第一膜的所述蚀刻。

38. 根据权利要求24的半导体器件的制造方法，其中，通过使用TMAH（四甲基氢氧化铵）的湿蚀刻进行所述第一膜的所述蚀刻。

半导体器件及其制造方法

技术领域

本发明涉及使用ZnO（氧化锌）的半导体器件及其制造方法。

背景技术

一般通过使用a-Si（非晶硅）或poly-Si（多晶硅）形成用于液晶显示器或EL（电致发光）显示器的显示面板的半导体器件，例如TFT（薄膜晶体管）的半导体部分半导体器件。

Si（硅）不具有大的带隙（例如，单晶硅为1.1eV）并且吸收可见光。通过用光照射，在Si中形成电子和空穴（载流子）。如果形成Si膜用于TFF的沟道形成区域，那么即使在OFF状态下也会通过用光照射在沟道形成区域中产生载流子。于是，电流从而在源极区和漏极区之间流动。在OFF状态中流动的电流被称为"OFF泄漏电流"。如果电流值较高，那么显示面板不正常工作。因此，形成光屏蔽膜以使得光不照射Si膜。但是，由于需要淀积步骤、光刻步骤和蚀刻步骤，因此，当形成光屏蔽膜时，工艺变得复杂。

为了解决该问题，关注使用氧化锌（ZnO）的透明晶体管，该氧化锌是具有比Si的带隙大的3.4eV的较大的带隙的半导体。关于这种透明晶体管，带隙比可见光带中的光能大，并且可见光不被吸收。因此，它具有在用光照射时OFF泄漏电流不增加的优点。

例如，在对比文件1中公开了对于沟道形成区域使用ZnO的半导体器件。参照图7A说明使用ZnO的半导体器件的结构。

图7A中的半导体器件在诸如玻璃衬底的绝缘衬底1000之上具有源电极1001、漏电极1002、被配置为与源电极1001和漏电极1002接触的ZnO层1003、层叠在ZnO层1003之上的栅绝缘层1004和栅电极1005。

对于源电极1001和漏电极1002，使用导电的ZnO。导电的ZnO掺

杂有以下的元素中的一种：作为第III族元素的B（硼）、Al（铝）、镓（Ga）、铟（In）或Tl（铊）；作为第VII族元素的F（氟）、Cl（氯）、Br（溴）或I（碘）；作为第I族元素的锂（Li）、Na（钠）、K（钾）、Rb（铷）或Cs（铯）；作为第V族元素的N（氮）、P（磷）、As（砷）、Sb（锑）或Bi（铋）。

[参考文件] 日本公开专利申请No. 2000-150900

发明内容

根据本发明的发明人的试验，揭示了当通过蚀刻形成图7A所示的顶栅半导体器件的源电极1001和漏电极1002时衬底1000在一些情况下被蚀刻。即使在形成通过在衬底1000上使用氧化硅膜或氧氮化硅膜形成的基膜1006的情况下，当基膜被蚀刻时衬底1000的表面也在一些情况下被露出。另外，在图7B所示的底栅半导体器件的情况下，揭示了当通过蚀刻形成源电极1001和漏电极1002时通过使用氧化硅膜或氧氮化硅膜形成的栅绝缘膜1004被蚀刻。

在顶栅半导体器件的情况下，当玻璃衬底1000或通过使用氧化硅膜或氧氮化硅膜形成的基膜1006被蚀刻时，诸如钠的杂质从衬底1000扩散到半导体膜1003中，使得特性劣化。

在底栅半导体器件（图7B）的情况下，如果当通过蚀刻形成源电极1001和漏电极1002时栅绝缘膜1004被蚀刻，那么特性是不稳定的并且导致故障。

考虑到以上情况，本发明的目的是，提供即使对沟道形成区域使用ZnO半导体膜并且对于源电极和漏电极使用其中添加n型或p型杂质的ZnO膜也不产生缺陷或故障的半导体器件及其制造方法。

本发明的半导体器件的一个方面具有：在氧化硅膜或氧氮化硅膜之上的Al膜或Al合金膜和在Al膜或Al合金膜之上的其中添加n型或p型杂质的ZnO膜。本说明书中的“氧化硅膜”、“氧氮化硅膜”、“Al膜”、“Al合金膜”和“ZnO膜”分别意味着包含氧化硅的膜、包含氧氮化硅的膜、包含Al的膜、包含Al合金的膜和包含ZnO的膜。

本发明的半导体器件的一个方面具有：在栅电极之上的通过使用氧化硅膜或氧氮化硅膜形成的栅绝缘膜、在栅绝缘膜之上的Al膜或Al合金膜、在Al膜或Al合金膜之上的其中添加n型或p型杂质的ZnO膜、以及在其中添加n型或p型杂质的ZnO膜和栅绝缘膜之上的ZnO半导体膜。

本发明的半导体器件的一个方面具有：在氧化硅膜或氧氮化硅膜之上的Al膜或Al合金膜、在Al膜或Al合金膜之上的其中添加n型或p型杂质的ZnO膜、在氧化硅膜或氧氮化硅膜和其中添加n型或p型杂质的ZnO膜之上的ZnO半导体膜、在ZnO半导体膜之上的栅绝缘膜、和在栅绝缘膜之上的栅电极。

本发明的半导体器件的制造方法的一个方面具有以下步骤：形成氧化硅膜或氧氮化硅膜；在氧化硅膜或氧氮化硅膜之上形成Al膜或Al合金膜；在Al膜或Al合金膜之上形成其中添加n型或p型杂质的ZnO膜，其中，其中添加n型或p型杂质的ZnO膜通过第一蚀刻被蚀刻为具有岛状形状，并且Al膜或Al合金膜通过第二蚀刻被蚀刻为具有岛状形状。

本发明的半导体器件的制造方法的一个方面，其中，在第二蚀刻之后，在其中添加n型或p型杂质的ZnO膜、和氧化硅膜或氧氮化硅膜之上形成ZnO半导体膜。

在底栅半导体器件的情况下，在形成栅电极之后，在栅电极之上形成通过使用氧化硅膜或氧氮化硅膜形成的栅绝缘膜。

在顶栅半导体器件的情况下，在形成ZnO半导体膜之后形成栅绝缘膜并且形成栅电极。

本发明的第一蚀刻可以是湿蚀刻。

本发明的第一蚀刻可以是使用缓冲的氢氟酸的湿蚀刻。

本发明的第一蚀刻可以是干蚀刻。

本发明的第一蚀刻可以是使用CH_4（甲烷）气体的干蚀刻。

本发明的第二蚀刻可以是湿蚀刻。

本发明的第二蚀刻可以是使用光刻胶的显影溶液的湿蚀刻。

本发明的第二蚀刻可以是使用有机碱溶液的湿蚀刻。

本发明的第二蚀刻可以是使用TMAH（四甲基氢氧化铵）的湿蚀刻。

本发明的半导体器件的一个方面具有：栅电极、在栅电极之上的栅绝缘膜、在栅绝缘膜之上的包含金属材料的第一膜、在第一膜之上的包含透明半导体材料和n型或p型杂质的第二膜、以及在第二膜和栅绝缘膜之上的包含透明半导体材料的第三膜。

本发明的半导体器件的一个方面具有：在衬底之上的绝缘膜、在绝缘膜之上的包含金属材料的第一膜、在金属膜之上的包含透明半导体材料和n型或p型杂质的第二膜、在绝缘膜和第二膜之上的包含透明半导体材料的第三膜、在第三膜之上的栅绝缘膜、和在栅绝缘膜之上的栅电极。

本发明的半导体器件的制造方法的一个方面具有以下步骤：在衬底之上形成绝缘膜；在绝缘膜之上形成包含金属材料的第一膜；在第一膜之上形成包含透明半导体材料和n型或p型杂质的第二膜；蚀刻第二膜；和蚀刻第一膜。

本发明的半导体器件的制造方法的一个方面具有以下步骤：在衬底之上形成栅电极；在栅电极之上形成栅绝缘膜；在栅绝缘膜之上形成包含金属材料的第一膜；在第二膜之上形成包含透明半导体材料和n型或p型杂质的第二膜；蚀刻第二膜；和蚀刻第一膜。

在顶栅半导体器件中，通过使用玻璃衬底、氧化硅膜或氧氮化硅膜形成的基膜不被蚀刻，并且诸如钠的杂质不从衬底扩散到半导体膜中，使得其特性不劣化。

在底栅半导体器件中，栅绝缘膜不被蚀刻并且其特性不会变得不稳定。

由于对于源电极和漏电极的一部分使用Al，因此可以获得低电阻的引线。

附图说明

在附图中，

图1A和图1B表示本发明的半导体器件；

图2A~2D表示本发明的半导体器件的制造步骤；

图3A~3D表示本发明的半导体器件的制造步骤；

图4A和图4B表示本发明的半导体器件的制造步骤；

图5A~5D表示本发明的半导体器件的制造步骤；

图6A~6C表示本发明的半导体器件的制造步骤；

图7A和图7B表示常规的例子；

图8A和图8B表示液晶显示器的制造步骤；

图9A和图9B表示液晶显示器的制造步骤；

图10A和图10B表示发光器件的制造步骤；

图11A和图11B表示发光器件的制造步骤；

图12A~12F分别表示发光器件的等效电路。

图13表示发光器件的等效电路。

图14A表示像素部分的顶部前视图，图14B表示发光器件的等效电路；

图15A~15E分别表示应用本发明的电子装置的例子；

图16表示应用本发明的电子装置的例子。

以下参照附图说明本发明的实施例。注意，本发明不限于以下的说明，并且本领域技术人员很容易理解可以在不背离本发明的目的和范围的条件下以各种方式修改这里公开的实施例和细节。因此，本发明不应被解释为限于以下给出的实施例的说明。

具体实施方式

[实施例1]

这里说明底栅半导体器件。

图1A是示出本发明的实施例的一个例子的截面图。在图1A中，附图标记1表示衬底，3表示栅电极，5表示栅绝缘膜、10表示源电极，10a表示第一导电膜，10b表示第二导电膜，11表示漏电极，11a表示第

一导电膜，11b表示第二导电膜，13表示半导体膜。可以在半导体膜13之上形成用于钝化或平坦化的绝缘膜。

在衬底1之上形成栅电极3，在栅电极3之上形成栅绝缘膜5，并且在栅绝缘膜5之上形成源电极10和漏电极11。源电极10由具有第一导电膜10a与第二导电膜10b的叠层膜形成，并且漏电极11由具有第一导电膜11a与第二导电膜11b的叠层膜形成。可以在第一导电膜10a和第二导电膜10b之间或者在第一导电膜11a和第二导电膜11b之间形成第三导电膜。源电极10和漏电极11可分别形成为通过栅绝缘膜5与栅电极3部分重叠。在源电极10之上形成半导体膜13并且在栅绝缘膜5之上形成漏电极11。

这里说明各结构。

（1）衬底

对于形成衬底，可以使用通过使用玻璃衬底形成的衬底、诸如氧化铝的绝缘材料和可以在后续步骤中抵抗处理温度的塑料衬底等。在对于衬底1使用塑料衬底的情况下，可以使用PC（聚碳酸酯）、PES（聚醚砜）、PET（聚对苯二甲酸乙二酯）或PEN（聚萘二甲酸乙二酯）等。在塑料衬底的情况下，可以在表面的上方设置无机层或有机层作为的气体阻挡层。在在塑料衬底的制造过程中在衬底上产生由灰尘等形成的突出物的情况下，可以在用CMP等抛光衬底以使其表面平坦化之后使用该衬底。可以在衬底1之上形成用于防止杂质等从衬底侧扩散的诸如氧化硅（SiOx）、氮化硅（SiNx）、氧氮化硅（SiOxNy）（x>y）和氮氧化硅（SiNxOy）（x>y）的绝缘膜。

（2）栅电极

可以通过使用Al（铝）膜、W（钨）膜、Mo（钼）膜、Ta（钽）膜、Cu（铜）膜、Ti（钛）膜或包含这些元素作为主要成分的合金材料（例如，Al合金膜、MoW（钼钨）合金膜）等形成栅电极。可以使用以掺杂有诸如P（磷）的杂质元素的多晶硅膜为代表的半导体膜。栅电极3可以是单层或其中层叠两层或更多层的叠层膜。

（3）栅绝缘膜

可以通过使用例如氧化硅膜和氧氮化硅膜的包含硅作为主要成分的绝缘膜形成栅绝缘膜5。另外，它可以是单层或叠层膜。

（4）源电极和漏电极

源电极10由第一导电膜10a与第二导电膜10b的叠层膜形成，并且漏电极11由第一导电膜11a与第二导电膜11b的叠层膜形成。

作为第一导电膜，可以使用Al膜、诸如AlNi（铝镍）膜和AlNd（钕铝）膜的Al合金膜。作为第二导电膜，可以使用其中添加B（硼）、Al（铝）、Ga（镓）、P（磷）或As（砷）的p型或n型杂质的ZnO（氧化锌）。可以在第一导电膜和第二导电膜之间设置诸如Ti膜的金属膜作为第三导电膜。

（5）半导体膜

使用ZnO膜作为半导体膜。由于与半导体膜接触的源电极和漏电极具有其中添加p型或n型杂质的ZnO膜，因此它们可以很容易地与半导体膜连接。

（6）绝缘膜

虽然没有示出，但可以在半导体膜13之上形成诸如钝化膜和平坦化膜的绝缘膜。可以使用氧化硅（SiOx）、氮化硅（SiNx）、氧氮化硅（SiOxNy）（x>y）和氮氧化硅（SiNxOy）（x>y）、SOG（旋涂玻璃）膜或丙烯的有机树脂膜或它们的叠层膜。

在底栅半导体器件中，栅绝缘膜在制造过程中不被蚀刻，并且特性不会变得不稳定。对于源电极和漏电极的一部分使用Al，由此实现低电阻的引线。

[实施例2]

这里说明顶栅半导体器件。

图1B是示出本发明的实施例的一个例子的截面图。在图1B中，附图标记1表示衬底，20表示绝缘膜、25表示源电极，25a表示第一导电膜，25b表示第二导电膜，26表示漏电极，26a表示第一导电膜，26b表示第二导电膜，27表示半导体膜，28表示栅绝缘膜，29表示栅电极。可以在栅电极之上形成用于钝化或平坦化的绝缘膜。

在衬底1上形成绝缘膜20，并且在绝缘膜20之上形成源电极25和漏电极26。源电极25由第一导电膜25a与第二导电膜25b的叠层膜形成，并且漏电极26由第一导电膜26a与第二导电膜26b的叠层膜形成。可以在第一导电膜25a和第二导电膜25b之间或者在第一导电膜26a和第二导电膜26b之间形成第三导电膜。在源电极25之上形成半导体膜27并且在绝缘膜20之上形成漏电极26，在半导体膜27之上形成栅绝缘膜28，并且在栅绝缘膜28之上形成栅电极29。栅电极29可形成为与源电极和漏电极部分重叠，使得栅绝缘膜28和半导体膜27被插入它们之间。

这里说明各结构。

对于衬底，可以使用与在实施例1中说明的那些相同的源电极、漏电极、半导体膜和栅电极。

（1）在衬底之上的绝缘膜

在衬底1之上形成氧化硅膜和氧氮化硅膜作为用于防止杂质等从衬底侧扩散的绝缘膜20。另外，它可以是单层或叠层膜。

（2）栅绝缘膜

可以通过使用例如氧化硅膜、氧氮化硅膜、氮氧化硅膜和氮化硅膜的包含硅作为主要成分的绝缘膜形成栅绝缘膜28。另外，它可以是单层或叠层膜。

（3）在栅电极之上的绝缘膜

虽然没有示出，但在栅电极29之上形成诸如钝化膜和平坦化膜的层间绝缘膜。可以使用SiO_x膜、SiNx膜、SiON膜、SiNO膜、SOG（旋涂玻璃）膜和丙烯的有机树脂膜或它们的叠层膜。

在顶栅半导体器件中，衬底或通过使用氧化硅膜或氧氮化硅膜形成的基膜不被蚀刻，使得诸如钠的杂质不从衬底扩散到半导体膜中，并且特性不劣化。对于源电极和漏电极的一部分使用Al，由此实现低电阻的引线。

[实施例3]

说明底栅半导体器件的制造方法，其中，在栅电极之上形成氧化硅膜或氧氮化硅膜作为栅绝缘膜，形成Al膜或Al合金膜作为第一导电

膜，形成其中添加n型或p型杂质的ZnO膜作为第二导电膜，然后，第二导电膜通过第一蚀刻被蚀刻为具有岛状形状并且第一导电膜通过第二蚀刻被蚀刻为具有岛状形状以形成源电极和漏电极，并且，形成ZnO半导体膜。

如图2A所示，形成栅电极3。在衬底1之上的栅电极的厚度可以为10~200nm。可以通过使用实施例1所示的材料形成衬底1。这里，使用玻璃衬底。

可以通过CVD或溅射形成厚度为10~200nm的包含氧化硅（SiOx）、氮化硅（SiNx）、氧氮化硅（SiOxNy）（x>y）和氮氧化硅（SiNxOy）（x>y）的绝缘膜2，以防止杂质等从衬底侧扩散（图2B）。

可以通过用高密度等离子处理衬底1的表面形成绝缘膜2。例如，可以通过使用2.45GHz的微波产生高密度等离子，并且仅要求电子密度为1×10^{11}~$1\times10^{13}/cm^3$并且电子温度为2eV或更低。这种高密度等离子具有较低的动能的活性物质，并且，与常规的等离子处理相比，可以形成由等离子造成的损伤更少的具有更少的缺陷的膜。

可以在诸如包含氮气和惰性气体的气氛，包含氮气、氢气和惰性气体的气氛，以及包含氨气和惰性气体的气氛的氮化气氛下通过高密度等离子处理氮化衬底1的表面。在使用玻璃衬底作为经受高密度等离子氮化处理的衬底1的情况下，作为在衬底1的表面之上形成的氮化物膜，可以形成包含氮化硅作为主要成分的绝缘膜2。可以通过使用通过等离子CVD在氮化物膜的上方形成氧化硅膜或氧氮化硅膜的多个层来形成绝缘膜2。

另外，可以类似地通过用高密度等离子在绝缘膜2的表面之上进行氮化形成氮化物膜。

通过用高密度等离子氮化形成的氮化物膜可抑制杂质从衬底1的扩散。

可以通过使用实施例1所示的材料形成栅电极3。这里，通过使用AlNd（铝钕）靶材的溅射形成AlNd膜并将其处理成岛状形状。对于将膜处理成岛状形状，使用光刻方法，并且使用干蚀刻或湿蚀刻。

在清洗栅电极3的表面和衬底1或绝缘膜2的表面之后，在栅电极3之上通过使用已知的CVD或溅射形成厚度为10~200nm的栅绝缘膜5（图2A和图2B）。可以在不暴露于空气的情况下连续实施表面清洗步骤和栅绝缘膜5的形成步骤。在对于栅电极3使用Al膜的情况下，当在高温下形成栅绝缘膜5时，在一些情况下产生隆起（hillock）。因此，优选地，在500°C或更低、优选350°C或更低的低温下形成膜。

可以通过使用实施例1所示的材料形成栅绝缘膜5。这里，形成氧化硅膜。注意，在以下的附图中省略绝缘膜2。

在栅绝缘膜5上形成厚度为10~200nm的用于源电极和漏电极的第一导电膜6。可以通过使用实施例1所示的材料形成第一导电膜6。这里，使用AlNi（铝镍）膜或AlNd膜。可以通过使用AlNi靶材或AlNd靶材的溅射形成第一导电膜6。在形成栅绝缘膜5之后，可以在不暴露于空气的情况下连续形成第一导电膜6。

在第一导电膜6上形成厚度为10~200nm的第二导电膜7（图2C）。可以通过使用实施例1所示的材料形成7。这里，使用其中添加诸如Al或Ga的杂质的ZnO（氧化锌）。因此，可以很容易地在第二导电膜7和后面形成为半导体层的ZnO膜之间产生欧姆接触。可以通过使用溅射形成第二导电膜7。例如，对于添加Al或Ga可以使用以下的方法：使用其中添加1~10重量%的Al或Ga的ZnO靶材的溅射；或在200~300°C下在ZnO靶材上安装Al或Ga芯片的溅射。

在形成第一导电膜6之后，可以在不暴露于空气的情况下连续形成第二导电膜7。因此，可以在不暴露于空气的情况下连续实施从栅绝缘膜5到第二导电膜7的形成。

在第一导电膜6和第二导电膜7之间形成厚度为10~200nm的第三导电膜8（图2D）。接触电阻根据制造过程中的热处理温度在第一导电膜6和第二导电膜7之间偶尔增加。但是，通过形成第三导电膜8，可减小第一导电膜6与第二导电膜7之间的接触电阻。可以通过使用诸如通过溅射等形成的Ti膜的金属膜形成第三导电膜8。

在第二导电膜7之上形成光刻胶掩模9，并且第二导电膜7被蚀刻

（图3A和图3B）。在使用湿蚀刻的情况下，使用例如HF:NH_4F（重量比）=1:100~1:10的溶液的缓冲的氢氟酸（其中混合了HF（氢氟酸）和NH_4F（氟化氨））。

在使用干蚀刻的情况下，可以采用使用CH_4气体的各向异性等离子蚀刻。

在第二导电膜7之下形成第一导电膜6。因此，当第二导电膜7被蚀刻时，第一导电膜6用作蚀刻阻止层。因此，在蚀刻中可以在不损伤栅绝缘膜5的情况下形成源电极和漏电极。

当第二导电膜7被蚀刻时，第一导电膜6的一部分会被蚀刻。但是，由于如果第一导电膜6被完全蚀刻，则栅绝缘膜受损，因此需要注意不要完全蚀刻第一导电膜6。

然后，通过使用光刻胶掩模9蚀刻第一导电膜6形成源电极10和漏电极11（图3C）。在本发明中，通过使用以作为光刻胶的显影剂的TMAH（四甲基氢氧化铵）为代表的有机碱溶液蚀刻第一导电膜6。

在对于第一导电膜6使用AlNi膜并且对于蚀刻溶液使用TMAH的情况下，在30°C下蚀刻速率为约300nm/min。另一方面，使用上述材料的第二导电膜7或栅绝缘膜5不被TMAH蚀刻。因此，可以在不损伤栅绝缘膜5的情况下形成源电极10和漏电极11。并且，岛状形状的第二导电膜10b和11b的尺寸不会减小。在本发明中，可以通过使用当在不使用特定的蚀刻溶液的情况下形成光刻胶掩模时使用的显影剂蚀刻第一导电膜6。因此，成本降低并且效率增加。

在形成源电极10和漏电极11之后，光刻胶掩模9被去除。

在源电极10、漏电极11和栅绝缘膜5之上通过溅射形成厚度为20~200nm的ZnO膜作为半导体膜12（图3D）。例如，可以在200~300°C下通过使用ZnO靶材、氧气/氩气的流量比为30~20的溅射形成膜。

通过光刻方法蚀刻半导体膜12以形成岛状形状的半导体膜13（图4A）。可以采用使用缓冲的氢氟酸的湿蚀刻方法或使用CH_4气体的各向异性干蚀刻方法。

在半导体膜12和第二导电膜10b和11b中通常使用ZnO，并且，难

以获得足够的蚀刻选择性。但是，由于要求在与半导体膜12接触的一部分中形成第二导电膜7，因此可以在例如引线部分的不与半导体膜12接触的一部分中蚀刻第二导电膜7。在上述的蚀刻方法中，第二导电膜10b和11b可被蚀刻，但第一导电膜10a和11a不被蚀刻。因此，第一导电膜10a和11a用作引线，并且与半导体器件的电连接得到保证。

通过CVD或溅射在半导体膜13之上形成厚度为50nm~1μm的绝缘膜14（图4B）。可以形成包含硅作为主要成分的绝缘膜作为绝缘膜14。可以在包含硅的绝缘膜之上层叠有机树脂膜等。绝缘膜14用作平坦化膜或钝化膜。由于在源电极10和漏电极11内包含Al，因此当在高温下形成绝缘膜14时偶尔产生隆起。因此，优选地，在500°C或更低、优选350°C或更低的低温下形成。

在绝缘膜14中形成接触孔，并且，如有必要设置与栅电极3、源电极10和漏电极11接触的导电膜。

根据本发明，在不损伤栅绝缘膜的情况下形成半导体器件。使用诸如AlNi膜的Al合金膜作为第一导电膜，由此实现低电阻的引线。

[实施例4]

这里，说明顶栅半导体器件的制造方法，其中，在氧化硅膜或氧氮化硅膜上形成Al膜或Al合金膜作为第一导电膜，并且形成其中添加n型或p型杂质的ZnO膜作为第二导电膜，然后，第二导电膜通过第一蚀刻形成为具有岛状形状，第一导电膜通过第二蚀刻形成为具有岛状形状以形成源电极和漏电极，形成ZnO半导体膜，形成栅绝缘膜，并且形成栅电极。注意，不用说，在实施例1~3中说明的材料和制造方法可被应用于本实施例。

如图5A所示，通过CVD或溅射以10~200nm的厚度在衬底1之上形成氧化硅（SiOx）膜作为绝缘膜20。绝缘膜20防止杂质等从衬底1侧扩散。

在绝缘膜20之上通过溅射或蒸镀形成厚度为10~200nm的用于源电极和漏电极的第一导电膜21。可以使用诸如在实施例1中示出的AlNi（铝镍）膜的Al合金膜作为第一导电膜21。在形成绝缘膜20之后，可

以在不暴露于空气的情况下连续形成第一导电膜21。

在第一导电膜21上通过溅射形成厚度为10~200nm的第二导电膜22（图5A）。作为第二导电膜22，可以使用其中添加B（硼）、Al（铝）、Ga（镓）、P（磷）或As（砷）等的p型或n型杂质的ZnO（氧化锌）。在形成第一导电膜21之后，可在不暴露于空气的情况下连续形成第二导电膜22。因此，可以在不暴露于空气的情况下连续实施形成绝缘膜20到第二导电膜22的步骤。

为了减小第一导电膜21与第二导电膜22之间的接触电阻，可以在第一导电膜21和第二导电膜22之间通过溅射形成厚度为10~200nm的诸如Ti膜的金属膜作为第三导电膜23（图5B）。

在第二导电膜22之上形成光刻胶掩模24，并且蚀刻第二导电膜22（图5C）。作为蚀刻方法，可以采用使用缓冲的氢氟酸的湿蚀刻或使用CH_4气体的干蚀刻方法。

在第二导电膜22之下形成第一导电膜21。因此，当第二导电膜22被蚀刻时，第一导电膜21用作蚀刻阻止层。因此，可以在不通过蚀刻绝缘膜20露出衬底1的情况下形成源电极和漏电极。

当第二导电膜22被蚀刻时，第一导电膜21的一部分可被蚀刻。注意，如果所有的第一导电膜21被蚀刻，那么绝缘膜20被蚀刻并且衬底1被露出，这会导致在衬底1中包含的杂质的扩散。

第一导电膜21被蚀刻以形成源电极25和漏电极26（图5D）。作为蚀刻方法，采用使用光刻胶的显影剂TMAH的湿蚀刻。因此，可以在不蚀刻绝缘膜20的情况下形成源电极25和漏电极26。并且，由于ZnO膜不会被TMAH蚀刻，所以岛状形状的第二导电膜25b和26b的尺寸不会减小。可以在不对第一导电膜21使用特殊的蚀刻溶液的情况下用在光刻胶掩模的形成中使用的显影剂进行蚀刻，这导致成本降低和效率提高。

在形成源电极25和漏电极26之后，去除光刻胶掩模24。

在源电极25、漏电极26和绝缘膜20之上通过溅射形成厚度为20~200nm的ZnO膜作为半导体膜27（图6A）。

通过光刻方法蚀刻半导体膜27以制成岛状形状半导体膜27。作为蚀刻方法，可以采用使用缓冲的氢氟酸的湿蚀刻或使用CH_4气体的干蚀刻方法。

对于半导体膜27和第二导电膜25b和26b通常使用ZnO，并且，难以获得较高的蚀刻选择性。但是，由于可与实施例3相同地在源电极和漏电极中形成第二导电膜22，因此可以在不与半导体膜27接触的部分特别是在引线部分中蚀刻第二导电膜。

在半导体膜27之上通过CVD或溅射形成厚度为10~200nm的栅绝缘膜28（图6B）。半导体膜27可经受在上述的实施例中示出的高密度等离子处理以形成栅绝缘膜。可以在诸如包含氮气和惰性气体的气氛，包含氮气、氢气和惰性气体的气氛和包含氨气和惰性气体的气氛的氮化气氛下通过高密度等离子处理氮化半导体膜27的表面。

可以通过使用例如氧化硅膜、氧氮化硅膜、氮化硅膜和氮氧化硅膜的包含硅作为主要成分的绝缘膜形成栅绝缘膜28。另外，它可以是单层或叠层膜。

在栅绝缘膜28之上形成栅电极29（图6B）。可以通过使用上述的实施例所示的材料形成栅电极29，并且它可以是单层或包含两个或更多层的叠层膜。作为用于成膜的方法，可以使用已知的CVD溅射或蒸镀等。对于用光刻方法将栅电极29处理成岛状形状，可以使用干蚀刻或湿蚀刻方法。

在栅电极29和栅绝缘膜28之上通过CVD或溅射形成厚度为50nm~1μm的绝缘膜30（图6C）。可以通过使用包含硅的绝缘膜形成绝缘膜30。可以在包含硅的绝缘膜之上层叠有机树脂膜等。绝缘膜30用作平坦化膜或钝化膜。由于在源电极25和漏电极26中包含Al，因此，当在高温下形成栅绝缘膜28、栅电极29和绝缘膜30时，偶尔产生隆起（hillock）。因此，优选地，在500°C或更低、优选350°C或更低的低温下形成它们。

如上所述，本发明可防止杂质由于衬底1的露出而扩散。诸如AlNi膜的Al合金膜被用作第一导电膜，由此实现引线的低电阻。

[实施例5]

这里参照图8A和图8B以及图9A和图9B说明通过使用实施例1~3所示的底栅半导体器件制造液晶显示器的方法。注意，不用说，可以应用在实施例2和4中示出的顶栅半导体器件。图8A和图9A表示沿图8B中的线X-Y切取的截面图。

在玻璃衬底或塑料衬底1之上形成栅极引线40和辅助电容器引线41。通过溅射然后通过已知的光刻方法和蚀刻形成AlNd膜。

通过使用通过CVD或溅射形成的氧化硅膜或氧氮化硅膜形成栅绝缘膜42。

在栅绝缘膜42之上通过溅射形成AlNi膜作为第一导电膜。第一导电膜在后面形成源电极45a、漏电极46a和源极引线47。

在第一导电膜之上通过溅射形成其中添加Al的ZnO（氧化锌）膜作为第二导电膜。第二导电膜在后面形成源电极45b、漏电极46b和源极引线47。

在第二导电膜（图中未示出）之上，在要成为源电极部分、漏电极部分和源极引线部分的区域中形成光刻胶掩模。然后，蚀刻第二导电膜。这里，通过使用缓冲的氢氟酸即$HF:NH_4F=1:100$（重量比）的溶液进行蚀刻。

然后，通过使用TMAH溶液蚀刻第一导电膜以形成源电极45a、漏电极46a和源极引线47。此后，光刻胶掩模被去除。然后，可以在不损伤栅绝缘膜42的情况下形成源电极45、漏电极46和源极引线47。另外，由于ZnO膜不被TMAH蚀刻，因此岛状形状的第二导电膜的尺寸不会减小。并且，由于AlNi膜被用于第一导电膜，因此源极引线的电阻可减小。

然后，形成半导体膜48。通过溅射形成ZnO膜，然后，通过光刻方法和蚀刻从ZnO膜形成半导体膜48。作为蚀刻，采用使用缓冲的氢氟酸的湿蚀刻。这里，由于在要成为引线的部分中形成第一导电膜，因此第二导电膜中的不与半导体膜48接触的部分可被部分去除。

在半导体膜48之上通过CVD、溅射或涂敷等形成绝缘膜49。可以

通过使用具有包含硅的绝缘膜或有机树脂膜等的叠层膜形成绝缘膜49。绝缘膜49可以是使得表面的不均匀性平坦化的膜。

通过使用光刻方法和蚀刻方法在绝缘膜49中形成通向漏电极46的接触孔和用于辅助电容器的接触孔。

通过溅射形成透明导电膜，然后，通过使用光刻方法和蚀刻形成像素电极50。例如，可以使用ITO（氧化铟锡）、ITSO（包含氧化硅的氧化铟锡）或IZO（氧化铟锌）。

在反射型液晶显示器的情况下，作为透明电极的替代，形成诸如Ag（银）、Au（金）、Cu（铜）、W（钨）或Al（铝）的反光金属材料。

像素电极50与辅助电容器引线41重叠的部分形成由像素电极50、栅绝缘膜42和辅助电容器引线41形成的辅助电容器100（图8A和图8B）。

在引线和电极中，弯曲部分或宽度改变的部分的角可被平滑化和修圆。可以通过使用采用光掩模的图案制造的光掩模图案实现斜切的角的形状。这将具有下述的优点。当进行使用等离子的干蚀刻时，可以通过斜切突出部分来抑制由于异常放电（discharge）导致的细粒子的产生。即使产生细粒子，也可在清洗时防止细粒子在角上蓄积，并且可通过斜切凹进的部分将细粒子洗去。因此，可以解决制造过程中的细粒子或灰尘的问题，并且可提高产量。

形成取向膜51，以使其覆盖像素电极50。通过液滴排放方法或印刷等形成取向膜。在形成取向膜之后，进行摩擦。

通过使用着色层和光屏蔽层（黑矩阵）形成滤色片55，并且，在相对衬底56上形成保护绝缘膜54。在保护绝缘膜54上形成透明电极57并且形成取向膜53（图9A）。对取向膜进行摩擦处理。

然后，通过液滴排放方法形成密封剂的闭合图案75（图9B）。用液晶组合物52填充由密封剂包围的区域（图9A）。

在将液晶组合物52滴在闭合图案75中之后，相对衬底56和其中形成半导体器件的衬底1被相互固定。当填充液晶组合物52时，可以采用

以下的替代方案：在衬底1上设置具有开口部分的密封图案；将相对衬底56和衬底1相互贴合；然后，通过利用毛细作用注入液晶。

作为液晶组合物52的对准模式，可以使用液晶分子的排列从光入射侧到光发射侧扭曲90°的TN模式、FLC模式或IPS模式等。注意，电极图案与图8B所示的电极图案不同，并且在IPS模式的情况下为梳状形状。

偏振片被固定到相对衬底56和其上面形成了半导体器件的衬底1上。另外，如果需要的话可以固定光学膜。

可以通过分散球形隔离件或形成由树脂形成的柱状隔离件或通过在密封剂中混入填充物来保持相对衬底56和其上面形成了半导体器件的衬底1之间的距离。上述的柱状隔离件由包含丙烯酸树脂、聚酰亚胺、聚酰亚胺酰胺（polyimide amide）或环氧树脂中的至少一种作为主要成分的有机树脂材料，或者具有氧化硅、氮化硅和含氮的氧化硅中的一种的无机材料，或者它们的叠层膜形成。

然后，通过使用已知的技术将FPC（柔性印刷电路）贴合到衬底1上，使得各向异性导电层被插入其间。

可以在衬底之上形成外围驱动电路。在图9B中示出示例性平面图。

在由玻璃等形成的衬底61之上形成栅极引线驱动电路62、源极引线驱动电路63和有源矩阵部分64。栅极引线驱动电路62至少由移位寄存器62a和缓冲器62b构成。源极引线驱动电路63至少由移位寄存器63a、缓冲器63b和对通过视频线68传送的视频信号进行采样的模拟开关69构成。从栅极引线驱动电路62延伸的多个栅极引线72在有源矩阵部分64中相互平行排列。从源极引线驱动电路63延伸的多根源极引线71与栅极引线72正交排列。另外，辅助电容器引线73与栅极引线72平行排列。另外，半导体器件65、液晶部分66和辅助电容器67被设置在被栅极引线72、源极引线71和辅助电容器引线73包围的区域中。

栅极引线驱动电路62、源极引线驱动电路63和模拟开关69具有通过与半导体器件65相同的制造方法制成以具有类似的结构的半导体器

件。

在半导体器件65中，栅电极与栅极引线72连接，并且源电极与源极引线71连接。通过在与半导体器件65的漏电极连接的像素电极和在相对衬底之上的相对电极之间引入并密封液晶来形成液晶部分66。辅助电容器引线73与具有与相对电极相同的电位的电极连接。

在上述的液晶显示器中，栅绝缘膜不被蚀刻，并且特性不会变得不稳定，因此实现较高的可靠性。在使用顶栅半导体器件的情况下，玻璃衬底或通过使用形成的基膜、氧化硅膜或氧氮化硅膜均不会被蚀刻，使得诸如钠的杂质不从衬底扩散到半导体膜中，并且特性不会劣化，由此可实现较高的可靠性。

对于源电极和漏电极的一部分使用Al，由此实现低电阻的引线。

[实施例6]

这里参照图10A和图10B以及图11A和图11B说明通过使用实施例1~3所示的底栅半导体器件制造发光器件的方法。注意，不用说，可以应用实施例2和4的半导体器件。

基于上述的实施例的说明制造半导体器件，并且实施到图10A所示的阶段的形成。注意，与上述的实施例相同的部分由相同的附图标记表示。

在EL显示器中，像素电极50用作阳极或阴极。作为用于像素电极50的材料，可以使用以下的材料：诸如铝（Al）、银（Ag）、金（Au）、铂（Pt）、镍（Ni）、钨（W）、铬（Cr）、钼（Mo）、铁（Fe）、钴（Co）、铜（Cu）、钯（Pd）、锂（Li）、铯（Cs）、镁（Mg）、钙（Ca）、锶（Sr）或钛（Ti）的导电金属；诸如铝硅（Al-Si）、铝钛（Al-Ti）或铝硅铜（Al-Si-Cu）的合金；诸如氮化钛（TiN）的金属材料的氮化物；诸如ITO、含硅的ITO或IZO的金属化合物。

仅需要通过使用透光的导电膜形成从中提取从EL层发射的光的电极，并且，可以使用诸如ITO、含硅的ITO或IZO的金属化合物以及诸如Al或Ag的金属的非常薄的膜。

当从与像素电极50相对的电极提取发射光时，可以对于像素电极

50使用高度反射材料（Al或Ag等）。在本实施例中，ITSO（即指含硅的ITO）被用作像素电极50（图10A）。

然后，形成通过使用有机材料或无机材料形成的绝缘膜以使其覆盖绝缘膜49和像素电极50。然后，处理绝缘膜以部分露出像素电极50，由此形成隔离壁81。作为隔离壁81的材料，优选光敏的有机材料（诸如丙烯酸树脂或聚酰亚胺）。作为替代方案，也可以使用非光敏的有机材料或无机材料。并且，可以通过以使得诸如钛黑或氮化硅的黑色颜料或染料借助于分散剂分散于隔离壁81的材料中的方式将隔离壁81着色成黑色，从而将隔离壁81用作黑矩阵。希望隔离壁81具有锥形形状，并且向着像素电极的那些端面81a具有连续变化的曲率（图10B）。

然后，形成包含发光物质的层82，并且形成覆盖包含发光物质的层82的相对电极83。然后，可以制造包含发光物质的层82被插入像素电极50和相对电极83之间的发光元件，并且可通过在相对电极83和像素电极50之间施加电压获得光发射。

作为用于形成相对电极83的电极材料，可使用与可用于像素电极的材料类似的材料。在本实施例中，对于第二电极使用铝。

通过蒸镀、喷墨、旋涂、浸涂、卷绕式方法（roll-to-roll method）或溅射等形成包含发光物质的层82。

在有机电致发光显示器的情况下，包含发光物质的层82可以是分别具有空穴传输、空穴注入、电子传输、电子注入或发光的功能的层的叠层膜或单层的发光层。作为包含发光物质的层，可以使用有机化合物的单层或叠层膜。

在阳极和空穴传输层之间设置空穴注入层。作为空穴注入层，可以使用有机化合物和金属氧化物的混合层。这防止由于在像素电极50的表面上形成的不均匀性或留在电极的表面上的外来物质在像素电极50和相对电极83之间出现短路。混合层的厚度优选为60nm或更厚，更优选120nm或更厚。由于膜厚的增加不导致驱动电压的增加，因此，可以选择膜厚，使得可充分掩盖不均匀性或外来物质的影响。因此，在通过本发明制造的发光器件中，不产生黑点，并且驱动电压或功耗

不增加。

作为金属氧化物，优选为过渡金属的氧化物或氮化物，具体而言，优选为氧化锆、氧化铪、氧化钒、氧化铌、氧化钽、氧化铬、氧化钼、氧化钨、氧化钛、氧化锰和氧化铼。

作为有机化合物，可以使用以下的有机化合物：诸如4,4′-二[*N*-（1-萘基）-*N*-苯基-氨基]- 联苯（NPB）、4,4′-二[*N*-（3-甲苯基）-*N*-苯基-氨基]-联苯（TPD）、4,4′,4″-三(*N*,*N*-联苯-氨基)-三苯胺（TDATA）、4,4′,4″-三[(*N*-(3-甲苯基)-*N*-苯基-氨基]-三苯胺（MTDATA）、4,4′-二(*N*-4(*N*,*N*-二间甲苯氨基)苯基)-*N*-苯氨基)联苯（DNTPD）、1,3,5-三[N,N-二(间甲苯基) 氨基]苯（m-MTDAB）和4,4′,4″-三(N-咔唑基) 三苯胺（TCTA）的具有芳氨基的有机材料，酞菁（缩写：H_2Pc）、铜酞菁（缩写：CuPc）或钒氧酞菁（缩写：VOPc）等。

在阳极和发光层之间，或者当设置空穴注入层时在空穴注入层和发光层之间设置空穴传输层。通过使用具有优异的空穴传输性能的层，例如，通过使用诸如NPB、TPD、TDATA、MTDATA和BSPB的芳香胺的化合物（即，具有苯环-氮键）形成的层，形成空穴传输层。这里提到的物质大体上具有1×10^{-6}~$10cm^2/Vs$的空穴迁移率。注意，作为这些材料，可以使用空穴传输性能比电子传输性能高的物质。注意，不仅可以通过单层而且可以通过层叠从上述的物质形成的两个或更多个层的叠层膜来形成空穴传输层。

在阳极和阴极之间，或者当设置空穴注入层和电子传输层时在空穴注入层和电子传输层之间设置发光层。对于发光层没有特别的限制；但是，用作发光层的层大致具有两种模式。一种是在由其能隙比变成发光中心的发光物质（掺杂材料）的能隙大的材料（宿主材料）形成的层中包含分散的发光物质的主客型层，另一种是其中发光层仅由发光物质制成的层。由于前一种几乎不会发生浓度淬火，因此它是优选的。作为要成为发光中心的发光物质，可以使用以下物质：4-二氰基亚甲基-2-甲基-6-[2-(1,1,7,7-四甲基久洛尼定基-9-烯基)]-4*H*-吡喃（DCJT）、4-二氰基亚甲基-2-叔丁基-6-[2-(1,1,7,7-四甲基久洛尼定基

-9-烯基)]-4*H*-吡喃、periflanthene、2,5-二氰基-1、4-二(10-甲氧基-1,1,7,7-四甲基久洛尼定基-9-烯基)苯；*N*,*N*′-二甲基喹吖啶酮（DMQd）、香豆素6、香豆素545T、三(8-羟基喹啉)铝（Alq_3）、9,9′-联蒽、9,10-二苯基蒽（DPA）、9,10-二（2-萘基）蒽（DNA）；2,5,8,11-四叔丁基二萘嵌苯（TBP）；PtOEP；$Ir(ppy)_3$；$Btp_2Ir(acac)$；或FIrpic；等等。在形成散布发光物质的层时，作为要成为宿主材料的基体材料，可以使用以下的材料：诸如9,10-二(2-萘基)-2-叔丁基蒽（t-BuDNA）的蒽衍生物；诸如4,4′-二(N-咔唑基)联苯（CPB）的咔唑衍生物；或诸如三(8-羟基喹啉)铝（Alq_3）、三(4-甲基-8-羟基喹啉)铝（$Almq_3$）、二(10-羟苯基[h]-喹啉) 铍（BeBq2）、二(2-甲基-8-羟基喹啉)-4-联苯氧基-铝（BAlq）、二[2-(2-羟苯基)吡啶]锌（$Znpp_2$）或二[2-(2-羟苯基)苯恶唑]锌（ZnBOX）的金属络合物。作为可仅用发光物质构成发光层的材料，可以使用三(8-羟基喹啉)铝（Alq_3）、9,10-二（2-萘基）蒽（DNA）或二(2-甲基-8-羟基喹啉)-4-联苯酚铝（BAlq）等。

在发光层和阴极之间、或者当设置电子注入层时在发光层和电子注入层之间设置电子传输层。电子传输层是具有优异的电子传输性能的层，并且，例如是通过使用诸如三(8-羟基喹啉)铝（缩写：Alq_3）、三(5-甲基-8-羟基喹啉)铝（缩写：$Almq_3$）、二(10-羟基苯基[*h*]-喹啉) 铍（缩写：$BeBq_2$）和二(2-甲基-8-羟基喹啉)-4-联苯酚铝（缩写：BAlq）的具有喹啉骨架或苯并喹啉骨架的金属络合物形成的层。另外，可以使用诸如二[2-(2-羟基苯基) 苯并恶唑]锌（缩写：$Zn(BOX)_2$）或二[2-(2-羟基苯基) 苯并噻唑]锌（缩写：$Zn(BTZ)_2$）等的具有恶唑配位体或噻唑配位体的金属络合物。除了金属络合物以外，可以使用2-(4-联苯基)-5-(4-叔丁苯基)-1,3,4-恶二唑（PBD）、1,3-双[5-(4-叔丁苯基)-1,3,4-恶二唑-2-基]苯（OXD-7）、3-(4-叔丁苯基)-4-苯基-5-(4-联苯基)-1,2,4-三唑（TAZ）、3-(4-叔丁苯基)-4-(4-乙苯基)-5-(4-联苯基)-1,2,4-三唑（p-EtTAZ）、菲咯啉（bathophenanthroline，BPhen）或浴铜灵（bathocuproin，BCP）等。这里提到的这些物质主要具有1×10^{-6}~$10cm^2/Vs$的电子迁移率。注意，可以对电子传输层使用其它的物

质，只要它的电子传输性能比空穴传输性能高即可。并且，不仅可以通过单层而且可以通过层叠由上述的物质形成的两个或更多个层的叠层膜来形成电子传输层。

在阴极和电子传输层之间设置电子注入层。作为电子注入层，可以使用诸如氟化锂（LiF）、氟化铯（CsF）或氟化钙（CaF_2）的碱金属或碱土金属的化合物。此外，可以通过使用包含碱金属或碱土金属，例如，包含镁（Mg）等的Alq_3的电子传输物质来形成层。

在无机电致发光显示器的情况下，可以使用在用于包含发光物质的层82的分散剂中散布荧光物质粒子的无机电致发光显示器。

可以使用在ZnS中添加诸如Cl（氯）、I（碘）或Al（铝）的施主杂质以及Cu（铜）的荧光物质。

作为分散剂，可以使用以下的材料：诸如氰乙基纤维素类树脂、聚乙烯类树脂、聚丙烯类树脂、聚苯乙烯类树脂、有机硅树脂、环氧树脂或偏二氟乙烯树脂等的具有相对较高的介电常数的聚合物。可以通过混合树脂和诸如$BaTiO_3$（钛酸钡）或$SrTiO_3$（钛酸锶）的具有较高的介电常数的小粒子来调整介电常数。作为扩散设备，可以使用超声波扩散机等。

可以在包含发光物质的层82与一个电极之间设置电介质层。对于电介质层，使用具有较高的电介质击穿电压的高度介电和绝缘材料。其中的一个选自例如TiO_2、$BaTiO_3$、$SrTiO_3$、$PbTiO_3$、$KNbO_3$、$PbNbO_3$、Ta_2O_3、BaT_2O_6、$LiTaO_3$、Y_2O_3、Al_2O_3、ZrO_2、AlON或ZnS等的金属氧化物或氮化物。它们可被设置为均匀的膜或具有粒子结构的膜。

在无机电致发光显示器的情况下，可以使用在绝缘层之间插入发光层的双绝缘结构。可以通过使用II-VI化合物，例如，包含稀土元素的Mn（锰）或ZnO（氧化锌）来形成发光层，并且，可以通过使用诸如Si_3N_4、SiO_2、Al_2O_3或TiO_2的氧化物或氮化物形成绝缘层。

通过等离子CVD（未示出）在相对电极83之上形成含氮的氧化硅膜作为钝化膜。在使用含氮的氧化硅膜的情况下，使用以下的膜：通过利用等离子CVD使用SiH_4、N_2O和NH_3形成的氧氮化硅膜；通过使

用SiH_4和N_2O形成的氧氮化硅膜；或通过使用用Ar稀释SiH_4和N_2O得到的气体形成的氧氮化硅膜。

可以使用由SiH_4、N_2O和H_2制造的氧氮氢化硅（silicon oxide nitride hydride）膜作为钝化膜。注意，钝化膜不限于上述的物质。也可以使用包含硅作为主要成分的其它绝缘膜。另外，可以使用叠层膜结构以及单层结构。并且，可以使用氮化碳膜和氮化硅膜的多层膜或苯乙烯聚合物的多层膜。可以使用氮化硅膜或类金刚石碳膜。

然后，密封显示部分以保护发光元件免受促进劣化的诸如水的材料影响。在使用用于密封的相对衬底的情况下，通过使用绝缘密封剂固定相对衬底以露出外部连接部分。可以用诸如干氮气的不活泼气体填充相对衬底和元件衬底之间的空间，或者，可以通过向整个像素部分施加密封剂来固定相对衬底。优选地，使用紫外线硬化树脂等作为密封剂。可以在密封剂中混合干燥剂或用于使衬底之间的间隙保持恒定的粒子。然后，通过将柔性布线板固定到外部连接部分上来完成发光器件。

参照图11A和图11B示出如上面所述的那样制造的发光器件的结构的一个例子。注意，具有相同功能的部分即使具有不同的形状有时也由相同的附图标记表示，并且有时省略解释。

图11A表示通过使用透光导电膜形成像素电极50的结构，并且向衬底1发射在包含发光物质的层82中产生的光。并且，附图标记86表示相对衬底。在形成发光元件之后，通过使用密封剂等将该相对电极牢固地固定到衬底1上。用具有透光性能等的树脂85填充相对衬底86与元件之间的空间以密封发光元件。因此，可以防止发光元件由于湿气等劣化。优选地，树脂85具有吸湿性能。更优选地，具有较高的透光性能的干燥剂84分散于树脂85中以防止湿气的不利影响。

图11B表示通过使用具有透光性能的导电膜形成像素电极50和相对衬底83的结构。因此，如虚线箭头所示，可以向衬底1和相对衬底86发射光。在该结构中，通过在衬底1和相对衬底86外面设置偏振片88，可以防止屏幕透明，由此改善可视性。优选在偏振片88外面设置保护

膜87。

具有显示功能的本发明的发光器件可使用模拟视频信号或数字视频信号。如果使用数字视频信号，那么视频信号可使用电压或电流。

当发光元件发光时，要被输入到像素的视频信号可具有恒定的电压或恒定的电流。当视频信号具有恒定的电压时，恒定的电压被施加到发光元件，或者恒定的电流流过发光元件。

并且，当视频信号具有恒定的电流时，恒定的电压被施加到发光元件，或者恒定的电流流过发光元件。恒定的电压被施加到发光元件上的驱动方法被称为恒压驱动。同时，恒定的电流流过发光元件的驱动方法被称为恒流驱动。在恒流驱动中，不管发光元件的电阻如何变化，均流过恒定的电流。根据本发明的发光显示器及其驱动方法可使用上述方法中的任一种。

在发光器件中，栅绝缘膜不被蚀刻，并且，发光元件的特性不会不稳定，因此其可靠性较高。在使用顶栅半导体器件的情况下，由于玻璃衬底或者通过使用氧化硅膜或氧氮化硅膜形成的基膜不被蚀刻，因此使特性劣化的诸如钠的杂质不从衬底扩散到半导体膜中，所以可获得较高的可靠性。

对源电极和漏电极的一部分使用Al，由此实现低电阻的引线。

参照图12A~12F和图13等示出在面板和模块中包含的像素电路和保护电路以及它们的操作。图10A和图10B以及图11A和图11B分别表示半导体器件的驱动TFT 1403的截面图。开关TFT 1401、电流控制TFT 1404和擦除器TFT 1406可以在驱动TFT 1403的同时被制造，并且可具有与驱动TFT 1403相同的结构。

图12A所示的像素包含沿列方向配置的信号线1410和电源线1411和1412以及沿行方向配置的扫描线1414。像素还包含开关TFT 1401、驱动TFT 1403、电流控制TFT 1404、辅助电容器1402和发光元件1405。

除了驱动TFT 1403的栅电极与沿行方向设置的电源线1412连接以外，图12C所示的像素具有与图12A所示的结构相同的结构。换句话说，图12A和图12C所示的像素具有等效的电路图。但是，在与通过使

用与在沿行方向配置电源线1412的情况下使用导电层形成电源线的层不同的层中，通过使用导电层形成在沿列方向配置电源线1412的情况下（图12A）形成的电源线。这里，关注与驱动TFT 1403的栅电极连接的引线，并且，为了表示这些引线由不同的层形成，在图12A和图12C中分别地示出其结构。

作为图12A和图12C所示的像素的特征，驱动TFT 1403和电流控制TFT 1404在像素内被串联，并且优选地，设置驱动TFT 1403的沟道长度L（1403）和沟道宽度W（1403）以及电流控制TFT 1404的沟道长度L（1404）和沟道宽度W（1404），以满足L(1403)/W(1403):L(1404)/W(1404) = 5~6000:1。

驱动TFT 1403在饱和区域中操作，并用于控制流入发光元件1405的电流的电流值。电流控制TFT 1404在线性区域中操作并用于控制供给到发光元件1405的电流。优选地，在本实施例中，这两种TFT在制造过程中具有相同的导电类型；并且，TFT是n沟道型TFT。驱动TFT 1403可以是增强模式TFT或耗尽模式TFT。由于电流控制TFT 1404在具有以上的结构的发光器件中的线性区域中操作，因此电流控制TFT 1404的Vgs的轻微波动不影响发光元件1405的电流值。也就是说，可以通过在饱和区域中操作的驱动TFT 1403确定发光元件1405的电流值。使用以上的结构，可以补偿由于TFT的特性的变化导致的发光元件的亮度的变化，由此提供具有改善的图像质量的发光器件。

在图12A~12D中所示的各像素中，开关TFT 1401是要控制向像素输入视频信号，并且当开关TFT 1401被接通时视频信号被输入到像素中。然后，在辅助电容器1402中保持视频信号的电压。虽然图12A和图12C表示其中设置了辅助电容器1402的结构，但本发明不限于此。当栅电极电容等可用作保持视频信号的电容器时，未必设置辅助电容器1402。

除了添加TFT 1406和扫描线1415以外，图12B所示的像素具有与图12A所示的像素结构相同的像素结构。同样地，除了添加TFT 1406和扫描线1415以外，图12D所示的像素具有与图12C所示的像素结构相

同的像素结构。

通过另外设置扫描线1415来控制TFT 1406的ON和OFF。当TFT 1406被接通时，保持在辅助电容器1402中的电荷被放电，由此关断电流控制TFT 1404。换句话说，通过设置TFT 1406，可以强制产生电流不流入发光元件1405中的状态。因此，TFT 1406可被称为擦除器TFT。因此，在图12B和图12D所示的结构中，可在将信号写入所有的像素之前，与写入周期的开始同时或紧接其后开始发光周期；由此增加负荷比。

在图12E所示的像素中，沿列方向配置信号线1410和电源线1411，并且沿行方向配置扫描线1414。并且，像素包含开关TFT 1401、驱动TFT 1403、辅助电容器1402和发光元件1405。除了添加TFT 1406和扫描线1415以外，图12F所示的像素具有与图12E所示的像素结构相同的像素结构。在图12F所示的结构中，也可以通过设置TFT 1406增加负荷比。

由于在各个像素中设置TFT，因此当像素密度增加时可以在低电压下驱动有源矩阵发光器件。因此，可以认为有源矩阵发光器件是有利的。

虽然本实施例说明了在各个像素中设置各个TFT的有源矩阵发光器件，但也可形成无源矩阵发光器件。由于在无源矩阵发光器件中不在各个像素中设置TFT，因此可获得较高的开口率（aperture ratio）。在向发光叠层（stack）的两侧发射光的发光器件的情况下，无源矩阵发光器件的透射率增加。

随后，将说明通过使用图12E所示的等效电路在扫描线和信号线上设置二极管作为保护电路的情况。

在图13中，在像素区域1500中设置开关TFT 1401、驱动TFT 1403、辅助电容器1402和发光元件1405。在信号线1410上设置二极管1561和1562。基于以上的实施例，以与开关TFT 1401和驱动TFT 1403类似的方式制造二极管1561和1562，并且具有栅电极、半导体层、源电极、漏电极等。二极管1561和1562通过将栅电极与漏电极或源电极

连接而作为二极管工作。

通过使用与栅电极相同的层形成与二极管1561和1562连接的共用的等势线1554和1555。因此，为了将共用的等势线1554和1555与二极管的源电极或漏电极连接，必须在栅绝缘层中形成接触孔。

在扫描线1414上设置的二极管1563和1564具有类似的结构。并且，共用的等势线1565和1566具有类似的结构。

这样，可以根据本发明在输入阶段中同时形成保护二极管。并且，保护二极管的设置不限于此，并且可以在驱动电路与像素之间设置它们。

在图14A中说明使用图12E所示的等效电路的情况下的像素部分的顶视图。另外，在图14B中示出与图12E中的等效电路相同的等效电路。图10A、图10B、图11A和图11B所示的各半导体器件与各个驱动TFT 1403对应。图10A、图10B、图11A和图11B表示沿图14A和图14B中的线X-Y切取的截面图。通过使用第一导电膜形成电源线1411、信号线1410和开关TFT 1401的源电极和漏电极，并且通过使用第二导电膜形成驱动TFT 1403的源电极和漏电极。

通过与驱动TFT 1403相同的方法制造开关TFT 1401。开关TFT 1401的漏电极和驱动TFT 1403的栅电极40通过在与栅绝缘膜42相同的层中的绝缘膜中形成的接触孔相互电连接。

通过使用驱动TFT 1403的栅电极延伸的部分、电源线1411和与栅绝缘膜42相同的层中的绝缘膜形成辅助电容器1402。

在隔离壁81的开口部分中形成发光区域1420。虽然没有示出，但在发光区域1420的附近形成隔离壁81。发光区域1420的角部分可被修圆。通过使隔离壁81的开口部分的角部分被修圆，发光区域1420的角部分可被修圆。当进行使用等离子的干蚀刻以处理隔离壁81时，可以通过使角部分被修圆来抑制由于异常放电导致的细粒子的产生。

本实施例可在适当情况下与以上的实施例的适当的结构组合。

[实施例7]

作为具有安装了在以上的实施例中作为例子示出的模块的根据

本发明的半导体器件的电子装置，可以举出诸如摄像机或数字照相机的照相机、护目镜型显示器（头戴式显示器）、导航系统、音频再生装置（例如，汽车音频部件）、计算机、游戏机、便携式信息终端（例如，移动计算机、蜂窝电话、便携式游戏机或电子图书等）和配备了记录介质的图像再生装置（特别是可再生诸如数字通用盘（DVD）的记录介质的内容并且具有用于显示存储在其中的图像的显示器的装置）等。在图15A~15E和图16中示出这些电子装置的具体例子。

图15A表示包含外壳3001、显示区域3003和扬声器3004等的用于电视接收机或个人计算机等的监视器。在显示区域3003中设置有源矩阵显示器。显示区域3003的各像素包含根据本发明制造的半导体器件。通过使用具有该结构的本发明的半导体器件，可以获得具有更小的特性劣化的电视机。

图15B表示包含主体3101、外壳3102、显示区域3103、音频输入部分3104、音频输出部分3105、操作键3106和天线3108的蜂窝电话。在显示区域3103中设置有源矩阵显示器。显示区域3103的各像素包含根据本发明制造的半导体器件。通过使用具有该结构的本发明的半导体器件，可以获得具有更小的特性劣化的蜂窝电话。

图15C表示包含主体3201、外壳3202、显示区域3203、键盘3204、外部连接端口3205和指示鼠标3206的计算机。在显示区域3203中设置有源矩阵显示器。显示区域3203的各像素包含根据本发明制造的半导体器件。通过使用具有该结构的本发明的半导体器件，可以获得具有更小的特性劣化的计算机。

图15D表示包含主体3301、显示区域3302、开关3303、操作键3304和红外端口3305等的移动计算机。在显示区域3302中设置有源矩阵显示器。显示区域3302的各像素包含根据本发明制造的半导体器件。通过使用具有该结构的本发明的半导体器件，可以获得具有更小的特性劣化的移动计算机。

图15E表示包含外壳3401、显示区域3402、扬声器3403、操作键3404和记录介质嵌入部分3405等的便携式游戏机。在显示区域3402中

设置有源矩阵显示器。显示区域3402的各像素包含根据本发明制造的半导体器件。通过使用具有该结构的本发明的半导体器件，可以获得具有更小的特性劣化的便携式游戏机。

图16表示包含主体3110、像素区域3111、驱动器IC 3112、接收装置3113和膜电池3114等的柔性显示器。接收装置可从上述的蜂窝电话的红外通信端口3107接收信号。在像素区域3111中设置有源矩阵显示器。像素区域3111的各像素包含根据本发明制造的半导体器件。通过使用具有该结构的本发明的半导体器件，可以获得具有更小的特性劣化的柔性显示器。

如上所述，本发明的应用范围是极宽的，并且本发明可被应用于所有领域中的电子装置。

本申请基于2005年11月15日在日本专利局提交的日本专利申请No. 2005-329806，在此加入其全部内容作为参考。

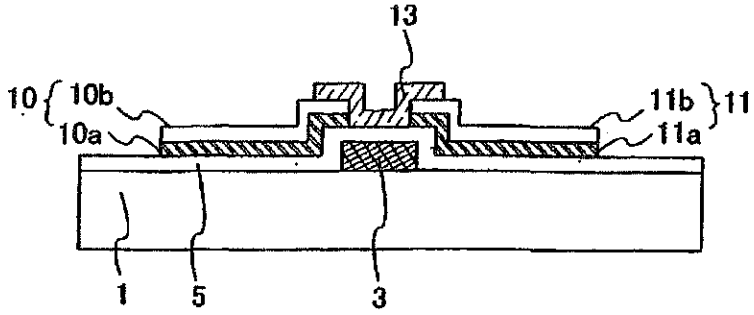


图1A

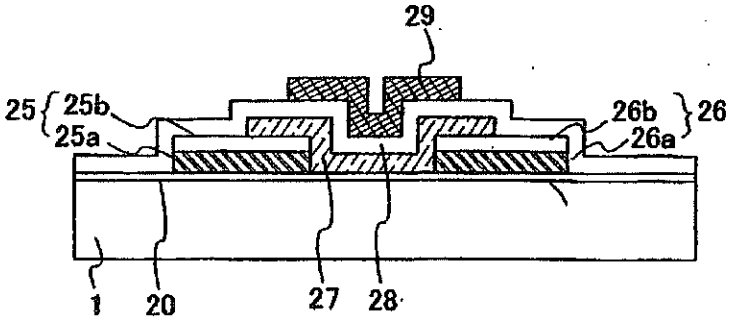


图1B

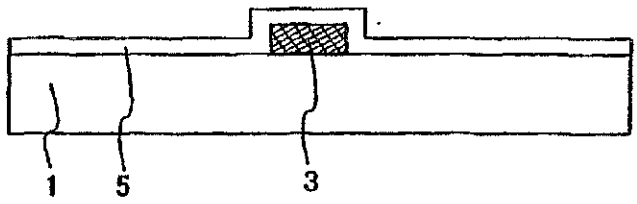


图2A

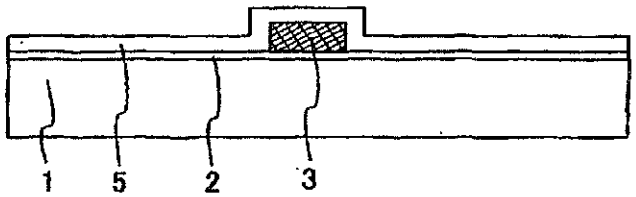


图2B

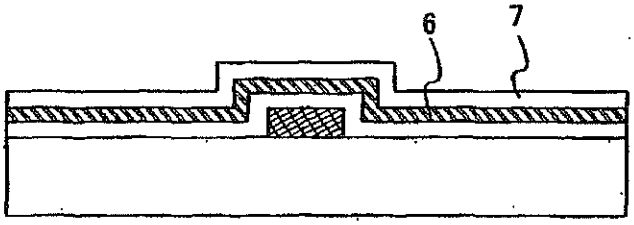


图2C

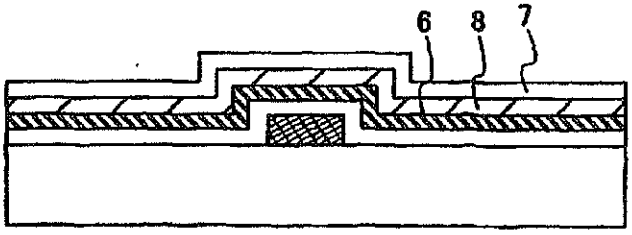


图2D

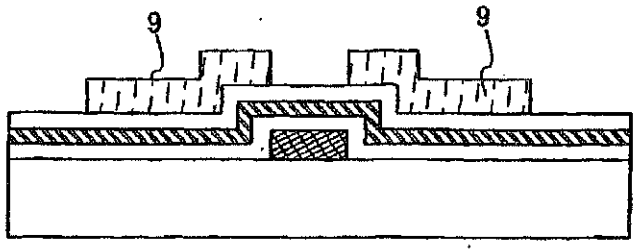


图 3A

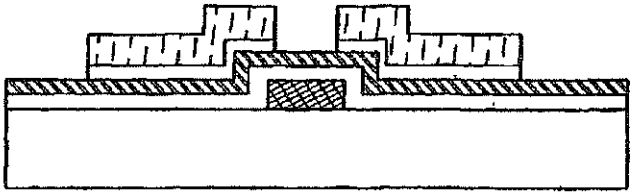


图 3B

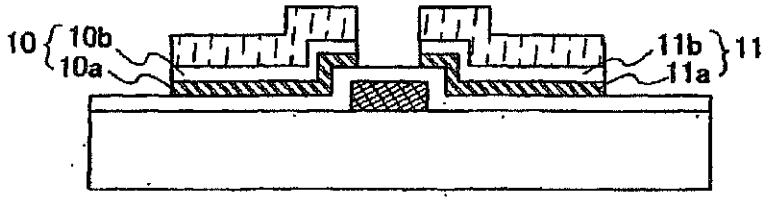


图 3C

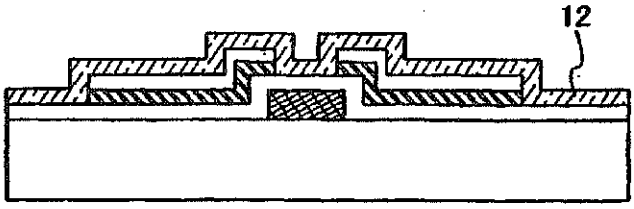


图 3D

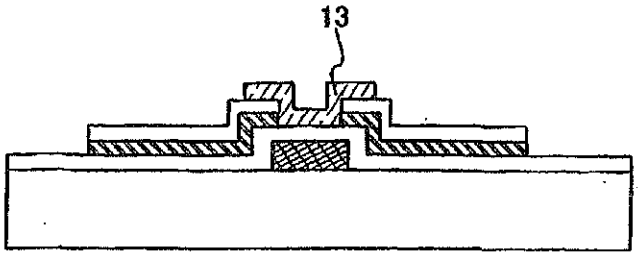


图4A

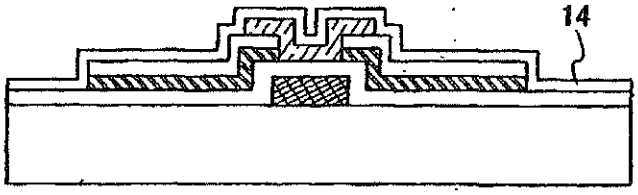


图4B

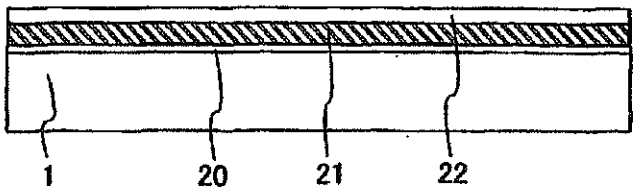


图5A

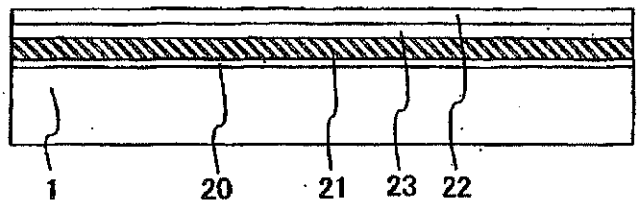


图5B

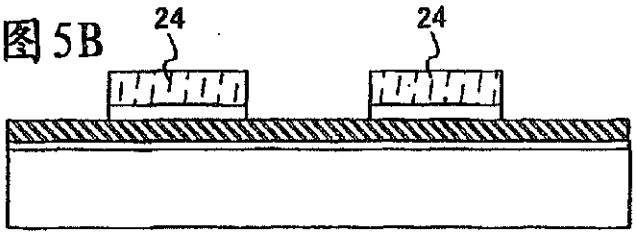


图5C

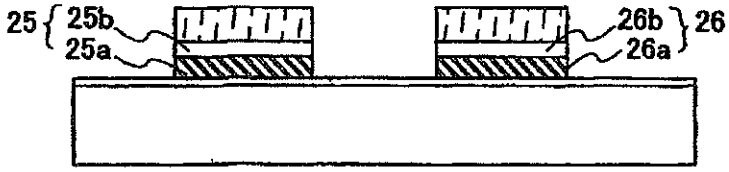


图5D

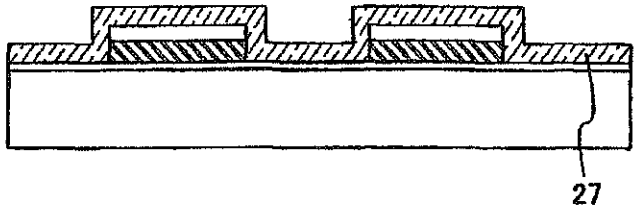


图6A

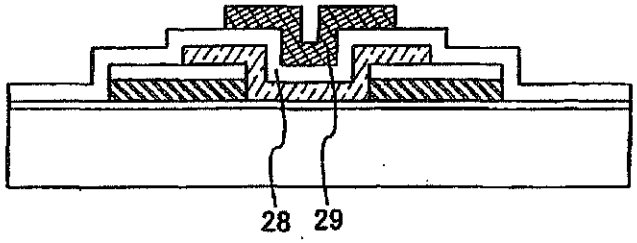


图6B

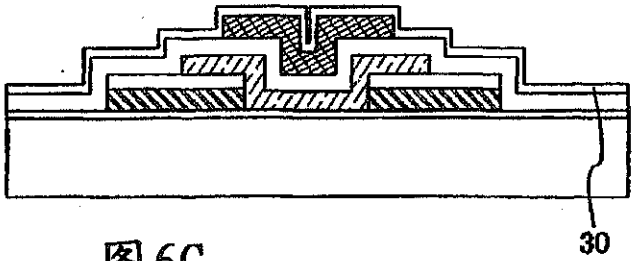


图6C

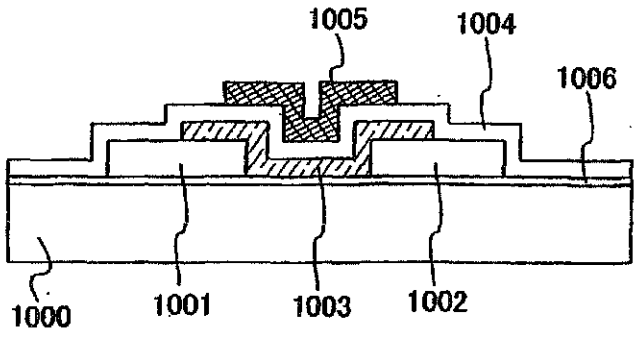

1005
1004
1006
1000
1001
1003
1002

图7A

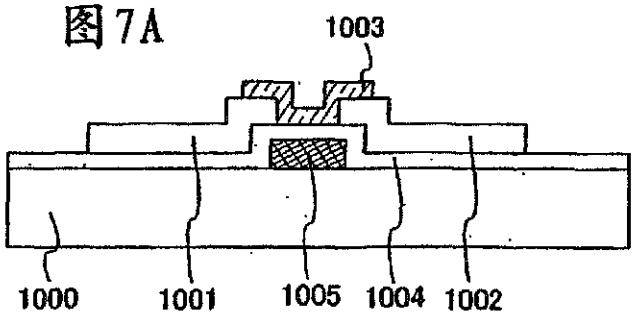

1003
1000
1001
1005
1004
1002

图7B

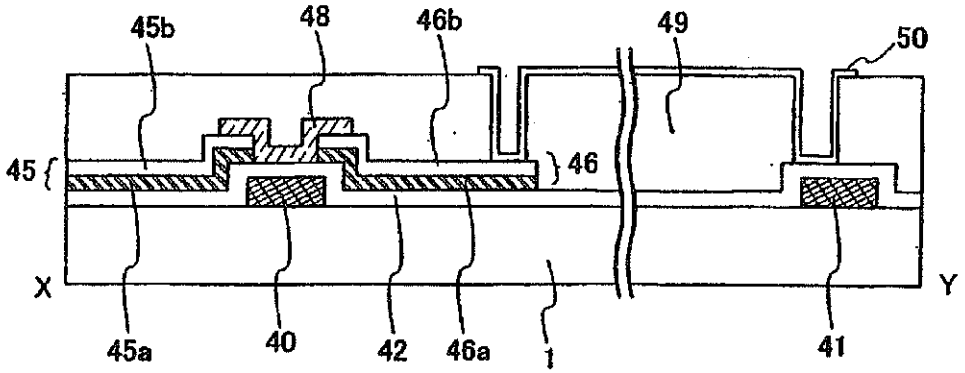


图8A

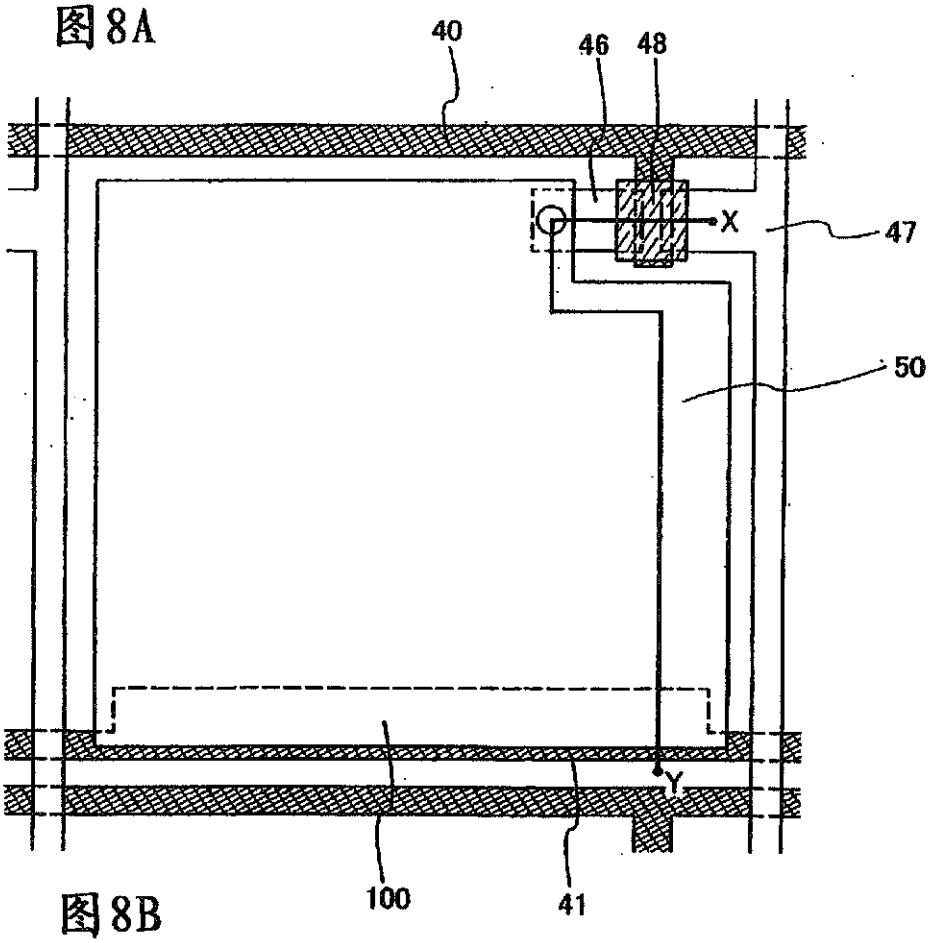


图8B

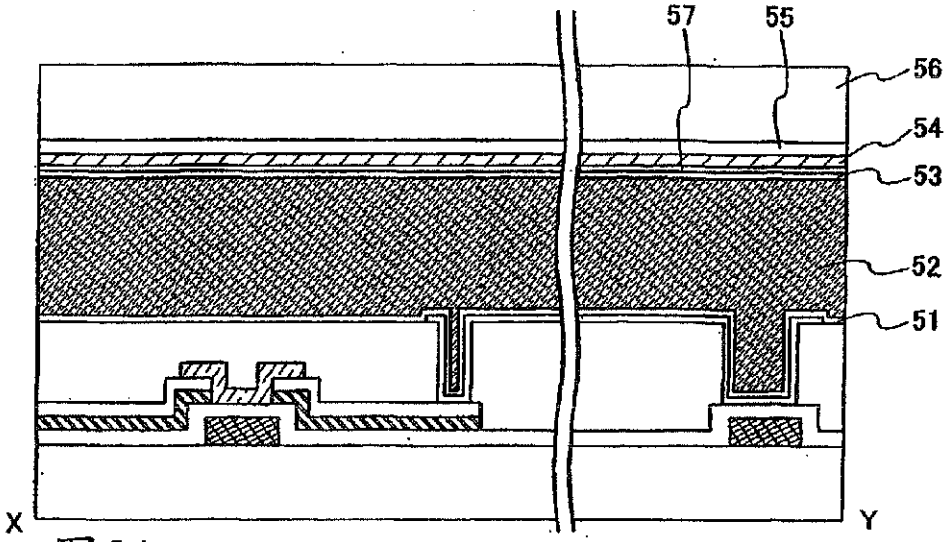

57
55
56
54
53
52
51
X
Y

图9A

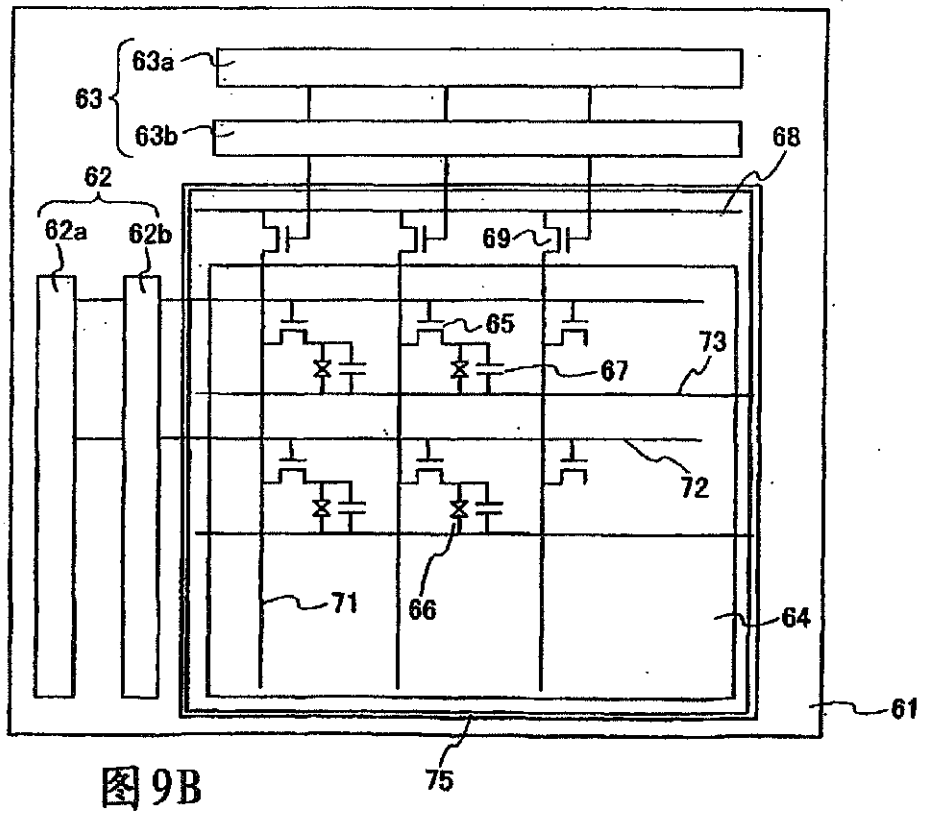

63a
63
63b
68
62
62a
62b
69
65
67
73
72
71
66
64
61
75

图9B

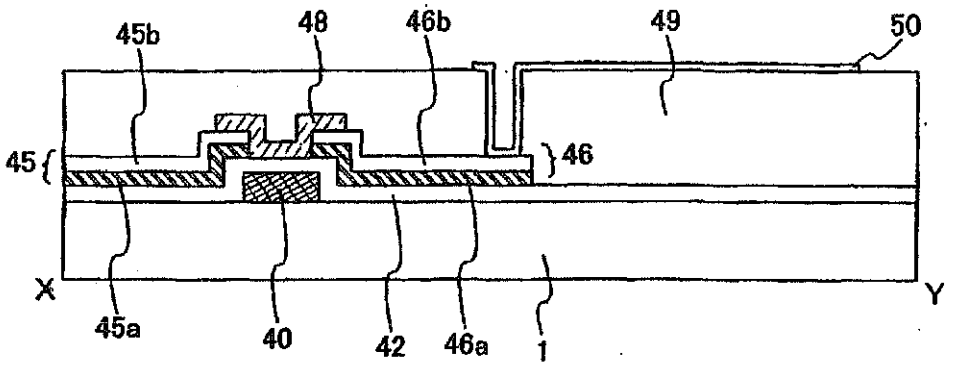


图10A

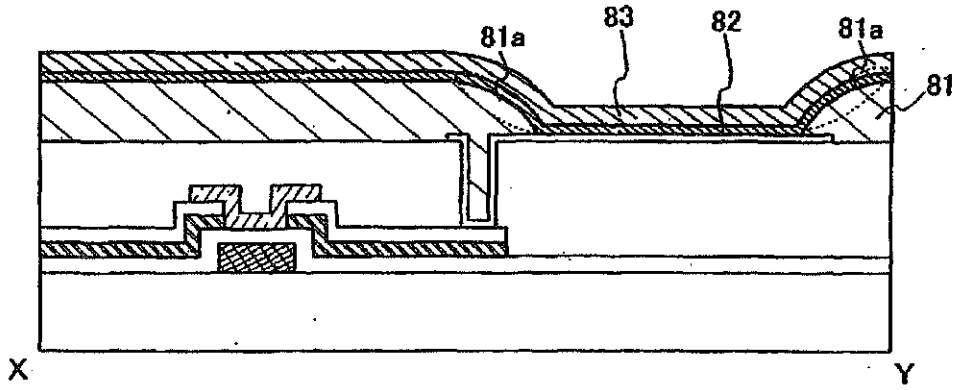


图10B

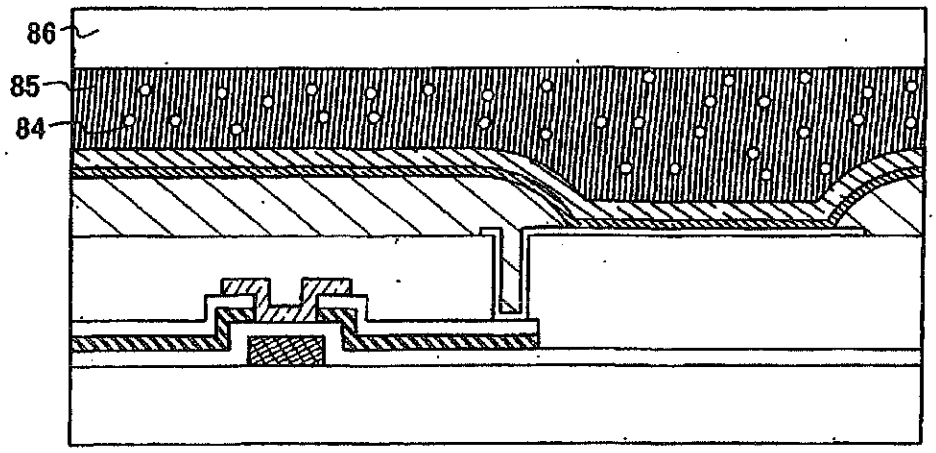


图11A

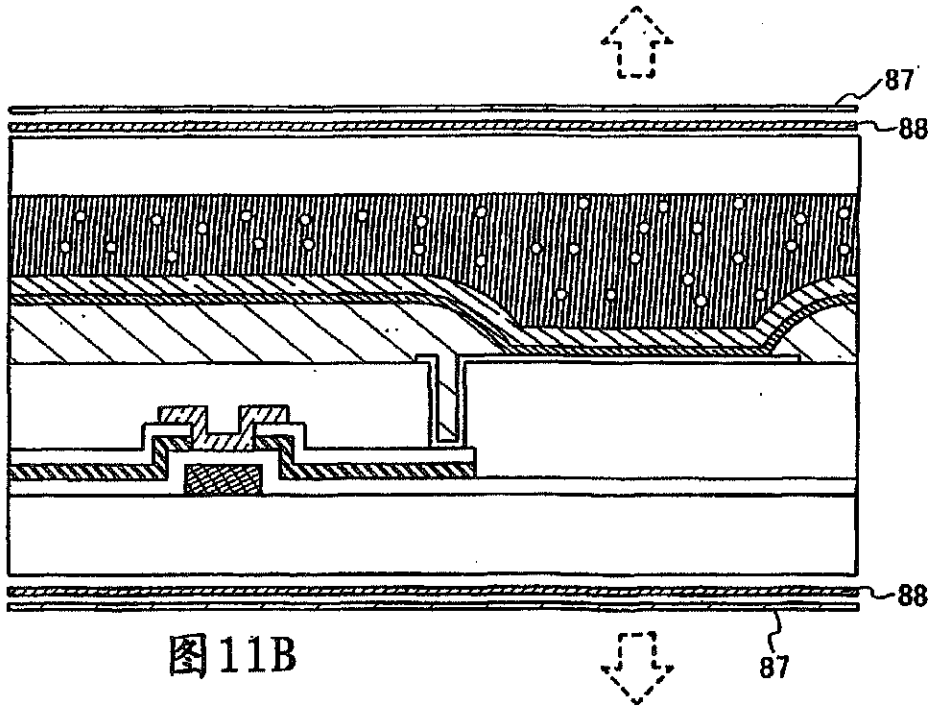


图11B

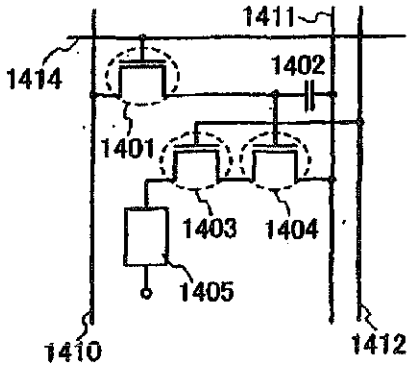


图12A

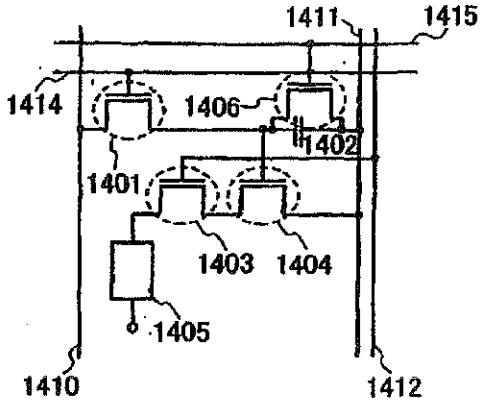


图12B

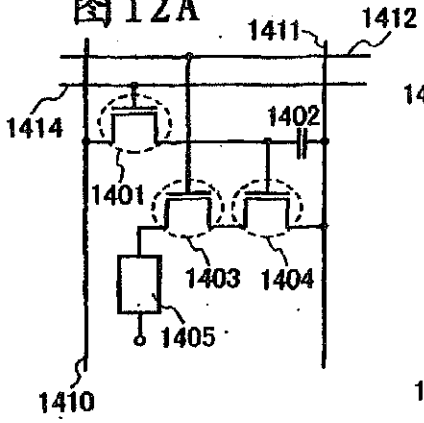


图12C

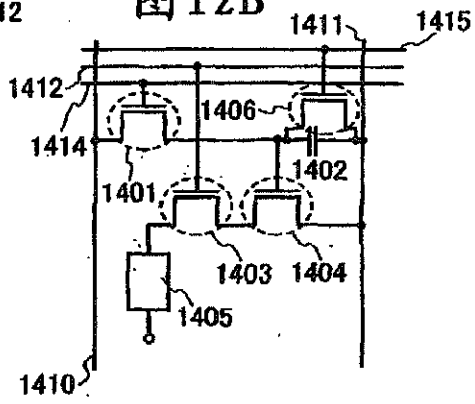


图12D

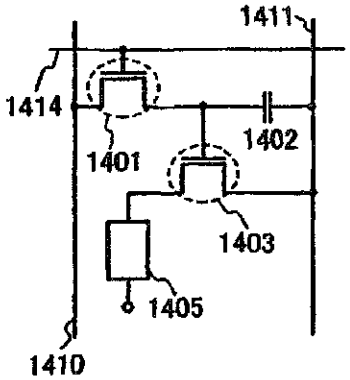


图12E

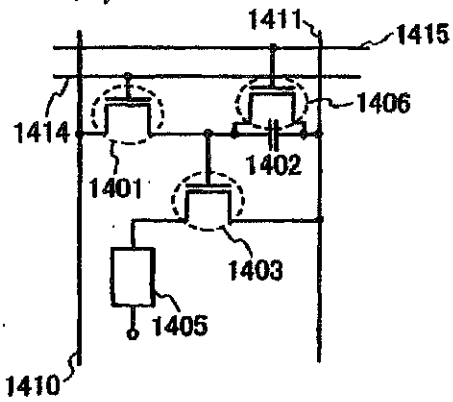


图12F

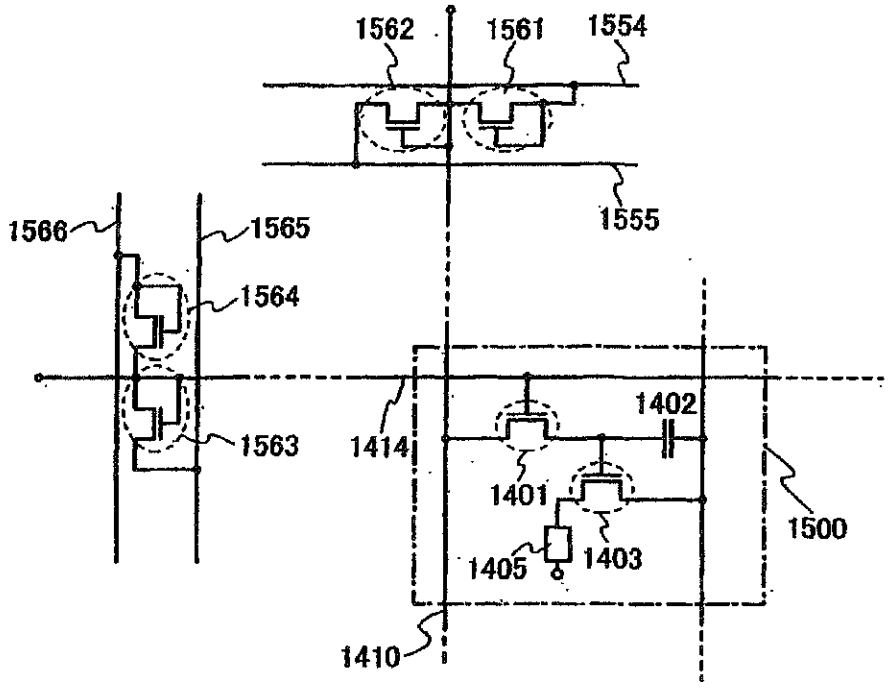

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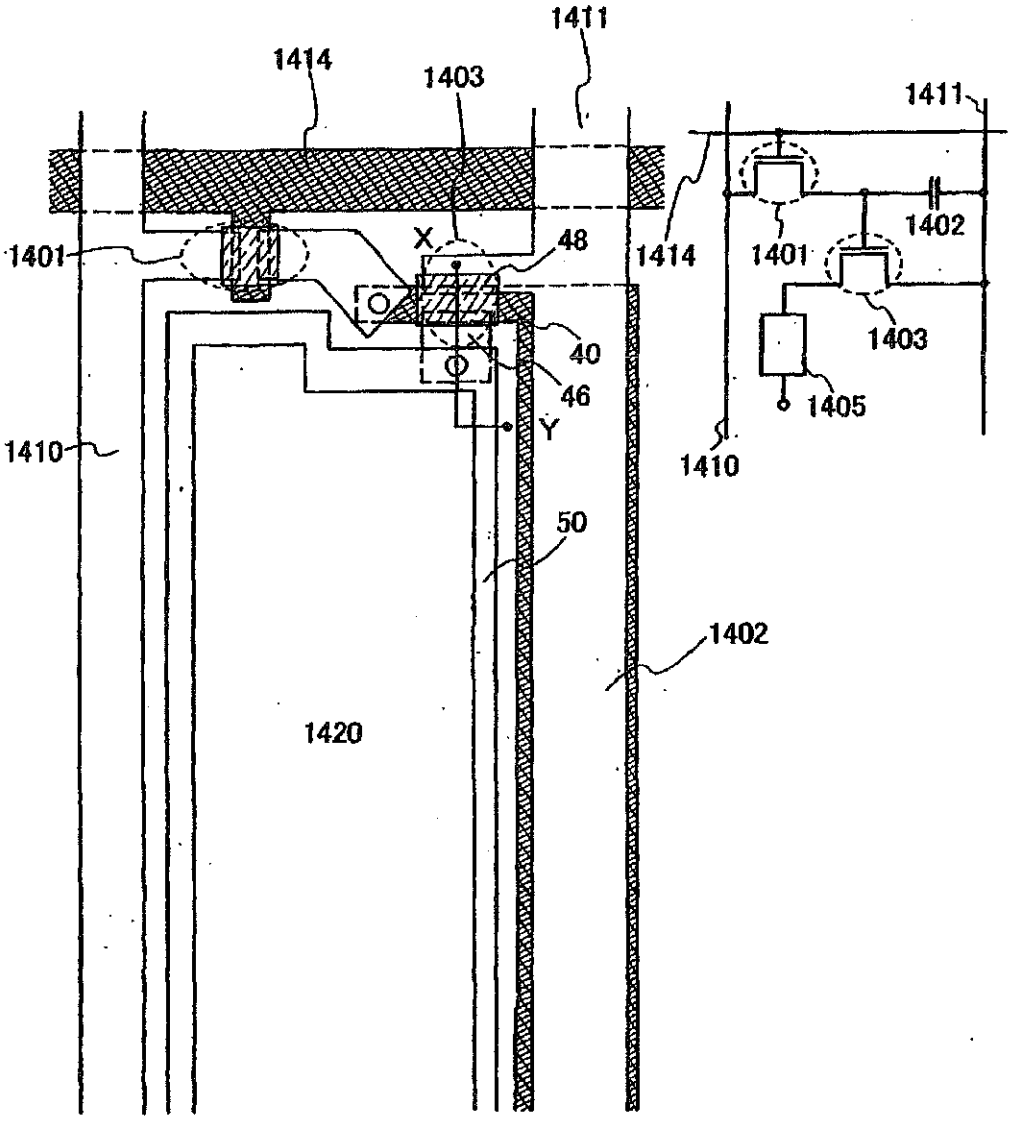
图13


1411
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46
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1410
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图14A 图14B

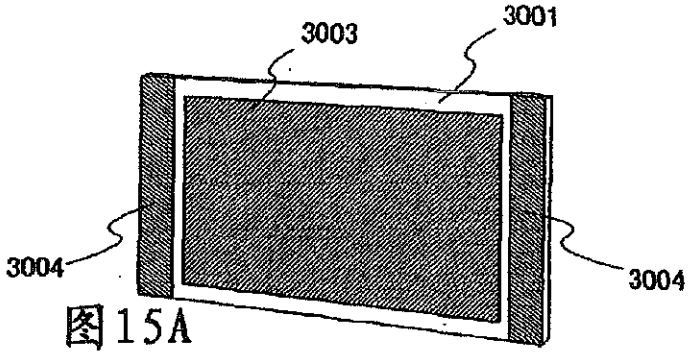

图15A

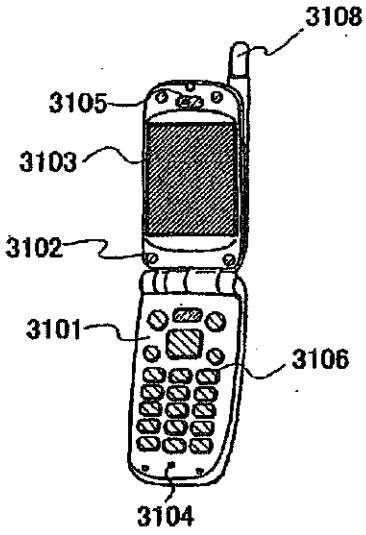

图15B

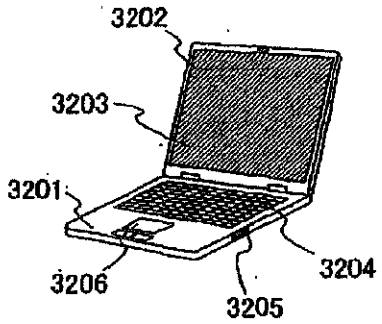

图15C

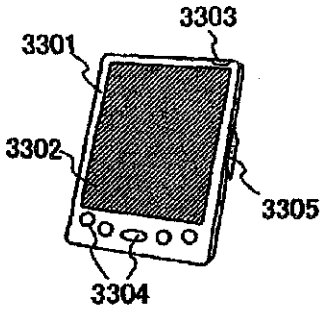

图15D

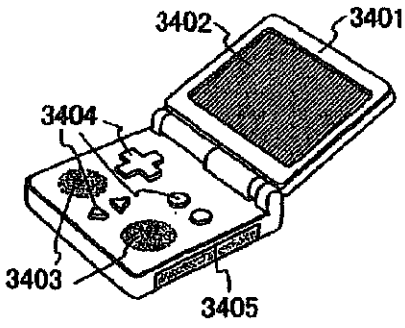

图15E

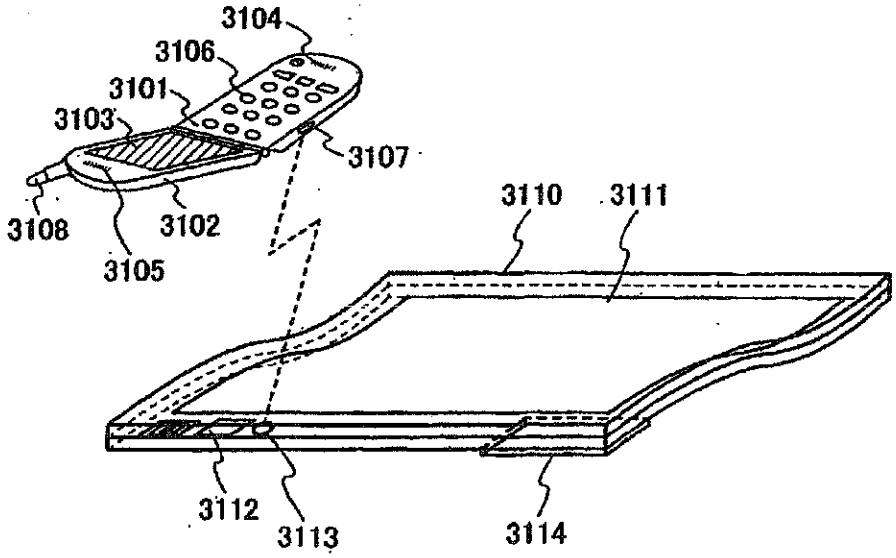
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图16

附图标记的解释

1：衬底；2：绝缘膜；3：栅电极；5：栅绝缘膜；6：第一导电膜；7：第二导电膜；8：第三导电膜；9：光刻胶掩模；10：源电极；10a：源电极、第一导电膜；10b：源电极、第二导电膜；11：漏电极；11a：漏电极、第一导电膜；11b：漏电极、第二导电膜；12：半导体膜；13：岛状形状半导体膜；14：绝缘膜；20：绝缘膜；21：第一导电膜；22：第二导电膜；23：第三导电膜；24：光刻胶掩模；25：源电极；25a：源电极、第一导电膜；25b：源电极、第二导电膜；26：漏电极；26a：漏电极、第一导电膜；26b：漏电极、第二导电膜；27：半导体膜；28：栅绝缘膜；29：栅电极；30：绝缘膜；40：栅电极、栅极引线；41：辅助电容器引线；42：栅绝缘膜；45：源电极；45a：源电极；45b：源电极；46：漏电极；46a：漏电极；46b：漏电极；47：源极引线；48：半导体膜；49：绝缘膜；50：像素电极；51：对准引线；52：液晶组合物；53：取向膜；54：保护绝缘膜；55：滤色片；56：相对衬底；61：衬底；62：栅极引线驱动电路；62a：移位寄存器；62b：缓冲器；63：源极引线驱动电路；63a：移位寄存器；63b：缓冲器；64：有源矩阵部分；65：半导体器件；66：液晶部分；67：辅助电容器；68：视频线；69：模拟开关；71：源极引线；72：栅极引线；73：辅助电容器引线；75：密封剂；81：隔离壁；81a：端面；82：包含发光衬底的层；83：相对电极；84：干燥剂；85：树脂；86：相对衬底；87：保护膜；88：偏振片；100：辅助电容器；1000：衬底；1001：源电极；1002：漏电极；1003：半导体膜；1004：栅绝缘膜；1005：栅电极；1006：基膜；1401：开关TFT；1402：辅助电容器；1403：驱动TFT；1404：

电流控制TFT；1405：发光元件；1406：TFT；1410：信号线；1411：电源线；1412：电源线；1414：扫描线；1415：扫描线；1420：发光区域；1500：像素部分；1554：共用的等势线；1555：共用的等势线；1561：二极管；1562：二极管；1563：二极管；1564：二极管；1565：共用的等势线；1566：共用的等势线；3001：外壳；3003：显示区域；3004：扬声器；3101：主体；3102：外壳；3102：外壳；3103：显示区域；3104：音频输入部分；3105：音频输出部分；3106：操作键；3107：红外通信端口；3108：天线；3110：主体；3111：像素部分；3112：驱动器IC；3113：接收装置；3114：膜电池；3201：主体；3202：外壳；3203：显示区域；3204：键盘；3205：外部连接端口；3206：指示鼠标；3301：主体；3302：显示区域；3303：开关；3304：操作键；3305：红外端口；3401：外壳；3402：显示区域；3403：扬声器；3404：操作键；3405：记录介质嵌入部分。

Attorney Docket No. 0756-10065

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 7085
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2812
Serial No. 13/763,874	)	
Filed: February 11, 2013	)	
For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

CN101283444 was cited by the Chinese Patent Office in counterpart Chinese Patent Application No. 200910206768.3 in an Office Action mailed March 15, 2013.

U.S. Patent Nos. 8,134,156; 8,158,464 and 8,368,079 and U.S. Publication Nos. 2009/0186445; 2009/0189155; 2009/0189156 and 2010/0003783 and WO2007/058329 are in the family of CN101283444. These references were not directly cited by the foreign patent office, but are submitted herewith for consideration by the Examiner.

Although no fee is due for this Information Disclosure Statement, the Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

Attorney Docket No. 0756-10065

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 7085
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2812
Serial No. 13/763,874	)	
Filed: February 11, 2013	)	
For: SEMICONDUCTOR DEVICE	)	
AND MANUFACTURING	)	
METHOD THEREOF	)	

RESPONSE TO NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION AND PRELIMINARY AMENDMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the *Notice to File Missing Parts of Nonprovisional Application, under 37 C.F.R. § 1.53(b)* dated March 8, 2013, submitted herewith are the fees due under 37 CFR 1.16 (Statutory basic filing fee - $280; Search fee - $600; Examination fee - $720; Surcharge - $140).

Furthermore, please consider the following amendments and remarks in connection with the above-identified application.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims, which begins on page 3 of this paper.

Remarks begin on page 9 of this paper.

Amendments to the Specification:

Please replace paragraph [0263] with the following amended paragraph:

[0263] A driver circuit for driving a pixel portion is formed using an inverter circuit, a capacitor, a resistor, and the like. When two n-channel TFTs are combined to form an inverter circuit, there are two types of combinations: a combination of an enhancement type transistor and a ~~depression type~~ depletion type transistor (hereinafter, a circuit formed by such a combination is referred to as an "EDMOS circuit") and a combination of enhancement type TFTs (hereinafter, a circuit formed by such a combination is referred to as an "EEMOS circuit"). Note that when the threshold voltage of the n-channel TFT is positive, the n-channel TFT is defined as an enhancement type transistor, while when the threshold voltage of the n-channel TFT is negative, the n-channel TFT is defined as a ~~depression type~~ depletion type transistor, and this specification follows the above definitions.

Please replace paragraph [0275] with the following amended paragraph:

[0275] Further, FIG. 32B illustrates an equivalent circuit of the EDMOS circuit. The circuit connection illustrated in FIGS. 32A and 32C corresponds to that illustrated in FIG. 32B. Illustrated is an example in which the first thin film transistor 1430 is an enhancement-type n-channel transistor and the second thin film transistor 1431 is a ~~depression type~~ depletion-type n-channel transistor.

Listing of Claims:

1. (Canceled)

2. (New) A semiconductor device comprising:

a glass substrate;

a transistor over the glass substrate, the transistor comprising:

a gate electrode;

a first insulating layer over the gate electrode;

an oxide semiconductor layer over the first insulating layer; and

a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer;

a second insulating layer over the transistor;

a pixel electrode over the second insulating layer;

a third insulating layer over the pixel electrode;

a light-emitting layer over the pixel electrode and the third insulating layer;

an electrode over the light-emitting layer,

wherein the oxide semiconductor layer comprises indium and zinc,

wherein each of a side surface of the source electrode and a side surface of the drain electrode has a tapered shape,

wherein a first angle of the tapered shape that is made between the side surface of the source electrode and an upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°, and

wherein a second angle of the tapered shape that is made between the side surface of the drain electrode and the upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°.

3. (New) The semiconductor device according to claim 2, wherein each of the

source electrode and the drain electrode is in contact with an upper surface of the first insulating layer.

4. (New) The semiconductor device according to claim 2, wherein the oxide semiconductor layer is over the source electrode and the drain electrode.

5. (New) The semiconductor device according to claim 2, wherein the oxide semiconductor layer is in contact with each of the side surface of the source electrode and the side surface of the drain electrode.

6. (New) The semiconductor device according to claim 2, wherein the oxide semiconductor layer further comprises gallium.

7. (New) The semiconductor device according to claim 2, wherein the pixel electrode is in contact with the drain electrode.

8. (New) The semiconductor device according to claim 2, wherein the oxide semiconductor layer is a non-single-crystal film.

9. (New) The semiconductor device according to claim 2, further comprising:

a first buffer layer between the oxide semiconductor layer and the source electrode; and

a second buffer layer between the oxide semiconductor layer and the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer.

10. (New) A semiconductor device comprising:

a glass substrate;

a transistor over the glass substrate, the transistor comprising:

a gate electrode;

a first insulating layer over the gate electrode;

an oxide semiconductor layer over the first insulating layer; and

a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer;

a second insulating layer over the transistor;

a pixel electrode over the second insulating layer;

a third insulating layer over the pixel electrode;

a light-emitting layer over the pixel electrode and the third insulating layer;

an electrode over the light-emitting layer,

wherein the oxide semiconductor layer comprises indium and zinc,

wherein each of a side surface of the source electrode and a side surface of the drain electrode has a step in a lower portion thereof,

wherein a first angle of the step that is made between the side surface of the source electrode and an upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°, and

wherein a second angle of the step that is made between the side surface of the drain electrode and the upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°.

11. (New) The semiconductor device according to claim 10, wherein each of the source electrode and the drain electrode is in contact with an upper surface of the first insulating layer.

12. (New) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is over the source electrode and the drain electrode.

13. (New) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is in contact with each of the side surface of the source electrode and the side surface of the drain electrode.

14. (New) The semiconductor device according to claim 10, wherein the oxide semiconductor layer further comprises gallium.

15. (New) The semiconductor device according to claim 10, wherein the pixel electrode is in contact with the drain electrode.

16. (New) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is a non-single-crystal film.

17. (New) The semiconductor device according to claim 10, further comprising:

a first buffer layer between the oxide semiconductor layer and the source electrode; and

a second buffer layer between the oxide semiconductor layer and the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer.

18. (New) A semiconductor device comprising:

a glass substrate;

a transistor over the glass substrate, the transistor comprising:

a gate electrode;

a first insulating layer over the gate electrode;

an oxide semiconductor layer over the first insulating layer; and

a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer;

a second insulating layer over the transistor;

a pixel electrode over the second insulating layer;

a third insulating layer over the pixel electrode;

a light-emitting layer over the pixel electrode and the third insulating layer;

an electrode over the light-emitting layer,

wherein the oxide semiconductor layer comprises indium and zinc,

wherein a first angle between a surface of the glass substrate and a side surface of a first bottom edge of the source electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the source electrode, and

wherein a second angle between the surface of the glass substrate and a side surface of a second bottom edge of the drain electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the drain electrode.

19. (New) The semiconductor device according to claim 18, wherein each of the source electrode and the drain electrode is in contact with an upper surface of the first insulating layer.

20. (New) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is over the source electrode and the drain electrode.

21. (New) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is in contact with each of the side surface of the source electrode and the side surface of the drain electrode.

22. (New) The semiconductor device according to claim 18, wherein the oxide semiconductor layer further comprises gallium.

23. (New) The semiconductor device according to claim 18, wherein the pixel electrode is in contact with the drain electrode.

24. (New) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is a non-single-crystal film.

25. (New) The semiconductor device according to claim 18, further comprising:

a first buffer layer between the oxide semiconductor layer and the source electrode; and

a second buffer layer between the oxide semiconductor layer and the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer.

REMARKS

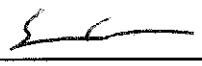
This *Preliminary Amendment* has been filed to correct minor typographical and grammatical errors in the specification as was done in the parent application. Specifically, in paragraphs [0263] and [0275], "depression type" has been replaced with "depletion-type." Furthermore, claim 1 has been canceled and new claims 2-25 have been added to better recite the features of the present invention.

No new matter has been added. Examination on the merits is requested.

If the Examiner feels that any further discussions about this case would be beneficial, the Examiner is invited to contact the undersigned.

Although no fee is due for this submission, the Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



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Electronic Patent Application Fee Transmittal

Application Number:	13763874
Filing Date:	11-Feb-2013
Title of Invention:	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Filer:	Eric J. Robinson
Attorney Docket Number:	0756-10065

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Claims in Excess of 20	1202	4	80	320
Miscellaneous-Filing:				
Late Filing Fee for Oath or Declaration	1051	1	140	140

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2060**

Electronic Acknowledgement Receipt	
EFS ID:	15713303
Application Number:	13763874
International Application Number:	
Confirmation Number:	7085
Title of Invention:	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Adele Stamper
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10065
Receipt Date:	07-MAY-2013
Filing Date:	11-FEB-2013
Time Stamp:	16:41:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$2060
RAM confirmation Number	3501
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Preliminary Amendment	NFMP_PAM_08MAY2013_075610065.pdf	1054134 92427f9b87880d57ea6da45a2925e9e02bf0132f	no	9
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	38345 ec3c684d51f306b2ae67c88c0f1bd9199f12a01c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1092479		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/763,874	Filing Date 02/11/2013	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	05/07/2013	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 24	Minus	** 20	= 4	X $80 =	320
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**320**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/CORALIA BETANCOURT/

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/763,874

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	24 minus 20 =	* 4			OR	x 80 =	320
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1920

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/763,874	02/11/2013	Shunpei YAMAZAKI	0756-10065

CONFIRMATION NO. 7085

31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

NOTICE

OC000000061156304

Date Mailed: 05/13/2013

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  All
  Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/763,874	02/11/2013	2812	2060	0756-10065	24	3

CONFIRMATION NO. 7085

UPDATED FILING RECEIPT

31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

OC000000061156303

Date Mailed: 05/13/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Shunpei YAMAZAKI, Setagaya, JAPAN;
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Assignment For Published Patent Application

SEMICONDUCTOR ENERGY LABORATORY CO., LTD., Atsugi-shi, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 31780

Domestic Priority data as claimed by applicant

This application is a CON of 12/613,769 11/06/2009 PAT 8373164 *
which is a CON of 12/606,262 10/27/2009 ABN
(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
JAPAN 2008-287187 11/07/2008

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 03/04/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/763,874**

Projected Publication Date: 08/22/2013

Non-Publication Request: No

Early Publication Request: No
TItle

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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日　本　国　特　許　庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日 Date of Application:	２００８年１１月　７日
出願番号 Application Number:	特願２００８－２８７１８７
パリ条約による外国への出願に用いる優先権の主張の基礎となる出願の国コードと出願番号 The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is	ＪＰ２００８－２８７１８７
出願人 Applicant(s):	株式会社半導体エネルギー研究所

２０１３年　５月２４日

特許庁長官
Commissioner,
Japan Patent Office　深野弘行

【書類名】　特許願
【整理番号】　P011986
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【あて先】　特許庁長官　鈴木　隆史　殿
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　【代表者】　山崎　舜平
【手数料の表示】
　【予納台帳番号】　002543
　【納付金額】　15,000円
【提出物件の目録】
　【物件名】　特許請求の範囲　1
　【物件名】　明細書　1
　【物件名】　図面　1
　【物件名】　要約書　1

【書類名】特許請求の範囲
【請求項１】
絶縁表面を有する基板上にゲート電極と、
前記ゲート電極上に絶縁層と、
前記絶縁層上にソース電極及びドレイン電極と、
前記ソース電極の側面と、該側面と向かい合う前記ドレイン電極の側面の間に前記ゲート電極と前記絶縁層を介して重なる酸化物半導体層とを有し、
前記基板の基板面と前記ソース電極の側面とがなす角と、前記基板の基板面と前記ドレイン電極の側面とがなす角とが２０°以上９０°未満であることを特徴とする半導体装置。
【請求項２】
請求項１において、前記ソース電極及び前記ドレイン電極の上面にバッファ層を有し、該バッファ層上に前記酸化物半導体層を有する半導体装置。
【請求項３】
請求項１または請求項２において、前記酸化物半導体層における前記ソース電極の側面及び前記ドレイン電極の側面と重なる領域は、電界集中緩和領域である半導体装置。
【請求項４】
請求項１乃至３のいずれか一において、前記酸化物半導体層は、インジウム、ガリウム、及び亜鉛を含むことを特徴とする半導体装置。
【請求項５】
絶縁表面を有する基板上にゲート電極と、
前記ゲート電極上に絶縁層と、
前記絶縁層上にソース電極及びドレイン電極と、
前記ソース電極の側面と、該側面と向かい合う前記ドレイン電極の側面の間に前記ゲート電極と前記絶縁層を介して重なる酸化物半導体層とを有し、
前記基板の基板面と前記ソース電極下端部の側面とがなす角と、前記基板の基板面と前記ドレイン電極下端部の側面とがなす角とが２０°以上９０°未満であることを特徴とする半導体装置。
【請求項６】
請求項５において、前記基板の基板面と前記ソース電極下端部の側面とがなす角は、前記基板の基板面とソース電極上端部の側面とがなす角と異なることを特徴とする半導体装置。
【請求項７】
請求項５または請求項６において、前記基板の基板面と前記ドレイン電極下端部の側面とがなす角は、前記基板の基板面とドレイン電極上端部の側面とがなす角と異なることを特徴とする半導体装置。
【請求項８】
請求項５乃至７のいずれか一において、前記ソース電極の側面及び前記ドレイン電極の側面は少なくとも一部に曲面を有していることを特徴とする半導体装置。
【請求項９】
請求項５乃至８のいずれか一において、前記ソース電極及び前記ドレイン電極の上面にバッファ層を有し、該バッファ層上に前記酸化物半導体層を有する半導体装置。
【請求項１０】
請求項５乃至９のいずれか一において、前記酸化物半導体層における前記ソース電極の側面及び前記ドレイン電極の側面と重なる領域は、電界集中緩和領域である半導体装置。
【請求項１１】
請求項５乃至１０のいずれか一において、前記酸化物半導体層は、インジウム、ガリウム、及び亜鉛を含むことを特徴とする半導体装置。
【請求項１２】
絶縁表面を有する基板上にゲート電極を形成し、
前記ゲート電極を覆うゲート絶縁層を形成し、

前記ゲート絶縁層上に導電層とバッファ層とを大気にふれることなく積層形成し、
前記バッファ層及び前記導電層を選択的にエッチングして前記基板の基板面となす角が２０°以上９０°未満である側面を有するソース電極及びドレイン電極を形成し、
前記ゲート絶縁層、前記ソース電極、及び前記ドレイン電極上に酸化物半導体層を形成する半導体装置の作製方法。
【請求項１３】
請求項１２において前記酸化物半導体層は、インジウム、ガリウム、及び亜鉛を含むことを特徴とする半導体装置の作製方法。
【請求項１４】
請求項１２または請求項１３において、前記バッファ層は、インジウム、ガリウム、及び亜鉛を含むことを特徴とする半導体装置の作製方法。
【請求項１５】
請求項１２乃至請求項１４のいずれか一において、前記酸化物半導体層と前記バッファ層は同じ組成のターゲットを用いることを特徴とする半導体装置の作製方法。

【書類名】明細書
【発明の名称】半導体装置およびその作製方法
【技術分野】
【０００１】
酸化物半導体を用いる表示装置及びその製造方法に関する。
【背景技術】
【０００２】
液晶表示装置に代表されるように、ガラス基板等の平板に形成される薄膜トランジスタは、アモルファスシリコン、多結晶シリコンによって作製されている。アモルファスシリコンを用いた薄膜トランジスタは、電界効果移動度が低いもののガラス基板の大面積化に対応することができ、一方、結晶シリコンを用いた薄膜トランジスタは電界効果移動度が高いものの、レーザアニール等の結晶化工程が必要であり、ガラス基板の大面積化には必ずしも適応しないといった特性を有している。
【０００３】
これに対し、酸化物半導体を用いて薄膜トランジスタを作製し、電子デバイスや光デバイスに応用する技術が注目されている。例えば、酸化物半導体膜として酸化亜鉛、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系酸化物半導体を用いて薄膜トランジスタを作製し、画像表示装置のスイッチング素子などに用いる技術が特許文献１及び特許文献２で開示されている。
【特許文献１】特開２００７－１２３８６１号公報
【特許文献２】特開２００７－０９６０５５号公報
【発明の開示】
【発明が解決しようとする課題】
【０００４】
ボトムゲート型の薄膜トランジスタにおいて、ソース電極とドレイン電極間に生じる恐れのある電界集中を緩和し、スイッチング特性の劣化を抑える構造及びその作製方法を提供することを課題の一とする。
【０００５】
また、酸化物半導体層の被覆性を向上させる構造およびその作製方法を提供することも課題の一とする。
【課題を解決するための手段】
【０００６】
ソース電極及びドレイン電極上に酸化物半導体層を有するボトムゲート型の薄膜トランジスタとし、酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とすることで、ソース電極及びドレイン電極の側面における電極上端から電極下端までの距離を大きくする。
【０００７】
本明細書で開示する発明の構成の一つは、絶縁表面を有する基板上にゲート電極と、ゲート電極上に絶縁層と、絶縁層上にソース電極及びドレイン電極と、ソース電極の側面と、該側面と向かい合うドレイン電極の側面の間にゲート電極と絶縁層を介して重なる酸化物半導体層とを有し、基板の基板面とソース電極の側面とがなす角と、基板の基板面とドレイン電極の側面とがなす角とが２０°以上９０°未満であることを特徴とする半導体装置である。
【０００８】
上記構成は、上記課題の少なくとも一つを解決する。
【０００９】
ソース電極及びドレイン電極に用いる金属材料にもよるが、ソース電極及びドレイン電極の少なくとも側面には自然酸化膜が形成される。この自然酸化膜は、エッチング後に大気などの酸素を含む雰囲気に触れると形成される。また、エッチング後に酸化物半導体層を形成する際の成膜雰囲気に酸素を含んでいる場合にも、電極側面に自然酸化膜が形成される。

【００１０】
また、電極上面に自然酸化膜が形成されることを防ぐために、スパッタ法で得られる金属膜上に接してバッファ層（ｎ＋層とも呼ぶ）を大気に触れることなく連続成膜することが好ましい。このバッファ層は、酸化物半導体層に比べて低抵抗な酸化物半導体層であり、ソース領域またはドレイン領域として機能させる。
【００１１】
上記構成において、ソース電極及び前記ドレイン電極の上面にバッファ層を有し、該バッファ層上に酸化物半導体層を有する。バッファ層（ｎ＋層とも呼ぶ）を大気に触れることなく連続成膜することにより、ソース電極及び前記ドレイン電極の上面に自然酸化膜が形成されることを防ぐ。
【００１２】
また、ボトムゲート型の薄膜トランジスタにおいて、ゲート電極にしきい値電圧よりも十分に大きい電圧をかけて、オン状態とした場合のドレイン電流の経路（チャネル長方向の電流経路）は、まず、ドレイン電極からゲート絶縁膜の界面近傍の酸化物半導体層を経てソース電極に達する経路となる。
【００１３】
なお、ソース電極及びドレイン電極上に酸化物半導体層を有するボトムゲート型の薄膜トランジスタのチャネル長は、ソース電極とドレイン電極の最短間隔距離に相当し、ソース電極とドレイン電極に挟まれ、ゲート絶縁膜との界面近傍の酸化物半導体層の距離とする。
【００１４】
ｎ＋層をドレイン電極及びソース電極の上面に接して形成する場合、電極側面に形成される自然酸化膜の導電率が低いと、ドレイン電流の主な経路は、ドレイン電極からｎ＋層を経由して、ドレイン電極側面の界面近傍の酸化物半導体層を通り、ゲート絶縁膜の界面近傍の酸化物半導体層を経て、ソース電極側面の界面近傍の酸化物半導体層を通り、ｎ＋層を経由してソース電極に達する経路となる。スパッタ法で得られる酸化物半導体層は、被成膜面との界面近傍の膜質が、被成膜面の材料に影響を受ける傾向がある。酸化物半導体層は、ｎ＋層との界面、ソース電極側面（及びドレイン電極側面）との界面、ゲート絶縁膜との界面とを有し、異なる材料との界面を少なくとも３つ有する。従って、酸化物半導体層において、ドレイン電極側面の自然酸化膜と界面状態と、ゲート絶縁膜との界面状態は異なるため、ドレイン電極側面の界面近傍の酸化物半導体層が第１の電界集中緩和領域として機能する。また、ソース電極側面の自然酸化膜と界面状態と、ゲート絶縁膜との界面状態は異なるため、ソース電極側面の界面近傍の酸化物半導体層が第２の電界集中緩和領域として機能する。
【００１５】
このように、酸化物半導体層におけるソース電極の側面及びドレイン電極の側面と重なる領域は、電界集中緩和領域として機能する。
【００１６】
本明細書中で用いる酸化物半導体は、$InMO_3(ZnO)_m$（m＞0）で表記される薄膜を形成し、その薄膜を半導体層として用いた薄膜トランジスタを作製する。なお、Ｍは、Ｇａ、Ｆｅ、Ｎｉ、Ｍｎ及びＣｏから選ばれた一の金属元素又は複数の金属元素を示す。例えばＭとして、Ｇａの場合があることの他、ＧａとＮｉ又はＧａとＦｅなど、Ｇａ以外の上記金属元素が含まれる場合がある。また、上記酸化物半導体において、Ｍとして含まれる金属元素の他に、不純物元素としてＦｅ、Ｎｉその他の遷移金属元素、又は該遷移金属の酸化物が含まれているものがある。本明細書においては、この薄膜をＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜とも呼ぶ。
【００１７】
Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の結晶構造は、スパッタ法で成膜した後、２００℃～５００℃、代表的には３００～４００℃で１０分～１００分行っても、アモルファス構造がＸＲＤの分析では観察される。

【００１８】
酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とし、ソース電極及びドレイン電極の側面における電極上端から電極下端までの距離を大きくすることによって第１の電界集中緩和領域の長さ及び第２電界集中緩和領域の長さを長くして電界集中を緩和させる。さらに、ソース電極及びドレイン電極の膜厚を厚くすることによっても電極側面における電極上端から電極下端までの距離を大きくできる。
【００１９】
また、酸化物半導体層をスパッタ法で成膜する場合、基板面に垂直な電極側面に成膜される膜厚は、電極上面に成膜される膜厚よりも薄くなる恐れがある。酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とすることで側面においても膜厚の均一性を高めることができ、電界集中を緩和することもできる。
【００２０】
また、図１に示すように、ソース電極側面の下端を始点としソース電極側面の上端を結んだ直線がソース電極側面にほぼ一致する場合、ソース電極はテーパ形状を有していると言え、基板の基板面とソース電極の側面がなす角度θ１は、第１のテーパ角とも呼べる。また、ドレイン電極側面の下端を始点としドレイン電極側面の上端を結んだ直線がドレイン電極側面にほぼ一致する場合、ドレイン電極はテーパ形状を有していると言え、基板の基板面とドレイン電極の側面がなす角度θ２は、第２のテーパ角とも呼べる。
【００２１】
また、電極側面が１つの角度を有している形状に限定されず、少なくともソース電極の下端部の側面の角度θ１、及びドレイン電極の下端部の側面の角度θ２が２０°以上９０°未満であれば、電極側面に段差を有してもよい。
【００２２】
また、他の発明の構成は、絶縁表面を有する基板上にゲート電極と、ゲート電極上に絶縁層と、絶縁層上にソース電極及びドレイン電極と、ソース電極の側面と、該側面と向かい合うドレイン電極の側面の間にゲート電極と絶縁層を介して重なる酸化物半導体層とを有し、基板の基板面とソース電極下端部の側面とがなす角と、基板の基板面とドレイン電極下端部の側面とがなす角とが２０°以上９０°未満であることを特徴とする半導体装置である。
【００２３】
上記構成において、基板の基板面とソース電極下端部の側面とがなす角は、基板の基板面とソース電極上端部の側面とがなす角と異ならせる。また、上記構成において、基板の基板面とドレイン電極下端部の側面とがなす角は、基板の基板面とドレイン電極上端部の側面とがなす角と異ならせる。なお、酸化物半導体層を挟んで対向するソース電極側面とドレイン電極側面の断面形状は同じエッチング工程を経るため、ほぼ同一である。
【００２４】
例えば、ソース電極（及びドレイン電極）下端部の側面の角度と、ソース電極（及びドレイン電極）上端部の側面の角度を異ならせ、ソース電極（及びドレイン電極）上端部の側面の角度を９０°としてもよい。ソース電極（及びドレイン電極）上端部の側面の角度をソース電極（及びドレイン電極）下端部の側面の角度よりも大きくすることで、ソース電極及びドレイン電極を形成するためのマスクの間隔を狭く設計することができ、結果としてチャネル長を短く設計する、例えばチャネル長を１μｍ～１０μｍに設計することができる。
【００２５】
また、ソース電極及びドレイン電極の側面形状は、すくなくとも一部に曲面を有していてもよく、例えば、ソース電極及びドレイン電極の断面形状において、電極の下端部は、電極の外側に位置する曲率半径の中心により決まる１つの曲面も有するようにしてもよい。また、ソース電極及びドレイン電極の側面形状は、電極上面から基板に向かって裾広がり

の断面形状を有していてもよい。
【００２６】
上述した様々な断面形状を有する電極の形成は、ドライエッチングまたはウェットエッチングによって形成する。ドライエッチングに用いるエッチング装置としては、反応性イオンエッチング法（ＲＩＥ法）を用いたエッチング装置や、ＥＣＲ（Ｅｌｅｃｔｒｏｎ Ｃｙｃｌｏｔｒｏｎ Ｒｅｓｏｎａｎｃｅ）やＩＣＰ（Ｉｎｄｕｃｔｉｖｅｌｙ Ｃｏｕｐｌｅｄ Ｐｌａｚｍａ）などの高密度プラズマ源を用いたドライエッチング装置を用いることができる。また、ＩＣＰエッチング装置と比べて広い面積に渡って一様な放電が得られやすいドライエッチング装置としては、上部電極を接地させ、下部電極に１３．５６ＭＨｚの高周波電源を接続し、さらに下部電極に３．２ＭＨｚの低周波電源を接続したＥＣＣＰ（Ｅｎｈａｎｃｅｄ Ｃａｐａｃｉｔｉｖｅｌｙ Ｃｏｕｐｌｅｄ Ｐｌａｓｍａ）モードのエッチング装置がある。このＥＣＣＰモードのエッチング装置であれば、例えば基板として、第１０世代の３ｍを超えるサイズの基板を用いる場合にも対応することができる。
【００２７】
また、ソース電極及びドレイン電極は単層であってもよいし、少なくとも異なる２つの材料からなる２層以上の多層であってもよい。
【００２８】
また、上記構造を実現するための作製方法に関する発明の構成の一つは、絶縁表面を有する基板上にゲート電極を形成し、ゲート電極を覆うゲート絶縁層を形成し、ゲート絶縁層上に導電層とバッファ層とを大気にふれることなく積層形成し、バッファ層及び導電層を選択的にエッチングして基板の基板面となす角が２０°以上９０°未満である側面を有するソース電極及びドレイン電極を形成し、ゲート絶縁層、ソース電極、及びドレイン電極上に酸化物半導体層を形成する半導体装置の作製方法である。
【００２９】
上記作製方法に関する構成において、バッファ層は、インジウム、ガリウム、及び亜鉛を含み、バッファ層上に形成する酸化物半導体層と同じターゲットを用いることができる。成膜雰囲気を変更することで、バッファ層と、酸化物半導体層とを作り分けることができ、共通のターゲットを用いることで製造コストを低減することができる。
【００３０】
上記作製方法に関する構成において、ゲート絶縁層上に導電層とバッファ層とを大気にふれることなく積層形成しており、連続成膜を行うことを特徴の一つとしている。
【００３１】
上記作製方法に関する構成において、ソース電極、及びドレイン電極を形成する導電層は、アルミニウム、タングステン、クロム、タンタル、チタン、モリブデンなどの金属材料またはその合金材料を用いて形成する。また、導電層は、２層以上の積層としてもよく、例えば、アルミニウム膜を下層とし、上層をチタン膜とする積層、タングステン膜を下層とし、上層をモリブデン膜とする積層、アルミニウム膜を下層とし、上層をモリブデン膜とする積層などを用いることができる。
【００３２】
本明細書中で連続成膜とは、スパッタ法で行う第１の成膜工程からスパッタ法で行う第２の成膜工程までの一連のプロセス中、被処理基板の置かれている雰囲気が大気等の汚染雰囲気に触れることなく、常に真空中または不活性ガス雰囲気（窒素雰囲気または希ガス雰囲気）で制御されていることを言う。連続成膜を行うことにより、清浄化された被処理基板の水分等の再付着を回避して成膜を行うことができる。
【００３３】
同一チャンバー内で第１の成膜工程から第２の成膜工程までの一連のプロセスを行うことは本明細書における連続成膜の範囲にあるとする。
【００３４】
また、異なるチャンバーで第１の成膜工程から第２の成膜工程までの一連のプロセスを行

う場合、第１の成膜工程を終えた後、大気にふれることなくチャンバー間を基板搬送して第２の成膜を施すことも本明細書における連続成膜の範囲にあるとする。

【００３５】

なお、第１の成膜工程と第２の成膜工程の間に、基板搬送工程、アライメント工程、徐冷工程、または第２の工程に必要な温度とするため基板を加熱または冷却する工程等を有しても、本明細書における連続成膜の範囲にあるとする。

【００３６】

ただし、洗浄工程、ウエットエッチング、レジスト形成といった液体を用いる工程が第１の成膜工程と第２の成膜工程の間にある場合、本明細書でいう連続成膜の範囲には当てはまらないとする。

【００３７】

本明細書において、上、下、側、水平、垂直等の方向を表す文言は、基板表面の上にデバイスを配置した場合の基板面を基準とする方向を指す。

【００３８】

なお、第１、第２として付される序数詞は便宜上用いるものであり、工程順又は積層順を示すものではない。また、本明細書において発明を特定するための事項として固有の名称を示すものではない。

【発明の効果】

【００３９】

基板の基板面とソース電極の側面とがなす角と、基板の基板面とドレイン電極の側面とがなす角を調節することで、ソース電極及びドレイン電極上に設けられる酸化物半導体層の被覆性を向上させる。

【００４０】

電界集中緩和領域を設けることにより、ソース電極とドレイン電極間に生じる恐れのある電界集中を緩和し、薄膜トランジスタのスイッチング特性の劣化を抑える。

【発明を実施するための最良の形態】

【００４１】

本実施形態について、以下に説明する。

【００４２】

（実施の形態１）

図１に薄膜トランジスタ１７０を基板上に設ける例を示す。なお、図１は薄膜トランジスタの断面図の一例である。

【００４３】

絶縁表面を有する基板１００上に設けられたゲート電極１０１は、ゲート絶縁層１０２に覆われ、ゲート電極１０１と重なるゲート絶縁層１０２上には第１配線または第２配線が設けられる。ソース電極層１０５ａまたはドレイン電極層１０５ｂとして機能する第１配線または第２配線上には、バッファ層がそれぞれ設けられている。ソース電極層１０５ａ上には第１のバッファ層１０４ａが設けられ、ドレイン電極層１０５ｂ上には第２のバッファ層１０４ｂが設けられている。そして、第１のバッファ層１０４ａ、及び第２のバッファ層１０４ｂ上には酸化物半導体層１０３を有する。

【００４４】

図１において、透光性を有する基板１００にはコーニング社の７０５９ガラスや１７３７ガラスなどに代表されるバリウムホウケイ酸ガラスやアルミノホウケイ酸ガラスなどのガラス基板を用いることができる。

【００４５】

ゲート電極１０１は、単層、または異なる金属材料からなる積層とする。また、ゲート電極１０１の材料は金属材料（アルミニウム（Ａｌ）、銅（Ｃｕ）、チタン（Ｔｉ）、タンタル（Ｔａ）、タングステン（Ｗ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）、Ｎｄ（ネオジム）、Ｓｃ（スカンジウム）から選ばれた元素、または上述した元素を成分とする合金）を用い、ゲート電極１０１の側面の角度を２０°以上９０°未満とする。少なくとも端

部にテーパー形状が形成されるようにエッチングしてゲート電極１０１を形成する。

【００４６】

また、ゲート絶縁層１０２はスパッタ法またはプラズマＣＶＤ法で得られる酸化シリコン膜、酸化窒化シリコン膜、窒化シリコン膜、酸化アルミニウム、酸化タンタル膜などの絶縁膜を用い、これらの材料から成る単層または積層構造として形成しても良い。なお、ゲート絶縁層１０２上に形成するソース電極層１０５ａ及びドレイン電極層１０５ｂをエッチングする際に、選択比が十分に取れる材料を選択することが好ましい。また、ソース電極層１０５ａ及びドレイン電極層１０５ｂをエッチングする際にゲート絶縁層１０２の表面が２０ｎｍ程度までエッチングされてもよく、金属材料のエッチング残渣をなくすためには少し表層を除去することが好ましい。

【００４７】

ソース電極層１０５ａ及びドレイン電極層１０５ｂは、単層、または異なる金属材料からなる積層とする。ソース電極層１０５ａ及びドレイン電極層１０５ｂの材料は金属材料（アルミニウム（Ａｌ）、銅（Ｃｕ）、チタン（Ｔｉ）、タンタル（Ｔａ）、タングステン（Ｗ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）、Ｎｄ（ネオジム）、Ｓｃ（スカンジウム）から選ばれた元素、または上述した元素を成分とする合金）を用いる。

【００４８】

ソース電極層１０５ａの断面形状は、図１に示すように、基板の基板面とソース電極層１０５ａの側面とがなす角度θ１が２０°以上９０°未満とする。また、ドレイン電極層１０５ｂの断面形状は、図１に示すように、基板の基板面とドレイン電極層１０５ｂの側面とがなす角度θ２が２０°以上９０°未満とする。同じエッチング工程（ドライエッチングまたはウェットエッチング）により形成されるため、角度θ１と角度θ２はほぼ同一である。酸化物半導体層と接するソース電極層１０５ａの側面の角度θ１及びドレイン電極層１０５ｂの側面の角度θ２を２０°以上９０°未満とすることで、ソース電極層１０５ａ及びドレイン電極層１０５ｂの側面における電極上端から電極下端までの距離を大きくする。

【００４９】

なお、図１では基板の裏面平面を基板面として角度θ１、角度θ２を表記しているが、特に限定されず、基板の表面平面を基板面としても基板の裏面平面と表面平面は平行であるため同じ角度となることは言うまでもない。

【００５０】

このような形状のソース電極層１０５ａ及びドレイン電極層１０５ｂ上に酸化物半導体層１０３を形成する。酸化物半導体層１０３は、Ｉｎ、Ｇａ、及びＺｎを含む酸化物半導体ターゲット（In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１）を用いて、基板とターゲットの間との距離を１７０ｍｍ、圧力０．４Ｐａ、直流（ＤＣ）電源０．５ｋＷ、酸素を含むアルゴン雰囲気下で成膜した後、レジストマスクを形成して選択的にエッチングし、不要な部分を除去して形成する。なお、パルス直流（ＤＣ）電源を用いると、ごみが軽減でき、膜厚分布も均一となるために好ましい。酸化物半導体膜の膜厚は、５ｎｍ～２００ｎｍとする。本実施の形態では酸化物半導体膜の膜厚は、１００ｎｍとする。

【００５１】

なお、ソース電極層１０５ａと酸化物半導体層１０３の間には、第１のバッファ層１０４ａを設けることが好ましい。また、ドレイン電極層１０５ｂと酸化物半導体層１０３の間には、第２のバッファ層１０４ｂを設けることが好ましい。

【００５２】

第１のバッファ層１０４ａ、及び第２のバッファ層１０４ｂは、酸化物半導体層１０３に比べて低抵抗な酸化物半導体層（ｎ＋層）であり、ソース領域またはドレイン領域として機能する。

【００５３】

ｎ＋層は、In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１としたターゲットを用い、成膜条件は、圧力を０．４Ｐａとし、電力を５００Ｗとし、成膜温度を室温とし、アルゴンガ

ス流量４０ｓｃｃｍを導入してスパッタ成膜を行う。In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１としたターゲットを意図的に用いているにも関わらず、成膜直後で大きさ１ｎｍ～１０ｎｍの結晶粒を含むＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜が形成されることがある。なお、ターゲットの成分比、成膜圧力（０．１Ｐａ～２．０Ｐａ）、電力（２５０Ｗ～３０００Ｗ：８インチφ）、温度（室温～１００℃）、反応性スパッタの成膜条件などを適宜調節することで結晶粒の有無や、結晶粒の密度や、直径サイズは、１ｎｍ～１０ｎｍの範囲で調節されうると言える。第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、５ｎｍ～２０ｎｍとする。勿論、膜中に結晶粒が含まれる場合、含まれる結晶粒のサイズが膜厚を超える大きさとならない。本実施の形態では第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、５ｎｍとする。

【００５４】

また、ソース電極層１０５ａ又はドレイン電極層１０５ｂとなる導電膜とｎ＋層となる酸化物半導体膜を大気に曝すことなくスパッタ法で積層することで製造プロセス中にソース電極層又はドレイン電極層が露呈してゴミが付着することを防止することができる。

【００５５】

スパッタ法で得られる酸化物半導体層１０３は、被成膜面との界面近傍の膜質が、被成膜面の材料に影響を受ける傾向がある。酸化物半導体層は、ｎ＋層との界面、ソース電極層側面（及びドレイン電極層側面）との界面、ゲート絶縁膜との界面とを有し、異なる材料との界面を少なくとも３つ有する。従って、酸化物半導体層１０３において、ドレイン電極側面の自然酸化膜と界面状態と、ゲート絶縁膜との界面状態は異なるため、ドレイン電極層側面の界面近傍の酸化物半導体層が第１の電界集中緩和領域１０６ａとして機能する。また、ソース電極側面の自然酸化膜と界面状態と、ゲート絶縁膜との界面状態は異なるため、ソース電極側面の界面近傍の酸化物半導体層が第２の電界集中緩和領域１０６ｂとして機能する。

酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とし、ソース電極及びドレイン電極の側面における電極上端から電極下端までの距離を大きくすることによって第１の電界集中緩和領域１０６ａの長さＬ１及び第２電界集中緩和領域１０６ｂの長さＬ２を長くして電界集中を緩和させる。さらに、ソース電極及びドレイン電極の膜厚を厚くすることによっても電極側面における電極上端から電極下端までの距離を大きくできる。

【００５６】

また、酸化物半導体層１０３をスパッタ法で成膜する場合、基板面に垂直な電極側面に成膜される膜厚は、電極上面に成膜される膜厚よりも薄くなる恐れがある。酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とすることで側面においても膜厚の均一性を高めることができ、酸化物半導体層１０３が局所的に薄くなる領域を低減し、電界集中を緩和することもできる。

【００５７】

（実施の形態２）

図１では、ソース電極層（ドレイン電極層）側面の下端を始点としソース電極層（ドレイン電極層）側面の上端を結んだ直線がソース電極（ドレイン電極層）側面にほぼ一致する例を示したが、本実施の形態では、ソース電極層（ドレイン電極層）側面に段差を有する例を図２を用いて説明する。少なくともソース電極層の下端部の側面の角度θ１、及びドレイン電極層の下端部の側面の角度θ２が２０°以上９０°未満であれば、電極側面に段差を有してもよい。なお、図２において図１と共通の部分には同じ符号を用いる。

【００５８】

絶縁表面を有する基板１００上に設けられたゲート電極１０１は、ゲート絶縁層１０２に覆われ、ゲート電極１０１と重なるゲート絶縁層１０２上には第１配線または第２配線が設けられる。ソース電極層４０５ａまたはドレイン電極層４０５ｂとして機能する第１配線または第２配線上には、バッファ層がそれぞれ設けられている。ソース電極層４０５ａ上には第１のバッファ層４０４ａが設けられ、ドレイン電極層４０５ｂ上には第２のバッ

ファ層４０４ｂが設けられている。そして、第１のバッファ層４０４ａ、及び第２のバッファ層４０４ｂ上には酸化物半導体層４０３を有する。

【００５９】

絶縁表面を有する基板１００、ゲート電極１０１、及びゲート絶縁層１０２に関しては実施の形態１と同一であるため、ここでは詳細な説明は省略する。

【００６０】

また、ソース電極層４０５ａ及びドレイン電極層４０５ｂは、単層、または異なる金属材料からなる積層とする。ソース電極層４０５ａ及びドレイン電極層４０５ｂの材料は金属材料（アルミニウム（Ａｌ）、銅（Ｃｕ）、チタン（Ｔｉ）、タンタル（Ｔａ）、タングステン（Ｗ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）、Ｎｄ（ネオジム）、Ｓｃ（スカンジウム）から選ばれた元素、または上述した元素を成分とする合金）を用いる。

【００６１】

ここではソース電極層４０５ａ及びドレイン電極層４０５ｂとして膜厚１００ｎｍのタングステン膜の単層を用い、コイル状アンテナを用いるＩＣＰエッチング装置を用いて図２に示すソース電極層４０５ａの側面形状、及びドレイン電極層４０５ｂの側面形状を形成する例を説明する。

【００６２】

本実施の形態では、CF_4のガス流量を２５（ｓｃｃｍ）、Cl_3のガス流量を２５（ｓｃｃｍ）、O_2のガス流量を１０（ｓｃｃｍ）とし、１．５Ｐａの圧力でコイル型の電極に５００ＷのＲＦ（１３．５６ＭＨｚ）電力を投入してプラズマを生成してエッチングを行う。基板側（試料ステージ）にも１０ＷのＲＦ（１３．５６ＭＨｚ）電力を投入し、実質的に負の自己バイアス電圧を印加する。少なくともゲート絶縁膜１０２がある程度露呈した段階で、このエッチングを途中で停止することにより、段差を有する電極側面が形成される。

【００６３】

上記エッチング条件により、ソース電極層４０５ａの断面形状は、基板の基板面とソース電極層４０５ａの下端部側面とがなす角度θ１が２０°以上９０°未満とすることができ、図２に示すように、θ１は約４０°である。また、基板の基板面とソース電極層４０５ａの上端部側面とがなす角度は約９０°である。なお、酸化物半導体層４０３を挟んで対向するソース電極層４０５ａ側面とドレイン電極層４０５ｂ側面の断面形状は同じエッチング工程を経るため、ほぼ同一である。

【００６４】

このように、ソース電極層４０５ａ（及びドレイン電極層４０５ｂ）上端部の側面の角度をソース電極層４０５ａ（及びドレイン電極層４０５ｂ）下端部の側面の角度よりも大きくすることで、ソース電極層４０５ａ及びドレイン電極層４０５ｂを形成するためのフォトマスク（またはレジストマスク）の間隔を狭く設計することができ、結果としてチャネル長を短く設計する、例えばチャネル長を１μｍ～１０μｍに設計することができる。

【００６５】

また、上述した方法に限定されず、ソース電極層４０５ａ及びドレイン電極層４０５ｂとして用いるエッチングガスのエッチングレートが異なる材料を積層させ、下層にエッチングレートの低い材料層、上層にエッチングレートの高い材料層とし、エッチングを行うと電極側面に段差を形成することができる。

【００６６】

酸化物半導体層４０３を挟んで対向する２つの電極側面に段差を持たせることにより、ソース電極層及びドレイン電極層の側面における電極上端から電極下端までの距離を大きくすることによって第１の電界集中緩和領域４０６ａの長さＬ３及び第２電界集中緩和領域４０６ｂの長さＬ４を長くして電界集中を緩和させる。

【００６７】

さらにソース電極層及びドレイン電極層の側面における電極上端から電極下端までの距離を大きくするため、上述したドライエッチング後に、さらにウェットエッチングを行って

酸化物半導体層４０３を挟んで対向する２つの電極側面の一部に曲面を持たせてもよい。

【００６８】

また、上述したドライエッチングではなく、ソース電極層及びドレイン電極層の形成をウェットエッチングを行って、少なくともソース電極層の下端部の側面の角度θ１、及びドレイン電極層の下端部の側面の角度θ２が２０°以上９０°未満としてもよく、電極上面から基板に向かって裾広がりの断面形状としてもよい。

【００６９】

また、本実施の形態は実施の形態１と自由に組み合わせることができる。

【００７０】

（実施の形態３）

本実施の形態では、薄膜トランジスタ及びその作製工程について、図３乃至図９を用いて説明する。

【００７１】

図３（Ａ）において、透光性を有する基板１００にはコーニング社の＃７０５９ガラスや＃１７３７ガラスなどに代表されるバリウムホウケイ酸ガラスやアルミノホウケイ酸ガラスなどのガラス基板を用いることができる。

【００７２】

次いで、導電層を基板１００全面に形成した後、第１のフォトリソグラフィー工程を行い、レジストマスクを形成し、エッチングにより不要な部分を除去して配線及び電極（ゲート電極１０１を含むゲート配線、容量配線１０８、及び第１の端子１２１）を形成する。このとき少なくともゲート電極１０１の端部にテーパー形状が形成されるようにエッチングする。この段階での上面図を図３（Ａ）に示した。なお、この段階での上面図が図５に相当する。

【００７３】

ゲート電極１０１を含むゲート配線と容量配線１０８、端子部の第１の端子１２１は、チタン（Ｔｉ）、タンタル（Ｔａ）、タングステン（Ｗ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）、Ｎｄ（ネオジム）、アルミニウム（Ａｌ）、銅（Ｃｕ）から選ばれた元素、または上述した元素を成分とする合金か、上述した元素を組み合わせた合金膜、または上述した元素を成分とする窒化物で形成する。仲でもアルミニウム（Ａｌ）や銅（Ｃｕ）などの低抵抗導電性材料で形成することが望ましいが、Ａｌ単体では耐熱性が劣り、また腐蝕しやすい等の問題点があるのでチタン（Ｔｉ）、タンタル（Ｔａ）、タングステン（Ｗ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）、Ｎｄ（ネオジム）から選ばれた元素、または上述した元素を組み合わせた合金膜、または上述した元素を成分とする窒化物で形成する。

【００７４】

次いで、ゲート電極１０１上にゲート絶縁層１０２を全面に成膜する。ゲート絶縁層１０２はスパッタ法などを用い、膜厚を５０～２５０ｎｍとする。

【００７５】

例えば、ゲート絶縁層１０２としてスパッタ法により酸化シリコン膜を用い、１００ｎｍの厚さで形成する。勿論、ゲート絶縁層１０２はこのような酸化シリコン膜に限定されるものでなく、酸化窒化シリコン膜、窒化シリコン膜、酸化アルミニウム、酸化タンタル膜などの他の絶縁膜を用い、これらの材料から成る単層または積層構造として形成しても良い。

【００７６】

次に、ゲート絶縁層１０２上に金属材料からなる導電膜をスパッタ法や真空蒸着法で形成する。導電膜の材料としては、Ａｌ、Ｃｒ、Ｔａ、Ｔｉ、Ｍｏ、Ｗから選ばれた元素、または上述した元素を成分とする合金か、上述した元素を組み合わせた合金膜等が挙げられる。ここでは、導電膜としてアルミニウム（Ａｌ）膜と、そのアルミニウム（Ａｌ）膜上に重ねてＴｉ膜を積層する。また、導電膜は、３層構造としてもよく、タングステン膜上にチタン膜を積層してもよい。また、導電膜は、シリコンを含むアルミニウム膜の単層構造や、タングステン膜の単層構造としてもよい。

【００７７】
次に、導電膜上に第１の酸化物半導体膜（本実施の形態では第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜）をスパッタ法で成膜する。ここでは、In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１としたターゲットを用い、成膜条件は、圧力を０．４Ｐａとし、電力を５００Ｗとし、成膜温度を室温とし、アルゴンガス流量４０ｓｃｃｍを導入してスパッタ成膜を行う。In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１としたターゲットを意図的に用いているにも関わらず、成膜直後で大きさ１ｎｍ～１０ｎｍの結晶粒を含むＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜が形成されることがある。なお、ターゲットの成分比、成膜圧力（０．１Ｐａ～２．０Ｐａ）、電力（２５０Ｗ～３０００Ｗ：８インチφ）、温度（室温～１００℃）、反応性スパッタの成膜条件などを適宜調節することで結晶粒の有無や、結晶粒の密度や、直径サイズは、１ｎｍ～１０ｎｍの範囲で調節されうると言える。第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、５ｎｍ～２０ｎｍとする。勿論、膜中に結晶粒が含まれる場合、含まれる結晶粒のサイズが膜厚を超える大きさとならない。本実施の形態では第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、５ｎｍとする。
【００７８】
次に、第２のフォトリソグラフィー工程を行い、レジストマスクを形成し、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜をエッチングする。ここではＩＴＯ０７Ｎ（関東化学社製）を用いたウェットエッチングにより、画素部において、不要な部分を除去して第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜１１１ａ、１１１ｂを形成する。なお、ここでのエッチングは、ウェットエッチングに限定されずドライエッチングを用いてもよい。
【００７９】
次に、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜のエッチングと同じレジストマスクを用いて、エッチングにより不要な部分を除去してソース電極層１０５ａ及びドレイン電極層１０５ｂを形成する。この際のエッチング方法としてウエットエッチングまたはドライエッチングを用いる。ここでは、$SiCl_4$とCl_2とBCl_3の混合ガスを反応ガスとしたドライエッチングにより、Ａｌ膜とＴｉ膜を積層した導電膜をエッチングしてソース電極層１０５ａ及びドレイン電極層１０５ｂを形成する。この段階での断面図を図３（Ｂ）に示した。なお、この段階での上面図が図６に相当する。
【００８０】
ここでのエッチングにより、後に形成する酸化物半導体層と接するソース電極層１０５ａの側面の角度θ１及びドレイン電極層１０５ｂの側面の角度θ２を２０°以上９０°未満とする。酸化物半導体層を挟んで対向する２つの電極側面をテーパ形状とすることで、酸化物半導体層におけるソース電極層の側面及びドレイン電極層の側面と重なる領域は、電界集中緩和領域として機能させることができる。
【００８１】
また、この第２のフォトリソグラフィー工程において、ソース電極層１０５ａ及びドレイン電極層１０５ｂと同じ材料である第２の端子１２２を端子部に残す。なお、第２の端子１２２はソース配線（ソース電極層１０５ａを含むソース配線）と電気的に接続されている。また、端子部において、第２の端子１２２の上方に存在し、且つ、第２の端子と重なる第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜１２３は残存する。
【００８２】
また、容量部においては、ソース電極層１０５ａ及びドレイン電極層１０５ｂと同じ材料である容量電極層１２４を残す。また、容量部において、容量電極層１２４の上方に存在し、且つ、容量電極層１２４と重なる第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜１１１ｃは残存する。
【００８３】
次に、レジストマスクを除去した後、大気に曝すことなく第２の酸化物半導体膜（本実施の形態では第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜）を成膜する。プラズマ処理後、大気に曝すことなく第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を成膜することは、ゲート絶縁層と半導体膜の界面にゴミなどを付着させない点で有用である。ここでは、直径８イン

チのＩｎ、Ｇａ、及びＺｎを含む酸化物半導体ターゲット（In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１）を用いて、基板とターゲットの間との距離を１７０ｍｍ、圧力０．４Ｐａ、直流（ＤＣ）電源０．５ｋＷ、アルゴン又は酸素雰囲気下で成膜する。なお、パルス直流（ＤＣ）電源を用いると、ごみが軽減でき、膜厚分布も均一となるために好ましい。第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、５ｎｍ～２００ｎｍとする。本実施の形態では第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、１００ｎｍとする。

【００８４】

第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜は、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜条件と異ならせることで、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜よりも電気抵抗の高い膜とする。例えば、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜条件における酸素ガス流量とアルゴンガス流量の比よりも第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜条件における酸素ガス流量の占める比率が多い条件とする。具体的には、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜条件は、希ガス（アルゴン、又はヘリウムなど）雰囲気下（または酸素ガス１０％以下、アルゴンガス９０％以上）とし、第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜条件は、酸素雰囲気下（又は酸素ガス流量とアルゴンガス流量の比１：１以上）とする。

【００８５】

次いで、２００℃～６００℃、代表的には３００℃～５００℃の熱処理を行うことが好ましい。ここでは炉に入れ、窒素雰囲気または大気雰囲気下で３５０℃、１時間の熱処理を行う。この熱処理によりＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の原子レベルの再配列が行われる。この熱処理によりキャリアの移動を阻害する歪が解放されるため、ここでの熱処理（光アニールも含む）は重要である。なお、熱処理を行うタイミングは、第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜後であれば特に限定されず、例えば画素電極形成後に行ってもよい。

【００８６】

次に、第３のフォトリソグラフィー工程を行い、レジストマスクを形成し、エッチングにより不要な部分を除去して半導体層１０３を形成する。ここではＩＴＯ０７Ｎ（関東化学社製）を用いたウェットエッチングにより、第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を除去して半導体層１０３を形成する。ウェットエッチングで除去する場合、エッチングの廃液から酸化物半導体を再生して、ターゲットの作製に再利用することができる。

【００８７】

酸化物半導体に含まれているインジウムやガリウムは、希少価値のある金属であることが知られており、再利用することによって、省資源化を図るとともに酸化物半導体を用いて形成される製品のコストダウンを図ることができる。

【００８８】

なお、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜と第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜は同じエッチャントを用いるため、ここでのエッチングにより第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜が除去される。従って、第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜で覆われた第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の側面は保護されるが、図４（Ａ）に示すように、露呈している第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜１１１ａ、１１１ｂはエッチングされ、第１のバッファ層１０４ａ、第２のバッファ層１０４ｂが形成される。なお、半導体層１０３のエッチングは、ウェットエッチングに限定されずドライエッチングを用いてもよい。以上の工程で半導体層１０３をチャネル形成領域とする薄膜トランジスタ１７０が作製できる。この段階での断面図を図４（Ａ）に示した。なお、この段階での上面図が図７に相当する。

【００８９】

次いで、レジストマスクを除去し、半導体層を覆う保護絶縁膜１０７を形成する。保護絶縁膜１０７はスパッタ法などを用いて得られる窒化シリコン膜、酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウム膜、酸化窒化アルミニウム膜、酸化タンタル膜などを用いることができる。

【００９０】
次に、第４のフォトリソグラフィー工程を行い、レジストマスクを形成し、保護絶縁膜１０７のエッチングによりドレイン電極層１０５ｂに達するコンタクトホール１２５を形成する。また、ここでのエッチングにより第２の端子１２２に達するコンタクトホール１２７も形成する。また、ここでのエッチングにより容量電極層１２４に達するコンタクトホール１０９も形成する。なお、マスク数を削減するため、同じレジストマスクを用いてさらにゲート絶縁層をエッチングしてゲート電極に達するコンタクトホール１２６も同じレジストマスクで形成することが好ましい。この段階での断面図を図４（Ｂ）に示す。
【００９１】
次いで、レジストマスクを除去した後、透明導電膜を成膜する。透明導電膜の材料としては、酸化インジウム（In_2O_3）や酸化インジウム酸化スズ合金（In_2O_3－SnO_2、ＩＴＯと略記する）などをスパッタ法や真空蒸着法などを用いて形成する。このような材料のエッチング処理は塩酸系の溶液により行う。しかし、特にＩＴＯのエッチングは残渣が発生しやすいので、エッチング加工性を改善するために酸化インジウム酸化亜鉛合金（In_2O_3－ＺｎＯ）を用いても良い。
【００９２】
次に、第５のフォトリソグラフィー工程を行い、レジストマスクを形成し、エッチングにより不要な部分を除去して画素電極１１０を形成する。
【００９３】
また、この第５のフォトリソグラフィー工程において、容量部におけるゲート絶縁層１０２を誘電体として、容量電極層１２４と画素電極１１０とで保持容量が形成される。容量配線１０８はコンタクトホール１０９を介して容量電極層１２４と電気的に接続する。
【００９４】
また、この第５のフォトリソグラフィー工程において、第１の端子及び第２の端子をレジストマスクで覆い端子部に形成された透明導電膜１２８、１２９を残す。透明導電膜１２８、１２９はＦＰＣとの接続に用いられる電極または配線となる。第２の端子１２２上に形成された透明導電膜１２９は、ソース配線の入力端子として機能する接続用の端子電極である。
【００９５】
次いで、レジストマスクを除去し、この段階での断面図を図４（Ｃ）に示す。なお、この段階での上面図が図８に相当する。
【００９６】
また、図９（Ａ１）、図９（Ａ２）は、この段階でのゲート配線端子部の上面図及び断面図をそれぞれ図示している。図９（Ａ１）は図９（Ａ２）中のＣ１－Ｃ２線に沿った断面図に相当する。図９（Ａ１）において、保護絶縁膜１５４上に形成される透明導電膜１５５は、入力端子として機能する接続用の端子電極である。また、図９（Ａ１）において、端子部では、ゲート配線と同じ材料で形成される第１の端子１５１と、ソース配線と同じ材料で形成される接続電極１５３とがゲート絶縁層１５２を介して重なり、透明導電膜１５５で導通させている。なお、図４（Ｃ）に図示した透明導電膜１２８と第１の端子１２１とが接触している部分が、図９（Ａ１）の透明導電膜１５５と第１の端子１５１が接触している部分に対応している。
【００９７】
また、図９（Ｂ１）、及び図９（Ｂ２）は、図４（Ｃ）に示すソース配線端子部とは異なるソース配線端子部の上面図及び断面図をそれぞれ図示している。また、図９（Ｂ１）は図９（Ｂ２）中のＤ１－Ｄ２線に沿った断面図に相当する。図９（Ｂ１）において、保護絶縁膜１５４上に形成される透明導電膜１５５は、入力端子として機能する接続用の端子電極である。また、図９（Ｂ１）において、端子部では、ゲート配線と同じ材料で形成される電極１５６が、ソース配線と電気的に接続される第２の端子１５０の下方にゲート絶縁層１０２を介して重なる。電極１５６は第２の端子１５０とは電気的に接続しておらず、電極１５６を第２の端子１５０と異なる電位、例えばフローティング、ＧＮＤ、０Ｖな

どに設定すれば、ノイズ対策のための容量または静電気対策のための容量を形成することができる。また、第２の端子１５０は、保護絶縁膜１５４を介して透明導電膜１５５と電気的に接続している。

【００９８】

ゲート配線、ソース配線、及び容量配線は画素密度に応じて複数本設けられるものである。また、端子部においては、ゲート配線と同電位の第１の端子、ソース配線と同電位の第２の端子、容量配線と同電位の第３の端子などが複数並べられて配置される。それぞれの端子の数は、それぞれ任意な数で設ければ良いものとし、実施者が適宜決定すれば良い。

【００９９】

こうして５回のフォトリソグラフィー工程により、５枚のフォトマスクを使用して、ボトムゲート型のｎチャネル型薄膜トランジスタである薄膜トランジスタ１７０を有する画素薄膜トランジスタ部、保持容量を完成させることができる。そして、これらを個々の画素に対応してマトリクス状に配置して画素部を構成することによりアクティブマトリクス型の表示装置を作製するための一方の基板とすることができる。本明細書では便宜上このような基板をアクティブマトリクス基板と呼ぶ。

【０１００】

アクティブマトリクス型の液晶表示装置を作製する場合には、アクティブマトリクス基板と、対向電極が設けられた対向基板との間に液晶層を設け、アクティブマトリクス基板と対向基板とを固定する。なお、対向基板に設けられた対向電極と電気的に接続する共通電極をアクティブマトリクス基板上に設け、共通電極と電気的に接続する第４の端子を端子部に設ける。この第４の端子は、共通電極を固定電位、例えばＧＮＤ、０Ｖなどに設定するための端子である。

【０１０１】

また、本実施の形態は、図８の画素構成に限定されず、図８とは異なる上面図の例を図１０に示す。図１０では容量配線を設けず、ゲート絶縁層を誘電体として画素電極を隣り合う画素のゲート配線とゲート絶縁層を介して重なる容量電極層とで保持容量を形成する例であり、この場合、容量配線及び容量配線と接続する第３の端子は省略することができる。なお、図１０において、図８と同じ部分には同じ符号を用いて説明する。

【０１０２】

アクティブマトリクス型の液晶表示装置においては、マトリクス状に配置された画素電極を駆動することによって、画面上に表示パターンが形成される。詳しくは選択された画素電極と該画素電極に対応する対向電極との間に電圧が印加されることによって、画素電極と対向電極との間に配置された液晶層の光学変調が行われ、この光学変調が表示パターンとして観察者に認識される。

【０１０３】

液晶表示装置の動画表示において、液晶分子自体の応答が遅いため、残像が生じる、または動画のぼけが生じるという問題がある。液晶表示装置の動画特性を改善するため、全面黒表示を１フレームおきに行う、所謂、黒挿入と呼ばれる駆動技術がある。

【０１０４】

また、通常の垂直周期を１．５倍若しくは２倍以上にすることで応答速度を改善するとともに各フレーム内の分割された複数フィールド毎に書き込む階調を選択する、所謂、倍速駆動と呼ばれる駆動技術もある。

【０１０５】

また、液晶表示装置の動画特性を改善するため、バックライトとして複数のＬＥＤ（発光ダイオード）光源または複数のＥＬ光源などを用いて面光源を構成し、面光源を構成している各光源を独立して１フレーム基板内で間欠点灯駆動する駆動技術もある。面光源として、３種類以上のＬＥＤを用いてもよいし、白色発光のＬＥＤを用いてもよい。独立して複数のＬＥＤを制御できるため、液晶層の光学変調の切り替えタイミングに合わせてＬＥＤの発光タイミングを同期させることもできる。この駆動技術は、ＬＥＤを部分的に消灯することができるため、特に一画面を占める黒い表示領域の割合が多い映像表示の場合に

は、消費電力の低減効果が図れる。
【０１０６】
これらの駆動技術を組み合わせることによって、液晶表示装置の動画特性などの表示特性を従来よりも改善することができる。
【０１０７】
本実施の形態で得られるｎチャネル型のトランジスタは、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の半導体層をチャネル形成領域に用いており、良好な動特性を有するため、これらの駆動技術を組み合わせることができる。
【０１０８】
また、発光表示装置を作製する場合、有機発光素子の一方の電極（カソードとも呼ぶ）は、低電源電位、例えばＧＮＤ、０Ｖなどに設定するため、端子部に、カソードを低電源電位、例えばＧＮＤ、０Ｖなどに設定するための第４の端子が設けられる。また、発光表示装置を作製する場合には、ソース配線、及びゲート配線に加えて電源供給線を設ける。従って、端子部には、電源供給線と電気的に接続する第５の端子を設ける。
【０１０９】
本実施の形態では、ゲート電極層、ゲート絶縁層、ソース電極層及びドレイン電極層、ソース領域又はドレイン領域（Ｉｎ、Ｇａ、及びＺｎを含む酸化物半導体層）、半導体層（Ｉｎ、Ｇａ、及びＺｎを含む酸化物半導体層）という積層構造を有する薄膜トランジスタとし、ゲート絶縁層表面をプラズマ処理で改質することによって、半導体層の膜厚を薄膜にしたままで、かつ寄生容量を抑制できる。なお、薄膜であっても、ゲート絶縁層に対する割合が十分であるため寄生容量は十分に抑制される。
【０１１０】
本実施の形態によって、オンオフ比の高い薄膜トランジスタを得ることができ、良好な動特性を有する薄膜トランジスタを作製できる。よって、電気特性が高く信頼性のよい薄膜トランジスタを有する半導体装置を提供することができる。
【０１１１】
（実施の形態４）
本実施の形態では、半導体装置として電子ペーパーの例を示す。
【０１１２】
図１１は、液晶表示装置とは異なる半導体装置の例としてアクティブマトリクス型の電子ペーパーを示す。半導体装置の画素部に用いられる薄膜トランジスタ５８１としては、実施の形態３で示す画素部の薄膜トランジスタと同様に作製でき、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を半導体層として含む薄膜トランジスタである。また、実施の形態１に示したように、酸化物半導体層を挟んで対向する２つの電極側面をテーパ形状とすることで、電界緩和領域が設けられた信頼性の高い薄膜トランジスタを備えた電子ペーパを実現することができる。
【０１１３】
図１１の電子ペーパーは、ツイストボール表示方式を用いた表示装置の例である。ツイストボール表示方式とは、白と黒に塗り分けられた球形粒子を表示素子に用いる電極層である第１の電極層及び第２の電極層の間に配置し、第１の電極層及び第２の電極層に電位差を生じさせて球形粒子の向きを制御することにより、表示を行う方法である。
【０１１４】
薄膜トランジスタ５８１はボトムゲート構造の薄膜トランジスタであり、ソース電極層又はドレイン電極層は、第１の電極層５８７と、絶縁層５８５に形成する開口で接しており電気的に接続している。第１の電極層５８７と第２の電極層５８８との間には黒色領域５９０ａ及び白色領域５９０ｂを有し、周りに液体で満たされているキャビティ５９４を含む球形粒子５８９が設けられており、球形粒子５８９の周囲は樹脂等の充填材５９５で充填されている（図１１参照。）。
【０１１５】
また、ツイストボールの代わりに、電気泳動素子を用いることも可能である。透明な液体

と、正に帯電した白い微粒子と負に帯電した黒い微粒子とを封入した直径１０μｍ～２００μｍ程度のマイクロカプセルを用いる。第１の電極層と第２の電極層との間に設けられるマイクロカプセルは、第１の電極層と第２の電極層によって、電場が与えられると、白い微粒子と、黒い微粒子が逆の方向に移動し、白または黒を表示することができる。この原理を応用した表示素子が電気泳動表示素子であり、電子ペーパーとよばれている。電気泳動表示素子は、液晶表示素子に比べて反射率が高いため、補助ライトは不要であり、また消費電力が小さく、薄暗い場所でも表示部を認識することが可能である。また、表示部に電源が供給されない場合であっても、一度表示した像を保持することが可能であるため、電波発信源から表示機能付き半導体装置（単に表示装置、又は表示装置を具備する半導体装置ともいう）を遠ざけた場合であっても、表示された像を保存しておくことが可能となる。

【０１１６】

以上の工程により、半導体装置として製造コストが低減された電子ペーパーを作製することができる。

【０１１７】

本実施の形態は、実施の形態１、実施の形態２、または実施の形態３に記載した構成と適宜組み合わせて実施することが可能である。

【０１１８】

（実施の形態５）

本実施の形態では、半導体装置の一例である表示装置において、同一基板上に少なくとも駆動回路の一部と、画素部に配置する薄膜トランジスタを作製する例について以下に説明する。

【０１１９】

画素部に配置する薄膜トランジスタは、実施の形態１又は実施の形態２に従って形成する。また、実施の形態１又は実施の形態２に示す薄膜トランジスタはｎチャネル型ＴＦＴであるため、駆動回路のうち、ｎチャネル型ＴＦＴで構成することができる駆動回路の一部を画素部の薄膜トランジスタと同一基板上に形成する。

【０１２０】

半導体装置の一例であるアクティブマトリクス型液晶表示装置のブロック図の一例を図１２（Ａ）に示す。図１２（Ａ）に示す表示装置は、基板５３００上に表示素子を備えた画素を複数有する画素部５３０１と、各画素を選択する走査線駆動回路５３０２と、選択された画素へのビデオ信号の入力を制御する信号線駆動回路５３０３とを有する。

【０１２１】

また、実施の形態１又は実施の形態２に示す薄膜トランジスタは、ｎチャネル型ＴＦＴであり、ｎチャネル型ＴＦＴで構成する信号線駆動回路について図１３を用いて説明する。

【０１２２】

図１３に示す信号線駆動回路は、ドライバＩＣ５６０１、スイッチ群５６０２＿１～５６０２＿Ｍ、第１の配線５６１１、第２の配線５６１２、第３の配線５６１３及び配線５６２１＿１～５６２１＿Ｍを有する。スイッチ群５６０２＿１～５６０２＿Ｍそれぞれは、第１の薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃを有する。

【０１２３】

ドライバＩＣ５６０１は第１の配線５６１１、第２の配線５６１２、第３の配線５６１３及び配線５６２１＿１～５６２１＿Ｍに接続される。そして、スイッチ群５６０２＿１～５６０２＿Ｍそれぞれは、第１の配線５６１１、第２の配線５６１２、第３の配線５６１３及びスイッチ群５６０２＿１～５６０２＿Ｍそれぞれに対応した配線５６２１＿１～５６２１＿Ｍに接続される。そして、配線５６２１＿１～５６２１＿Ｍそれぞれは、第１の薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃを介して、３つの信号線に接続される。例えば、Ｊ列目の配線５６２１＿Ｊ（配線５６２１＿１～配線５６２１＿Ｍのうちいずれか一）は、スイッチ群５６０２

＿Ｊが有する第１の薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃを介して、信号線Ｓｊ－１、信号線Ｓｊ、信号線Ｓｊ＋１に接続される。

【０１２４】

なお、第１の配線５６１１、第２の配線５６１２、第３の配線５６１３には、それぞれ信号が入力される。

【０１２５】

なお、ドライバＩＣ５６０１は、単結晶基板上に形成されていることが望ましい。さらに、スイッチ群５６０２＿１～５６０２＿Ｍは、画素部と同一基板上に形成されていることが望ましい。したがって、ドライバＩＣ５６０１とスイッチ群５６０２＿１～５６０２＿ＭとはＦＰＣなどを介して接続するとよい。

【０１２６】

次に、図１３に示した信号線駆動回路の動作について、図１４のタイミングチャートを参照して説明する。なお、図１４のタイミングチャートは、ｉ行目の走査線Ｇｉが選択されている場合のタイミングチャートを示している。さらに、ｉ行目の走査線Ｇｉの選択期間は、第１のサブ選択期間Ｔ１、第２のサブ選択期間Ｔ２及び第３のサブ選択期間Ｔ３に分割されている。さらに、図１３の信号線駆動回路は、他の行の走査線が選択されている場合でも図１４と同様の動作をする。

【０１２７】

なお、図１４のタイミングチャートは、Ｊ列目の配線５６２１＿Ｊが第１の薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃを介して、信号線Ｓｊ－１、信号線Ｓｊ、信号線Ｓｊ＋１に接続される場合について示している。

【０１２８】

なお、図１４のタイミングチャートは、ｉ行目の走査線Ｇｉが選択されるタイミング、第１の薄膜トランジスタ５６０３ａのオン・オフのタイミング５７０３ａ、第２の薄膜トランジスタ５６０３ｂのオン・オフのタイミング５７０３ｂ、第３の薄膜トランジスタ５６０３ｃのオン・オフのタイミング５７０３ｃ及びＪ列目の配線５６２１＿Ｊに入力される信号５７２１＿Ｊを示している。

【０１２９】

なお、配線５６２１＿１～配線５６２１＿Ｍには第１のサブ選択期間Ｔ１、第２のサブ選択期間Ｔ２及び第３のサブ選択期間Ｔ３において、それぞれ別のビデオ信号が入力される。例えば、第１のサブ選択期間Ｔ１において配線５６２１＿Ｊに入力されるビデオ信号は信号線Ｓｊ－１に入力され、第２のサブ選択期間Ｔ２において配線５６２１＿Ｊに入力されるビデオ信号は信号線Ｓｊに入力され、第３のサブ選択期間Ｔ３において配線５６２１＿Ｊに入力されるビデオ信号は信号線Ｓｊ＋１に入力される。さらに、第１のサブ選択期間Ｔ１、第２のサブ選択期間Ｔ２及び第３のサブ選択期間Ｔ３において、配線５６２１＿Ｊに入力されるビデオ信号をそれぞれＤａｔａ＿ｊ－１、Ｄａｔａ＿ｊ、Ｄａｔａ＿ｊ＋１とする。

【０１３０】

図１４に示すように、第１のサブ選択期間Ｔ１において第１の薄膜トランジスタ５６０３ａがオンし、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊ－１が、第１の薄膜トランジスタ５６０３ａを介して信号線Ｓｊ－１に入力される。第２のサブ選択期間Ｔ２では、第２の薄膜トランジスタ５６０３ｂがオンし、第１の薄膜トランジスタ５６０３ａ及び第３の薄膜トランジスタ５６０３ｃがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊが、第２の薄膜トランジスタ５６０３ｂを介して信号線Ｓｊに入力される。第３のサブ選択期間Ｔ３では、第３の薄膜トランジスタ５６０３ｃがオンし、第１の薄膜トランジスタ５６０３ａ及び第２の薄膜トランジスタ５６０３ｂがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊ＋１が、第３の薄膜トランジスタ５６

０３ｃを介して信号線Ｓｊ＋１に入力される。
【０１３１】
以上のことから、図１３の信号線駆動回路は、１ゲート選択期間を３つに分割することで、１ゲート選択期間中に１つの配線５６２１から３つの信号線にビデオ信号を入力することができる。したがって、図１３の信号線駆動回路は、ドライバＩＣ５６０１が形成される基板と、画素部が形成されている基板との接続数を信号線の数に比べて約１／３にすることができる。接続数が約１／３になることによって、図１３の信号線駆動回路は、信頼性、歩留まりなどを向上できる。
【０１３２】
なお、図１３のように、１ゲート選択期間を複数のサブ選択期間に分割し、複数のサブ選択期間それぞれにおいて、ある１つの配線から複数の信号線それぞれにビデオ信号を入力することができれば、薄膜トランジスタの配置や数、駆動方法などは限定されない。
【０１３３】
例えば、３つ以上のサブ選択期間それぞれにおいて１つの配線から３つ以上の信号線それぞれにビデオ信号を入力する場合は、薄膜トランジスタ及び薄膜トランジスタを制御するための配線を追加すればよい。ただし、１ゲート選択期間を４つ以上のサブ選択期間に分割すると、１つのサブ選択期間が短くなる。したがって、１ゲート選択期間は、２つ又は３つのサブ選択期間に分割されることが望ましい。
【０１３４】
別の例として、図１５のタイミングチャートに示すように、１つの選択期間をプリチャージ期間Ｔｐ、第１のサブ選択期間Ｔ１、第２のサブ選択期間Ｔ２、第３の選択期間Ｔ３に分割してもよい。さらに、図１５のタイミングチャートは、ｉ行目の走査線Ｇｉが選択されるタイミング、第１の薄膜トランジスタ５６０３ａのオン・オフのタイミング５８０３ａ、第２の薄膜トランジスタ５６０３ｂのオン・オフのタイミング５８０３ｂ、第３の薄膜トランジスタ５６０３ｃのオン・オフのタイミング５８０３ｃ及びＪ列目の配線５６２１＿Ｊに入力される信号５８２１＿Ｊを示している。図１５に示すように、プリチャージ期間Ｔｐにおいて第１の薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃがオンする。このとき、配線５６２１＿Ｊに入力されるプリチャージ電圧Ｖｐが第１の薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃを介してそれぞれ信号線Ｓｊ－１、信号線Ｓｊ、信号線Ｓｊ＋１に入力される。第１のサブ選択期間Ｔ１において第１の薄膜トランジスタ５６０３ａがオンし、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊ－１が、第１の薄膜トランジスタ５６０３ａを介して信号線Ｓｊ－１に入力される。第２のサブ選択期間Ｔ２では、第２の薄膜トランジスタ５６０３ｂがオンし、第１の薄膜トランジスタ５６０３ａ及び第３の薄膜トランジスタ５６０３ｃがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊが、第２の薄膜トランジスタ５６０３ｂを介して信号線Ｓｊに入力される。第３のサブ選択期間Ｔ３では、第３の薄膜トランジスタ５６０３ｃがオンし、第１の薄膜トランジスタ５６０３ａ及び第２の薄膜トランジスタ５６０３ｂがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊ＋１が、第３の薄膜トランジスタ５６０３ｃを介して信号線Ｓｊ＋１に入力される。
【０１３５】
以上のことから、図１５のタイミングチャートを適用した図１３の信号線駆動回路は、サブ選択期間の前にプリチャージ選択期間を設けることによって、信号線をプリチャージできるため、画素へのビデオ信号の書き込みを高速に行うことができる。なお、図１５において、図１４と同様なものに関しては共通の符号を用いて示し、同一部分又は同様な機能を有する部分の詳細な説明は省略する。
【０１３６】
また、走査線駆動回路の構成について説明する。走査線駆動回路は、シフトレジスタ、バッファを有している。また場合によってはレベルシフタを有していても良い。走査線駆動

回路において、シフトレジスタにクロック信号（ＣＬＫ）及びスタートパルス信号（ＳＰ）が入力されることによって、選択信号が生成される。生成された選択信号はバッファにおいて緩衝増幅され、対応する走査線に供給される。走査線には、１ライン分の画素のトランジスタのゲート電極が接続されている。そして、１ライン分の画素のトランジスタを一斉にＯＮにしなくてはならないので、バッファは大きな電流を流すことが可能なものが用いられる。

【０１３７】

走査線駆動回路の一部に用いるシフトレジスタの一形態について図１６及び図１７を用いて説明する。

【０１３８】

図１６にシフトレジスタの回路構成を示す。図１６に示すシフトレジスタは、複数のフリップフロップ５７０１＿ｉ（フリップフロップ５７０１＿１～５７０１＿ｎのうちいずれか一）で構成される。また、第１のクロック信号、第２のクロック信号、スタートパルス信号、リセット信号が入力されて動作する。

【０１３９】

図１６のシフトレジスタの接続関係について説明する。図１６のシフトレジスタは、ｉ段目のフリップフロップ５７０１＿ｉ（フリップフロップ５７０１＿１～５７０１＿ｎのうちいずれか一）は、図１７に示した第１の配線５５０１が第７の配線５７１７＿ｉ－１に接続され、図１７に示した第２の配線５５０２が第７の配線５７１７＿ｉ＋１に接続され、図１７に示した第３の配線５５０３が第７の配線５７１７＿ｉに接続され、図１７に示した第６の配線５５０６が第５の配線５７１５に接続される。

【０１４０】

また、図１７に示した第４の配線５５０４が奇数段目のフリップフロップでは第２の配線５７１２に接続され、偶数段目のフリップフロップでは第３の配線５７１３に接続され、図１７に示した第５の配線５５０５が第４の配線５７１４に接続される。

【０１４１】

ただし、１段目のフリップフロップ５７０１＿１の図１７に示す第１の配線５５０１は第１の配線５７１１に接続され、ｎ段目のフリップフロップ５７０１＿ｎの図１７に示す第２の配線５５０２は第６の配線５７１６に接続される。

【０１４２】

なお、第１の配線５７１１、第２の配線５７１２、第３の配線５７１３、第６の配線５７１６を、それぞれ第１の信号線、第２の信号線、第３の信号線、第４の信号線と呼んでもよい。さらに、第４の配線５７１４、第５の配線５７１５を、それぞれ第１の電源線、第２の電源線と呼んでもよい。

【０１４３】

次に、図１６に示すフリップフロップの詳細について、図１７に示す。図１７に示すフリップフロップは、第１の薄膜トランジスタ５５７１、第２の薄膜トランジスタ５５７２、第３の薄膜トランジスタ５５７３、第４の薄膜トランジスタ５５７４、第５の薄膜トランジスタ５５７５、第６の薄膜トランジスタ５５７６、第７の薄膜トランジスタ５５７７及び第８の薄膜トランジスタ５５７８を有する。なお、第１の薄膜トランジスタ５５７１、第２の薄膜トランジスタ５５７２、第３の薄膜トランジスタ５５７３、第４の薄膜トランジスタ５５７４、第５の薄膜トランジスタ５５７５、第６の薄膜トランジスタ５５７６、第７の薄膜トランジスタ５５７７及び第８の薄膜トランジスタ５５７８は、ｎチャネル型トランジスタであり、ゲート・ソース間電圧（Ｖｇｓ）がしきい値電圧（Ｖｔｈ）を上回ったとき導通状態になるものとする。

【０１４４】

次に、図１６に示すフリップフロップの接続構成について、以下に示す。

【０１４５】

第１の薄膜トランジスタ５５７１の第１の電極（ソース電極またはドレイン電極の一方）が第５の配線５５０４に接続され、第１の薄膜トランジスタ５５７１の第２の電極（ソー

ス電極またはドレイン電極の他方）が第３の配線５５０３に接続される。
【０１４６】
第２の薄膜トランジスタ５５７２の第１の電極が第４の配線第６の配線５５０６に接続され、第２の薄膜トランジスタ５５７２第２の電極が第３の配線５５０３に接続される。
【０１４７】
第３の薄膜トランジスタ５５７３の第１の電極が第５の配線５５０５に接続され、第３の薄膜トランジスタ５５７３の第２の電極が第２の薄膜トランジスタ５５７２のゲート電極に接続され、第３の薄膜トランジスタ５５７３のゲート電極が第５の配線５５０５に接続される。
【０１４８】
第４の薄膜トランジスタ５５７４の第１の電極が第６の配線５５０６に接続され、第４の薄膜トランジスタ５５７４の第２の電極が第２の薄膜トランジスタ５５７２のゲート電極に接続され、第４の薄膜トランジスタ５５７４のゲート電極が第１の薄膜トランジスタ５５７１のゲート電極に接続される。
【０１４９】
第５の薄膜トランジスタ５５７５の第１の電極が第５の配線５５０５に接続され、第５の薄膜トランジスタ５５７５の第２の電極が第１の薄膜トランジスタ５５７１のゲート電極に接続され、第５の薄膜トランジスタ５５７５のゲート電極が第１の配線５５０１に接続される。
【０１５０】
第６の薄膜トランジスタ５５７６の第１の電極が第６の配線５５０６に接続され、第６の薄膜トランジスタ５５７６の第２の電極が第１の薄膜トランジスタ５５７１のゲート電極に接続され、第６の薄膜トランジスタ５５７６のゲート電極が第２の薄膜トランジスタ５５７２のゲート電極に接続される。
【０１５１】
第７の薄膜トランジスタ５５７７の第１の電極が第６の配線５５０６に接続され、第７の薄膜トランジスタ５５７７の第２の電極が第１の薄膜トランジスタ５５７１のゲート電極に接続され、第７の薄膜トランジスタ５５７７のゲート電極が第２の配線５５０２に接続される。第８の薄膜トランジスタ５５７８の第１の電極が第６の配線５５０６に接続され、第８の薄膜トランジスタ５５７８の第２の電極が第２の薄膜トランジスタ５５７２のゲート電極に接続され、第８の薄膜トランジスタ５５７８のゲート電極が第１の配線５５０１に接続される。
【０１５２】
なお、第１の薄膜トランジスタ５５７１のゲート電極、第４の薄膜トランジスタ５５７４のゲート電極、第５の薄膜トランジスタ５５７５の第２の電極、第６の薄膜トランジスタ５５７６の第２の電極及び第７の薄膜トランジスタ５５７７の第２の電極の接続箇所をノード５５４３とする。さらに、第２の薄膜トランジスタ５５７２のゲート電極、第３の薄膜トランジスタ５５７３の第２の電極、第４の薄膜トランジスタ５５７４の第２の電極、第６の薄膜トランジスタ５５７６のゲート電極及び第８の薄膜トランジスタ５５７８の第２の電極の接続箇所をノード５５４４とする。
【０１５３】
なお、第１の配線５５０１、第２の配線５５０２、第３の配線５５０３及び第４の配線５５０４を、それぞれ第１の信号線、第２の信号、第３の信号線、第４の信号線と呼んでもよい。さらに、第５の配線５５０５を第１の電源線、第６の配線５５０６を第２の電源線と呼んでもよい。
【０１５４】
また、信号線駆動回路及び走査線駆動回路を実施の形態１又は実施の形態２に示すｎチャネル型ＴＦＴのみで作製することも可能である。酸化物半導体層を用いるトランジスタの移動度は大きいため、駆動回路の駆動周波数を高くすることが可能となる。また、実施の形態１又は実施の形態２に示すｎチャネル型ＴＦＴはソース領域又はドレイン領域により

寄生容量が低減されるため、周波数特性（ｆ特性と呼ばれる）が高い。例えば、実施の形態１又は実施の形態２に示すｎチャネル型ＴＦＴを用いた走査線駆動回路は、高速に動作させることが出来るため、フレーム周波数を高くすること、または、黒画面挿入を実現することなども実現することが出来る。

【０１５５】

さらに、走査線駆動回路のトランジスタのチャネル幅を大きくすることや、複数の走査線駆動回路を配置することなどによって、さらに高いフレーム周波数を実現することが出来る。複数の走査線駆動回路を配置する場合は、偶数行の走査線を駆動する為の走査線駆動回路を片側に配置し、奇数行の走査線を駆動するための走査線駆動回路をその反対側に配置することにより、フレーム周波数を高くすることを実現することが出来る。

【０１５６】

また、半導体装置の一例であるアクティブマトリクス型発光表示装置を作製する場合、少なくとも一つの画素に複数の薄膜トランジスタを配置するため、走査線駆動回路を複数配置することが好ましい。アクティブマトリクス型発光表示装置のブロック図の一例を図１２（Ｂ）に示す。

【０１５７】

図１２（Ｂ）に示す発光表示装置は、基板５４００上に表示素子を備えた画素を複数有する画素部５４０１と、各画素を選択する第１の走査線駆動回路５４０２及び第２の走査線駆動回路５４０４と、選択された画素へのビデオ信号の入力を制御する信号線駆動回路５４０３とを有する。

【０１５８】

図１２（Ｂ）に示す発光表示装置の画素に入力されるビデオ信号をデジタル形式とする場合、画素はトランジスタのオンとオフの切り替えによって、発光もしくは非発光の状態となる。よって、面積階調法または時間階調法を用いて階調の表示を行うことができる。面積階調法は、１画素を複数の副画素に分割し、各副画素を独立にビデオ信号に基づいて駆動させることによって、階調表示を行う駆動法である。また時間階調法は、画素が発光する期間を制御することによって、階調表示を行う駆動法である。

【０１５９】

発光素子は、液晶素子などに比べて応答速度が高いので、液晶素子よりも時間階調法に適している。具体的に時間階調法で表示を行なう場合、１フレーム期間を複数のサブフレーム期間に分割する。そしてビデオ信号に従い、各サブフレーム期間において画素の発光素子を発光または非発光の状態にする。複数のサブフレーム期間に分割することによって、１フレーム期間中に画素が実際に発光する期間のトータルの長さを、ビデオ信号により制御することができ、階調を表示することができる。

【０１６０】

なお、図１２（Ｂ）に示す発光表示装置では、一つの画素にスイッチング用ＴＦＴと、電流制御用ＴＦＴとの２つを配置する場合、スイッチング用ＴＦＴのゲート配線である第１の走査線に入力される信号を第１走査線駆動回路５４０２で生成し、電流制御用ＴＦＴのゲート配線である第２の走査線に入力される信号を第２の走査線駆動回路５４０４で生成している例を示しているが、第１の走査線に入力される信号と、第２の走査線に入力される信号とを、共に１つの走査線駆動回路で生成するようにしても良い。また、例えば、スイッチング素子が有する各トランジスタの数によって、スイッチング素子の動作を制御するのに用いられる第１の走査線が、各画素に複数設けられることもあり得る。この場合、複数の第１の走査線に入力される信号を、全て１つの走査線駆動回路で生成しても良いし、複数の各走査線駆動回路で生成しても良い。

【０１６１】

また、発光表示装置においても、駆動回路のうち、ｎチャネル型ＴＦＴで構成することができる駆動回路の一部を画素部の薄膜トランジスタと同一基板上に形成することができる。また、信号線駆動回路及び走査線駆動回路を実施の形態１又は実施の形態２に示すｎチャネル型ＴＦＴのみで作製することも可能である。

【０１６２】
以上の工程により、半導体装置として信頼性の高い表示装置を作製することができる。
【０１６３】
本実施の形態は、他の実施の形態に記載した構成と適宜組み合わせて実施することが可能である。
【０１６４】
（実施の形態６）
本実施の形態では、半導体装置として発光表示装置の例を示す。表示装置の有する表示素子としては、ここではエレクトロルミネッセンスを利用する発光素子を用いて示す。エレクトロルミネッセンスを利用する発光素子は、発光材料が有機化合物であるか、無機化合物であるかによって区別され、一般的に、前者は有機ＥＬ素子、後者は無機ＥＬ素子と呼ばれている。
【０１６５】
有機ＥＬ素子は、発光素子に電圧を印加することにより、一対の電極から電子および正孔がそれぞれ発光性の有機化合物を含む層に注入され、電流が流れる。そして、それらキャリア（電子および正孔）が再結合することにより、発光性の有機化合物が励起状態を形成し、その励起状態が基底状態に戻る際に発光する。このようなメカニズムから、このような発光素子は、電流励起型の発光素子と呼ばれる。
【０１６６】
無機ＥＬ素子は、その素子構成により、分散型無機ＥＬ素子と薄膜型無機ＥＬ素子とに分類される。分散型無機ＥＬ素子は、発光材料の粒子をバインダ中に分散させた発光層を有するものであり、発光メカニズムはドナー準位とアクセプター準位を利用するドナー－アクセプター再結合型発光である。薄膜型無機ＥＬ素子は、発光層を誘電体層で挟み込み、さらにそれを電極で挟んだ構造であり、発光メカニズムは金属イオンの内殻電子遷移を利用する局在型発光である。なお、ここでは、発光素子として有機ＥＬ素子を用いて説明する。
【０１６７】
図１８は、半導体装置の例としてデジタル時間階調駆動を適用可能な画素構成の一例を示す図である。
【０１６８】
デジタル時間階調駆動を適用可能な画素の構成及び画素の動作について説明する。ここでは酸化物半導体層（Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜）をチャネル形成領域に用いるｎチャネル型のトランジスタを１つの画素に２つ用いる例を示す。
【０１６９】
画素６４００は、スイッチング用トランジスタ６４０１、駆動用トランジスタ６４０２、発光素子６４０４及び容量素子６４０３を有している。スイッチング用トランジスタ６４０１はゲートが走査線６４０６に接続され、第１電極（ソース電極及びドレイン電極の一方）が信号線６４０５に接続され、第２電極（ソース電極及びドレイン電極の他方）が駆動用トランジスタ６４０２のゲートに接続されている。駆動用トランジスタ６４０２は、ゲートが容量素子６４０３を介して電源線６４０７に接続され、第１電極が電源線６４０７に接続され、第２電極が発光素子６４０４の第１電極（画素電極）に接続されている。発光素子６４０４の第２電極は共通電極６４０８に相当する。
【０１７０】
なお、発光素子６４０４の第２電極（共通電極６４０８）には低電源電位が設定されている。なお、低電源電位とは、電源線６４０７に設定される高電源電位を基準にして低電源電位＜高電源電位を満たす電位であり、低電源電位としては例えばＧＮＤ、０Ｖなどが設定されていても良い。この高電源電位と低電源電位との電位差を発光素子６４０４に印加して、発光素子６４０４に電流を流して発光素子６４０４を発光させるため、高電源電位と低電源電位との電位差が発光素子６４０４の順方向しきい値電圧以上となるようにそれぞれの電位を設定する。

【０１７１】
なお、容量素子６４０３は駆動用トランジスタ６４０２のゲート容量を代用して省略することも可能である。駆動用トランジスタ６４０２のゲート容量については、チャネル領域とゲート電極との間で容量が形成されていてもよい。
【０１７２】
ここで、電圧入力電圧駆動方式の場合には、駆動用トランジスタ６４０２のゲートには、駆動用トランジスタ６４０２が十分にオンするか、オフするかの二つの状態となるようなビデオ信号を入力する。つまり、駆動用トランジスタ６４０２は線形領域で動作させる。駆動用トランジスタ６４０２は線形領域で動作させるため、電源線６４０７の電圧よりも高い電圧を駆動用トランジスタ６４０２のゲートにかける。なお、信号線６４０５には、（電源線電圧＋駆動用トランジスタ６４０２のＶｔｈ）以上の電圧をかける。
【０１７３】
また、デジタル時間階調駆動に代えて、アナログ階調駆動を行う場合、信号の入力を異ならせることで、図１８と同じ画素構成を用いることができる。
【０１７４】
アナログ階調駆動を行う場合、駆動用トランジスタ６４０２のゲートに発光素子６４０４の順方向電圧＋駆動用トランジスタ６４０２のＶｔｈ以上の電圧をかける。発光素子６４０４の順方向電圧とは、所望の輝度とする場合の電圧を指しており、少なくとも順方向しきい値電圧を含む。なお、駆動用トランジスタ６４０２が飽和領域で動作するようなビデオ信号を入力することで、発光素子６４０４に電流を流すことができる。駆動用トランジスタ６４０２を飽和領域で動作させるため、電源線６４０７の電位は、駆動用トランジスタ６４０２のゲート電位よりも高くする。ビデオ信号をアナログとすることで、発光素子６４０４にビデオ信号に応じた電流を流し、アナログ階調駆動を行うことができる。
【０１７５】
なお、図１８に示す画素構成は、これに限定されない。例えば、図１８に示す画素に新たにスイッチ、抵抗素子、容量素子、トランジスタ又は論理回路などを追加してもよい。
【０１７６】
次に、発光素子の構成について、図１９（Ａ）、図１９（Ｂ）、図１９（Ｃ）を用いて説明する。ここでは、駆動用ＴＦＴが図１（Ｂ）に示す薄膜トランジスタ１７０の場合を例に挙げて、画素の断面構造について説明する。図１９（Ａ）、図１９（Ｂ）、図１９（Ｃ）の半導体装置に用いられる駆動用ＴＦＴであるＴＦＴ７００１、７０１１、７０２１は、実施の形態１で示す薄膜トランジスタ１７０と同様に作製でき、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を半導体層として含む高い電気特性を有する薄膜トランジスタである。
【０１７７】
発光素子は発光を取り出すために少なくとも陽極又は陰極の一方が透明であればよい。そして、基板上に薄膜トランジスタ及び発光素子を形成し、基板とは逆側の面から発光を取り出す上面射出や、基板側の面から発光を取り出す下面射出や、基板側及び基板とは反対側の面から発光を取り出す両面射出構造の発光素子があり、図１８に示す画素構成はどの射出構造の発光素子にも適用することができる。
【０１７８】
上面射出構造の発光素子について図１９（Ａ）を用いて説明する。
【０１７９】
図１９（Ａ）に、駆動用ＴＦＴであるＴＦＴ７００１が図１（Ｂ）に示す薄膜トランジスタ１７０であり、発光素子７００２から発せられる光が陽極７００５側に抜ける場合の、画素の断面図を示す。図１９（Ａ）では、発光素子７００２の陰極７００３と駆動用ＴＦＴであるＴＦＴ７００１が電気的に接続されており、陰極７００３上に発光層７００４、陽極７００５が順に積層されている。陰極７００３は仕事関数が小さく、なおかつ光を反射する導電膜であれば様々の材料を用いることができる。例えば、Ｃａ、Ａｌ、ＣａＦ、ＭｇＡｇ、ＡｌＬｉ等が望ましい。そして発光層７００４は、単数の層で構成されていても、複数の層が積層されるように構成されていてもどちらでも良い。複数の層で構成され

ている場合、陰極７００３上に電子注入層、電子輸送層、発光層、ホール輸送層、ホール注入層の順に積層する。なおこれらの層を全て設ける必要はない。陽極７００５は光を透過する透光性を有する導電性材料を用いて形成し、例えば酸化タングステンを含むインジウム酸化物、酸化タングステンを含むインジウム亜鉛酸化物、酸化チタンを含むインジウム酸化物、酸化チタンを含むインジウム錫酸化物、インジウム錫酸化物（以下、ＩＴＯと示す。）、インジウム亜鉛酸化物、酸化ケイ素を添加したインジウム錫酸化物などの透光性を有する導電性導電膜を用いても良い。

【０１８０】

陰極７００３及び陽極７００５で発光層７００４を挟んでいる領域が発光素子７００２に相当する。図１９（Ａ）に示した画素の場合、発光素子７００２から発せられる光は、矢印で示すように陽極７００５側に射出する。

【０１８１】

次に、下面射出構造の発光素子について図１９（Ｂ）を用いて説明する。駆動用ＴＦＴ７０１１が図１（Ａ）に示す薄膜トランジスタ１７０であり、発光素子７０１２から発せられる光が陰極７０１３側に射出する場合の、画素の断面図を示す。図１９（Ｂ）では、駆動用ＴＦＴ７０１１と電気的に接続された透光性を有する導電膜７０１７上に、発光素子７０１２の陰極７０１３が成膜されており、陰極７０１３上に発光層７０１４、陽極７０１５が順に積層されている。なお、陽極７０１５が透光性を有する場合、陽極上を覆うように、光を反射または遮蔽するための遮蔽膜７０１６が成膜されていてもよい。陰極７０１３は、図１９（Ａ）の場合と同様に、仕事関数が小さい導電性材料であれば様々な材料を用いることができる。ただしその膜厚は、光を透過する程度（好ましくは、５ｎｍ～３０ｎｍ程度）とする。例えば２０ｎｍの膜厚を有するアルミニウム膜を、陰極７０１３として用いることができる。そして発光層７０１４は、図１９（Ａ）と同様に、単数の層で構成されていても、複数の層が積層されるように構成されていてもどちらでも良い。陽極７０１５は光を透過する必要はないが、図１９（Ａ）と同様に、透光性を有する導電性材料を用いて形成することができる。そして遮蔽膜７０１６は、例えば光を反射する金属等を用いることができるが、金属膜に限定されない。例えば黒の顔料を添加した樹脂等を用いることもできる。

【０１８２】

陰極７０１３及び陽極７０１５で、発光層７０１４を挟んでいる領域が発光素子７０１２に相当する。図１９（Ｂ）に示した画素の場合、発光素子７０１２から発せられる光は、矢印で示すように陰極７０１３側に射出する。

【０１８３】

次に、両面射出構造の発光素子について、図１９（Ｃ）を用いて説明する。図１９（Ｃ）では、駆動用ＴＦＴ７０２１と電気的に接続された透光性を有する導電膜７０２７上に、発光素子７０２２の陰極７０２３が成膜されており、陰極７０２３上に発光層７０２４、陽極７０２５が順に積層されている。陰極７０２３は、図１９（Ａ）の場合と同様に、仕事関数が小さい導電性材料であれば様々な材料を用いることができる。ただしその膜厚は、光を透過する程度とする。例えば２０ｎｍの膜厚を有するＡｌを、陰極７０２３として用いることができる。そして発光層７０２４は、図１９（Ａ）と同様に、単数の層で構成されていても、複数の層が積層されるように構成されていてもどちらでも良い。陽極７０２５は、図１９（Ａ）と同様に、光を透過する透光性を有する導電性材料を用いて形成することができる。

【０１８４】

陰極７０２３と、発光層７０２４と、陽極７０２５とが重なっている部分が発光素子７０２２に相当する。図１９（Ｃ）に示した画素の場合、発光素子７０２２から発せられる光は、矢印で示すように陽極７０２５側と陰極７０２３側の両方に射出する。

【０１８５】

なお、ここでは、発光素子として有機ＥＬ素子について述べたが、発光素子として無機ＥＬ素子を設けることも可能である。

【０１８６】
なお本実施の形態では、発光素子の駆動を制御する薄膜トランジスタ（駆動用ＴＦＴ）と発光素子が電気的に接続されている例を示したが、駆動用ＴＦＴと発光素子との間に電流制御用ＴＦＴが接続されている構成であってもよい。
【０１８７】
なお本実施の形態で示す半導体装置は、図１９（Ａ）、図１９（Ｂ）、図１９（Ｃ）に示した構成に限定されるものではなく、開示した技術的思想に基づく各種の変形が可能である。
【０１８８】
次に、半導体装置の一形態に相当する発光表示パネル（発光パネルともいう）の上面及び断面について、図２０（Ａ）、図２０（Ｂ）を用いて説明する。図２０（Ａ）は、第１の基板上に形成された薄膜トランジスタ及び発光素子を、第２の基板との間にシール材によって封止した、パネルの上面図であり、図２０（Ｂ）は、図２０（Ａ）のＨ－Ｉにおける断面図に相当する。
【０１８９】
第１の基板４５０１上に設けられた画素部４５０２、信号線駆動回路４５０３ａ、４５０３ｂ、及び走査線駆動回路４５０４ａ、４５０４ｂを囲むようにして、シール材４５０５が設けられている。また画素部４５０２、信号線駆動回路４５０３ａ、４５０３ｂ、及び走査線駆動回路４５０４ａ、４５０４ｂの上に第２の基板４５０６が設けられている。よって画素部４５０２、信号線駆動回路４５０３ａ、４５０３ｂ、及び走査線駆動回路４５０４ａ、４５０４ｂは、第１の基板４５０１とシール材４５０５と第２の基板４５０６とによって、充填材４５０７と共に密封されている。このように外気に曝されないように気密性が高く、脱ガスの少ない保護フィルム（貼り合わせフィルム、紫外線硬化樹脂フィルム等）やカバー材でパッケージング（封入）することが好ましい。
【０１９０】
また第１の基板４５０１上に設けられた画素部４５０２、信号線駆動回路４５０３ａ、４５０３ｂ、及び走査線駆動回路４５０４ａ、４５０４ｂは、薄膜トランジスタを複数有しており、図２０（Ｂ）では、画素部４５０２に含まれる薄膜トランジスタ４５１０と、信号線駆動回路４５０３ａに含まれる薄膜トランジスタ４５０９とを例示している。
【０１９１】
薄膜トランジスタ４５０９、４５１０は、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を半導体層として含む信頼性の高い実施の形態１に示す薄膜トランジスタを適用することができる。
【０１９２】
また４５１１は発光素子に相当し、発光素子４５１１が有する画素電極である第１の電極層４５１７は、薄膜トランジスタ４５１０のソース電極層またはドレイン電極層と電気的に接続されている。なお発光素子４５１１の構成は、第１の電極層４５１７、電界発光層４５１２、第２の電極層４５１３の積層構造であるが、本実施の形態に示した構成に限定されない。発光素子４５１１から取り出す光の方向などに合わせて、発光素子４５１１の構成は適宜変えることができる。
【０１９３】
隔壁４５２０は、有機樹脂膜、無機絶縁膜または有機ポリシロキサンを用いて形成する。特に感光性の材料を用い、第１の電極層４５１７上に開口部を形成し、その開口部の側壁が連続した曲率を持って形成される傾斜面となるように形成することが好ましい。
【０１９４】
電界発光層４５１２は、単数の層で構成されていても、複数の層が積層されるように構成されていてもどちらでも良い。
【０１９５】
発光素子４５１１に酸素、水素、水分、二酸化炭素等が侵入しないように、第２の電極層４５１３及び隔壁４５２０上に保護膜を形成してもよい。保護膜としては、窒化珪素膜、窒化酸化珪素膜、ＤＬＣ膜等を形成することができる。

【０１９６】
また、信号線駆動回路４５０３ａ、４５０３ｂ、走査線駆動回路４５０４ａ、４５０４ｂ、または画素部４５０２に与えられる各種信号及び電位は、ＦＰＣ４５１８ａ、４５１８ｂから供給されている。
【０１９７】
本実施の形態では、接続端子電極４５１５が、発光素子４５１１が有する第１の電極層４５１７と同じ導電膜から形成され、端子電極４５１６は、薄膜トランジスタ４５０９、４５１０が有するソース電極層及びドレイン電極層と同じ導電膜から形成されている。
【０１９８】
接続端子電極４５１５は、ＦＰＣ４５１８ａが有する端子と、異方性導電膜４５１９を介して電気的に接続されている。
【０１９９】
発光素子４５１１からの光の取り出し方向に位置する基板には、第２の基板は透光性でなければならない。その場合には、ガラス板、プラスチック板、ポリエステルフィルムまたはアクリルフィルムのような透光性を有する材料を用いる。
【０２００】
また、充填材４５０７としては窒素やアルゴンなどの不活性な気体の他に、紫外線硬化樹脂または熱硬化樹脂を用いることができ、ＰＶＣ（ポリビニルクロライド）、アクリル、ポリイミド、エポキシ樹脂、シリコン樹脂、ＰＶＢ（ポリビニルブチラル）またはＥＶＡ（エチレンビニルアセテート）を用いることができる。
【０２０１】
また、必要であれば、発光素子の射出面に偏光板、又は円偏光板（楕円偏光板を含む）、位相差板（λ／４板、λ／２板）、カラーフィルタなどの光学フィルムを適宜設けてもよい。また、偏光板又は円偏光板に反射防止膜を設けてもよい。例えば、表面の凹凸により反射光を拡散し、映り込みを低減できるアンチグレア処理を施すことができる。
【０２０２】
信号線駆動回路４５０３ａ、４５０３ｂ、及び走査線駆動回路４５０４ａ、４５０４ｂは、別途用意された単結晶半導体基板、或いは絶縁基板上に単結晶半導体膜又は多結晶半導体膜によって形成された駆動回路で実装されていてもよい。また、信号線駆動回路のみ、或いは一部、又は走査線駆動回路のみ、或いは一部のみを別途形成して実装しても良く、本実施の形態は図２０（Ａ）及び図２０（Ｂ）の構成に限定されない。
【０２０３】
以上の工程により、製造コストを低減した発光表示装置（表示パネル）を作製することができる。
【０２０４】
本実施の形態は、実施の形態１、実施の形態２、または実施の形態３に記載した構成と適宜組み合わせて実施することが可能である。
【０２０５】
（実施の形態７）
本実施の形態では、半導体装置の一形態に相当する液晶表示パネルの上面及び断面について、図２１（Ａ１）、図２１（Ａ２）、図２１（Ｂ）を用いて説明する。図２１（Ａ１）、図２１（Ａ２）は、第１の基板４００１上に形成された実施の形態１で示したＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を半導体層として含む薄膜トランジスタ４０１０、４０１１、及び液晶素子４０１３を、第２の基板４００６との間にシール材４００５によって封止した、パネルの上面図であり、図２１（Ｂ）は、図２１（Ａ１）、図２１（Ａ２）のＭ－Ｎにおける断面図に相当する。
【０２０６】
第１の基板４００１上に設けられた画素部４００２と、走査線駆動回路４００４とを囲むようにして、シール材４００５が設けられている。また画素部４００２と、走査線駆動回路４００４の上に第２の基板４００６が設けられている。よって画素部４００２と、走査

線駆動回路４００４とは、第１の基板４００１とシール材４００５と第２の基板４００６とによって、液晶層４００８と共に封止されている。また第１の基板４００１上のシール材４００５によって囲まれている領域とは異なる領域に、別途用意された基板上に単結晶半導体膜又は多結晶半導体膜で形成された信号線駆動回路４００３が実装されている。

【０２０７】

なお、別途形成した駆動回路の接続方法は、特に限定されるものではなく、ＣＯＧ方法、ワイヤボンディング方法、或いはＴＡＢ方法などを用いることができる。図２１（Ａ１）は、ＣＯＧ方法により信号線駆動回路４００３を実装する例であり、図２１（Ａ２）は、ＴＡＢ方法により信号線駆動回路４００３を実装する例である。

【０２０８】

また第１の基板４００１上に設けられた画素部４００２と、走査線駆動回路４００４は、薄膜トランジスタを複数有しており、図２１（Ｂ）では、画素部４００２に含まれる薄膜トランジスタ４０１０と、走査線駆動回路４００４に含まれる薄膜トランジスタ４０１１とを例示している。薄膜トランジスタ４０１０、４０１１上には絶縁層４０２０、４０２１が設けられている。

【０２０９】

薄膜トランジスタ４０１０、４０１１は、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を半導体層として含む実施の形態１に示す薄膜トランジスタを適用することができる。薄膜トランジスタ４０１１は、実施の形態１の図１に示した薄膜トランジスタ１７０に相当する。

【０２１０】

また、液晶素子４０１３が有する画素電極層４０３０は、薄膜トランジスタ４０１０と電気的に接続されている。そして液晶素子４０１３の対向電極層４０３１は第２の基板４００６上に形成されている。画素電極層４０３０と対向電極層４０３１と液晶層４００８とが重なっている部分が、液晶素子４０１３に相当する。なお、画素電極層４０３０、対向電極層４０３１はそれぞれ配向膜として機能する絶縁層４０３２、４０３３が設けられ、絶縁層４０３２、４０３３を介して液晶層４００８を挟持している。

【０２１１】

なお、第１の基板４００１、第２の基板４００６としては、ガラス、金属（代表的にはステンレス）、セラミックス、プラスチックを用いることができる。プラスチックとしては、ＦＲＰ（Ｆｉｂｅｒｇｌａｓｓ－Ｒｅｉｎｆｏｒｃｅｄ　Ｐｌａｓｔｉｃｓ）板、ＰＶＦ（ポリビニルフルオライド）フィルム、ポリエステルフィルムまたはアクリル樹脂フィルムを用いることができる。また、アルミニウムホイルをＰＶＦフィルムやポリエステルフィルムで挟んだ構造のシートを用いることもできる。

【０２１２】

また４０３５は絶縁膜を選択的にエッチングすることで得られる柱状のスペーサであり、画素電極層４０３０と対向電極層４０３１との間の距離（セルギャップ）を制御するために設けられている。なお球状のスペーサを用いていても良い。また、対向電極層４０３１は、薄膜トランジスタ４０１０と同一基板上に設けられる共通電位線と電気的に接続される。共通接続部を用いて、一対の基板間に配置される導電性粒子を介して対向電極層４０３１と共通電位線とを電気的に接続することができる。なお、導電性粒子はシール材４００５に含有させる。

【０２１３】

また、配向膜を用いないブルー相を示す液晶を用いてもよい。ブルー相は液晶相の一つであり、コレステリック液晶を昇温していくと、コレステリック相から等方相へ転移する直前に発現する相である。ブルー相は狭い温度範囲でしか発現しないため、温度範囲を改善するために５重量％以上のカイラル剤を混合させた液晶組成物を用いて液晶層４００８に用いる。ブルー相を示す液晶とカイラル剤とを含む液晶組成物は、応答速度が１０μｓ～１００μｓと短く、光学的等方性であるため配向処理が不要であり、視野角依存性が小さい。

【０２１４】

なお本実施の形態は透過型液晶表示装置の例であるが、反射型液晶表示装置でも半透過型液晶表示装置でも適用できる。

【０２１５】

また、本実施の形態の液晶表示装置では、基板の外側（視認側）に偏光板を設け、内側に着色層、表示素子に用いる電極層という順に設ける例を示すが、偏光板は基板の内側に設けてもよい。また、偏光板と着色層の積層構造も本実施の形態に限定されず、偏光板及び着色層の材料や作製工程条件によって適宜設定すればよい。また、ブラックマトリクスとして機能する遮光膜を設けてもよい。

【０２１６】

また、本実施の形態では、薄膜トランジスタの表面凹凸を低減するため、及び薄膜トランジスタの信頼性を向上させるため、実施の形態１で得られた薄膜トランジスタを保護膜や平坦化絶縁膜として機能する絶縁層（絶縁層４０２０、絶縁層４０２１）で覆う構成となっている。なお、保護膜は、大気中に浮遊する有機物や金属物、水蒸気などの汚染不純物の侵入を防ぐためのものであり、緻密な膜が好ましい。保護膜は、スパッタ法を用いて、酸化珪素膜、窒化珪素膜、酸化窒化珪素膜、窒化酸化珪素膜、酸化アルミニウム膜、窒化アルミニウム膜、酸化窒化アルミニウム膜、又は窒化酸化アルミニウム膜の単層、又は積層で形成すればよい。本実施の形態では保護膜をスパッタ法で形成する例を示すが、特に限定されずＰＣＶＤ法などの種々の方法で形成すればよい。

【０２１７】

ここでは、保護膜として積層構造の絶縁層４０２０を形成する。ここでは、絶縁層４０２０の一層目として、スパッタ法を用いて酸化珪素膜を形成する。保護膜として酸化珪素膜を用いると、ソース電極層及びドレイン電極層として用いるアルミニウム膜のヒロック防止に効果がある。

【０２１８】

また、保護膜の二層目として絶縁層を形成する。ここでは、ここでは、絶縁層４０２０の二層目として、スパッタ法を用いて窒化珪素膜を形成する。保護膜として窒化珪素膜を用いると、ナトリウム等のイオンが半導体領域中に侵入して、ＴＦＴの電気特性を変化させることを抑制することができる。

【０２１９】

また、保護膜を形成した後に、半導体層のアニール（３００℃～４００℃）を行ってもよい。

【０２２０】

また、平坦化絶縁膜として絶縁層４０２１を形成する。絶縁層４０２１としては、ポリイミド、アクリル、ポリイミド、ベンゾシクロブテン、ポリアミド、エポキシ等の、耐熱性を有する有機材料を用いることができる。また上記有機材料の他に、低誘電率材料（ｌｏｗ－ｋ材料）、シロキサン系樹脂、ＰＳＧ（リンガラス）、ＢＰＳＧ（リンボロンガラス）等を用いることができる。なお、これらの材料で形成される絶縁膜を複数積層させることで、絶縁層４０２１を形成してもよい。

【０２２１】

なおシロキサン系樹脂とは、シロキサン系材料を出発材料として形成されたＳｉ－Ｏ－Ｓｉ結合を含む樹脂に相当する。シロキサン系樹脂は置換基としては有機基（例えばアルキル基やアリール基）やフルオロ基を用いても良い。また、有機基はフルオロ基を有していても良い。

【０２２２】

絶縁層４０２１の形成法は、特に限定されず、その材料に応じて、スパッタ法、ＳＯＧ法、スピンコート、ディップ、スプレー塗布、液滴吐出法（インクジェット法、スクリーン印刷、オフセット印刷等）、ドクターナイフ、ロールコーター、カーテンコーター、ナイフコーター等を用いることができる。絶縁層４０２１を材料液を用いて形成する場合、ベークする工程で同時に、半導体層のアニール（３００℃～４００℃）を行ってもよい。絶縁層４０２１の焼成工程と半導体層のアニールを兼ねることで効率よく半導体装置を作製

することが可能となる。
【０２２３】
画素電極層４０３０、対向電極層４０３１は、酸化タングステンを含むインジウム酸化物、酸化タングステンを含むインジウム亜鉛酸化物、酸化チタンを含むインジウム酸化物、酸化チタンを含むインジウム錫酸化物、インジウム錫酸化物（以下、ＩＴＯと示す。）、インジウム亜鉛酸化物、酸化ケイ素を添加したインジウム錫酸化物などの透光性を有する導電性材料を用いることができる。
【０２２４】
また、画素電極層４０３０、対向電極層４０３１として、導電性高分子（導電性ポリマーともいう）を含む導電性組成物を用いて形成することができる。導電性組成物を用いて形成した画素電極は、シート抵抗が１００００Ω／□以下、波長５５０ｎｍにおける透光率が７０％以上であることが好ましい。また、導電性組成物に含まれる導電性高分子の抵抗率が０．１Ω・ｃｍ以下であることが好ましい。
【０２２５】
導電性高分子としては、いわゆるπ電子共役系導電性高分子が用いることができる。例えば、ポリアニリンまたはその誘導体、ポリピロールまたはその誘導体、ポリチオフェンまたはその誘導体、若しくはこれらの２種以上の共重合体などがあげられる。
【０２２６】
また別途形成された信号線駆動回路４００３と、走査線駆動回路４００４または画素部４００２に与えられる各種信号及び電位は、ＦＰＣ４０１８から供給されている。
【０２２７】
本実施の形態では、接続端子電極４０１５が、液晶素子４０１３が有する画素電極層４０３０と同じ導電膜から形成され、端子電極４０１６は、薄膜トランジスタ４０１０、４０１１のソース電極層及びドレイン電極層と同じ導電膜で形成されている。
【０２２８】
接続端子電極４０１５は、ＦＰＣ４０１８が有する端子と、異方性導電膜４０１９を介して電気的に接続されている。
【０２２９】
また図２１（Ａ１）、図２１（Ａ２）においては、信号線駆動回路４００３を別途形成し、第１の基板４００１に実装している例を示しているが、本実施の形態はこの構成に限定されない。走査線駆動回路を別途形成して実装しても良いし、信号線駆動回路の一部または走査線駆動回路の一部のみを別途形成して実装しても良い。
【０２３０】
図２２は、ＴＦＴ基板２６００を用いて半導体装置として液晶表示モジュールを構成する一例を示している。
【０２３１】
図２２は液晶表示モジュールの一例であり、ＴＦＴ基板２６００と対向基板２６０１がシール材２６０２により固着され、その間にＴＦＴ等を含む画素部２６０３、液晶層を含む表示素子２６０４、着色層２６０５、偏光板２６０６が設けられ表示領域を形成している。着色層２６０５はカラー表示を行う場合に必要であり、ＲＧＢ方式の場合は、赤、緑、青の各色に対応した着色層が各画素に対応して設けられている。ＴＦＴ基板２６００と対向基板２６０１の外側には偏光板２６０６、偏光板２６０７、拡散板２６１３が配設されている。光源は冷陰極管２６１０と反射板２６１１により構成され、回路基板２６１２は、フレキシブル配線基板２６０９によりＴＦＴ基板２６００の配線回路部２６０８と接続され、コントロール回路や電源回路などの外部回路が組みこまれている。また偏光板と、液晶層との間に位相差板を有した状態で積層してもよい。
【０２３２】
液晶表示モジュールには、ＴＮ（Ｔｗｉｓｔｅｄ　Ｎｅｍａｔｉｃ）モード、ＩＰＳ（Ｉｎ－Ｐｌａｎｅ－Ｓｗｉｔｃｈｉｎｇ）モード、ＦＦＳ（Ｆｒｉｎｇｅ　Ｆｉｅｌｄ　Ｓｗｉｔｃｈｉｎｇ）モード、ＭＶＡ（Ｍｕｌｔｉ－ｄｏｍａｉｎ　Ｖｅｒｔｉｃａｌ　Ａ

ｌｉｇｎｍｅｎｔ）モード、ＰＶＡ（Ｐａｔｔｅｒｎｅｄ　Ｖｅｒｔｉｃａｌ　Ａｌｉｇｎｍｅｎｔ）、ＡＳＭ（Ａｘｉａｌｌｙ　Ｓｙｍｍｅｔｒｉｃ　ａｌｉｇｎｅｄ　Ｍｉｃｒｏ－ｃｅｌｌ）モード、ＯＣＢ（Ｏｐｔｉｃａｌ　Ｃｏｍｐｅｎｓａｔｅｄ　Ｂｉｒｅｆｒｉｎｇｅｎｃｅ）モード、ＦＬＣ（Ｆｅｒｒｏｅｌｅｃｔｒｉｃ　Ｌｉｑｕｉｄ　Ｃｒｙｓｔａｌ）モード、ＡＦＬＣ（ＡｎｔｉＦｅｒｒｏｅｌｅｃｔｒｉｃ　Ｌｉｑｕｉｄ　Ｃｒｙｓｔａｌ）などを用いることができる。

【０２３３】

以上の工程により、半導体装置として製造コストを低減した液晶表示パネルを作製することができる。

【０２３４】

本実施の形態は、実施の形態１、実施の形態２、または実施の形態３に記載した構成と適宜組み合わせて実施することが可能である。

【０２３５】

（実施の形態８）

電子ペーパーは、情報を表示するものであればあらゆる分野の電子機器に用いることが可能である。例えば、電子ペーパーを用いて、電子書籍（電子ブック）、ポスター、電車などの乗り物の車内広告、クレジットカード等の各種カードにおける表示等に適用することができる。電子機器の一例を図２３、図２４に示す。

【０２３６】

図２３（Ａ）は、電子ペーパーで作られたポスター２６３１を示している。広告媒体が紙の印刷物である場合には、広告の交換は人手によって行われるが、本実施の形態３を適用した電子ペーパーを用いれば短時間で広告の表示を変えることができる。また、表示も崩れることなく安定した画像が得られる。なお、ポスターは無線で情報を送受信できる構成としてもよい。

【０２３７】

また、図２３（Ｂ）は、電車などの乗り物の車内広告２６３２を示している。広告媒体が紙の印刷物である場合には、広告の交換は人手によって行われるが、本実施の形態３を適用した電子ペーパーを用いれば人手を多くかけることなく短時間で広告の表示を変えることができる。また表示も崩れることなく安定した画像が得られる。なお、ポスターは無線で情報を送受信できる構成としてもよい。

【０２３８】

また、図２４は、電子書籍２７００の一例を示している。例えば、電子書籍２７００は、筐体２７０１および筐体２７０３の２つの筐体で構成されている。筐体２７０１および筐体２７０３は、軸部２７１１により一体とされており、該軸部２７１１を軸として開閉動作を行うことができる。このような構成により、紙の書籍のような動作を行うことが可能となる。

【０２３９】

筐体２７０１には表示部２７０５が組み込まれ、筐体２７０３には表示部２７０７が組み込まれている。表示部２７０５および表示部２７０７は、続き画面を表示する構成としてもよいし、異なる画面を表示する構成としてもよい。異なる画面を表示する構成とすることで、例えば右側の表示部（図２４では表示部２７０５）に文章を表示し、左側の表示部（図２４では表示部２７０７）に画像を表示することができる。

【０２４０】

また、図２４では、筐体２７０１に操作部などを備えた例を示している。例えば、筐体２７０１において、電源２７２１、操作キー２７２３、スピーカ２７２５などを備えている。操作キー２７２３により、頁を送ることができる。なお、筐体の表示部と同一面にキーボードやポインティングディバイスなどを備える構成としてもよい。また、筐体の裏面や側面に、外部接続用端子（イヤホン端子、ＵＳＢ端子、またはＡＣアダプタおよびＵＳＢケーブルなどの各種ケーブルと接続可能な端子など）、記録媒体挿入部などを備える構成としてもよい。さらに、電子書籍２７００は、電子辞書としての機能を持たせた構成とし

てもよい。
【０２４１】
また、電子書籍２７００は、無線で情報を送受信できる構成としてもよい。無線により、電子書籍サーバから、所望の書籍データなどを購入し、ダウンロードする構成とすることも可能である。
【０２４２】
（実施の形態９）
半導体装置は、さまざまな電子機器（遊技機も含む）に適用することができる。電子機器としては、例えば、テレビジョン装置（テレビ、またはテレビジョン受信機ともいう）、コンピュータ用などのモニタ、デジタルカメラ、デジタルビデオカメラ、デジタルフォトフレーム、携帯電話機（携帯電話、携帯電話装置ともいう）、携帯型ゲーム機、携帯情報端末、音響再生装置、パチンコ機などの大型ゲーム機などが挙げられる。
【０２４３】
図２５（Ａ）は、テレビジョン装置９６００の一例を示している。テレビジョン装置９６００は、筐体９６０１に表示部９６０３が組み込まれている。表示部９７０３により、映像を表示することが可能である。また、ここでは、スタンド９６０５により筐体９６０１を支持した構成を示している。
【０２４４】
テレビジョン装置９６００の操作は、筐体９６０１が備える操作スイッチや、別体のリモコン操作機９６１０により行うことができる。リモコン操作機９６１０が備える操作キー９６０９により、チャンネルや音量の操作を行うことができ、表示部９６０３に表示される映像を操作することができる。また、リモコン操作機９６１０に、当該リモコン操作機９６１０から出力する情報を表示する表示部９６０７を設ける構成としてもよい。
【０２４５】
なお、テレビジョン装置９６００は、受信機やモデムなどを備えた構成とする。受信機により一般のテレビ放送の受信を行うことができ、さらにモデムを介して優先または無線による通信ネットワークに接続することにより、一方向（送信者から受信者）または双方向（送信者と受信者間、あるいは受信者間同士など）の情報通信を行うことも可能である。
【０２４６】
図２５（Ｂ）は、デジタルフォトフレーム９７００の一例を示している。例えば、デジタルフォトフレーム９７００は、筐体９７０１に表示部９７０３が組み込まれている。表示部９７０３は、各種画像を表示することが可能であり、例えばデジタルカメラなどで撮影した画像データを表示させることで、通常の写真立てと同様に機能させることができる。
【０２４７】
なお、デジタルフォトフレーム９７００は、操作部、外部接続用端子（ＵＳＢ端子、ＵＳＢケーブルなどの各種ケーブルと接続可能な端子など）、記録媒体挿入部などを備える構成とする。これらの構成は、表示部と同一面に組み込まれていてもよいが、側面や裏面に備えるとデザイン性が向上するため好ましい。例えば、デジタルフォトフレームの記録媒体挿入部に、デジタルカメラで撮影した画像データを記憶したメモリを挿入して画像データを取り込み、取り込んだ画像データを表示部９７０３に表示させることができる。
【０２４８】
また、デジタルフォトフレーム９７００は、無線で情報を送受信出来る構成としてもよい。無線により、所望の画像データを取り込み、表示させる構成とすることもできる。
【０２４９】
図２６（Ａ）は携帯型遊技機であり、筐体９８８１と筐体９８９１の２つの筐体で構成されており、連結部９８９３により、開閉可能に連結されている。筐体９８８１には表示部９８８２が組み込まれ、筐体９８９１には表示部９８８３が組み込まれている。また、図２６（Ａ）に示す携帯型遊技機は、その他、スピーカ部９８８４、記録媒体挿入部９８８６、ＬＥＤランプ９８９０、入力手段（操作キー９８８５、接続端子９８８７、センサ９８８８（力、変位、位置、速度、加速度、角速度、回転数、距離、光、液、磁気、温度、

化学物質、音声、時間、硬度、電場、電流、電圧、電力、放射線、流量、湿度、傾度、振動、におい又は赤外線を測定する機能を含むもの）、マイクロフォン９８８９）等を備えている。もちろん、携帯型遊技機の構成は上述のものに限定されず、少なくとも実施の形態１または実施の形態２に示す薄膜トランジスタを有する半導体装置を備えた構成であればよく、その他付属設備が適宜設けられた構成とすることができる。図２６（Ａ）に示す携帯型遊技機は、記録媒体に記録されているプログラム又はデータを読み出して表示部に表示する機能や、他の携帯型遊技機と無線通信を行って情報を共有する機能を有する。なお、図２６（Ａ）に示す携帯型遊技機が有する機能はこれに限定されず、様々な機能を有することができる。

【０２５０】

図２６（Ｂ）は大型遊技機であるスロットマシン９９００の一例を示している。スロットマシン９９００は、筐体９９０１に表示部９９０３が組み込まれている。また、スロットマシン９９００は、その他、スタートレバーやストップスイッチなどの操作手段、コイン投入口、スピーカなどを備えている。もちろん、スロットマシン９９００の構成は上述のものに限定されず、少なくとも実施の形態１または実施の形態２に示す薄膜トランジスタを有する半導体装置を備えた構成であればよく、その他付属設備が適宜設けられた構成とすることができる。

【０２５１】

図２７は、携帯電話機１０００の一例を示している。携帯電話機１０００は、筐体１００１に組み込まれた表示部１００２の他、操作ボタン１００３、外部接続ポート１００４、スピーカ１００５、マイク１００６などを備えている。

【０２５２】

図２７に示す携帯電話機１０００は、表示部１００２を指などで触れることで、情報を入力ことができる。また、電話を掛ける、或いはメールを打つなどの操作は、表示部１００２を指などで触れることにより行うことができる。

【０２５３】

表示部１００２の画面は主として３つのモードがある。第１は、画像の表示を主とする表示モードであり、第２は、文字等の情報の入力を主とする入力モードである。第３は表示モードと入力モードの２つのモードが混合した表示＋入力モードである。

【０２５４】

例えば、電話を掛ける、或いはメールを作成する場合は、表示部１００２を文字の入力を主とする文字入力モードとし、画面に表示させた文字の入力操作を行えばよい。この場合、表示部１００２の画面のほとんどにキーボードまたは番号ボタンを表示させることが好ましい。

【０２５５】

また、携帯電話機１０００内部に、ジャイロ、加速度センサ等の傾きを検出するセンサを有する検出装置を設けることで、携帯電話機１０００の向き（縦か横か）を判断して、表示部１００２の画面表示を自動的に切り替えるようにすることができる。

【０２５６】

また、画面モードの切り替えは、表示部１００２を触れること、又は筐体１００１の操作ボタン１００３の操作により行われる。また、表示部１００２に表示される画像の種類によって切り替えるようにすることもできる。例えば、表示部に表示する画像信号が動画のデータであれば表示モード、テキストデータであれば入力モードに切り替える。

【０２５７】

また、入力モードにおいて、表示部１００２の光センサで検出される信号を検知し、表示部１００２のタッチ操作による入力が一定期間ない場合には、画面のモードを入力モードから表示モードに切り替えるように制御してもよい。

【０２５８】

表示部１００２は、イメージセンサとして機能させることもできる。例えば、表示部１００２に掌や指を触れることで、掌紋、指紋等を撮像することで、本人認証を行うことがで

きる。また、表示部に近赤外光を発光するバックライトまたは近赤外光を発光するセンシング用光源を用いれば、指静脈、掌静脈などを撮像することもできる。

【０２５９】

（実施の形態１０）

実施の形態１または実施の形態２においては、バッファ層を設ける例を示したが、本実施の形態ではバッファ層を設けない例を示す。また、２つのｎチャネル型の薄膜トランジスタを用いてインバータ回路を構成する例を以下に説明する。

【０２６０】

画素部を駆動するための駆動回路は、インバータ回路、容量、抵抗などを用いて構成する。２つのｎチャネル型ＴＦＴを組み合わせてインバータ回路を形成する場合、エンハンスメント型トランジスタとデプレッション型トランジスタとを組み合わせて形成する場合（以下、ＥＤＭＯＳ回路という）と、エンハンスメント型ＴＦＴ同士で形成する場合（以下、ＥＥＭＯＳ回路という）がある。なお、ｎチャネル型ＴＦＴのしきい値電圧が正の場合は、エンハンスメント型トランジスタと定義し、ｎチャネル型ＴＦＴのしきい値電圧が負の場合は、デプレッション型トランジスタと定義し、本明細書を通してこの定義に従うものとする。

【０２６１】

画素部と駆動回路は、同一基板上に形成し、画素部においては、マトリクス状に配置したエンハンスメント型トランジスタを用いて画素電極への電圧印加のオンオフを切り替える。この画素部に配置するエンハンスメント型トランジスタは、酸化物半導体を用いており、その電気特性は、ゲート電圧±２０Ｖにおいて、オンオフ比が１０９以上であるため、リーク電流が少なく、低消費電力駆動を実現することができる。

【０２６２】

駆動回路のインバータ回路の断面構造を図３２（Ａ）に示す。図３２（Ａ）において、基板１４００上に第１のゲート電極１４０１及び第２のゲート電極１４０２を設ける。第１のゲート電極１４０１及び第２のゲート電極１４０２の材料は、モリブデン、チタン、クロム、タンタル、タングステン、アルミニウム、銅、ネオジム、スカンジウム等の金属材料又はこれらを主成分とする合金材料を用いて、単層で又は積層して形成することができる。

【０２６３】

例えば、第１のゲート電極１４０１及び第２のゲート電極１４０２の２層の積層構造としては、アルミニウム層上にモリブデン層が積層された二層の積層構造、または銅層上にモリブデン層を積層した二層構造、または銅層上に窒化チタン層若しくは窒化タンタルを積層した二層構造、窒化チタン層とモリブデン層とを積層した二層構造とすることが好ましい。２層の積層構造としては、タングステン層または窒化タングステンと、アルミニウムとシリコンの合金またはアルミニウムとチタンの合金と、窒化チタンまたはチタン層とを積層した積層とすることが好ましい。

【０２６４】

また、第１のゲート電極１４０１及び第２のゲート電極１４０２を覆うゲート絶縁層１４０３上には、第１配線１４０９、第２配線１４１０、及び第３配線１４１１を設け、第２の配線１４１０は、ゲート絶縁層１４０３に形成されたコンタクトホール１４０４を介して第２のゲート電極１４０２と直接接続する。

【０２６５】

また、第１のゲート電極１４０１と重なる位置に第１配線１４０９及び第２配線１４１０上に接する第１の酸化物半導体層１４０５と、第２のゲート電極１４０２と重なる位置に第２配線１４１０及び第３配線１４１１上に接する第２の酸化物半導体層１４０７とを設ける。

【０２６６】

第１の薄膜トランジスタ１４３０は、第１のゲート電極１４０１と、ゲート絶縁層１４０３を介して第１のゲート電極１４０１と重なる第１の酸化物半導体層１４０５とを有し、

第１配線１４０９は、接地電位の電源線（接地電源線）である。この接地電位の電源線は、負の電圧ＶＤＬが印加される電源線（負電源線）としてもよい。

【０２６７】

また、第２の薄膜トランジスタ１４３１は、第２のゲート電極１４０２と、ゲート絶縁層１４０３を介して第２のゲート電極１４０２と重なる第２の酸化物半導体層１４０７とを有し、第３配線１４１１は、正の電圧ＶＤＤが印加される電源線（正電源線）である。

【０２６８】

第１の酸化物半導体層１４０５を挟んで対向する第１配線１４０９の側面と第２配線１４１０の側面とをテーパ形状とすることで、酸化物半導体層におけるソース電極層の側面及びドレイン電極層の側面と重なる領域は、電界集中緩和領域として機能させる。

【０２６９】

また、第２の酸化物半導体層１４０７を挟んで対向する第２配線１４１０の側面と第３配線１４１１の側面とをテーパ形状とすることで、酸化物半導体層におけるソース電極層の側面及びドレイン電極層の側面と重なる領域は、電界集中緩和領域として機能させる。

【０２７０】

図３２（Ａ）に示すように、第１の酸化物半導体層１４０５と第２の酸化物半導体層１４０７の両方に電気的に接続する第２の配線１４１０は、ゲート絶縁層１４０３に形成されたコンタクトホール１４０４を介して第２の薄膜トランジスタ１４３１の第２のゲート電極１４０２と直接接続する。第２の配線１４１０と第２のゲート電極１４０２とを直接接続させることにより、良好なコンタクトを得ることができ、接触抵抗を低減することができる。第２のゲート電極１４０２と第２配線１４１０を他の導電膜、例えば透明導電膜を介して接続する場合に比べて、コンタクトホールの数の低減、コンタクトホールの数の低減による占有面積の縮小を図ることができる。

【０２７１】

また、駆動回路のインバータ回路の上面図を図３２（Ｃ）に示す。図３２（Ｃ）において、鎖線Ｚ１－Ｚ２で切断した断面が図３２（Ａ）に相当する。

【０２７２】

また、ＥＤＭＯＳ回路の等価回路を図３２（Ｂ）に示す。図３２（Ａ）及び図３２（Ｃ）示す回路接続は、図３２（Ｂ）に相当し、第１の薄膜トランジスタ１４３０をエンハンスメント型のｎチャネル型トランジスタとし、第２の薄膜トランジスタ１４３１をデプレッション型のｎチャネル型トランジスタとする例である。

【０２７３】

また、本実施の形態ではＥＤＭＯＳ回路の例を示したが、どちらもエンハンスメント型のｎチャネル型トランジスタとするＥＥＭＯＳ回路を用いて駆動回路を構成してもよい。

【０２７４】

また、本実施の形態においては、バッファ層を設けない例を示したが、特に限定されず、実施の形態１と同様に、第１配線１４０９の上面、第２配線１４１０上面、及び第３配線１４１１上面にバッファ層を設けてもよい。

【０２７５】

また、本実施の形態は、実施の形態１乃至９のいずれか一と組み合わせることができる。

【０２７６】

以上の構成でなる実施の形態について、以下に示す実施例でもってさらに詳細な説明を行うこととする。

【実施例１】

【０２７７】

本実施例では、酸化物半導体層を用いて作製された薄膜トランジスタの特性に関して示す。

【０２７８】

以下に、本実施例で用いたトランジスタの作製方法について説明する。

【０２７９】

まず、基板上に第１の導電膜を形成した後、当該第１の導電膜をフォトリソグラフィ法を用いてパターニングすることによりゲート電極５０２を形成した。続いて、当該ゲート電極５０２上にゲート絶縁層５０３を形成した。続いて、ゲート絶縁層５０３上に第２の導電膜とバッファ層を形成した。なお、基板を大気に曝すことなく連続して第２の導電膜とバッファ層を形成した。続いて、当該第２の導電膜及びバッファ層をフォトリソグラフィ法を用いてパターニングすることにより、一部がゲート電極と重なるソース電極層５０６ａ及びドレイン電極層５０６ｂを形成した。続いて、ゲート絶縁層、ソース電極層及びドレイン電極層上に酸化物半導体層を形成した後、当該酸化物半導体層をフォトリソグラフィ法を用いてパターニングすることにより、チャネル形成領域として機能する島状の酸化物半導体層５１０を形成した。続いて、窒素雰囲気下で３５０℃、１時間の熱処理を行った。

【０２８０】

基板として、旭ガラス社製のガラス基板（商品名ＡＮ１００）を用いた。

【０２８１】

ゲート電極５０２となる第１の導電膜として、スパッタ法を用いて膜厚１００ｎｍのタングステン膜を形成した。

【０２８２】

ゲート絶縁層５０３として、プラズマＣＶＤ法を用いて膜厚１００ｎｍの酸化窒化シリコン膜を形成した。

【０２８３】

ソース電極層５０６ａ及びドレイン電極層５０６ｂとなる第２の導電膜として、スパッタ法を用いて膜厚１００ｎｍのタングステン膜を形成した。

【０２８４】

バッファ層は、スパッタ法によって５～１０ｎｍのＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を形成した。成膜条件は、アルゴンガスのみを用い、ターゲットは、In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１としたターゲットを用いた。

【０２８５】

酸化物半導体層は、スパッタ法によって１５０ｎｍのＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を成膜した。成膜条件は、圧力を０．４Ｐａとし、電力を５００Ｗとし、成膜温度を２５℃とし、アルゴンガス流量を１０ｓｃｃｍとし、酸素流量を５ｓｃｃｍとし、ガラス基板とターゲット間の距離を１７０ｍｍとし、直流（ＤＣ（Ｄｉｒｅｃｔ　Ｃｕｒｒｅｎｔ））で行った。ターゲットは、In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１としたターゲット（Ｉｎ：Ｇａ：Ｚｎ＝１：１：０．５）を用いた。また、プラズマ処理を行った後、基板５００を大気に曝すことなく連続して酸化物半導体層を形成した。なお、この成膜条件で得られた酸化物半導体層の組成を誘導結合プラズマ質量分析法（Ｉｎｄｕｃｔｉｖｅｌｙ　Ｃｏｕｐｌｅｄ　Ｐｌａｓｍａ　Ｍａｓｓ　Ｓｐｅｃｔｒｏｍｅｔｒｙ：ＩＣＰ－ＭＳ分析法）により測定した結果は、$InGa_{0.94}Zn_{0.40}O_{3.31}$であった。

【０２８６】

図２８に薄膜トランジスタのＶｇ－Ｉｇ曲線を示す。なお、本実施例では、トランジスタの測定は、ドレイン電圧（ソースの電圧に対するドレインの電圧）を１Ｖに設定して行った。

【０２８７】

また、本実施例では、トランジスタの構造を図２９に示すように形成した。具体的には、トランジスタのチャネル長Ｗを１００μｍ、チャネル幅Ｗを１００μｍ、ソース電極層５０６ａとゲート電極５０２が重なる長さＬｓを５μｍ、ドレイン電極層５０６ｂとゲート電極５０２が重なる長さＬｄを５μｍ、チャネル幅方向と平行な方向において酸化物半導体層５１０がソース電極層５０６ａ及びドレイン電極層５０６ｂと重ならない領域の長さＡを５μｍとした。

【０２８８】

以上により、基板を大気に曝すことなく連続して第２の導電膜とバッファ層を形成したことによって、トランジスタのオン・オフ比を高くし、電界効果移動度を高くすることができることがわかった。

【実施例２】

【０２８９】

また、本実施例では、エッチング後の電極形状の一例を示す。まず、サンプルを作製するプロセスについて図３０を用いて説明する。なお、実施例１とは、ソース電極層及びドレイン電極層の断面形状が異なっている点とバッファ層を形成しない点で異なっているだけであるため、同一の箇所には同一の符号を用いて説明する。

【０２９０】

まず、基板上に第１の導電膜を形成した後、当該第１の導電膜をフォトリソグラフィ法を用いてパターニングすることによりゲート電極５０２を形成した。続いて、当該ゲート電極５０２上にゲート絶縁層５０３を形成した（図３０（Ａ）参照）。続いて、ゲート絶縁層５０３上に第２の導電膜を形成した。続いて、当該第２の導電膜をフォトリソグラフィ法を用いてパターニングすることにより、一部がゲート電極と重なるソース電極層５０６ａ及びドレイン電極層５０６ｂを形成した（図３０（Ｂ）参照）。続いて、ゲート絶縁層、ソース電極層及びドレイン電極層上に酸化物半導体層を形成した後、当該酸化物半導体層をフォトリソグラフィ法を用いてパターニングすることにより、チャネル形成領域として機能する島状の酸化物半導体層５１０を形成した（図３０（Ｃ）参照）。

【０２９１】

基板として、旭ガラス社製のガラス基板（商品名ＡＮ１００）を用いた。

【０２９２】

ゲート電極５０２となる第１の導電膜として、スパッタ法を用いて膜厚１００ｎｍのタングステン膜を形成した。

【０２９３】

ゲート絶縁層５０３として、プラズマＣＶＤ法を用いて膜厚１００ｎｍの酸化窒化シリコン膜を形成した。

【０２９４】

ソース電極層６０６ａ及びドレイン電極層６０６ｂとなる第２の導電膜として、スパッタ法を用いて膜厚１００ｎｍのタングステン膜を形成した。

【０２９５】

酸化物半導体層は、スパッタ法によって１５０ｎｍのＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を成膜した。成膜条件は、実施例１と同じである。

【０２９６】

ソース電極層６０６ａ及びドレイン電極層６０６ｂのエッチングは、コイル状アンテナを用いるＩＣＰエッチング装置を用いて行った。CF_4のガス流量を２５（ｓｃｃｍ）、Cl_3のガス流量を２５（ｓｃｃｍ）、O_2のガス流量を１０（ｓｃｃｍ）とし、１．５Ｐａの圧力でコイル型の電極に５００ＷのＲＦ（１３．５６ＭＨｚ）電力を投入してプラズマを生成してエッチングを行う。基板側（試料ステージ）にも１０ＷのＲＦ（１３．５６ＭＨｚ）電力を投入し、実質的に負の自己バイアス電圧を印加する。少なくともゲート絶縁膜５０３がある程度露呈した段階で、このエッチングを途中で停止することにより、段差を有する電極側面が形成される。

【０２９７】

上記エッチング条件により、ソース電極層６０６ａの断面形状は、基板の基板面とソース電極層６０６ａの下端部側面とがなす角度θ１が２０°以上９０°未満とすることができる。図３０（Ｃ）中に示す点線で囲まれた部分の断面写真を図３１（Ａ）に示す。なお、図３１（Ｂ）は図３１（Ａ）の模式図である。図３１（Ａ）に示すように、θ１は約４０°である。また、図３１（Ａ）に示すように、基板の基板面とソース電極層６０６ａの上端部側面とがなす角度は約９０°である。なお、酸化物半導体層６１０を挟んで対向するソース電極層６０６ａ側面とドレイン電極層６０６ｂ側面の断面形状は同じエッチング工

程を経るため、ほぼ同一である。

【０２９８】

本実施例により、実施の形態２に示すソース電極層及びドレイン電極層の断面形状を作製することを示唆することができたと言える。

【図面の簡単な説明】

【０２９９】

【図１】半導体装置の一例を説明する断面図である。

【図２】半導体装置の一例を説明する断面図である。

【図３】半導体装置の作製方法の一例を説明する断面図である。

【図４】半導体装置の作製方法の一例を説明する断面図である。

【図５】半導体装置の作製方法の一例を説明する上面図である。

【図６】半導体装置の作製方法の一例を説明する上面図である。

【図７】半導体装置の作製方法の一例を説明する上面図である。

【図８】半導体装置の作製方法の一例を説明する上面図である。

【図９】端子部の断面図の一例及び上面図の一例を示す図である。

【図１０】半導体装置の作製方法の一例を説明する上面図である。

【図１１】半導体装置の一例を説明する断面図である。

【図１２】半導体装置のブロック図の一例を説明する図である。

【図１３】信号線駆動回路の構成の一例を説明する図である。

【図１４】信号線駆動回路の動作の一例を説明するタイミングチャートである。

【図１５】信号線駆動回路の動作の一例を説明するタイミングチャートである。

【図１６】シフトレジスタの構成の一例を説明する図である。

【図１７】図１６に示すフリップフロップの接続構成を説明する図である。

【図１８】半導体装置の画素等価回路の一例を説明する図である。

【図１９】半導体装置の一例を説明する断面図である。

【図２０】半導体装置の一例を説明する断面図及び上面図である。

【図２１】半導体装置の一例を説明する断面図である。

【図２２】半導体装置の一例を説明する断面図及び上面図である。

【図２３】電子ペーパーの使用形態の例を説明する図である。

【図２４】電子書籍の一例を示す外観図である。

【図２５】テレビジョン装置およびデジタルフォトフレームの例を示す外観図である。

【図２６】遊技機の例を示す外観図である。

【図２７】携帯電話機の一例を示す外観図である。

【図２８】薄膜トランジスタの電気特性の一例を示す図である。

【図２９】電気特性を得るために作製した薄膜トランジスタの上面図である。

【図３０】サンプルを作製する工程を示す断面図である。

【図３１】サンプルの断面一部を示す写真である。

【図３２】（Ａ）半導体装置の断面構造の一例を示す図、（Ｂ）等価回路図、（Ｃ）上面図。

【符号の説明】

【０３００】

１００：基板

１０１：ゲート電極

１０２：ゲート絶縁層

１０３：酸化物半導体層

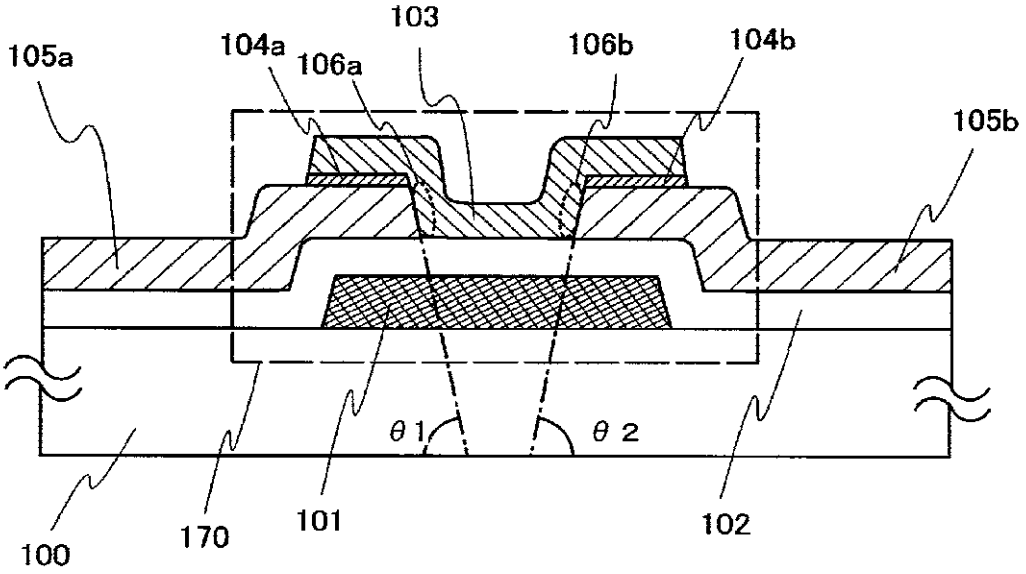
１０４ａ：第１のバッファ層

１０４ｂ：第２のバッファ層

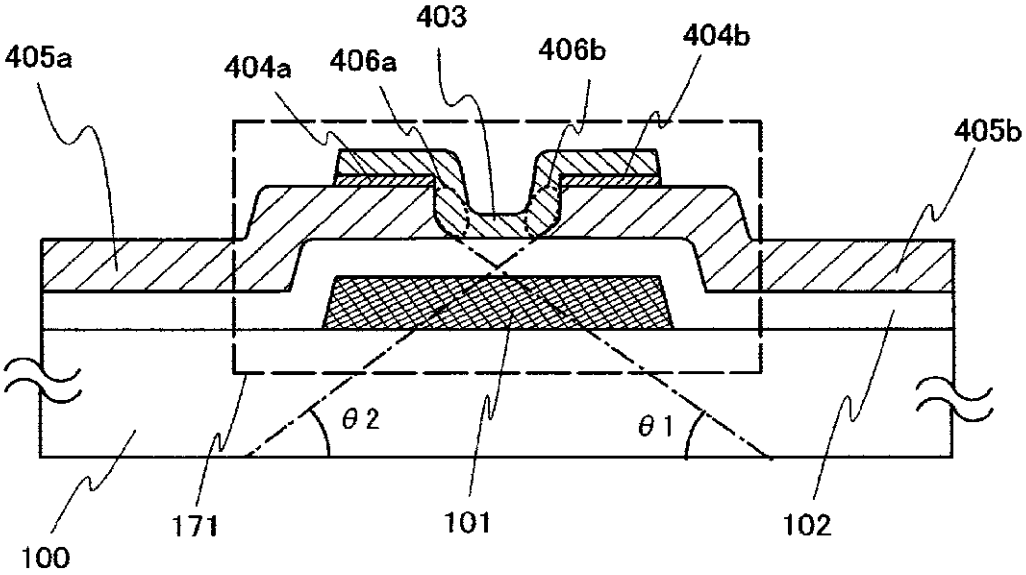
１０５ａ：ソース電極層

１０５ｂ：ドレイン電極層

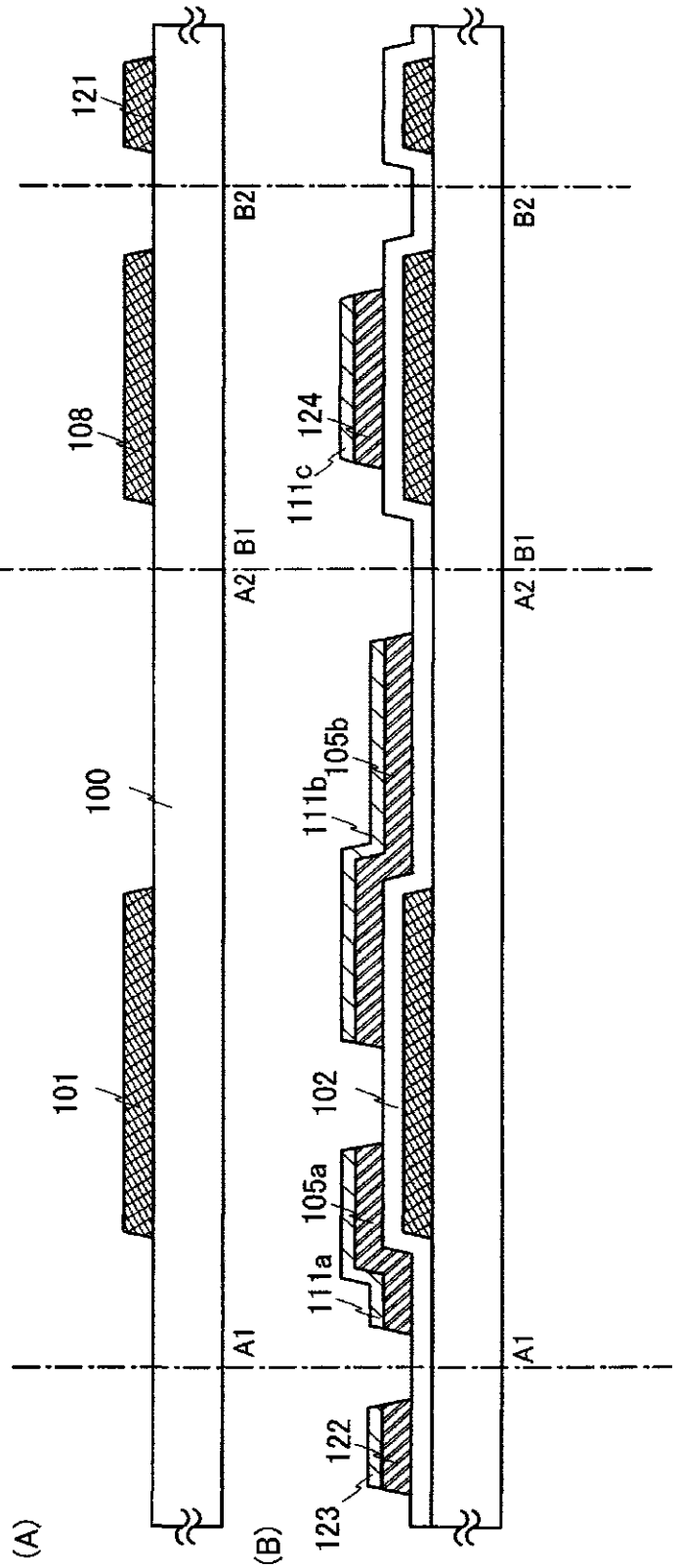
【書類名】図面
【図１】


105a
104a
106a
103
106b
104b
105b
θ1
θ2
100
170
101
102

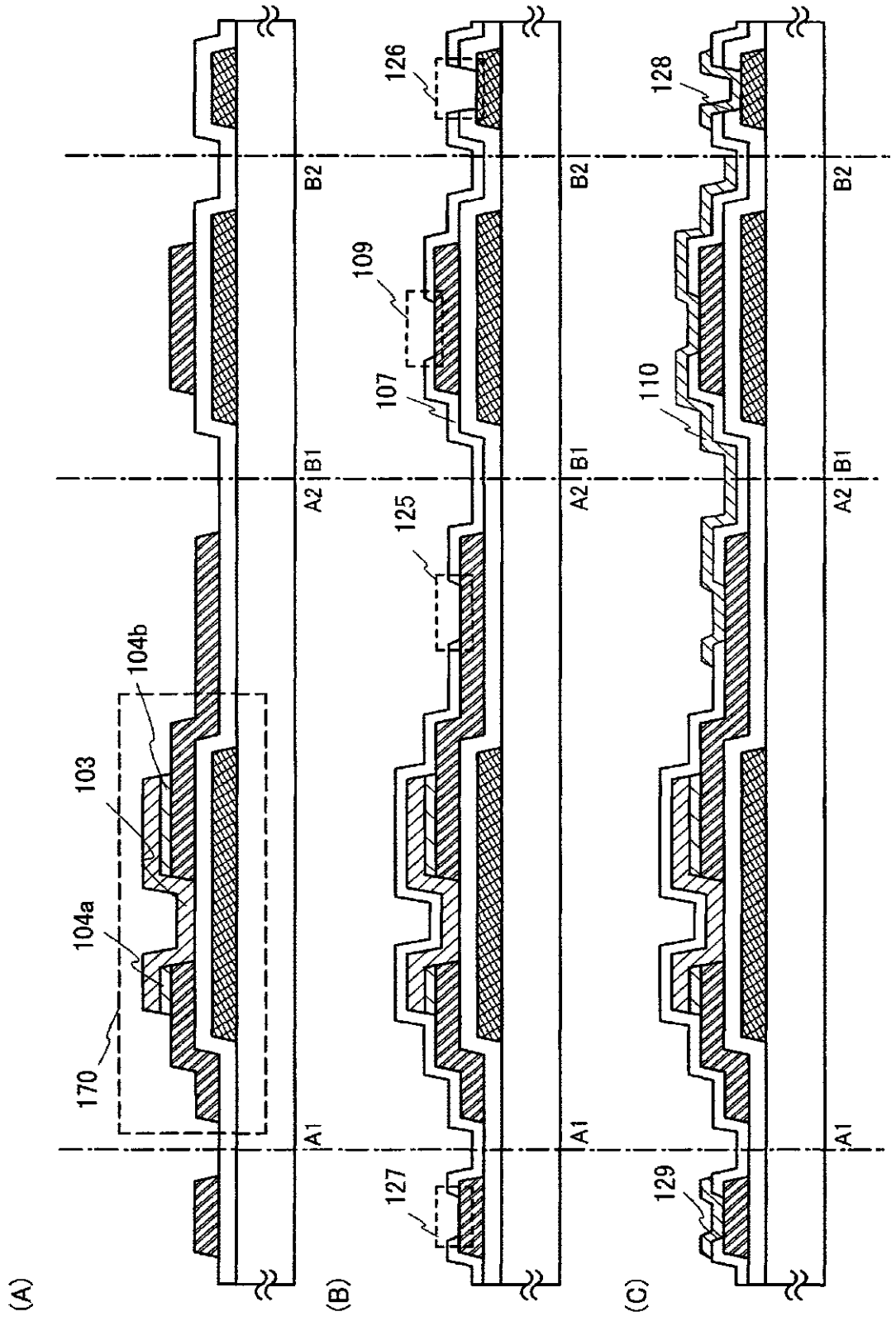
【図２】


405a
404a
406a
403
406b
404b
405b
θ2
θ1
100
171
101
102

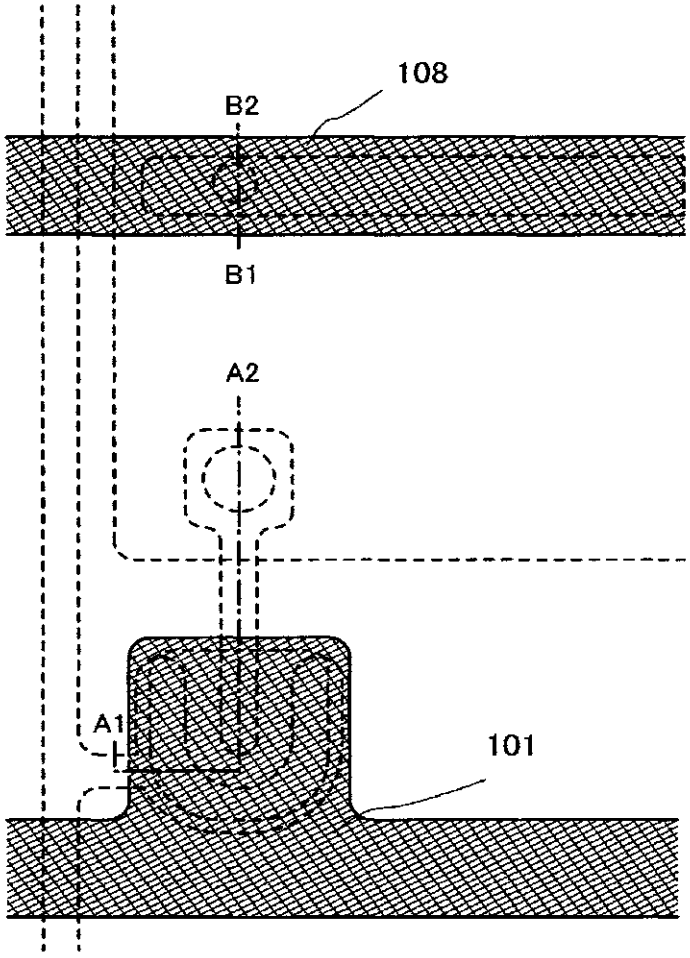
【図３】


121
B2
108
124
111c
B1
A2
100
105b
111b
101
102
105a
111a
A1
122
123
(A)
(B)

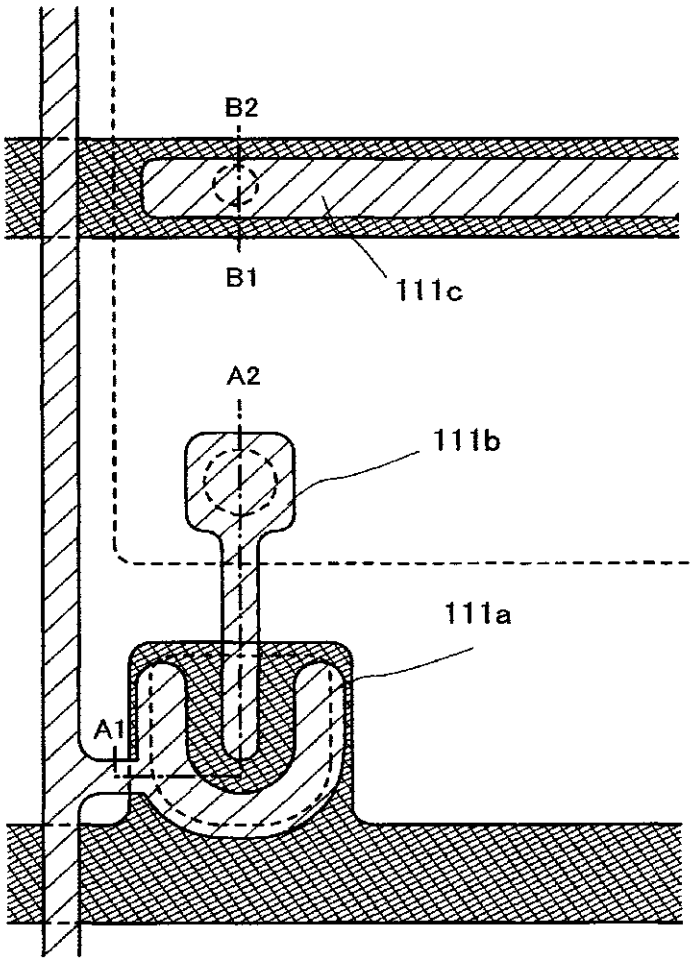
【図４】



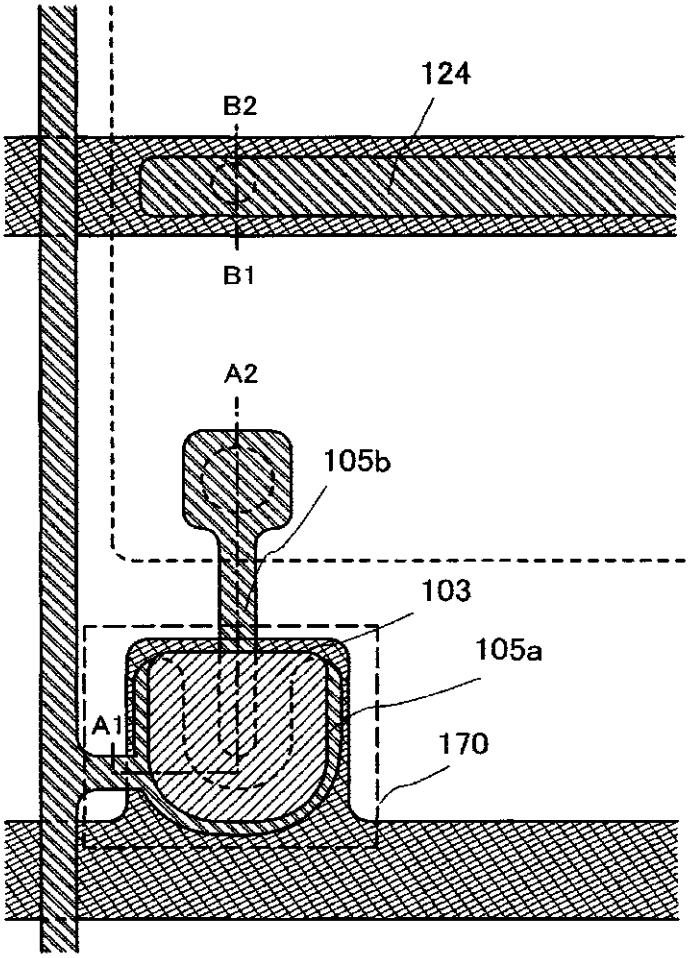
【図５】



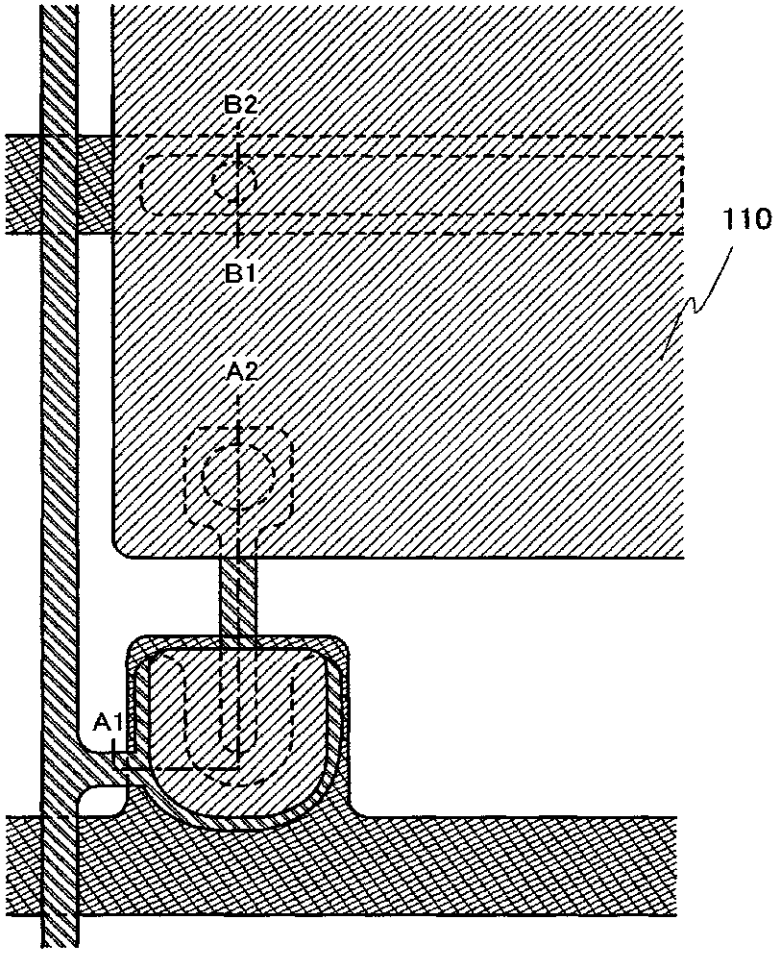
【図６】



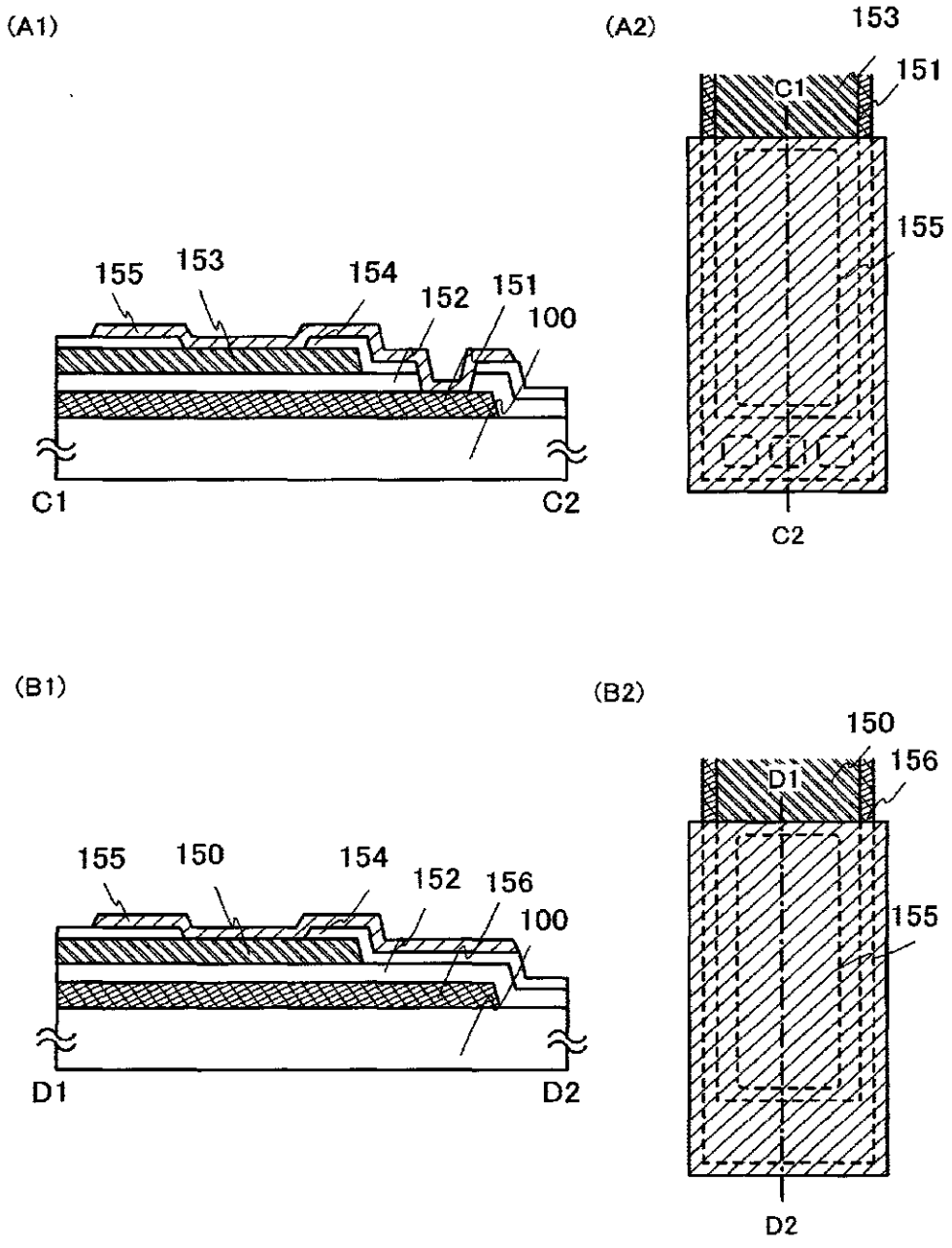
【図７】



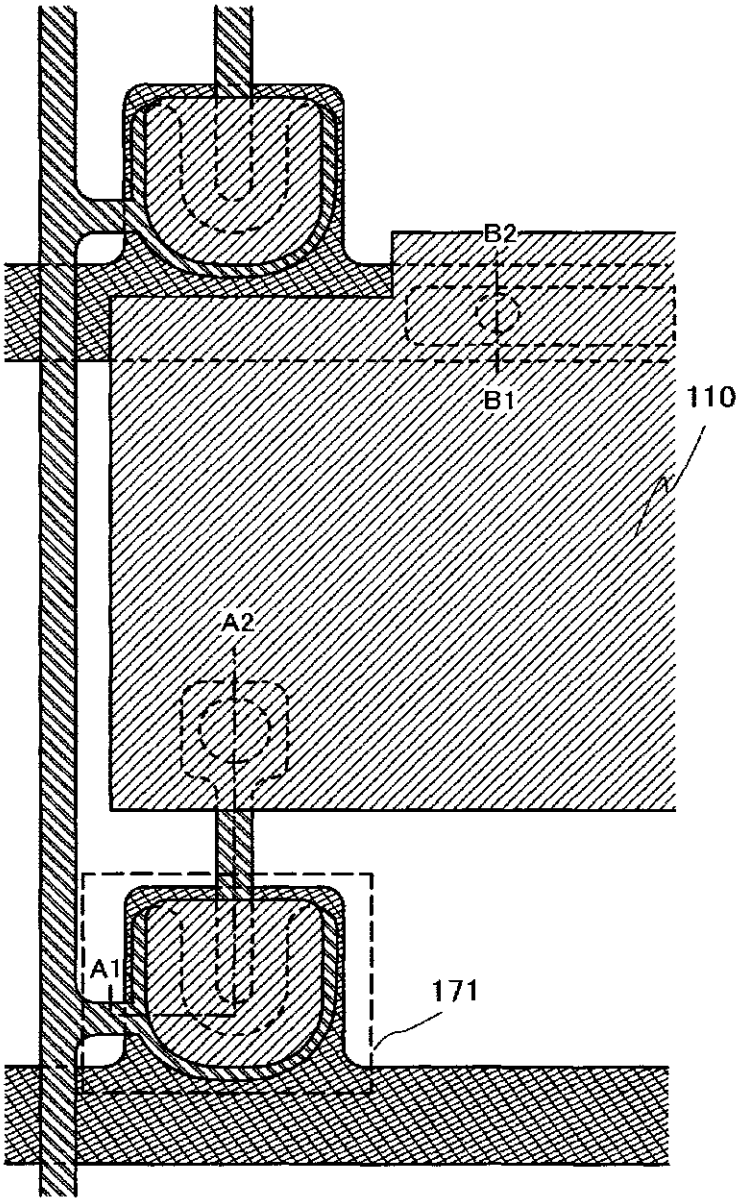
【図８】



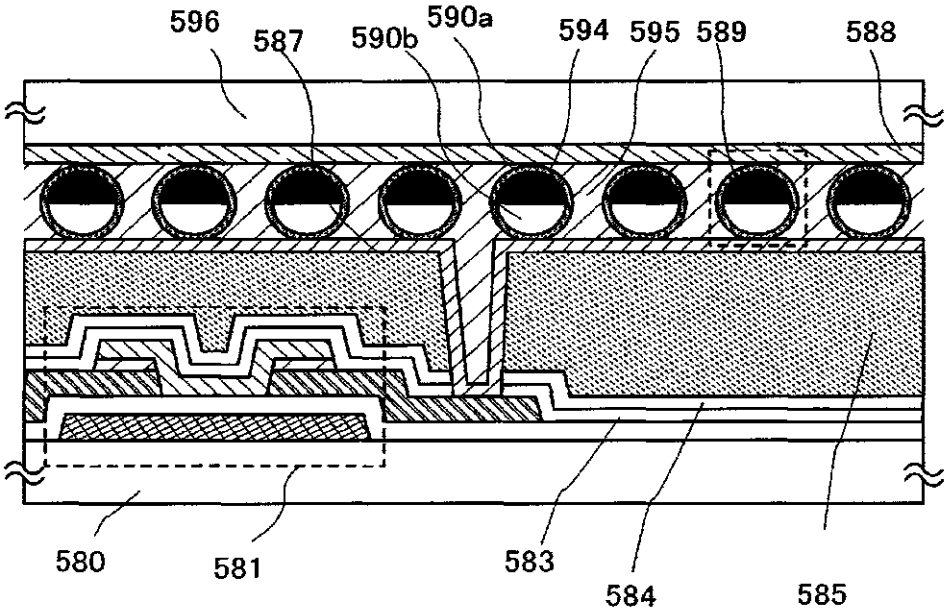
【図９】


(A1)
155
153
154
152
151
100
C1
C2
(A2)
153
151
C1
155
C2
(B1)
155
150
154
152
156
100
D1
D2
(B2)
150
156
D1
155
D2

【図１０】

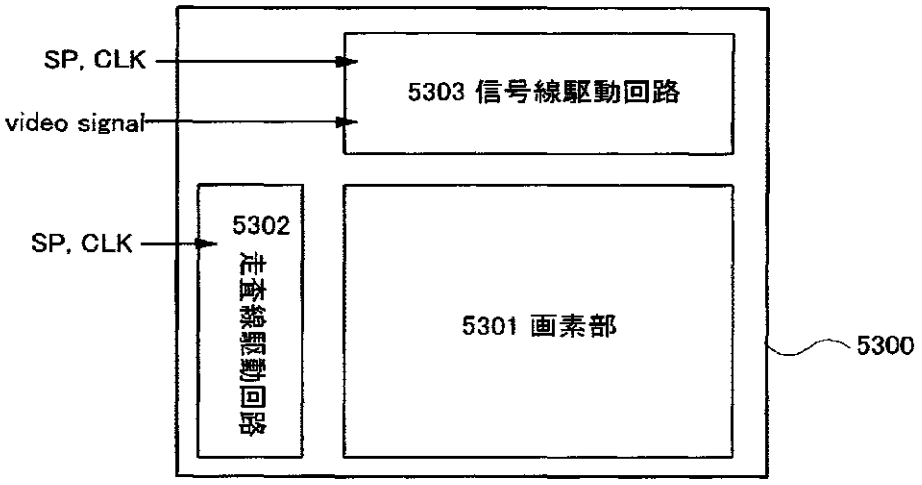


【図１１】

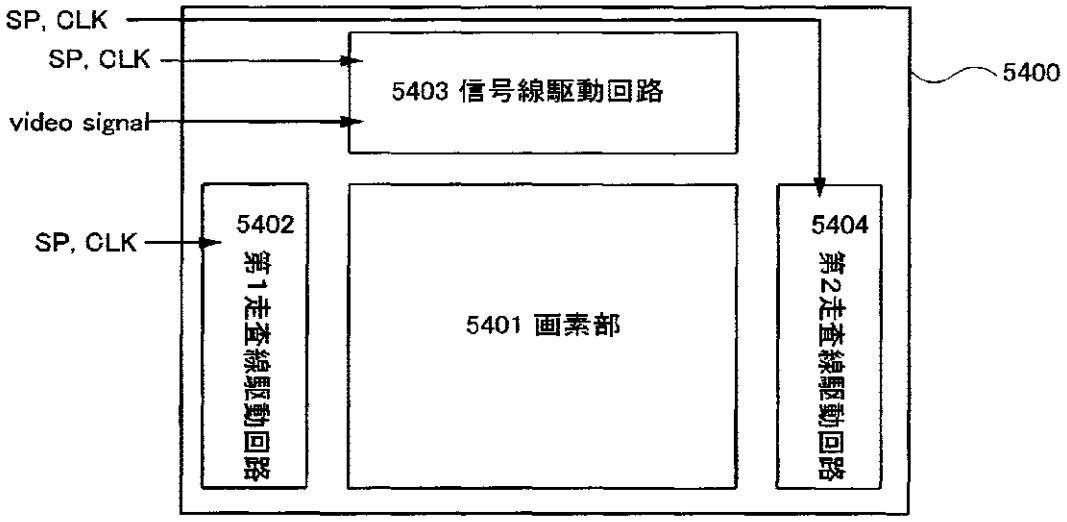


【図１２】

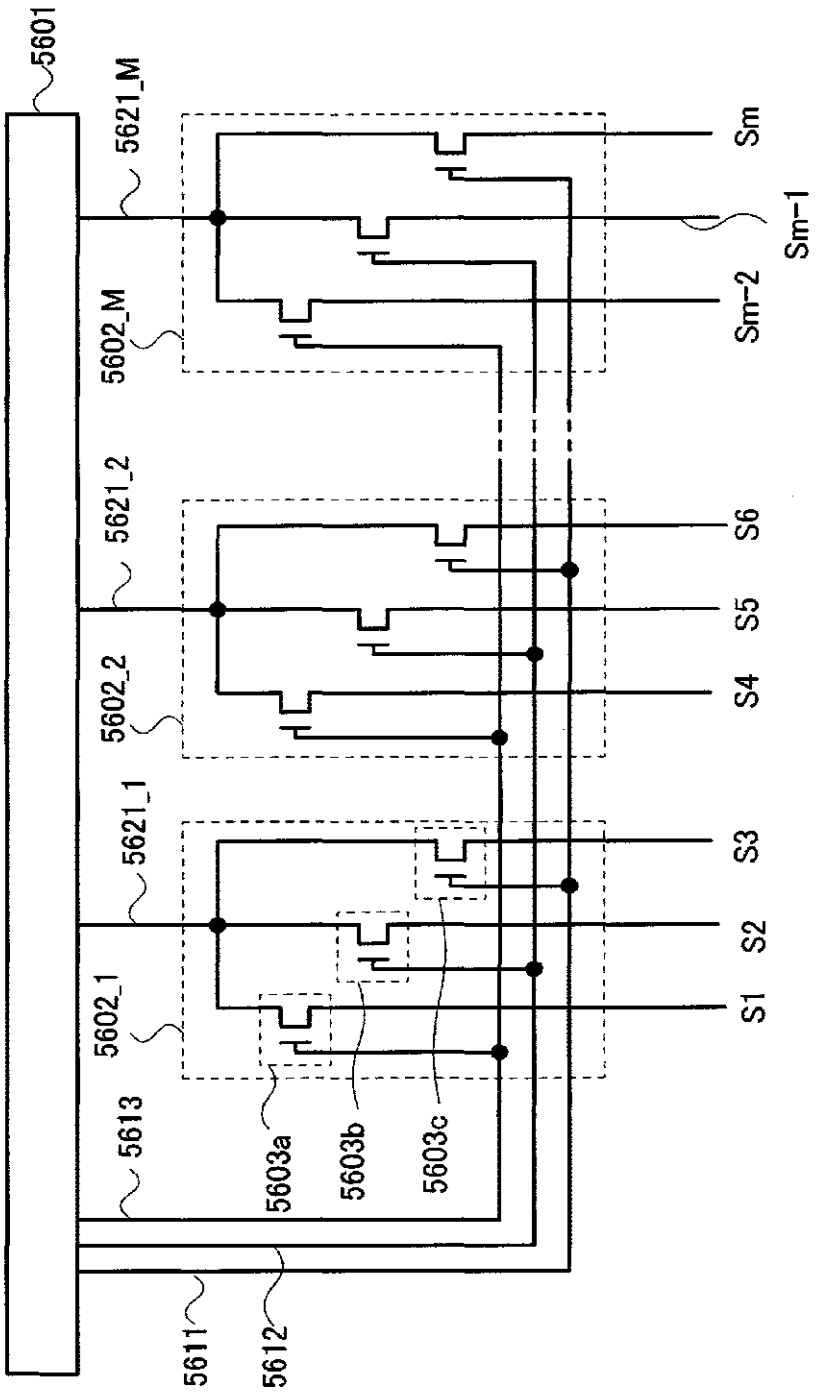
(A)


SP, CLK
video signal
SP, CLK
5303 信号線駆動回路
5302
走査線駆動回路
5301 画素部
5300

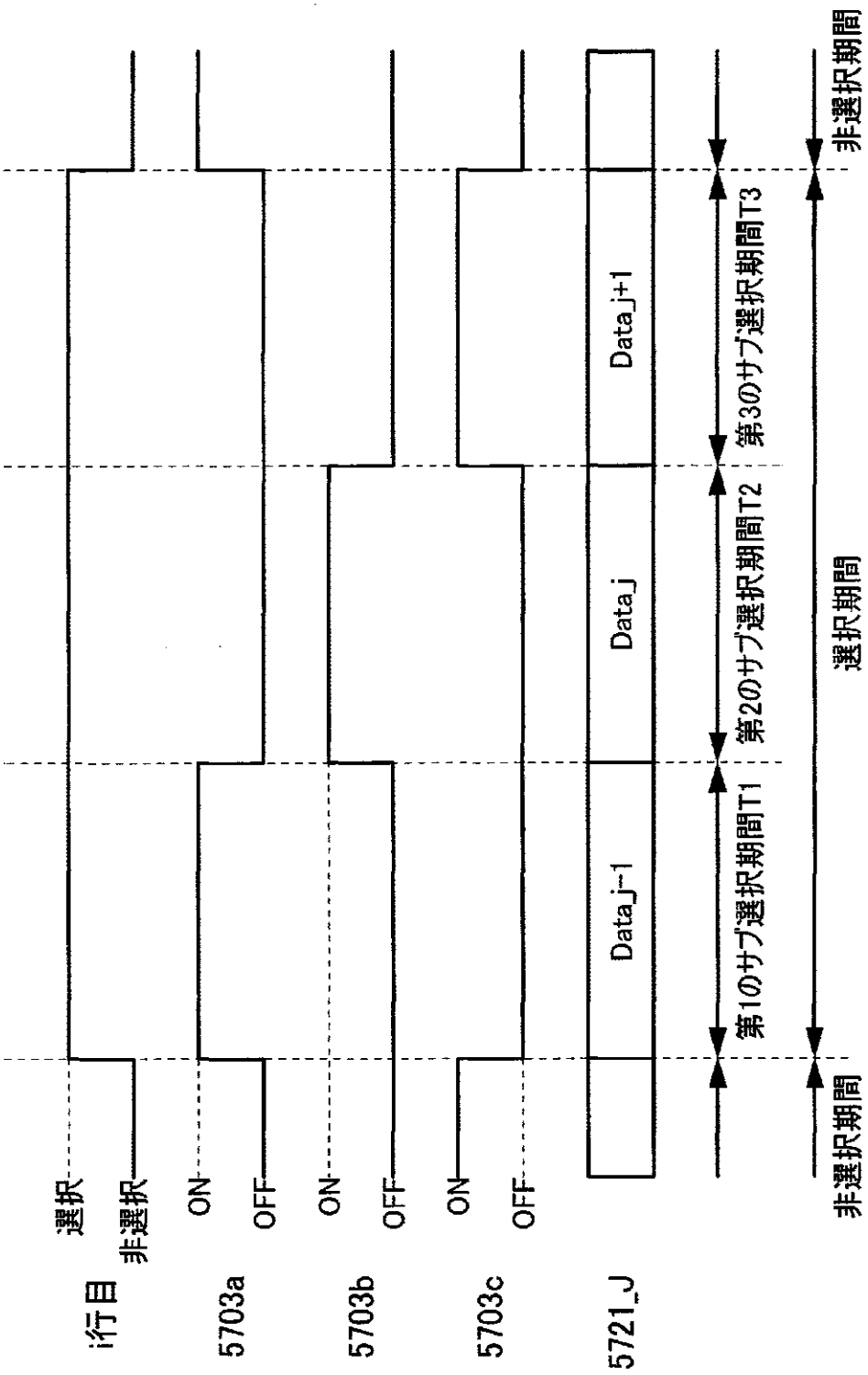
(B)


SP, CLK
SP, CLK
video signal
SP, CLK
5403 信号線駆動回路
5402
第1走査線駆動回路
5401 画素部
5404
第2走査線駆動回路
5400

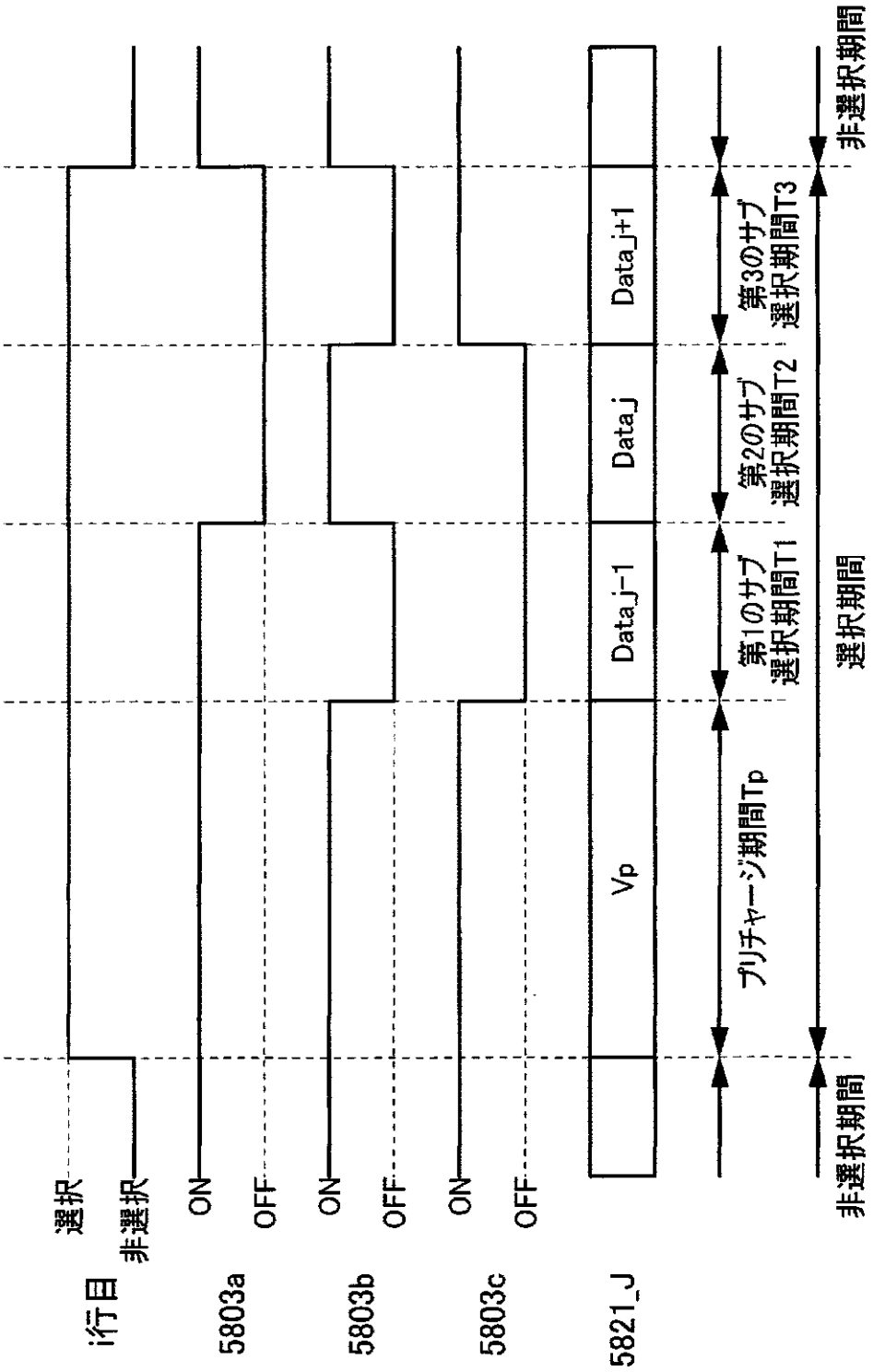
【図１３】


5601
5621_M
5602_M
5621_2
5602_2
5621_1
5602_1
5613
5611
5612
5603a
5603b
5603c
Sm
Sm-1
Sm-2
S6
S5
S4
S3
S2
S1

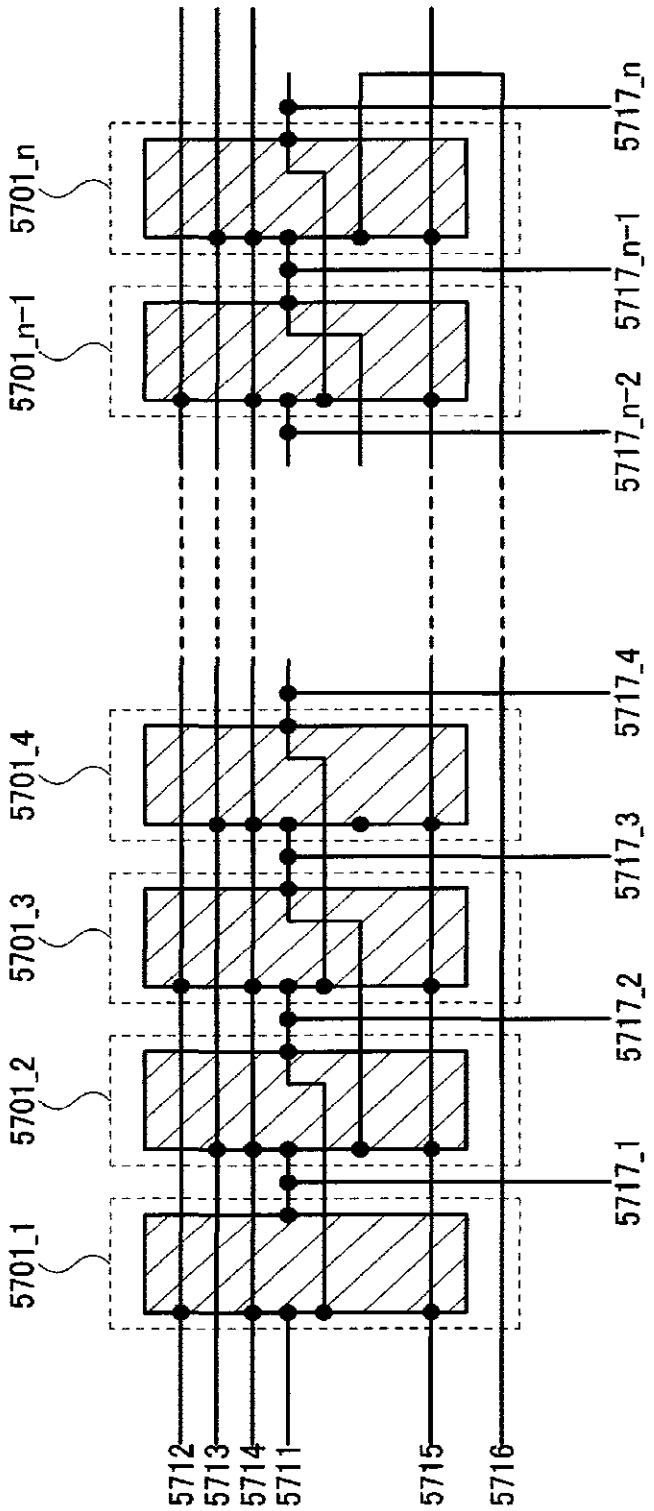
【図１４】


i行目
選択
非選択
5703a
ON
OFF
5703b
ON
OFF
5703c
ON
OFF
5721_J
Data_j-1
Data_j
Data_j+1
第1のサブ選択期間T1
第2のサブ選択期間T2
第3のサブ選択期間T3
非選択期間
選択期間
非選択期間

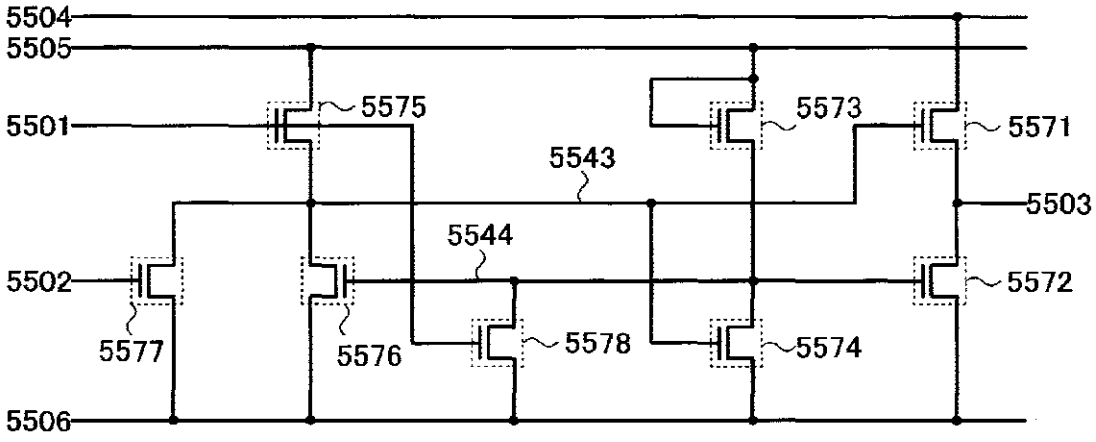
【図１５】


i行目
選択
非選択
5803a
ON
OFF
5803b
ON
OFF
5803c
ON
OFF
5821_J
Vp
Data_j-1
Data_j
Data_j+1
プリチャージ期間Tp
第1のサブ選択期間T1
第2のサブ選択期間T2
第3のサブ選択期間T3
選択期間
非選択期間
非選択期間

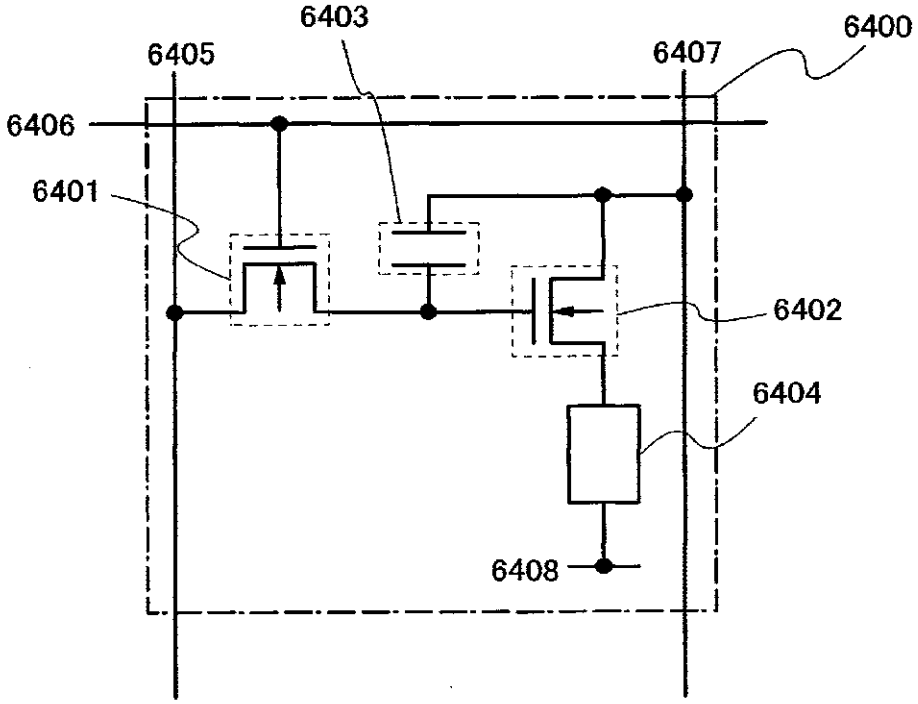
【図１６】


5701_n
5701_n-1
5701_4
5701_3
5701_2
5701_1
5717_n
5717_n-1
5717_n-2
5717_4
5717_3
5717_2
5717_1
5712
5713
5714
5711
5715
5716

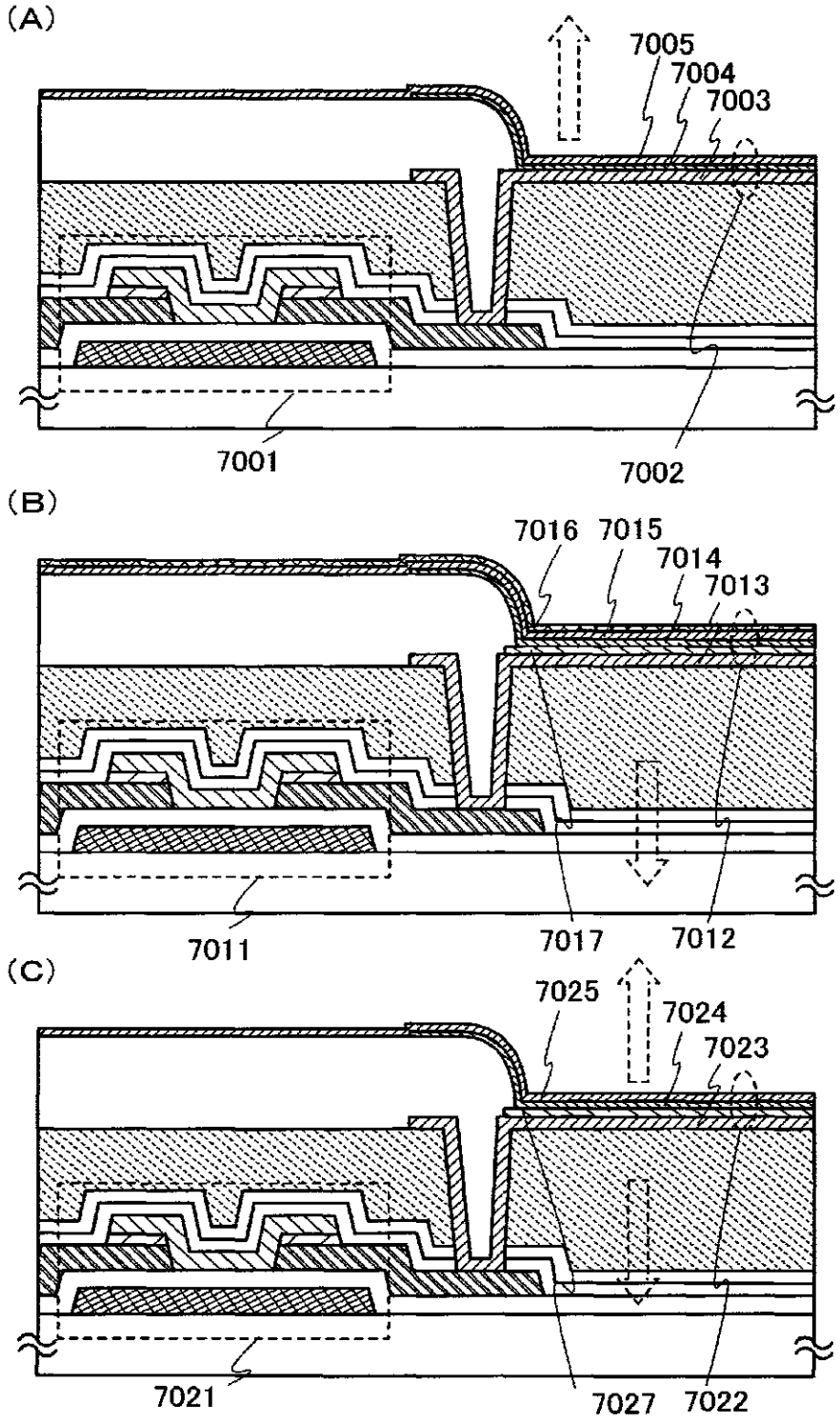
【図１７】


5504
5505
5501
5575
5573
5571
5543
5503
5544
5502
5572
5577
5576
5578
5574
5506

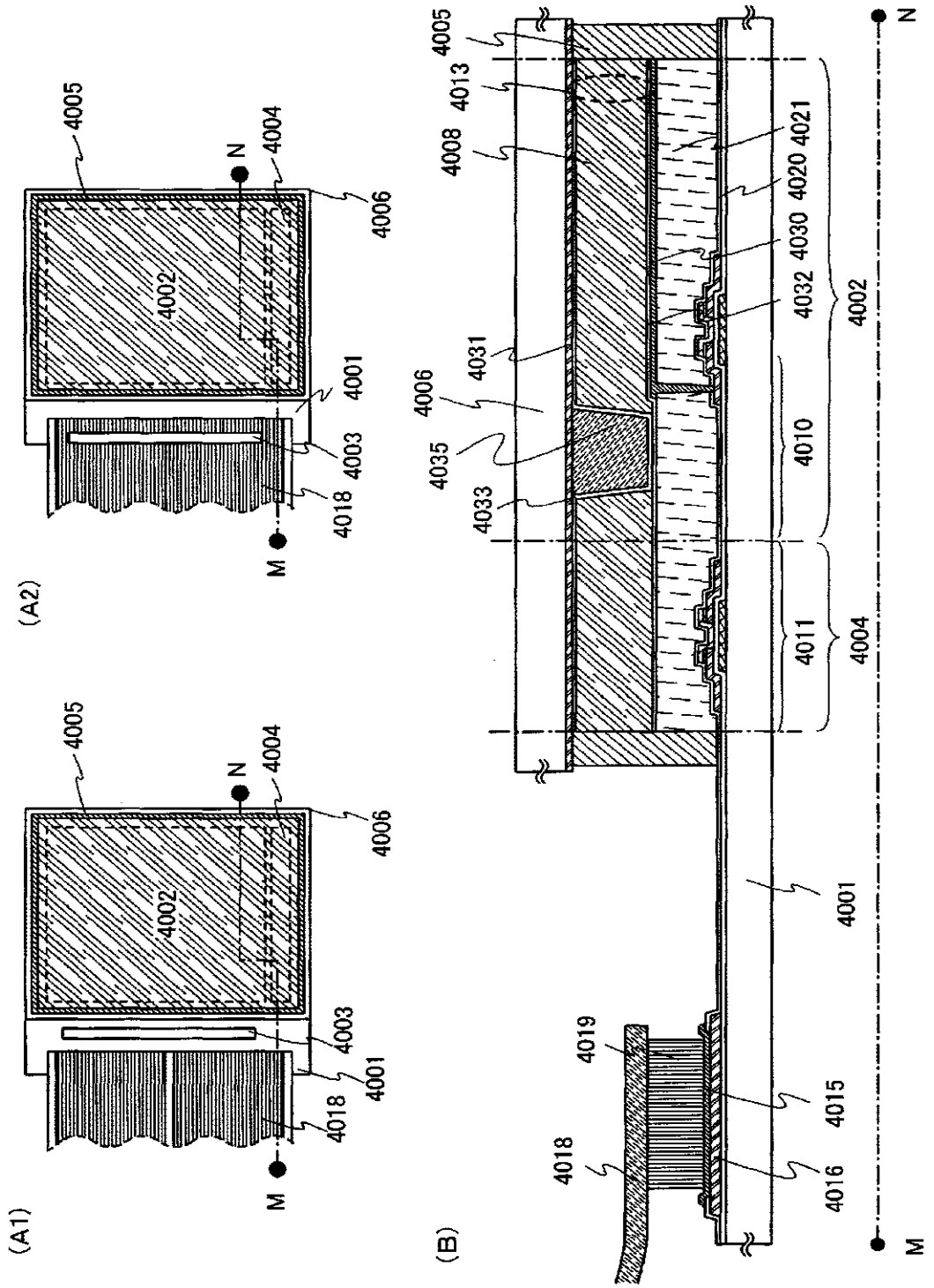
【図１８】


6403
6405
6407
6400
6406
6401
6402
6404
6408

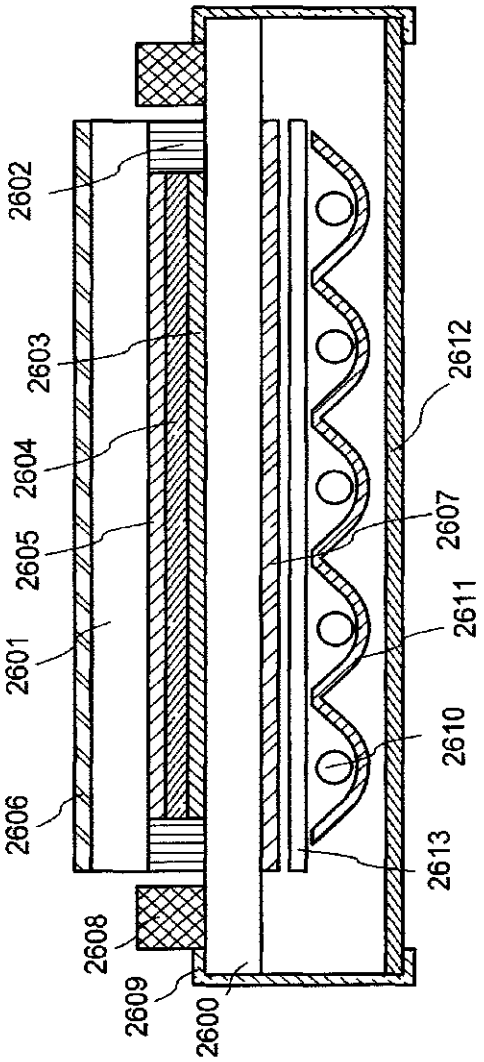
【図１９】


(A)
7005
7004
7003
7001
7002
(B)
7016
7015
7014
7013
7011
7017
7012
(C)
7025
7024
7023
7021
7027
7022

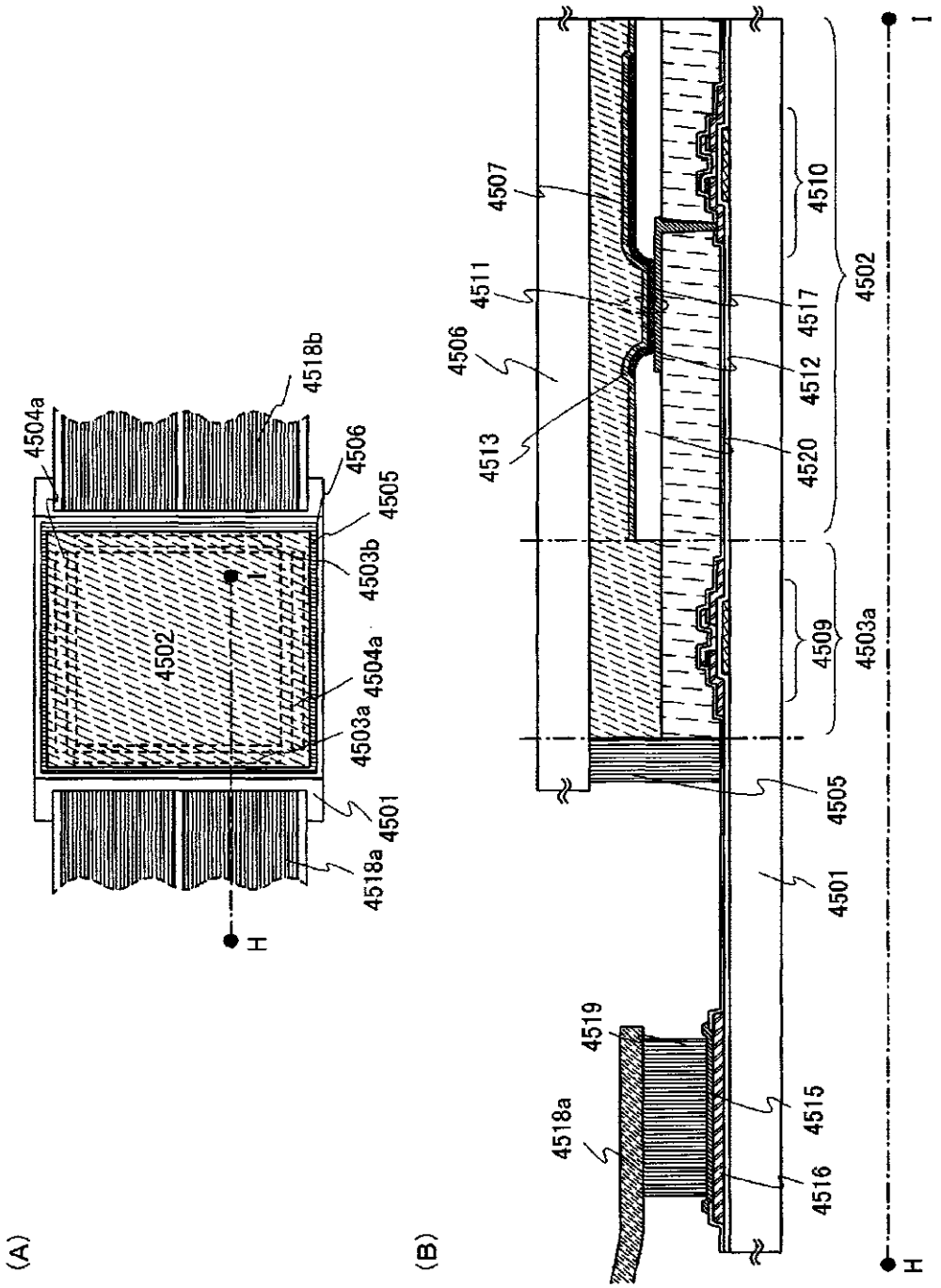
【図２０】


(A1)
(A2)
(B)
4005
4004
4006
4002
4003
4001
4018
N
M
4013
4008
4021
4020
4030
4032
4031
4035
4033
4010
4011
4019
4015
4016

【図２１】

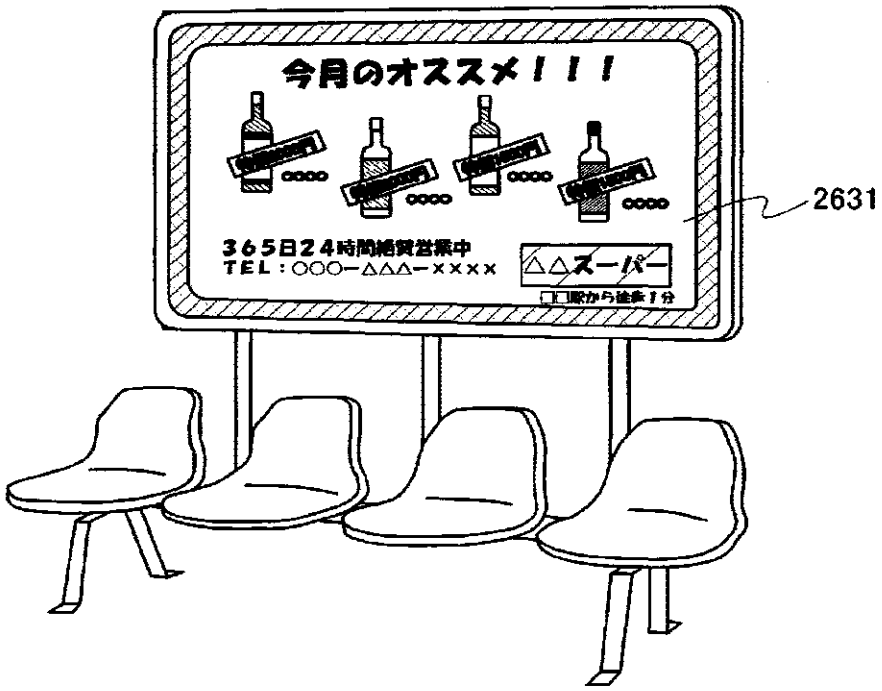

2602
2603
2604
2605
2601
2606
2608
2609
2600
2612
2607
2611
2610
2613

【図２２】

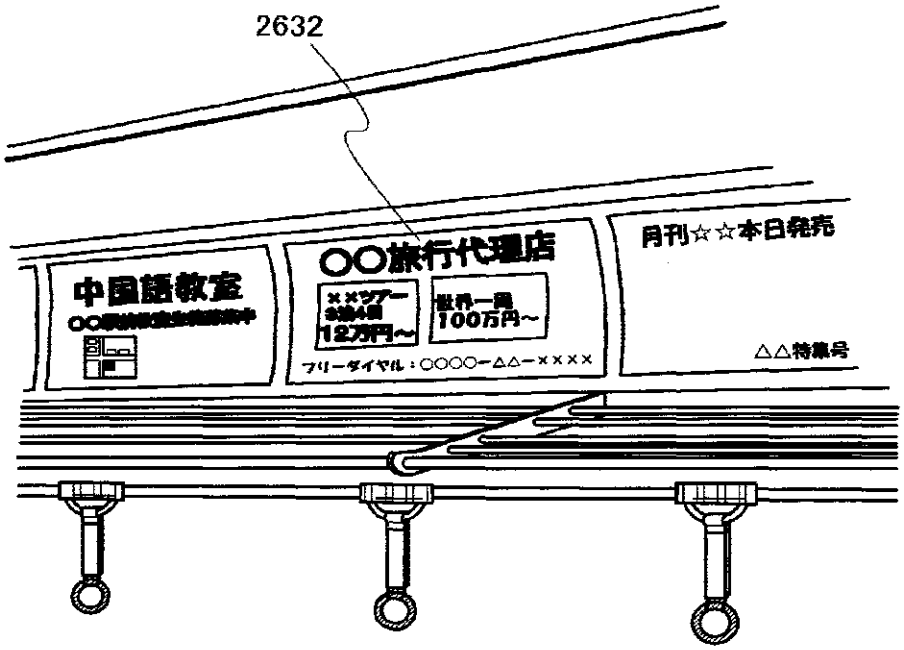

(A)
4504a
4518b
4506
4505
4503b
4502
4504a
4503a
4501
4518a
H
(B)
4507
4511
4506
4513
4510
4517
4512
4520
4502
4509
4503a
4505
4501
4519
4518a
4515
4516
I
H

【図２３】

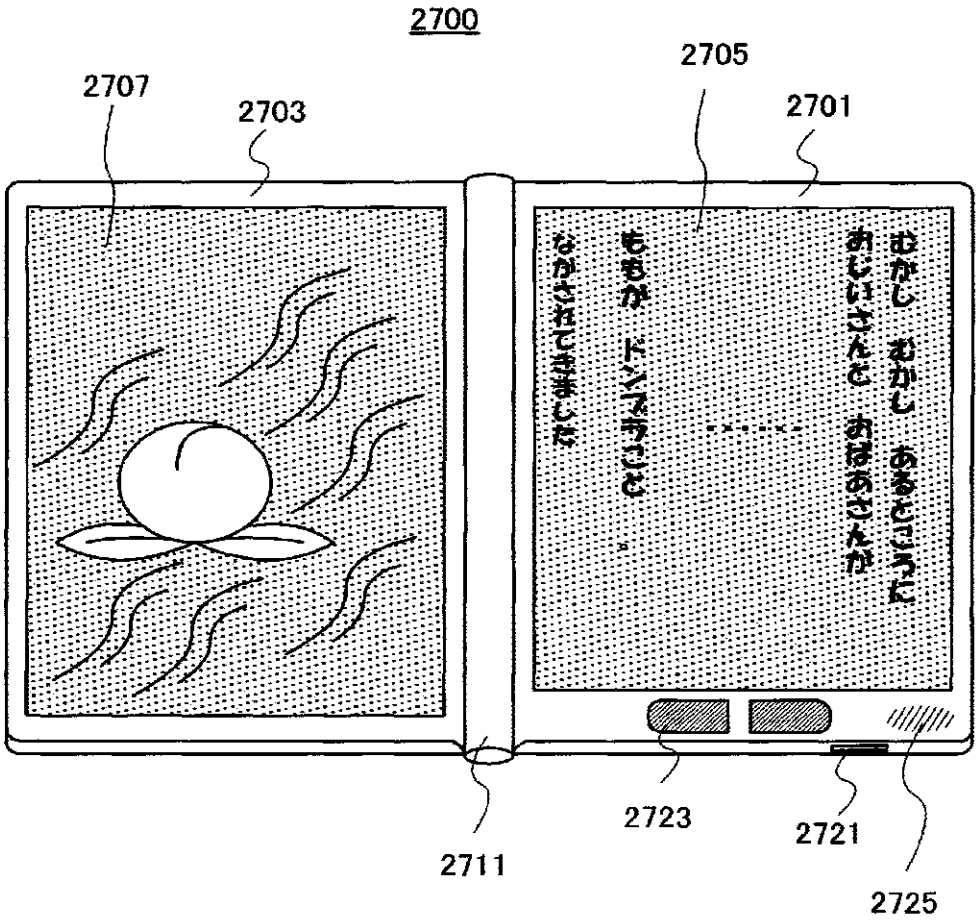
(A)


今月のオススメ！！！
365日24時間絶賛営業中
TEL：○○○－△△△－××××
△△スーパー
□□駅から徒歩１分
2631

(B)

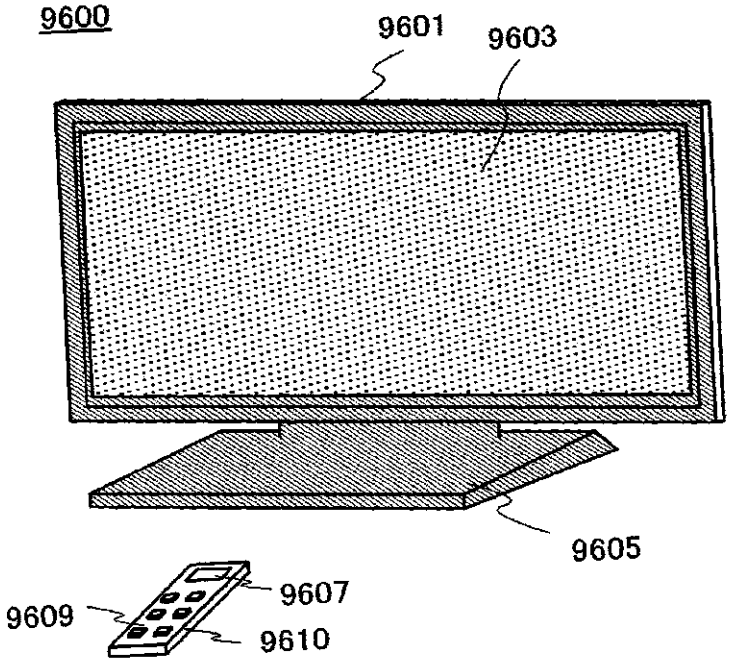

2632
中国語教室
○○旅行代理店
××ツアー
3泊4日
12万円～
往復一般
100万円～
フリーダイヤル：○○○○－△△－××××
月刊☆☆本日発売
△△特集号

【図２４】

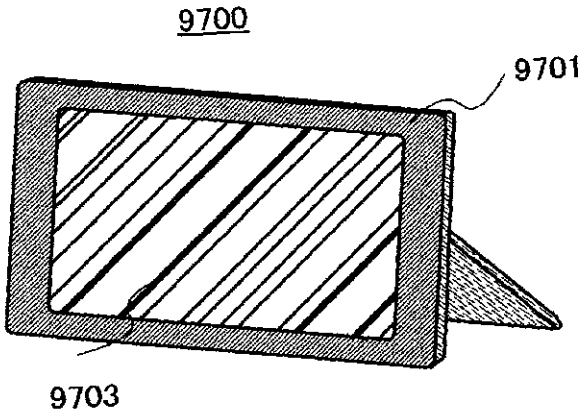

2700
2705
2707
2703
2701
むかし むかし あるところに
おじいさんと おばあさんが
ももが ドンブラコと
ながされてきました
2723
2721
2711
2725

【図２５】

(A)

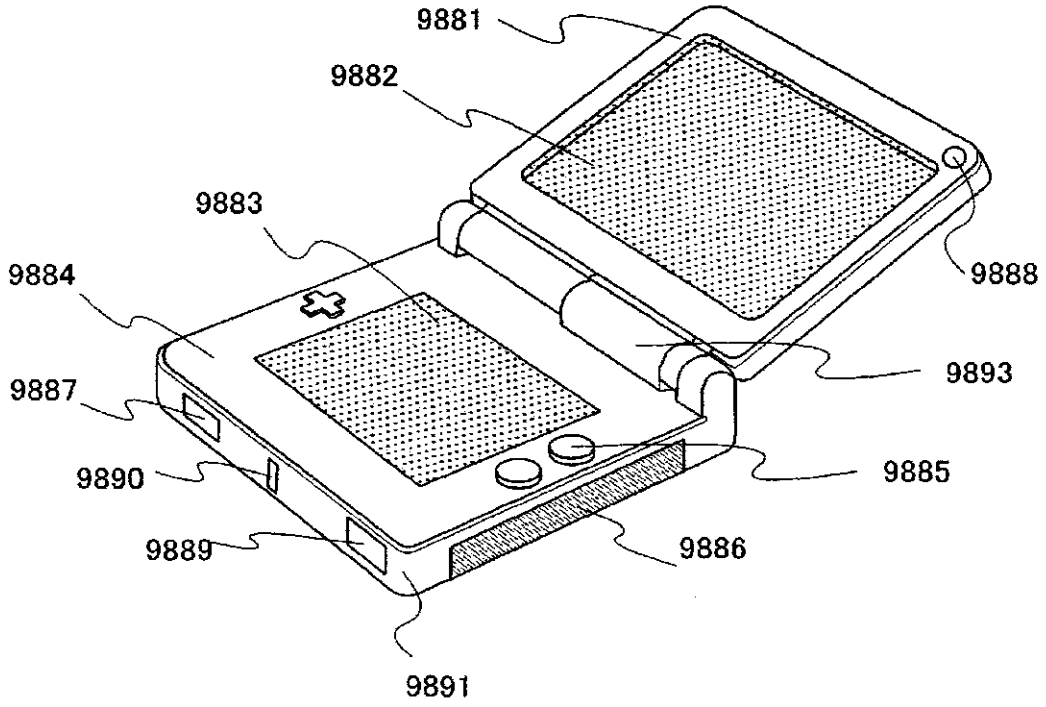


(B)

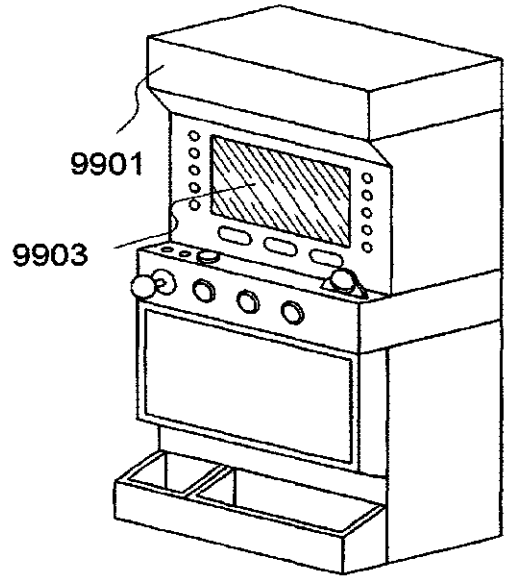


【図２６】

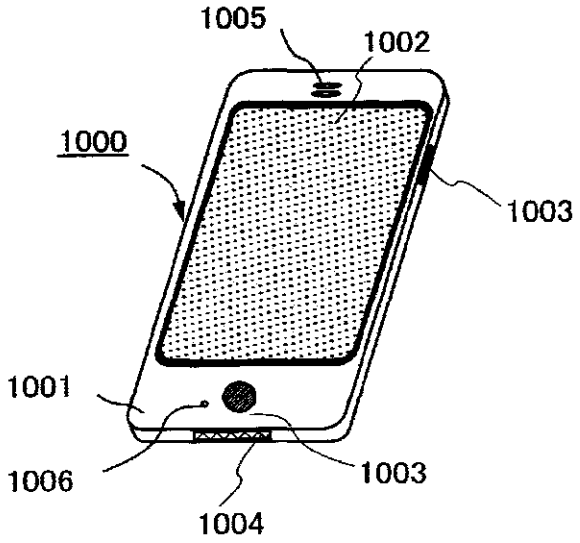
(A)


9881
9882
9883
9884
9887
9890
9889
9891
9886
9885
9893
9888

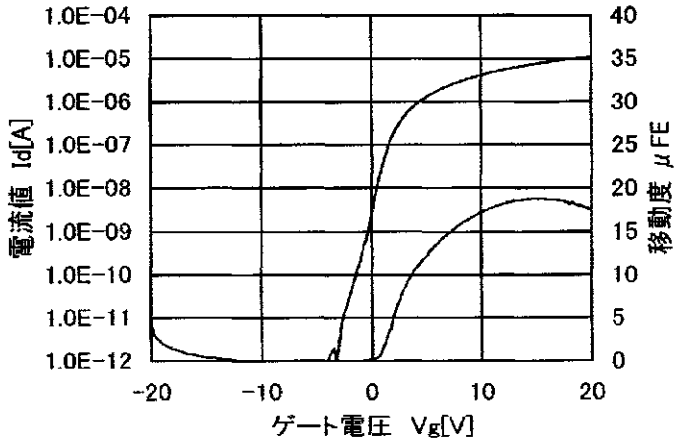
(B)


9901
9903
9900

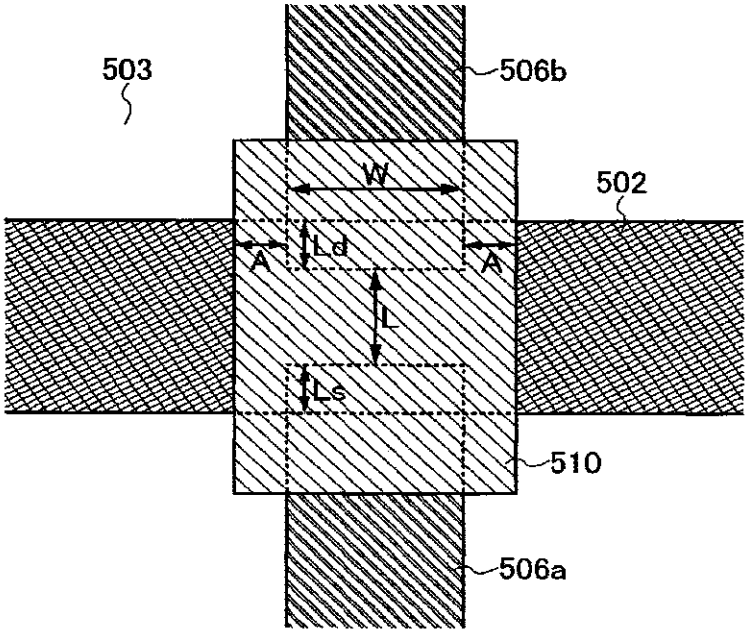
【図２７】


1005
1002
1000
1003
1001
1006
1003
1004

【図２８】

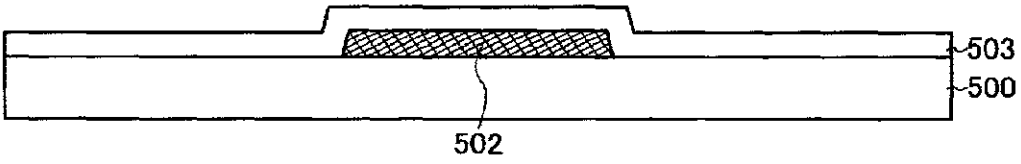

1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
1.0E-12
電流値 Id[A]
40
35
30
25
20
15
10
5
0
移動度 μFE
-20
-10
0
10
20
ゲート電圧 Vg[V]

【図２９】

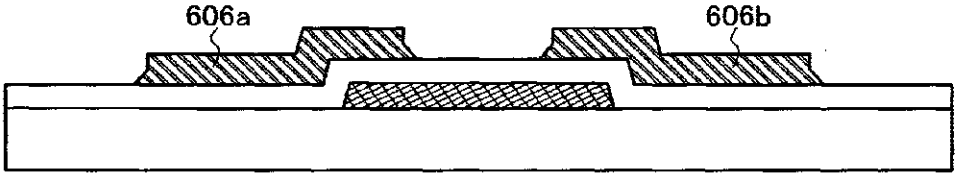


【図３０】

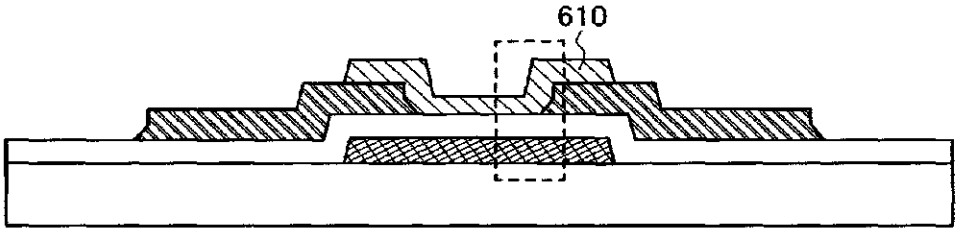
(A)



(B)

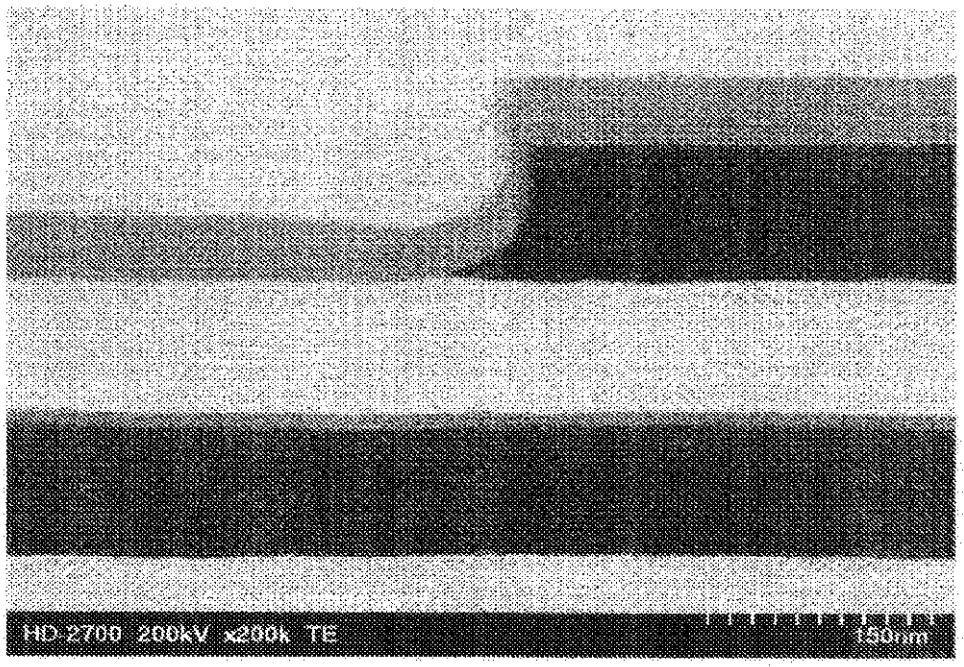


(C)

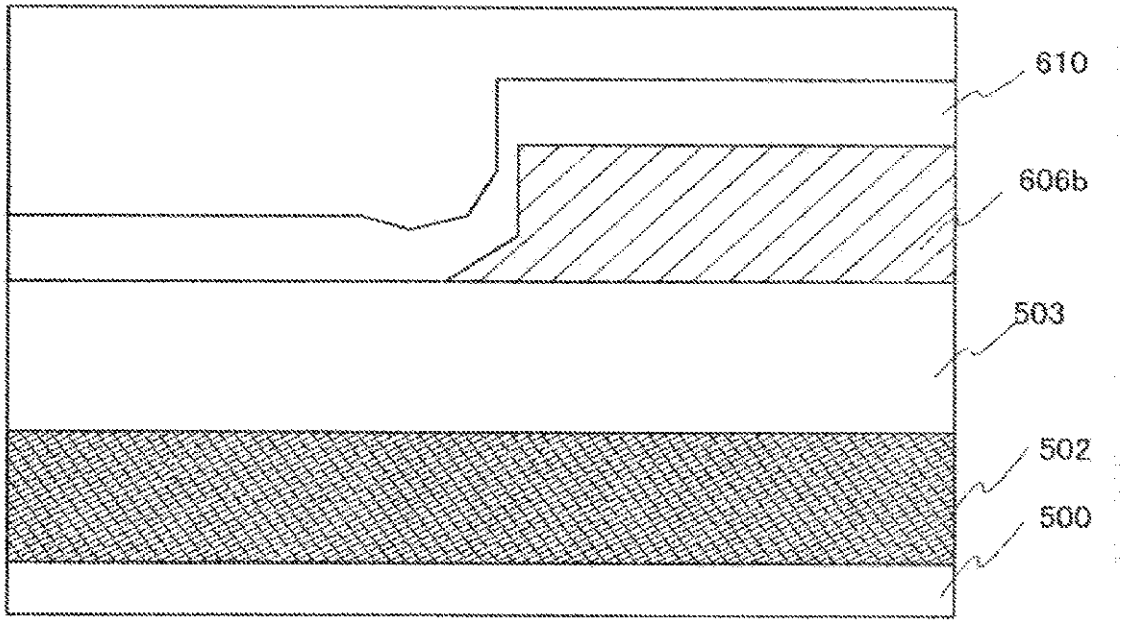


【図３１】

（Ａ）

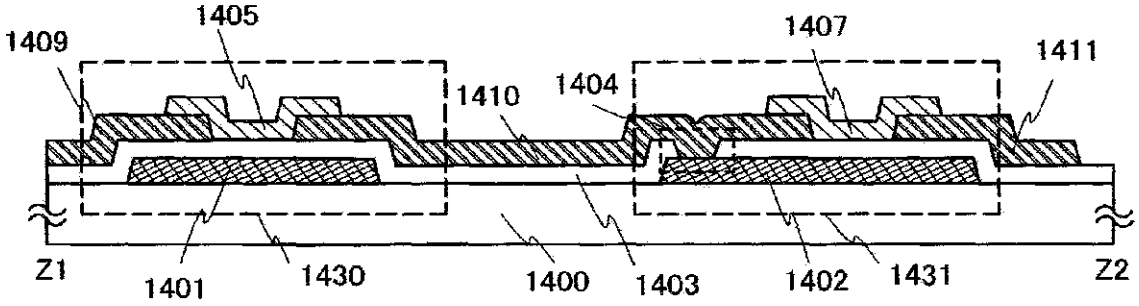


（Ｂ）

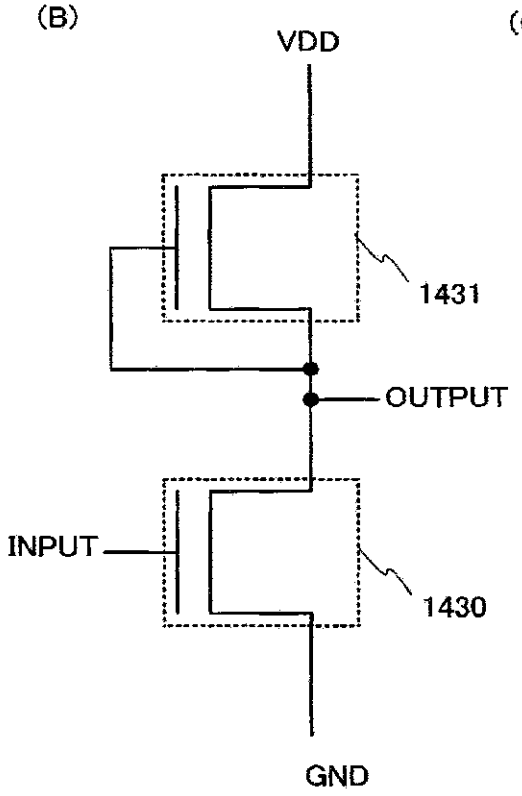


【図３２】

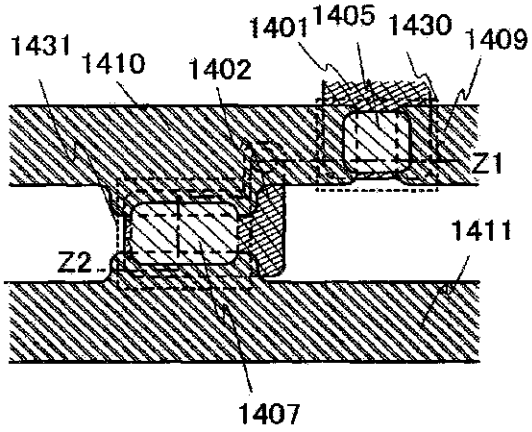
(A)


1409
1405
1410
1404
1407
1411
Z1
1401
1430
1400
1403
1402
1431
Z2

(B)


VDD
1431
OUTPUT
INPUT
1430
GND

(C)


1431
1410
1402
1401
1405
1430
1409
Z1
1411
Z2
1407

【書類名】要約書
【要約】
【課題】ボトムゲート型の薄膜トランジスタにおいて、ソース電極とドレイン電極間に生じる恐れのある電界集中を緩和し、スイッチング特性の劣化を抑える構造及びその作製方法を提供する。
【解決手段】ソース電極及びドレイン電極上に酸化物半導体層を有するボトムゲート型の薄膜トランジスタとし、酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とすることで、ソース電極及びドレイン電極の側面における電極上端から電極下端までの距離を大きくする。
【選択図】図１

出願人履歴

０００１５３８７８

19900817

新規登録

神奈川県厚木市長谷３９８番地

株式会社半導体エネルギー研究所

Attorney Docket No. 0756-10065

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 7085
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2896
Serial No. 13/763,874	)	Examiner: J. Joy
Filed: February 11, 2013	)	
For: SEMICONDUCTOR DEVICE	)	
AND MANUFACTURING	)	
METHOD THEREOF	)	

SUBMISSION OF LATE OATH/DECLARATION

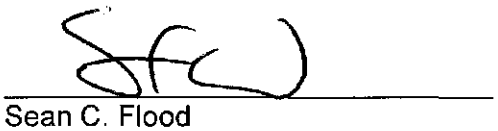
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the *Informational Notice to Applicant* dated May 13, 2013, please accept the executed declaration submitted herewith. Please be advised, the required surcharge fee under 37 C.F.R. § 1.16(f) was paid on May 7, 2013.

Furthermore, the Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



Sean C. Flood
Reg. No. 64,378

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3975 Fair Ridge Drive
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Fairfax, Virginia 22033
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下記発明者である私は、つぎのことがらを宣誓します。
As the below named inventor, I hereby declare that:

本宣誓は This declaration is directed to:

☐ 添付されている、あるいは The attached application, or

■ 米国出願、あるいは_____に出願されたPCT国際願番号_____として出願されているものに宛てられています。
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発明者の正式氏名
LEGAL NAME OF INVENTOR

発明者: Inventor: Shunpei YAMAZAKI　　日付(任意): Date (Optional): 07/18/2013

署名: Signature: Shunpei Yamazaki

備考: 出願データシート(PTO/AIA/14 あるいはその同等用紙)は、発明の自主独立体全体の命名を含め、本用紙に添付すること。なお残余の発明者ごとに PTO/SB/AIA01 用紙を使用する。
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発明者の正式氏名
LEGAL NAME OF INVENTOR

発明者: Inventor: Kengo AKIMOTO　　日付(任意): Date (Optional): 07/22/2013

署名: Signature: Kengo AKIMOTO

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発明者の正式氏名
LEGAL NAME OF INVENTOR

発明者: Inventor: Daisuke KAWAE　　日付(任意): Date (Optional): 07/21/2013

署名: Signature: Daisuke Kawae

備考: 出願データシート(PTO/AIA/14 あるいはその同等用紙) は、発明の自主独立体全体の命名を含め、本用紙に添付すること。なお残余の発明者ごとに PTO/SB/AIA01 用紙を使用する。
Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

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Electronic Acknowledgement Receipt	
EFS ID:	16453349
Application Number:	13763874
International Application Number:	
Confirmation Number:	7085
Title of Invention:	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Doris Vasquez Soriano
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Attorney Docket Number:	0756-10065
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		DEC_SUBMISSION30JULY2013.pdf	1502147 d732151691e521770b285d59a4883a269a18b4fd	yes	7

	Multipart Description/PDF files in .zip description		
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	Miscellaneous Incoming Letter	1	1
	Oath or Declaration filed	2	7
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National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/763,874	02/11/2013	Shunpei YAMAZAKI	0756-10065

CONFIRMATION NO. 7085

31780
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3975 Fair Ridge Drive
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/763,874	02/11/2013	Shunpei YAMAZAKI	0756-10065	7085

31780 7590 08/29/2013

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EXAMINER	
JOY, JEREMY J	
ART UNIT	PAPER NUMBER
2896	
MAIL DATE	DELIVERY MODE
08/29/2013	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/763,874	Applicant(s) YAMAZAKI ET AL.	
	Examiner JEREMY JOY	Art Unit 2896	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7 May 2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *2-25* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *10-25* is/are allowed.

7)☒ Claim(s) *2-9* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *11 February 2013* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☒ All b)☐ Some * c)☐ None of the:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/11/2013, 04/23/2013*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment to the claims filed on 05/07/2013 has been acknowledged and entered. Claim 1 has been cancelled and claims 2-25 have been added. Non-final office action on the merits is as follows:

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **2-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Akimoto* (**U.S. Patent Pub. No. 2007/0108446**) in view of *Kawasaki et al.* (**U.S. 2005/0056897**, from hereinafter "*Kawasaki*") in view of *Iwasaki* (**U.S. Patent Pub. No. 2008/0073653**, from hereinafter "*Iwasaki*").

Regarding Claim 2, *Akimoto* teaches a glass substrate (Fig. 1A, substrate 1); a transistor over the glass substrate, the transistor comprising: a gate electrode (Fig. 1A,

gate electrode 3); a first insulating layer over the gate electrode (Fig. 1A, insulating layer 5); an oxide semiconductor layer over the first insulating layer (Fig. 1A, oxide semiconductor layer 13); and a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer (Fig. 1A, source/drain electrode 10a/11a; (¶'s 0053-0069); a second insulating layer over the transistor (Fig. 10, layer 49); a pixel electrode over the second insulating layer (Fig. 10, pixel electrode 50); a third insulating layer over the pixel electrode (Fig. 10, second insulating layer 81); a light emitting layer over the pixel electrode and the third insulating layer (Fig. 10, light emitting layer 82); and an electrode over the light emitting layer (Fig. 10, electrode 83; ¶'s 0155- 0180).

Akimoto fails to teach wherein each of the side surface of the source electrode and a side surface of the drain electrode has a tapered shape, and wherein a first and second angle of the tapered shape that is made between the side surface of the source electrode and the drain electrode respectively and an upper surface of the glass substrate is greater than or equal to 20° and less than 90°.

Kawasaki teaches, in a similar bottom gate TFT, source and drain electrodes wherein a first angle formed a first angle between a surface of the substrate and a side surface of a first bottom edge of the source electrode and a second angle between the surface of the substrate and a side surface of a second bottom edge of the drain electrode are each greater than or equal to 20° and less than 90° (Fig. 1 and 5; source and drain regions 105, substrate 10; ¶'s 0027-0031; 45° angle).

In view of the teachings of *Kawasaki*, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the teachings of

Akimoto to include the source and drain electrodes having angles formed as claimed with respect to the substrate and the side surfaces of the electrodes because forming tapered sidewalls as disclosed by *Kawasaki* in a TFT increases device performance by reducing contact resistance between the channel region (oxide semiconductor layer of *Akimoto*) and the source and drain electrodes.

Akimoto above fails to teach the oxide semiconductor layer comprises indium and zinc but rather just teaches using a zinc oxide layer.

Iwasaki however teaches a similar TFT wherein the semiconductor channel layer comprises a semiconductor oxide channel layer comprises indium and zinc (Fig. 1, channel layer 11a; ¶ 0072-0077).

In view of the teachings of *Iwasaki*, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the teachings of *Akimoto* to include the semiconductor oxide layer comprises indium and zinc because as taught by *Iwasaki* a semiconductor oxide layer comprising multiple metals including indium and zinc can help to control the threshold voltage in a device. Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

.**Regarding Claim 3**, *Akimoto* teaches wherein each of the source and drain electrode is in contact with an upper surface of the first insulating layer (Fig. 1A).

Regarding Claim 4, *Akimoto* teaches wherein the oxide semiconductor layer is over the source and drain electrode (Fig. 1A).

Regarding Claim 5, as in the combination of *Akimoto* and *Kawasaki* above, *Akimoto* teaches wherein the oxide semiconductor layer is in contact with each of the side surface of the source and drain electrodes (Fig. 1A).

Regarding Claim 6, as in the combination of *Akimoto* and *Iwasaki* above, *Iwasaki* teaches the oxide semiconductor layer further comprises gallium (¶ 0072-0077).

Regarding Claim 7, *Akimoto* teaches the pixel electrode is in contact with the drain electrode (Fig. 10).

Regarding Claim 8, as in the combination of *Akimoto* and *Iwasaki* above, *Iwasaki* teaches the oxide semiconductor layer is a non-single-crystal film (¶ 0072-0077, amorphous semiconductor film).

Regarding Claim 9, *Akimoto* teaches a first and second buffer layer between the oxide semiconductor layer and the source electrode respectively wherein each of the first and second buffer layers has a lower resistivity than the oxide semiconductor layer (Fig. 1A, buffer layers 10b/11b; ¶ 0064-0065).

Allowable Subject Matter

4. Claims **10-25** are allowed because the prior art of record neither anticipate nor rendered obvious the limitations of base claims 10 including "wherein each of a side surface of the source electrode and a side surface of the drain electrode has a step in the lower portion thereof, wherein the first angle of the step that is made between the side surface of the source electrode and an upper surface of the glass substrate is greater than or equal to 20° and less than 90°, and wherein a second angle of the step

that is made between the side surface of the drain electrode and the upper surface of the glass substrate is greater than or equal to 20° and less than 90°" and the limitations of base claim 18 including "wherein the first angle between a surface of the glass substrate and a side surface of a first bottom edge of the source electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the source electrode, and wherein the second angle between a surface of the glass substrate and a side surface of a first bottom edge of the drain electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the drain.". In particular, the prior art of record falls short with regards to teaching that the source and drain electrodes have a step on the side surfaces of them and wherein the step comprises two different angles in relationship to the substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEREMY JOY whose telephone number is (571)270-7445. The examiner can normally be reached on Monday - Friday, 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Such can be reached on (571)-272-8895. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeremy J. Joy/
Examiner, Art Unit 2896
August 12, 2013

/Cheung Lee/
Primary Examiner, Art Unit 2896

Notice of References Cited	Application/Control No. 13/763,874	Applicant(s)/Patent Under Reexamination YAMAZAKI ET AL.	
	Examiner JEREMY JOY	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2007/0108446	05-2007	Akimoto, Kengo	257/061
*	B	US-2005/0056897	03-2005	Kawasaki et al.	257/359
*	C	US-2008/0073653	03-2008	Iwasaki, Tatsuya	257/79
	D	US-			
	E	US-			
	F	US-			
	G	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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BIB DATA SHEET

CONFIRMATION NO. 7085

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/763,874	02/11/2013	257	2896	0756-10065

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**** CONTINUING DATA ***************************

This application is a CON of 12/613,769 11/06/2009 PAT 8373164 *
which is a CON of 12/606,262 10/27/2009 ABN
(*)Data provided by applicant is not consistent with PTO records.

**** FOREIGN APPLICATIONS ***************************

JAPAN 2008-287187 11/07/2008

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

03/04/2013

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /JEREMY J JOY/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	37	24	3

ADDRESS

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UNITED STATES

TITLE

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13763874	YAMAZAKI ET AL.
	Examiner	Art Unit
	JEREMY JOY	2896

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Spoke with primary, Cheung Lee, regarding this application.	7/25/2013	Jeremy J. Joy
See search history of parent application 12/613,769	8/12/2013	Jeremy J. Joy
General keyword and EAST search is attached.	8/12/2013	Jeremy J. Joy

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/JEREMY JOY/ Examiner.Art Unit 2896	August 12, 2013

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13763874	YAMAZAKI ET AL.
	Examiner	**Art Unit**
	JEREMY JOY	2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/12/2013								
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	2	✓								
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	5	✓								
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Sheet 1 of 14

Complete if Known	
Application Number	Based on 12/613,769
Filing Date	November 6, 2009
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2896
Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10065

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7,323,368		Takayama et al.	01/29/2008	
		2007/0272922		Kim et al.	11/29/2007	
		2007/0158652		Lee et al.	07/12/2007	
		2008/0128689		Lee et al.	06/05/2008	
		7,298,084		Baude et al.	11/20/2007	
		6,532,045		Chung et al.	03/11/2003	
		2007/0108446		Akimoto	05/17/2007	
		2007/0072439		Akimoto et al.	03/29/2007	
		5,847,410		Nakajima	12/08/1998	
		6,586,346		Yamazaki et al.	07/01/2003	
		2003/0189401		Kido et al.	10/09/2003	
		6,960,812		Yamazaki et al.	11/01/2005	
		6,727,522		Kawasaki et al.	04/27/2004	
		7,061,014		Hosono et al.	06/13/2006	
		2008/0296568		Ryu et al.	12/04/2008	
		2008/0308806		Akimoto et al.	12/18/2008	
		2008/0308805		Akimoto et al.	12/18/2008	
		2008/0308804		Akimoto et al.	12/18/2008	
		2008/0308797		Akimoto et al.	12/18/2008	
		2008/0308796		Akimoto et al.	12/18/2008	

FOREIGN PATENT DOCUMENTS

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		JP	2007-123861			05/17/2007		Abst.
		JP	2007-096055			04/12/2007		Full

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Attorney Docket Number	0756-10065

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		2009/0008639		Akimoto et al.	01/08/2009	
		2007/0172591		Seo et al.	07/26/2007	
		2007/0187760		Furuta et al.	08/16/2007	
		2008/0203387		Kang et al.	08/28/2008	
		2009/0065771		Iwasaki et al.	03/12/2009	
		7,301,211		Yamazaki et al.	11/27/2007	
		2006/0244107		Sugihara et al.	11/02/2006	
		5,744,864		Cillessen et al.	04/28/1998	
		2010/0025678		Yamazaki et al.	02/04/2010	
		7,674,650		Akimoto et al.	03/09/2010	
		6,563,174		Kawasaki et al.	05/13/2003	

FOREIGN PATENT DOCUMENTS

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		JP	03-231472	A		10/15/1991		Abst.
		JP	2000-150900	A		05/30/2000		Abst.
		JP	2004-103957	A		04/02/2004		Abst.
		JP	11-505377			05/18/1999		Abst.
		JP	08-264794	A		10/11/1996		Full
		JP	2007-250983	A		09/27/2007		Abst.
		WO	2007/119386			10/25/2007		Eng.
		JP	05-251705	A		09/28/1993		Full
		WO	2004/114391			12/29/2004		Abst.
		JP	2003-086000	A		03/20/2003		Full
		JP	2003-086808	A		03/20/2003		Abst.

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		Dembo et al., "RFCPUS on Glass and Plastic Substrates Fabricated by TFT Transfer Technology," IEDM 05: TECHNICAL DIGEST OF INTERNATIONAL ELECTRON DEVICES MEETING, December 5, 2005, pp. 1067-1069.	Eng.

Examiner Signature	/Jeremy Joy/	Date Considered	08/12/2013

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		Ikeda et al., "Full-Functional System Liquid Crystal Display Using CG-Silicon Technology," SID DIGEST '04: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, 2004, Vol. 35, pp. 860-863.	Eng.
		Nomura et al., "Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Amorphous Oxide Semiconductors," NATURE, November 25, 2004, Vol. 432, pp. 488-492.	Eng.
		Takahashi et al., "Theoretical Analysis of IGZO Transparent Amorphous Oxide Semiconductor," IDW '08: PROCEEDINGS OF THE 15th INTERNATIONAL DISPLAY WORKSHOPS, December 3, 2008, pp. 1637-1640.	Eng.
		Prins et al., "A Ferroelectric Transparent Thin-Film Transistor," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), June 17, 1996, Vol. 68, No. 25, pp. 3650-3652.	Eng.
		Nakamura et al., "The Phase Relations In the In_2O_3-Ga_2ZnO_4-ZnO System at 1350°C," JOURNAL OF SOLID STATE CHEMISTRY, August 1, 1991, Vol. 93, No. 2, pp. 298-315.	Eng.
		Kimizuka et al., "Syntheses and Single-Crystal Data of Homologous Compounds, $In_2O_3(ZnO)_m$ (m = 3, 4, and 5), $InGaO_3(ZnO)_3$, and $Ga_2O_3(ZnO)_m$ (m = 7, 8, 9, and 16) in the In_2O_3-$ZnGa_2O_4$-ZnO System," JOURNAL OF SOLID STATE CHEMISTRY, April 1, 1995, Vol. 116, No. 1, pp. 170-178.	Eng.
		Nomura et al., "Thin-Film Transistor Fabricated in Single-Crystalline Transparent Oxide Semiconductor," SCIENCE, May 23, 2003, Vol. 300, No. 5623, pp. 1269-1272.	Eng.
		Osada et al., "15.2: Development of Driver-Integrated Panel using Amorphous In-Ga-Zn-Oxide TFT," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 184-187.	Eng.
		Li et al., "Modulated Structures of Homologous Compounds $InMO_3(ZnO)_m$ (M=In,Ga; m=Integer) Described by Four-Dimensional Superspace Group," JOURNAL OF SOLID STATE CHEMISTRY, 1998, Vol. 139, pp. 347-355.	Eng.

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		Lee et al., "World's Largest (15-inch) XGA AMLCD Panel Using IGZO Oxide TFT," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, pp. 625-628.	Eng.
		Nowatari et al., "60.2: Intermediate Connector with Suppressed Voltage Loss for White Tandem OLEDs," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, Vol. 40, pp. 899-902.	Eng.
		Kanno et al., "White Stacked Electrophosphorecent Organic Light-Emitting Devices Employing MoO_3 as a Charge-Generation Layer," ADV. MATER. (ADVANCED MATERIALS), 2006, Vol. 18, No. 3, pp. 339-342.	Eng.
		Tsuda et al., "Ultra Low Power Consumption Technologies for Mobile TFT-LCDs," IDW '02: PROCEEDINGS OF THE 9th INTERNATIONAL DISPLAY WORKSHOPS, December 4, 2002, pp. 295-298.	Eng.
		Jeong et al., "3.1: Distinguished Paper: 12.1-Inch WXGA AMOLED Display Driven by Indium-Gallium-Zinc Oxide TFTs Array," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, No. 1, pp. 1-4.	Eng.
		Kurokawa et al., "UHF RFCPUs on Flexible and Glass Substrates for Secure RFID Systems," JOURNAL OF SOLID-STATE CIRCUITS, 2008, Vol. 43, No. 1, pp. 292-299.	Eng.
		Ohara et al., "Amorphous In-Ga-Zn-Oxide TFTs with Suppressed Variation for 4.0 inch QVGA AMOLED Display," AM-FPD '09 DIGEST OF TECHNICAL PAPERS, July 1, 2009, pp. 227-230, THE JAPAN SOCIETY OF APPLIED PHYSICS.	Eng.
		Coates et al., "OPTICAL STUDIES OF THE AMORPHOUS LIQUID-CHOLESTERIC LIQUID CRYSTAL TRANSITION: THE "BLUE PHASE"," PHYSICS LETTERS, September 10, 1973, Vol. 45A, No. 2, pp. 115-116.	Eng.
		Cho et al., "21.2: Al and Sn-doped Zinc Indium Oxide Thin Film Transistors For AMOLED Back-Plane," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 280-283.	Eng.

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		Lee et al., "15.4: Excellent Performance of Indium-Oxide-Based Thin-Film Transistors by DC Sputtering," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 191-193.	Eng.
		Jin et al., "65.2: Distinguished Paper: World-Largest (6.5") Flexible Full Color Top Emission AMOLED Display on Plastic Film and Its Bending Properties," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 983-985.	Eng.
		Sakata et al., "Development of 4.0-In. AMOLED Display with Driver Circuit Using Amorphous In-Ga-Zn-Oxide TFTs," IDW '09: PROCEEDINGS OF THE 16th INTERNATIONAL DISPLAY WORKSHOPS, 2009, pp. 689-692.	Eng.
		Park et al., "Amorphous Indium-Gallium-Zinc Oxide TFTs and their Application for Large Size AMOLED," AM-FPD '08 DIGEST OF TECHNICAL PAPERS, July 2, 2008, pp. 275-278.	Eng.
		Park et al., "Challenge to Future Displays: Transparent AM-OLED Driven by PEALD Grown ZnO TFT," IMID '07 DIGEST, 2007, pp. 1249-1252.	Eng.
		Godo et al., "Temperature Dependence of Characteristics and Electronic Structure for Amorphous In-Ga-Zn-Oxide TFT," AM-FPD '09 DIGEST OF TECHNICAL PAPERS, July 1, 2009, pp. 41-44.	Eng.
		Osada et al., "Development of Driver-Integrated Panel using Amorphous In-Ga-Zn-Oxide TFT," AM-FPD '09 DIGEST OF TECHNICAL PAPERS, July 1, 2009, pp. 33-36.	Eng.
		Hirao et al., "Novel Top-Gate Zinc Oxide Thin-Film Transistors (ZnO TFTs) for AMLCDs," JOURNAL OF THE SID, 2007, Vol. 15, No. 1, pp. 17-22.	Eng.
		Hosono, "68.3: INVITED PAPER: TRANSPARENT AMORPHOUS OXIDE SEMICONDUCTORS FOR HIGH PERFORMANCE TFT," SID DIGEST '07: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, 2007, Vol. 38, pp. 1830-1833.	Eng.
		Godo et al., "P-9: Numerical Analysis on Temperature Dependence of Characteristics of Amorphous In-Ga-Zn-Oxide TFT," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 1110-1112.	Eng.

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		Ohara et al., "21.3: 4.0 IN. QVGA AMOLED Display Using In-Ga-Zn-Oxide TFTs with a Novel Passivation Layer," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 284-287.	Eng.
		Miyasaka, "58.2: Invited Paper: Suftla Flexible Microelectronics on their Way to Business," SID DIGEST '07: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, 2007, Vol. 38, pp. 1673-1676.	Eng.
		Chern et al., "An Analytical Model for the Above-Threshold Characteristics of Polysilicon Thin-Film Transistors," IEEE TRANSACTIONS ON ELECTRON DEVICES, July 1, 1995, Vol. 42, No. 7, pp. 1240-1246.	Eng.
		Kikuchi et al., "39.1: INVITED PAPER: OPTICALLY ISOTROPIC NANO-STRUCTURED LIQUID CRYSTAL COMPOSITES FOR DISPLAY APPLICATIONS," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 578-581.	Eng.
		Asaoka et al., "29.1: POLARIZER-FREE REFLECTIVE LCD COMBINED WITH ULTRA LOW-POWER DRIVING TECHNOLOGY," SID DIGEST '09: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 31, 2009, pp. 395-398.	Eng.
		Lee et al., "Current Status of, Challenges to, and Perspective View of AM-OLED," IDW '06: PROCEEDINGS OF THE 13th INTERNATIONAL DISPLAY WORKSHOPS, December 7, 2006, pp. 663-666.	Eng.
		Kikuchi et al., "62.2: Invited Paper: Fast Electro-Optical Switching in Polymer-Stabilized Liquid Crystalline Blue Phases for Display Application," SID DIGEST '07: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, 2007, Vol. 38, pp. 1737-1740.	Eng.
		Kikuchi et al., "Polymer-Stabilized Liquid Crystal Blue Phases," NATURE MATERIALS, September 2, 2002, Vol. 1, pp. 64-68.	Eng.

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Attorney Docket Number	0756-10065

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2002/0056838		Ogawa	05/16/2002	
		2006/0169973		Isa et al.	08/03/2006	
		2006/0208977		Kimura	09/21/2006	
		2006/0238135		Kimura	10/26/2006	
		7,064,346		Kawasaki et al.	06/20/2006	
		2006/0170111		Isa et al.	08/03/2006	
		2007/0054507		Kaji et al.	03/08/2007	
		2004/0127038		Carcia et al.	07/01/2004	
		2004/0038446		Takeda et al.	02/26/2004	
		2006/0108636		Sano et al.	05/25/2006	
		2006/0108529		Saito et al.	05/25/2006	
		2006/0110867		Yabuta et al.	05/25/2006	
		2006/0113536		Kumomi et al.	06/01/2006	
		2006/0113565		Abe et al.	06/01/2006	
		2006/0113539		Sano et al.	06/01/2006	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Kimizuka et al., "Spinel, $YbFe_2O_4$, and $Yb_2Fe_3O_7$ Types of Structures for Compounds in the In_2O_3 and Sc_2O_3-A_2O_3-BO Systems [A: Fe, Ga, Or Al; B: Mg, Mn, Fe, Ni, Cu, or Zn] at Temperatures Over 1000°C," JOURNAL OF SOLID STATE CHEMISTRY, 1985, Vol. 60, pp. 382-384.	Eng.
		Kitzerow et al., "Observation of Blue Phases in Chiral Networks," Liquid Crystals, 1993, Vol. 14, No. 3, pp. 911-916.	Eng.
		Costello et al., "Electron Microscopy of a Cholesteric Liquid Crystal and its Blue Phase," PHYS. REV. A (PHYSICAL REVIEW A), May 1, 1984, Vol. 29, No. 5, pp. 2957-2959.	Eng.
		Meiboom et al., "Theory of the Blue Phase of Cholesteric Liquid Crystals," PHYS. REV. LETT. (PHYSICAL REVIEW LETTERS), May 4, 1981, Vol. 46, No. 18, pp. 1216-1219.	Eng.

Examiner Signature	/Jeremy Joy/	Date Considered	08/12/2013

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 8 of 14

Complete if Known	
Application Number	Based on 12/613,769
Filing Date	November 6, 2009
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2896
Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10065

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		2006/0113549		Den et al.	06/01/2006	
		7,323,356		Hosono et al.	01/29/2008	
		6,294,274		Kawazoe et al.	09/25/2001	
		7,282,782		Hoffman et al.	10/16/2007	
		7,297,977		Hoffman et al.	11/20/2007	
		7,462,862		Hoffman et al.	12/09/2008	
		2008/0254569		Hoffman et al.	10/16/2008	
		2009/0073325		Kuwabara et al.	03/19/2009	
		2005/0199959		Chiang et al.	09/15/2005	
		7,049,190		Takeda et al.	05/23/2006	
		2007/0194379		Hosono et al.	08/23/2007	
		2009/0134399		Sakakura et al.	05/28/2009	
		2006/0231882		Kim et al.	10/19/2006	
		2006/0284171		Levy et al.	12/21/2006	
		2006/0284172		Ishii	12/21/2006	
		2006/0292777		Dunbar	12/28/2006	
		2007/0024187		Shin et al.	02/01/2007	
		2007/0046191		Saito	03/01/2007	
		2007/0052025		Yabuta	03/08/2007	
		2007/0090365		Hayashi et al.	04/26/2007	
		2007/0187678		Hirao et al.	08/16/2007	
		2007/0252928		Ito et al.	11/01/2007	
		2007/0287296		Chang	12/13/2007	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP	60-198861	A		10/08/1985		Full
		JP	2000-044236	A		02/15/2000		Full
		JP	2002-289859	A		10/04/2002		Full
		JP	2002-076356	A		03/15/2002		Full
		JP	2004-273732	A		09/30/2004		Full
		JP	2004-273614	A		09/30/2004		Full

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U.S. PATENT DOCUMENTS

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		2008/0038882		Takechi et al.	02/14/2008	
		2008/0038929		Chang	02/14/2008	
		2008/0050595		Nakagawara et al.	02/28/2008	
		2008/0073653		Iwasaki	03/27/2008	
		2008/0083950		Pan et al.	04/10/2008	
		2008/0106191		Kawase	05/08/2008	
		2008/0129195		Ishizaki et al.	06/05/2008	
		2008/0166834		Kim et al.	07/10/2008	
		2008/0182358		Cowdery-Corvan et al.	07/31/2008	
		2008/0224133		Park et al.	09/18/2008	
		2008/0258139		Ito et al.	10/23/2008	
		2008/0258140		Lee et al.	10/23/2008	
		2008/0258141		Park et al.	10/23/2008	
		2008/0258143		Kim et al.	10/23/2008	
		2009/0114910		Chang	05/07/2009	
		7,105,868		Nause et al.	09/12/2006	
		7,402,506		Levy et al.	07/22/2008	
		7,411,209		Endo et al.	08/12/2008	
		7,453,065		Saito et al.	11/18/2008	
		7,453,087		Iwasaki	11/18/2008	
		7,468,304		Kaji et al.	12/23/2008	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP	63-210022	A		08/31/1988		Full
		JP	63-210023	A		08/31/1988		Full
		JP	63-210024	A		08/31/1988		Full
		JP	63-215519	A		09/08/1988		Full
		JP	63-239117	A		10/05/1988		Full
		JP	63-265818	A		11/02/1988		Full
		EP	1 737 044	A		12/27/2006		Eng.
		EP	2 226 847	A		09/08/2010		Eng.

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		2006/0197092		Hoffman et al.	09/07/2006	
		2008/0006877		Mardilovich et al.	01/10/2008	
		2006/0228974		Thelss et al.	10/12/2006	
		2002/0132454		Ohtsu et al.	09/19/2002	
		2009/0152541		Maekawa et al.	06/18/2009	
		2001/0046027		Tai et al.	11/29/2001	
		2006/0035452		Carcia et al.	02/16/2006	
		7,501,293		Ito et al.	03/10/2009	
		7,211,825		Shih et al.	05/01/2007	
		2005/0017302		Hoffman	01/27/2005	
		5,731,856		Kim et al.	03/24/1998	
		2003/0218222		Wager et al.	11/27/2003	
		7,385,224		Ishii et al.	06/10/2008	
		2007/0152217		Lai et al.	07/05/2007	
		2009/0068773		Lai et al.	03/12/2009	
		7,732,819		Akimoto et al.	06/08/2010	
		2006/0043377		Hoffman et al.	03/02/2006	
		2009/0278122		Hosono et al.	11/12/2009	
		2009/0280600		Hosono et al.	11/12/2009	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Fortunato et al., "WIDE-BANDGAP HIGH-MOBILITY ZNO THIN-FILM TRANSISTORS PRODUCED AT ROOM TEMPERATURE," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), September 27, 2004, Vol. 85, No. 13, pp. 2541-2543.	Eng.
		Park et al., "Improvements in the Device Characteristics of Amorphous Indium Gallium Zinc Oxide Thin-Film Transistors by Ar Plasma Treatment," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), June 26, 2007, Vol. 90, No. 26, pp. 262106-1-262106-3.	Eng.

Examiner Signature	/Jeremy Joy/	Date Considered	08/12/2013

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		Hayashi et al., "42.1: Invited Paper: Improved Amorphous In-Ga-Zn-O TFTs," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, pp. 621-624.	Eng.
		Masuda et al., "Transparent thin film transistors using ZnO as an active channel layer and their electrical properties," J. APPL. PHYS. (JOURNAL OF APPLIED PHYSICS), February 1, 2003, Vol. 93, No. 3, pp. 1624-1630.	Eng.
		Asakuma et al., "Crystallization and Reduction of Sol-Gel-Derived Zinc Oxide Films by Irradiation with Ultraviolet Lamp," JOURNAL OF SOL-GEL SCIENCE AND TECHNOLOGY, 2003, Vol. 26, pp. 181-184.	Eng.
		Nomura et al., "Carrier transport in transparent oxide semiconductor with intrinsic structural randomness probed using single-crystalline $InGaO_3(ZnO)_5$ films," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), September 13, 2004, Vol. 85, No. 11, pp. 1993-1995.	Eng.
		Son et al., "42.4L: Late-News Paper: 4 Inch QVGA AMOLED Driven by the Threshold Voltage Controlled Amorphous GIZO (Ga_2O_3-In_2O_3-ZnO) TFT," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, pp. 633-636.	Eng.
		Van de Walle, "Hydrogen as a Cause of Doping in Zinc Oxide," PHYS. REV. LETT. (PHYSICAL REVIEW LETTERS), July 31, 2000, Vol. 85, No. 5, pp. 1012-1015.	Eng.
		Fung et al., "2-D Numerical Simulation of High Performance Amorphous In-Ga-Zn-O TFTs for Flat Panel Displays," AM-FPD '08 DIGEST OF TECHNICAL PAPERS, July 2, 2008, pp. 251-252, THE JAPAN SOCIETY OF APPLIED PHYSICS.	Eng.
		Park et al., "High performance amorphous oxide thin film transistors with self-aligned top-gate structure," IEDM 09: TECHNICAL DIGEST OF INTERNATIONAL ELECTRON DEVICES MEETING, December 7, 2009, pp. 191-194.	Eng.

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Sheet 12 of 14

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Group Art Unit	2896
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		Nakamura, "Synthesis of Homologous Compound with New Long-Period Structure," NIRIM NEWSLETTER, March 1, 1995, Vol. 150, pp. 1-4.	Full
		Park et al., "42.3: Transparent ZnO Thin Film Transistor for the Application of High Aperture Ratio Bottom Emission AM-OLED Display," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, pp. 629-632.	Eng.
		Orita et al., "Mechanism of Electrical Conductivity of Transparent $InGaZnO_4$," PHYS. REV. B (PHYSICAL REVIEW B), January 15, 2000, Vol. 61, No. 3, pp. 1811-1816.	Eng.
		Nomura et al., "Amorphous Oxide Semiconductors for High-Performance Flexible Thin-Film Transistors," JPN. J. APPL. PHYS. (JAPANESE JOURNAL OF APPLIED PHYSICS), 2006, Vol. 45, No. 5B, pp. 4303-4308.	Eng.
		Janotti et al., "Native Point Defects in ZnO," PHYS. REV. B (PHYSICAL REVIEW. B), October 4, 2007, Vol. 76, No. 16, pp. 165202-1–165202-22.	Eng.
		Park et al., "Electronic Transport Properties of Amorphous Indium-Gallium-Zinc Oxide Semiconductor Upon Exposure to Water," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), 2008, Vol. 92, pp. 072104-1-072104-3.	Eng.
		Hsieh et al., "P-29: Modeling of Amorphous Oxide Semiconductor Thin Film Transistors and Subgap Density of States," SID DIGEST '08: SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, 2008, Vol. 39, pp. 1277-1280.	Eng.
		Janotti et al., "Oxygen Vacancies in ZnO," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), 2005, Vol. 87, pp. 122102-1-122102-3.	Eng.
		Oba et al., "Defect energetics in ZnO: A hybrid Hartree-Fock density functional study," PHYS. REV. B (PHYSICAL REVIEW B), 2008, Vol. 77, pp. 245202-1-245202-6.	Eng.

Examiner Signature	/Jeremy Joy/	Date Considered	08/12/2013

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		Orita et al., "Amorphous transparent conductive oxide $InGaO_3(ZnO)_m$ ($m<4$): a Zn 4s conductor," PHILOSOPHICAL MAGAZINE, 2001, Vol. 81, No. 5, pp. 501-515.	Eng.
		Hosono et al., "Working hypothesis to explore novel wide band gap electrically conducting amorphous oxides and examples," J. NON-CRYST. SOLIDS (JOURNAL OF NON-CRYSTALLINE SOLIDS), 1996, Vol. 198-200, pp. 165-169.	Eng.
		Mo et al., "Amorphous Oxide TFT Backplanes for Large Size AMOLED Displays," IDW '08: PROCEEDINGS OF THE 6th INTERNATIONAL DISPLAY WORKSHOPS, December 3, 2008, pp. 581-584.	Eng.
		Kim et al., "High-Performance oxide thin film transistors passivated by various gas plasmas," 214th ECS MEETING, 2008, No. 2317.	Eng.
		Clark et al., "First Principles Methods Using CASTEP," Zeitschrift fur Kristallographie, 2005, Vol. 220, pp. 567-570.	Eng.
		Lany et al., "Dopability, Intrinsic Conductivity, and Nonstoichiometry of Transparent Conducting Oxides," PHYS. REV. LETT. (PHYSICAL REVIEW LETTERS), January 26, 2007, Vol. 98, pp. 045501-1-045501-4.	Eng.
		Park et al., "Dry etching of ZnO films and plasma-induced damage to optical properties," J. VAC. SCI. TECHNOL. B (JOURNAL OF VACUUM SCIENCE & TECHNOLOGY B), March 1, 2003, Vol. 21, No. 2, pp. 800-803.	Eng.
		Oh et al., "Improving the Gate Stability of ZnO Thin-Film Transistors with Aluminum Oxide Dielectric Layers," J. ELECTROCHEM. SOC. (JOURNAL OF THE ELECTROCHEMICAL SOCIETY), 2008, Vol. 155, No. 12, pp. H1009-H1014.	Eng.
		Ueno et al., "Field-Effect Transistor on $SrTiO_3$ with Sputtered Al_2O_3 Gate Insulator," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), September 1, 2003, Vol. 83, No. 9, pp. 1755-1757.	Eng.

Examiner Signature	/Jeremy Joy/	Date Considered	08/12/2013

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		2009/0152506		Umeda et al.	06/18/2009	
		2010/0092800		Itagaki et al.	04/15/2010	
		2010/0109002		Itagaki et al.	05/06/2010	
		2010/0065844		Tokunaga	03/18/2010	
		8,021,917		Akimoto et al.	09/20/2011	
		2011/0318916		Akimoto et al.	12/29/2011	
		8,030,663		Yamazaki et al.	10/04/2011	
		2012/0058599		Yamazaki et al.	03/08/2012	
		8,115,201		Yamazaki et al.	02/14/2012	
		2012/0132910		Yamazaki et al.	05/31/2012	
		2005/0056897		Kawasaki et al.	03/17/2005	
		2006/0027804		Yamazaki et al.	02/09/2006	
		2010/0117086		Akimoto et al.	05/13/2010	
		2009/0114917		Yamazaki et al.	05/07/2009	
		2010/0044711		Imai	02/25/2010	
		2005/0050897		Lewis	03/10/2005	
		2006/0292726		Akimoto et al.	12/28/2006	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	/Jeremy Joy/	Date Considered	08/12/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.J./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	268	("20030189401" | "20050050897" | "20060110867" | "20060284172" | "20080128689" | "20080258141" | "20080308796" | "20080308806" | "20090068773" | "7061014" | "20090189155" | "20020132454" | "20060231882" | "20060244107" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090114917" | "20090152541" | "20100044711" | "20110318916" | "20120132910" | "5847410" | "6294274" | "6563174" | "7323368" | "7402506" | "7411209" | "8030663" | "8115201" | "8158464" | "20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "20100065844" | "20100117086" | "5731856" | "7385224" | "7462862" | "7732819" | "20030218222" | "20060027804" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080203387" | "20080254569" | "20080258140" | "20090008639" | "20090278122" | "20090280600" | "20100025678" | "7049190" | "20090189156" | "8134156" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "20070172591" | "20080296568" | "20100109002" | "7211825" | "7453065" | "20080182358" | "20090073325" | "6532045" | "7453087" | "7501293" | "7674650" | "8021917" | "20050056897" | "20060035452" | "20060108636" | "20060113549" | "20060197092" | "20070072439" | "20070090365" | "20070158652" | "20070187760" | "20080166834" | "20080308797" | "20090134399" | "20090152506" | "5744864" | "6586346" | "6727522" | "6960812" | "7064346" | "7282782" | "7298084" | "7301211" | "7468304" | "20090186445" | "8368079" | "20040038446" | "20040127038" | "20050017302" | "20050199959"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 09:01

		"20060043377" | "20060113536" | "20060170111" | "20060292726" | "20070046191" | "20070108446" | "20070252928" | "20070272922" | "20080073653" | "20080129195" | "20080258143" | "20080308804" | "20080308805" | "20090065771" | "20090114910" | "20100092800" | "20120058599" | "7105868" | "7297977" | "7323356" | "20100003783").PN.				
L3	6320	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/12 09:01
L4	368	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/12 09:01
L5	77	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/12 09:01
L6	6569	L3 L4 L5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 09:01
L7	143950	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 09:01
L8	11923	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 09:01
L9	1895	L7 and L8	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 09:01
L10	617	L6 and L9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 09:01
L15	133	("20030189401" | "20050050897" | "20060110867" | "20060284172" | "20080128689" | "20080258141" | "20080308796" | "20080308806" | "20090068773" | "7061014" | "20090189155" | "20020132454" | "20060231882" | "20060244107" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090114917" | "20090152541" | "20100044711" | "20110318916" | "20120132910" | "5847410" | "6294274" | "6563174" | "7323368" | "7402506" | "7411209" | "8030663" | "8115201" | "8158464" | "20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "20100065844" | "20100117086" | "5731856" |	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2013/08/12 09:02

		"7385224" | "7462862" | "7732819" | "20030218222" | "20060027804" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080203387" | "20080254569" | "20080258140" | "20090008639" | "20090278122" | "20090280600" | "20100025678" | "7049190" | "20090189156" | "8134156" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "20070172591" | "20080296568" | "20100109002" | "7211825" | "7453065" | "20080182358" | "20090073325" | "6532045" | "7453087" | "7501293" | "7674650" | "8021917" | "20050056897" | "20060035452" | "20060108636" | "20060113549" | "20060197092" | "20070072439" | "20070090365" | "20070158652" | "20070187760" | "20080166834" | "20080308797" | "20090134399" | "20090152506" | "5744864" | "6586346" | "6727522" | "6960812" | "7064346" | "7282782" | "7298084" | "7301211" | "7468304" | "20090186445" | "8368079" | "20040038446" | "20040127038" | "20050017302" | "20050199959" | "20060043377" | "20060113536" | "20060170111" | "20060292726" | "20070046191" | "20070108446" | "20070252928" | "20070272922" | "20080073653" | "20080129195" | "20080258143" | "20080308804" | "20080308805" | "20090065771" | "20090114910" | "20100092800" | "20120058599" | "7105868" | "7297977" | "7323356" | "20100003783").PN.				
S1	2	"US 20100117077"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 14:18
S2	1806	"257/43".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S3	128	"257/E21.459".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S4	1431	"438/158".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S5	537	"257/E29.296".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S6	1194	"257/57".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S7	1225	"438/104".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S8	5416	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:35

S9	274	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:35
S10	54	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:36
S11	109	("20080128689" | "20030189401" | "20080308796" | "20080308806" | "7061014" | "20060110867" | "20060284172" | "20080258141" | "20090068773" | "7323368" | "20060244107" | "5847410" | "6563174" | "20020132454" | "20060231882" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090152541" | "6294274" | "7402506" | "7411209" | "20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "5731856" | "7385224" | "7462862" | "7732819" | "20080203387" | "20090008639" | "20100025678" | "20030218222" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080254569" | "20080258140" | "20090278122" | "20090280600" | "7049190" | "20070172591" | "20080296568" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "7211825" | "7453065" | "6532045" | "7674650" | "20080182358" | "20090073325" | "7453087" | "7501293" | "20070072439" | "20070158652" | "7298084" | "20070187760" | "20080308797" | "5744864" | "6586346" | "6727522" | "6960812" | "7301211" | "20060035452" | "20060108636" | "20060113549" | "20060197092" | "20070090365" | "20080166834" | "20090134399" | "7064346" | "7282782" | "7468304" | "20070108446" | "20070272922" | "20080308804" | "20080308805" | "20090065771" | "20040038446" | "20040127038" | "20050017302" | "20050199959" | "20060043377" | "20060113536" | "20060170111" | "20070046191" | "20070252928" | "20080073653" | "20080129195" | "20080258143" | "20090114910" | "7105868" | "7297977" | "7323356").PN.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:36
S12	6	"2007123861"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2012/04/04 14:47

			IBM_TDB			
S13	7	"2007096055"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/04 14:47
S14	41	("20020153587" | "20030013261" | "20030047785" | "20030111663" | "20030207502" | "20030218221" | "20030218222" | "20030219530" | "20040023432" | "4887255" | "5744864" | "6225655" | "6255130" | "6362499" | "6563174" | "7067843").PN. OR ("7282782").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:20
S15	51	("20020171085" | "20030047785" | "20030111663" | "20030218221" | "20030218222" | "20040023432" | "20040127038" | "20050017244" | "3294660" | "5289016" | "5744864" | "6362499" | "6391462" | "6727522").PN. OR ("7297977").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:21
S16	132	("20010046027" | "20020056838" | "20020109796" | "20020132454" | "20040038446" | "20040127038" | "20040132293" | "20050017302" | "20050199959" | "20050259206" | "20050275038" | "20060035452" | "20060086933" | "20060091793" | "20060108529" | "20060108636" | "20060110867" | "20060113536" | "20060113539" | "20060113549" | "20060113565" | "20060163743" | "20060169973" | "20060170067" | "20060170111" | "20060197092" | "20060208977" | "20060228974" | "20060231882" | "20060238135" | "20060244107" | "20060284171" | "20060284172" | "20060286737" | "20060292777" | "20070024187" | "20070046191" | "20070052025" | "20070054507" | "20070072439" | "20070090365" | "20070108446" | "20070158652" | "20070172591" | "20070187678" | "20070187760" | "20070194379" | "20070252928" | "20070272922" | "20070287296" | "20080006877" | "20080038882" | "20080038929" | "20080050595" | "20080073653" | "20080083950" | "20080106191" | "20080128689" | "20080129195" | "20080166834" | "20080182358" | "20080198108" | "20080224133" | "20080254569" | "20080258139" | "20080258140" | "20080258141" | "20080258143" | "20080308796" | "20080308797" | "20080308804" | "20080308805" | "20080308806" | "20090008639" | "20090073325" | "20090114910" | "20090114911" | "20090134399" | "20090152541" | "20090153762"	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:23

		"20090186437" | "20090186445" | "20090189155" | "20090189156" | "5530265" | "5696011" | "5701167" | "5731856" | "5817548" | "6294274" | "6532045" | "6674136" | "6727522" | "6852998" | "6900461" | "7009204" | "7049190").PN. OR ("7061014" | "7064346" | "7075614" | "7105868" | "7211825" | "7282782" | "7297977" | "7323356" | "7402506" | "7411209" | "7453065" | "7453087" | "7462862" | "7468304" | "7501293").PN. OR ("7674650").URPN.				
S17	9604	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:25
S18	4685	S17 and ((semiconductor adj oxide) ((zinc indium gallium zn in ga) adj oxide))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:25
S19	322	(((semiconductor adj oxide) ((zinc indium gallium zn in ga) adj oxide)) near3 channel)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:26
S20	118	S17 and S19	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:26
S21	1	("7638360").PN.	US-PGPUB; USPAT	OR	OFF	2012/04/04 16:33
S22	7	("20050017302" | "20060244107" | "20070048970" | "20070072439" | "20070184571" | "20080254569").PN. OR ("7638360").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:33
S23	2	"US 8134156"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 16:36
S24	3	"US 20070108446"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 16:36
S25	177	("20010046027" | "20020011978" | "20020044111" | "20020056838" | "20020106839" | "20020109796" | "20020110703" | "20020132454" | "20030047785" | "20030207506" | "20030218222" | "20040038446" | "20040127038" | "20040132293" | "20040252270" | "20050017302" | "20050082541" | "20050084999" | "20050104071" | "20050164423" | "20050199959" | "20050231107" | "20050233509" | "20050250308" | "20050259206" | "20050275038" | "20060035452" | "20060043377" | "20060054888" | "20060086933" | "20060091793" | "20060108529" | "20060108636" | "20060110867" | "20060113536" | "20060113539" | "20060113549" | "20060113565" | "20060163743" | "20060169973" | "20060170067" | "20060170111" | "20060183274" | "20060197092"	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:36

		"20060208977" | "20060228974" | "20060231882" | "20060238135" | "20060244107" | "20060249733" | "20060284171" | "20060284172" | "20060286737" | "20060292777" | "20070024187" | "20070046191" | "20070052025" | "20070054507" | "20070072439" | "20070090365" | "20070108446" | "20070141784" | "20070152217" | "20070158652" | "20070172591" | "20070187678" | "20070187760" | "20070194379" | "20070238228" | "20070252928" | "20070272922" | "20070287296" | "20080006877" | "20080038882" | "20080038929" | "20080050595" | "20080073653" | "20080083950" | "20080106191" | "20080108198" | "20080128689" | "20080129195" | "20080166834" | "20080174710" | "20080182358" | "20080198108" | "20080224133" | "20080254569" | "20080258139" | "20080258140" | "20080258141" | "20080258143" | "20080308796").PN. OR ("20080308797" | "20080308804" | "20080308805" | "20080308806" | "20090008639" | "20090068773" | "20090073325" | "20090114910" | "20090114911" | "20090134399" | "20090152541" | "20090153762" | "20090186437" | "20090186445" | "20090189155" | "20090189156" | "20090239335" | "20090278122" | "20090280600" | "20090305461" | "20100003783" | "20100038639" | "20100085283" | "20100240157" | "20110012119" | "20110024787" | "5382457" | "5530265" | "5696011" | "5701167" | "5731856" | "5803975" | "5817548" | "5888410" | "5930607" | "5952708" | "5994157" | "6294274" | "6459418" | "6529251" | "6532045" | "6563174" | "6674136" | "6727522" | "6819368" | "6852998" | "6900461" | "6921627" | "7009204" | "7012658" | "7049190" | "7061014" | "7064346" | "7067843" | "7075614" | "7105868" | "7189992" | "7211825" | "7264979" | "7268842" | "7282782" | "7297977" | "7323356" | "7330234" | "7339187" | "7365805" | "7385224" | "7391055" | "7402506" | "7411209" | "7453065" | "7453087" | "7456430" | "7462862" | "7468304" | "7470607" | "7485478" | "7501293" | "7560396" | "7633471" | "7732818" | "7825419" | "7855380" | "RE38292").PN. OR ("8134156").URPN.				
S26	95	S25 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:44
S27	0	(buffer near5 (source drain) with (ozide near2 semiconductor))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:48

S28	0	(buffer with (source drain) with (ozide near2 semiconductor))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:48
S29	0	(source drain) with (ozide near2 semiconductor) with channel	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:49
S30	5583	(source drain) with (oxide near2 semiconductor) with channel	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:03
S31	371	(buffer with (source drain) with (oxide near2 semiconductor))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:03
S32	118	(buffer with (source drain) with (oxide near2 semiconductor) with channel)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:03
S33	24	S32 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:04
S34	108	("20010046027" | "20020056838" | "20020132454" | "20030189401" | "20030218222" | "20040038446" | "20040127038" | "20050017302" | "20050199959" | "20060035452" | "20060043377" | "20060091793" | "20060108529" | "20060108636" | "20060110867" | "20060113536" | "20060113539" | "20060113549" | "20060113565" | "20060169973" | "20060170111" | "20060197092" | "20060208977" | "20060228974" | "20060231882" | "20060238135" | "20060244107" | "20060284171" | "20060284172" | "20060292777" | "20070024187" | "20070046191" | "20070052025" | "20070054507" | "20070072439" | "20070090365" | "20070108446" | "20070152217" | "20070172591" | "20070187678" | "20070187760" | "20070194379" | "20070252928" | "20070272922" | "20070287296" | "20080006877" | "20080038882" | "20080038929" | "20080050595" | "20080073653" | "20080083950" | "20080106191" | "20080128689" | "20080129195" | "20080166834" | "20080182358" | "20080203387" | "20080224133" | "20080254569" | "20080258139" | "20080258140" | "20080258141" | "20080258143" | "20080296568" | "20080308796" | "20080308797" | "20080308804" | "20080308805" | "20080308806" | "20090008639" | "20090065771" | "20090068773" | "20090073325" | "20090114910" | "20090134399" | "20090152541" | "20090278122" | "20090280600" | "20100025678" | "20110012118" | "5731856" | "5744864" | "5847410" | "6294274" | "6563174" | "6586346" | "6727522" | "6960812" | "7049190" | "7061014" | "7064346" | "7105868"	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:08

		"7211825" | "7282782" | "7297977" | "7301211" | "7323356" | "7385224").PN. OR ("7402506" | "7411209" | "7453065" | "7453087" | "7462862" | "7468304" | "7501293" | "7674650" | "7732819" | "7915075").PN. OR ("8021917").URPN.				
S35	43	S34 and (angle taper)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:10
S36	0	S34 and ((angle taper) near5 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:10
S37	54124	((angle taper) near5 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:13
S38	217	S37 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:13
S39	164	S38 not (angle adj implant$3)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:15
S40	3037	((taper incline decline angle) near3 (side sidewall surface) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:23
S41	178	(tft (thin adj film adj transistor)) and S40	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:24
S42	10	"US 7081641"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 17:29
S43	11	("20050056897" | "6569707" | "6858527").PN. OR ("7081641").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:30
S44	48	((taper near2 angle) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:40
S45	32689	((taper angle) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:41
S46	161	S45 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:42
S47	243	((taper angle) near3 ((source drain) adj electrode))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:42
S48	243	(taper angle) near3 ((source drain) adj electrode)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:42
S49	206	(tft (thin adj film adj transistor)) and S48	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:43
S50	69	S25 and (angle taper)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:53
S51	519	(source drain) near3 (tilt adj angle)	US-PGPUB; USPAT;	OR	ON	2012/04/04 17:56

			USOCR			
S52	54	S51 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:56
S53	5614	S8 S9 S10	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:59
S54	3354	S53 and (tft (thin adj film)) and (angle taper)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:59
S55	145	S53 and (tft (thin adj film)) and ((angle taper) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 18:00
S56	5	"US 7564058"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 18:04
S57	20	("20020043662" | "20030148561" | "20030213959" | "20030234424" | "20040189188" | "4797108" | "5028551" | "5151806" | "5640067" | "6037197" | "6121660" | "6388270" | "6433363" | "6448116" | "6476416" | "6639244" | "6709901").PN. OR ("7564058").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 18:04
S58	8	S57 and angle	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 18:05
S59	218	("20030189401" | "20080128689" | "20080308796" | "20080308806" | "7061014" | "20060110867" | "20060284172" | "20080258141" | "20090068773" | "20060244107" | "5847410" | "6563174" | "20020132454" | "20060231882" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090152541" | "6294274" | "7402506" | "7411209" | "20110012118" | "7915075" | "7462862" | "20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "5731856" | "7385224" | "7732819" | "20080203387" | "20090008639" | "20100025678" | "20030218222" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080254569" | "20080258140" | "20090278122" | "20090280600" | "7049190" | "20070172591" | "20080296568" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "7211825" | "7453065" | "7674650" | "20080182358" | "20090073325" | "7453087" | "7501293" |	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/18 18:08

		"20070072439" | "7282782" | "20070187760" | "20080308797" | "5744864" | "6586346" | "6727522" | "6960812" | "7301211" | "20060035452" | "20060091793" | "20060108636" | "20060113549" | "20060197092" | "20070090365" | "20080166834" | "20090134399" | "7064346" | "7468304" | "20050199959" | "20070108446" | "7297977" | "20080308804" | "20080308805" | "20090065771" | "20040038446" | "20040127038" | "20050017302" | "20060043377" | "20060113536" | "20060170111" | "20070046191" | "20070252928" | "20070272922" | "20080073653" | "20080129195" | "20080258143" | "20090114910" | "7105868" | "7323356").PN.				
S60	18460	(tft (thin adj film)) and ((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:28
S61	133336	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:29
S62	10304	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:29
S63	1628	S61 and S62	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:29
S64	34920	((angle taper gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:30
S65	193	S64 and S62	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:30
S66	1	("20120132910").PN.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:00
S67	10	("20110318916" | "20120058599" | "8021917" | "8030663" | "8115201").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:01
S68	11	S66 S67	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:01
S69	5731	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2012/09/26 22:04
S70	294	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2012/09/26 22:04
S71	62	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2012/09/26 22:04

S72	5942	S69 S70 S71	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:04
S73	5403	S72 and (tft (thin$1film) (thin adj film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:04
S74	3556	S73 and (angle taper)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:04
S75	878	S73 and ((angle taper) with electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:05
S76	133560	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:06
S77	10334	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:06
S78	1631	S76 and S77	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:06
S79	532	S72 and S78	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:06
S80	89	((angle taper gradation stair) near3 (source drain)) and S77 and S72	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:08
S81	5466	(257/59).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:19
S82	5099	(257/72).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:19
S83	45	((angle taper gradation stair) near3 (source drain)) and S77 and S81	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:19
S84	40	((angle taper gradation stair) near3 (source drain)) and S77 and S82	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:19
S85	60	S83 S84	US-PGPUB; USPAT;	OR	ON	2012/09/26 22:19

			USOCR			
S86	674	(257/e29.277).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:21
S87	311	(257/e21.535).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:24
S88	1543	(438/158).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:27
S89	15	((angle taper gradation stair) near3 (source drain)) and S77 and S88	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:27
S90	3682	(438/149).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:28
S91	17	((angle taper gradation stair) near3 (source drain)) and S77 and S90	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:28
S95	6242	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2013/07/01 10:27
S96	356	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2013/07/01 10:27
S97	75	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2013/07/01 10:27
S98	6489	S95 S96 S97	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/07/01 10:27
S99	142606	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2013/07/01 10:27
S100	11746	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2013/07/01 10:27
S101	1860	S99 and S100	US-PGPUB; USPAT; USOCR	OR	ON	2013/07/01 10:27
S102	600	S98 and S101	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/07/01 10:27
S103	5191	(semiconductor near5 ((indium in) and (gallium ga) and (zinc zn)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 02:30
S104	11923	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 02:30
S105	1268	S103 and S104	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 02:30

S106	1058	(IN$2ga$2zn)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 02:33

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PTO/SB/08A (07-06)
Approved for use through 03/31/2007. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	13/763,874
Filing Date	February 11, 2013
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2896 ~~2812~~
Examiner Name	~~Unknown~~ Jeremy J. Joy
Attorney Docket Number	0756-10065

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-2009/0186445	07-23-2009	AKIMOTO.K	
		US-2009/0189156	07-30-2009	AKIMOTO.K	
		US-2009/0189155	07-30-2009	AKIMOTO.K	
		US-2010/0003783	01-07-2010	AKIMOTO.K	
		US-8134156	03-13-2012	AKIMOTO.K	
		US-8158464	04-17-2012	AKIMOTO.K	
		US-8368079	02-05-2013	AKIMOTO.K	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] -Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		WO-2007/058329	05-24-2007			Eng.
		CN-101283444	10-08-2008			Abst.

Examiner Signature	/Jeremy Joy/	Date Considered	08/12/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.J./

PTO/SB/08A (07-06)
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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	13/763,874
				Filing Date	February 11, 2013
				First Named Inventor	Shunpei YAMAZAKI et al.
(Use as many sheets as necessary)				Art Unit	2812
				Examiner Name	Unknown
Sheet	2	of	2	Attorney Docket Number	0756-10065

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		CHINESE OFFICE ACTION (APPLICATION NO.200910206768.3) DATED March 15, 2013.	Full

Examiner Signature	/Jeremy Joy/	Date Considered	08/12/2013

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.J./

Attorney Docket No. 0756-10065

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No.: 7085
Shunpei YAMAZAKI et al.	)	Examiner: Jeremy J. Joy
Serial No. 13/763,874	)	Group Art Unit: 2896
Filed: February 11, 2013	)	
For: SEMICONDUCTOR DEVICE	)	
AND MANUFACTURING	)	
METHOD THEREOF	)	

AMENDMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action dated August 29, 2013, please consider the following amendments and remarks in connection with the above-identified application.

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Currently Amended) A semiconductor device comprising:

a glass substrate;

a transistor over the glass substrate, the transistor comprising:

a gate electrode;

a first insulating layer over the gate electrode;

an oxide semiconductor layer over the first insulating layer; [[and]]

a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer;

a first buffer layer between the oxide semiconductor layer and the source electrode; and

a second buffer layer between the oxide semiconductor layer and the drain electrode;

a second insulating layer over the transistor;

a pixel electrode over the second insulating layer;

a third insulating layer over the pixel electrode;

a light-emitting layer over the pixel electrode and the third insulating layer;

an electrode over the light-emitting layer,

wherein the oxide semiconductor layer comprises indium and zinc,

wherein each of a side surface of the source electrode and a side surface of the drain electrode has a tapered shape,

wherein the second insulating layer is in contact with an upper surface of the

source electrode and an upper surface of the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer,

wherein a first angle of the tapered shape that is made between the side surface of the source electrode and an upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°, and

wherein a second angle of the tapered shape that is made between the side surface of the drain electrode and the upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°.

3. (Previously Presented) The semiconductor device according to claim 2, wherein each of the source electrode and the drain electrode is in contact with an upper surface of the first insulating layer.

4. (Previously Presented) The semiconductor device according to claim 2, wherein the oxide semiconductor layer is over the source electrode and the drain electrode.

5. (Previously Presented) The semiconductor device according to claim 2, wherein the oxide semiconductor layer is in contact with each of the side surface of the source electrode and the side surface of the drain electrode.

6. (Previously Presented) The semiconductor device according to claim 2, wherein the oxide semiconductor layer further comprises gallium.

7. (Previously Presented) The semiconductor device according to claim 2, wherein the pixel electrode is in contact with the drain electrode.

8. (Previously Presented) The semiconductor device according to claim 2, wherein the oxide semiconductor layer is a non-single-crystal film.

9. (Canceled)

10. (Previously Presented) A semiconductor device comprising:

a glass substrate;

a transistor over the glass substrate, the transistor comprising:

a gate electrode;

a first insulating layer over the gate electrode;

an oxide semiconductor layer over the first insulating layer; and

a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer;

a second insulating layer over the transistor;

a pixel electrode over the second insulating layer;

a third insulating layer over the pixel electrode;

a light-emitting layer over the pixel electrode and the third insulating layer;

an electrode over the light-emitting layer,

wherein the oxide semiconductor layer comprises indium and zinc,

wherein each of a side surface of the source electrode and a side surface of the drain electrode has a step in a lower portion thereof,

wherein a first angle of the step that is made between the side surface of the source electrode and an upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°, and

wherein a second angle of the step that is made between the side surface of the drain electrode and the upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°.

11. (Previously Presented) The semiconductor device according to claim 10, wherein each of the source electrode and the drain electrode is in contact with an upper surface of the first insulating layer.

12. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is over the source electrode and the drain electrode.

13. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is in contact with each of the side surface of the source electrode and the side surface of the drain electrode.

14. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer further comprises gallium.

15. (Previously Presented) The semiconductor device according to claim 10, wherein the pixel electrode is in contact with the drain electrode.

16. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is a non-single-crystal film.

17. (Previously Presented) The semiconductor device according to claim 10, further comprising:

a first buffer layer between the oxide semiconductor layer and the source electrode; and

a second buffer layer between the oxide semiconductor layer and the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer.

18. (Previously Presented) A semiconductor device comprising:

a glass substrate;

a transistor over the glass substrate, the transistor comprising:

a gate electrode;

a first insulating layer over the gate electrode;

an oxide semiconductor layer over the first insulating layer; and

a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer;

a second insulating layer over the transistor;

a pixel electrode over the second insulating layer;

a third insulating layer over the pixel electrode;

a light-emitting layer over the pixel electrode and the third insulating layer;

an electrode over the light-emitting layer,

wherein the oxide semiconductor layer comprises indium and zinc,

wherein a first angle between a surface of the glass substrate and a side surface of a first bottom edge of the source electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the source electrode, and

wherein a second angle between the surface of the glass substrate and a side surface of a second bottom edge of the drain electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the drain electrode.

19. (Previously Presented) The semiconductor device according to claim 18, wherein each of the source electrode and the drain electrode is in contact with an upper

surface of the first insulating layer.

20. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is over the source electrode and the drain electrode.

21. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is in contact with each of the side surface of the source electrode and the side surface of the drain electrode.

22. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer further comprises gallium.

23. (Previously Presented) The semiconductor device according to claim 18, wherein the pixel electrode is in contact with the drain electrode.

24. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is a non-single-crystal film.

25. (Previously Presented) The semiconductor device according to claim 18, further comprising:

a first buffer layer between the oxide semiconductor layer and the source electrode; and

a second buffer layer between the oxide semiconductor layer and the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer.

REMARKS

The Official Action mailed August 29, 2013, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on February 11, 2013 and April 23, 2013.

Claims 2-25 were pending in the present application prior to the above amendment. Claim 9 has been canceled without prejudice or disclaimer and claim 2 has been amended to better recite the features of the present invention. The Applicant notes with appreciation the allowance of claims 10-25. Accordingly, claims 2-8 and 10-25 are now pending in the present application, of which claims 2, 10 and 18 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 3 of the Official Action rejects claims 2-9 as obvious based on the combination of U.S. Publication No. 2007/0108446 to Akimoto, U.S. Publication No. 2005/0056897 to Kawasaki and U.S. Publication No. 2008/0073653 to Iwasaki. The Applicant respectfully submits that a *prima facie* case of obviousness cannot be maintained against the independent claims of the present application, as amended.

As stated in MPEP §§ 2142-2144.04, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some reason to do so found either explicitly or implicitly in the references themselves or in the knowledge generally

available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims, as amended. Initially, independent claim 2 has been amended to recite a first buffer layer between the oxide semiconductor layer and the source electrode; and a second buffer layer between the oxide semiconductor layer and the drain electrode, wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer, previously recited in claim 9. In addition, claim 2 has been further amended to recite that the second insulating layer is in contact with an upper surface of the source electrode and an upper surface of the drain electrode, which is supported in the specification at least by FIG. 4C. For the reasons provided below, Akimoto, Kawasaki and Iwasaki, either alone or in combination, do not teach or suggest the above-referenced features of the present invention.

With respect to canceled claim 9, the Official Action asserts that Akimoto discloses "a first and second buffer layer between the oxide semiconductor layer and the source electrode respectively wherein each of the first and second buffer layers has a lower resistivity than the oxide semiconductor layer (Fig. 1A, buffer layers 10b/11b; ¶0064-0065)" (page 5, Id.). However, Akimoto either alone or in combination with Kawasaki and Iwasaki does not disclose that the second insulating layer is in contact with an upper surface of the source electrode and an upper surface of the drain electrode. Instead, Akimoto appears to show that the alleged first and second buffer layers 10b and 11b are interposed between an insulating layer 14 and the alleged source and drain electrodes 10a and 11a. See, for example, Akimoto at FIG. 4B.

Accordingly, Akimoto does not teach that a second insulating layer is in contact with an upper surface of the source electrode and an upper surface of the drain electrode. Furthermore, Kawasaki and Iwasaki do not cure the deficiencies of Akimoto in this regard. Therefore, the Applicant respectfully submits that Akimoto, Kawasaki and Iwasaki, either alone or in combination, do not teach or suggest that the second insulating layer is in contact with an upper surface of the source electrode and an upper surface of the drain electrode.

Since Akimoto, Kawasaki and Iwasaki do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Sean C. Flood
Reg. No. 64,378

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Electronic Acknowledgement Receipt	
EFS ID:	17494503
Application Number:	13763874
International Application Number:	
Confirmation Number:	7085
Title of Invention:	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Adele Stamper
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	AMENDMENT_25NOV2013_075610065.pdf	1309309 ace20153f1035091cf19e8a5583c78a1358696e4	no	10
Warnings:					
Information:					

Total Files Size (in bytes):	1309309

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/763,874	Filing Date 02/11/2013	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/25/2013	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 23	Minus	** 24	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/EVELYN NIMMONS/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/763,874	02/11/2013	Shunpei YAMAZAKI	0756-10065	7085

31780 7590 12/20/2013

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3975 Fair Ridge Drive
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EXAMINER	
JOY, JEREMY J	
ART UNIT	PAPER NUMBER
2896	

MAIL DATE	DELIVERY MODE
12/20/2013	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/763,874	Applicant(s) YAMAZAKI ET AL.	
	Examiner JEREMY JOY	Art Unit 2896	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/25/2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *2-8 and 10-25* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *10-25* is/are allowed.

7)☒ Claim(s) *2-8* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☒ All b)☐ Some** c)☐ None of the:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Response to Amendment

Applicant's amendment to the claims filed on 11/25/2013 has been acknowledged and entered. Final office action on the merits is as follows:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims **2-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Akimoto* (**U.S. Patent Pub. No. 2007/0108446**) in view of *Kawasaki et al.* (**U.S. 2005/0056897**, from hereinafter "*Kawasaki*") in view of *Iwasaki* (**U.S. Patent Pub. No. 2008/0073653**, from hereinafter "*Iwasaki*") in view of *Shih et al.* (**U.S. Patent Pub. No. 2006/0033098**, from hereinafter "*Shih*").

Regarding Claim 2, *Akimoto* teaches a glass substrate (Fig. 1A, substrate 1); a transistor over the glass substrate, the transistor comprising: a gate electrode (Fig. 1A, gate electrode 3); a first insulating layer over the gate electrode (Fig. 1A, insulating layer 5); an oxide semiconductor layer over the first insulating layer (Fig. 1A, oxide semiconductor layer 13); and a source electrode and a drain electrode each electrically

connected to the oxide semiconductor layer (Fig. 1A, source/drain electrode 10a/11a); a first buffer layer between the oxide semiconductor layer and the source electrode and a second buffer layer between the oxide semiconductor layer and the drain electrode (Fig. 1A, buffer layer 10b/11b, ¶ 0053-0069); a second insulating layer over the transistor (Fig. 10, layer 49); a pixel electrode over the second insulating layer (Fig. 10, pixel electrode 50); a third insulating layer over the pixel electrode (Fig. 10, second insulating layer 81); a light emitting layer over the pixel electrode and the third insulating layer (Fig. 10, light emitting layer 82); and an electrode over the light emitting layer (Fig. 10, electrode 83; ¶'s 0155- 0180), wherein each of the first buffer layer and the second buffer layer has a lower resistivity than the oxide semiconductor layer (¶ 0064). In particular, *Akimoto* teaches doping said first and second buffer layers comprising ZnO such that said buffer layers will have a lower resistance than that of the channel.

Akimoto fails to teach wherein each of the side surface of the source electrode and a side surface of the drain electrode has a tapered shape, and wherein a first and second angle of the tapered shape that is made between the side surface of the source electrode and the drain electrode respectively and an upper surface of the glass substrate is greater than or equal to 20° and less than 90°.

Kawasaki teaches, in a similar bottom gate TFT, source and drain electrodes wherein a first angle formed a first angle between a surface of the substrate and a side surface of a first bottom edge of the source electrode and a second angle between the surface of the substrate and a side surface of a second bottom edge of the drain

electrode are each greater than or equal to 20° and less than 90° (Fig. 1 and 5; source and drain regions 105, substrate 10; ¶'s 0027-0031; 45° angle).

In view of the teachings of *Kawasaki*, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the teachings of *Akimoto* to include the source and drain electrodes having angles formed as claimed with respect to the substrate and the side surfaces of the electrodes because forming tapered sidewalls as disclosed by *Kawasaki* in a TFT increases device performance by reducing contact resistance between the channel region (oxide semiconductor layer of *Akimoto*) and the source and drain electrodes.

Akimoto above fails to teach the oxide semiconductor layer comprises indium and zinc but rather just teaches using a zinc oxide layer.

Iwasaki however teaches a similar TFT wherein the semiconductor channel layer comprises a semiconductor oxide channel layer comprises indium and zinc (Fig. 1, channel layer 11a; ¶ 0072-0077).

In view of the teachings of *Iwasaki*, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the teachings of *Akimoto* to include the semiconductor oxide layer comprises indium and zinc because as taught by *Iwasaki* a semiconductor oxide layer comprising multiple metals including indium and zinc can help to control the threshold voltage in a device. Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Akimoto also fails to teach wherein the second insulating layer is in contact with an upper surface of the source electrode and an upper surface of the drain electrode and is also silent wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer although *Akimoto* does teach doping said buffer layer that comprises the same material as the oxide semiconductor layer which does substantially make it lower in resistance.

Shih however teaches in a similar device to that of *Akimoto* first and second buffer layers formed between a channel and source and drain electrodes respectively wherein each of the buffer layers has a lower resistivity than the channel layer and furthermore, wherein an upper surface of the source and drain electrode is exposed from the buffer layers (Fig. 3, channel layer 26, source/drain electrodes 24/25, first and second buffer layers24/28; ¶ 0020-0022).

In view of the teachings of *Shih*, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the teachings of *Akimoto* to include that the first and second buffer layers specifically has lower resistivity than the oxide semiconductor layer because this will improve electrical optoelectronic performance in the device as the current that flows through the device will not need to be limited due to a typical high contact resistance without the buffer layers and to include that the second insulating layer is in contact with an upper surface of the source and drain electrode because this is an obvious matter of design choice and would allow a subsequently formed pixel electrode to contact the drain electrode directly without the buffer layer also being disposed there between.

.**Regarding Claim 3**, *Akimoto* teaches wherein each of the source and drain electrode is in contact with an upper surface of the first insulating layer (Fig. 1A).

Regarding Claim 4, *Akimoto* teaches wherein the oxide semiconductor layer is over the source and drain electrode (Fig. 1A).

Regarding Claim 5, as in the combination of *Akimoto* and *Kawasaki* above, *Akimoto* teaches wherein the oxide semiconductor layer is in contact with each of the side surface of the source and drain electrodes (Fig. 1A).

Regarding Claim 6, as in the combination of *Akimoto* and *Iwasaki* above, *Iwasaki* teaches the oxide semiconductor layer further comprises gallium (¶ 0072-0077).

Regarding Claim 7, *Akimoto* teaches the pixel electrode is in contact with the drain electrode (Fig. 10).

Regarding Claim 8, as in the combination of *Akimoto* and *Iwasaki* above, *Iwasaki* teaches the oxide semiconductor layer is a non-single-crystal film (¶ 0072-0077, amorphous semiconductor film).

Allowable Subject Matter

2. Claims **10-25** are allowed because the prior art of record neither anticipate nor rendered obvious the limitations of base claims 10 including "wherein each of a side surface of the source electrode and a side surface of the drain electrode has a step in the lower portion thereof, wherein the first angle of the step that is made between the side surface of the source electrode and an upper surface of the glass substrate is greater than or equal to 20° and less than 90°, and wherein a second angle of the step

that is made between the side surface of the drain electrode and the upper surface of the glass substrate is greater than or equal to 20° and less than 90°" and the limitations of base claim 18 including "wherein the first angle between a surface of the glass substrate and a side surface of a first bottom edge of the source electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the source electrode, and wherein the second angle between a surface of the glass substrate and a side surface of a first bottom edge of the drain electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the drain.". In particular, the prior art of record falls short with regards to teaching that the source and drain electrodes have a step on the side surfaces of them and wherein the step comprises two different angles in relationship to the substrate.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEREMY JOY whose telephone number is (571)270-7445. The examiner can normally be reached on Monday - Friday, 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Such can be reached on (571)-272-8895. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JEREMY JOY/
Examiner, Art Unit 2896
December 11, 2013

/CHEUNG LEE/
Primary Examiner, Art Unit 2896

Notice of References Cited	Application/Control No. 13/763,874	Applicant(s)/Patent Under Reexamination YAMAZAKI ET AL.	
	Examiner JEREMY JOY	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2007/0108446	05-2007	Akimoto, Kengo	257/061
*	B	US-2005/0056897	03-2005	Kawasaki et al.	257/359
*	C	US-2008/0073653	03-2008	Iwasaki, Tatsuya	257/79
*	D	US-2006/0033098	02-2006	Shih et al.	257/040
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L11	2	"US 20130214270"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2013/12/11 01:46
L25	1	("20060033098").PN.	US-PGPUB; USPAT	OR	OFF	2013/12/11 01:57
L26	6558	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2013/12/11 02:41
L27	385	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2013/12/11 02:41
L28	82	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2013/12/11 02:41
L29	6814	L26 L27 L28	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/12/11 02:41
L30	148280	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2013/12/11 02:41
L31	12541	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2013/12/11 02:41
L32	1990	L30 and L31	US-PGPUB; USPAT; USOCR	OR	ON	2013/12/11 02:41
L33	649	L29 and L32	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/12/11 02:41
S1	2	"US 20100117077"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 14:18
S2	1806	"257/43".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S3	128	"257/E21.459".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S4	1431	"438/158".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S5	537	"257/E29.296".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32

S6	1194	"257/57".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S7	1225	"438/104".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S8	5416	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:35
S9	274	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:35
S10	54	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:36
S11	109	("20080128689" | "20030189401" | "20080308796" | "20080308806" | "7061014" | "20060110867" | "20060284172" | "20080258141" | "20090068773" | "7323368" | "20060244107" | "5847410" | "6563174" | "20020132454" | "20060231882" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090152541" | "6294274" | "7402506" | "7411209" | "20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "5731856" | "7385224" | "7462862" | "7732819" | "20080203387" | "20090008639" | "20100025678" | "20030218222" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080254569" | "20080258140" | "20090278122" | "20090280600" | "7049190" | "20070172591" | "20080296568" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "7211825" | "7453065" | "6532045" | "7674650" | "20080182358" | "20090073325" | "7453087" | "7501293" | "20070072439" | "20070158652" | "7298084" | "20070187760" | "20080308797" | "5744864" | "6586346" | "6727522" | "6960812" | "7301211" | "20060035452" | "20060108636" | "20060113549" | "20060197092" | "20070090365" | "20080166834" | "20090134399" | "7064346" | "7282782" | "7468304" | "20070108446" | "20070272922" | "20080308804" | "20080308805" | "20090065771" | "20040038446" | "20040127038" | "20050017302" | "20050199959" | "20060043377" | "20060113536" | "20060170111" | "20070046191" | "20070252928" | "20080073653" | "20080129195" | "20080258143" | "20090114910" | "7105868" | "7297977" |	US-PGPUB; USPAT	OR	ON	2012/04/04 14:36

		"7323356").PN.				
S12	6	"2007123861"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/04 14:47
S13	7	"2007096055"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/04 14:47
S14	41	("20020153587" | "20030013261" | "20030047785" | "20030111663" | "20030207502" | "20030218221" | "20030218222" | "20030219530" | "20040023432" | "4887255" | "5744864" | "6225655" | "6255130" | "6362499" | "6563174" | "7067843").PN. OR ("7282782").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:20
S15	51	("20020171085" | "20030047785" | "20030111663" | "20030218221" | "20030218222" | "20040023432" | "20040127038" | "20050017244" | "3294660" | "5289016" | "5744864" | "6362499" | "6391462" | "6727522").PN. OR ("7297977").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:21
S16	132	("20010046027" | "20020056838" | "20020109796" | "20020132454" | "20040038446" | "20040127038" | "20040132293" | "20050017302" | "20050199959" | "20050259206" | "20050275038" | "20060035452" | "20060086933" | "20060091793" | "20060108529" | "20060108636" | "20060110867" | "20060113536" | "20060113539" | "20060113549" | "20060113565" | "20060163743" | "20060169973" | "20060170067" | "20060170111" | "20060197092" | "20060208977" | "20060228974" | "20060231882" | "20060238135" | "20060244107" | "20060284171" | "20060284172" | "20060286737" | "20060292777" | "20070024187" | "20070046191" | "20070052025" | "20070054507" | "20070072439" | "20070090365" | "20070108446" | "20070158652" | "20070172591" | "20070187678" | "20070187760" | "20070194379" | "20070252928" | "20070272922" | "20070287296" | "20080006877" | "20080038882" | "20080038929" | "20080050595" | "20080073653" | "20080083950" | "20080106191" | "20080128689" | "20080129195" | "20080166834" | "20080182358" | "20080198108" | "20080224133" | "20080254569" |	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:23

		"20080258139" | "20080258140" | "20080258141" | "20080258143" | "20080308796" | "20080308797" | "20080308804" | "20080308805" | "20080308806" | "20090008639" | "20090073325" | "20090114910" | "20090114911" | "20090134399" | "20090152541" | "20090153762" | "20090186437" | "20090186445" | "20090189155" | "20090189156" | "5530265" | "5696011" | "5701167" | "5731856" | "5817548" | "6294274" | "6532045" | "6674136" | "6727522" | "6852998" | "6900461" | "7009204" | "7049190").PN. OR ("7061014" | "7064346" | "7075614" | "7105868" | "7211825" | "7282782" | "7297977" | "7323356" | "7402506" | "7411209" | "7453065" | "7453087" | "7462862" | "7468304" | "7501293").PN. OR ("7674650").URPN.				
S17	9604	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:25
S18	4685	S17 and ((semiconductor adj oxide) ((zinc indium gallium zn in ga) adj oxide))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:25
S19	322	(((semiconductor adj oxide) ((zinc indium gallium zn in ga) adj oxide)) near3 channel)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:26
S20	118	S17 and S19	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:26
S21	1	("7638360").PN.	US-PGPUB; USPAT	OR	OFF	2012/04/04 16:33
S22	7	("20050017302" | "20060244107" | "20070048970" | "20070072439" | "20070184571" | "20080254569").PN. OR ("7638360").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:33
S23	2	"US 8134156"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 16:36
S24	3	"US 20070108446"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 16:36
S25	177	("20010046027" | "20020011978" | "20020044111" | "20020056838" | "20020106839" | "20020109796" | "20020110703" | "20020132454" | "20030047785" | "20030207506" | "20030218222" | "20040038446" | "20040127038" | "20040132293" | "20040252270" | "20050017302" | "20050082541" | "20050084999" | "20050104071" | "20050164423" | "20050199959" | "20050231107" | "20050233509" | "20050250308" | "20050259206" | "20050275038" | "20060035452" | "20060043377"	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:36

"20060054888" | "20060086933" |
"20060091793" | "20060108529" |
"20060108636" | "20060110867" |
"20060113536" | "20060113539" |
"20060113549" | "20060113565" |
"20060163743" | "20060169973" |
"20060170067" | "20060170111" |
"20060183274" | "20060197092" |
"20060208977" | "20060228974" |
"20060231882" | "20060238135" |
"20060244107" | "20060249733" |
"20060284171" | "20060284172" |
"20060286737" | "20060292777" |
"20070024187" | "20070046191" |
"20070052025" | "20070054507" |
"20070072439" | "20070090365" |
"20070108446" | "20070141784" |
"20070152217" | "20070158652" |
"20070172591" | "20070187678" |
"20070187760" | "20070194379" |
"20070238228" | "20070252928" |
"20070272922" | "20070287296" |
"20080006877" | "20080038882" |
"20080038929" | "20080050595" |
"20080073653" | "20080083950" |
"20080106191" | "20080108198" |
"20080128689" | "20080129195" |
"20080166834" | "20080174710" |
"20080182358" | "20080198108" |
"20080224133" | "20080254569" |
"20080258139" | "20080258140" |
"20080258141" | "20080258143" |
"20080308796").PN. OR
("20080308797" | "20080308804" |
"20080308805" | "20080308806" |
"20090008639" | "20090068773" |
"20090073325" | "20090114910" |
"20090114911" | "20090134399" |
"20090152541" | "20090153762" |
"20090186437" | "20090186445" |
"20090189155" | "20090189156" |
"20090239335" | "20090278122" |
"20090280600" | "20090305461" |
"20100003783" | "20100038639" |
"20100085283" | "20100240157" |
"20110012119" | "20110024787" |
"5382457" | "5530265" | "5696011" |
"5701167" | "5731856" | "5803975" |
"5817548" | "5888410" | "5930607" |
"5952708" | "5994157" | "6294274" |
"6459418" | "6529251" | "6532045" |
"6563174" | "6674136" | "6727522" |
"6819368" | "6852998" | "6900461" |
"6921627" | "7009204" | "7012658" |
"7049190" | "7061014" | "7064346" |
"7067843" | "7075614" | "7105868" |
"7189992" | "7211825" | "7264979" |
"7268842" | "7282782" | "7297977" |
"7323356" | "7330234" | "7339187" |
"7365805" | "7385224" | "7391055" |
"7402506" | "7411209" | "7453065" |
"7453087" | "7456430" | "7462862" |
"7468304" | "7470607" | "7485478" |
"7501293" | "7560396" | "7633471" |

		"7732818" | "7825419" | "7855380" | "RE38292").PN. OR ("8134156").URPN.				
S26	95	S25 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:44
S27	0	(buffer near5 (source drain) with (ozide near2 semiconductor))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:48
S28	0	(buffer with (source drain) with (ozide near2 semiconductor))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:48
S29	0	(source drain) with (ozide near2 semiconductor) with channel	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:49
S30	5583	(source drain) with (oxide near2 semiconductor) with channel	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:03
S31	371	(buffer with (source drain) with (oxide near2 semiconductor))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:03
S32	118	(buffer with (source drain) with (oxide near2 semiconductor) with channel)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:03
S33	24	S32 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:04
S34	108	("20010046027" | "20020056838" | "20020132454" | "20030189401" | "20030218222" | "20040038446" | "20040127038" | "20050017302" | "20050199959" | "20060035452" | "20060043377" | "20060091793" | "20060108529" | "20060108636" | "20060110867" | "20060113536" | "20060113539" | "20060113549" | "20060113565" | "20060169973" | "20060170111" | "20060197092" | "20060208977" | "20060228974" | "20060231882" | "20060238135" | "20060244107" | "20060284171" | "20060284172" | "20060292777" | "20070024187" | "20070046191" | "20070052025" | "20070054507" | "20070072439" | "20070090365" | "20070108446" | "20070152217" | "20070172591" | "20070187678" | "20070187760" | "20070194379" | "20070252928" | "20070272922" | "20070287296" | "20080006877" | "20080038882" | "20080038929" | "20080050595" | "20080073653" | "20080083950" | "20080106191" | "20080128689" | "20080129195" | "20080166834" | "20080182358" | "20080203387" | "20080224133" | "20080254569" | "20080258139" | "20080258140" | "20080258141" | "20080258143" | "20080296568" | "20080308796" | "20080308797" | "20080308804" | "20080308805" | "20080308806" | "20090008639" |	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:08

		"20090065771" | "20090068773" | "20090073325" | "20090114910" | "20090134399" | "20090152541" | "20090278122" | "20090280600" | "20100025678" | "20110012118" | "5731856" | "5744864" | "5847410" | "6294274" | "6563174" | "6586346" | "6727522" | "6960812" | "7049190" | "7061014" | "7064346" | "7105868" | "7211825" | "7282782" | "7297977" | "7301211" | "7323356" | "7385224").PN. OR ("7402506" | "7411209" | "7453065" | "7453087" | "7462862" | "7468304" | "7501293" | "7674650" | "7732819" | "7915075").PN. OR ("8021917").URPN.				
S35	43	S34 and (angle taper)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:10
S36	0	S34 and ((angle taper) near5 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:10
S37	54124	((angle taper) near5 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:13
S38	217	S37 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:13
S39	164	S38 not (angle adj implant$3)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:15
S40	3037	((taper incline decline angle) near3 (side sidewall surface) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:23
S41	178	(tft (thin adj film adj transistor)) and S40	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:24
S42	10	"US 7081641"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 17:29
S43	11	("20050056897" | "6569707" | "6858527").PN. OR ("7081641").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:30
S44	48	((taper near2 angle) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:40
S45	32689	((taper angle) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:41
S46	161	S45 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:42
S47	243	((taper angle) near3 ((source drain) adj electrode))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:42
S48	243	(taper angle) near3 ((source drain) adj electrode)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:42

S49	206	(tft (thin adj film adj transistor)) and S48	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:43
S50	69	S25 and (angle taper)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:53
S51	519	(source drain) near3 (tilt adj angle)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:56
S52	54	S51 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:56
S53	5614	S8 S9 S10	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:59
S54	3354	S53 and (tft (thin adj film)) and (angle taper)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:59
S55	145	S53 and (tft (thin adj film)) and ((angle taper) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 18:00
S56	5	"US 7564058"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 18:04
S57	20	("20020043662" | "20030148561" | "20030213959" | "20030234424" | "20040189188" | "4797108" | "5028551" | "5151806" | "5640067" | "6037197" | "6121660" | "6388270" | "6433363" | "6448116" | "6476416" | "6639244" | "6709901").PN. OR ("7564058").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 18:04
S58	8	S57 and angle	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 18:05
S59	218	("20030189401" | "20080128689" | "20080308796" | "20080308806" | "7061014" | "20060110867" | "20060284172" | "20080258141" | "20090068773" | "20060244107" | "5847410" | "6563174" | "20020132454" | "20060231882" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090152541" | "6294274" | "7402506" | "7411209" | "20110012118" | "7915075" | "7462862" | "20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "5731856" | "7385224" | "7732819" | "20080203387" | "20090008639" | "20100025678" | "20030218222" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080254569" |	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/18 18:08

		"20080258140" | "20090278122" | "20090280600" | "7049190" | "20070172591" | "20080296568" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "7211825" | "7453065" | "7674650" | "20080182358" | "20090073325" | "7453087" | "7501293" | "20070072439" | "7282782" | "20070187760" | "20080308797" | "5744864" | "6586346" | "6727522" | "6960812" | "7301211" | "20060035452" | "20060091793" | "20060108636" | "20060113549" | "20060197092" | "20070090365" | "20080166834" | "20090134399" | "7064346" | "7468304" | "20050199959" | "20070108446" | "7297977" | "20080308804" | "20080308805" | "20090065771" | "20040038446" | "20040127038" | "20050017302" | "20060043377" | "20060113536" | "20060170111" | "20070046191" | "20070252928" | "20070272922" | "20080073653" | "20080129195" | "20080258143" | "20090114910" | "7105868" | "7323356").PN.				
S60	18460	(tft (thin adj film)) and ((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:28
S61	133336	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:29
S62	10304	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:29
S63	1628	S61 and S62	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:29
S64	34920	((angle taper gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:30
S65	193	S64 and S62	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:30
S66	1	("20120132910").PN.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:00
S67	10	("20110318916" | "20120058599" | "8021917" | "8030663" | "8115201").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:01
S68	11	S66 S67	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2012/09/26 22:01

			DERWENT; IBM_TDB			
S69	5731	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2012/09/26 22:04
S70	294	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2012/09/26 22:04
S71	62	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2012/09/26 22:04
S72	5942	S69 S70 S71	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:04
S73	5403	S72 and (tft (thin$1film) (thin adj film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:04
S74	3556	S73 and (angle taper)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:04
S75	878	S73 and ((angle taper) with electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:05
S76	133560	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:06
S77	10334	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:06
S78	1631	S76 and S77	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:06
S79	532	S72 and S78	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:06
S80	89	((angle taper gradation stair) near3 (source drain)) and S77 and S72	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:08
S81	5466	(257/59).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:19
S82	5099	(257/72).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:19

S83	45	((angle taper gradation stair) near3 (source drain)) and S77 and S81	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:19
S84	40	((angle taper gradation stair) near3 (source drain)) and S77 and S82	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:19
S85	60	S83 S84	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:19
S86	674	(257/e29.277).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:21
S87	311	(257/e21.535).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:24
S88	1543	(438/158).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:27
S89	15	((angle taper gradation stair) near3 (source drain)) and S77 and S88	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:27
S90	3682	(438/149).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:28
S91	17	((angle taper gradation stair) near3 (source drain)) and S77 and S90	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:28
S95	6242	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2013/07/01 10:27
S96	356	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2013/07/01 10:27
S97	75	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2013/07/01 10:27
S98	6489	S95 S96 S97	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/07/01 10:27
S99	142606	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2013/07/01 10:27
S100	11746	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2013/07/01 10:27
S101	1860	S99 and S100	US-PGPUB; USPAT; USOCR	OR	ON	2013/07/01 10:27
S102	600	S98 and S101	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/07/01 10:27
S103	5191	(semiconductor near5 ((indium in) and (gallium ga) and (zinc zn)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/08/12 02:30

			DERWENT; IBM_TDB			
S104	11923	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 02:30
S105	1268	S103 and S104	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 02:30
S106	1058	(IN$2ga$2zn)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 02:33
S107	268	("20030189401" | "20050050897" | "20060110867" | "20060284172" | "20080128689" | "20080258141" | "20080308796" | "20080308806" | "20090068773" | "7061014" | "20090189155" | "20020132454" | "20060231882" | "20060244107" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090114917" | "20090152541" | "20100044711" | "20110318916" | "20120132910" | "5847410" | "6294274" | "6563174" | "7323368" | "7402506" | "7411209" | "8030663" | "8115201" | "8158464" | "20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "20100065844" | "20100117086" | "5731856" | "7385224" | "7462862" | "7732819" | "20030218222" | "20060027804" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080203387" | "20080254569" | "20080258140" | "20090008639" | "20090278122" | "20090280600" | "20100025678" | "7049190" | "20090189156" | "8134156" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "20070172591" | "20080296568" | "20100109002" | "7211825" | "7453065" | "20080182358" | "20090073325" | "6532045" | "7453087" | "7501293" | "7674650" | "8021917" | "20050056897" | "20060035452" | "20060108636" | "20060113549" | "20060197092" | "20070072439" | "20070090365" | "20070158652" | "20070187760" | "20080166834" | "20080308797" | "20090134399" | "20090152506" | "5744864" | "6586346" | "6727522" | "6960812"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 09:01

		"7064346" | "7282782" | "7298084" | "7301211" | "7468304" | "20090186445" | "8368079" | "20040038446" | "20040127038" | "20050017302" | "20050199959" | "20060043377" | "20060113536" | "20060170111" | "20060292726" | "20070046191" | "20070108446" | "20070252928" | "20070272922" | "20080073653" | "20080129195" | "20080258143" | "20080308804" | "20080308805" | "20090065771" | "20090114910" | "20100092800" | "20120058599" | "7105868" | "7297977" | "7323356" | "20100003783").PN.				
S108	6320	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/12 09:01
S109	368	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/12 09:01
S110	77	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/12 09:01
S111	6569	S108 S109 S110	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 09:01
S112	143950	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 09:01
S113	11923	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 09:01
S114	1895	S112 and S113	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 09:01
S115	617	S111 and S114	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 09:01
S116	133	("20030189401" | "20050050897" | "20060110867" | "20060284172" | "20080128689" | "20080258141" | "20080308796" | "20080308806" | "20090068773" | "7061014" | "20090189155" | "20020132454" | "20060231882" | "20060244107" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090114917" | "20090152541" | "20100044711" | "20110318916" | "20120132910" | "5847410" | "6294274" | "6563174" | "7323368" | "7402506" | "7411209" | "8030663" | "8115201" | "8158464" |	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2013/08/12 09:02

		"20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "20100065844" | "20100117086" | "5731856" | "7385224" | "7462862" | "7732819" | "20030218222" | "20060027804" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080203387" | "20080254569" | "20080258140" | "20090008639" | "20090278122" | "20090280600" | "20100025678" | "7049190" | "20090189156" | "8134156" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "20070172591" | "20080296568" | "20100109002" | "7211825" | "7453065" | "20080182358" | "20090073325" | "6532045" | "7453087" | "7501293" | "7674650" | "8021917" | "20050056897" | "20060035452" | "20060108636" | "20060113549" | "20060197092" | "20070072439" | "20070090365" | "20070158652" | "20070187760" | "20080166834" | "20080308797" | "20090134399" | "20090152506" | "5744864" | "6586346" | "6727522" | "6960812" | "7064346" | "7282782" | "7298084" | "7301211" | "7468304" | "20090186445" | "8368079" | "20040038446" | "20040127038" | "20050017302" | "20050199959" | "20060043377" | "20060113536" | "20060170111" | "20060292726" | "20070046191" | "20070108446" | "20070252928" | "20070272922" | "20080073653" | "20080129195" | "20080258143" | "20080308804" | "20080308805" | "20090065771" | "20090114910" | "20090092800" | "20120058599" | "7105868" | "7297977" | "7323356" | "20100003783").PN.				

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13763874	YAMAZAKI ET AL.
	Examiner	**Art Unit**
	JEREMY JOY	2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/12/2013	12/11/2013							
	1	-	-							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	-							
	10	=	=							
	11	=	=							
	12	=	=							
	13	=	=							
	14	=	=							
	15	=	=							
	16	=	=							
	17	=	=							
	18	=	=							
	19	=	=							
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	21	=	=							
	22	=	=							
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13763874	YAMAZAKI ET AL.
	Examiner	Art Unit
	JEREMY JOY	2896

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Spoke with primary, Cheung Lee, regarding this application.	7/25/2013	Jeremy J. Joy
See search history of parent application 12/613,769	8/12/2013	Jeremy J. Joy
General keyword and EAST search is attached.	8/12/2013	Jeremy J. Joy
General keyword and EAST search is attached.	12/18/2013	Jeremy J. Joy

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/JEREMY JOY/ Examiner.Art Unit 2896	December 18, 2013

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BIB DATA SHEET

CONFIRMATION NO. 7085

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/763,874	02/11/2013 **RULE**	257	2896	0756-10065

APPLICANTS
SEMICONDUCTOR ENERGY LABORATORY CO., LTD., Atsugi-shi, JAPAN

INVENTORS
Shunpei YAMAZAKI, Setagaya, JAPAN;
Kengo AKIMOTO, Atsugi, JAPAN;
Daisuke KAWAE, Yamato, JAPAN;

** **CONTINUING DATA** *************************
This application is a CON of 12/613,769 11/06/2009 PAT 8373164 *
which is a CON of 12/606,262 10/27/2009 ABN
(*)Data provided by applicant is not consistent with PTO records.

** **FOREIGN APPLICATIONS** *************************
JAPAN 2008-287187 11/07/2008

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** **
03/04/2013

		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /JEREMY J JOY/ Examiner's Signature	☐ Met after Allowance Initials	JAPAN	37	24	3

ADDRESS

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033
UNITED STATES

TITLE

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

FILING FEE RECEIVED		
2060	FEES: Authority has been given in Paper No.__________ to charge/credit DEPOSIT ACCOUNT No.__________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other __________ ☐ Credit

BIB (Rev. 05/07).

Attorney Docket No. 0756-10065

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No.: 7085
Shunpei YAMAZAKI et al.	)	Examiner: Jeremy J. Joy
Serial No. 13/763,874	)	Group Art Unit: 2896
Filed: February 11, 2013	)	
For: SEMICONDUCTOR DEVICE	)	
AND MANUFACTURING	)	
METHOD THEREOF	)	

AFTER FINAL AMENDMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action dated December 20, 2013, please consider the following amendments and remarks in connection with the above-identified application.

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-9. (Canceled)

10. (Previously Presented) A semiconductor device comprising:

a glass substrate;

a transistor over the glass substrate, the transistor comprising:

a gate electrode;

a first insulating layer over the gate electrode;

an oxide semiconductor layer over the first insulating layer; and

a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer;

a second insulating layer over the transistor;

a pixel electrode over the second insulating layer;

a third insulating layer over the pixel electrode;

a light-emitting layer over the pixel electrode and the third insulating layer;

an electrode over the light-emitting layer,

wherein the oxide semiconductor layer comprises indium and zinc,

wherein each of a side surface of the source electrode and a side surface of the drain electrode has a step in a lower portion thereof,

wherein a first angle of the step that is made between the side surface of the source electrode and an upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°, and

wherein a second angle of the step that is made between the side surface of the drain electrode and the upper surface of the glass substrate is greater than or equal to

20° and smaller than or equal to 90°.

11. (Previously Presented) The semiconductor device according to claim 10, wherein each of the source electrode and the drain electrode is in contact with an upper surface of the first insulating layer.

12. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is over the source electrode and the drain electrode.

13. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is in contact with each of the side surface of the source electrode and the side surface of the drain electrode.

14. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer further comprises gallium.

15. (Previously Presented) The semiconductor device according to claim 10, wherein the pixel electrode is in contact with the drain electrode.

16. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is a non-single-crystal film.

17. (Previously Presented) The semiconductor device according to claim 10, further comprising:

a first buffer layer between the oxide semiconductor layer and the source electrode; and

a second buffer layer between the oxide semiconductor layer and the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer.

18. (Previously Presented) A semiconductor device comprising:

a glass substrate;

a transistor over the glass substrate, the transistor comprising:

a gate electrode;

a first insulating layer over the gate electrode;

an oxide semiconductor layer over the first insulating layer; and

a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer;

a second insulating layer over the transistor;

a pixel electrode over the second insulating layer;

a third insulating layer over the pixel electrode;

a light-emitting layer over the pixel electrode and the third insulating layer;

an electrode over the light-emitting layer,

wherein the oxide semiconductor layer comprises indium and zinc,

wherein a first angle between a surface of the glass substrate and a side surface of a first bottom edge of the source electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the source electrode, and

wherein a second angle between the surface of the glass substrate and a side surface of a second bottom edge of the drain electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the drain electrode.

19. (Previously Presented) The semiconductor device according to claim 18, wherein each of the source electrode and the drain electrode is in contact with an upper surface of the first insulating layer.

20. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is over the source electrode and the drain electrode.

21. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is in contact with each of the side surface of the source electrode and the side surface of the drain electrode.

22. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer further comprises gallium.

23. (Previously Presented) The semiconductor device according to claim 18, wherein the pixel electrode is in contact with the drain electrode.

24. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is a non-single-crystal film.

25. (Previously Presented) The semiconductor device according to claim 18, further comprising:

a first buffer layer between the oxide semiconductor layer and the source electrode; and

a second buffer layer between the oxide semiconductor layer and the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer.

REMARKS

The Official Action mailed December 20, 2013, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on February 11, 2013 and April 23, 2013.

A further Information Disclosure Statement is submitted herewith and consideration of this Information Disclosure Statement is respectfully requested.

Claims 2-8 and 10-25 were pending in the present application prior to the above amendment. Claims 2-8 have been canceled without prejudice or disclaimer. The Applicant notes with appreciation the allowance of claims 10-25.

Paragraph 1 of the Official Action rejects claims 2-8 as obvious based on the combination of U.S. Publication No. 2007/0108446 to Akimoto, U.S. Publication No. 2005/0056897 to Kawasaki, U.S. Publication No. 2008/0073653 to Iwasaki and U.S. Publication No. 2006/0033098 to Shih. As noted above, claims 2-8 have been canceled without prejudice or disclaimer; therefore, the rejection is moot. Accordingly, claims 10-25 are now pending in the present application, of which claims 10 and 18 are independent and all of which are allowed.

Should the Examiner believe that anything further would be desirable to maintain this application in condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

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Suite 20 North
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Attorney Docket No. 0756-10065

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No.: 7085
Shunpei YAMAZAKI et al.	)	Examiner: Jeremy J. Joy
Serial No. 13/763,874	)	Group Art Unit: 2896
Filed: February 11, 2013	)	
For: SEMICONDUCTOR DEVICE	)	
AND MANUFACTURING	)	
METHOD THEREOF	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(e), it is certified that each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

The references submitted were cited by the Japanese Patent Office in counterpart Japanese Patent Application No. 2009-254181 in an Office Action mailed February 18, 2014.

A payment in the amount of $180 is being submitted to comply with the provisions of 37 C.F.R. § 1.97.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

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PTO/SB/08A (07-06)
Approved for use through 03/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/763,874
Filing Date	February 11, 2013
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2896
Examiner Name	J. JOY
Attorney Docket Number	0756-10065

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP-2008-205451A	09-04-2008			Abst.
		JP-2005-223049A	08-18-2005			Abst.
		JP-07-064112A	03-10-1995			Abst.

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

Espacenet

Bibliographic data: JP2008205451 (A) — 2008-09-04

THIN-FILM TRANSISTOR ARRAY AND METHOD OF MANUFACTURING THE SAME

No documents available for this priority number.

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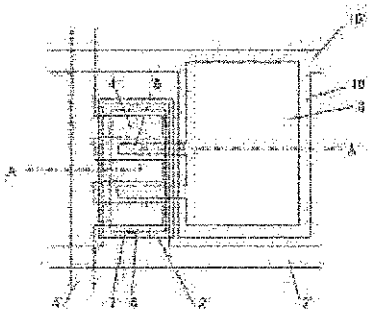
Abstract of JP2008205451 (A)

PROBLEM TO BE SOLVED: To provide a thin-film transistor array in which the electrical resistance increase in the electrodes and difficulty of manufacturing are suppressed, while reducing feedthrough of a thin-film transistor which uses interdigital electrodes. SOLUTION: Source/drain electrodes are made into interdigital shape; width of the drain electrode is made shorter than that of the source electrode; and roots of the drain electrode or of source/drain electrodes are made tapered; thereby the electrical resistance increase is suppressed, and the yield is improved for the thin-film transistor array. ; COPYRIGHT: (C)2008,JPO&INPIT



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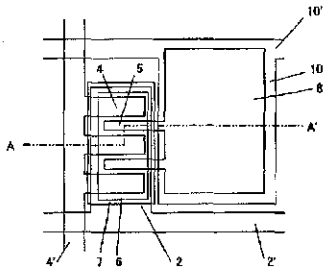
(54)【発明の名称】薄膜トランジスタアレイおよびその製造方法

(57)【要約】
【課題】　本発明は、クシ型電極を用いた薄膜トランジスタのフィードスルーを低減しつつ、電極の電気抵抗の増大や作製の難しさを改善した薄膜トランジスタアレイを提供することを課題とする。
【解決手段】　ソース・ドレイン電極をクシ型とし、ドレイン電極の幅をソース電極の幅より細くし、ドレイン電極あるいはソース・ドレイン電極の根元をテーパー状にすることにより、電気抵抗の増大を抑制し、かつ歩留まりを向上した薄膜トランジスタアレイ。
【選択図】　図1



【特許請求の範囲】
【請求項１】
絶縁基板上に、少なくともゲート配線に接続されたゲート電極と、ゲート絶縁膜と、ソース配線に接続されたソース電極と、画素電極に接続されたドレイン電極と、前記ソース電極と前記ドレイン間に形成された半導体層とを有する薄膜トランジスタをマトリクス状に配置した薄膜トランジスタアレイであって、前記ソース電極と前記ドレイン電極がクシ型であり、且つ前記ドレイン電極の幅が前記ソース電極の幅より小さいことを特徴とする薄膜トランジスタアレイ。
【請求項２】
前記ドレイン電極の前記画素電極との接続部分の形状が、テーパー形状であることを特徴とする請求項１記載の薄膜トランジスタアレイ。
【請求項３】
前記ソース電極の前記ソース配線との接続部分の形状がテーパー形状になっていることを特徴とする請求項１または２に記載の薄膜トランジスタアレイ。
【請求項４】
前記半導体が、有機半導体または酸化物半導体であることを特徴とする請求項１乃至３のいずれかに記載の薄膜トランジスタアレイ。
【請求項５】
請求項１乃至４のいずれかに記載の薄膜トランジスタアレイの製造方法であって、前記ソース電極と前記ドレイン電極を、反転印刷によって形成することを特徴とする薄膜トランジスタアレイの製造方法。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、画像表示装置等に用いる薄膜トランジスタアレイに関する。
【背景技術】
【０００２】
半導体自体を基板としたトランジスタや集積回路技術を基礎として、ガラス基板上にアモルファスシリコン（ａ－Ｓｉ）やポリシリコン（ｐｏｌｙ－Ｓｉ）の薄膜トランジスタ（Ｔｈｉｎ　Ｆｉｌｍ　Ｔｒａｎｓｉｓｔｏｒ：ＴＦＴ）が製造され、液晶ディスプレイに応用されている（非特許文献１）。ＴＦＴとしては、例えば図１０のようなものが用いられている。ここでＴＦＴはスイッチの役割を果たしており、ゲート配線２’に与えられた選択電圧によってＴＦＴをオンにした時に、ソース配線４’に与えられた信号電圧をドレイン５に接続された画素電極８に書き込む。書き込まれた電圧は、画素電極８／ゲート絶縁膜３／キャパシタ電極１０によって構成される蓄積キャパシタに保持される。
【０００３】
ここで、ＴＦＴアレイの場合、ソースとドレインの働きは書き込む電圧の極性によって変わるため、動作で名称を決められない。そこで、便宜的に一方をソース、他方をドレインと、呼び方を統一しておく。本発明では、配線に接続されている方をソース、画素電極に接続されている方をドレインと呼ぶ。
【０００４】
近年、有機半導体や酸化物半導体が登場し、２００℃以下の低温でＴＦＴを作製できることが示され、プラスチック基板を用いたフレキシブルディスプレイへの期待が高まっている。フレキシブルという特長以外に、軽量、壊れにくい、薄型化できるというメリットも期待されている。また、印刷によってＴＦＴを形成することにより、安価で大面積なディスプレイが期待されている。
【０００５】
ところで、ディスプレイを大面積化するには、大面積にパターニングできるだけでなく、ｏｎ電流を大きくする必要がある。チャネル幅をＷ、チャネル長をＬとした時、ｏｎ電流はＷ／Ｌに比例する。大きなｏｎ電流を得たい場合、ソース・ドレイン電極としては、直

線状のクシ歯を交互に配置したクシ型電極がよく用いられる。クシ型は、大きなWと小さなLを有するからである。ここで、通常、クシ型電極は、図９（ａ）のように等しい幅を有する。

【０００６】

しかし、クシ型電極の場合、クシの長さや歯の数が大きいため、ゲート・ドレイン間の電極重なり面積が大きくなって、フィードスルーが大きくなるという問題があった。

【０００７】

ここで、フィードスルーとは、ゲート電位がｏｎからｏｆｆに変わる際に、画素の電位が変化する現象であり、ゲート・ドレイン間のキャパシタンスが原因である。

フィードスルーが大きいと、画素の電位が設計値からずれてしまうため、想定通りの表示ができなくなる。

【０００８】

一方、電極重なり面積を小さくする目的で電極幅を小さくすれば、電極の電気抵抗が大きくなる、電極の作製が難しくなる、という問題があった。

【非特許文献１】松本正一編著：「液晶ディスプレイ技術　－アクティブマトリクスＬＣＤ－」産業図書。

【発明の開示】

【発明が解決しようとする課題】

【０００９】

本発明は、係る従来技術の状況に鑑みてなされたもので、クシ型電極を用いた薄膜トランジスタのフィードスルーを低減しつつ、電極の電気抵抗の増大や作製の難しさを改善した薄膜トランジスタアレイを提供することを課題とする。

【課題を解決するための手段】

【００１０】

上記課題を解決するための、請求項１に記載の発明は、絶縁基板上に、少なくともゲート配線に接続されたゲート電極と、ゲート絶縁膜と、ソース配線に接続されたソース電極と、画素電極に接続されたドレイン電極と、前記ソース電極と前記ドレイン間に形成された半導体層とを有する薄膜トランジスタをマトリクス状に配置した薄膜トランジスタアレイであって、前記ソース電極と前記ドレイン電極がクシ型であり、且つ前記ドレイン電極の幅が前記ソース電極の幅より小さいことを特徴とする薄膜トランジスタアレイである。

【００１１】

請求項２に記載の発明は、前記ドレイン電極の前記画素電極との接続部分の形状が、テーパー形状であることを特徴とする請求項１記載の薄膜トランジスタアレイである。

【００１２】

請求項３に記載の発明は、前記ソース電極の前記ソース配線との接続部分の形状がテーパー形状になっていることを特徴とする請求項１または２に記載の薄膜トランジスタアレイである。

【００１３】

請求項４に記載の発明は、前記半導体が、有機半導体または酸化物半導体であることを特徴とする請求項１乃至３のいずれかに記載の薄膜トランジスタアレイである。

【００１４】

請求項５に記載の発明は、請求項１乃至４のいずれかに記載の薄膜トランジスタアレイの製造方法であって、前記ソース電極と前記ドレイン電極を、反転印刷によって形成することを特徴とする薄膜トランジスタアレイの製造方法である。

【００１５】

請求項１に記載の発明によれば、ソース電極の幅を太く保ちながらドレイン電極の幅を細くすることにより、電気抵抗の増大、作製時の断線の恐れの両方を、ドレイン電極側だけに留めることができる。従って、電気抵抗の増大を低減し、歩留まりを向上させることができる。

【００１６】

請求項２に記載の発明によれば、ドレイン電極の画素電極との接続部分の形状を、テーパー形状にすることにより、ドレイン電極においても作製時の断線の恐れを低減することができる。従って、歩留まりを向上させることができる。

【００１７】

請求項３に記載の発明によれば、ソース電極のソース配線との接続部分の形状を、テーパー形状にすることにより、ソース電極作製時の断線の恐れをより低減することができる。従って、歩留まりを向上させることができる。

【００１８】

請求項４に記載の発明によれば、半導体として有機半導体または酸化物半導体を用いることにより、薄膜トランジスタアレイを２００℃以下の低温で作製することが可能になり、熱に弱いプラスチック基板の使用ができて、フレキシブルディスプレイを作製できる。

【００１９】

請求項５に記載の発明によれば、ソース・ドレイン電極を反転印刷法で形成することにより、高精度のパターニングを簡便かつ高速に行うことができ、性能のよい薄膜トランジスタアレイを容易に製造できる。

【発明の効果】

【００２０】

本発明によれば、まず、ソース・ドレイン電極をクシ型とし、ドレイン電極の幅をソース電極の幅より細くすることにより、ゲート・ドレイン間容量を小さく抑えつつ、電気抵抗の増大を抑制し、かつ歩留まりを向上できた。また、ドレイン電極の画素電極との接続部分の形状をテーパー形状にすること、あるいはソース電極のソース配線との接続部分の形状及びドレイン電極のドレイン配線との接続部分の形状をテーパー形状にすることにより、さらに歩留まりを向上できた。さらには、半導体を、有機半導体または酸化物半導体とすることにより、低温での作製が可能になり、プラスチック基板を使用できた。さらにはソース・ドレイン電極を反転印刷法で形成することにより、高精度の素子を容易に製造できた。

【発明を実施するための最良の形態】

【００２１】

本発明の実施の形態について、以下に図面を使用して詳細に説明する。なお、以下に使用する図面では、説明を判り易くするために縮尺は正確には描かれていない。

【００２２】

本発明の実施形態に係わる薄膜トランジスタアレイの例を、図１に示す。薄膜トランジスタアレイの１画素領域を示す平面配置図を示している。即ち、図１の画素をマトリクス状に並べたものが、本発明の薄膜トランジスタアレイである。　図１に示すように本発明の実施形態に係わる薄膜トランジスタアレイは、ソース電極４・ドレイン電極５がクシ型であり、ドレイン電極５の幅がソース電極４の幅より小さい。そのため、ソース電極４の電気抵抗の増大および歩留りの減少（形成時の断線）を抑えつつ、ゲート電極２・ドレイン電極５の重なり面積を小さくすることができる。

【００２３】

ソース電極４およびドレイン電極５の電気抵抗の目安は、電極幅をそれぞれＬｓ、Ｌｄとし、クシの長さをｗ、厚さｔ、抵抗率ρとすれば、それぞれρｗ／Ｌｓｔ、ρｗ／Ｌｄｔと考えることができる。即ち、電気抵抗は電極幅に反比例する。例えばソース電極４およびドレイン電極５の幅を両方とも半分にすれば電気抵抗は２倍になってしまうが、ドレイン電極５の幅のみを半分にすれば電気抵抗は１．５倍で済む。一方、ドレイン電極５とゲート電極２との重なりは、１／２倍になる。また、ソース電極４は太いので形成が容易であり、ドレイン電極５の歩留り減少（形成時の断線）が懸念事項となるのみである。

【００２４】

さらに改善されたソース電極４・ドレイン電極５の例を、図２に示す。図２（ａ）のようにドレイン電極５の画素電極８との接続部分の形状を、テーパー形状にすることにより、ドレイン電極５の歩留りの減少（形成時の断線）を抑えることができる。また、図２（ｂ

）のようにソース電極４のソース配線４’との接続部分の形状もテーパー形状にしてもよいし、図２（ｃ）のようにテーパー部を曲線にしてもよい。

【００２５】

なお、ソース電極４の歯の数をドレイン電極５の数よりも１本多くしているのも、ゲート電極２・ドレイン電極５の重なり面積を小さくするために有効である。

【００２６】

半導体層６は、ソース電極４・ドレイン電極５が近接している領域に形成され、ゲート絶縁膜３を挟んで、ゲート電極２と重なっている。ゲート電極２の電位によって、半導体層６／ゲート絶縁膜３の界面の電荷を制御し、ドレイン電流を制御できる。素子構造は、ボトムゲートでもよいし、トップゲートでもよい。また、ボトムコンタクトでもよいし、トップコンタクトでもよい。これらについて、図３で説明する。図３は、図１の線Ａ－Ａ’の断面図である。ボトムゲート・ボトムコンタクト（図３（ａ））では、積層順序が、基板１、ゲート電極２、ゲート絶縁膜３、ソース電極４およびドレイン電極５、半導体層６となる。ボトムゲート・トップコンタクト（図３（ｂ））では、積層順序が、基板１、ゲート電極２、ゲート絶縁膜３、半導体層６、ソース電極４およびドレイン電極５となる。トップゲート・ボトムコンタクト（図３（ｃ））では、積層順序が、基板１、ソース電極４およびドレイン電極５、半導体層６、ゲート絶縁膜３、ゲート電極２となる。トップゲート・トップコンタクト（図３（ｄ））では、積層順序が、基板１、半導体層６、ソース電極４およびドレイン電極５、ゲート絶縁膜３、ゲート電極２となる。ゲート電極２と同層にゲート配線２’を、ソース電極４・ドレイン電極５と同層にソース配線４’、画素電極８を有することは、言うまでもない。また、ゲート電極２と同層または別層に、キャパシタ電極１０およびキャパシタ配線１０’を有してもよい。ボトムゲートの場合、半導体層６上に封止層７を有してもよい。

【００２７】

また、さらに層間絶縁膜９および上部画素電極１２を有し、上部画素電極１２が画素電極８と接続されていてもよい。特にトップゲートでは、層間絶縁膜９および上部画素電極１２を有することが望ましい。

【００２８】

ただし、上部画素電極１２は画素電極８に接続されている必要があり、ボトムゲートでは層間絶縁膜９に、トップゲートでは層間絶縁膜９およびゲート絶縁膜３に開口が必要である。

【００２９】

半導体層６としては、有機半導体や、酸化物半導体を用いる。具体的には、ポリチオフェン誘導体、ポリフェニレンビニレン誘導体、ポリチエニレンビニレン誘導体、ポリアリルアミン誘導体、ポリアセチレン誘導体、アセン誘導体、オリゴチオフェン誘導体等の有機半導体や、ＩｎＧａＺｎＯ系、ＺｎＧａＯ系、ＩｎＺｎＯ系、ＩｎＯ系、ＧａＯ系、ＳｎＯ系、あるいはそれらの混合物等の酸化物半導体を用いることができる。有機半導体は、溶液をスピンコート、ダイコート、インクジェット等で塗布・焼成することにより、酸化物半導体は、スパッタ、蒸着、レーザアブレーション等により、２００℃以下の低温で成膜できる。

【００３０】

また、有機半導体は、溶液をフレキソ印刷で塗布・焼成することによっても、２００℃以下の低温で成膜できる。

【００３１】

そのため、絶縁基板１としてプラスチックを使用することが可能になる。具体的には、ポリエチレンテレフタレート（ＰＥＴ）、ポリエチレンナフタレート（ＰＥＮ）、ポリエーテルスルフォン（ＰＥＳ）、ポリイミド（ＰＩ）、ポリエーテルイミド（ＰＥＩ）、ポリスチレン（ＰＳ）、ポリ塩化ビニル（ＰＶＣ）、ポリエチレン（ＰＥ）、ポリプロピレン（ＰＰ）、ナイロン（Ｎｙ）等が使用できる。

【００３２】

なお、半導体層６は全面形成でも動作可能だが、図１や図５～８のようにパターニングされている方が、オフ電流を小さくできて好ましい。スピンコート、ダイコート、スパッタ、蒸着、レーザアブレーション等で全面成膜後に、フォトリソグラフィ、あるいはそれに類する方法を用いてパターニングするか、成膜とパターニングを同時に行うことができる印刷、マスク蒸着等を用いるか、あらかじめレジストパターンを形成しておき、全面成膜後にレジストを除去するリフトオフ法を用いることができる。あるいは有機半導体の場合、後述する封止層７を形成後、封止層７をマスクとして、O_2プラズマ、N_2プラズマ、Ａｒプラズマ等によるエッチングを行うか、封止層７を溶解せず半導体層６を溶解する液体でリンスする等の方法によっても、パターニングが可能である。

【００３３】

ゲート電極２、キャパシタ電極１０としては、Ａｌ、Ｃｒ、Ａｕ、Ａｇ、Ｎｉ、Ｃｕ、Ｍｏ等の金属や、ＩＴＯ等の透明導電膜を使用することができる。製法としては、蒸着やスパッタ成膜後にフォトリソ＋エッチングで形成する方法が一般的であるが、印刷法（スクリーン印刷、フレキソ印刷、グラビア印刷、オフセット印刷、反転印刷等）を用いることができる。印刷を用いる場合、Ａｇインク、Ｎｉインク、Ｃｕインク等を用いることができる。

【００３４】

ゲート絶縁膜３としては、ポリビニルフェノール、エポキシ、ポリイミド等の有機絶縁膜や、SiO_2、ＳｉＮ、ＳｉＯＮ、Al_2O_3等の無機絶縁膜を用いることができる。製法としては、溶媒可溶性有機物の場合にはスピンコート、ダイコート、インクジェット等を、それ以外の場合にはスパッタ、蒸着、レーザアブレーション等を用いることができる。

【００３５】

例えば、トップゲートのようにパターニングが必要な場合、フォトリソグラフィとエッチング、リフトオフ等でパターニングするか、インクジェット等の印刷法や、感光性有機物をゲート絶縁膜３の材料とし露光・現像するなどして、直接パターニングすることが可能である。

【００３６】

ソース電極４、ソース配線４’、ドレイン電極５、画素電極８としては、ゲート電極２等と同様の材料と同様の方法が使用できるが、特に反転印刷が最適である。

【００３７】

封止層７としては、フッ素化樹脂が好適である。製法としては、スクリーン印刷が好適である。層間絶縁膜９としては、ポリビニルフェノール、アクリル、エポキシ、ポリイミド等が使用可能である。製法としては、スクリーン印刷が好適であるが、感光性膜を形成後、露光・現像によって形成してもよい。上部画素電極１２としては、Ａｌ、Ｃｒ、Ａｕ、Ａｇ、Ｎｉ、Ｃｕ等の金属や、ＩＴＯ等の透明導電膜等を用いることができる。製法としては、蒸着、スパッタ等の成膜後にフォトリソ、エッチングする等の方法も可能であるが、Ａｇインク、Ｎｉインク、Ｃｕインク等をスクリーン印刷するのが好適である。

【００３８】

次に、本発明の薄膜トランジスタの製造方法の特徴である、反転印刷について説明する。図４に、反転印刷の概略を示す。

【００３９】

反転印刷は、インク剥離性を有するブランケット２１上へインク液膜２３を形成する工程と、該インク液膜２３に凸版２４を接触させて凸部形状のインクを除去する工程と、前記ブランケット２１上に残ったインクを基材２５に接触することにより基材２５上に画像パターンを転写する工程とを有する印刷方法である。通常、ブランケット２１にはシリコーン樹脂を表面に有する円筒（転写胴）が用いられ、凸版２４にはガラスに画像パターンのネガ形状の凸部を残したものが用いられる。

【００４０】

使用するインクとしては、平均粒子径が５０ｎｍ以下の金属粒子と、水性溶媒と、水溶性

樹脂を含む導電性インクが望ましい。金属としてはＡｇが好適である。印刷後に焼成することにより、低抵抗の電極が得られる。

【００４１】

図５及び図６は、図１の薄膜トランジスタの製造方法の一例である。絶縁基板１上にゲート電極２およびキャパシタ電極１０を形成し（図５（ａ））、全面にゲート絶縁膜３を形成する（図５（ｂ））。さらに、ソース電極４、ソース配線４’、ドレイン電極５、画素電極８を上記反転印刷によって形成し（図５（ｃ））、半導体層６を形成する（図５（ｄ））。

【００４２】

以上は、ボトムゲート・ボトムコンタクトの場合の手順であるが、ボトムゲート・トップトンタクトや、トップゲート・ボトムコンタクト、トップゲート・トップコンタクトの場合には、層順を入れ替えればよい。

【００４３】

例えば、図７および図８はボトムゲート・トップコンタクトの場合であり、ソース電極４、ソース配線４’、ドレイン電極５、画素電極８を形成する工程と、半導体層６を形成する工程とを入れ替えている。

【００４４】

また、さらに封止層７（図６（ｅ））、層間絶縁膜９（図６（ｆ））、上部画素電極１２（図６（ｇ））を形成してもよいことも、既に述べた。

【実施例】

【００４５】

（実施例１）

本発明の実施例について、図１および図５、図６を用いて説明する。図１に示す素子を、図５（ａ）～図６（ｇ）の工程によって作製した。まず初めに、絶縁基板１であるＰＥＮ上に、蒸着によってＡｌを５０ｎｍ成膜し、フォトリソおよびウェットエッチによってゲート電極２、キャパシタ電極１０を形成した（図５（ａ））。次に、ポリビニルフェノール溶液をスピンコートし、１５０℃焼成することにより、ゲート絶縁膜３としてポリビニルフェノールを１μｍ形成した（図５（ｂ））。さらに、ソース電極４、ソース配線４’、ドレイン電極５、画素電極８として、Ａｇインクを反転印刷し１８０℃で焼成することによって厚さ５０ｎｍのパターンを形成した（図５（ｃ））。その時のソース電極４・ドレイン電極５の形状は、図１のようであり、ドレイン電極幅は５μｍ、ソース電極幅は１０μｍ、チャネル長は５μｍ、チャネル幅は８００μｍである。顕微鏡観察によれば、ソース電極の歩留りは９０％、ドレイン電極の歩留りは６０％であった。

【００４６】

ここで、歩留まりとは、電極のクシの本数のうち、長さが設計値の９０％以上のクシの割合である。

【００４７】

さらに、ポリチオフェン溶液をスピンコート、１００℃焼成することにより、半導体層６を形成した（図５（ｄ））。

【００４８】

ただし、半導体層６は未パターニングである。

【００４９】

そして、フッ素化樹脂であるサイトップをスクリーン印刷して封止層７を形成した（図６（ｅ））。

【００５０】

その後、キシレンでリンスすることよって封止層下以外の半導体層を除去した（図６（ｅ））。

【００５１】

さらにエポキシ樹脂をスクリーン印刷して層間絶縁膜９を形成し（図６（ｆ））、Ａｇペーストをスクリーン印刷して上部画素電極１２を形成した（図６（ｇ））。

【００５２】
こうして作製した薄膜トランジスタアレイと、対向電極付き基板の間に電気泳動表示体を挟んだ構造の電気泳動ディスプレイを作製した。ドレイン電極欠損分のばらつきはあるものの、ほぼ想定通りに動作することを確認した。
【００５３】
詳しくは、電気泳動表示体の特性およびトランジスタの特性から計算される所定の書き込み動作（所定のソース電圧、ゲート電圧、ゲートパルス幅、書き込み周期、書き込み回数）を行ったところ、無欠陥の画素部分はほぼ想定通りの書き込み回数で動作することを確認した。
【００５４】
以下の実施例においても「想定通りの動作」とは所定の書き込み条件下、想定通りの書き込み回数で動作したという意味である。
【００５５】
（実施例２）
ソース電極４・ドレイン電極５の形状が図２（ａ）である以外は、実施例１と同様の薄膜トランジスタアレイを作製した。具体的には、ドレイン電極の画素電極と接している幅は２５μｍであり、この接している部分から２０μｍ以上離れた部分で幅が一定（５μｍ）となるテーパー形状である。顕微鏡観察によれば、ソース電極の歩留りは９０％、ドレイン電極の歩留りも９０％になった。
【００５６】
（実施例３）
ソース電極４・ドレイン電極５の形状が図２（ｂ）である以外は、実施例１と同様の薄膜トランジスタアレイを作製した。具体的には、ソース電極のソース配線と接している部分の幅は２０μｍであり、この接している部分から５μｍ以上離れた部分で幅が一定（１０μｍ）となるテーパー形状である。顕微鏡観察によれば、ソース電極の歩留りは９５％、ドレイン電極の歩留りは９０％になった。
【００５７】
（実施例４）
ソース電極４・ドレイン電極５の形状が図２（ｃ）である以外は、実施例１と同様の薄膜トランジスタアレイを作製した。具体的には、ドレイン電極の画素電極と接している部分は半径１０μｍの円弧、ソース電極のソース配線と接している部分は半径７．５μｍの円弧で丸めたテーパー形状である。顕微鏡観察によれば、ソース電極の歩留りは９５％、ドレイン電極の歩留りは９０％になった。
【００５８】
（実施例５）
本発明の実施例について、図１および図７、図８を用いて説明する。図１に示す素子（ただし、ドレイン電極形状は図２（ａ））を、図７（ａ）～図８（ｇ）の工程によって作製した。まず初めに、絶縁基板１であるＰＥＮ上に、蒸着によってＡｌを５０ｎｍ成膜し、フォトリソおよびウェットエッチによってゲート電極２、キャパシタ電極１０を形成した（図７（ａ））。次に、ＳｉＮをターゲットとし、Ａｒ、O_2、N_2を流してＲＦスパッタを行うことにより、ゲート絶縁膜３としてＳｉＯＮを５００ｎｍ形成した（図７（ｂ））。さらに、$InGaZnO_4$をターゲットとし、Ａｒ、O_2を流してＲＦスパッタを行うことにより、半導体層６としてＩｎＧａＺｎＯを５０ｎｍ成膜し、フォトリソおよび塩酸によるウェットエッチによりパターニングした（図７（ｃ））。さらに、ソース電極４、ソース配線４’、ドレイン電極５、画素電極８として、Ａｇインクを反転印刷し１８０℃で焼成することによって厚さ５０ｎｍのパターンを形成した（図７（ｄ））。その時のソース電極４・ドレイン電極５の形状は、図２（ａ）のようであり、ドレイン電極幅は５μｍ、ソース電極幅は１０μｍ、チャネル長は５μｍ、チャネル幅は８００μｍである。
【００５９】
また、ドレイン電極の画素電極と接している幅は２５μｍであり、この接している部分か

ら２０μｍ以上離れた部分で幅が一定（５μｍ）となるテーパー形状である。
【００６０】
顕微鏡観察によれば、ソース電極の歩留りは９０％、ドレイン電極の歩留りも９０％であった。
【００６１】
そして、フッ素化樹脂であるサイトップをスクリーン印刷して封止層７を形成した（図８（ｅ））。さらにエポキシ樹脂をスクリーン印刷して層間絶縁膜９を形成し（図８（ｆ））、Ａｇペーストをスクリーン印刷して上部画素電極１２を形成した（図８（ｇ））。
【００６２】
こうして作製した薄膜トランジスタアレイと、対向電極付き基板の間に電気泳動表示体を挟んだ構造の電気泳動ディスプレイを作製し、ほぼ想定通りに動作することを確認した。
【００６３】
（実施例６）
本発明の実施例について、図１および図５、図６を用いて説明する。図１に示す素子（ただし、ドレイン電極形状は図２（ａ））を、図５（ａ）～図６（ｇ）の工程によって作製した。まず初めに、絶縁基板１であるＰＥＮ上に、蒸着によってＡｌを５０ｎｍ成膜し、フォトリソおよびウェットエッチによってゲート電極２、キャパシタ電極１０を形成した（図５（ａ））。次に、ポリビニルフェノール溶液をスピンコートし、１５０℃焼成することにより、ゲート絶縁膜３としてポリビニルフェノールを１μｍ形成した（図５（ｂ））。さらに、ソース電極４、ソース配線４’、ドレイン電極５、画素電極８として、Ａｇインクを反転印刷し１８０℃で焼成することによって厚さ５０ｎｍのパターンを形成した（図５（ｃ））。その時のソース電極４・ドレイン電極５の形状は、図２（ａ）のようであり、ドレイン電極幅は５μｍ、ソース電極幅は１０μｍ、チャネル長は５μｍ、チャネル幅は８００μｍ、ドレイン電極の画素電極と接している幅は２５μｍであり、この接している部分から２０μｍ以上離れた部分で幅が一定（５μｍ）となるテーパー形状である。顕微鏡観察によれば、ソース電極の歩留りは９０％、ドレイン電極の歩留りも９０％であった。
【００６４】
さらに、ポリチオフェン溶液をフレキソ印刷、１００℃焼成することにより、半導体層６を形成した（図５（ｄ））。そして、フッ素化樹脂であるサイトップをスクリーン印刷して封止層７を形成した（図６（ｅ））。さらにエポキシ樹脂をスクリーン印刷して層間絶縁膜９を形成し（図６（ｆ））、Ａｇペーストをスクリーン印刷して上部画素電極１２を形成した（図６（ｇ））。
【００６５】
こうして作製した薄膜トランジスタアレイと、対向電極付き基板の間に電気泳動表示体を挟んだ構造の電気泳動ディスプレイを作製し、ほぼ想定通りに動作することを確認した。
【００６６】
（比較例１）
ソース電極４・ドレイン電極５の形状が図９（ａ）である以外は、実施例１と同様の薄膜トランジスタアレイを作製した。具体的には、ドレイン電極幅は５μｍ、ソース電極幅も５μｍ、チャネル長は５μｍ、チャネル幅は８００μｍである。顕微鏡観察によれば、例えば、図９（ｂ）のように一部の電極に欠損が見られ、ソース電極の歩留りは６０％、ドレイン電極の歩留りも６０％であった。図９（ｂ）では、ソース電極３本のうち1本が欠損し、ドレイン電極２本のうち1本が欠損している。
【００６７】
（比較例２）
ソース電極４・ドレイン電極５の形状が図９（ａ）である以外は、実施例１と同様の薄膜トランジスタアレイを作製した。具体的には、ドレイン電極幅は１０μｍ、ソース電極幅も１０μｍ、チャネル長は１０μｍ、チャネル幅は１６００μｍである。顕微鏡観察によれば、ソース電極の歩留りは９０％、ドレイン電極の歩留りも９０％であった。

【００６８】
こうして作製した薄膜トランジスタアレイと、対向電極付き基板の間に電気泳動表示体を挟んだ構造の電気泳動ディスプレイを作製したところ、フィードスルーが大きいため、想定の１０倍の回数の書込みを行わないと表示できなかった。

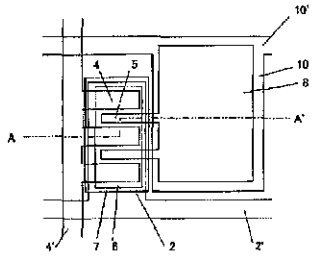
【図面の簡単な説明】

【００６９】
【図１】本発明の薄膜トランジスタアレイの一例を示す平面図である。
【図２】本発明の薄膜トランジスタアレイのソース・ドレイン電極形状の他の例を示す平面図である。
【図３】図１の薄膜トランジスタアレイの積層構造の例を示す断面図である。
【図４】反転印刷法を示す説明図である。
【図５】本発明の薄膜トランジスタの製造工程の一例を示す断面図および平面図である。
【図６】本発明の薄膜トランジスタの製造工程の一例を示す断面図および平面図である。
【図７】本発明の薄膜トランジスタの製造工程の別の一例を示す断面図および平面図である。
【図８】本発明の薄膜トランジスタの製造工程の別の一例を示す断面図および平面図である。
【図９】従来のクシ型電極を有する薄膜トランジスタアレイのソース・ドレイン電極形状を示す平面図である。
【図１０】従来の薄膜トランジスタアレイの構造を示す平面図である。

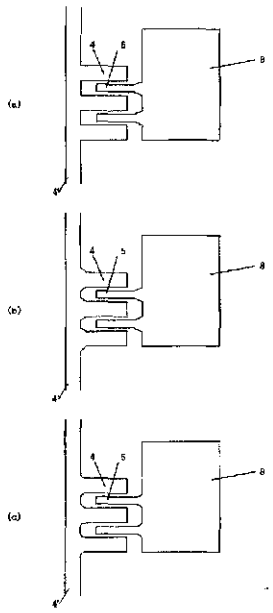
【符号の説明】

【００７０】
１　…　絶縁基板
２　…　ゲート電極
２’　…　ゲート配線
３　…　ゲート絶縁膜
４　…　ソース電極
４’　…　ソース配線
５　…　ドレイン電極
６　…　半導体層
７　…　封止層
８　…　画素電極
９　…　層間絶縁膜
１０　…　キャパシタ電極
１０’　…　キャパシタ配線
１２　…　上部画素電極
２１　…　ブランケット
２２　…　インク塗布機構
２３　…　インク液膜
２４　…　凸版（除去版）
２５　…　基材
２６　…　ステージ

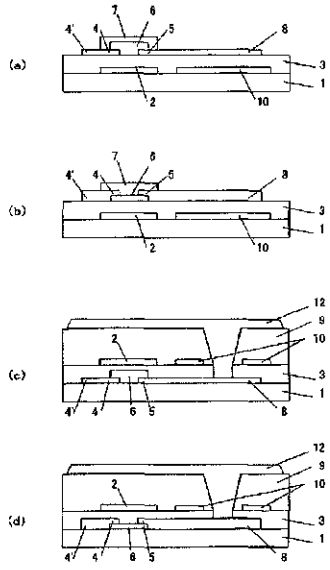
【図１】



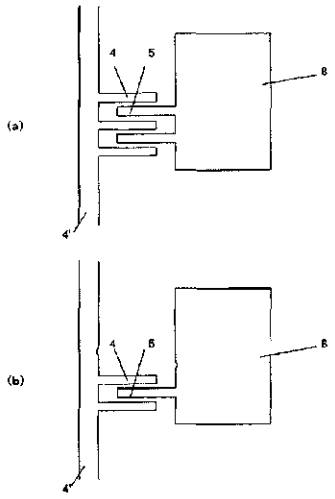
【図２】



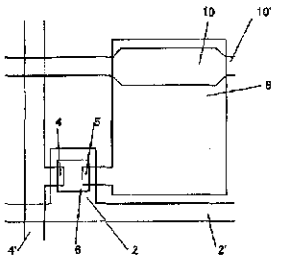
【図３】



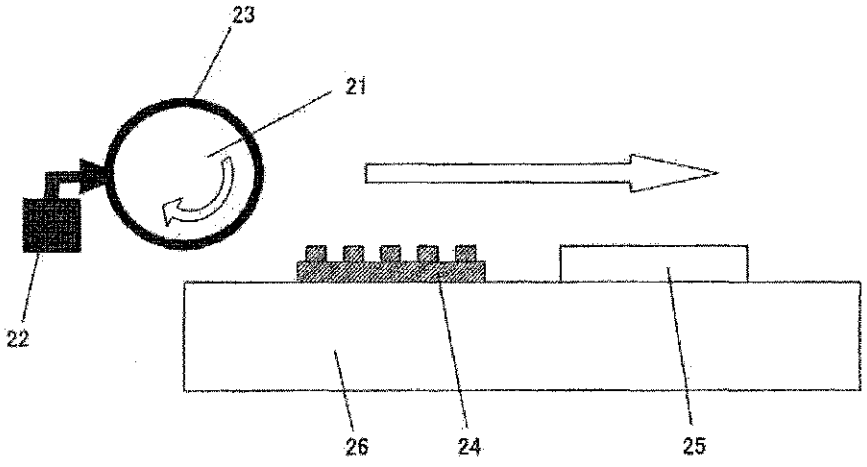
【図９】



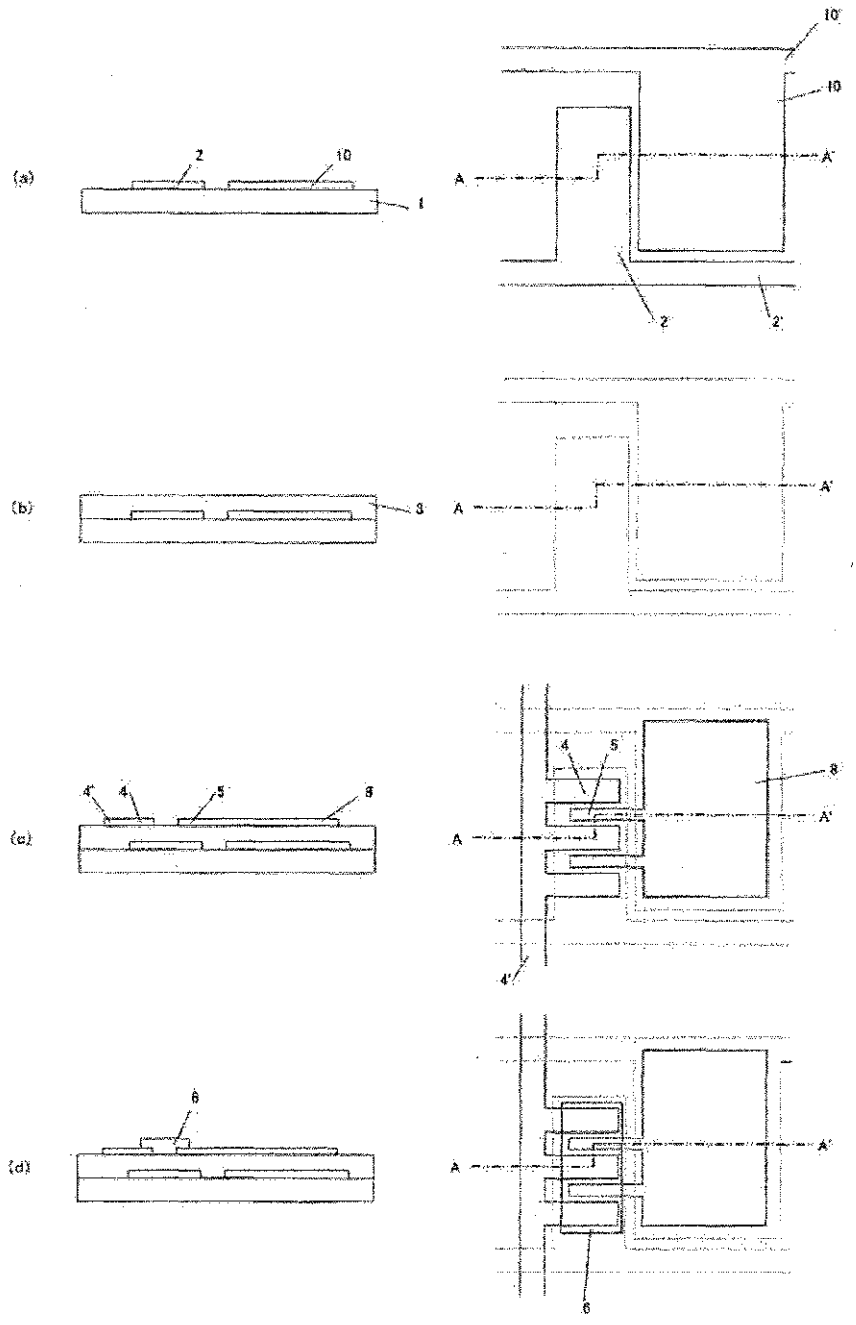
【図１０】



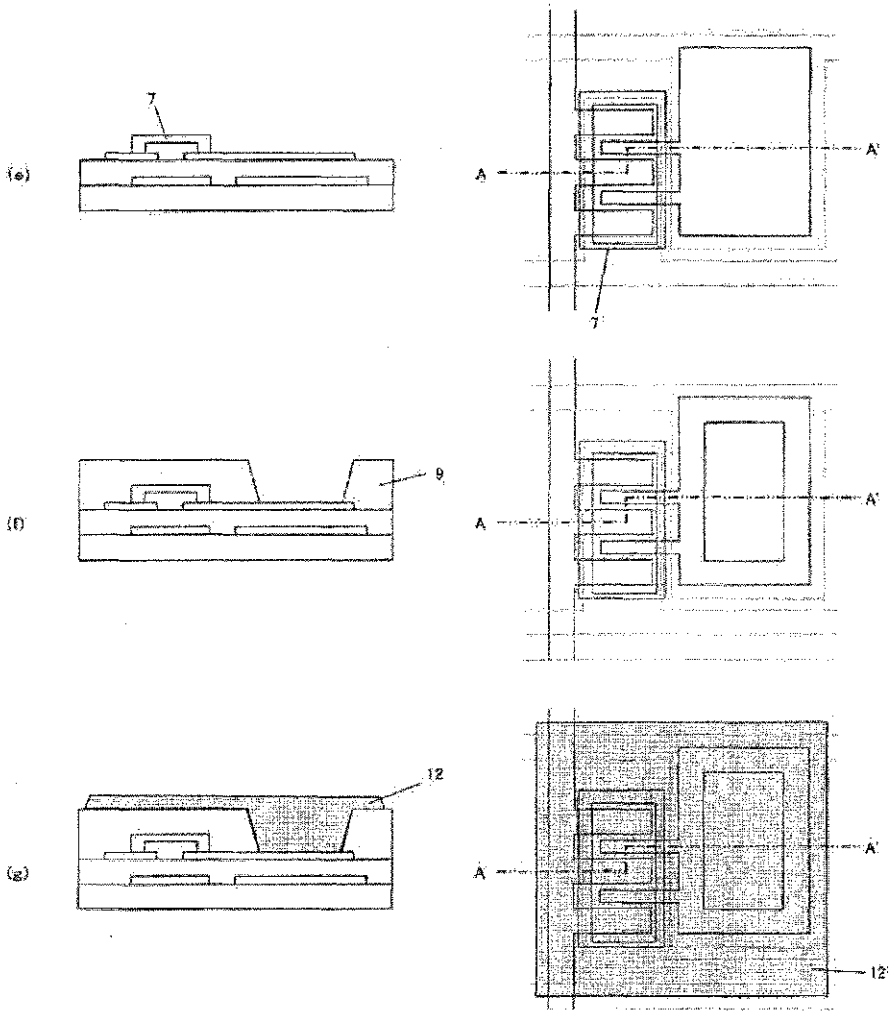
【図４】



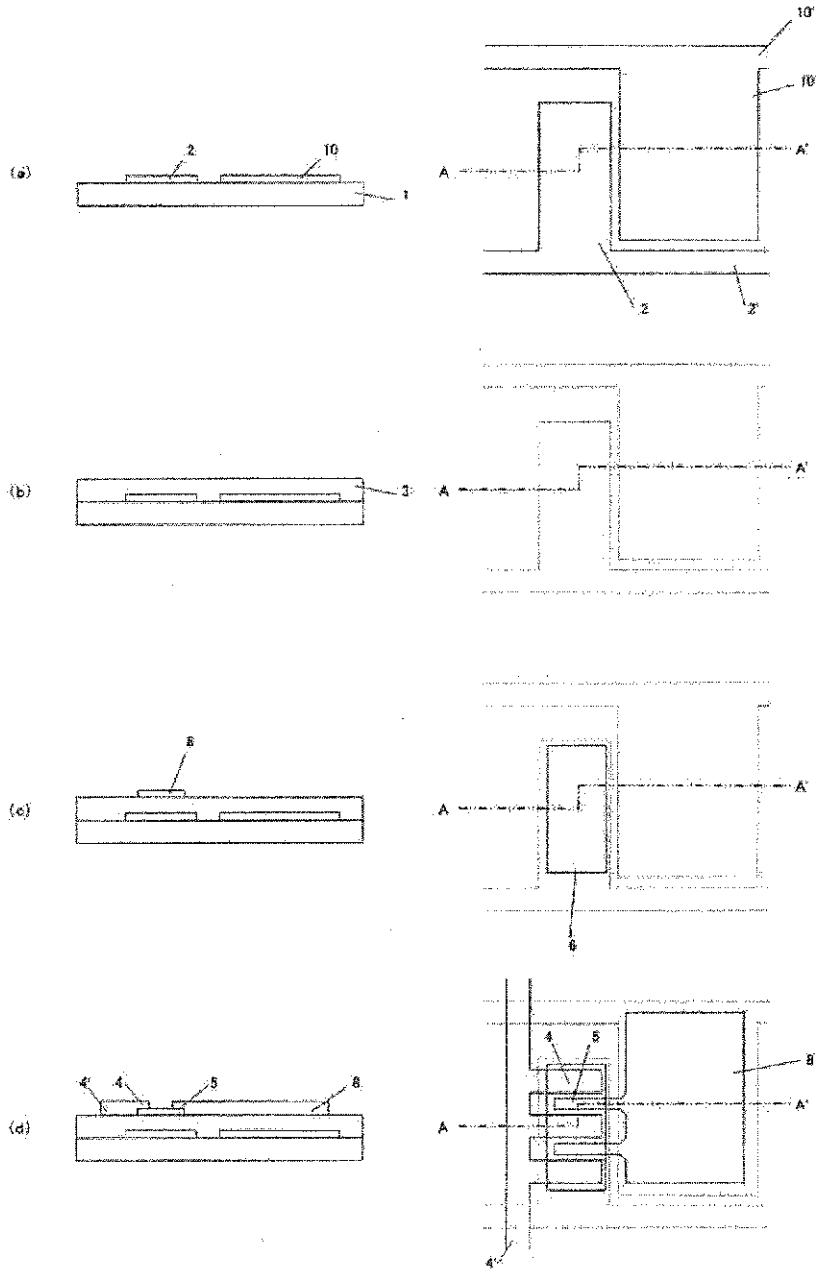
【図５】



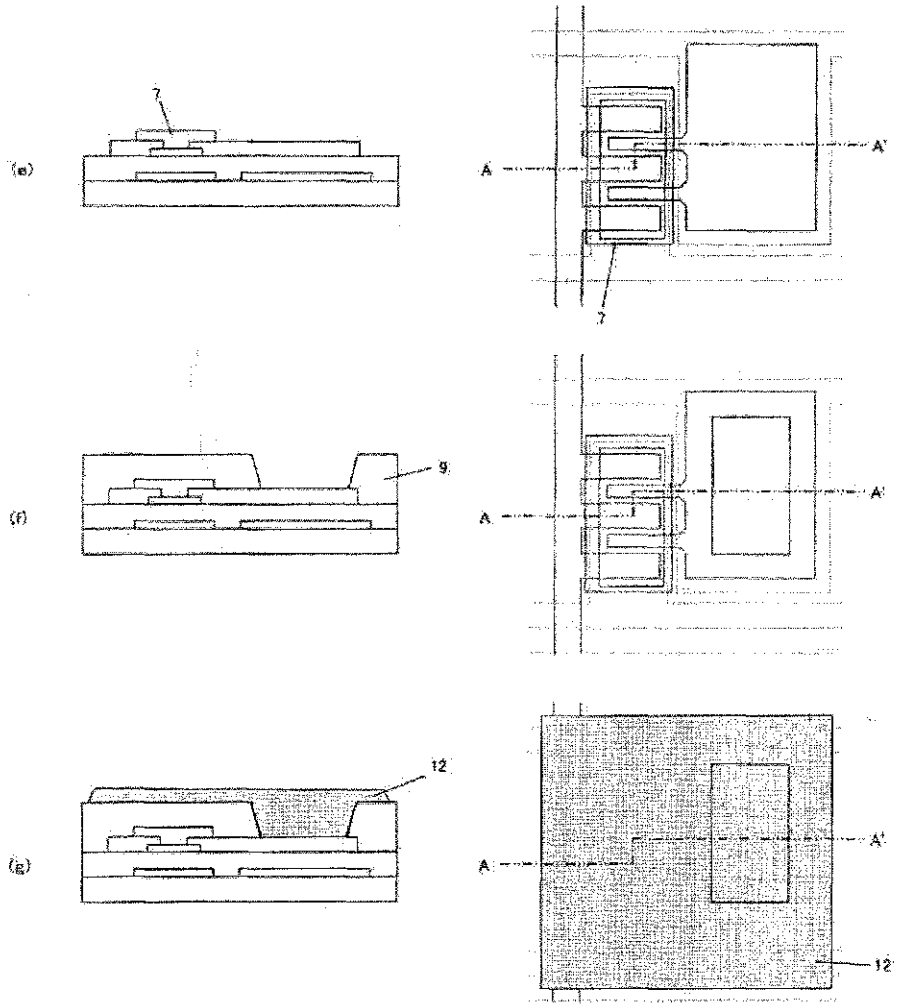
【図６】



【図７】



【図８】



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SEMICONDUCTOR DEVICE, ITS FABRICATION PROCESS, AND DISPLAY

No documents available for this priority number.

Inventor(s): TANO TAKANORI; TOMONO HIDENORI; KONDO HITOSHI ± (TANO TAKANORI, ; TOMONO HIDENORI, ; KONDO HITOSHI)

Applicant(s): RICOH KK ± (RICOH CO LTD)

Classification: - **international:** ***G02F1/1368; H01L29/417; H01L29/786; H01L51/00; H01L51/05;*** (IPC1-7): G02F1/1368; H01L29/417; H01L29/786; H01L51/00

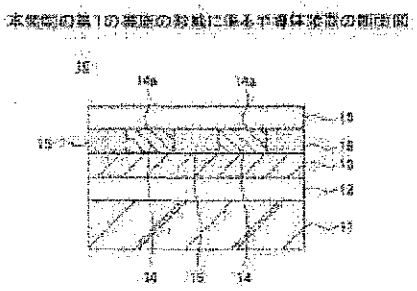
- **cooperative:**

Application number: JP20040027902 20040204

Priority number (s): JP20040027902 20040204

Abstract of JP2005223049 (A)

PROBLEM TO BE SOLVED: To enhance the on/off ratio of a semiconductor device having an organic semiconductor layer by suppressing a drain off current. ; SOLUTION: The semiconductor device 10 comprises an insulating substrate 11, a gate electrode 12 and a gate insulating film 13 formed sequentially on the insulating substrate 11, two source-drain electrodes 14 arranged on the gate insulating film 13 while spaced apart by a predetermined distance, a semiconductor layer 15 covering the surface of the gate insulating film 13 and filling the gap of the source-drain electrodes 14, and an insulating film 16 covering the source-drain electrodes 14 and the surface of the semiconductor layer 15 wherein the insulating film 16 touches the surface of the source-drain electrodes 14. A drain off current is prevented from flowing from the insulating film 16 side surface of one source-drain electrode 14 to the other source-drain electrode 14 through the semiconductor layer 15. The two source-drain electrodes are sandwiched by the insulating substrate and the gate insulating film even in an inverse stagger structure. ; COPYRIGHT: (C)2005,JPO&NCIPI



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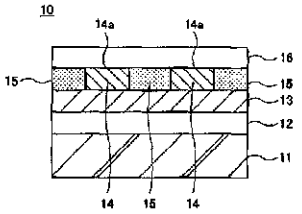
最終頁に続く

(54)【発明の名称】半導体装置、半導体装置の製造方法、および表示装置

(57)【要約】
【課題】　有機半導体層を備えた半導体装置のドレイン・オフ電流を抑制し、オン／オフ比の向上を図る。
【解決手段】　半導体装置１０は、絶縁性基板１１と、絶縁性基板１１上にゲート電極１２と、ゲート絶縁膜１３とが順次形成され、ゲート絶縁膜１３上に所定の距離を有して離隔して配置された２つのソース／ドレイン電極１４と、ゲート絶縁膜１３表面を覆うと共にソース／ドレイン電極１４間を充填する半導体層１５と、ソース／ドレイン電極１４および半導体層１５の表面を覆う絶縁膜１６から構成され、絶縁膜１６がソース／ドレイン電極１４の表面に接する構成とする。一方のソース／ドレイン電極１４の絶縁膜１６側表面から半導体層１４を介して他方のソース／ドレイン電極１４にドレイン・オフ電流が流れることを防止する。逆スタガー型構造においてもソース／ドレイン電極を絶縁性基板とゲート絶縁膜とで挟む構成とする。
【選択図】　図２

本発明の第1の実施の形態に係る半導体装置の断面図



【特許請求の範囲】
【請求項１】
絶縁性基板と、
前記絶縁性基板上に形成されたゲート電極と、
前記ゲート電極を覆うゲート絶縁膜と、
前記ゲート絶縁膜の表面に、所定の間隙を有して配置された第１のソース／ドレイン電極および第２のソース／ドレイン電極と、該第１のソース／ドレイン電極と第２のソース／ドレイン電極との間に充填された有機物からなる半導体層と、を備えた半導体装置であって、
前記第１のソース／ドレイン電極および第２のソース／ドレイン電極の表面が前記半導体層から露出して形成されてなることを特徴とする半導体装置。
【請求項２】
前記第１のソース／ドレイン電極および第２のソース／ドレイン電極と半導体層を覆う絶縁膜を更に備え、
前記絶縁膜が第１のソース／ドレイン電極および第２のソース／ドレイン電極と接して形成されてなることを特徴とする請求項１記載の半導体装置。
【請求項３】
絶縁性基板と、
前記絶縁性基板の表面に、所定の間隙を有して配置された第１のソース／ドレイン電極および第２のソース／ドレイン電極と、該第１のソース／ドレイン電極と第２のソース／ドレイン電極との間に充填された有機物からなる半導体層と、
前記第１のソース／ドレイン電極および第２のソース／ドレイン電極と半導体層を覆うゲート絶縁膜と、
前記ゲート絶縁膜上に形成されたゲート電極と、を備えた半導体装置。
【請求項４】
前記第１のソース／ドレイン電極および第２のソース／ドレイン電極は、互いに対向する各々の面がテーパー形状あるいは曲面形状を有することを特徴とする請求項１～３のうち、いずれか一項記載の半導体装置。
【請求項５】
前記第１のソース／ドレイン電極および第２のソース／ドレイン電極は互いに仕事関数が異なる材料よりなることを特徴とする請求項１～４のうち、いずれか一項記載の半導体装置。
【請求項６】
前記第１のソース／ドレイン電極および／または第２のソース／ドレイン電極は導電性有機材料よりなることを特徴とする請求項１～５のうち、いずれか一項記載の半導体装置。
【請求項７】
前記半導体層はキャリア密度の異なる有機半導体材料を混合してなることを特徴とする請求項１～６のうち、いずれか一項記載の半導体装置。
【請求項８】
画像素子部と、
請求項１～７のうちいずれか一項記載の半導体装置が配置されなり、前記半導体装置を選択的にオンあるいはオフさせて、前記素子部に電界を印加し、あるいは前記素子部にキャリアを注入して画像素子部の光学的性質を制御する画像素子部駆動手段と、を備える表示装置。
【請求項９】
絶縁性基板上にゲート電極を形成する工程と、
前記ゲート電極を覆うゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜上に有機物からなる半導体層を形成する工程と、
前記半導体層を選択的に研削しゲート絶縁膜を露出する溝を形成する工程と、

前記半導体層を覆うと共に溝を充填するソース／ドレイン電極層を形成する工程と、
前記半導体層表面のソース／ドレイン電極層を除去しソース／ドレイン電極を形成する工程と、を備えた半導体装置の製造方法。
【請求項１０】
絶縁性基板上にゲート電極を形成する工程と、
前記ゲート電極を覆うゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜上に有機物からなる半導体層を形成する工程と、
前記半導体層表面にレジスト膜を形成し、該レジスト膜を選択的に除去する工程と、
前記レジスト膜をマスクとして半導体層を選択的に研削しゲート絶縁膜表面を露出する溝を形成する工程と、
前記レジスト膜を覆うと共に溝を充填するソース／ドレイン電極層を形成する工程と、
前記レジスト膜をリフトオフ法により半導体層表面を露出してソース／ドレイン電極を形成する工程と、を備えた半導体装置の製造方法。
【請求項１１】
絶縁性基板上にゲート電極を形成する工程と、
前記ゲート電極を覆うゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜上にソース／ドレイン電極層を形成する工程と、
前記ソース／ドレイン電極層を選択的に研削しソース／ドレイン電極およびゲート絶縁膜を露出する溝を形成する工程と、
前記ソース／ドレイン電極を覆うと共に溝を充填する有機物からなる半導体層を形成する工程と、
前記ソース／ドレイン電極表面の半導体層を除去する工程と、を備えた半導体装置の製造方法。
【請求項１２】
絶縁性基板上にゲート電極を形成する工程と、
前記ゲート電極を覆うゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜上にソース／ドレイン電極層を形成する工程と、
前記ソース／ドレイン電極層表面にレジスト膜を形成し、該レジスト膜を選択的に除去する工程と、
前記レジスト膜をマスクとしてソース／ドレイン電極層を選択的に研削しソース／ドレイン電極およびゲート絶縁膜表面を露出する溝を形成する工程と、
前記レジスト膜を覆うと共に溝を充填する有機物からなる半導体層を形成する工程と、
前記レジスト膜をリフトオフ法によりソース／ドレイン電極表面を露出する工程と、を備えた半導体装置の製造方法。
【請求項１３】
絶縁性基板上に有機物からなる半導体層を形成する工程と、
前記半導体層を選択的に研削し絶縁性基板表面を露出する溝を形成する工程と、
前記半導体層を覆うと共に溝を充填するソース／ドレイン電極層を形成する工程と、
前記半導体層表面のソース／ドレイン電極層を除去しソース／ドレイン電極を形成する工程と、
前記半導体層とソース／ドレイン電極を覆うゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜表面に選択的にゲート電極を形成する工程と、を備えた半導体装置の製造方法。
【請求項１４】
絶縁性基板上に有機物からなる半導体層を形成する工程と、
前記半導体層表面にレジスト膜を形成し、該レジスト膜を選択的に除去する工程と、
前記レジスト膜をマスクとして半導体層を選択的に研削し絶縁性基板表面を露出する溝を形成する工程と、
前記レジスト膜を覆うと共に溝を充填するソース／ドレイン電極層を形成する工程と、
前記レジスト膜をリフトオフ法により半導体層表面を露出してソース／ドレイン電極を

形成する工程と、
前記半導体層とソース／ドレイン電極を覆うゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜表面に選択的にゲート電極を形成する工程と、を備えた半導体装置の製造方法。
【請求項１５】
絶縁性基板上にソース／ドレイン電極層を形成する工程と、
前記ソース／ドレイン電極層を選択的に研削しソース／ドレイン電極および絶縁性基板表面を露出する溝を形成する工程と、
前記ソース／ドレイン電極を覆うと共に溝を充填する有機物からなる半導体層を形成する工程と、
前記ソース／ドレイン電極表面の半導体層を除去する工程と、
前記ソース／ドレイン電極と半導体層を覆うゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜表面に選択的にゲート電極を形成する工程と、を備えた半導体装置の製造方法。
【請求項１６】
絶縁性基板上にソース／ドレイン電極層を形成する工程と、
前記ソース／ドレイン電極層表面にレジスト膜を形成し、該レジスト膜を選択的に除去する工程と、
前記レジスト膜をマスクとしてソース／ドレイン電極層を選択的に研削しソース／ドレイン電極および絶縁性基板表面を露出する溝を形成する工程と、
前記レジスト膜を覆うと共に溝を充填する有機物からなる半導体層を形成する工程と、
前記レジスト膜をリフトオフ法によりソース／ドレイン電極表面を露出する工程と、
前記ソース／ドレイン電極と半導体層を覆うゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜表面に選択的にゲート電極を形成する工程と、を備えた半導体装置の製造方法。
【請求項１７】
前記ソース／ドレイン電極層を形成する工程は、導電性微粒子材料あるいは導電性有機材料を溶媒中に分散あるいは溶解し、塗布法により行うことを特徴とする請求項９～１６のうち、いずれか一項記載の半導体装置の製造方法。
【請求項１８】
前記半導体層を形成する工程は、有機低分子、有機高分子、あるいは有機オリゴマーからなる有機半導体材料を塗布法により行うことを特徴とする請求項９～１７のうち、いずれか一項記載の半導体装置の製造方法。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、有機物からなる半導体層を備えた半導体装置、半導体装置の製造方法、および表示装置に関する。
【背景技術】
【０００２】
近年、有機半導体材料をチャネル生成層とした有機トランジスタを印刷法などの廉価なプロセスにより基板上に形成し、これを用いた軽量・柔軟・薄型かつ廉価な電子装置を実現しようとする研究が活発化している。例えば、デュルリらは、この試みとしてポリマーフィルム上に、ゲート絶縁膜、半導体層、電極の全てに有機材料を用いた有機トランジスタを作製している（C. J. Drury, C. M. J. Mutsaers, C. M. Hart, M. Matters, D. M. de Leeuw, Appl. Phys. Lett. Vol.73, p108 (1998).）。また、パオらは、ＩＴＯ電極を形成したポリエチレンテレフタレート基板上に、低温焼成のポリイミドからなるゲート絶縁膜、ポリチオフェンからなる高分子半導体チャネル層、導電性インクからなる電極層を順次スクリーン印刷することにより有機トランジスタを形成している（Z. Bao, Y. Feng, A. Dodabalapur, V. R. Raju, A. J. Lovinger, Chem. Mater., vol.9, p1299 (1997)）

【０００３】
更に近年では、有機トランジスタを液晶素子、有機電界発光素子（有機ＥＬ素子）や電気泳動素子などのスイッチング素子に応用するという検討がなされている。この場合にはドレイン電流のオン／オフ比が高いこと、つまりドレイン・オフ電流（トランジスタがオフの場合にソース・ドレイン間に流れる電流）が小さいこと、及びドレイン・オン電流（トランジスタがオンの場合にソース・ドレイン間に流れる電流）が大きいことが、コントラスト比向上や応答高速化にあたって要求される。
【０００４】
一般に、電界効果型トランジスタにおいて、ソース、ドレイン間に充分な電圧を印加したときに、両電極間に流れる電流I_Dは、ドレイン・オン電流のみを考慮すると、次式で表されることが知られている。
$I_D = (W/2L)\,\mu C_0 (V_G - V_{th})^2$ … （１）
ここで、Ｗ：ゲート幅、Ｌ：ゲート長、μ：電界効果移動度、C_0：ゲート絶縁膜の単位面積当たりのキャパシタンス、V_G：ゲート電圧、V_{th}：閾値電圧である。ここで、電界効果移動度μは、電界効果型トランジスタのオン電流とゲート電圧との関係から求められ、オン時に半導体層を流れる電流の実効的なキャリア移動度を表す。上記式（１）から、電界効果型トランジスタにおいて大きいドレイン・オン電流を得るためには、電界効果移動度μが大きいことが必要となることが分かる。
【０００５】
しかし、有機半導体材料においてキャリアの伝導機構はホッピング伝導によるものと考えられており、ホッピング伝導による移動度の最大値は数cm^2/Vsが限度と云われている。それ故、オン／オフ比を大きくするには、移動度を大きくすることでオン電流を増やすという方法では限度がある。
【０００６】
図１に示す有機トランジスタ１００は、絶縁性基板１０１上に、ゲート電極１０２、ゲート絶縁膜１０３、ソース電極１０４ａおよびドレイン電極１０４ｂ、および有機半導体層１０５が順次堆積された構造を有し、この構造はプレーナー型あるいはボトムコンタクト型構造とよばれている。この構造の有機トランジスタ１００は、半導体層１０５がソース電極１０４ａおよびドレイン電極１０４ｂを覆うように形成されているため、トランジスタがオフの場合にソース電極１０４ａおよびドレイン電極１０４ｂの上面から半導体層１０５を介して電流が流れ、ソース電極１０４ａとドレイン電極１０４ｂとの間のドレイン・オフ電流が増加する。したがって、このような構造の有機トランジスタでは、オン／オフ比の向上が困難となっている。
【０００７】
この対策として、ソース電極１０４ａとドレイン電極１０４ｂとの間の領域を除く領域にパターニングした絶縁膜を形成し、ソース電極１０４ａとドレイン電極１０４ｂとの間に有機半導体層１０５を選択的に形成する手法が提案されている（特許文献１参照。）。
【特許文献１】特開２０００－２６９５０４号公報
【特許文献２】特開平１０－２５５９４５号公報
【発明の開示】
【発明が解決しようとする課題】
【０００８】
しかしながら、上記特許文献１の手法ではソース電極とドレイン電極をパターニングにより形成した上で、ソース電極およびドレイン電極の位置に合わせて正確に絶縁膜をパターニングする必要があり、絶縁膜のパターニング位置によりチャネルとして機能する有機半導体層が形成される位置が決まってくる。したがって、工程数が増加し複雑化すると共に、高精度の位置決めが必要とされるので位置ずれによる歩留まり低下が懸念される。特に有機トランジスタが適用されるアクティブマトリックス方式の液晶表示装置では、数百万個という画素の各々に対して１つの有機トランジスタが使用される一方、数個程度の有

機トランジスタが動作不良となっただけで表示性能の劣化を招いてしまう。

【０００９】

そこで、本発明は上記問題点に鑑みてなされたもので、本発明の目的は、簡略化した構造でドレイン・オフ電流を抑制しオン／オフ比の大きな有機半導体層を有する半導体装置、およびその半導体装置を備えた表示装置を提供することである。本発明の他の目的は、工程の簡略化および低コスト化を図った半導体装置の製造方法を提供することである。

【課題を解決するための手段】

【００１０】

請求項１に記載の如く、絶縁性基板と、前記絶縁性基板上に形成されたゲート電極と、前記ゲート電極を覆うゲート絶縁膜と、前記ゲート絶縁膜の表面に、所定の間隙を有して配置された第１のソース／ドレイン電極および第２のソース／ドレイン電極と、該第１のソース／ドレイン電極と第２のソース／ドレイン電極との間に充填された有機物からなる半導体層と、を備えた半導体装置であって、前記第１のソース／ドレイン電極および第２のソース／ドレイン電極の表面が前記半導体層から露出して形成されてなることを特徴とする半導体装置が提供される。

【００１１】

請求項１に記載の発明によれば、第１および第２のソース／ドレイン電極は、その表面が半導体層から露出し、その表面上に半導体層が形成されないので、第１および第２のソース／ドレイン電極表面から半導体層を介して電流が流れることを防止して、ドレイン・オフ電流を抑制し、半導体装置のオン／オフ比を向上することができる。

【００１２】

請求項２に記載の如く、請求項１記載の半導体装置において、前記第１のソース／ドレイン電極および第２のソース／ドレイン電極と半導体層を覆う絶縁膜を更に備え、前記絶縁膜が第１のソース／ドレイン電極および第２のソース／ドレイン電極と接して形成されてなる。

【００１３】

請求項２に記載の発明によれば、第１および第２のソース／ドレイン電極の表面に絶縁膜が接して形成されているので、表面からの半導体層への電流流通を一層防止することができる。

【００１４】

請求項３に記載の如く、絶縁性基板と、前記絶縁性基板の表面に、所定の間隙を有して配置された第１のソース／ドレイン電極および第２のソース／ドレイン電極と、該第１のソース／ドレイン電極と第２のソース／ドレイン電極との間に充填された有機物からなる半導体層と、前記第１のソース／ドレイン電極および第２のソース／ドレイン電極と半導体層を覆うゲート絶縁膜と、前記ゲート絶縁膜上に形成されたゲート電極と、を備えた半導体装置が提供される。

【００１５】

請求項３に記載の発明によれば、第１および第２のソース／ドレイン電極が絶縁性基板とゲート絶縁膜に挟まれて形成されているので、絶縁性基板側やゲート絶縁膜側の表面からの半導体層を介しての電流流通を防止することができる。また、半導体層が絶縁性基板とゲート絶縁膜に挟まれて形成されているので、半導体装置の使用時に外部の雰囲気に曝されることがない。したがって、半導体層の有機半導体材料の電気特性を劣化させる水分や酸素との接触や侵入を回避することができ、耐久性を向上することができる。

【００１６】

請求項４に記載の如く、請求項１～３のうち、いずれか一項記載の半導体装置において、前記第１のソース／ドレイン電極および第２のソース／ドレイン電極は、互いに対向する各々の面がテーパー形状あるいは曲面形状を有する。

【００１７】

請求項４に記載の発明によれば、断面形状が矩形である場合よりも第１および第２のソース／ドレイン電極と半導体層との界面に空隙が生じ難くなって接触状態が良好となり、

電界効果に寄与する実効面積を増加することができる。

【００１８】

請求項５に記載の如く、請求項１～４のうち、いずれか一項記載の半導体装置において、前記第１のソース／ドレイン電極および第２のソース／ドレイン電極は互いに仕事関数が異なる材料よりなる。

【００１９】

請求項５に記載の発明によれば、仕事関数の差違により第１のソース／ドレイン電極と第２のソース／ドレイン電極との間に電位差が生じ、ドレイン電圧として印加する電圧を低減することができる。

【００２０】

請求項６に記載の如く、請求項１～５のうち、いずれか一項記載の半導体装置において、前記第１のソース／ドレイン電極および／または第２のソース／ドレイン電極は導電性有機材料よりなる。

【００２１】

請求項６に記載の発明によれば、第１および第２のソース／ドレイン電極の材料に導電性有機材料を用いることにより、第１および第２のソース／ドレイン電極と半導体層との界面張力を低減し素子特性の悪化を防止することができる。

【００２２】

請求項７に記載の如く、請求項１～６のうち、いずれか一項記載の半導体装置において、前記半導体層はキャリア密度の異なる有機半導体材料を混合してなる。

【００２３】

請求項７に記載の発明によれば、キャリア移動度の低下を回避しつつドレイン・オフ電流を一層低減することができる。

【００２４】

請求項８に記載の如く　画像素子部と、請求項１～７のうちいずれか一項記載の半導体装置が配置されなり、前記半導体装置を選択的にオンあるいはオフさせて、前記素子部に電界を印加し、あるいは前記素子部にキャリアを注入して画像素子部の光学的性質を制御する画像素子部駆動手段と、を備える表示装置が提供される。

【００２５】

請求項８に記載の発明によれば、請求項１～７のうちいずれか一項記載の半導体装置がドレイン・オフ電流が抑制されオン／オフ比の向上が図られているので、表示性能として高いコントラスト比を有する表示装置を実現できる。

【００２６】

請求項９に記載の如く、絶縁性基板上にゲート電極を形成する工程と、前記ゲート電極を覆うゲート絶縁膜を形成する工程と、前記ゲート絶縁膜上に有機物からなる半導体層を形成する工程と、前記半導体層を選択的に研削しゲート絶縁膜を露出する溝を形成する工程と、前記半導体層を覆うと共に溝を充填するソース／ドレイン電極層を形成する工程と、前記半導体層表面のソース／ドレイン電極層を除去しソース／ドレイン電極を形成する工程と、を備えた半導体装置の製造方法が提供される。

【００２７】

請求項９に記載の発明によれば、半導体層をソース／ドレイン電極よりも先に形成しているので、ソース／ドレイン電極表面に半導体層が形成されることがなく、また、半導体層表面のソース／ドレイン電極層が除去されているので、ソース／ドレイン電極表面から半導体層を介して流れる電流を防止し、ドレイン・オフ電流を抑制することができる。

【００２８】

請求項１０に記載の如く、絶縁性基板上にゲート電極を形成する工程と、前記ゲート電極を覆うゲート絶縁膜を形成する工程と、前記ゲート絶縁膜上に有機物からなる半導体層を形成する工程と、前記半導体層表面にレジスト膜を形成し、該レジスト膜を選択的に除去する工程と、前記レジスト膜をマスクとして半導体層を選択的に研削しゲート絶縁膜表面を露出する溝を形成する工程と、前記レジスト膜を覆うと共に溝を充填するソース／ド

レイン電極層を形成する工程と、前記レジスト膜をリフトオフ法により半導体層表面を露出してソース／ドレイン電極を形成する工程と、を備えた半導体装置の製造方法が提供される。

【００２９】

請求項１０に記載の発明によれば、請求項９の発明の効果に加え、レジスト膜上のソース／ドレイン電極層をリフトオフによって除去することにより、請求項９の発明の半導体層表面のソース／ドレイン電極層の研削工程を省略することができ、製造工程を簡略化できる。

【００３０】

請求項１１に記載の如く、絶縁性基板上にゲート電極を形成する工程と、前記ゲート電極を覆うゲート絶縁膜を形成する工程と、前記ゲート絶縁膜上にソース／ドレイン電極層を形成する工程と、前記ソース／ドレイン電極層を選択的に研削しソース／ドレイン電極およびゲート絶縁膜を露出する溝を形成する工程と、前記ソース／ドレイン電極を覆うと共に溝を充填する有機物からなる半導体層を形成する工程と、前記ソース／ドレイン電極表面の半導体層を除去する工程と、を備えた半導体装置の製造方法が提供される。

【００３１】

請求項１１に記載の発明によれば、ソース／ドレイン電極を形成した後に有機物からなる半導体層を形成し、ソース／ドレイン電極表面の半導体層を除去することにより、ソース／ドレイン電極表面から半導体層を介して流れる電流を防止してドレイン・オフ電流を抑制することができる。

【００３２】

請求項１２に記載の如く、絶縁性基板上にゲート電極を形成する工程と、前記ゲート電極を覆うゲート絶縁膜を形成する工程と、前記ゲート絶縁膜上にソース／ドレイン電極層を形成する工程と、前記ソース／ドレイン電極層表面にレジスト膜を形成し、該レジスト膜を選択的に除去する工程と、前記レジスト膜をマスクとしてソース／ドレイン電極層を選択的に研削しソース／ドレイン電極およびゲート絶縁膜表面を露出する溝を形成する工程と、前記レジスト膜を覆うと共に溝を充填する有機物からなる半導体層を形成する工程と、前記レジスト膜をリフトオフ法によりソース／ドレイン電極表面を露出する工程と、を備えた半導体装置の製造方法が提供される。

【００３３】

請求項１２に記載の発明によれば、請求項１１の発明の効果に加えて、レジスト膜上の半導体層をリフトオフによって除去することにより、ソース／ドレイン電極表面の半導体層の研削工程を省略することができ、製造工程を簡略化できる。また、清浄なソース／ドレイン電極表面を容易に得ることができる。

【００３４】

請求項１３に記載の如く、絶縁性基板上に有機物からなる半導体層を形成する工程と、前記半導体層を選択的に研削し絶縁性基板表面を露出する溝を形成する工程と、前記半導体層を覆うと共に溝を充填するソース／ドレイン電極層を形成する工程と、前記半導体層表面のソース／ドレイン電極層を除去しソース／ドレイン電極を形成する工程と、前記半導体層とソース／ドレイン電極を覆うゲート絶縁膜を形成する工程と、前記ゲート絶縁膜表面に選択的にゲート電極を形成する工程と、を備えた半導体装置の製造方法が提供される。

【００３５】

請求項１３に記載の発明によれば、半導体層を形成した後にソース／ドレイン電極層を形成し、半導体層上のソース／ドレイン電極層を除去することにより、ソース／ドレイン電極表面から半導体層を介して流れる電流を防止してドレイン・オフ電流を抑制することができる。

【００３６】

請求項１４に記載の如く、絶縁性基板上に有機物からなる半導体層を形成する工程と、前記半導体層表面にレジスト膜を形成し、該レジスト膜を選択的に除去する工程と、前記

レジスト膜をマスクとして半導体層を選択的に研削し絶縁性基板表面を露出する溝を形成する工程と、前記レジスト膜を覆うと共に溝を充填するソース／ドレイン電極層を形成する工程と、前記レジスト膜をリフトオフ法により半導体層表面を露出してソース／ドレイン電極を形成する工程と、前記半導体層とソース／ドレイン電極を覆うゲート絶縁膜を形成する工程と、前記ゲート絶縁膜表面に選択的にゲート電極を形成する工程と、を備えた半導体装置の製造方法が提供される。

【００３７】

請求項１４に記載の発明によれば、請求項１３の発明の効果に加えて、レジスト膜上のソース／ドレイン電極層をリフトオフによって除去することにより、半導体層表面のソース／ドレイン電極層の研削工程を省略することができ、製造工程を簡略化できる。また、清浄な半導体層表面を容易に得ることができる。

【００３８】

請求項１５に記載の如く、絶縁性基板上にソース／ドレイン電極層を形成する工程と、前記ソース／ドレイン電極層を選択的に研削しソース／ドレイン電極および絶縁性基板表面を露出する溝を形成する工程と、前記ソース／ドレイン電極を覆うと共に溝を充填する有機物からなる半導体層を形成する工程と、前記ソース／ドレイン電極表面の半導体層を除去する工程と、前記ソース／ドレイン電極と半導体層を覆うゲート絶縁膜を形成する工程と、前記ゲート絶縁膜表面に選択的にゲート電極を形成する工程と、を備えた半導体装置の製造方法が提供される。

【００３９】

請求項１５に記載の発明によれば、ソース／ドレイン電極層を形成した後に半導体層を形成し、ソース／ドレイン電極層上の半導体層を除去することにより、ソース／ドレイン電極表面から半導体層を介して流れる電流を防止してドレイン・オフ電流を抑制することができる。

【００４０】

請求項１６に記載の如く、絶縁性基板上にソース／ドレイン電極層を形成する工程と、前記ソース／ドレイン電極層表面にレジスト膜を形成し、該レジスト膜を選択的に除去する工程と、前記レジスト膜をマスクとしてソース／ドレイン電極層を選択的に研削しソース／ドレイン電極および絶縁性基板表面を露出する溝を形成する工程と、前記レジスト膜を覆うと共に溝を充填する有機物からなる半導体層を形成する工程と、前記レジスト膜をリフトオフ法によりソース／ドレイン電極表面を露出する工程と、前記ソース／ドレインと半導体層を覆うゲート絶縁膜を形成する工程と、前記ゲート絶縁膜表面に選択的にゲート電極を形成する工程と、を備えた半導体装置の製造方法が提供される。

【００４１】

請求項１６に記載の発明によれば、請求項１６の発明の効果に加えて、レジスト膜上の半導体層をリフトオフによって除去することにより、ソース／ドレイン電極表面の半導体層の研削工程を省略することができ、製造工程を簡略化できる。また、清浄な半導体層表面を容易に得ることができる。

【００４２】

請求項１７に記載の如く、請求項９～１６のうち、いずれか一項記載の半導体装置の製造方法において、前記ソース／ドレイン電極層を形成する工程は、導電性微粒子材料あるいは導電性有機材料を溶媒中に分散あるいは溶解し、塗布法により行う。

【００４３】

請求項１７に記載の発明によれば、ソース／ドレイン電極層を塗布法により形成しているので、真空プロセス等よりも製造コストを低減することができる。

【００４４】

請求項１８に記載の如く、請求項９～１７のうち、いずれか一項記載の半導体装置の製造方法において、前記半導体層を形成する工程は、有機低分子、有機高分子、あるいは有機オリゴマーからなる有機半導体材料を塗布法により形成する。

【００４５】

請求項１８に記載の発明によれば、半導体層を塗布法により行うので、真空プロセス等よりも製造コストを低減することができる。

【発明の効果】

【００４６】

本発明によれば、第１および第２のソース／ドレイン電極は、その表面が半導体層から露出しその表面上に半導体層が形成されていないので、第１および第２のソース／ドレイン電極表面から半導体層を介して電流が流れることを防止して、ドレイン・オフ電流を抑制し、半導体装置のオン／オフ比を向上することができる。

【発明を実施するための最良の形態】

【００４７】

以下図面を参照しつつ実施の形態を説明する。

【００４８】

（第１の実施の形態）

図２は、本発明の第１の実施の形態に係る半導体装置の断面図である。図２を参照するに、本実施の形態の半導体装置１０は、絶縁性基板１１と、絶縁性基板１１上にゲート電極１２と、ゲート絶縁膜１３とが順次形成され、ゲート絶縁膜１３上に所定の距離を有して離隔して配置された２つのソース／ドレイン電極１４と、ゲート絶縁膜１３表面を覆うと共にソース／ドレイン電極１４間を充填する半導体層１５と、ソース／ドレイン電極１４および半導体層１５の表面を覆う絶縁膜１６から構成されている。

【００４９】

半導体装置１０は、ゲート電極１２に印加されるゲート電圧が閾値電圧を超えてオンの状態では、ソース／ドレイン電極１４間の半導体層１５に形成されるチャネルを流れるドレイン電流量がゲート電圧に対応して変化すると共に、ゲート電圧が閾値電圧以下のオフの状態では、絶縁膜１６側のソース／ドレイン電極表面１４ａには半導体層１５が形成されていないので、ソース／ドレイン電極表面１４ａ側から半導体層１５を介してのリーク電流を防止することができ、ドレイン・オフ電流を低減することができる。その結果オン／オフ比を向上することができる。以下、具体的に半導体装置１０の構成について説明する。

【００５０】

絶縁性基板１１は、絶縁性の樹脂基板、ガラス基板、半導体基板、およびセラミックス基板等、特に限定されないが、本実施の形態の半導体装置１０が適用される表示装置や電子装置に可撓性を付与する場合は樹脂基板が好ましく、その樹脂材料としては例えば、スチレン系重合体、スチレンーブタジエン共重合体、スチレンーアクリロニトリル共重合体、スチレンーマレイン酸共重合体、アクリル共重合体、スチレンーアクリル酸共重合体、ポリエチレン、エチレン－酢酸ビニル共重合体、塩素化ポリエチレン、ポリ塩化ビニル、ポリプロピレン、塩化ビニル－酢酸ビニル共重合体、ポリエステルアルキド樹脂、ポリアミド、ポリイミド、ポリウレタン、ポリカーボネート、ポリアリレート、ポリスルホン、ジアリルフタレート樹脂、ケトン樹脂、ポリビニルブチラール樹脂、ポリエーテル樹脂、ポリエステル樹脂等の熱可塑性樹脂や、シリコーン樹脂、エポキシ樹脂、フェノール樹脂、尿素樹脂、メラミン樹脂、その他架橋性の熱硬化性樹脂、さらにエポキシアクリレート、ウレタンーアクリレート等の光硬化性樹脂等があげられる。耐熱性、防湿性の点からポリイミドが好ましく、例えば市販品としてＳＥ－１１８０（日産化学社製商品名）、ＡＬ３０４６（ＪＳＲ社製商品名）が挙げられる。

【００５１】

ゲート電極１２は、例えばゲート長方向が長さ１μｍ～１０００μｍ、ゲート幅方向が長さ５μｍ～４０００μｍ、膜厚１０ｎｍ～２００ｎｍを有し、導電性材料であれば特に限定されないが、例えば、白金、金、銀、ニッケル、クロム、銅、鉄、錫、アンチモン、鉛、タンタル、インジウム、パラジウム、テルル、レニウム、イリジウム、アルミニウム、ルテニウム、ゲルマニウム、モリブデン、タングステン、およびこれらの金属の合金や、酸化スズ・アンチモン、酸化インジウム・スズ（ＩＴＯ）、酸化インジウム・酸化亜鉛

（ＩＺＯ）、フッ素ドープ酸化亜鉛、亜鉛、炭素、グラファイト、グラッシーカーボン、銀ペーストおよびカーボンペースト、リチウム、フッ化リチウム、ベリリウム、カリウム、カルシウム、スカンジウム、チタン、マンガン、ジルコニウム、ガリウム、ニオブ、ナトリウム、ナトリウムーカリウム合金、マグネシウム、マグネシウム／銅混合物、マグネシウム／銀混合物、マグネシウム／アルミニウム混合物、マグネシウム／インジウム混合物、アルミニウム／酸化アルミニウム混合物、リチウム／アルミニウム混合物、あるいはこれらの積層体を用いることができる。これらのうち、大気中での安定性の点で、白金、金、銀、銅、アルミニウム、インジウム、ＩＴＯ、ＩＺＯおよび炭素が好適である。

【００５２】

また、導電性微粒子の加熱融着体を用いることができる。導電性微粒子としては、平均粒子径（直径）が１～５０ｎｍ、好ましくは１～１０ｎｍの白金、金、銀、銅、コバルト、クロム、イリジウム、ニッケル、パラジウム、モリブデン、タングステンなどの金属微粒子が挙げられる。

【００５３】

さらに、導電性のカーボンブラック、カーボンナノチューブ、およびフラーレン（Ｃ６０、Ｃ７０）などのカーボン材料を用いることができる。

【００５４】

ゲート絶縁膜１３は、例えば膜厚が１０ｎｍ～１０００ｎｍ（好ましくは１００ｎｍ～１０００ｎｍ）の範囲に設定され、絶縁性材料であれば有機材料、無機材料の何れの材料でも用いることができる。有機材料としては、例えば、ポリクロロピレン、ポリエチレンテレフタレート、ポリオキシメチレン、ポリビニルクロライド、ポリフッ化ビニリデン、シアノエチルプルラン、ポリメチルメタクリレート、ポリサルフォン、ポリカーボネート、ポリイミド、ポリエチレン、ポリエステル、ポリビニルフェノール、メラミン樹脂、フェノール樹脂、フッ素樹脂、ポリフェニレンスルフィド、ポリパラキシレン、ポリアクリロニトリルなどが挙げられる。また、無機材料としては、酸化シリコン、窒化シリコン、酸化アルミニウム、窒化アルミニウム、酸化チタン、および窒素酸化シリコンなどが挙げられる。さらにゲート絶縁膜１３には各種絶縁性Ｌａｎｇｍｕｉｒ－Ｂｌｏｄｇｅｔｔ膜等を用いることができる。もちろんこれらの材料に限られるわけではなく、また、これらの材料を２種類以上用いてもよく、異なる材料からなる絶縁膜を２層以上積層してもよい。

【００５５】

これらの絶縁性材料のうち、比誘電率の点で、窒化シリコン、酸化アルミニウム、窒化アルミニウム、酸化チタン、窒素酸化シリコンが好ましい。ゲート絶縁膜全体の比誘電率を向上すると共にゲートリーク電流を一層抑制することができる。また、ゲート電極１２との接着強度の向上を図る絶縁性材料を適宜選択することができる。

【００５６】

ゲート絶縁膜１３の形成方法は特に制限はなく、例えばＣＶＤ法、プラズマＣＶＤ法、プラズマ重合法、真空蒸着法、スパッタ法、スピンコーティング法、ディッピング法、クラスタイオンビーム蒸着法およびＬａｎｇｍｕｉｒ－Ｂｌｏｄｇｅｔｔ法などが挙げられ、何れも使用可能である。

【００５７】

ソース／ドレイン電極１４は、ゲート絶縁膜１３上にゲート電極１２と対向するように互いに離隔して、例えばゲート長方向が長さ１μｍ～１０００μｍ、ゲート幅方向が長さ５μｍ～４０００μｍ、２つのソース／ドレイン電極１４のゲート長方向の間隙０．０１μｍ～１０００μｍの範囲に設定される。

【００５８】

ソース／ドレイン電極１４の膜厚は、例えば１０ｎｍ～２００ｎｍの範囲に設定され、半導体装置１０が動作時にゲート絶縁膜との界面付近の半導体層に形成されるチャネル厚さよりも大きくすることが好ましく、具体的には２０ｎｍ～１００ｎｍの範囲に設定されることが好ましい。チャネルを十分厚く形成することによりドレイン・オン電流を確保す

ることができる。

【００５９】

ソース／ドレイン電極１４の材料は、上述したゲート電極１２と同様の材料を用いることができる。さらに、有機溶媒または水に溶解あるいは分散する導電性材料を用いることができる。このような導電性材料は塗布可能であるので、真空蒸着法等の真空プロセスに比べ製造コストを低減できる。

【００６０】

ソース／ドレイン電極１４に用いられる、有機溶媒または水に溶解あるいは分散する導電性材料としては、例えば、銀ペースト、金ペーストや銅ペースト、グラファイトインクのように導電性微粒子を有機溶媒中に分散させたポリマー混合物や導電性有機材料が挙げられる。

【００６１】

ソース／ドレイン電極１４に用いられる導電性有機材料は以下の点で金属材料よりも好ましい。すなわち、電極材料が金属の場合は、金属と半導体層１５の有機物との界面張力が大きいため、界面近傍の有機分子の配列が乱れキャリアのトラップサイトが形成され、素子特性が悪化することが報告されている（J. Wang, D. J. Gundlach, C. C. Kuo, and T. N. Jackson, 41st Electronic Materials Conference Digest, p. 16, June 1999）。そこで、電極材料に導電性有機材料を用いることで界面張力を低減し素子特性の悪化を防止することができる。

【００６２】

このような導電性有機材料としては、例えば、ポリアセチレン、ポリピロール、ポリチオフェン、ポリパラフェニレン、ポリパラフェニレンビニレン、ポリチエニレンビニレン、ポリフルオレン、ポリアニリン、ポリアセン、ポリフランなどの共役系高分子やその誘導体が挙げられる。さらに、適当なドーパントをドーピングすることにより導電率を高くして用いてもよい。ドーパントとしては、溶液状態での分散安定性の点でポリスルホン酸、ポリスチレンスルホン酸、ナフタレンスルホン酸、アルキルナフタレンスルホン酸などの蒸気圧の低いものを用いるのが好ましい。なお、これらの有機溶媒または水に溶解あるいは分散する導電性材料をゲート電極１２に用いてもよい。

【００６３】

なお、有機溶媒または水に溶解あるいは分散する導電性材料の市販品の例としては、パーフェクトゴールド（登録商標）（金ペースト、真空冶金社製商品名）、パーフェクトカッパー（銅ペースト、真空冶金社製商品名）、Ｏｒｇａｃｏｎ　Ｐａｓｔｅ　ｖａｒｉａｎｔ　１／４、Ｐａｓｔｅ　ｖａｒｉａｎｔ　１／３（以上、印刷用透明ＰＥＤＯＴ／ＰＳＳインク、日本アグファ・ゲバルト社製商品名）、Ｏｒｇａｃｏｎ　Ｃａｒｂｏｎ　Ｐａｓｔｅ　ｖａｒｉａｎｔ　２／２（カーボン電極ペースト、日本アグファ・ゲバルト社製商品名）、ＢＡＹＴＲＯＮ（登録商標）　Ｐ（ＰＥＤＴ／ＰＳＳ水溶液、日本スタルクヴィテック社製商品名）などが挙げられる。

【００６４】

また、ソース／ドレイン電極１４の材料は、半導体層１５とオーミック接触を形成する電極材料を用いることが好ましい。ソース／ドレイン電極１４と半導体層１５とのエネルギー障壁を低減することができる。具体的には半導体層１５に、キャリアがホールであるｐ型半導体を用いた場合は、電極材料の仕事関数（真空準位からフェルミ準位までのエネルギー差）が半導体層１５の仕事関数よりも大きい電極材料が好ましく、例えば、金（５．１ｅＶ）、白金（５．６５ｅＶ）、イリジウム（５．２７ｅＶ）、パラジウム（５．１２ｅＶ）、ニッケル（５．１５ｅＶ）やスズ・インジウム酸化物（ＩＴＯ）や酸化亜鉛（ＺｎＯ）などが挙げられる。また、ｎ型半導体を用いた場合は、電極材料の仕事関数が半導体層１５の仕事関数よりも小さい電極材料が好ましく、例えば、マグネシウム（３．６６ｅＶ）やバリウム（２．７ｅＶ）などのアルカリ土類金属、ガリウム（４．２ｅＶ）、インジウム（４．１２ｅＶ）、アルミニウム（４．２８ｅＶ）、銀（４．２６ｅＶ）などが挙げられる。なお、かっこ内の数値は仕事関数を示している。なお、ソース／ドレイン

電極１４材料と半導体層１５材料の組み合わせは、具体的には半導体装置１０の電流一電圧特性を調べることにより、これらの接触面において電気抵抗がより低下するように選択してもよい。

【００６５】

さらに、２つのソース／ドレイン電極１４を互いに異なる仕事関数を有する材料より構成してもよい。半導体層１５にキャリアがホールであるｐ型半導体を用いた場合は、２つのソース／ドレイン電極のうち、ソース電極の材料に対してドレイン電極の材料の仕事関数を小さくなるように選択する。このように選択することにより、負のソース・ドレイン間電圧を印加した際と同じ方向に電位差が生じ、ソース・ドレイン間電圧として印加する電圧を低減することができる。例えばソース電極に金、ドレイン電極に銀を用いる。なお、ｎ型半導体を用いた場合は、ソース電極とドレイン電極の材料を入れ換えればよい。

【００６６】

ゲート電極１２およびソース／ドレイン電極１４の形成方法としては、公知のフォトリソグラフィ法やリフトオフ法を用いてこれらの電極のパターンを形成し、上記の導電性材料を蒸着法、スパッタ法によりパターニングされた導電膜を形成する方法や、アルミニウムや銅などの金属箔上に熱転写あるいはインクジェット等によりレジストのパターンを形成し、エッチングにより電極を形成してもよい。また、導電性ポリマーの溶液あるいは分散液、導電性微粒子分散液を直接インクジェット装置により噴射して電極を形成してもよく、カーボンブラックや導電性ポリマー、導電性微粒子を含む導電性インクや導電性ペーストなどを塗布した塗工膜をリソグラフィ法やレーザーアブレーション法などによりパターニングして形成してもよく、かかる導電性インクや導電性ペーストを凸版、凹版、平版、スクリーン印刷などの印刷法でパターニングされた電極を形成してもよい。

【００６７】

ソース／ドレイン電極１４は、断面形状が図２に示すように矩形形状の他、次に説明するようにテーパー形状等であってもよい。

【００６８】

図３（Ａ）～（Ｃ）は、ソース／ドレイン電極の断面形状を異ならせた第１の実施の形態の変形例に係る半導体装置の断面図である。図中、先に説明した部分に対応する部分には同一の参照符号を付し、説明を省略する。

【００６９】

図３（Ａ）を参照するに、半導体装置２０の２つのソース／ドレイン電極１４－１は、積層方向に対して互いの間隙が広がるテーパー形状、すなわち、下辺１４－１ｂよりも上辺１４－１ａが短い形状を有している。特に、２つのソース／ドレイン電極１４－１が互いに対向する面１４－１ｃがテーパー形状すなわち傾斜面を有していることに特徴がある。このような形状とすることにより、断面形状が矩形である場合よりもソース／ドレイン電極１４－１の互いに対向する面１４－１ｃと半導体層１５との界面に空隙が生じ難くなって接触状態が良好となり、電界効果に寄与する実効面積を増加することができる。なお、図示を省略するが、ソース／ドレイン電極１４－１を積層方向に対して互いの間隙が狭まるテーパー形状、すなわち下辺１４－１ｂよりも上辺１４－１ａが長い形状としてもよい。

【００７０】

また、図３（Ｂ）あるいは（Ｃ）に示すように、半導体装置２１、２２の２つのソース／ドレイン電極１４－２、１４－３の互いに対向する面１４－２ｃ、１４－３ｃが直線的な傾斜面のみならず、図３（Ｂ）に示す内側に凸状、あるいは図３（Ｃ）に示す内側に凹状の曲面形状としてもよい。テーパー形状と同様の効果を得ることができる。

【００７１】

図２に戻り、半導体層１５は、例えば膜厚が５ｎｍ～５００ｎｍ（好ましくは１０ｎｍ～２００ｎｍ）の範囲に設定される。５ｎｍより薄膜とすると半導体層１５中に形成される活性層の厚さが十分ではなく、トランジスタ特性を低下させてしまう。また、５００ｎｍよりも厚膜とすると、活性層の厚さと比較して過度に厚くなるためチャネル形成に寄与

せず、さらにドレイン・オフ電流の増加の原因となる。

【００７２】

半導体層１５の材料としては、公知の有機半導体材料を用いることができ、特に塗布可能な有機低分子や有機高分子、有機オリゴマー等の有機半導体材料を用いることが製造容易、低製造コストの点で好ましい。有機低分子および有機オリゴマー材料としては、例えば、アントラセン、テトラセン、ペンタセンやそれらの置換誘導体を含むアセン分子材料、金属フタロシアニン、チオフェンオリゴマーやその誘導体、フラーレンＣ６０やカーボンナノチューブとその誘導体などが挙げられる。ペンタセンのような低分子系材料は真空蒸着法により成膜することが一般的であるが、J. E. Anthonyra et al, Org. Lett. vol. 4 p15 (2002)や、P. T. Herwig et al, Adv. Mater. vol.11, p480 (1999)に記載されるペンタセンの前駆体を用いて塗布した後に化学変化させることによりペンタセン膜を形成する方法を用いることができる。

【００７３】

また、有機高分子材料としては、π電子共役系高分子やσ電子共役系高分子またはこれらの誘導体が用いられる。π電子共役系高分子としては、例えば、ポリパラフェニレン、ポリアセチレン、ポリピロール、ポリチオフェン、ポリフラン、ポリセレノフェン、ポリアニリン、ポリアズレン、ポリピレン、ポリフルオレン、ポリパラフェニレンビニレン、ポリチエニレンビニレン、ポリベンゾフラン、ポリベンゾチオフェン、ポリインドール、ポリカルバゾール、ポリジベンゾフラン、ポリイソチアナフテン、ポリイソナフトチオフェン、ポリジアセチレン、ポリフェニレンスルフィド、ポリフェニレンオキシドなどが挙げられる。また生体材料としてデオキシリボ核酸（ＤＮＡ）を使用することも可能である。さらに、電子受容体と電子供与体からなる電荷移動錯体を使用することもできる。電子受容体の例としては、２，３－ジクロロ－５，６－ジシアノ－ｐ－ベンゾキノン、２，５－ジメチルテトラシアノキノジメタン、テトラシアノキノジメタンなどが挙げられる。電子供与体の例としては、ジベンゾテトラチアフルバレン、テトラセレナフルバレン、テトラチアフルバレン、テトラチアテトラセン、テトラメチルテトラチアフルバレンなどが挙げられる。上記の有機半導体材料は、複数を混合して用いてもよく、バインダ樹脂に分散して用いてもよい。

【００７４】

半導体層１５の材料として、キャリア密度の高い高分子有機半導体材料とキャリア密度の低い低分子有機半導体材料を混合して用いてもよい。ドレイン・オフ電流を低減すると共にキャリア移動度の低下を回避することができる。例えば、キャリア密度の高い高分子有機半導体材料としてはポリフルオレン誘導体が挙げられ、キャリア密度の低い低分子有機半導体材料としては電荷発生材料として用いられるブタジエン誘導体や芳香族第三級アミン誘導体が挙げられる。

【００７５】

半導体層１５の形成方法としては、スプレーコート法、スピンコート法、ブレードコート法、ディップコート法、キャスト法、ロールコート法、バーコート法、ダイコート法、スクリーン法およびＬＢ法等の塗布方法や、真空蒸着法、分子線エピタキシャル成長法、イオンクラスタービーム法、低エネルギーイオンビーム法、イオンプレーティング法、ＣＶＤ法、スパッタリング法、プラズマ重合法、電解重合法、化学重合法等が挙げられ、半導体層１５の材料に応じて使用することができる。

【００７６】

図４（Ａ）～（Ｃ）は半導体層の表面形状を異ならせた第１の実施の形態の他の変形例に係る半導体装置の断面図である。図４（Ａ）～（Ｃ）を参照するに、半導体装置３０～３２の半導体層１５－１～１５－３の絶縁膜１６側の表面１５－１ａ～１５－３ａは、図２に示すように平面形状に限定されず、図４（Ａ）に示す凹状の表面１５－１ａや、図４（Ｂ）に示す凸状の表面１５－２ａ、あるいは図４（Ｃ）に示す曲面形状の表面１５－３ａを有していてもよい。これらの表面は半導体層１５－１～１５－３を塗布した場合に形成されやすいが、ドレイン・オン電流に影響はなく、かつソース／ドレイン電極表面１４

－１ａには半導体層１５－１～１５－３が形成されないので、ドレイン・オフ電流を増加させることはない。絶縁膜１６との密着性および絶縁膜１６の被覆性の点で図２の平面形状表面や図４（Ａ）の凹状表面１５－１ａが好ましい。

【００７７】

図２に戻り、絶縁膜１６は、２つのソース／ドレイン電極１４および半導体層１５の表面に接して形成され、膜厚は特に限定されず、例えば１００ｎｍに設定される。絶縁膜１６の材料は、上述したゲート絶縁膜１３と同様の材料を用いることができる。なお、絶縁膜１６は、後述する第２の実施の形態に係る表示装置等に適用される場合は封止層や配向膜であってもよく、また、ソース／ドレイン電極１４および半導体層１５が空気中、減圧雰囲気中、絶縁性液体などの絶縁性の外部雰囲気に露出される際は絶縁膜１６を設けなくてもよい。

【００７８】

本実施の形態によれば、２つのソース／ドレイン電極１４の表面が半導体層１５から露出しており、さらに、その表面に絶縁膜１６が形成され、あるいはその表面が絶縁性の外部雰囲気に露出しているので、その表面から半導体層１５を介して電流が流れることを防止してドレイン・オフ電流を抑制し、オン／オフ比を向上することができる。

【００７９】

次に本実施の形態の半導体装置の製造方法について説明する。ここでは、図２に示す第１の実施の形態に係る半導体装置を例として説明する。

【００８０】

図５（Ａ）～（Ｄ）は、第１の実施の形態の半導体装置の製造工程を示す図である。

【００８１】

まず、図５（Ａ）の工程では、絶縁性基板１１上に、例えばオフセット印刷法により金ナノ粒子を含むインクを用いてゲート電極１２のパターンを印刷し、乾燥（例えば加熱温度１００℃）および焼成（例えば加熱温度３００℃）して例えば膜厚１００ｎｍのゲート電極１２を形成する。次いでゲート電極１２上にスプレー法やディッピング法を用いてポリイミド膜などの有機絶縁膜を形成し加熱処理して膜厚３００ｎｍのゲート絶縁膜１３を形成する。

【００８２】

図５（Ａ）の工程ではさらに、ゲート絶縁膜１３を覆うように例えば電子ビーム蒸着法により例えば膜厚１００ｎｍのペンタセン膜の半導体層１５を形成する。

【００８３】

次いで図５（Ｂ）の工程では、ゲート絶縁膜１３上に例えば膜厚１μｍのレジスト膜４１を形成し、ソース／ドレイン電極１４のパターンをフォトリソグラフィ法によりレジスト膜４１に形成して開口部４１ｈを形成する。

【００８４】

図５（Ｂ）の工程ではさらに、パターニングされたレジスト膜４１をマスクとして、ＲＩＥ（反応性イオンエッチング）法やイオンミリング法などのドライエッチングやフェノールとハロゲン系溶剤を主成分とするレジスト剥離溶液等を用いたウェットエッチングを用いて半導体層１５にゲート絶縁膜１３の表面を露出する開口部１５ｈ（次の図５（Ｃ）および図５（Ｄ）の工程でソース／ドレイン電極１４が形成される。）を形成する。

【００８５】

次いで図５（Ｃ）の工程では、図５（Ｂ）の構造体のレジスト膜４１を除去し、ポリアセチレン等の導電性有機材料を含む溶液をスピンコート法、スプレー法などにより半導体層１５の開口部１５ｈを充填すると共に半導体層１５を覆うように塗布し、加熱乾燥して例えば膜厚３００ｎｍの電極層１４Ａを形成する。

【００８６】

次いで図５（Ｄ）の工程では、図５（Ｃ）の構造体の電極層１４Ａをプラズマエッチング法などのドライエッチングにより、半導体層１５の表面が露出するまで電極層１４Ａを研削し、ソース／ドレイン電極１４を形成する。半導体層１５上の電極層１４Ａはドレイ

ン・オフ電流を増加する原因となるので完全に除去することが好ましい。

【００８７】

図５（Ｄ）の工程ではさらに、ソース／ドレイン電極１４、および半導体層１５を覆うように、例えば電子ビーム蒸着法により膜厚２００ｎｍのポリイミドからなる絶縁膜１６を形成する。以上により、第１の実施の形態の半導体装置が完成する。

【００８８】

本実施の形態の製造方法では、半導体層１５をソース／ドレイン電極１４よりも先に形成しているので、ソース／ドレイン電極１４表面に半導体層１５が形成されることがなく、かつ半導体層１５表面の電極層１４Ａが除去されているので、ソース／ドレイン電極１４表面から半導体層１５を介して流れる電流を防止し、ドレイン・オフ電流を抑制することができる。

【００８９】

次に第１変形例に係る製造方法を説明する。上述した第１の実施の形態の製造方法では、図５（Ｃ）においてレジスト膜４１を除去した後に開口部１５ｈに電極層１４Ａを充填したが、本変形例に係る製造方法では、レジスト膜４１を除去する前に電極層１４Ａを充填し、その後でレジスト膜４１とその上に堆積した電極層１４Ａをリフトオフする。

【００９０】

図６（Ａ）～（Ｃ）は、第１の実施の形態の半導体装置の製造工程の第１変形例を示す図である。

【００９１】

まず、本変形例では上述した図５（Ａ）および図５（Ｂ）の工程と同様にして、図５（Ｂ）の構造体を形成する。

【００９２】

次いで図６（Ａ）の工程では、図５（Ｂ）の構造体に、例えばスパッタ法、ＣＶＤ法、真空蒸着法等により膜厚１２００ｎｍのニッケルの電極層１４Ａを形成する。

【００９３】

次いで図６（Ｂ）の工程では、図６（Ａ）の構造体のレジスト膜４１を溶解する溶剤を用いてレジスト膜４１とその上の電極層１４Ａをリフトオフし、半導体層１５表面を露出すると共にソース／ドレイン電極１４を形成する。

【００９４】

次いで図６（Ｃ）の工程では、必要があればウェットエッチングあるいはドライエッチングにより図６（Ｂ）の構造体のソース／ドレイン電極１４表面を研削する。次いで、図５（Ｄ）の工程と同様にして、ソース／ドレイン電極１４、および半導体層１５を覆う絶縁膜１６を形成する。

【００９５】

第１変形例の製造方法によれば、上述した第１の実施の形態の半導体装置の製造方法の効果に加えて、レジスト膜４１上の電極層１４Ａをリフトオフによって除去することにより、図５（Ｄ）において説明した半導体層１５表面の電極層１４Ａの研削工程を省略することができる。

【００９６】

次に第２変形例に係る製造方法を説明する。上述した製造方法では、半導体層を先に形成し、次いで電極層を塗布法等により形成したが、第２変形例に係る製造方法ではソース／ドレイン電極を先に形成し、次いで塗布法等により半導体層を形成する。

【００９７】

図７（Ａ）～（Ｄ）は、第１の実施の形態の半導体装置の製造工程の第２変形例を示す図である。

【００９８】

まず、図７（Ａ）の工程では、図５（Ａ）の工程と同様にして絶縁性基板１１上にゲート電極１２およびゲート絶縁膜１３を順次形成する。

【００９９】

図７（Ａ）の工程ではさらに、ゲート絶縁膜上にスピンコート法、ディップ法等により導電性有機材料を塗布し例えば膜厚２００ｎｍの電極層１４Ａを形成する。

【０１００】

次いで図７（Ｂ）の工程では、電極層１４Ａ上に例えば膜厚１μｍのレジスト膜４２を形成し、ソース／ドレイン電極１４のパターンをフォトリソグラフィ法によりパターニングし、レジスト膜４２に開口部４２ｈを形成する。

【０１０１】

図７（Ｂ）の工程ではさらに、パターニングされたレジスト膜４２をマスクとして、ＲＩＥ（反応性イオンエッチング）法やイオンミリング法などのドライエッチングやフェノールなどのアルカリ性の剥離溶液等を用いたウェットエッチングにより電極層１４Ａをゲート絶縁膜１３表面が露出するまで研削し、開口部１４ｈ（次の図７（Ｃ）および図７（Ｄ）の工程で半導体層１５が形成される。）、およびソース／ドレイン電極１４を形成する。

【０１０２】

次いで図７（Ｃ）の工程では、図７（Ｂ）の構造体の表面を覆う半導体層１５を形成する。半導体層１５は、例えばスピンコート法を用いてポリヘキシルチオフェンからなる溶液を塗布し加熱して、例えば膜厚１００ｎｍの半導体層１５を形成する。

【０１０３】

次いで図７（Ｄ）の工程では、半導体層１５の表面をウェットエッチングあるいはドライエッチングによりソース／ドレイン電極１４表面が露出するまで研削する。ここで、エッチング液はエッチング選択性を有する、例えばフェノールを含むアルカリ性のエッチング液を用いる。また、アルゴンガスを用いたイオンミリングを用いてもよい。

【０１０４】

図７（Ｄ）の工程ではさらに、ソース／ドレイン電極１４および半導体層１５の表面を覆う絶縁膜を図５（Ｄ）の工程と同様にして形成する。以上により、第１の実施の形態の半導体装置が完成する。

【０１０５】

第２変形例の製造方法では、パターニングしたソース／ドレイン電極１４を形成した後に半導体層１５を形成し、ソース／ドレイン電極１４表面の半導体層１５をエッチングにより容易に除去することができ、ソース／ドレイン電極１４表面から半導体層１５を介して流れる電流を防止してドレイン・オフ電流を抑制することができる。

【０１０６】

次に、第３変形例に係る製造方法を説明する。第３変形例に係る製造方法では、第２変形例においてソース／ドレイン電極１４表面の半導体層１５をリフトオフ法を用いて除去する。

【０１０７】

図８（Ａ）～（Ｃ）は、第１の実施の形態の半導体装置の製造方法の第３変形例を示す図である。

【０１０８】

まず、本変形例では上述した図７（Ａ）および図７（Ｂ）の工程と同様にして、図７（Ｂ）の構造体を形成する。

【０１０９】

次いで図８（Ａ）の工程では、図７（Ｂ）の構造体に、例えばスピンコート法により、膜厚約１５００ｎｍのポリフェニレンビニレンの半導体層１５を形成する。

【０１１０】

次いで図８（Ｂ）の工程では、レジスト膜４２を溶解する溶剤を用いてレジスト膜４２とその上の半導体層１５をリフトオフし、ソース／ドレイン電極１４の表面を露出する。

【０１１１】

次いで図８（Ｃ）の工程では、必要があればウェットエッチングあるいはドライエッチングにより図８（Ｂ）の構造体の半導体層１５表面を研削する。次いで、ソース／ドレイ

ン電極１４および半導体層１５の表面を覆う絶縁膜を図５（Ｄ）の工程と同様にして形成する。

【０１１２】

第３変形例の製造方法によれば、第２変形例の製造方法の効果に加えて、レジスト膜４２上の半導体層１５をリフトオフによって除去することにより、ソース／ドレイン電極１４表面の半導体層１５の研削工程を省略することができ、清浄なソース／ドレイン電極１４表面を容易に得ることができる。

【０１１３】

なお、上述した第１の実施の形態および第１～第３変形例の製造方法では、フォトリソグラフィ法およびエッチング法等により半導体層あるいはソース／ドレイン電極をパターニングする例を示したが、印刷法によりパターニングされた半導体層あるいはソース／ドレイン電極をゲート絶縁膜あるいは絶縁性基板上に直接形成してもよい。印刷法はフォトリソグラフィ法等のパターニング工程を省略できると共に、量産性が良好であるので半導体装置の低コスト化を図ることができる。印刷法としては、例えばオフセット印刷法、スクリーン印刷法、孔版印刷法等の公知の印刷法を用いることができ、高精細なパターンが形成できる点でオフセット印刷法が好ましい。

【０１１４】

上述した第１の実施の形態に係る半導体装置ではプレーナー型構造の半導体装置を例に説明したが、次に逆スタガー型構造の半導体装置について説明する。

【０１１５】

図９は、第１の実施の形態のその他の変形例に係る逆スタガー型構造の半導体装置の断面図である。図中、先に説明した部分に対応する部分には同一の参照符号を付し、説明を省略する。

【０１１６】

図９を参照するに、第１の実施の形態のその他の変形例に係る半導体装置４０は、絶縁性基板１１と、絶縁性基板１１上に所定の距離を有して離隔して配置された２つのソース／ドレイン電極１４と、絶縁性基板１１表面を覆うと共にソース／ドレイン電極１４間を充填する半導体層１５と、ソース／ドレイン電極１４および半導体層１５の表面を覆うゲート絶縁膜１３と、ゲート絶縁膜１３上に選択的に形成されたゲート電極１２から構成されている。

【０１１７】

半導体装置４０は、ソース／ドレイン電極１４が絶縁性基板１１とゲート絶縁膜１３に挟まれて形成されているので、絶縁性基板１１側やゲート絶縁膜１３側の表面からの半導体層１５を介してのドレイン電流のリークを防止することができる。また、半導体層１５が絶縁性基板１１とゲート絶縁膜１３に挟まれて形成されているので、半導体装置４０の使用時に外部の雰囲気に曝されることがない。したがって、半導体層１５の有機半導体材料の電気特性を劣化させる水分や酸素との接触や侵入を回避することができ、耐久性を向上することができる。

【０１１８】

なお、半導体装置４０のソース／ドレイン電極１４は、図３（Ａ）～（Ｃ）に示す変形例に係る半導体装置のソース／ドレイン電極１４－１～１４－３の形状を有していてもよい。

【０１１９】

半導体装置４０の製造方法は、ソース／ドレイン電極１４および半導体層１５を先に形成し、その後にゲート絶縁膜１３とゲート電極１２を形成する以外は上述した図５～図８において説明した実施の形態および変形例の製造方法と略同様であるので説明を省略する。

【０１２０】

次に、本実施の形態に係る実施例と本発明によらない比較例について説明する。

【０１２１】

［実施例１］
本実施例では、図２に示す第１の実施の形態に係る半導体装置と同様の構造の有機トランジスタを作製した。
【０１２２】
まず、３０ｍｍ角、厚さ１．１ｍｍのガラス基板（コーニング社製、商品名７０５９）の表面に、真空蒸着装置を用いて厚さ７０ｎｍのアルミニウム膜のゲート電極（ゲート長５０μｍ、ゲート幅２５０μｍ）を形成した。このときの真空度は６．７×10^{-4}Ｐａ（５×10^{-6}Ｔｏｒｒ）、成膜速度は０．３～０．５ｎｍ／秒、基板温度は特に制御せず室温（２５℃）とし、膜厚は真空蒸着装置の水晶振動子によりモニターした。
【０１２３】
次いで、ゲート電極を覆うゲート絶縁膜をシアノエチルプルラン膜（膜厚３００ｎｍ）とポリイミド樹脂膜（膜厚３００ｎｍ）をスピンコート法を用いて順次積層して形成した。なお、このゲート絶縁膜の比誘電率は６であった。
【０１２４】
次いで、ゲート絶縁膜上にソース／ドレイン電極形状の開口部を有するメタルマスクを配置した後、金（Ａｕ）を用いて真空蒸着装置を用いてソース／ドレイン電極を形成した。ソース／ドレイン電極の形状を１ｍｍ×１０ｍｍの矩形とし膜厚を５０ｎｍとした。蒸着の際の真空度は６．７×10^{-4}Ｐａ（５×10^{-6}Ｔｏｒｒ）、成膜速度は０．２～０．３ｎｍ／秒、基板温度は特に制御せず室温（２５℃）とした。反射型光学顕微鏡（オリンパス社製、商品名ＢＨＭＪ－５０）によりこの膜を観察したところ、ソース電極とドレイン電極間距離（チャネル長）は１０μｍ、電極長さ（チャネル幅）は１０ｍｍであった。
【０１２５】
次いで、真空蒸着装置を用いてゲート絶縁膜表面とソース／ドレイン電極を覆うペンタセン（アルドリッチ社製）を用いて半導体層（膜厚１００ｎｍ）を形成した。蒸着の際の真空度４．０×10^{-4}Ｐａ（３×10^{-6}Ｔｏｒｒ）、蒸着源温度２２０℃、成膜速度０．３ｎｍ／秒、基板温度２５℃に設定した。なお、蒸着源温度が２２０℃になるまでに昇華等する蒸気はシャッターを用いて遮断し、被蒸着物に到達しないようにした。
【０１２６】
次いで、ペンタセン膜をソース／ドレイン電極が露出するまでプラズマエッチング装置（出力１００Ｗ、時間９０秒）により研削し、ソース／ドレイン電極上のペンタセン膜が完全に除去されていることを反射型光学顕微鏡（前出）により確認した。以上により実施例１に係る有機トランジスタが得られた。なお、本実施例の有機トランジスタの形成雰囲気は真空蒸着を除いて窒素雰囲気で行った。後述する他の実施例および比較例においても同様である。
【０１２７】
［比較例１］
本発明によらない比較例１の有機トランジスタは、実施例１においてソース／ドレイン電極上のペンタセン膜を除去するプラズマエッチングを行わなかった以外は実施例１と同様にして形成した。
【０１２８】
図１０は実施例１および比較例１の有機トランジスタの特性図であり、０Ｖのゲート電圧V_gに対して、ソース・ドレイン間電圧Ｖｄｓを０Ｖから－２０Ｖまで印加したときにソース・ドレイン間に流れるドレイン電流Ｉｄを示した図である。横軸がソース・ドレイン間電圧Ｖｄｓ、縦軸がドレイン電流Ｉｄを示す。
【０１２９】
図１０を参照するに、ソース・ドレイン間電圧Ｖｄｓが－２０Ｖにおいて比較例１はドレイン・オフ電流が２８０μＡであるのに対して、実施例１はドレイン・オフ電流が２２０μＡであり比較例１よりも低減されていることが分かる。これは、実施例１ではソース／ドレイン電極上のペンタセン膜を除去しているので、ソース／ドレイン電極上のペンタセン膜を介して流れるドレイン・オフ電流の分が低減されているためである。

【０１３０】
なお、電流－電圧特性の測定は窒素雰囲気下で半導体パラメータアナライザー（ヒューレット・パッカード社製、型式：４１４５Ｂ）を使用した。
【０１３１】
［実施例２］
本実施例では、実施例１と同様の構造の有機トランジスタを作製した。
【０１３２】
まず、実施例１と同様にして３０ｍｍ角、厚さ１．１ｍｍのガラス基板（前出）の表面に膜厚７０ｎｍのアルミニウム膜のゲート電極を形成した。
【０１３３】
次いで、ゲート電極を覆うゲート絶縁膜を電子ビーム蒸着法を用いてシリコン酸化膜を（膜厚３００ｎｍ）を形成した。成膜条件は、真空度１．１×10^{-3}Ｐａ（８×10^{-6}Ｔｏｒｒ）、加速電圧４．５ｋＶ、エミッション電流３０ｍＡ、蒸着源温度２２０℃、成膜速度１．６７ｎｍ／秒に設定した。
【０１３４】
次いで、ゲート絶縁膜上に、真空蒸着法によりクロム膜（膜厚１０ｎｍ）／Ａｕ膜（膜厚６０ｎｍ）を順次積層し電極層を形成した。蒸着の際の真空度は６．７×10^{-4}Ｐａ（５×10^{-6}Ｔｏｒｒ）、成膜速度は０．２～０．３ｎｍ／秒、基板温度は特に制御せず室温（２５℃）とした。
【０１３５】
次いで、電極層上にスピンコート法によりポジ型レジスト膜を膜厚約１μｍに形成し、フォトリソグラフィ法を用いてソース電極およびドレイン電極のパターンをパターニングした。
【０１３６】
次いでレジスト膜をマスクとしてＲＩＥ法により電極層をゲート絶縁膜が露出するまでパターニングしてソース／ドレイン電極を形成した。ソース／ドレイン電極の形状を１ｍｍ×１０ｍｍの矩形とし、ソース電極とドレイン電極間距離（チャネル長）は１０μｍ、チャネル幅は１０ｍｍとした。
【０１３７】
次いで、ゲート絶縁膜表面およびパターニングしたレジスト膜上に真空蒸着法を用いてペンタセン（前出）を用いてペンタセン半導体層（膜厚２００ｎｍ）を形成した。蒸着の際の真空度４．０×10^{-4}Ｐａ（３×10^{-6}Ｔｏｒｒ）、蒸着源温度２２０℃、成膜速度０．３ｎｍ／秒、基板温度２５℃に設定した。なお、蒸着源温度が２２０℃になるまでに昇華等する蒸気はシャッターを用いて遮断し、被蒸着物に到達しないようにした。
【０１３８】
次いで、アセトンを用いてレジスト膜およびその表面のペンタセン半導体層をリフトオフし、ソース／ドレイン電極上のペンタセン膜が完全に除去されていることを反射型光学顕微鏡（前出）により確認した。以上により実施例２に係る有機トランジスタが得られた。
【０１３９】
［実施例３］
本実施例では、実施例１と同様の構造の有機トランジスタを作製した。
【０１４０】
まず、実施例２と同様にして、ガラス基板上にアルミニウム膜のゲート電極、シリコン酸化膜のゲート絶縁膜、電極層、ポジ型レジスト膜を順次形成し、ソース／ドレイン電極のパターンをパターニングした。
【０１４１】
パターニングしたレジスト膜をマスクとして、フェノールを主成分とするアルカリ性溶剤を用いて電極層をゲート絶縁膜が露出するまでウェットエッチングを行って、実施例２と同様の形状および寸法のソース／ドレイン電極を形成し、次いでレジスト膜を除去した

。

【０１４２】

次いで、ゲート絶縁膜表面およびソース／ドレイン電極上に真空蒸着法を用いてペンタセン（前出）を用いてペンタセン半導体層（膜厚１００ｎｍ）を形成した。蒸着の際の真空度４．０×１０$^{-4}$Ｐａ（３×１０$^{-6}$Ｔｏｒｒ）、蒸着源温度２２０℃、成膜速度０．３ｎｍ／秒、基板温度２５℃に設定した。なお、蒸着源温度が２２０℃になるまでに昇華等する蒸気はシャッターを用いて遮断し、被蒸着物に到達しないようにした。

【０１４３】

次いで、ペンタセン膜をソース／ドレイン電極が露出するまでプラズマエッチング装置（出力１００Ｗ、時間９０秒）により研削し、ソース／ドレイン電極上のペンタセン膜が完全に除去されていることを反射型光学顕微鏡（前出）により確認した。以上により実施例３に係る有機トランジスタが得られた。

【０１４４】

［比較例２］

本発明によらない比較例２の有機トランジスタは、実施例３においてソース／ドレイン電極上のペンタセン膜を除去するプラズマエッチングを行わなかった以外は実施例３と同様にして形成した。

【０１４５】

図１１は実施例２、３、および比較例１の有機トランジスタの特性図であり、０Ｖのゲート電圧V_Gに対して、ソース・ドレイン間電圧Ｖｄｓを０Ｖから－２０Ｖまで印加したときにソース・ドレイン間に流れるドレイン電流Ｉｄを示した図である。横軸がソース・ドレイン間電圧Ｖｄｓ、縦軸がドレイン電流Ｉｄを示す。

【０１４６】

図１１を参照するに、ソース・ドレイン間電圧Ｖｄｓが－２０Ｖにおいて比較例２はドレイン・オフ電流が２５０μＡであるのに対して、実施例２は１５５μＡ、実施例３は１４０μＡであり、比較例２よりも低減されていることが分かる。このことから、ソース／ドレイン電極上のペンタセン半導体層を除去することにより、この部分ペンタセン半導体層を介して流れるドレイン・オフ電流を防止してドレイン・オフ電流の総量を低減でき、オン・オフ比を向上することができる。

【０１４７】

（第２の実施の形態）

図１２は、本発明の第２の実施の形態に係る液晶表示装置の要部断面図である。図１２を参照するに、本実施の形態の液晶表示装置５０は、透明基板５１と、透明基板５１上に、ＴＦＴアレイ部５２、液晶素子部５３、透明電極部５４、透明基板５５が順次積層された構成となっている。

【０１４８】

透明基板５１、５５は、ガラス基板や、ポリエステル、ポリカーボネート、ポリアリレート、ポリエーテルスルフォン等のプラスチック基板を用いることができる。透明電極部５４は、ＩＴＯ膜、ＺＴＯ膜等の透明な導電性酸化物材料などを用いることができる。

【０１４９】

液晶素子部５３は配向膜／液晶／配向膜から構成され、液晶はその表示方式として、例えば、ツイステッドネマティック（ＴＮ）方式、スーパーツイステッドネマティック（ＳＴＮ）方式、ゲストホスト液晶、高分子分散型液晶（ＰＤＬＣ）など、公知の表示方式を用いることができる。反射型液晶表示装置には明るい白色表示が得られる点でＰＤＬＣが好ましい。

【０１５０】

ＴＦＴアレイ部５２は、透明基板５１上にマトリックス状に配列されたトランジスタ５６と、トランジスタ５６のドレイン電極５８に電気的に接続された画素電極５９と、ゲート電極６０に電気的に接続され、ゲート電圧を供給するゲートバスライン（不図示）と、ソース電極６１に駆動電圧を供給するソースバスライン（不図示）などから構成されてい

る。トランジスタ５６は、透明基板５１上に形成されたゲート電極６０、透明基板５１表面およびゲート電極６０を覆うゲート絶縁膜６２、ゲート絶縁膜６２上に形成された半導体層６３、半導体層上６３に離隔して形成されたソース電極６１およびドレイン電極５８、半導体層６３表面とソース電極６１およびドレイン電極５８を覆う絶縁膜６４から構成されている。

【０１５１】

液晶表示装置５０は、ゲートバスラインおよびソースバスラインを介して信号が供給されることにより選択的にトランジスタ５６がオンとなりドレイン電極５８を介して駆動電圧が画素電極５９に供給され、画素電極５９と透明電極部５４との間の液晶素子部５３の液晶に電界が印加されることにより、透明基板５１の裏面側から入射されるバックライト光の透過あるいは遮断の切り換えが行われ、透明基板５４から出射された光により画像表示が行われる。

【０１５２】

本実施の形態の液晶表示装置５０はＴＦＴアレイ部５２のトランジスタ５６に特徴がある。トランジスタ５６には、第１の実施の形態の半導体装置およびその変形例の半導体装置のいずれかを用いる。具体的には、図１２には、図２に示す第１の実施の形態の半導体装置１０を例に示したが、図３（Ａ）～（Ｃ）に示す変形例に係る半導体装置２０～２２、あるいは図４（Ａ）～（Ｃ）に示す他の変形例に係る半導体装置３０～３２、あるいは図９に示すその他の変形例に係る半導体装置４０を用いてもよい。トランジスタ５６は、上述したようにソース電極６１およびドレイン電極５８の表面が半導体層６３に覆われていないので、ドレイン・オフ電流が抑制されオン／オフ比の向上が図られている。したがって、液晶表示装置５０は表示性能として高いコントラスト比、優れた視認性、および長期信頼性を有している。

【０１５３】

なお、透明基板５５上に公知のカラーフィルターを形成することによりカラー液晶表示装置として用いることができる。

【０１５４】

また、表示装置としては、上記の液晶表示装置５０の液晶素子部５３の替わりに公知の有機ＥＬ（エレクトロルミネッセンス）素子部や電気泳動素子部を用いることにより、それぞれ有機ＥＬ表示装置、電気泳動表示装置としてもよい。

【０１５５】

以上本発明の好ましい実施の形態について詳述したが、本発明は係る特定の実施の形態に限定されるものではなく、特許請求の範囲に記載された本発明の範囲内において、種々の変形・変更が可能である。

【図面の簡単な説明】

【０１５６】

【図１】従来の有機トランジスタの断面図である。

【図２】本発明の第１の実施の形態に係る半導体装置の断面図である。

【図３】（Ａ）～（Ｃ）は第１の実施の形態の変形例に係る半導体装置の断面図である。

【図４】（Ａ）～（Ｃ）は第１の実施の形態の他の変形例に係る半導体装置の断面図である。

【図５】（Ａ）～（Ｄ）は第１の実施の形態の半導体装置の製造工程を示す図である。

【図６】（Ａ）～（Ｃ）は、第１の実施の形態の半導体装置の製造工程の第１変形例を示す図である。

【図７】（Ａ）～（Ｄ）は、第１の実施の形態の半導体装置の製造工程の第２変形例を示す図である。

【図８】（Ａ）～（Ｃ）は、第１の実施の形態の半導体装置の製造工程の第３変形例を示す図である。

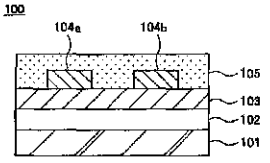
【図９】第１の実施の形態のその他の変形例に係る半導体装置の断面図である。

【図１０】実施例１および比較例１の有機トランジスタの特性図である。

【図１１】実施例２、３、および比較例１の有機トランジスタの特性図である。
【図１２】本発明の第２の実施の形態に係る液晶表示装置の要部断面図である。
【符号の説明】
【０１５７】
１０、２０～２２、３０～３２、４０　半導体装置
１１　絶縁性基板
１２、６０　ゲート電極
１３、６２　ゲート絶縁膜
１４、１４－１～３　ソース／ドレイン電極
１４Ａ　電極層
１５、６３　半導体層
１６、６４　絶縁膜
５０　液晶表示装置
５１、５５　透明基板
５２　ＴＦＴアレイ部
５３　液晶素子部
５４　透明電極部
５６　トランジスタ
５８　ドレイン電極
５９　画素電極
６１　ソース電極

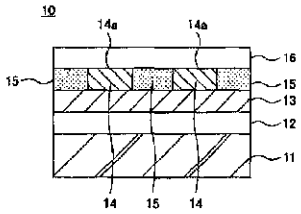
【図１】

従来の有機トランジスタの断面図



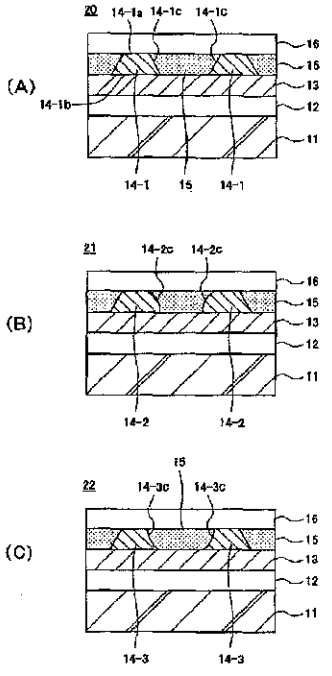
【図２】

本発明の第1の実施の形態に係る半導体装置の断面図



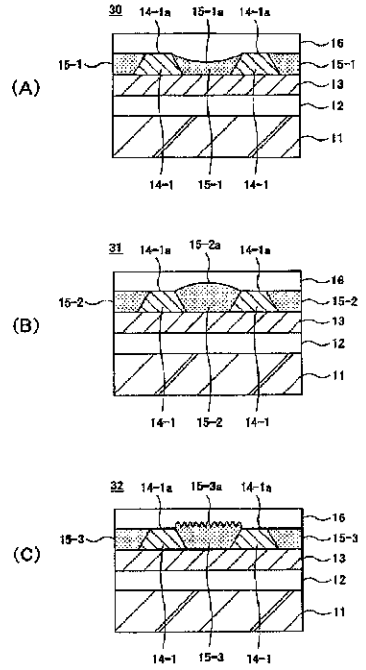
【図３】

第1の実施の形態の変形例に係る半導体装置の断面図



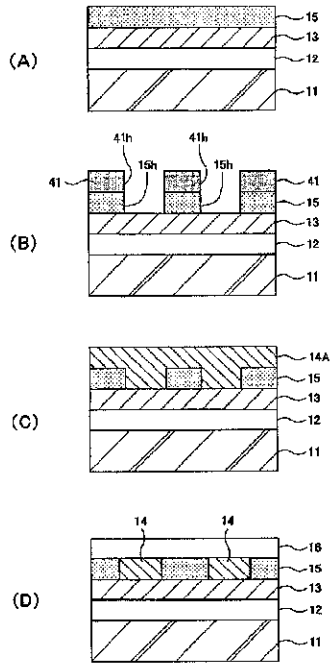
【図４】

第1の実施の形態の他の変形例に係る半導体装置の断面図



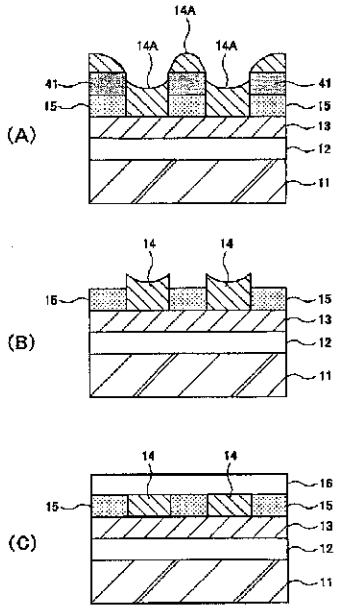
【図５】

第1の実施の形態の半導体装置の製造工程を示す図



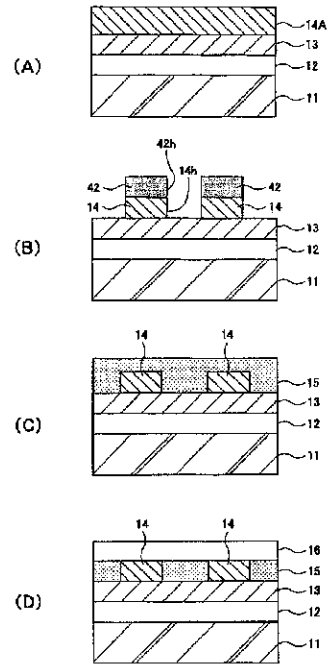
【図６】

第1の実施の形態の半導体装置の製造工程の第1変形例



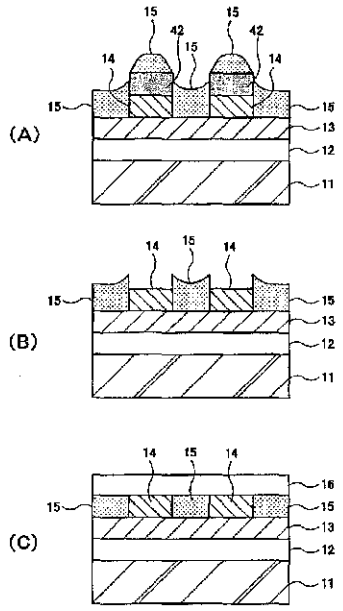
【図７】

第1の実施の形態の半導体装置の製造工程の第2変形例



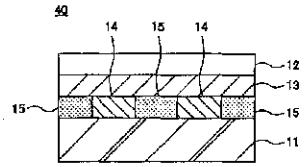
【図８】

第1の実施の形態の半導体装置の製造工程の第3変形例



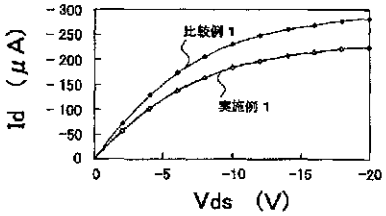
【図９】

第1の実施の形態のその他の変形例に係る半導体装置の断面図



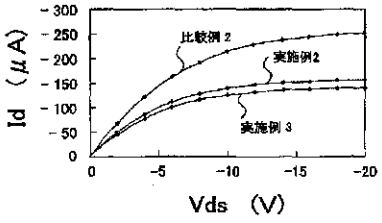
【図１０】

実施例1および比較例1の有機トランジスタの特性図



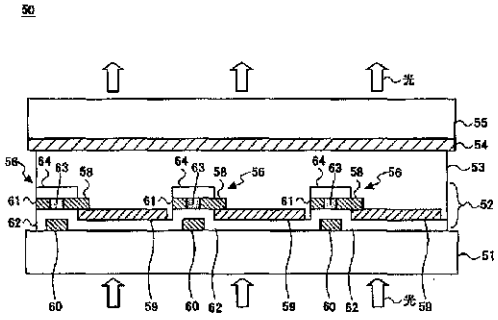
【図１１】

実施例2、3、および比較例1の有機トランジスタの特性図



【図１２】

本発明の第2の実施の形態に係る液晶表示装置の要部断面図



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Bibliographic data: JPH0764112 (A) — 1995-03-10

LIQUID CRYSTAL DISPLAY DEVICE AND ITS PRODUCTION

No documents available for this priority number.

Inventor(s): NISHIKAWA RYUJI ± (NISHIKAWA RYUJI)

Applicant(s): SANYO ELECTRIC CO ± (SANYO ELECTRIC CO LTD)

Classification: - **international:** ***G02F1/1335; G02F1/136; G02F1/1368; H01L29/40; H01L29/78; H01L29/786;*** (IPC1-7): G02F1/1335; G02F1/136; H01L29/40; H01L29/786

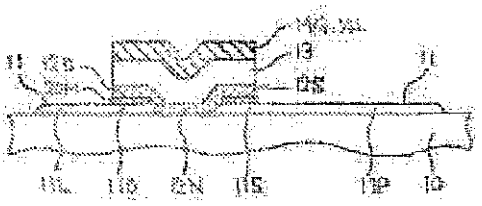
- **cooperative:**

Application number: JP19930214088 19930830

Priority number (s): JP19930214088 19930830

Abstract of JPH0764112 (A)

PURPOSE:To prevent the film defect of a-Si and to stabilize TFT characteristics with the active matrix type liquid crystal display device for which a-SiTFTs of a positive stagger type are used by tapering the edge parts of source-drain wirings consisting of ITO. CONSTITUTION:Mo 20M or Al of an etching rate higher than the etching rate of the ITO 11 is laminated by an etchant consisting of a liquid mixture composed of hydrochloric acid and ferric chloride on an ITO 11 film and is subjected to wet etching of Mo/ITO OR Al/ITO, by which the ITO 11 film is patterned to a tapered shape. The ITO film of the etching rate higher than the etching rate of ordinary ITO films is formed by changing condition setting at the time of sputtering of the ITO 11 and is subjected to wet etching, by which the ITO film is patterned to a tapered shape.



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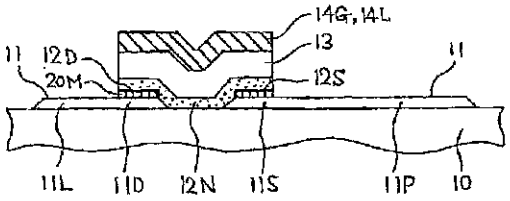
(54)【発明の名称】　液晶表示装置とその製造方法

(57)【要約】

【目的】　正スタガー型のａ－ＳｉＴＦＴを用いたアクティブマトリク液晶表示装置において、ＩＴＯよりなるソース・ドレイン配線のエッジ部をテーパー加工することにより、ａ－Ｓｉの膜欠陥を防止し、ＴＦＴ特性の安定化を達成する。

【構成】　ＩＴＯ（１１）膜上に、塩酸と塩化第２鉄の混合液よりなるエッチャントで、ＩＴＯ（１１）よりもエッチングレートの早いＭｏ（２０Ｍ）またはＡｌ（２０Ａ）を積層し、Ｍｏ／ＩＴＯまたはＡｌ／ＩＴＯのウエットエッチを行うことにより、ＩＴＯ（１１）膜をテーパー状にパターニングする。また、ＩＴＯ（１１）のスパッタリングの際に、条件設定を変えて、通常のＩＴＯ膜上に、それよりもエッチングレートの早いＩＴＯ膜を形成してウエットエッチを行うことにより、ＩＴＯ膜をテーパー状にパターニングする。



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【特許請求の範囲】

【請求項１】　透明な絶縁性基板上にマトリクス状に設けられた表示電極と、前記表示電極の列間に設けられたドレインラインと、前記表示電極の行間に設けられたゲートラインと、

前記ドレインラインと一体のドレイン電極、前記表示電極と一体のソース電極、前記ドレイン電極及び前記ソース電極を覆うａ－Ｓｉ層、前記ゲートラインと一体で、絶縁膜を介して前記ａ－Ｓｉ層に対向して配置されたゲート電極より構成される薄膜トランジスタを有する液晶表示装置であって、

前記ドレイン電極及び前記ソース電極はＩＴＯからなり、エッジ部の断面がテーパー状に形成されており、かつ、前記ドレイン電極と前記ａ－Ｓｉ層の接続部分、及び、前記ソース電極と前記ａ－Ｓｉ層との接続部分には、N^+ａ－Ｓｉ層が介在されていることを特徴とする液晶表示装置。

【請求項２】　透明な絶縁性基板上にマトリクス状に設けられた表示電極と、前記表示電極の列間に設けられたドレインラインと、前記表示電極の行間に設けられたゲートラインと、

前記ドレインラインと接続するドレイン電極、前記表示電極と接続するソース電極、前記ドレイン電極及び前記ソース電極を覆うａ－Ｓｉ層、前記ゲートラインと一体で、絶縁膜を介して前記ａ－Ｓｉ層に対向して配置されたゲート電極より構成される薄膜トランジスタを有する液晶表示装置であって、

前記ドレイン電極及び前記ソース電極は下層がＩＴＯ、上層がＭｏの２層構造からなり、エッジ部の断面がテーパー状に形成されており、かつ、前記ドレイン電極と前記ａ－Ｓｉ層の接続部分、及び、前記ソース電極と前記ａ－Ｓｉ層との接続部分には、N^+ａ－Ｓｉ層が介在されていることを特徴とする液晶表示装置。

【請求項３】　透明な絶縁性基板上にＩＴＯ膜を形成する工程と、該ＩＴＯ膜上にＭｏ膜を形成する工程と、前記Ｍｏ膜及び前記ＩＴＯ膜を塩酸と塩化第２鉄より調合されるエッチャントを用いたフォトエッチで、パターニングすることにより、マトリクス状に配置された表示電極、該表示電極と一体のソース電極、該表示電極の列間に位置するドレインライン、及び、該ドレインラインと一体のドレイン電極を形成する工程と、前記Ｍｏ膜表面にN^+ａ－Ｓｉ層を形成する工程と、これらの上にａ－Ｓｉ層を形成する工程と、該ａ－Ｓｉ層上に絶縁膜を形成する工程と、該絶縁膜上に導電層を形成する工程と、前記導電層、前記絶縁膜、前記ａ－Ｓｉ層、前記N^+ａ－Ｓｉ層及び前記Ｍｏ膜を同一のマスクでパターニングすることにより、前記ソース電極上及び前記ドレイン電極上にN^+ａ－Ｓｉ層、該両N^+ａ－Ｓｉ層を被覆するａ－Ｓｉ層、前記絶縁膜を挟んで前記ａ－Ｓｉ層に対向して配置されるゲート電極、及び該ゲート電極と一体で前記表示電極の行間に設けられるゲートラインを形成するとともに、前記表示電極の前記Ｍｏ膜を除去する工程とを有する液晶表示装置の製造方法。

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【請求項４】　透明な絶縁性基板上にＩＴＯ膜を形成する工程と、該ＩＴＯ膜上にＡｌ膜を形成する工程と、前記Ａｌ膜及び前記ＩＴＯ膜を塩酸と塩化第２鉄より調合されるエッチャントを用いたフォトエッチで、パターニングすることにより、マトリクス状に配置された表示電極、該表示電極と一体のソース電極、該表示電極の列間に位置するドレインライン、及び、該ドレインラインと一体のドレイン電極を形成する工程と、前記ソース電極、前記ドレイン電極及び前記表示電極の前記Ａｌ膜をエッチング除去する工程と、前記ＩＴＯ膜表面にＰをドープする工程と、これらの上にａ－Ｓｉを積層しながら、前記ＩＴＯ膜との界面にN^+ａ－Ｓｉ層を形成する工程と、前記ａ－Ｓｉ層上に絶縁膜を形成する工程と、該絶縁膜上に導電層を形成する工程と、前記導電層、前記絶縁膜、前記ａ－Ｓｉ層及び前記N^+ａ－Ｓｉ層を同一のマスクでパターニングすることにより、前記ソース電極上及び前記ドレイン電極上にN^+ａ－Ｓｉ層、該両N^+ａ－Ｓｉ層を被覆するａ－Ｓｉ層、前記絶縁膜を挟んで前記ａ－Ｓｉ層に対向して配置されるゲート電極、及び該ゲート電極と一体で前記表示電極の行間に設けられるゲートラインを形成する工程とを有する液晶表示装置の製造方法。

【請求項５】　透明な絶縁性基板上にＩＴＯ膜を、所定の温度及び所定の酸素流量でスパッタリングする第１次成長、及び、該第１次成長よりも低い温度、または、該第１次成長よりも少ない酸素流量でスパッタリングする第２次成長よりなる工程と、前記ＩＴＯ膜をパターニングすることにより、マトリクス状に配置された表示電極、該表示電極と一体のソース電極、該表示電極の列間に位置するドレインライン、及び、該ドレインラインと一体のドレイン電極を形成する工程と、前記ＩＴＯ膜表面にＰをドープする工程と、これらの上にａ－Ｓｉを積層しながら、前記ＩＴＯ膜との界面にN^+ａ－Ｓｉ層を形成する工程と、前記ａ－Ｓｉ層上に絶縁膜を形成する工程と、該絶縁膜上に導電層を形成する工程と、前記導電層、前記絶縁膜、前記ａ－Ｓｉ層、前記N^+ａ－Ｓｉ層を同一のマスクでパターニングすることにより、前記ソース電極上及び前記ドレイン電極上にN^+ａ－Ｓｉ層、該両N^+ａ－Ｓｉ層を被覆するａ－Ｓｉ層、前記絶縁膜を挟んで前記ａ－Ｓｉ層に対向して配置されるゲート電極、及び該ゲート電極と一体で前記表示電極の行間に設けられるゲートラインを形成する工程とを有する液晶表示装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、液晶表示装置に関し、特に、歩留まりの向上と特性の安定化を達成した液晶表

示装置に関する。

【０００２】

【従来の技術】液晶表示装置は小型、薄型、低消費電力などの利点があり、ＯＡ機器、ＡＶ機器などの分野で実用化が進んでいる。特に、スイッチング素子として、正スタガー型の薄膜トランジスタ（以下、ＴＦＴと略す）を用いたアクティブマトリクス型は、構造が簡単であるので大画面の動画表示に適し、ディスプレイに使用されている。

【０００３】以下で従来例を図４を参照しながら説明する。まず透明基板（１０）上に表示電極（１１Ｐ）、表示電極（１１Ｐ）と一体のソース電極（１１Ｓ）、ドレインライン（１１Ｌ）及びドレインライン（１１Ｌ）と一体のドレイン電極（１１Ｄ）が、ＩＴＯ（１１）より形成されている。ソース電極（１１Ｓ）とドレイン電極（１１Ｄ）を覆ってはａ－Ｓｉ（１２）が設けられ、更にSiN_xなどのゲート絶縁膜（１３）を挟んで、ゲートライン（１４Ｌ）と一体のゲート電極（１４Ｇ）が、ａ－Ｓｉ（１２）に対向して設けられている。

【０００４】

【発明が解決しようとする課題】表示電極及びソース・ドレイン配線に用いられているＩＴＯ（１１）は、１０００Å程度の厚さに形成されており、また、ａ－Ｓｉ（１２）はＯＦＦ電流の低減のために薄く、５００～１０００Åの程度の厚さにされる。そのため、ＩＴＯ（１１）膜のエッジ部の断面形状によっては、ａ－Ｓｉ（１２）の段切れやａ－Ｓｉ（１２）層とＩＴＯ（１１）膜のコンタクト不良が生じて、ＴＦＴ特性の不安定化や歩留まりの低下につながっていた。

【０００５】本発明の目的は、ａ－Ｓｉ（１２）の膜欠陥を防止し、ａ－Ｓｉ（１２）層とＩＴＯ（１１）膜の良好なコンタクトを得るために、ＩＴＯ（１１）膜のエッジ部の断面形状を改善することにある。

【０００６】

【課題を解決するための手段】本発明は、前記目的を達成するために成され、第１に、透明な絶縁性基板上にマトリクス状に設けられた表示電極と、前記表示電極の列間に設けられたドレインラインと、前記表示電極の行間に設けられたゲートラインと、前記ドレインラインと一体のドレイン電極、前記表示電極と一体のソース電極、前記ドレイン電極及び前記ソース電極を覆うａ－Ｓｉ層、前記ゲートラインと一体で、絶縁膜を介して前記ａ－Ｓｉ層に対向して配置されたゲート電極より構成される薄膜トランジスタを有する液晶表示装置であって、前記ドレイン電極及び前記ソース電極はＩＴＯからなり、エッジ部の断面がテーパー状に形成されており、かつ、前記ドレイン電極と前記ａ－Ｓｉ層の接続部分、及び、前記ソース電極と前記ａ－Ｓｉ層との接続部分には、N^+ａ－Ｓｉ層が介在されている構造である。

【０００７】第２に、透明な絶縁性基板上にマトリクス状に設けられた表示電極と、前記表示電極の列間に設けられたドレインラインと、前記表示電極の行間に設けられたゲートラインと、前記ドレインラインと接続するドレイン電極、前記表示電極と接続するソース電極、前記ドレイン電極及び前記ソース電極を覆うａ－Ｓｉ層、前記ゲートラインと一体で、絶縁膜を介して前記ａ－Ｓｉ層に対向して配置されたゲート電極より構成される薄膜トランジスタを有する液晶表示装置であって、前記ドレイン電極及び前記ソース電極は下層がＩＴＯ、上層がＭｏの２層構造からなり、エッジ部の断面がテーパー状に形成されており、かつ、前記ドレイン電極と前記ａ－Ｓｉ層の接続部分、及び、前記ソース電極と前記ａ－Ｓｉ層との接続部分には、N^+ａ－Ｓｉ層が介在されている構造である。

【０００８】第３に、透明な絶縁性基板上にＩＴＯ膜を形成する工程と、該ＩＴＯ膜上にＭｏ膜を形成する工程と、前記Ｍｏ膜及び前記ＩＴＯ膜を塩酸と塩化第２鉄より調合されるエッチャントを用いたフォトエッチで、パターニングすることにより、マトリクス状に配置された表示電極、該表示電極と一体のソース電極、該表示電極の列間に位置するドレインライン、及び、該ドレインラインと一体のドレイン電極を形成する工程と、前記Ｍｏ膜表面にN^+ａ－Ｓｉ層を形成する工程と、これらの上にａ－Ｓｉ層を形成する工程と、該ａ－Ｓｉ層上に絶縁膜を形成する工程と、該絶縁膜上に導電層を形成する工程と、前記導電層、前記絶縁膜、前記ａ－Ｓｉ層、前記N^+ａ－Ｓｉ層及び前記Ｍｏ膜を同一のマスクでパターニングすることにより、前記ソース電極上及び前記ドレイン電極上にN^+ａ－Ｓｉ層、該両N^+ａ－Ｓｉ層を被覆するａ－Ｓｉ層、前記絶縁膜を挟んで前記ａ－Ｓｉ層に対向して配置されるゲート電極、及び該ゲート電極と一体で前記表示電極の行間に設けられるゲートラインを形成するとともに、前記表示電極の前記Ｍｏ膜を除去する工程とを有する製造方法である。

【０００９】第４に、透明な絶縁性基板上にＩＴＯ膜を形成する工程と、該ＩＴＯ膜上にＡｌ膜を形成する工程と、前記Ａｌ膜及び前記ＩＴＯ膜を塩酸と塩化第２鉄より調合されるエッチャントを用いたフォトエッチで、パターニングすることにより、マトリクス状に配置された表示電極、該表示電極と一体のソース電極、該表示電極の列間に位置するドレインライン、及び、該ドレインラインと一体のドレイン電極を形成する工程と、前記ソース電極、前記ドレイン電極及び前記表示電極の前記Ａｌ膜をエッチング除去する工程と、前記ＩＴＯ膜表面にＰをドープする工程と、これらの上にａ－Ｓｉを積層しながら、前記ＩＴＯ膜との界面にN^+ａ－Ｓｉ層を形成する工程と、前記ａ－Ｓｉ層上に絶縁膜を形成する工程と、該絶縁膜上に導電層を形成する工程と、前記導電層、前記絶縁膜、前記ａ－Ｓｉ層、前記N^+ａ－Ｓｉ層を同一のマスクでパターニングすることにより、前記ソ

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ース電極上及び前記ドレイン電極上にN^+ａ－Ｓｉ層、該両N^+ａ－Ｓｉ層を被覆するａ－Ｓｉ層、前記絶縁膜を挟んで前記ａ－Ｓｉ層に対向して配置されるゲート電極、及び該ゲート電極と一体で前記表示電極の行間に設けられるゲートラインを形成する工程とを有する製造方法である。

【００１０】第５に、透明な絶縁性基板上にＩＴＯ膜を、所定の温度及び所定の酸素流量でスパッタリングする第１次成長、及び、該第１次成長よりも低い温度、または、該第１次成長よりも少ない酸素流量でスパッタリングする第２次成長よりなる工程と、前記ＩＴＯ膜をパターニングすることにより、マトリクス状に配置された表示電極、該表示電極と一体のソース電極、該表示電極の列間に位置するドレインライン、及び、該ドレインラインと一体のドレイン電極を形成する工程と、前記ＩＴＯ膜表面にＰをドープする工程と、これらの上にａ－Ｓｉを積層しながら、前記ＩＴＯ膜との界面にN^+ａ－Ｓｉ層を形成する工程と、前記ａ－Ｓｉ層上に絶縁膜を形成する工程と、該絶縁膜上に導電層を形成する工程と、前記導電層、前記絶縁膜、前記ａ－Ｓｉ層、前記N^+ａ－Ｓｉ層を同一のマスクでパターニングすることにより、前記ソース電極上及び前記ドレイン電極上にN^+ａ－Ｓｉ層、該両N^+ａ－Ｓｉ層を被覆するａ－Ｓｉ層、前記絶縁膜を挟んで前記ａ－Ｓｉ層に対向して配置されるゲート電極、及び該ゲート電極と一体で前記表示電極の行間に設けられるゲートラインを形成する工程とを有する製造方法である。

【００１１】

【作用】表示電極及びソース・ドレイン配線の材料となるＩＴＯ（１１）上に、Ｍｏ（２０Ｍ）又はＡｌ（２０Ａ）を積層することにより、下層のエッチングレートが遅く、上層のエッチングレートが早い２層構造となる。すなわち、パターニングにおいて、塩酸と塩化第２鉄を調合して得られるエッチャントを用いることにより、Ｍｏ／ＩＴＯまたはＡｌ／ＩＴＯのエッチングレート比を５程度に設定したウエットエッチングを行うことができる。これにより、界面を境にして、上層のＭｏ（２０Ｍ）又はＡｌ（２０Ａ）のエッチングが下層のＩＴＯ（１１）よりも早く進むため、エッジ部においてＩＴＯ（１１）膜の断面はテーパー形状に加工することができる。

【００１２】また、ＩＴＯ（１１）を成膜する際、通常のスパッタリングを行った後、温度を下げる、または、O_2の流量を下げるなどの条件を変えたスパッタリングを行うことにより、上層のエッチングレートが下層よりも早いＩＴＯ（１１）膜が得られる。この膜をウエットエッチすることによっても、同様にエッジ部をテーパー加工することができる。

【００１３】

【実施例】以下で、本発明の第１の実施例を図１を参照

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しながら説明する。まず透明基板（１０）上に、スパッタリングによりＩＴＯ（１１）を約１０００Åの厚さに積層し、続いて、Ｍｏ（２０Ｍ）を約５００Åの厚さに積層する。次に、塩酸と塩化第２鉄の混合液で、Ｍｏ／ＩＴＯのエッチングレート比が５程度になるように調整したエッチャントでウエットエッチングを行って、パターニングする。これにより、表示電極（１１Ｐ）、ドレインライン（１１Ｌ）、及び表示電極（１１Ｐ）と一体のソース電極（１１Ｓ）、ドレインライン（１１Ｌ）と一体のドレイン電極（１１Ｄ）のパターンが、エッジ部の断面がテーパー状になって形成される。

【００１４】次に、プラズマＣＶＤ装置において、SiH_3中にPH_3を１％含んだ材料ガスを高周波グロー放電により活性化することによる膜成長と、H_2のプラズマ照射を交互に繰り返すことにより、Ｍｏ（２０Ｍ）の表面に、選択的にN^+ａ－Ｓｉ薄膜が形成される。引き続き、プラズマＣＶＤによりａ－Ｓｉ（１２Ｎ）を５００～１０００Å、ゲート絶縁膜（１３）としてSiN_xを２０００～４０００Å程度の厚さに順次積層する。次に、ゲート配線材料として、例えばＡｌをスパッタリングなどにより５０００Å程度の厚さに積層する。そして、Ａｌ、SiN_x、ａ－Ｓｉ、N^+ａ－Ｓｉ及びＭｏを同一マスクでパターニングすることにより、Ｍｏ／ＩＴＯの積層体でなるソース及びドレイン電極（１１Ｓ，１１Ｄ）、ソース及びドレイン電極（１１Ｓ，１１Ｄ）上に、それぞれのコンタクト層となるN^+ａ－Ｓｉ（１２Ｓ，１２Ｄ）、チャンネル層として両N^+ａ－Ｓｉ（１２Ｓ，１２Ｄ）を被覆するａ－Ｓｉ（１２Ｎ）、更に、SiN_xのゲート絶縁膜（１３）を挟んで、ａ－Ｓｉ（１２Ｎ）に対向するゲート電極（１４Ｇ）、及び、ゲート電極（１４Ｇ）と一体で、ゲート絶縁膜（１３）を介して、ドレインライン（１１Ｌ）と交差するゲートライン（１４Ｌ）がＡｌにより形成されるとともに、表示電極（１１Ｐ）とドレインライン（１１Ｌ）のＭｏ（２０Ｍ）が除去されて、ＩＴＯ（１１）の１層となり、図１の構造が得られる。

【００１５】上で述べたように、ソース電極（１１Ｓ）及びドレイン電極（１１Ｄ）となっているＩＴＯ（１１）膜は、エッジ部がテーパー状の断面を有しているため、ａ－Ｓｉ層（１２Ｎ）は良好なステップカヴァレッジをもって被覆される。そのため、ＩＴＯ（１１）膜の段差の影響が緩和され、膜欠陥などによるＴＦＴ特性の悪化が防止される。

【００１６】また、ＩＴＯ（１１）膜上のＭｏ（２０Ｍ）膜は、ＩＴＯ（１１）膜のテーパー加工と同時に、コンタクト層の形成のために設けられる。そのため、Ｍｏ（２０Ｍ）膜の段差がａ－Ｓｉ（１２Ｎ）の欠陥の原因にならないように薄く形成している。また、製造過程において、マスクを１枚増やして、Ｍｏ（２０Ｍ）のパターニングを、別のマスクで行って、ドレインライン

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（11L）上にも残すことにより、Mo／ITOの2層構造とし、ドレイン配線の低抵抗化を図ることができる。

【0017】以下で、ITO膜のテーパー加工についての他の実施例について説明する。図2は本発明の第2の実施例である。透明基板（10）上に、スパッタリングによりITO（11）を約1000Åの厚さに積層し、続いて、Al（20A）を約500Åの厚さに積層する。次に、塩酸と塩化第2鉄の混合液で、Al／ITOのエッチングレート比が5程度になるように調整したエッチャントを用いて、ウエットエッチングによるパターニングを行う。これにより、表示電極（11P）、ドレインライン（11L）、ソース電極（11S）、及びドレイン電極（11D）のパターンが、エッジ部の断面がテーパー状になって形成される。そして、ドレインライン（11L）以外の全てのAl（20A）をエッチング除去することにより、表示電極（11P）、ソース電極（11S）及びドレイン電極（11D）をITO（11）の1層とし、ドレインライン（11L）をAl／ITOの2層構造とする。これにより、ドレイン配線が低抵抗化される。また、マスク数減のためAl（20A）を全てエッチングしてもよい。

【0018】次に、プラズマCVD装置を用いた、PH_3ガスの高周波グロー放電により、ITO（11）膜の表面にPをドープし、引き続き、a－Siの膜形成を行うことにより、同時に、ITO（11）とa－Siの界面に選択的にN^+a－Si薄膜が形成される。続いて、SiN_x、Alを順次積層した後、パターニングすることにより、ITOでなるソース及びドレイン電極（11S，11D）、ソース及びドレイン電極（11S，11D）上に、それぞれのコンタクト層となるN^+a－Si（12S，12D）、チャンネル層として両N^+a－Si（12S，12D）を被覆するa－Si（12N）、更に、SiN_xのゲート絶縁膜（13）を挟んで、a－Si（12N）に対向するゲート電極（14G）、及び、ゲート電極（14G）と一体で、ゲート絶縁膜（13）を介して、ドレインライン（11L）と交差するゲートライン（14L）がAlにより形成されて、図2の構造が得られる。

【0019】次に、本発明の第3の実施例を図3を参照しながら説明する。透明基板（10）上に、ITO（11）のスパッタリングを、温度285℃、酸素流量1.5sccmの条件下で行って、1000Å程度の厚さに第1次成長した後、条件を温度150～200℃、酸素流量1.0sccm以下に変えて、500Å程度の厚さに第2次成長する。これにより、エッチングレートが、第1次成長により形成された下層よりも、第2次成長により形成された上層の方が早くなるので、第1及び第2の実施例と同様に、ウエットエッチングで表示電極（11P）、ドレインライン（11L）、ソース電極（11S）及びドレイン電極（11D）のパターン形成を行えば、エッジ部の断面がテーパー状に加工される。

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【0020】後は、第2の実施例と同様に、ITO（11）膜表面にPをドープした後、a－Si（12N）を成膜し、SiN_x、Alを積層し、パターニングを行うことにより、2層のITOよりなるソース・ドレイン電極（11S，11D）及びドレインライン（11L）、N^+a－Si（12S，12D）、a－Si（12N）、ゲート絶縁膜（13）、ゲート電極（14G）、及び、ゲートライン（14L）が形成されて、図3の構造が得られる。

【0021】

【発明の効果】以上の説明から明らかなように、ITOからなるソース・ドレイン配線及び表示電極のパターン形成を行う際、ITOと同じエッチャントでエッチングでき、かつ、ITOよりもエッチングレートが早いMo、Alなどと組み合わせることにより、エッジ部をテーパー加工できる。これにより、チャンネル領域において、a－Si層の膜欠陥が防止され、安定なTFT特性が得られた。特に、Moは、その表面に選択的にN^+a－Si薄膜をプラズマ成膜できるので、Moと同一のマスクでパターニングすることにより、マスク数が減らせる。

【0022】また、MoまたはAlをa－Siと別のマスクでパターニングして、ドレインライン上に残して、ITOとの2層構造にすることにより、ドレインを低抵抗化できた。また、ITO膜のスパッタリングの際に、条件設定を変えて、通常のITO膜上に、それよりもエッチングレートの早い膜を形成して、パターニングすることによっても、エッジ部をテーパー状に加工できた。更に、ITO表面にPをプラズマドープすることにより、a－Siのプラズマ成膜中に、ITO上にN^+a－Si薄膜を選択的に形成できるので、N^+a－Si用のマスクが不要になった。

【図面の簡単な説明】

【図1】本発明の第1の実施例である液晶表示装置の断面図である。

【図2】本発明の第2の実施例である液晶表示装置の断面図である。

【図3】本発明の第3の実施例である液晶表示装置の断面図である。

【図4】従来の液晶表示装置の断面図である。

【符号の説明】

10　透明基板
11　ITO
11P　表示電極
11L　ドレインライン
11S　ソース電極
11D　ドレイン電極
12N　a－Si

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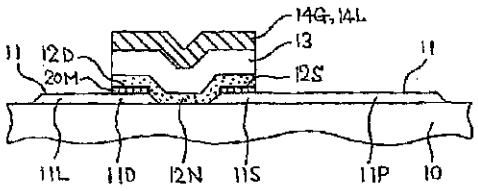
12S，12D　N⁺a－Si
13　ゲート絶縁膜
14G　ゲート電極

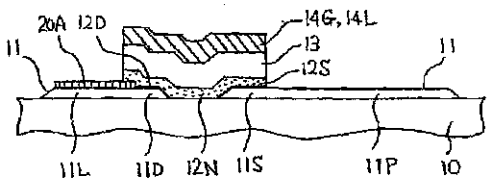
10

＊14L　ゲートライン
20M　Mo
＊　20A　Al

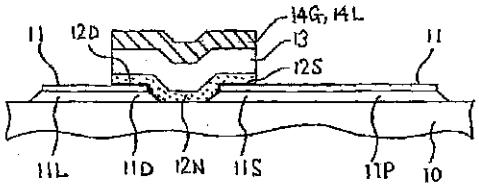
【図1】



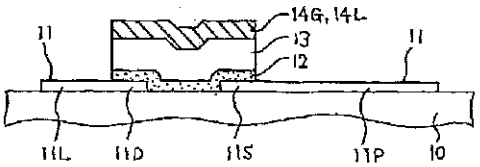
【図2】



【図3】



【図4】



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Information:					
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Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	30392 7fbfe91d7acd1d675b0114ba2050e816194a533e	no	2
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☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
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AMENDMENT	03/20/2014	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
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	☐ Application Size Fee (37 CFR 1.16(s))						
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						TOTAL ADD'L FEE	0

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	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
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2896	

DATE MAILED: 03/31/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/763,874	02/11/2013	Shunpei YAMAZAKI	0756-10065	7085

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/30/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31780 7590 03/31/2014
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

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13/763,874	02/11/2013	Shunpei YAMAZAKI	0756-10065	7085

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APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/30/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
JOY, JEREMY J	2896	257-057000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

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13/763,874	02/11/2013	Shunpei YAMAZAKI	0756-10065	7085

31780 7590 03/31/2014

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

EXAMINER	
JOY, JEREMY J	

ART UNIT	PAPER NUMBER
2896	

DATE MAILED: 03/31/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/763,874	Applicant(s) YAMAZAKI ET AL.	
	Examiner JEREMY JOY	Art Unit 2896	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the response after final action mailed on 03/20/2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *10-25*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 03/20/2014
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/CHEUNG LEE/ Primary Examiner, Art Unit 2896	/JEREMY JOY/ Examiner, Art Unit 2896

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment to the claims filed on 03/20/2014 has been acknowledged and entered. Claims 2-8 have been.

Allowable Subject Matter

2. Claims **10-25** are allowed over the prior art.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

3. Claims **10-25** are allowed because the prior art of record neither anticipate nor rendered obvious the limitations of base claims 10 including "wherein each of a side surface of the source electrode and a side surface of the drain electrode has a step in the lower portion thereof, wherein the first angle of the step that is made between the side surface of the source electrode and an upper surface of the glass substrate is greater than or equal to 20° and less than 90°, and wherein a second angle of the step that is made between the side surface of the drain electrode and the upper surface of the glass substrate is greater than or equal to 20° and less than 90°" and the limitations of base claim 18 including "wherein the first angle between a surface of the glass

substrate and a side surface of a first bottom edge of the source electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the source electrode, and wherein the second angle between a surface of the glass substrate and a side surface of a first bottom edge of the drain electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the drain.". In particular, the prior art of record falls short with regards to teaching that the source and drain electrodes have a step on the side surfaces of them and wherein the step comprises two different angles in relationship to the substrate.

In example:

(i) *Akimoto* (**U.S. Patent Pub. No. 2007/0108446**) teaches a glass substrate; a transistor over the glass substrate, the transistor comprising: a gate electrode; a first insulating layer over the gate electrode; an oxide semiconductor layer over the first insulating layer; and a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer; a first buffer layer between the oxide semiconductor layer and the source electrode and a second buffer layer between the oxide semiconductor layer and the drain electrode; a second insulating layer over the transistor; a pixel electrode over the second insulating layer; a third insulating layer over the pixel electrode; a light emitting layer over the pixel electrode and the third insulating layer; and an electrode over the light emitting layer, wherein each of the first buffer layer and the second buffer layer has a lower resistivity than the oxide semiconductor layer,

but fails to specifically teach wherein each of the side surface of the source electrode and a side surface of the drain electrode has a tapered shape and more specifically wherein the side surface of the source and drain electrodes has a step and the specifics of said step as mentioned above.

(ii) *Kawasaki et al.* (**U.S. 2005/0056897**) teaches source and drain electrodes wherein a first angle formed a first angle between a surface of the substrate and a side surface of a first bottom edge of the source electrode and a second angle between the surface of the substrate and a side surface of a second bottom edge of the drain electrode are each greater than or equal to 20° and less than 90°, but fails to specifically teach wherein the side surface of the source and drain electrodes has a step and the specifics of said step as mentioned above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEREMY JOY whose telephone number is (571)270-7445. The examiner can normally be reached on Monday - Friday, 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Such can be reached on (571)-272-8895. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JEREMY JOY/
Examiner, Art Unit 2896
March 23, 2014

/CHEUNG LEE/
Primary Examiner, Art Unit 2896

Notice of References Cited	Application/Control No. 13/763,874	Applicant(s)/Patent Under Reexamination YAMAZAKI ET AL.	
	Examiner JEREMY JOY	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2007/0072439	03-2007	Akimoto et al.	438/795
*	B	US-2007/0108446	05-2007	Akimoto, Kengo	257/061
*	C	US-2007/0172591	07-2007	SEO et al.	427/248.1
*	D	US-2008/0038882	02-2008	Takechi et al.	438/151
*	E	US-2010/0117086	05-2010	AKIMOTO et al.	257/57
*	F	US-2009/0114917	05-2009	YAMAZAKI et al.	257/59
*	G	US-2010/0044711	02-2010	IMAI, Shinji	257/59
*	H	US-2005/0056897	03-2005	Kawasaki et al.	257/359
*	I	US-2006/0027804	02-2006	Yamazaki et al.	257/059
*	J	US-2006/0292726	12-2006	Akimoto et al.	438/030
*	K	US-2008/0073653	03-2008	Iwasaki, Tatsuya	257/79
*	L	US-2006/0033098	02-2006	Shih et al.	257/040
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13763874	YAMAZAKI ET AL.
	Examiner	**Art Unit**
	JEREMY JOY	2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/12/2013	12/11/2013	03/23/2014						
-	1	-	-	-						
-	2	✓	✓	-						
-	3	✓	✓	-						
-	4	✓	✓	-						
-	5	✓	✓	-						
-	6	✓	✓	-						
-	7	✓	✓	-						
-	8	✓	✓	-						
-	9	✓	-	-						
1	10	=	=	=						
2	11	=	=	=						
3	12	=	=	=						
4	13	=	=	=						
5	14	=	=	=						
6	15	=	=	=						
7	16	=	=	=						
8	17	=	=	=						
9	18	=	=	=						
10	19	=	=	=						
11	20	=	=	=						
12	21	=	=	=						
13	22	=	=	=						
14	23	=	=	=						
15	24	=	=	=						
16	25	=	=	=						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13763874	YAMAZAKI ET AL.
	Examiner	Art Unit
	JEREMY JOY	2896

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	59, e21.535	3/23/2014	Jeremy J. Joy
438	149, 158	3/23/2014	Jeremy J. Joy

SEARCH NOTES		
Search Notes	Date	Examiner
Spoke with primary, Cheung Lee, regarding this application.	7/25/2013	Jeremy J. Joy
See search history of parent application 12/613,769	8/12/2013	Jeremy J. Joy
General keyword and EAST search is attached.	8/12/2013	Jeremy J. Joy
General keyword and EAST search is attached.	12/18/2013	Jeremy J. Joy
General keyword, interference and EAST search is attached.	3/23/2014	Jeremy J. Joy

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	57	3/23/2014	Jeremy J. Joy

/JEREMY JOY/ Examiner.Art Unit 2896	March 23, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

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BIB DATA SHEET

CONFIRMATION NO. 7085

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/763,874	02/11/2013 RULE	257	2896	0756-10065

APPLICANTS
SEMICONDUCTOR ENERGY LABORATORY CO., LTD., Atsugi-shi, JAPAN

INVENTORS
Shunpei YAMAZAKI, Setagaya, JAPAN;
Kengo AKIMOTO, Atsugi, JAPAN;
Daisuke KAWAE, Yamato, JAPAN;

**** CONTINUING DATA ***********************
This application is a CON of 12/613,769 11/06/2009 PAT 8373164 *
which is a CON of 12/606,262 10/27/2009 ABN
(*)Data provided by applicant is not consistent with PTO records.

**** FOREIGN APPLICATIONS ***********************
JAPAN 2008-287187 11/07/2008

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/04/2013

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☑ Yes ☐ No	☑ Yes ☐ No	/JEREMY J JOY/ Examiner's Signature	☐ Initials	JAPAN	37	24	3

ADDRESS
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033
UNITED STATES

TITLE
SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
2060	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	6765	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2014/03/23 19:33
L5	395	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2014/03/23 19:33
L6	87	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2014/03/23 19:33
L7	7028	L4 L5 L6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/23 19:33
L8	151627	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2014/03/23 19:33
L9	13059	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2014/03/23 19:33
L10	2067	L8 and L9	US-PGPUB; USPAT; USOCR	OR	ON	2014/03/23 19:33
L11	680	L7 and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/23 19:33
L12	9	"2008205451"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/23 19:34
L13	10	"2005223049"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/23 19:34
L14	3	"07064112"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2014/03/23 19:34

			IBM_TDB			
L18	13059	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2014/03/23 19:57
L19	6584	(257/59).CCLS.	US-PGPUB; USPAT	OR	OFF	2014/03/23 19:57
L20	48	((angle taper gradation stair) near3 (source drain)) and L18 and L19	US-PGPUB; USPAT; USOCR	OR	ON	2014/03/23 19:57
L21	4077	(438/149).CCLS.	US-PGPUB; USPAT	OR	OFF	2014/03/23 19:57
L22	18	((angle taper gradation stair) near3 (source drain)) and L18 and L21	US-PGPUB; USPAT; USOCR	OR	ON	2014/03/23 19:57
L23	1947	(438/158).CCLS.	US-PGPUB; USPAT	OR	OFF	2014/03/23 19:58
L24	17	((angle taper gradation stair) near3 (source drain)) and L18 and L23	US-PGPUB; USPAT; USOCR	OR	ON	2014/03/23 19:58
L25	17	L24	US-PGPUB; USPAT; USOCR	OR	ON	2014/03/23 19:58
L26	320	(257/e21.535).CCLS.	US-PGPUB; USPAT	OR	OFF	2014/03/23 19:58
L27	72	20 22 24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/23 19:58
S1	2	"US 20100117077"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 14:18
S2	1806	"257/43".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S3	128	"257/E21.459".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S4	1431	"438/158".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S5	537	"257/E29.296".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S6	1194	"257/57".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S7	1225	"438/104".CCLS.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:32
S8	5416	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:35
S9	274	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:35
S10	54	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2012/04/04 14:36
S11	109	("20080128689" | "20030189401" | "20080308796" | "20080308806" | "7061014" | "20060110867" |	US-PGPUB; USPAT	OR	ON	2012/04/04 14:36

		"20060284172" | "20080258141" | "20090068773" | "7323368" | "20060244107" | "5847410" | "6563174" | "20020132454" | "20060231882" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090152541" | "6294274" | "7402506" | "7411209" | "20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "5731856" | "7385224" | "7462862" | "7732819" | "20080203387" | "20090008639" | "20100025678" | "20030218222" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080254569" | "20080258140" | "20090278122" | "20090280600" | "7049190" | "20070172591" | "20080296568" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "7211825" | "7453065" | "6532045" | "7674650" | "20080182358" | "20090073325" | "7453087" | "7501293" | "20070072439" | "20070158652" | "7298084" | "20070187760" | "20080308797" | "5744864" | "6586346" | "6727522" | "6960812" | "7301211" | "20060035452" | "20060108636" | "20060113549" | "20060197092" | "20070090365" | "20080166834" | "20090134399" | "7064346" | "7282782" | "7468304" | "20070108446" | "20070272922" | "20080308804" | "20080308805" | "20090065771" | "20040038446" | "20040127038" | "20050017302" | "20050199959" | "20060043377" | "20060113536" | "20060170111" | "20070046191" | "20070252928" | "20080073653" | "20080129195" | "20080258143" | "20090114910" | "7105868" | "7297977" | "7323356").PN.				
S12	6	"2007123861"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/04 14:47
S13	7	"2007096055"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/04/04 14:47

S14	41	("20020153587" | "20030013261" | "20030047785" | "20030111663" | "20030207502" | "20030218221" | "20030218222" | "20030219530" | "20040023432" | "4887255" | "5744864" | "6225655" | "6255130" | "6362499" | "6563174" | "7067843").PN. OR ("7282782").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:20
S15	51	("20020171085" | "20030047785" | "20030111663" | "20030218221" | "20030218222" | "20040023432" | "20040127038" | "20050017244" | "3294660" | "5289016" | "5744864" | "6362499" | "6391462" | "6727522").PN. OR ("7297977").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:21
S16	132	("20010046027" | "20020056838" | "20020109796" | "20020132454" | "20040038446" | "20040127038" | "20040132293" | "20050017302" | "20050199959" | "20050259206" | "20050275038" | "20060035452" | "20060086933" | "20060091793" | "20060108529" | "20060108636" | "20060110867" | "20060113536" | "20060113539" | "20060113549" | "20060113565" | "20060163743" | "20060169973" | "20060170067" | "20060170111" | "20060197092" | "20060208977" | "20060228974" | "20060231882" | "20060238135" | "20060244107" | "20060284171" | "20060284172" | "20060286737" | "20060292777" | "20070024187" | "20070046191" | "20070052025" | "20070054507" | "20070072439" | "20070090365" | "20070108446" | "20070158652" | "20070172591" | "20070187678" | "20070187760" | "20070194379" | "20070252928" | "20070272922" | "20070287296" | "20080006877" | "20080038882" | "20080038929" | "20080050595" | "20080073653" | "20080083950" | "20080106191" | "20080128689" | "20080129195" | "20080166834" | "20080182358" | "20080198108" | "20080224133" | "20080254569" | "20080258139" | "20080258140" | "20080258141" | "20080258143" | "20080308796" | "20080308797" | "20080308804" | "20080308805" | "20080308806" | "20090008639" | "20090073325" | "20090114910" | "20090114911" | "20090134399" | "20090152541" | "20090153762" | "20090186437" | "20090186445" | "20090189155" | "20090189156" | "5530265" | "5696011" | "5701167" | "5731856" | "5817548" | "6294274" | "6532045" | "6674136" | "6727522" | "6852998" | "6900461" | "7009204" | "7049190").PN. OR ("7061014" | "7064346" | "7075614" | "7105868" |	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:23

		"7211825" | "7282782" | "7297977" | "7323356" | "7402506" | "7411209" | "7453065" | "7453087" | "7462862" | "7468304" | "7501293").PN. OR ("7674650").URPN.				
S17	9604	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:25
S18	4685	S17 and ((semiconductor adj oxide) ((zinc indium gallium zn in ga) adj oxide))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:25
S19	322	(((semiconductor adj oxide) ((zinc indium gallium zn in ga) adj oxide)) near3 channel)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:26
S20	118	S17 and S19	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:26
S21	1	("7638360").PN.	US-PGPUB; USPAT	OR	OFF	2012/04/04 16:33
S22	7	("20050017302" | "20060244107" | "20070048970" | "20070072439" | "20070184571" | "20080254569").PN. OR ("7638360").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:33
S23	2	"US 8134156"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 16:36
S24	3	"US 20070108446"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 16:36
S25	177	("20010046027" | "20020011978" | "20020044111" | "20020056838" | "20020106839" | "20020109796" | "20020110703" | "20020132454" | "20030047785" | "20030207506" | "20030218222" | "20040038446" | "20040127038" | "20040132293" | "20040252270" | "20050017302" | "20050082541" | "20050084999" | "20050104071" | "20050164423" | "20050199959" | "20050231107" | "20050233509" | "20050250308" | "20050259206" | "20050275038" | "20060035452" | "20060043377" | "20060054888" | "20060086933" | "20060091793" | "20060108529" | "20060108636" | "20060110867" | "20060113536" | "20060113539" | "20060113549" | "20060113565" | "20060163743" | "20060169973" | "20060170067" | "20060170111" | "20060183274" | "20060197092" | "20060208977" | "20060228974" | "20060231882" | "20060238135" | "20060244107" | "20060249733" | "20060284171" | "20060284172" | "20060286737" | "20060292777" | "20070024187" | "20070046191" | "20070052025" | "20070054507" | "20070072439" | "20070090365" |	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:36

		"20070108446" | "20070141784" | "20070152217" | "20070158652" | "20070172591" | "20070187678" | "20070187760" | "20070194379" | "20070238228" | "20070252928" | "20070272922" | "20070287296" | "20080006877" | "20080038882" | "20080038929" | "20080050595" | "20080073653" | "20080083950" | "20080106191" | "20080108198" | "20080128689" | "20080129195" | "20080166834" | "20080174710" | "20080182358" | "20080198108" | "20080224133" | "20080254569" | "20080258139" | "20080258140" | "20080258141" | "20080258143" | "20080308796").PN. OR ("20080308797" | "20080308804" | "20080308805" | "20080308806" | "20090008639" | "20090068773" | "20090073325" | "20090114910" | "20090114911" | "20090134399" | "20090152541" | "20090153762" | "20090186437" | "20090186445" | "20090189155" | "20090189156" | "20090239335" | "20090278122" | "20090280600" | "20090305461" | "20100003783" | "20100038639" | "20100085283" | "20100240157" | "20110012119" | "20110024787" | "5382457" | "5530265" | "5696011" | "5701167" | "5731856" | "5803975" | "5817548" | "5888410" | "5930607" | "5952708" | "5994157" | "6294274" | "6459418" | "6529251" | "6532045" | "6563174" | "6674136" | "6727522" | "6819368" | "6852998" | "6900461" | "6921627" | "7009204" | "7012658" | "7049190" | "7061014" | "7064346" | "7067843" | "7075614" | "7105868" | "7189992" | "7211825" | "7264979" | "7268842" | "7282782" | "7297977" | "7323356" | "7330234" | "7339187" | "7365805" | "7385224" | "7391055" | "7402506" | "7411209" | "7453065" | "7453087" | "7456430" | "7462862" | "7468304" | "7470607" | "7485478" | "7501293" | "7560396" | "7633471" | "7732818" | "7825419" | "7855380" | "RE38292").PN. OR ("8134156").URPN.				
S26	95	S25 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:44
S27	0	(buffer near5 (source drain) with (ozide near2 semiconductor))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:48
S28	0	(buffer with (source drain) with (ozide near2 semiconductor))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:48
S29	0	(source drain) with (ozide near2 semiconductor) with channel	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 16:49

S30	5583	(source drain) with (oxide near2 semiconductor) with channel	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:03
S31	371	(buffer with (source drain) with (oxide near2 semiconductor))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:03
S32	118	(buffer with (source drain) with (oxide near2 semiconductor) with channel)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:03
S33	24	S32 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:04
S34	108	("20010046027" | "20020056838" | "20020132454" | "20030189401" | "20030218222" | "20040038446" | "20040127038" | "20050017302" | "20050199959" | "20060035452" | "20060043377" | "20060091793" | "20060108529" | "20060108636" | "20060110867" | "20060113536" | "20060113539" | "20060113549" | "20060113565" | "20060169973" | "20060170111" | "20060197092" | "20060208977" | "20060228974" | "20060231882" | "20060238135" | "20060244107" | "20060284171" | "20060284172" | "20060292777" | "20070024187" | "20070046191" | "20070052025" | "20070054507" | "20070072439" | "20070090365" | "20070108446" | "20070152217" | "20070172591" | "20070187678" | "20070187760" | "20070194379" | "20070252928" | "20070272922" | "20070287296" | "20080006877" | "20080038882" | "20080038929" | "20080050595" | "20080073653" | "20080083950" | "20080106191" | "20080128689" | "20080129195" | "20080166834" | "20080182358" | "20080203387" | "20080224133" | "20080254569" | "20080258139" | "20080258140" | "20080258141" | "20080258143" | "20080296568" | "20080308796" | "20080308797" | "20080308804" | "20080308805" | "20080308806" | "20090008639" | "20090065771" | "20090068773" | "20090073325" | "20090114910" | "20090134399" | "20090152541" | "20090278122" | "20090280600" | "20100025678" | "20110012118" | "5731856" | "5744864" | "5847410" | "6294274" | "6563174" | "6586346" | "6727522" | "6960812" | "7049190" | "7061014" | "7064346" | "7105868" | "7211825" | "7282782" | "7297977" | "7301211" | "7323356" | "7385224").PN. OR ("7402506" | "7411209" | "7453065" | "7453087" | "7462862" | "7468304" | "7501293" | "7674650" | "7732819" | "7915075").PN. OR ("8021917").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:08

S35	43	S34 and (angle taper)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:10
S36	0	S34 and ((angle taper) near5 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:10
S37	54124	((angle taper) near5 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:13
S38	217	S37 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:13
S39	164	S38 not (angle adj implant$3)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:15
S40	3037	((taper incline decline angle) near3 (side sidewall surface) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:23
S41	178	(tft (thin adj film adj transistor)) and S40	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:24
S42	10	"US 7081641"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 17:29
S43	11	("20050056897" | "6569707" | "6858527").PN. OR ("7081641").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:30
S44	48	((taper near2 angle) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:40
S45	32689	((taper angle) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:41
S46	161	S45 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:42
S47	243	((taper angle) near3 ((source drain) adj electrode))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:42
S48	243	(taper angle) near3 ((source drain) adj electrode)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:42
S49	206	(tft (thin adj film adj transistor)) and S48	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:43
S50	69	S25 and (angle taper)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:53
S51	519	(source drain) near3 (tilt adj angle)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:56
S52	54	S51 and S17	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:56
S53	5614	S8 S9 S10	US-PGPUB; USPAT;	OR	ON	2012/04/04 17:59

			USOCR			
S54	3354	S53 and (tft (thin adj film)) and (angle taper)	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 17:59
S55	145	S53 and (tft (thin adj film)) and ((angle taper) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 18:00
S56	5	"US 7564058"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2012/04/04 18:04
S57	20	("20020043662" | "20030148561" | "20030213959" | "20030234424" | "20040189188" | "4797108" | "5028551" | "5151806" | "5640067" | "6037197" | "6121660" | "6388270" | "6433363" | "6448116" | "6476416" | "6639244" | "6709901").PN. OR ("7564058").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 18:04
S58	8	S57 and angle	US-PGPUB; USPAT; USOCR	OR	ON	2012/04/04 18:05
S59	218	("20030189401" | "20080128689" | "20080308796" | "20080308806" | "7061014" | "20060110867" | "20060284172" | "20080258141" | "20090068773" | "20060244107" | "5847410" | "6563174" | "20020132454" | "20060231882" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090152541" | "6294274" | "7402506" | "7411209" | "20110012118" | "7915075" | "7462862" | "20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "5731856" | "7385224" | "7732819" | "20080203387" | "20090008639" | "20100025678" | "20030218222" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080254569" | "20080258140" | "20090278122" | "20090280600" | "7049190" | "20070172591" | "20080296568" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "7211825" | "7453065" | "7674650" | "20080182358" | "20090073325" | "7453087" | "7501293" | "20070072439" | "7282782" | "20070187760" | "20080308797" | "5744864" | "6586346" | "6727522" | "6960812" | "7301211" | "20060035452" | "20060091793" | "20060108636" | "20060113549" | "20060197092" | "20070090365"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/18 18:08

		"20080166834" | "20090134399" | "7064346" | "7468304" | "20050199959" | "20070108446" | "7297977" | "20080308804" | "20080308805" | "20090065771" | "20040038446" | "20040127038" | "20050017302" | "20060043377" | "20060113536" | "20060170111" | "20070046191" | "20070252928" | "20070272922" | "20080073653" | "20080129195" | "20080258143" | "20090114910" | "7105868" | "7323356").PN.				
S60	18460	(tft (thin adj film)) and ((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:28
S61	133336	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:29
S62	10304	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:29
S63	1628	S61 and S62	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:29
S64	34920	((angle taper gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:30
S65	193	S64 and S62	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/18 18:30
S66	1	("20120132910").PN.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:00
S67	10	("20110318916" | "20120058599" | "8021917" | "8030663" | "8115201").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:01
S68	11	S66 S67	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:01
S69	5731	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2012/09/26 22:04
S70	294	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2012/09/26 22:04
S71	62	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2012/09/26 22:04
S72	5942	S69 S70 S71	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2012/09/26 22:04

			IBM_TDB			
S73	5403	S72 and (tft (thin$1film) (thin adj film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:04
S74	3556	S73 and (angle taper)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:04
S75	878	S73 and ((angle taper) with electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:05
S76	133560	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:06
S77	10334	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:06
S78	1631	S76 and S77	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:06
S79	532	S72 and S78	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/26 22:06
S80	89	((angle taper gradation stair) near3 (source drain)) and S77 and S72	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:08
S81	5466	(257/59).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:19
S82	5099	(257/72).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:19
S83	45	((angle taper gradation stair) near3 (source drain)) and S77 and S81	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:19
S84	40	((angle taper gradation stair) near3 (source drain)) and S77 and S82	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:19
S85	60	S83 S84	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:19
S86	674	(257/e29.277).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:21
S87	311	(257/e21.535).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:24

S88	1543	(438/158).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:27
S89	15	((angle taper gradation stair) near3 (source drain)) and S77 and S88	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:27
S90	3682	(438/149).CCLS.	US-PGPUB; USPAT	OR	OFF	2012/09/26 22:28
S91	17	((angle taper gradation stair) near3 (source drain)) and S77 and S90	US-PGPUB; USPAT; USOCR	OR	ON	2012/09/26 22:28
S95	6242	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2013/07/01 10:27
S96	356	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2013/07/01 10:27
S97	75	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2013/07/01 10:27
S98	6489	S95 S96 S97	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/07/01 10:27
S99	142606	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2013/07/01 10:27
S100	11746	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2013/07/01 10:27
S101	1860	S99 and S100	US-PGPUB; USPAT; USOCR	OR	ON	2013/07/01 10:27
S102	600	S98 and S101	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/07/01 10:27
S103	5191	(semiconductor near5 ((indium in) and (gallium ga) and (zinc zn)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 02:30
S104	11923	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 02:30
S105	1268	S103 and S104	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 02:30
S106	1058	(IN$2ga$2zn)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2013/08/12 02:33

			IBM_TDB			
S107	268	("20030189401" | "20050050897" | "20060110867" | "20060284172" | "20080128689" | "20080258141" | "20080308796" | "20080308806" | "20090068773" | "7061014" | "20090189155" | "20020132454" | "20060231882" | "20060244107" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090114917" | "20090152541" | "20100044711" | "20110318916" | "20120132910" | "5847410" | "6294274" | "6563174" | "7323368" | "7402506" | "7411209" | "8030663" | "8115201" | "8158464" | "20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "20100065844" | "20100117086" | "5731856" | "7385224" | "7462862" | "7732819" | "20030218222" | "20060027804" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080203387" | "20080254569" | "20080258140" | "20090008639" | "20090278122" | "20090280600" | "20100025678" | "7049190" | "20090189156" | "8134156" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "20070172591" | "20080296568" | "20100109002" | "7211825" | "7453065" | "20080182358" | "20090073325" | "6532045" | "7453087" | "7501293" | "7674650" | "8021917" | "20050056897" | "20060035452" | "20060108636" | "20060113549" | "20060197092" | "20070072439" | "20070090365" | "20070158652" | "20070187760" | "20080166834" | "20080308797" | "20090134399" | "20090152506" | "5744864" | "6586346" | "6727522" | "6960812" | "7064346" | "7282782" | "7298084" | "7301211" | "7468304" | "20090186445" | "8368079" | "20040038446" | "20040127038" | "20050017302" | "20050199959" | "20060043377" | "20060113536" | "20060170111" | "20060292726" | "20070046191" | "20070108446" | "20070252928" | "20070272922" | "20080073653" | "20080129195" | "20080258143" | "20080308804" | "20080308805" | "20090065771" | "20090114910" | "20100092800" | "20120058599" | "7105868" | "7297977" | "7323356" |	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 09:01

		"20100003783").PN.				
S108	6320	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/12 09:01
S109	368	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/12 09:01
S110	77	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/12 09:01
S111	6569	S108 S109 S110	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 09:01
S112	143950	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 09:01
S113	11923	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 09:01
S114	1895	S112 and S113	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/12 09:01
S115	617	S111 and S114	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/12 09:01
S116	133	("20030189401" | "20050050897" | "20060110867" | "20060284172" | "20080128689" | "20080258141" | "20080308796" | "20080308806" | "20090068773" | "7061014" | "20090189155" | "20020132454" | "20060231882" | "20060244107" | "20060284171" | "20070054507" | "20070152217" | "20070287296" | "20080224133" | "20080258139" | "20090114917" | "20090152541" | "20100044711" | "20110318916" | "20120132910" | "5847410" | "6294274" | "6563174" | "7323368" | "7402506" | "7411209" | "8030663" | "8115201" | "8158464" | "20060108529" | "20060113565" | "20060169973" | "20060228974" | "20060292777" | "20080050595" | "20080106191" | "20100065844" | "20100117086" | "5731856" | "7385224" | "7462862" | "7732819" | "20030218222" | "20060027804" | "20070024187" | "20070187678" | "20070194379" | "20080006877" | "20080038882" | "20080038929" | "20080083950" | "20080203387" | "20080254569" | "20080258140" | "20090008639" | "20090278122" | "20090280600" | "20100025678" | "7049190" | "20090189156" |	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2013/08/12 09:02

		"8134156" | "20010046027" | "20020056838" | "20060113539" | "20060208977" | "20060238135" | "20070052025" | "20070172591" | "20080296568" | "20100109002" | "7211825" | "7453065" | "20080182358" | "20090073325" | "6532045" | "7453087" | "7501293" | "7674650" | "8021917" | "20050056897" | "20060035452" | "20060108636" | "20060113549" | "20060197092" | "20070072439" | "20070090365" | "20070158652" | "20070187760" | "20080166834" | "20080308797" | "20090134399" | "20090152506" | "5744864" | "6586346" | "6727522" | "6960812" | "7064346" | "7282782" | "7298084" | "7301211" | "7468304" | "20090186445" | "8368079" | "20040038446" | "20040127038" | "20050017302" | "20050199959" | "20060043377" | "20060113536" | "20060170111" | "20060292726" | "20070046191" | "20070108446" | "20070252928" | "20070272922" | "20080073653" | "20080129195" | "20080258143" | "20080308804" | "20080308805" | "20090065771" | "20090114910" | "20100092800" | "20120058599" | "7105868" | "7297977" | "7323356" | "20100003783").PN.				
S117	2	"US 20130214270"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2013/12/11 01:46
S118	1	("20060033098").PN.	US-PGPUB; USPAT	OR	OFF	2013/12/11 01:57
S119	6558	((SHUNPEI) near2 (YAMAZAKI)).INV.	US-PGPUB; USPAT	OR	ON	2013/12/11 02:41
S120	385	((KENGO) near2 (AKIMOTO)).INV.	US-PGPUB; USPAT	OR	ON	2013/12/11 02:41
S121	82	((DAISUKE) near2 (KAWAE)).INV.	US-PGPUB; USPAT	OR	ON	2013/12/11 02:41
S122	6814	S119 S120 S121	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/12/11 02:41
S123	148280	((angle taper step gradation stair) near3 (source drain))	US-PGPUB; USPAT; USOCR	OR	ON	2013/12/11 02:41
S124	12541	(tft (thin adj film adj transistor)) and ((bottom adj gate) bottom$1gate)	US-PGPUB; USPAT; USOCR	OR	ON	2013/12/11 02:41
S125	1990	S123 and S124	US-PGPUB; USPAT; USOCR	OR	ON	2013/12/11 02:41

S126	649	S122 and S125	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/12/11 02:41

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1694	(257/57).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2014/03/23 19:32
L2	12	(((source adj electrode) with (angle with (bottom top))) and ((drain adj electrode) with (angle with (bottom top)))).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/23 19:32
L3	21	((gate adj electrode) and (source adj electrode) and (drain adj electrode) and oxide and (angle with (bottom top))).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/23 19:32
S92	1300	(257/57).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/26 22:18
S93	16	((gate adj electrode) and (source adj electrode) and (drain adj electrode) and oxide and (angle with (bottom top))).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2012/09/26 23:11
S94	9	(((source adj electrode) with (angle with (bottom top))) and ((drain adj electrode) with (angle with (bottom top)))).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2012/09/26 23:13

3/23/2014 7:59:40 PM
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The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-9. (Canceled)

10. (Previously Presented) A semiconductor device comprising:

a glass substrate;

a transistor over the glass substrate, the transistor comprising:

a gate electrode;

a first insulating layer over the gate electrode;

an oxide semiconductor layer over the first insulating layer; and

a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer;

a second insulating layer over the transistor;

a pixel electrode over the second insulating layer;

a third insulating layer over the pixel electrode;

a light-emitting layer over the pixel electrode and the third insulating layer;

an electrode over the light-emitting layer,

wherein the oxide semiconductor layer comprises indium and zinc,

wherein each of a side surface of the source electrode and a side surface of the drain electrode has a step in a lower portion thereof,

wherein a first angle of the step that is made between the side surface of the source electrode and an upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°, and

wherein a second angle of the step that is made between the side surface of the drain electrode and the upper surface of the glass substrate is greater than or equal to

20° and smaller than or equal to 90°.

11. (Previously Presented) The semiconductor device according to claim 10, wherein each of the source electrode and the drain electrode is in contact with an upper surface of the first insulating layer.

12. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is over the source electrode and the drain electrode.

13. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is in contact with each of the side surface of the source electrode and the side surface of the drain electrode.

14. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer further comprises gallium.

15. (Previously Presented) The semiconductor device according to claim 10, wherein the pixel electrode is in contact with the drain electrode.

16. (Previously Presented) The semiconductor device according to claim 10, wherein the oxide semiconductor layer is a non-single-crystal film.

17. (Previously Presented) The semiconductor device according to claim 10, further comprising:

a first buffer layer between the oxide semiconductor layer and the source electrode; and

a second buffer layer between the oxide semiconductor layer and the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer.

18. (Previously Presented) A semiconductor device comprising:

a glass substrate;

a transistor over the glass substrate, the transistor comprising:

a gate electrode;

a first insulating layer over the gate electrode;

an oxide semiconductor layer over the first insulating layer; and

a source electrode and a drain electrode each electrically connected to the oxide semiconductor layer;

a second insulating layer over the transistor;

a pixel electrode over the second insulating layer;

a third insulating layer over the pixel electrode;

a light-emitting layer over the pixel electrode and the third insulating layer;

an electrode over the light-emitting layer,

wherein the oxide semiconductor layer comprises indium and zinc,

wherein a first angle between a surface of the glass substrate and a side surface of a first bottom edge of the source electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the source electrode, and

wherein a second angle between the surface of the glass substrate and a side surface of a second bottom edge of the drain electrode is made to be different from an angle between the surface of the glass substrate and a side surface of a top edge of the drain electrode.

19. (Previously Presented) The semiconductor device according to claim 18, wherein each of the source electrode and the drain electrode is in contact with an upper surface of the first insulating layer.

20. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is over the source electrode and the drain electrode.

21. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is in contact with each of the side surface of the source electrode and the side surface of the drain electrode.

22. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer further comprises gallium.

23. (Previously Presented) The semiconductor device according to claim 18, wherein the pixel electrode is in contact with the drain electrode.

24. (Previously Presented) The semiconductor device according to claim 18, wherein the oxide semiconductor layer is a non-single-crystal film.

25. (Previously Presented) The semiconductor device according to claim 18, further comprising:

a first buffer layer between the oxide semiconductor layer and the source electrode; and

a second buffer layer between the oxide semiconductor layer and the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor layer.

PTO/SB/08A (07-06)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/763,874
Filing Date	February 11, 2013
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2896
Examiner Name	J. JOY
Attorney Docket Number	0756-10065

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
/J.J./		JP-2008-205451A	09-04-2008			Abst.
/J.J./		JP-2005-223049A	08-18-2005			Abst.
/J.J./		JP-07-064112A	03-10-1995			Abst.

Examiner Signature	/Jeremy Joy/	Date Considered	03/23/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13763874	YAMAZAKI ET AL.
	Examiner	**Art Unit**
	JEREMY JOY	2896

CPC		
Symbol	**Type**	**Version**

CPC Combination Sets				
Symbol	**Type**	**Set**	**Ranking**	**Version**

/JEREMY JOY/ Examiner.Art Unit 2896	03/23/2014	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	16	
/CHEUNG LEE/ Primary Examiner.Art Unit 2896	03/24/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	10	2

U.S. Patent and Trademark Office — Part of Paper No. 20140323

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13763874	YAMAZAKI ET AL.
	Examiner	Art Unit
	JEREMY JOY	2896

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS					CLAIMED						NON-CLAIMED			
257	57					H	0	1	L	29 / 04 (2006.01.01)		H	0	1	L	21 / 00 (2006.01.01)
CROSS REFERENCE(S)						H	0	1	L	29 / 10 (2006.01.01)						
						H	0	1	L	31 / 00 (2006.01.01)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)															
257	59	E21.535														
438	149	158														

/JEREMY JOY/ Examiner.Art Unit 2896	03/23/2014	Total Claims Allowed:	
(Assistant Examiner)	(Date)	16	
/CHEUNG LEE/ Primary Examiner.Art Unit 2896	03/24/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	10	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13763874	YAMAZAKI ET AL.
	Examiner	**Art Unit**
	JEREMY JOY	2896

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
-	1	8	17												
-	2	9	18												
-	3	10	19												
-	4	11	20												
-	5	12	21												
-	6	13	22												
-	7	14	23												
-	8	15	24												
-	9	16	25												
1	10														
2	11														
3	12														
4	13														
5	14														
6	15														
7	16														

/JEREMY JOY/ Examiner.Art Unit 2896	03/23/2014	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	16	
/CHEUNG LEE/ Primary Examiner.Art Unit 2896	03/24/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	10	2

U.S. Patent and Trademark Office

Part of Paper No. 20140323

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31780 7590 03/31/2014
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/763,874	02/11/2013	Shunpei YAMAZAKI	0756-10065	7085

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/30/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
JOY, JEREMY J	2896	257-057000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Eric J. Robinson,
Robinson Intellectual
Property Law Office, P.C.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Semiconductor Energy Laboratory Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Atsugi-shi, Kanagawa-ken, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 3

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
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☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-2280 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date June 30, 2014

Typed or printed name Eric J. Robinson Registration No. 38,285

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal

Application Number:	13763874
Filing Date:	11-Feb-2013
Title of Invention:	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Filer:	Eric J. Robinson/Fatima Brown
Attorney Docket Number:	0756-10065

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Printed Copy of Patent - No Color	8001	3	3	9
		Total in USD ($)		**969**

Electronic Acknowledgement Receipt	
EFS ID:	19445921
Application Number:	13763874
International Application Number:	
Confirmation Number:	7085
Title of Invention:	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Fatima Brown
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10065
Receipt Date:	30-JUN-2014
Filing Date:	11-FEB-2013
Time Stamp:	10:17:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$969
RAM confirmation Number	10062
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	IF.pdf	201452 2e8455c33637187dbdfe005b40430274d620a703	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32467 c91f7f63a9ac3ffe7bb92d3690b922fc306f184c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	233919		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/763,874	08/12/2014	8803146	0756-10065	7085

31780 7590 07/23/2014

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Shunpei YAMAZAKI, Setagaya, JAPAN;
Kengo AKIMOTO, Atsugi, JAPAN;
Daisuke KAWAE, Yamato, JAPAN;
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