Petitioner Bluehouse Global Ltd.

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Continued
(Pages 247-490)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	15

Complete if Known	
Application Number	14/451,680
Filing Date	August 5, 2014
First Named Inventor	Shunpei YAMAZAKI
Art Unit	2896
Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10566

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Sheet 2 of 15

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First Named Inventor	Shunpei YAMAZAKI
Art Unit	2896
Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10566

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Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10566

Sheet 4 of 15

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Sheet 7 of 15

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Application Number	14/451,680
Filing Date	August 5, 2014
First Named Inventor	Shunpei YAMAZAKI
Art Unit	2896
Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10566

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Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		US-2006/0033098	02-16-2006	SHIH.I et al.	

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Art Unit	2896
Examiner Name	Jeremy J. Joy
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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	14/451,680
Filing Date	August 5, 2014
First Named Inventor	Shunpei YAMAZAKI
Art Unit	2896
Examiner Name	Jeremy J. Joy
Attorney Docket Number	0756-10566

Sheet 13 of 15

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		MEIBOOM.S et al., "THEORY OF THE BLUE PHASE OF CHOLESTERIC LIQUID CRYSTALS", PHYS. REV. LETT. (PHYSICAL REVIEW LETTERS), May 4, 1981, Vol. 46, No. 18, pp. 1216-1219.	Eng.
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		NOMURA.K et al., "AMORPHOUS OXIDE SEMICONDUCTORS FOR HIGH-PERFORMANCE FLEXIBLE THIN-FILM TRANSISTORS", JPN. J. APPL. PHYS. (JAPANESE JOURNAL OF APPLIED PHYSICS), 2006, Vol. 45, No. 5B, pp. 4303-4308.	Eng.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	14/451,680
				Filing Date	August 5, 2014
				First Named Inventor	Shunpei YAMAZAKI
(Use as many sheets as necessary)				Art Unit	2896
				Examiner Name	Jeremy J. Joy
Sheet	14	of	15	Attorney Docket Number	0756-10566

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		JANOTTI.A et al., "NATIVE POINT DEFECTS IN ZnO", PHYS. REV. B (PHYSICAL REVIEW. B), October 4, 2007, Vol. 76, No. 16, pp. 165202-1-165202-22.	Eng.
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		PARK.J et al., "IMPROVEMENTS IN THE DEVICE CHARACTERISTICS OF AMORPHOUS INDIUM GALLIUM ZINC OXIDE THIN-FILM TRANSISTORS BY Ar PLASMA TREATMENT", APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS) , June 26, 2007, Vol. 90, No. 26, pp. 262106-1-262106-3.	Eng.
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		HSIEH.H et al., "P-29:Modeling of Amorphous Oxide Semiconductor Thin Film Transistors and Subgap Density of States", SID DIGEST '08 : SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, pp. 1277-1280.	Eng.
		OBA.F et al., "Defect energetics in ZnO: A hybrid Hartree-Fock density functional study", PHYS. REV. B (PHYSICAL REVIEW. B), 2008, Vol. 77, pp. 245202-1-245202-6.	Eng.
		KIM.S et al., "High-Performance oxide thin film transistors passivated by various gas plasmas", 214TH ECS MEETING, 2008, No. 2317, ECS.	Eng.
		HAYASHI.R et al., "42.1: INVITED PAPER: IMPROVED AMORPHOUS In-Ga-Zn-O TFTS", SID DIGEST '08 : SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, pp. 621-624.	Eng.
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		PARK.SANG-HEE et al., "42.3: Transparent ZnO Thin Film Transistor for the Application of High Aperture Ratio Bottom Emission AM-OLED Display", SID DIGEST '08 : SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, May 20, 2008, Vol. 39, pp. 629-632.	Eng.

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Substitute for form 1449/PTO				**Complete if Known**	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	14/451,680
				Filing Date	August 5, 2014
				First Named Inventor	Shunpei YAMAZAKI
(Use as many sheets as necessary)				Art Unit	2896
				Examiner Name	Jeremy J. Joy
Sheet	15	of	15	Attorney Docket Number	0756-10566

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		FUNG.T et al., "2-D Numerical Simulation of High Performance Amorphous In-Ga-Zn-O TFTs for Flat Panel Displays", AM-FPD '08 DIGEST OF TECHNICAL PAPERS, July 2, 2008, pp. 251-252, THE JAPAN SOCIETY OF APPLIED PHYSICS.	Eng.
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		ASAKUMA.N et al., "CRYSTALLIZATION AND REDUCTION OF SOL-GEL-DERIVED ZINC OXIDE FILMS BY IRRADIATION WITH ULTRAVIOLET LAMP", JOURNAL OF SOL-GEL SCIENCE AND TECHNOLOGY, 2003, Vol. 26, pp. 181-184.	Eng.
		FORTUNATO.E et al., "WIDE-BANDGAP HIGH-MOBILITY ZNO THIN-FILM TRANSISTORS PRODUCED AT ROOM TEMPERATURE", APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS) , September 27, 2004, Vol. 85, No. 13, pp. 2541-2543.	Eng.
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		OH.M et al., "IMPROVING THE GATE STABILITY OF ZNO THIN-FILM TRANSISTORS WITH ALUMINUM OXIDE DIELECTRIC LAYERS", J. ELECTROCHEM. SOC. (JOURNAL OF THE ELECTROCHEMICAL SOCIETY), 2008, Vol. 155, No. 12, pp. H1009-H1014.	Eng.
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		NOMURA.K et al., "Carrier transport in transparent oxide semiconductor with intrinsic structural randomness probed using single-crystalline InGaO3(ZnO)5 films", APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS) , September 13, 2004, Vol. 85, No. 11, pp. 1993-1995.	Eng.
		CHINESE OFFICE ACTION (APPLICATION NO.200910206768.3) DATED March 15, 2013.	Full

Examiner Signature		Date Considered	

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Electronic Acknowledgement Receipt

EFS ID:	20007574
Application Number:	14451680
International Application Number:	
Confirmation Number:	5776
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Adele Stamper
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10566
Receipt Date:	29-AUG-2014
Filing Date:	05-AUG-2014
Time Stamp:	15:30:20
Application Type:	Utility under 35 USC 111(a)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_29AUG2014_075610566.pdf	3357759 e4f57e1088fe1d217f1f2b402846810acfea7048	yes	17

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New Applications Under 35 U.S.C. 111
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
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Attorney Docket No. 0756-10566

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 5776
Shunpei YAMAZAKI et al.	)	Examiner: Jeremy J. Joy
Serial No. 14/451,680	)	Group Art Unit: 2896
Filed: August 5, 2014	)	
For: SEMICONDUCTOR DEVICE AND	)	
MANUFACTURING METHOD	)	
THEREOF	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application.

The references listed on the attached Form PTO-1449 were cited in parent Application Serial No. 13/763,874, and/or predecessor Application Serial Nos. 12/613,769 and 12/606,262. Copies of the references can be found in these applications (37 C.F.R. § 1.98(d)(1)-(2)).

U.S. Publication No. 2007/0072439 is in the family of JP 2007-123861.

U.S. Patent No. 6,727,522 is in the family of JP 2000-150900.

U.S. Patent No. 7,061,014 is in the family of JP 2004-103957.

U.S. Patent No. 5,744,864 is in the family of JP 11-505377.

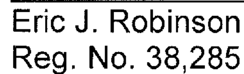
U.S. Patent No. 6,563,174 is in the family of JP 2003-086808.

U.S. Publication No. 2006/0244107 is in the family of WO 2004/114391.

U.S. Patent Nos. 8,134,156; 8,158,464 and 8,368,079 and U.S. Publication Nos. 2009/0186445; 2009/0189155; 2009/0189156 and 2010/0003783 and WO2007/058329 are in the family of CN101283444.

This Information Disclosure Statement is being submitted before the issuance of a first Office Action on the merits, therefore, no fee is required. However, the Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



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This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日 Date of Application:	２００８年１１月　７日
出願番号 Application Number:	特願２００８－２８７１８７
パリ条約による外国への出願に用いる優先権の主張の基礎となる出願の国コードと出願番号 The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is	ＪＰ２００８－２８７１８７
出願人 Applicant(s):	株式会社半導体エネルギー研究所

２０１４年　８月２５日

特許庁長官
Commissioner,
Japan Patent Office

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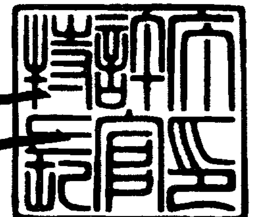

【書類名】　　　　　　特許願
【整理番号】　　　　　P011986
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【あて先】　　　　　　特許庁長官　鈴木　隆史　殿
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　　【代表者】　　　　山崎　舜平
【手数料の表示】
　　【予納台帳番号】　002543
　　【納付金額】　　　15,000円
【提出物件の目録】
　　【物件名】　　　　特許請求の範囲　1
　　【物件名】　　　　明細書　1
　　【物件名】　　　　図面　1
　　【物件名】　　　　要約書　1

【書類名】特許請求の範囲
【請求項１】
絶縁表面を有する基板上にゲート電極と、
前記ゲート電極上に絶縁層と、
前記絶縁層上にソース電極及びドレイン電極と、
前記ソース電極の側面と、該側面と向かい合う前記ドレイン電極の側面の間に前記ゲート電極と前記絶縁層を介して重なる酸化物半導体層とを有し、
前記基板の基板面と前記ソース電極の側面とがなす角と、前記基板の基板面と前記ドレイン電極の側面とがなす角とが２０°以上９０°未満であることを特徴とする半導体装置。
【請求項２】
請求項１において、前記ソース電極及び前記ドレイン電極の上面にバッファ層を有し、該バッファ層上に前記酸化物半導体層を有する半導体装置。
【請求項３】
請求項１または請求項２において、前記酸化物半導体層における前記ソース電極の側面及び前記ドレイン電極の側面と重なる領域は、電界集中緩和領域である半導体装置。
【請求項４】
請求項１乃至３のいずれか一において、前記酸化物半導体層は、インジウム、ガリウム、及び亜鉛を含むことを特徴とする半導体装置。
【請求項５】
絶縁表面を有する基板上にゲート電極と、
前記ゲート電極上に絶縁層と、
前記絶縁層上にソース電極及びドレイン電極と、
前記ソース電極の側面と、該側面と向かい合う前記ドレイン電極の側面の間に前記ゲート電極と前記絶縁層を介して重なる酸化物半導体層とを有し、
前記基板の基板面と前記ソース電極下端部の側面とがなす角と、前記基板の基板面と前記ドレイン電極下端部の側面とがなす角とが２０°以上９０°未満であることを特徴とする半導体装置。
【請求項６】
請求項５において、前記基板の基板面と前記ソース電極下端部の側面とがなす角は、前記基板の基板面とソース電極上端部の側面とがなす角と異なることを特徴とする半導体装置。
【請求項７】
請求項５または請求項６において、前記基板の基板面と前記ドレイン電極下端部の側面とがなす角は、前記基板の基板面とドレイン電極上端部の側面とがなす角と異なることを特徴とする半導体装置。
【請求項８】
請求項５乃至７のいずれか一において、前記ソース電極の側面及び前記ドレイン電極の側面は少なくとも一部に曲面を有していることを特徴とする半導体装置。
【請求項９】
請求項５乃至８のいずれか一において、前記ソース電極及び前記ドレイン電極の上面にバッファ層を有し、該バッファ層上に前記酸化物半導体層を有する半導体装置。
【請求項１０】
請求項５乃至９のいずれか一において、前記酸化物半導体層における前記ソース電極の側面及び前記ドレイン電極の側面と重なる領域は、電界集中緩和領域である半導体装置。
【請求項１１】
請求項５乃至１０のいずれか一において、前記酸化物半導体層は、インジウム、ガリウム、及び亜鉛を含むことを特徴とする半導体装置。
【請求項１２】
絶縁表面を有する基板上にゲート電極を形成し、
前記ゲート電極を覆うゲート絶縁層を形成し、

前記ゲート絶縁層上に導電層とバッファ層とを大気にふれることなく積層形成し、
前記バッファ層及び前記導電層を選択的にエッチングして前記基板の基板面となす角が２０°以上９０°未満である側面を有するソース電極及びドレイン電極を形成し、
前記ゲート絶縁層、前記ソース電極、及び前記ドレイン電極上に酸化物半導体層を形成する半導体装置の作製方法。
【請求項１３】
請求項１２において前記酸化物半導体層は、インジウム、ガリウム、及び亜鉛を含むことを特徴とする半導体装置の作製方法。
【請求項１４】
請求項１２または請求項１３において、前記バッファ層は、インジウム、ガリウム、及び亜鉛を含むことを特徴とする半導体装置の作製方法。
【請求項１５】
請求項１２乃至請求項１４のいずれか一において、前記酸化物半導体層と前記バッファ層は同じ組成のターゲットを用いることを特徴とする半導体装置の作製方法。

【書類名】明細書
【発明の名称】半導体装置およびその作製方法
【技術分野】
【０００１】
酸化物半導体を用いる表示装置及びその製造方法に関する。
【背景技術】
【０００２】
液晶表示装置に代表されるように、ガラス基板等の平板に形成される薄膜トランジスタは、アモルファスシリコン、多結晶シリコンによって作製されている。アモルファスシリコンを用いた薄膜トランジスタは、電界効果移動度が低いもののガラス基板の大面積化に対応することができ、一方、結晶シリコンを用いた薄膜トランジスタは電界効果移動度が高いものの、レーザアニール等の結晶化工程が必要であり、ガラス基板の大面積化には必ずしも適応しないといった特性を有している。
【０００３】
これに対し、酸化物半導体を用いて薄膜トランジスタを作製し、電子デバイスや光デバイスに応用する技術が注目されている。例えば、酸化物半導体膜として酸化亜鉛、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系酸化物半導体を用いて薄膜トランジスタを作製し、画像表示装置のスイッチング素子などに用いる技術が特許文献１及び特許文献２で開示されている。
【特許文献１】特開２００７－１２３８６１号公報
【特許文献２】特開２００７－０９６０５５号公報
【発明の開示】
【発明が解決しようとする課題】
【０００４】
ボトムゲート型の薄膜トランジスタにおいて、ソース電極とドレイン電極間に生じる恐れのある電界集中を緩和し、スイッチング特性の劣化を抑える構造及びその作製方法を提供することを課題の一とする。
【０００５】
また、酸化物半導体層の被覆性を向上させる構造およびその作製方法を提供することも課題の一とする。
【課題を解決するための手段】
【０００６】
ソース電極及びドレイン電極上に酸化物半導体層を有するボトムゲート型の薄膜トランジスタとし、酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とすることで、ソース電極及びドレイン電極の側面における電極上端から電極下端までの距離を大きくする。
【０００７】
本明細書で開示する発明の構成の一つは、絶縁表面を有する基板上にゲート電極と、ゲート電極上に絶縁層と、絶縁層上にソース電極及びドレイン電極と、ソース電極の側面と、該側面と向かい合うドレイン電極の側面の間にゲート電極と絶縁層を介して重なる酸化物半導体層とを有し、基板の基板面とソース電極の側面とがなす角と、基板の基板面とドレイン電極の側面とがなす角とが２０°以上９０°未満であることを特徴とする半導体装置である。
【０００８】
上記構成は、上記課題の少なくとも一つを解決する。
【０００９】
ソース電極及びドレイン電極に用いる金属材料にもよるが、ソース電極及びドレイン電極の少なくとも側面には自然酸化膜が形成される。この自然酸化膜は、エッチング後に大気などの酸素を含む雰囲気に触れると形成される。また、エッチング後に酸化物半導体層を形成する際の成膜雰囲気に酸素を含んでいる場合にも、電極側面に自然酸化膜が形成される。

【００１０】
また、電極上面に自然酸化膜が形成されることを防ぐために、スパッタ法で得られる金属膜上に接してバッファ層（ｎ＋層とも呼ぶ）を大気に触れることなく連続成膜することが好ましい。このバッファ層は、酸化物半導体層に比べて低抵抗な酸化物半導体層であり、ソース領域またはドレイン領域として機能させる。

【００１１】
上記構成において、ソース電極及び前記ドレイン電極の上面にバッファ層を有し、該バッファ層上に酸化物半導体層を有する。バッファ層（ｎ＋層とも呼ぶ）を大気に触れることなく連続成膜することにより、ソース電極及び前記ドレイン電極の上面に自然酸化膜が形成されることを防ぐ。

【００１２】
また、ボトムゲート型の薄膜トランジスタにおいて、ゲート電極にしきい値電圧よりも十分に大きい電圧をかけて、オン状態とした場合のドレイン電流の経路（チャネル長方向の電流経路）は、まず、ドレイン電極からゲート絶縁膜の界面近傍の酸化物半導体層を経てソース電極に達する経路となる。

【００１３】
なお、ソース電極及びドレイン電極上に酸化物半導体層を有するボトムゲート型の薄膜トランジスタのチャネル長は、ソース電極とドレイン電極の最短間隔距離に相当し、ソース電極とドレイン電極に挟まれ、ゲート絶縁膜との界面近傍の酸化物半導体層の距離とする。

【００１４】
ｎ＋層をドレイン電極及びソース電極の上面に接して形成する場合、電極側面に形成される自然酸化膜の導電率が低いと、ドレイン電流の主な経路は、ドレイン電極からｎ＋層を経由して、ドレイン電極側面の界面近傍の酸化物半導体層を通り、ゲート絶縁膜の界面近傍の酸化物半導体層を経て、ソース電極側面の界面近傍の酸化物半導体層を通り、ｎ＋層を経由してソース電極に達する経路となる。スパッタ法で得られる酸化物半導体層は、被成膜面との界面近傍の膜質が、被成膜面の材料に影響を受ける傾向がある。酸化物半導体層は、ｎ＋層との界面、ソース電極側面（及びドレイン電極側面）との界面、ゲート絶縁膜との界面とを有し、異なる材料との界面を少なくとも３つ有する。従って、酸化物半導体層において、ドレイン電極側面の自然酸化膜と界面状態と、ゲート絶縁膜との界面状態は異なるため、ドレイン電極側面の界面近傍の酸化物半導体層が第１の電界集中緩和領域として機能する。また、ソース電極側面の自然酸化膜と界面状態と、ゲート絶縁膜との界面状態は異なるため、ソース電極側面の界面近傍の酸化物半導体層が第２の電界集中緩和領域として機能する。

【００１５】
このように、酸化物半導体層におけるソース電極の側面及びドレイン電極の側面と重なる領域は、電界集中緩和領域として機能する。

【００１６】
本明細書中で用いる酸化物半導体は、$InMO_3(ZnO)_m$（ｍ＞０）で表記される薄膜を形成し、その薄膜を半導体層として用いた薄膜トランジスタを作製する。なお、Ｍは、Ｇａ、Ｆｅ、Ｎｉ、Ｍｎ及びＣｏから選ばれた一の金属元素又は複数の金属元素を示す。例えばＭとして、Ｇａの場合があることの他、ＧａとＮｉ又はＧａとＦｅなど、Ｇａ以外の上記金属元素が含まれる場合がある。また、上記酸化物半導体において、Ｍとして含まれる金属元素の他に、不純物元素としてＦｅ、Ｎｉその他の遷移金属元素、又は該遷移金属の酸化物が含まれているものがある。本明細書においては、この薄膜をＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜とも呼ぶ。

【００１７】
Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の結晶構造は、スパッタ法で成膜した後、２００℃～５００℃、代表的には３００～４００℃で１０分～１００分行っても、アモルファス構造がＸＲＤの分析では観察される。

【００１８】
酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とし、ソース電極及びドレイン電極の側面における電極上端から電極下端までの距離を大きくすることによって第１の電界集中緩和領域の長さ及び第２電界集中緩和領域の長さを長くして電界集中を緩和させる。さらに、ソース電極及びドレイン電極の膜厚を厚くすることによっても電極側面における電極上端から電極下端までの距離を大きくできる。
【００１９】
また、酸化物半導体層をスパッタ法で成膜する場合、基板面に垂直な電極側面に成膜される膜厚は、電極上面に成膜される膜厚よりも薄くなる恐れがある。酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とすることで側面においても膜厚の均一性を高めることができ、電界集中を緩和することもできる。
【００２０】
また、図１に示すように、ソース電極側面の下端を始点としソース電極側面の上端を結んだ直線がソース電極側面にほぼ一致する場合、ソース電極はテーパ形状を有していると言え、基板の基板面とソース電極の側面がなす角度θ１は、第１のテーパ角とも呼べる。また、ドレイン電極側面の下端を始点としドレイン電極側面の上端を結んだ直線がドレイン電極側面にほぼ一致する場合、ドレイン電極はテーパ形状を有していると言え、基板の基板面とドレイン電極の側面がなす角度θ２は、第２のテーパ角とも呼べる。
【００２１】
また、電極側面が１つの角度を有している形状に限定されず、少なくともソース電極の下端部の側面の角度θ１、及びドレイン電極の下端部の側面の角度θ２が２０°以上９０°未満であれば、電極側面に段差を有してもよい。
【００２２】
また、他の発明の構成は、絶縁表面を有する基板上にゲート電極と、ゲート電極上に絶縁層と、絶縁層上にソース電極及びドレイン電極と、ソース電極の側面と、該側面と向かい合うドレイン電極の側面の間にゲート電極と絶縁層を介して重なる酸化物半導体層とを有し、基板の基板面とソース電極下端部の側面とがなす角と、基板の基板面とドレイン電極下端部の側面とがなす角とが２０°以上９０°未満であることを特徴とする半導体装置である。
【００２３】
上記構成において、基板の基板面とソース電極下端部の側面とがなす角は、基板の基板面とソース電極上端部の側面とがなす角と異ならせる。また、上記構成において、基板の基板面とドレイン電極下端部の側面とがなす角は、基板の基板面とドレイン電極上端部の側面とがなす角と異ならせる。なお、酸化物半導体層を挟んで対向するソース電極側面とドレイン電極側面の断面形状は同じエッチング工程を経るため、ほぼ同一である。
【００２４】
例えば、ソース電極（及びドレイン電極）下端部の側面の角度と、ソース電極（及びドレイン電極）上端部の側面の角度を異ならせ、ソース電極（及びドレイン電極）上端部の側面の角度を９０°としてもよい。ソース電極（及びドレイン電極）上端部の側面の角度をソース電極（及びドレイン電極）下端部の側面の角度よりも大きくすることで、ソース電極及びドレイン電極を形成するためのマスクの間隔を狭く設計することができ、結果としてチャネル長を短く設計する、例えばチャネル長を１μｍ～１０μｍに設計することができる。
【００２５】
また、ソース電極及びドレイン電極の側面形状は、すくなくとも一部に曲面を有していてもよく、例えば、ソース電極及びドレイン電極の断面形状において、電極の下端部は、電極の外側に位置する曲率半径の中心により決まる１つの曲面も有するようにしてもよい。また、ソース電極及びドレイン電極の側面形状は、電極上面から基板に向かって裾広がり

の断面形状を有していてもよい。
【００２６】
上述した様々な断面形状を有する電極の形成は、ドライエッチングまたはウェットエッチングによって形成する。ドライエッチングに用いるエッチング装置としては、反応性イオンエッチング法（ＲＩＥ法）を用いたエッチング装置や、ＥＣＲ（Ｅｌｅｃｔｒｏｎ　Ｃｙｃｌｏｔｒｏｎ　Ｒｅｓｏｎａｎｃｅ）やＩＣＰ（Ｉｎｄｕｃｔｉｖｅｌｙ　Ｃｏｕｐｌｅｄ　Ｐｌａｚｍａ）などの高密度プラズマ源を用いたドライエッチング装置を用いることができる。また、ＩＣＰエッチング装置と比べて広い面積に渡って一様な放電が得られやすいドライエッチング装置としては、上部電極を接地させ、下部電極に１３．５６ＭＨｚの高周波電源を接続し、さらに下部電極に３．２ＭＨｚの低周波電源を接続したＥＣＣＰ（Ｅｎｈａｎｃｅｄ　Ｃａｐａｃｉｔｉｖｅｌｙ　Ｃｏｕｐｌｅｄ　Ｐｌａｓｍａ）モードのエッチング装置がある。このＥＣＣＰモードのエッチング装置であれば、例えば基板として、第１０世代の３ｍを超えるサイズの基板を用いる場合にも対応することができる。
【００２７】
また、ソース電極及びドレイン電極は単層であってもよいし、少なくとも異なる２つの材料からなる２層以上の多層であってもよい。
【００２８】
また、上記構造を実現するための作製方法に関する発明の構成の一つは、絶縁表面を有する基板上にゲート電極を形成し、ゲート電極を覆うゲート絶縁層を形成し、ゲート絶縁層上に導電層とバッファ層とを大気にふれることなく積層形成し、バッファ層及び導電層を選択的にエッチングして基板の基板面となす角が２０°以上９０°未満である側面を有するソース電極及びドレイン電極を形成し、ゲート絶縁層、ソース電極、及びドレイン電極上に酸化物半導体層を形成する半導体装置の作製方法である。
【００２９】
上記作製方法に関する構成において、バッファ層は、インジウム、ガリウム、及び亜鉛を含み、バッファ層上に形成する酸化物半導体層と同じターゲットを用いることができる。成膜雰囲気を変更することで、バッファ層と、酸化物半導体層とを作り分けることができ、共通のターゲットを用いることで製造コストを低減することができる。
【００３０】
上記作製方法に関する構成において、ゲート絶縁層上に導電層とバッファ層とを大気にふれることなく積層形成しており、連続成膜を行うことを特徴の一つとしている。
【００３１】
上記作製方法に関する構成において、ソース電極、及びドレイン電極を形成する導電層は、アルミニウム、タングステン、クロム、タンタル、チタン、モリブデンなどの金属材料またはその合金材料を用いて形成する。また、導電層は、２層以上の積層としてもよく、例えば、アルミニウム膜を下層とし、上層をチタン膜とする積層、タングステン膜を下層とし、上層をモリブデン膜とする積層、アルミニウム膜を下層とし、上層をモリブデン膜とする積層などを用いることができる。
【００３２】
本明細書中で連続成膜とは、スパッタ法で行う第１の成膜工程からスパッタ法で行う第２の成膜工程までの一連のプロセス中、被処理基板の置かれている雰囲気が大気等の汚染雰囲気に触れることなく、常に真空中または不活性ガス雰囲気（窒素雰囲気または希ガス雰囲気）で制御されていることを言う。連続成膜を行うことにより、清浄化された被処理基板の水分等の再付着を回避して成膜を行うことができる。
【００３３】
同一チャンバー内で第１の成膜工程から第２の成膜工程までの一連のプロセスを行うことは本明細書における連続成膜の範囲にあるとする。
【００３４】
また、異なるチャンバーで第１の成膜工程から第２の成膜工程までの一連のプロセスを行

う場合、第１の成膜工程を終えた後、大気にふれることなくチャンバー間を基板搬送して第２の成膜を施すことも本明細書における連続成膜の範囲にあるとする。
【００３５】
なお、第１の成膜工程と第２の成膜工程の間に、基板搬送工程、アライメント工程、徐冷工程、または第２の工程に必要な温度とするため基板を加熱または冷却する工程等を有しても、本明細書における連続成膜の範囲にあるとする。
【００３６】
ただし、洗浄工程、ウエットエッチング、レジスト形成といった液体を用いる工程が第１の成膜工程と第２の成膜工程の間にある場合、本明細書でいう連続成膜の範囲には当てはまらないとする。
【００３７】
本明細書において、上、下、側、水平、垂直等の方向を表す文言は、基板表面の上にデバイスを配置した場合の基板面を基準とする方向を指す。
【００３８】
なお、第１、第２として付される序数詞は便宜上用いるものであり、工程順又は積層順を示すものではない。また、本明細書において発明を特定するための事項として固有の名称を示すものではない。
【発明の効果】
【００３９】
基板の基板面とソース電極の側面とがなす角と、基板の基板面とドレイン電極の側面とがなす角を調節することで、ソース電極及びドレイン電極上に設けられる酸化物半導体層の被覆性を向上させる。
【００４０】
電界集中緩和領域を設けることにより、ソース電極とドレイン電極間に生じる恐れのある電界集中を緩和し、薄膜トランジスタのスイッチング特性の劣化を抑える。
【発明を実施するための最良の形態】
【００４１】
本実施形態について、以下に説明する。
【００４２】
（実施の形態１）
図１に薄膜トランジスタ１７０を基板上に設ける例を示す。なお、図１は薄膜トランジスタの断面図の一例である。
【００４３】
絶縁表面を有する基板１００上に設けられたゲート電極１０１は、ゲート絶縁層１０２に覆われ、ゲート電極１０１と重なるゲート絶縁層１０２上には第１配線または第２配線が設けられる。ソース電極層１０５ａまたはドレイン電極層１０５ｂとして機能する第１配線または第２配線上には、バッファ層がそれぞれ設けられている。ソース電極層１０５ａ上には第１のバッファ層１０４ａが設けられ、ドレイン電極層１０５ｂ上には第２のバッファ層１０４ｂが設けられている。そして、第１のバッファ層１０４ａ、及び第２のバッファ層１０４ｂ上には酸化物半導体層１０３を有する。
【００４４】
図１において、透光性を有する基板１００にはコーニング社の７０５９ガラスや１７３７ガラスなどに代表されるバリウムホウケイ酸ガラスやアルミノホウケイ酸ガラスなどのガラス基板を用いることができる。
【００４５】
ゲート電極１０１は、単層、または異なる金属材料からなる積層とする。また、ゲート電極１０１の材料は金属材料（アルミニウム（Ａｌ）、銅（Ｃｕ）、チタン（Ｔｉ）、タンタル（Ｔａ）、タングステン（Ｗ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）、Ｎｄ（ネオジム）、Ｓｃ（スカンジウム）から選ばれた元素、または上述した元素を成分とする合金）を用い、ゲート電極１０１の側面の角度を２０°以上９０°未満とする。少なくとも端

部にテーパー形状が形成されるようにエッチングしてゲート電極１０１を形成する。
【００４６】
また、ゲート絶縁層１０２はスパッタ法またはプラズマＣＶＤ法で得られる酸化シリコン膜、酸化窒化シリコン膜、窒化シリコン膜、酸化アルミニウム、酸化タンタル膜などの絶縁膜を用い、これらの材料から成る単層または積層構造として形成しても良い。なお、ゲート絶縁層１０２上に形成するソース電極層１０５ａ及びドレイン電極層１０５ｂをエッチングする際に、選択比が十分に取れる材料を選択することが好ましい。また、ソース電極層１０５ａ及びドレイン電極層１０５ｂをエッチングする際にゲート絶縁層１０２の表面が２０ｎｍ程度までエッチングされてもよく、金属材料のエッチング残渣をなくすためには少し表層を除去することが好ましい。
【００４７】
ソース電極層１０５ａ及びドレイン電極層１０５ｂは、単層、または異なる金属材料からなる積層とする。ソース電極層１０５ａ及びドレイン電極層１０５ｂの材料は金属材料（アルミニウム（Ａｌ）、銅（Ｃｕ）、チタン（Ｔｉ）、タンタル（Ｔａ）、タングステン（Ｗ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）、Ｎｄ（ネオジム）、Ｓｃ（スカンジウム）から選ばれた元素、または上述した元素を成分とする合金）を用いる。
【００４８】
ソース電極層１０５ａの断面形状は、図１に示すように、基板の基板面とソース電極層１０５ａの側面とがなす角度θ１が２０°以上９０°未満とする。また、ドレイン電極層１０５ｂの断面形状は、図１に示すように、基板の基板面とドレイン電極層１０５ｂの側面とがなす角度θ２が２０°以上９０°未満とする。同じエッチング工程（ドライエッチングまたはウェットエッチング）により形成されるため、角度θ１と角度θ２はほぼ同一である。酸化物半導体層と接するソース電極層１０５ａの側面の角度θ１及びドレイン電極層１０５ｂの側面の角度θ２を２０°以上９０°未満とすることで、ソース電極層１０５ａ及びドレイン電極層１０５ｂの側面における電極上端から電極下端までの距離を大きくする。
【００４９】
なお、図１では基板の裏面平面を基板面として角度θ１、角度θ２を表記しているが、特に限定されず、基板の表面平面を基板面としても基板の裏面平面と表面平面は平行であるため同じ角度となることは言うまでもない。
【００５０】
このような形状のソース電極層１０５ａ及びドレイン電極層１０５ｂ上に酸化物半導体層１０３を形成する。酸化物半導体層１０３は、Ｉｎ、Ｇａ、及びＺｎを含む酸化物半導体ターゲット（$Ｉｎ_2Ｏ_3$：$Ｇａ_2Ｏ_3$：ＺｎＯ＝１：１：１）を用いて、基板とターゲットの間との距離を１７０ｍｍ、圧力０．４Ｐａ、直流（ＤＣ）電源０．５ｋＷ、酸素を含むアルゴン雰囲気下で成膜した後、レジストマスクを形成して選択的にエッチングし、不要な部分を除去して形成する。なお、パルス直流（ＤＣ）電源を用いると、ごみが軽減でき、膜厚分布も均一となるために好ましい。酸化物半導体膜の膜厚は、５ｎｍ～２００ｎｍとする。本実施の形態では酸化物半導体膜の膜厚は、１００ｎｍとする。
【００５１】
なお、ソース電極層１０５ａと酸化物半導体層１０３の間には、第１のバッファ層１０４ａを設けることが好ましい。また、ドレイン電極層１０５ｂと酸化物半導体層１０３の間には、第２のバッファ層１０４ｂを設けることが好ましい。
【００５２】
第１のバッファ層１０４ａ、及び第２のバッファ層１０４ｂは、酸化物半導体層１０３に比べて低抵抗な酸化物半導体層（ｎ＋層）であり、ソース領域またはドレイン領域として機能する。
【００５３】
ｎ＋層は、$Ｉｎ_2Ｏ_3$：$Ｇａ_2Ｏ_3$：ＺｎＯ＝１：１：１としたターゲットを用い、成膜条件は、圧力を０．４Ｐａとし、電力を５００Ｗとし、成膜温度を室温とし、アルゴンガ

ス流量４０ｓｃｃｍを導入してスパッタ成膜を行う。In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１としたターゲットを意図的に用いているにも関わらず、成膜直後で大きさ１ｎｍ～１０ｎｍの結晶粒を含むＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜が形成されることがある。なお、ターゲットの成分比、成膜圧力（０．１Ｐａ～２．０Ｐａ）、電力（２５０Ｗ～３０００Ｗ：８インチφ）、温度（室温～１００℃）、反応性スパッタの成膜条件などを適宜調節することで結晶粒の有無や、結晶粒の密度や、直径サイズは、１ｎｍ～１０ｎｍの範囲で調節されうると言える。第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、５ｎｍ～２０ｎｍとする。勿論、膜中に結晶粒が含まれる場合、含まれる結晶粒のサイズが膜厚を超える大きさとならない。本実施の形態では第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、５ｎｍとする。

【００５４】

また、ソース電極層１０５ａ又はドレイン電極層１０５ｂとなる導電膜とn^+層となる酸化物半導体膜を大気に曝すことなくスパッタ法で積層することで製造プロセス中にソース電極層又はドレイン電極層が露呈してゴミが付着することを防止することができる。

【００５５】

スパッタ法で得られる酸化物半導体層１０３は、被成膜面との界面近傍の膜質が、被成膜面の材料に影響を受ける傾向がある。酸化物半導体層は、n^+層との界面、ソース電極層側面（及びドレイン電極層側面）との界面、ゲート絶縁膜との界面とを有し、異なる材料との界面を少なくとも３つ有する。従って、酸化物半導体層１０３において、ドレイン電極側面の自然酸化膜と界面状態と、ゲート絶縁膜との界面状態は異なるため、ドレイン電極層側面の界面近傍の酸化物半導体層が第１の電界集中緩和領域１０６ａとして機能する。また、ソース電極側面の自然酸化膜と界面状態と、ゲート絶縁膜との界面状態は異なるため、ソース電極側面の界面近傍の酸化物半導体層が第２の電界集中緩和領域１０６ｂとして機能する。

酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とし、ソース電極及びドレイン電極の側面における電極上端から電極下端までの距離を大きくすることによって第１の電界集中緩和領域１０６ａの長さＬ１及び第２電界集中緩和領域１０６ｂの長さＬ２を長くして電界集中を緩和させる。さらに、ソース電極及びドレイン電極の膜厚を厚くすることによっても電極側面における電極上端から電極下端までの距離を大きくできる。

【００５６】

また、酸化物半導体層１０３をスパッタ法で成膜する場合、基板面に垂直な電極側面に成膜される膜厚は、電極上面に成膜される膜厚よりも薄くなる恐れがある。酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とすることで側面においても膜厚の均一性を高めることができ、酸化物半導体層１０３が局所的に薄くなる領域を低減し、電界集中を緩和することもできる。

【００５７】

（実施の形態２）

図１では、ソース電極層（ドレイン電極層）側面の下端を始点としソース電極層（ドレイン電極層）側面の上端を結んだ直線がソース電極（ドレイン電極層）側面にほぼ一致する例を示したが、本実施の形態では、ソース電極層（ドレイン電極層）側面に段差を有する例を図２を用いて説明する。少なくともソース電極層の下端部の側面の角度θ１、及びドレイン電極層の下端部の側面の角度θ２が２０°以上９０°未満であれば、電極側面に段差を有してもよい。なお、図２において図１と共通の部分には同じ符号を用いる。

【００５８】

絶縁表面を有する基板１００上に設けられたゲート電極１０１は、ゲート絶縁層１０２に覆われ、ゲート電極１０１と重なるゲート絶縁層１０２上には第１配線または第２配線が設けられる。ソース電極層４０５ａまたはドレイン電極層４０５ｂとして機能する第１配線または第２配線上には、バッファ層がそれぞれ設けられている。ソース電極層４０５ａ上には第１のバッファ層４０４ａが設けられ、ドレイン電極層４０５ｂ上には第２のバッ

ファ層４０４ｂが設けられている。そして、第１のバッファ層４０４ａ、及び第２のバッファ層４０４ｂ上には酸化物半導体層４０３を有する。
【００５９】
絶縁表面を有する基板１００、ゲート電極１０１、及びゲート絶縁層１０２に関しては実施の形態１と同一であるため、ここでは詳細な説明は省略する。
【００６０】
また、ソース電極層４０５ａ及びドレイン電極層４０５ｂは、単層、または異なる金属材料からなる積層とする。ソース電極層４０５ａ及びドレイン電極層４０５ｂの材料は金属材料（アルミニウム（Ａｌ）、銅（Ｃｕ）、チタン（Ｔｉ）、タンタル（Ｔａ）、タングステン（Ｗ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）、Ｎｄ（ネオジム）、Ｓｃ（スカンジウム）から選ばれた元素、または上述した元素を成分とする合金）を用いる。
【００６１】
ここではソース電極層４０５ａ及びドレイン電極層４０５ｂとして膜厚１００ｎｍのタングステン膜の単層を用い、コイル状アンテナを用いるＩＣＰエッチング装置を用いて図２に示すソース電極層４０５ａの側面形状、及びドレイン電極層４０５ｂの側面形状を形成する例を説明する。
【００６２】
本実施の形態では、CF_4のガス流量を２５（ｓｃｃｍ）、Cl_3のガス流量を２５（ｓｃｃｍ）、O_2のガス流量を１０（ｓｃｃｍ）とし、１．５Ｐａの圧力でコイル型の電極に５００ＷのＲＦ（１３．５６ＭＨｚ）電力を投入してプラズマを生成してエッチングを行う。基板側（試料ステージ）にも１０ＷのＲＦ（１３．５６ＭＨｚ）電力を投入し、実質的に負の自己バイアス電圧を印加する。少なくともゲート絶縁膜１０２がある程度露呈した段階で、このエッチングを途中で停止することにより、段差を有する電極側面が形成される。
【００６３】
上記エッチング条件により、ソース電極層４０５ａの断面形状は、基板の基板面とソース電極層４０５ａの下端部側面とがなす角度θ１が２０°以上９０°未満とすることができ、図２に示すように、θ１は約４０°である。また、基板の基板面とソース電極層４０５ａの上端部側面とがなす角度は約９０°である。なお、酸化物半導体層４０３を挟んで対向するソース電極層４０５ａ側面とドレイン電極層４０５ｂ側面の断面形状は同じエッチング工程を経るため、ほぼ同一である。
【００６４】
このように、ソース電極層４０５ａ（及びドレイン電極層４０５ｂ）上端部の側面の角度をソース電極層４０５ａ（及びドレイン電極層４０５ｂ）下端部の側面の角度よりも大きくすることで、ソース電極層４０５ａ及びドレイン電極層４０５ｂを形成するためのフォトマスク（またはレジストマスク）の間隔を狭く設計することができ、結果としてチャネル長を短く設計する、例えばチャネル長を１μｍ～１０μｍに設計することができる。
【００６５】
また、上述した方法に限定されず、ソース電極層４０５ａ及びドレイン電極層４０５ｂとして用いるエッチングガスのエッチングレートが異なる材料を積層させ、下層にエッチングレートの低い材料層、上層にエッチングレートの高い材料層とし、エッチングを行うと電極側面に段差を形成することができる。
【００６６】
酸化物半導体層４０３を挟んで対向する２つの電極側面に段差を持たせることにより、ソース電極層及びドレイン電極層の側面における電極上端から電極下端までの距離を大きくすることによって第１の電界集中緩和領域４０６ａの長さＬ３及び第２電界集中緩和領域４０６ｂの長さＬ４を長くして電界集中を緩和させる。
【００６７】
さらにソース電極層及びドレイン電極層の側面における電極上端から電極下端までの距離を大きくするため、上述したドライエッチング後に、さらにウェットエッチングを行って

酸化物半導体層４０３を挟んで対向する２つの電極側面の一部に曲面を持たせてもよい。
【００６８】
また、上述したドライエッチングではなく、ソース電極層及びドレイン電極層の形成をウェットエッチングを行って、少なくともソース電極層の下端部の側面の角度θ１、及びドレイン電極層の下端部の側面の角度θ２が２０°以上９０°未満としてもよく、電極上面から基板に向かって裾広がりの断面形状としてもよい。
【００６９】
また、本実施の形態は実施の形態１と自由に組み合わせることができる。
【００７０】
（実施の形態３）
本実施の形態では、薄膜トランジスタ及びその作製工程について、図３乃至図９を用いて説明する。
【００７１】
図３（Ａ）において、透光性を有する基板１００にはコーニング社の＃７０５９ガラスや＃１７３７ガラスなどに代表されるバリウムホウケイ酸ガラスやアルミノホウケイ酸ガラスなどのガラス基板を用いることができる。
【００７２】
次いで、導電層を基板１００全面に形成した後、第１のフォトリソグラフィー工程を行い、レジストマスクを形成し、エッチングにより不要な部分を除去して配線及び電極（ゲート電極１０１を含むゲート配線、容量配線１０８、及び第１の端子１２１）を形成する。このとき少なくともゲート電極１０１の端部にテーパー形状が形成されるようにエッチングする。この段階での上面図を図３（Ａ）に示した。なお、この段階での上面図が図５に相当する。
【００７３】
ゲート電極１０１を含むゲート配線と容量配線１０８、端子部の第１の端子１２１は、チタン（Ｔｉ）、タンタル（Ｔａ）、タングステン（Ｗ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）、Ｎｄ（ネオジム）、アルミニウム（Ａｌ）、銅（Ｃｕ）から選ばれた元素、または上述した元素を成分とする合金か、上述した元素を組み合わせた合金膜、または上述した元素を成分とする窒化物で形成する。中でもアルミニウム（Ａｌ）や銅（Ｃｕ）などの低抵抗導電性材料で形成することが望ましいが、Ａｌ単体では耐熱性が劣り、また腐蝕しやすい等の問題点があるのでチタン（Ｔｉ）、タンタル（Ｔａ）、タングステン（Ｗ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）、Ｎｄ（ネオジム）から選ばれた元素、または上述した元素を組み合わせた合金膜、または上述した元素を成分とする窒化物で形成する。
【００７４】
次いで、ゲート電極１０１上にゲート絶縁層１０２を全面に成膜する。ゲート絶縁層１０２はスパッタ法などを用い、膜厚を５０～２５０ｎｍとする。
【００７５】
例えば、ゲート絶縁層１０２としてスパッタ法により酸化シリコン膜を用い、１００ｎｍの厚さで形成する。勿論、ゲート絶縁層１０２はこのような酸化シリコン膜に限定されるものでなく、酸化窒化シリコン膜、窒化シリコン膜、酸化アルミニウム、酸化タンタル膜などの他の絶縁膜を用い、これらの材料から成る単層または積層構造として形成しても良い。
【００７６】
次に、ゲート絶縁層１０２上に金属材料からなる導電膜をスパッタ法や真空蒸着法で形成する。導電膜の材料としては、Ａｌ、Ｃｒ、Ｔａ、Ｔｉ、Ｍｏ、Ｗから選ばれた元素、または上述した元素を成分とする合金か、上述した元素を組み合わせた合金膜等が挙げられる。ここでは、導電膜としてアルミニウム（Ａｌ）膜と、そのアルミニウム（Ａｌ）膜上に重ねてＴｉ膜を積層する。また、導電膜は、３層構造としてもよく、タングステン膜上にチタン膜を積層してもよい。また、導電膜は、シリコンを含むアルミニウム膜の単層構造や、タングステン膜の単層構造としてもよい。

【００７７】
次に、導電膜上に第１の酸化物半導体膜（本実施の形態では第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜）をスパッタ法で成膜する。ここでは、In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１としたターゲットを用い、成膜条件は、圧力を０．４Ｐａとし、電力を５００Ｗとし、成膜温度を室温とし、アルゴンガス流量４０ｓｃｃｍを導入してスパッタ成膜を行う。In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１としたターゲットを意図的に用いているにも関わらず、成膜直後で大きさ１ｎｍ～１０ｎｍの結晶粒を含むＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜が形成されることがある。なお、ターゲットの成分比、成膜圧力（０．１Ｐａ～２．０Ｐａ）、電力（２５０Ｗ～３０００Ｗ：８インチφ）、温度（室温～１００℃）、反応性スパッタの成膜条件などを適宜調節することで結晶粒の有無や、結晶粒の密度や、直径サイズは、１ｎｍ～１０ｎｍの範囲で調節されうると言える。第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、５ｎｍ～２０ｎｍとする。勿論、膜中に結晶粒が含まれる場合、含まれる結晶粒のサイズが膜厚を超える大きさとならない。本実施の形態では第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、５ｎｍとする。
【００７８】
次に、第２のフォトリソグラフィー工程を行い、レジストマスクを形成し、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜をエッチングする。ここではＩＴＯ０７Ｎ（関東化学社製）を用いたウェットエッチングにより、画素部において、不要な部分を除去して第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜１１１ａ、１１１ｂを形成する。なお、ここでのエッチングは、ウェットエッチングに限定されずドライエッチングを用いてもよい。
【００７９】
次に、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜のエッチングと同じレジストマスクを用いて、エッチングにより不要な部分を除去してソース電極層１０５ａ及びドレイン電極層１０５ｂを形成する。この際のエッチング方法としてウエットエッチングまたはドライエッチングを用いる。ここでは、$SiCl_4$とCl_2とBCl_3の混合ガスを反応ガスとしたドライエッチングにより、Ａｌ膜とＴｉ膜を積層した導電膜をエッチングしてソース電極層１０５ａ及びドレイン電極層１０５ｂを形成する。この段階での断面図を図３（Ｂ）に示した。なお、この段階での上面図が図６に相当する。
【００８０】
ここでのエッチングにより、後に形成する酸化物半導体層と接するソース電極層１０５ａの側面の角度θ１及びドレイン電極層１０５ｂの側面の角度θ２を２０°以上９０°未満とする。酸化物半導体層を挟んで対向する２つの電極側面をテーパ形状とすることで、酸化物半導体層におけるソース電極層の側面及びドレイン電極層の側面と重なる領域は、電界集中緩和領域として機能させることができる。
【００８１】
また、この第２のフォトリソグラフィー工程において、ソース電極層１０５ａ及びドレイン電極層１０５ｂと同じ材料である第２の端子１２２を端子部に残す。なお、第２の端子１２２はソース配線（ソース電極層１０５ａを含むソース配線）と電気的に接続されている。また、端子部において、第２の端子１２２の上方に存在し、且つ、第２の端子と重なる第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜１２３は残存する。
【００８２】
また、容量部においては、ソース電極層１０５ａ及びドレイン電極層１０５ｂと同じ材料である容量電極層１２４を残す。また、容量部において、容量電極層１２４の上方に存在し、且つ、容量電極層１２４と重なる第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜１１１ｃは残存する。
【００８３】
次に、レジストマスクを除去した後、大気に曝すことなく第２の酸化物半導体膜（本実施の形態では第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜）を成膜する。プラズマ処理後、大気に曝すことなく第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を成膜することは、ゲート絶縁層と半導体膜の界面にゴミなどを付着させない点で有用である。ここでは、直径８イン

チのＩｎ、Ｇａ、及びＺｎを含む酸化物半導体ターゲット（$Ｉｎ_2Ｏ_3$：$Ｇａ_2Ｏ_3$：ＺｎＯ＝１：１：１）を用いて、基板とターゲットの間との距離を１７０ｍｍ、圧力０．４Ｐａ、直流（ＤＣ）電源０．５ｋＷ、アルゴン又は酸素雰囲気下で成膜する。なお、パルス直流（ＤＣ）電源を用いると、ごみが軽減でき、膜厚分布も均一となるために好ましい。第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、５ｎｍ～２００ｎｍとする。本実施の形態では第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の膜厚は、１００ｎｍとする。

【００８４】
第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜は、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜条件と異ならせることで、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜よりも電気抵抗の高い膜とする。例えば、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜条件における酸素ガス流量とアルゴンガス流量の比よりも第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜条件における酸素ガス流量の占める比率が多い条件とする。具体的には、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜条件は、希ガス（アルゴン、又はヘリウムなど）雰囲気下（または酸素ガス１０％以下、アルゴンガス９０％以上）とし、第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜条件は、酸素雰囲気下（又は酸素ガス流量とアルゴンガス流量の比１：１以上）とする。

【００８５】
次いで、２００℃～６００℃、代表的には３００℃～５００℃の熱処理を行うことが好ましい。ここでは炉に入れ、窒素雰囲気または大気雰囲気下で３５０℃、１時間の熱処理を行う。この熱処理によりＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の原子レベルの再配列が行われる。この熱処理によりキャリアの移動を阻害する歪が解放されるため、ここでの熱処理（光アニールも含む）は重要である。なお、熱処理を行うタイミングは、第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の成膜後であれば特に限定されず、例えば画素電極形成後に行ってもよい。

【００８６】
次に、第３のフォトリソグラフィー工程を行い、レジストマスクを形成し、エッチングにより不要な部分を除去して半導体層１０３を形成する。ここではＩＴＯ０７Ｎ（関東化学社製）を用いたウェットエッチングにより、第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を除去して半導体層１０３を形成する。ウェットエッチングで除去する場合、エッチングの廃液から酸化物半導体を再生して、ターゲットの作製に再利用することができる。

【００８７】
酸化物半導体に含まれているインジウムやガリウムは、希少価値のある金属であることが知られており、再利用することによって、省資源化を図るとともに酸化物半導体を用いて形成される製品のコストダウンを図ることができる。

【００８８】
なお、第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜と第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜は同じエッチャントを用いるため、ここでのエッチングにより第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜が除去される。従って、第２のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜で覆われた第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の側面は保護されるが、図４（Ａ）に示すように、露呈している第１のＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜１１１ａ、１１１ｂはエッチングされ、第１のバッファ層１０４ａ、第２のバッファ層１０４ｂが形成される。なお、半導体層１０３のエッチングは、ウェットエッチングに限定されずドライエッチングを用いてもよい。以上の工程で半導体層１０３をチャネル形成領域とする薄膜トランジスタ１７０が作製できる。この段階での断面図を図４（Ａ）に示した。なお、この段階での上面図が図７に相当する。

【００８９】
次いで、レジストマスクを除去し、半導体層を覆う保護絶縁膜１０７を形成する。保護絶縁膜１０７はスパッタ法などを用いて得られる窒化シリコン膜、酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウム膜、酸化窒化アルミニウム膜、酸化タンタル膜などを用いることができる。

【００９０】
次に、第４のフォトリソグラフィー工程を行い、レジストマスクを形成し、保護絶縁膜１０７のエッチングによりドレイン電極層１０５ｂに達するコンタクトホール１２５を形成する。また、ここでのエッチングにより第２の端子１２２に達するコンタクトホール１２７も形成する。また、ここでのエッチングにより容量電極層１２４に達するコンタクトホール１０９も形成する。なお、マスク数を削減するため、同じレジストマスクを用いてさらにゲート絶縁層をエッチングしてゲート電極に達するコンタクトホール１２６も同じレジストマスクで形成することが好ましい。この段階での断面図を図４（Ｂ）に示す。
【００９１】
次いで、レジストマスクを除去した後、透明導電膜を成膜する。透明導電膜の材料としては、酸化インジウム（$Ｉｎ_２Ｏ_３$）や酸化インジウム酸化スズ合金（$Ｉｎ_２Ｏ_３－ＳｎＯ_２$、ＩＴＯと略記する）などをスパッタ法や真空蒸着法などを用いて形成する。このような材料のエッチング処理は塩酸系の溶液により行う。しかし、特にＩＴＯのエッチングは残渣が発生しやすいので、エッチング加工性を改善するために酸化インジウム酸化亜鉛合金（$Ｉｎ_２Ｏ_３－ＺｎＯ$）を用いても良い。
【００９２】
次に、第５のフォトリソグラフィー工程を行い、レジストマスクを形成し、エッチングにより不要な部分を除去して画素電極１１０を形成する。
【００９３】
また、この第５のフォトリソグラフィー工程において、容量部におけるゲート絶縁層１０２を誘電体として、容量電極層１２４と画素電極１１０とで保持容量が形成される。容量配線１０８はコンタクトホール１０９を介して容量電極層１２４と電気的に接続する。
【００９４】
また、この第５のフォトリソグラフィー工程において、第１の端子及び第２の端子をレジストマスクで覆い端子部に形成された透明導電膜１２８、１２９を残す。透明導電膜１２８、１２９はＦＰＣとの接続に用いられる電極または配線となる。第２の端子１２２上に形成された透明導電膜１２９は、ソース配線の入力端子として機能する接続用の端子電極である。
【００９５】
次いで、レジストマスクを除去し、この段階での断面図を図４（Ｃ）に示す。なお、この段階での上面図が図８に相当する。
【００９６】
また、図９（Ａ１）、図９（Ａ２）は、この段階でのゲート配線端子部の上面図及び断面図をそれぞれ図示している。図９（Ａ１）は図９（Ａ２）中のＣ１－Ｃ２線に沿った断面図に相当する。図９（Ａ１）において、保護絶縁膜１５４上に形成される透明導電膜１５５は、入力端子として機能する接続用の端子電極である。また、図９（Ａ１）において、端子部では、ゲート配線と同じ材料で形成される第１の端子１５１と、ソース配線と同じ材料で形成される接続電極１５３とがゲート絶縁層１５２を介して重なり、透明導電膜１５５で導通させている。なお、図４（Ｃ）に図示した透明導電膜１２８と第１の端子１２１とが接触している部分が、図９（Ａ１）の透明導電膜１５５と第１の端子１５１が接触している部分に対応している。
【００９７】
また、図９（Ｂ１）、及び図９（Ｂ２）は、図４（Ｃ）に示すソース配線端子部とは異なるソース配線端子部の上面図及び断面図をそれぞれ図示している。また、図９（Ｂ１）は図９（Ｂ２）中のＤ１－Ｄ２線に沿った断面図に相当する。図９（Ｂ１）において、保護絶縁膜１５４上に形成される透明導電膜１５５は、入力端子として機能する接続用の端子電極である。また、図９（Ｂ１）において、端子部では、ゲート配線と同じ材料で形成される電極１５６が、ソース配線と電気的に接続される第２の端子１５０の下方にゲート絶縁層１０２を介して重なる。電極１５６は第２の端子１５０とは電気的に接続しておらず、電極１５６を第２の端子１５０と異なる電位、例えばフローティング、ＧＮＤ、０Ｖな

どに設定すれば、ノイズ対策のための容量または静電気対策のための容量を形成することができる。また、第２の端子１５０は、保護絶縁膜１５４を介して透明導電膜１５５と電気的に接続している。

【００９８】

ゲート配線、ソース配線、及び容量配線は画素密度に応じて複数本設けられるものである。また、端子部においては、ゲート配線と同電位の第１の端子、ソース配線と同電位の第２の端子、容量配線と同電位の第３の端子などが複数並べられて配置される。それぞれの端子の数は、それぞれ任意な数で設ければ良いものとし、実施者が適宜決定すれば良い。

【００９９】

こうして５回のフォトリソグラフィー工程により、５枚のフォトマスクを使用して、ボトムゲート型のｎチャネル型薄膜トランジスタである薄膜トランジスタ１７０を有する画素薄膜トランジスタ部、保持容量を完成させることができる。そして、これらを個々の画素に対応してマトリクス状に配置して画素部を構成することによりアクティブマトリクス型の表示装置を作製するための一方の基板とすることができる。本明細書では便宜上このような基板をアクティブマトリクス基板と呼ぶ。

【０１００】

アクティブマトリクス型の液晶表示装置を作製する場合には、アクティブマトリクス基板と、対向電極が設けられた対向基板との間に液晶層を設け、アクティブマトリクス基板と対向基板とを固定する。なお、対向基板に設けられた対向電極と電気的に接続する共通電極をアクティブマトリクス基板上に設け、共通電極と電気的に接続する第４の端子を端子部に設ける。この第４の端子は、共通電極を固定電位、例えばＧＮＤ、０Ｖなどに設定するための端子である。

【０１０１】

また、本実施の形態は、図８の画素構成に限定されず、図８とは異なる上面図の例を図１０に示す。図１０では容量配線を設けず、ゲート絶縁層を誘電体として画素電極を隣り合う画素のゲート配線とゲート絶縁層を介して重なる容量電極層とで保持容量を形成する例であり、この場合、容量配線及び容量配線と接続する第３の端子は省略することができる。なお、図１０において、図８と同じ部分には同じ符号を用いて説明する。

【０１０２】

アクティブマトリクス型の液晶表示装置においては、マトリクス状に配置された画素電極を駆動することによって、画面上に表示パターンが形成される。詳しくは選択された画素電極と該画素電極に対応する対向電極との間に電圧が印加されることによって、画素電極と対向電極との間に配置された液晶層の光学変調が行われ、この光学変調が表示パターンとして観察者に認識される。

【０１０３】

液晶表示装置の動画表示において、液晶分子自体の応答が遅いため、残像が生じる、または動画のぼけが生じるという問題がある。液晶表示装置の動画特性を改善するため、全面黒表示を１フレームおきに行う、所謂、黒挿入と呼ばれる駆動技術がある。

【０１０４】

また、通常の垂直周期を１．５倍若しくは２倍以上にすることで応答速度を改善するとともに各フレーム内の分割された複数フィールド毎に書き込む階調を選択する、所謂、倍速駆動と呼ばれる駆動技術もある。

【０１０５】

また、液晶表示装置の動画特性を改善するため、バックライトとして複数のＬＥＤ（発光ダイオード）光源または複数のＥＬ光源などを用いて面光源を構成し、面光源を構成している各光源を独立して１フレーム基板内で間欠点灯駆動する駆動技術もある。面光源として、３種類以上のＬＥＤを用いてもよいし、白色発光のＬＥＤを用いてもよい。独立して複数のＬＥＤを制御できるため、液晶層の光学変調の切り替えタイミングに合わせてＬＥＤの発光タイミングを同期させることもできる。この駆動技術は、ＬＥＤを部分的に消灯することができるため、特に一画面を占める黒い表示領域の割合が多い映像表示の場合に

は、消費電力の低減効果が図れる。
【０１０６】
これらの駆動技術を組み合わせることによって、液晶表示装置の動画特性などの表示特性を従来よりも改善することができる。
【０１０７】
本実施の形態で得られるｎチャネル型のトランジスタは、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜の半導体層をチャネル形成領域に用いており、良好な動特性を有するため、これらの駆動技術を組み合わせることができる。
【０１０８】
また、発光表示装置を作製する場合、有機発光素子の一方の電極（カソードとも呼ぶ）は、低電源電位、例えばＧＮＤ、０Ｖなどに設定するため、端子部に、カソードを低電源電位、例えばＧＮＤ、０Ｖなどに設定するための第４の端子が設けられる。また、発光表示装置を作製する場合には、ソース配線、及びゲート配線に加えて電源供給線を設ける。従って、端子部には、電源供給線と電気的に接続する第５の端子を設ける。
【０１０９】
本実施の形態では、ゲート電極層、ゲート絶縁層、ソース電極層及びドレイン電極層、ソース領域又はドレイン領域（Ｉｎ、Ｇａ、及びＺｎを含む酸化物半導体層）、半導体層（Ｉｎ、Ｇａ、及びＺｎを含む酸化物半導体層）という積層構造を有する薄膜トランジスタとし、ゲート絶縁層表面をプラズマ処理で改質することによって、半導体層の膜厚を薄膜にしたままで、かつ寄生容量を抑制できる。なお、薄膜であっても、ゲート絶縁層に対する割合が十分であるため寄生容量は十分に抑制される。
【０１１０】
本実施の形態によって、オンオフ比の高い薄膜トランジスタを得ることができ、良好な動特性を有する薄膜トランジスタを作製できる。よって、電気特性が高く信頼性のよい薄膜トランジスタを有する半導体装置を提供することができる。
【０１１１】
（実施の形態４）
本実施の形態では、半導体装置として電子ペーパーの例を示す。
【０１１２】
図１１は、液晶表示装置とは異なる半導体装置の例としてアクティブマトリクス型の電子ペーパーを示す。半導体装置の画素部に用いられる薄膜トランジスタ５８１としては、実施の形態３で示す画素部の薄膜トランジスタと同様に作製でき、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を半導体層として含む薄膜トランジスタである。また、実施の形態１に示したように、酸化物半導体層を挟んで対向する２つの電極側面をテーパ形状とすることで、電界緩和領域が設けられた信頼性の高い薄膜トランジスタを備えた電子ペーパを実現することができる。
【０１１３】
図１１の電子ペーパーは、ツイストボール表示方式を用いた表示装置の例である。ツイストボール表示方式とは、白と黒に塗り分けられた球形粒子を表示素子に用いる電極層である第１の電極層及び第２の電極層の間に配置し、第１の電極層及び第２の電極層に電位差を生じさせて球形粒子の向きを制御することにより、表示を行う方法である。
【０１１４】
薄膜トランジスタ５８１はボトムゲート構造の薄膜トランジスタであり、ソース電極層又はドレイン電極層は、第１の電極層５８７と、絶縁層５８５に形成する開口で接しており電気的に接続している。第１の電極層５８７と第２の電極層５８８との間には黒色領域５９０ａ及び白色領域５９０ｂを有し、周りに液体で満たされているキャビティ５９４を含む球形粒子５８９が設けられており、球形粒子５８９の周囲は樹脂等の充填材５９５で充填されている（図１１参照。）。
【０１１５】
また、ツイストボールの代わりに、電気泳動素子を用いることも可能である。透明な液体

と、正に帯電した白い微粒子と負に帯電した黒い微粒子とを封入した直径１０μｍ～２０
０μｍ程度のマイクロカプセルを用いる。第１の電極層と第２の電極層との間に設けられ
るマイクロカプセルは、第１の電極層と第２の電極層によって、電場が与えられると、白
い微粒子と、黒い微粒子が逆の方向に移動し、白または黒を表示することができる。この
原理を応用した表示素子が電気泳動表示素子であり、電子ペーパーとよばれている。電気
泳動表示素子は、液晶表示素子に比べて反射率が高いため、補助ライトは不要であり、ま
た消費電力が小さく、薄暗い場所でも表示部を認識することが可能である。また、表示部
に電源が供給されない場合であっても、一度表示した像を保持することが可能であるため
、電波発信源から表示機能付き半導体装置（単に表示装置、又は表示装置を具備する半導
体装置ともいう）を遠ざけた場合であっても、表示された像を保存しておくことが可能と
なる。

【０１１６】
以上の工程により、半導体装置として製造コストが低減された電子ペーパーを作製するこ
とができる。

【０１１７】
本実施の形態は、実施の形態１、実施の形態２、または実施の形態３に記載した構成と適
宜組み合わせて実施することが可能である。

【０１１８】
（実施の形態５）
本実施の形態では、半導体装置の一例である表示装置において、同一基板上に少なくとも
駆動回路の一部と、画素部に配置する薄膜トランジスタを作製する例について以下に説明
する。

【０１１９】
画素部に配置する薄膜トランジスタは、実施の形態１又は実施の形態２に従って形成する
。また、実施の形態１又は実施の形態２に示す薄膜トランジスタはｎチャネル型ＴＦＴで
あるため、駆動回路のうち、ｎチャネル型ＴＦＴで構成することができる駆動回路の一部
を画素部の薄膜トランジスタと同一基板上に形成する。

【０１２０】
半導体装置の一例であるアクティブマトリクス型液晶表示装置のブロック図の一例を図１
２（Ａ）に示す。図１２（Ａ）に示す表示装置は、基板５３００上に表示素子を備えた画
素を複数有する画素部５３０１と、各画素を選択する走査線駆動回路５３０２と、選択さ
れた画素へのビデオ信号の入力を制御する信号線駆動回路５３０３とを有する。

【０１２１】
また、実施の形態１又は実施の形態２に示す薄膜トランジスタは、ｎチャネル型ＴＦＴで
あり、ｎチャネル型ＴＦＴで構成する信号線駆動回路について図１３を用いて説明する。

【０１２２】
図１３に示す信号線駆動回路は、ドライバＩＣ５６０１、スイッチ群５６０２＿１～５６
０２＿Ｍ、第１の配線５６１１、第２の配線５６１２、第３の配線５６１３及び配線５６
２１＿１～５６２１＿Ｍを有する。スイッチ群５６０２＿１～５６０２＿Ｍそれぞれは、
第１の薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜
トランジスタ５６０３ｃを有する。

【０１２３】
ドライバＩＣ５６０１は第１の配線５６１１、第２の配線５６１２、第３の配線５６１３
及び配線５６２１＿１～５６２１＿Ｍに接続される。そして、スイッチ群５６０２＿１～
５６０２＿Ｍそれぞれは、第１の配線５６１１、第２の配線５６１２、第３の配線５６１
３及びスイッチ群５６０２＿１～５６０２＿Ｍそれぞれに対応した配線５６２１＿１～５
６２１＿Ｍに接続される。そして、配線５６２１＿１～５６２１＿Ｍそれぞれは、第１の
薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トラン
ジスタ５６０３ｃを介して、３つの信号線に接続される。例えば、Ｊ列目の配線５６２１
＿Ｊ（配線５６２１＿１～配線５６２１＿Ｍのうちいずれか一）は、スイッチ群５６０２

＿Ｊが有する第１の薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃを介して、信号線Ｓｊ－１、信号線Ｓｊ、信号線Ｓｊ＋１に接続される。
【０１２４】
なお、第１の配線５６１１、第２の配線５６１２、第３の配線５６１３には、それぞれ信号が入力される。
【０１２５】
なお、ドライバＩＣ５６０１は、単結晶基板上に形成されていることが望ましい。さらに、スイッチ群５６０２＿１～５６０２＿Ｍは、画素部と同一基板上に形成されていることが望ましい。したがって、ドライバＩＣ５６０１とスイッチ群５６０２＿１～５６０２＿ＭとはＦＰＣなどを介して接続するとよい。
【０１２６】
次に、図１３に示した信号線駆動回路の動作について、図１４のタイミングチャートを参照して説明する。なお、図１４のタイミングチャートは、ｉ行目の走査線Ｇｉが選択されている場合のタイミングチャートを示している。さらに、ｉ行目の走査線Ｇｉの選択期間は、第１のサブ選択期間Ｔ１、第２のサブ選択期間Ｔ２及び第３のサブ選択期間Ｔ３に分割されている。さらに、図１３の信号線駆動回路は、他の行の走査線が選択されている場合でも図１４と同様の動作をする。
【０１２７】
なお、図１４のタイミングチャートは、Ｊ列目の配線５６２１＿Ｊが第１の薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃを介して、信号線Ｓｊ－１、信号線Ｓｊ、信号線Ｓｊ＋１に接続される場合について示している。
【０１２８】
なお、図１４のタイミングチャートは、ｉ行目の走査線Ｇｉが選択されるタイミング、第１の薄膜トランジスタ５６０３ａのオン・オフのタイミング５７０３ａ、第２の薄膜トランジスタ５６０３ｂのオン・オフのタイミング５７０３ｂ、第３の薄膜トランジスタ５６０３ｃのオン・オフのタイミング５７０３ｃ及びＪ列目の配線５６２１＿Ｊに入力される信号５７２１＿Ｊを示している。
【０１２９】
なお、配線５６２１＿１～配線５６２１＿Ｍには第１のサブ選択期間Ｔ１、第２のサブ選択期間Ｔ２及び第３のサブ選択期間Ｔ３において、それぞれ別のビデオ信号が入力される。例えば、第１のサブ選択期間Ｔ１において配線５６２１＿Ｊに入力されるビデオ信号は信号線Ｓｊ－１に入力され、第２のサブ選択期間Ｔ２において配線５６２１＿Ｊに入力されるビデオ信号は信号線Ｓｊに入力され、第３のサブ選択期間Ｔ３において配線５６２１＿Ｊに入力されるビデオ信号は信号線Ｓｊ＋１に入力される。さらに、第１のサブ選択期間Ｔ１、第２のサブ選択期間Ｔ２及び第３のサブ選択期間Ｔ３において、配線５６２１＿Ｊに入力されるビデオ信号をそれぞれＤａｔａ＿ｊ－１、Ｄａｔａ＿ｊ、Ｄａｔａ＿ｊ＋１とする。
【０１３０】
図１４に示すように、第１のサブ選択期間Ｔ１において第１の薄膜トランジスタ５６０３ａがオンし、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊ－１が、第１の薄膜トランジスタ５６０３ａを介して信号線Ｓｊ－１に入力される。第２のサブ選択期間Ｔ２では、第２の薄膜トランジスタ５６０３ｂがオンし、第１の薄膜トランジスタ５６０３ａ及び第３の薄膜トランジスタ５６０３ｃがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊが、第２の薄膜トランジスタ５６０３ｂを介して信号線Ｓｊに入力される。第３のサブ選択期間Ｔ３では、第３の薄膜トランジスタ５６０３ｃがオンし、第１の薄膜トランジスタ５６０３ａ及び第２の薄膜トランジスタ５６０３ｂがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊ＋１が、第３の薄膜トランジスタ５６

０３ｃを介して信号線Ｓｊ＋１に入力される。
【０１３１】
以上のことから、図１３の信号線駆動回路は、１ゲート選択期間を３つに分割することで、１ゲート選択期間中に１つの配線５６２１から３つの信号線にビデオ信号を入力することができる。したがって、図１３の信号線駆動回路は、ドライバＩＣ５６０１が形成される基板と、画素部が形成されている基板との接続数を信号線の数に比べて約１／３にすることができる。接続数が約１／３になることによって、図１３の信号線駆動回路は、信頼性、歩留まりなどを向上できる。
【０１３２】
なお、図１３のように、１ゲート選択期間を複数のサブ選択期間に分割し、複数のサブ選択期間それぞれにおいて、ある１つの配線から複数の信号線それぞれにビデオ信号を入力することができれば、薄膜トランジスタの配置や数、駆動方法などは限定されない。
【０１３３】
例えば、３つ以上のサブ選択期間それぞれにおいて１つの配線から３つ以上の信号線それぞれにビデオ信号を入力する場合は、薄膜トランジスタ及び薄膜トランジスタを制御するための配線を追加すればよい。ただし、１ゲート選択期間を４つ以上のサブ選択期間に分割すると、１つのサブ選択期間が短くなる。したがって、１ゲート選択期間は、２つ又は３つのサブ選択期間に分割されることが望ましい。
【０１３４】
別の例として、図１５のタイミングチャートに示すように、１つの選択期間をプリチャージ期間Ｔｐ、第１のサブ選択期間Ｔ１、第２のサブ選択期間Ｔ２、第３の選択期間Ｔ３に分割してもよい。さらに、図１５のタイミングチャートは、ｉ行目の走査線Ｇｉが選択されるタイミング、第１の薄膜トランジスタ５６０３ａのオン・オフのタイミング５８０３ａ、第２の薄膜トランジスタ５６０３ｂのオン・オフのタイミング５８０３ｂ、第３の薄膜トランジスタ５６０３ｃのオン・オフのタイミング５８０３ｃ及びＪ列目の配線５６２１＿Ｊに入力される信号５８２１＿Ｊを示している。図１５に示すように、プリチャージ期間Ｔｐにおいて第１の薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃがオンする。このとき、配線５６２１＿Ｊに入力されるプリチャージ電圧Ｖｐが第１の薄膜トランジスタ５６０３ａ、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃを介してそれぞれ信号線Ｓｊ－１、信号線Ｓｊ、信号線Ｓｊ＋１に入力される。第１のサブ選択期間Ｔ１において第１の薄膜トランジスタ５６０３ａがオンし、第２の薄膜トランジスタ５６０３ｂ及び第３の薄膜トランジスタ５６０３ｃがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊ－１が、第１の薄膜トランジスタ５６０３ａを介して信号線Ｓｊ－１に入力される。第２のサブ選択期間Ｔ２では、第２の薄膜トランジスタ５６０３ｂがオンし、第１の薄膜トランジスタ５６０３ａ及び第３の薄膜トランジスタ５６０３ｃがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊが、第２の薄膜トランジスタ５６０３ｂを介して信号線Ｓｊに入力される。第３のサブ選択期間Ｔ３では、第３の薄膜トランジスタ５６０３ｃがオンし、第１の薄膜トランジスタ５６０３ａ及び第２の薄膜トランジスタ５６０３ｂがオフする。このとき、配線５６２１＿Ｊに入力されるＤａｔａ＿ｊ＋１が、第３の薄膜トランジスタ５６０３ｃを介して信号線Ｓｊ＋１に入力される。
【０１３５】
以上のことから、図１５のタイミングチャートを適用した図１３の信号線駆動回路は、サブ選択期間の前にプリチャージ選択期間を設けることによって、信号線をプリチャージできるため、画素へのビデオ信号の書き込みを高速に行うことができる。なお、図１５において、図１４と同様なものに関しては共通の符号を用いて示し、同一部分又は同様な機能を有する部分の詳細な説明は省略する。
【０１３６】
また、走査線駆動回路の構成について説明する。走査線駆動回路は、シフトレジスタ、バッファを有している。また場合によってはレベルシフタを有していても良い。走査線駆動

回路において、シフトレジスタにクロック信号（ＣＬＫ）及びスタートパルス信号（ＳＰ）が入力されることによって、選択信号が生成される。生成された選択信号はバッファにおいて緩衝増幅され、対応する走査線に供給される。走査線には、１ライン分の画素のトランジスタのゲート電極が接続されている。そして、１ライン分の画素のトランジスタを一斉にＯＮにしなくてはならないので、バッファは大きな電流を流すことが可能なものが用いられる。

【０１３７】

走査線駆動回路の一部に用いるシフトレジスタの一形態について図１６及び図１７を用いて説明する。

【０１３８】

図１６にシフトレジスタの回路構成を示す。図１６に示すシフトレジスタは、複数のフリップフロップ５７０１＿ｉ（フリップフロップ５７０１＿１～５７０１＿ｎのうちいずれか一）で構成される。また、第１のクロック信号、第２のクロック信号、スタートパルス信号、リセット信号が入力されて動作する。

【０１３９】

図１６のシフトレジスタの接続関係について説明する。図１６のシフトレジスタは、ｉ段目のフリップフロップ５７０１＿ｉ（フリップフロップ５７０１＿１～５７０１＿ｎのうちいずれか一）は、図１７に示した第１の配線５５０１が第７の配線５７１７＿ｉ－１に接続され、図１７に示した第２の配線５５０２が第７の配線５７１７＿ｉ＋１に接続され、図１７に示した第３の配線５５０３が第７の配線５７１７＿ｉに接続され、図１７に示した第６の配線５５０６が第５の配線５７１５に接続される。

【０１４０】

また、図１７に示した第４の配線５５０４が奇数段目のフリップフロップでは第２の配線５７１２に接続され、偶数段目のフリップフロップでは第３の配線５７１３に接続され、図１７に示した第５の配線５５０５が第４の配線５７１４に接続される。

【０１４１】

ただし、１段目のフリップフロップ５７０１＿１の図１７に示す第１の配線５５０１は第１の配線５７１１に接続され、ｎ段目のフリップフロップ５７０１＿ｎの図１７に示す第２の配線５５０２は第６の配線５７１６に接続される。

【０１４２】

なお、第１の配線５７１１、第２の配線５７１２、第３の配線５７１３、第６の配線５７１６を、それぞれ第１の信号線、第２の信号線、第３の信号線、第４の信号線と呼んでもよい。さらに、第４の配線５７１４、第５の配線５７１５を、それぞれ第１の電源線、第２の電源線と呼んでもよい。

【０１４３】

次に、図１６に示すフリップフロップの詳細について、図１７に示す。図１７に示すフリップフロップは、第１の薄膜トランジスタ５５７１、第２の薄膜トランジスタ５５７２、第３の薄膜トランジスタ５５７３、第４の薄膜トランジスタ５５７４、第５の薄膜トランジスタ５５７５、第６の薄膜トランジスタ５５７６、第７の薄膜トランジスタ５５７７及び第８の薄膜トランジスタ５５７８を有する。なお、第１の薄膜トランジスタ５５７１、第２の薄膜トランジスタ５５７２、第３の薄膜トランジスタ５５７３、第４の薄膜トランジスタ５５７４、第５の薄膜トランジスタ５５７５、第６の薄膜トランジスタ５５７６、第７の薄膜トランジスタ５５７７及び第８の薄膜トランジスタ５５７８は、ｎチャネル型トランジスタであり、ゲート・ソース間電圧（Ｖｇｓ）がしきい値電圧（Ｖｔｈ）を上回ったとき導通状態になるものとする。

【０１４４】

次に、図１６に示すフリップフロップの接続構成について、以下に示す。

【０１４５】

第１の薄膜トランジスタ５５７１の第１の電極（ソース電極またはドレイン電極の一方）が第５の配線５５０４に接続され、第１の薄膜トランジスタ５５７１の第２の電極（ソー

ス電極またはドレイン電極の他方）が第３の配線５５０３に接続される。

【０１４６】

第２の薄膜トランジスタ５５７２の第１の電極が第４の配線第６の配線５５０６に接続され、第２の薄膜トランジスタ５５７２第２の電極が第３の配線５５０３に接続される。

【０１４７】

第３の薄膜トランジスタ５５７３の第１の電極が第５の配線５５０５に接続され、第３の薄膜トランジスタ５５７３の第２の電極が第２の薄膜トランジスタ５５７２のゲート電極に接続され、第３の薄膜トランジスタ５５７３のゲート電極が第５の配線５５０５に接続される。

【０１４８】

第４の薄膜トランジスタ５５７４の第１の電極が第６の配線５５０６に接続され、第４の薄膜トランジスタ５５７４の第２の電極が第２の薄膜トランジスタ５５７２のゲート電極に接続され、第４の薄膜トランジスタ５５７４のゲート電極が第１の薄膜トランジスタ５５７１のゲート電極に接続される。

【０１４９】

第５の薄膜トランジスタ５５７５の第１の電極が第５の配線５５０５に接続され、第５の薄膜トランジスタ５５７５の第２の電極が第１の薄膜トランジスタ５５７１のゲート電極に接続され、第５の薄膜トランジスタ５５７５のゲート電極が第１の配線５５０１に接続される。

【０１５０】

第６の薄膜トランジスタ５５７６の第１の電極が第６の配線５５０６に接続され、第６の薄膜トランジスタ５５７６の第２の電極が第１の薄膜トランジスタ５５７１のゲート電極に接続され、第６の薄膜トランジスタ５５７６のゲート電極が第２の薄膜トランジスタ５５７２のゲート電極に接続される。

【０１５１】

第７の薄膜トランジスタ５５７７の第１の電極が第６の配線５５０６に接続され、第７の薄膜トランジスタ５５７７の第２の電極が第１の薄膜トランジスタ５５７１のゲート電極に接続され、第７の薄膜トランジスタ５５７７のゲート電極が第２の配線５５０２に接続される。第８の薄膜トランジスタ５５７８の第１の電極が第６の配線５５０６に接続され、第８の薄膜トランジスタ５５７８の第２の電極が第２の薄膜トランジスタ５５７２のゲート電極に接続され、第８の薄膜トランジスタ５５７８のゲート電極が第１の配線５５０１に接続される。

【０１５２】

なお、第１の薄膜トランジスタ５５７１のゲート電極、第４の薄膜トランジスタ５５７４のゲート電極、第５の薄膜トランジスタ５５７５の第２の電極、第６の薄膜トランジスタ５５７６の第２の電極及び第７の薄膜トランジスタ５５７７の第２の電極の接続箇所をノード５５４３とする。さらに、第２の薄膜トランジスタ５５７２のゲート電極、第３の薄膜トランジスタ５５７３の第２の電極、第４の薄膜トランジスタ５５７４の第２の電極、第６の薄膜トランジスタ５５７６のゲート電極及び第８の薄膜トランジスタ５５７８の第２の電極の接続箇所をノード５５４４とする。

【０１５３】

なお、第１の配線５５０１、第２の配線５５０２、第３の配線５５０３及び第４の配線５５０４を、それぞれ第１の信号線、第２の信号、第３の信号線、第４の信号線と呼んでもよい。さらに、第５の配線５５０５を第１の電源線、第６の配線５５０６を第２の電源線と呼んでもよい。

【０１５４】

また、信号線駆動回路及び走査線駆動回路を実施の形態１又は実施の形態２に示すｎチャネル型ＴＦＴのみで作製することも可能である。酸化物半導体層を用いるトランジスタの移動度は大きいため、駆動回路の駆動周波数を高くすることが可能となる。また、実施の形態１又は実施の形態２に示すｎチャネル型ＴＦＴはソース領域又はドレイン領域により

寄生容量が低減されるため、周波数特性（ｆ特性と呼ばれる）が高い。例えば、実施の形態１又は実施の形態２に示すｎチャネル型ＴＦＴを用いた走査線駆動回路は、高速に動作させることが出来るため、フレーム周波数を高くすること、または、黒画面挿入を実現することなども実現することが出来る。

【０１５５】

さらに、走査線駆動回路のトランジスタのチャネル幅を大きくすることや、複数の走査線駆動回路を配置することなどによって、さらに高いフレーム周波数を実現することが出来る。複数の走査線駆動回路を配置する場合は、偶数行の走査線を駆動する為の走査線駆動回路を片側に配置し、奇数行の走査線を駆動するための走査線駆動回路をその反対側に配置することにより、フレーム周波数を高くすることを実現することが出来る。

【０１５６】

また、半導体装置の一例であるアクティブマトリクス型発光表示装置を作製する場合、少なくとも一つの画素に複数の薄膜トランジスタを配置するため、走査線駆動回路を複数配置することが好ましい。アクティブマトリクス型発光表示装置のブロック図の一例を図１２（Ｂ）に示す。

【０１５７】

図１２（Ｂ）に示す発光表示装置は、基板５４００上に表示素子を備えた画素を複数有する画素部５４０１と、各画素を選択する第１の走査線駆動回路５４０２及び第２の走査線駆動回路５４０４と、選択された画素へのビデオ信号の入力を制御する信号線駆動回路５４０３とを有する。

【０１５８】

図１２（Ｂ）に示す発光表示装置の画素に入力されるビデオ信号をデジタル形式とする場合、画素はトランジスタのオンとオフの切り替えによって、発光もしくは非発光の状態となる。よって、面積階調法または時間階調法を用いて階調の表示を行うことができる。面積階調法は、１画素を複数の副画素に分割し、各副画素を独立にビデオ信号に基づいて駆動させることによって、階調表示を行う駆動法である。また時間階調法は、画素が発光する期間を制御することによって、階調表示を行う駆動法である。

【０１５９】

発光素子は、液晶素子などに比べて応答速度が高いので、液晶素子よりも時間階調法に適している。具体的に時間階調法で表示を行なう場合、１フレーム期間を複数のサブフレーム期間に分割する。そしてビデオ信号に従い、各サブフレーム期間において画素の発光素子を発光または非発光の状態にする。複数のサブフレーム期間に分割することによって、１フレーム期間中に画素が実際に発光する期間のトータルの長さを、ビデオ信号により制御することができ、階調を表示することができる。

【０１６０】

なお、図１２（Ｂ）に示す発光表示装置では、一つの画素にスイッチング用ＴＦＴと、電流制御用ＴＦＴとの２つを配置する場合、スイッチング用ＴＦＴのゲート配線である第１の走査線に入力される信号を第１走査線駆動回路５４０２で生成し、電流制御用ＴＦＴのゲート配線である第２の走査線に入力される信号を第２の走査線駆動回路５４０４で生成している例を示しているが、第１の走査線に入力される信号と、第２の走査線に入力される信号とを、共に１つの走査線駆動回路で生成するようにしても良い。また、例えば、スイッチング素子が有する各トランジスタの数によって、スイッチング素子の動作を制御するのに用いられる第１の走査線が、各画素に複数設けられることもあり得る。この場合、複数の第１の走査線に入力される信号を、全て１つの走査線駆動回路で生成しても良いし、複数の各走査線駆動回路で生成しても良い。

【０１６１】

また、発光表示装置においても、駆動回路のうち、ｎチャネル型ＴＦＴで構成することができる駆動回路の一部を画素部の薄膜トランジスタと同一基板上に形成することができる。また、信号線駆動回路及び走査線駆動回路を実施の形態１又は実施の形態２に示すｎチャネル型ＴＦＴのみで作製することも可能である。

【０１６２】
以上の工程により、半導体装置として信頼性の高い表示装置を作製することができる。
【０１６３】
本実施の形態は、他の実施の形態に記載した構成と適宜組み合わせて実施することが可能である。
【０１６４】
（実施の形態６）
本実施の形態では、半導体装置として発光表示装置の例を示す。表示装置の有する表示素子としては、ここではエレクトロルミネッセンスを利用する発光素子を用いて示す。エレクトロルミネッセンスを利用する発光素子は、発光材料が有機化合物であるか、無機化合物であるかによって区別され、一般的に、前者は有機ＥＬ素子、後者は無機ＥＬ素子と呼ばれている。
【０１６５】
有機ＥＬ素子は、発光素子に電圧を印加することにより、一対の電極から電子および正孔がそれぞれ発光性の有機化合物を含む層に注入され、電流が流れる。そして、それらキャリア（電子および正孔）が再結合することにより、発光性の有機化合物が励起状態を形成し、その励起状態が基底状態に戻る際に発光する。このようなメカニズムから、このような発光素子は、電流励起型の発光素子と呼ばれる。
【０１６６】
無機ＥＬ素子は、その素子構成により、分散型無機ＥＬ素子と薄膜型無機ＥＬ素子とに分類される。分散型無機ＥＬ素子は、発光材料の粒子をバインダ中に分散させた発光層を有するものであり、発光メカニズムはドナー準位とアクセプター準位を利用するドナー－アクセプター再結合型発光である。薄膜型無機ＥＬ素子は、発光層を誘電体層で挟み込み、さらにそれを電極で挟んだ構造であり、発光メカニズムは金属イオンの内殻電子遷移を利用する局在型発光である。なお、ここでは、発光素子として有機ＥＬ素子を用いて説明する。
【０１６７】
図１８は、半導体装置の例としてデジタル時間階調駆動を適用可能な画素構成の一例を示す図である。
【０１６８】
デジタル時間階調駆動を適用可能な画素の構成及び画素の動作について説明する。ここでは酸化物半導体層（Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜）をチャネル形成領域に用いるｎチャネル型のトランジスタを１つの画素に２つ用いる例を示す。
【０１６９】
画素６４００は、スイッチング用トランジスタ６４０１、駆動用トランジスタ６４０２、発光素子６４０４及び容量素子６４０３を有している。スイッチング用トランジスタ６４０１はゲートが走査線６４０６に接続され、第１電極（ソース電極及びドレイン電極の一方）が信号線６４０５に接続され、第２電極（ソース電極及びドレイン電極の他方）が駆動用トランジスタ６４０２のゲートに接続されている。駆動用トランジスタ６４０２は、ゲートが容量素子６４０３を介して電源線６４０７に接続され、第１電極が電源線６４０７に接続され、第２電極が発光素子６４０４の第１電極（画素電極）に接続されている。発光素子６４０４の第２電極は共通電極６４０８に相当する。
【０１７０】
なお、発光素子６４０４の第２電極（共通電極６４０８）には低電源電位が設定されている。なお、低電源電位とは、電源線６４０７に設定される高電源電位を基準にして低電源電位＜高電源電位を満たす電位であり、低電源電位としては例えばＧＮＤ、０Ｖなどが設定されていても良い。この高電源電位と低電源電位との電位差を発光素子６４０４に印加して、発光素子６４０４に電流を流して発光素子６４０４を発光させるため、高電源電位と低電源電位との電位差が発光素子６４０４の順方向しきい値電圧以上となるようにそれぞれの電位を設定する。

【０１７１】
なお、容量素子６４０３は駆動用トランジスタ６４０２のゲート容量を代用して省略することも可能である。駆動用トランジスタ６４０２のゲート容量については、チャネル領域とゲート電極との間で容量が形成されていてもよい。
【０１７２】
ここで、電圧入力電圧駆動方式の場合には、駆動用トランジスタ６４０２のゲートには、駆動用トランジスタ６４０２が十分にオンするか、オフするかの二つの状態となるようなビデオ信号を入力する。つまり、駆動用トランジスタ６４０２は線形領域で動作させる。駆動用トランジスタ６４０２は線形領域で動作させるため、電源線６４０７の電圧よりも高い電圧を駆動用トランジスタ６４０２のゲートにかける。なお、信号線６４０５には、（電源線電圧＋駆動用トランジスタ６４０２のＶｔｈ）以上の電圧をかける。
【０１７３】
また、デジタル時間階調駆動に代えて、アナログ階調駆動を行う場合、信号の入力を異ならせることで、図１８と同じ画素構成を用いることができる。
【０１７４】
アナログ階調駆動を行う場合、駆動用トランジスタ６４０２のゲートに発光素子６４０４の順方向電圧＋駆動用トランジスタ６４０２のＶｔｈ以上の電圧をかける。発光素子６４０４の順方向電圧とは、所望の輝度とする場合の電圧を指しており、少なくとも順方向しきい値電圧を含む。なお、駆動用トランジスタ６４０２が飽和領域で動作するようなビデオ信号を入力することで、発光素子６４０４に電流を流すことができる。駆動用トランジスタ６４０２を飽和領域で動作させるため、電源線６４０７の電位は、駆動用トランジスタ６４０２のゲート電位よりも高くする。ビデオ信号をアナログとすることで、発光素子６４０４にビデオ信号に応じた電流を流し、アナログ階調駆動を行うことができる。
【０１７５】
なお、図１８に示す画素構成は、これに限定されない。例えば、図１８に示す画素に新たにスイッチ、抵抗素子、容量素子、トランジスタ又は論理回路などを追加してもよい。
【０１７６】
次に、発光素子の構成について、図１９（Ａ）、図１９（Ｂ）、図１９（Ｃ）を用いて説明する。ここでは、駆動用ＴＦＴが図１（Ｂ）に示す薄膜トランジスタ１７０の場合を例に挙げて、画素の断面構造について説明する。図１９（Ａ）、図１９（Ｂ）、図１９（Ｃ）の半導体装置に用いられる駆動用ＴＦＴであるＴＦＴ７００１、７０１１、７０２１は、実施の形態１で示す薄膜トランジスタ１７０と同様に作製でき、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を半導体層として含む高い電気特性を有する薄膜トランジスタである。
【０１７７】
発光素子は発光を取り出すために少なくとも陽極又は陰極の一方が透明であればよい。そして、基板上に薄膜トランジスタ及び発光素子を形成し、基板とは逆側の面から発光を取り出す上面射出や、基板側の面から発光を取り出す下面射出や、基板側及び基板とは反対側の面から発光を取り出す両面射出構造の発光素子があり、図１８に示す画素構成はどの射出構造の発光素子にも適用することができる。
【０１７８】
上面射出構造の発光素子について図１９（Ａ）を用いて説明する。
【０１７９】
図１９（Ａ）に、駆動用ＴＦＴであるＴＦＴ７００１が図１（Ｂ）に示す薄膜トランジスタ１７０であり、発光素子７００２から発せられる光が陽極７００５側に抜ける場合の、画素の断面図を示す。図１９（Ａ）では、発光素子７００２の陰極７００３と駆動用ＴＦＴであるＴＦＴ７００１が電気的に接続されており、陰極７００３上に発光層７００４、陽極７００５が順に積層されている。陰極７００３は仕事関数が小さく、なおかつ光を反射する導電膜であれば様々の材料を用いることができる。例えば、Ｃａ、Ａｌ、ＣａＦ、ＭｇＡｇ、ＡｌＬｉ等が望ましい。そして発光層７００４は、単数の層で構成されていても、複数の層が積層されるように構成されていてもどちらでも良い。複数の層で構成され

ている場合、陰極７００３上に電子注入層、電子輸送層、発光層、ホール輸送層、ホール注入層の順に積層する。なおこれらの層を全て設ける必要はない。陽極７００５は光を透過する透光性を有する導電性材料を用いて形成し、例えば酸化タングステンを含むインジウム酸化物、酸化タングステンを含むインジウム亜鉛酸化物、酸化チタンを含むインジウム酸化物、酸化チタンを含むインジウム錫酸化物、インジウム錫酸化物（以下、ＩＴＯと示す。）、インジウム亜鉛酸化物、酸化ケイ素を添加したインジウム錫酸化物などの透光性を有する導電性導電膜を用いても良い。

【０１８０】

陰極７００３及び陽極７００５で発光層７００４を挟んでいる領域が発光素子７００２に相当する。図１９（Ａ）に示した画素の場合、発光素子７００２から発せられる光は、矢印で示すように陽極７００５側に射出する。

【０１８１】

次に、下面射出構造の発光素子について図１９（Ｂ）を用いて説明する。駆動用ＴＦＴ７０１１が図１（Ａ）に示す薄膜トランジスタ１７０であり、発光素子７０１２から発せられる光が陰極７０１３側に射出する場合の、画素の断面図を示す。図１９（Ｂ）では、駆動用ＴＦＴ７０１１と電気的に接続された透光性を有する導電膜７０１７上に、発光素子７０１２の陰極７０１３が成膜されており、陰極７０１３上に発光層７０１４、陽極７０１５が順に積層されている。なお、陽極７０１５が透光性を有する場合、陽極上を覆うように、光を反射または遮蔽するための遮蔽膜７０１６が成膜されていてもよい。陰極７０１３は、図１９（Ａ）の場合と同様に、仕事関数が小さい導電性材料であれば様々な材料を用いることができる。ただしその膜厚は、光を透過する程度（好ましくは、５ｎｍ～３０ｎｍ程度）とする。例えば２０ｎｍの膜厚を有するアルミニウム膜を、陰極７０１３として用いることができる。そして発光層７０１４は、図１９（Ａ）と同様に、単数の層で構成されていても、複数の層が積層されるように構成されていてもどちらでも良い。陽極７０１５は光を透過する必要はないが、図１９（Ａ）と同様に、透光性を有する導電性材料を用いて形成することができる。そして遮蔽膜７０１６は、例えば光を反射する金属等を用いることができるが、金属膜に限定されない。例えば黒の顔料を添加した樹脂等を用いることもできる。

【０１８２】

陰極７０１３及び陽極７０１５で、発光層７０１４を挟んでいる領域が発光素子７０１２に相当する。図１９（Ｂ）に示した画素の場合、発光素子７０１２から発せられる光は、矢印で示すように陰極７０１３側に射出する。

【０１８３】

次に、両面射出構造の発光素子について、図１９（Ｃ）を用いて説明する。図１９（Ｃ）では、駆動用ＴＦＴ７０２１と電気的に接続された透光性を有する導電膜７０２７上に、発光素子７０２２の陰極７０２３が成膜されており、陰極７０２３上に発光層７０２４、陽極７０２５が順に積層されている。陰極７０２３は、図１９（Ａ）の場合と同様に、仕事関数が小さい導電性材料であれば様々な材料を用いることができる。ただしその膜厚は、光を透過する程度とする。例えば２０ｎｍの膜厚を有するＡｌを、陰極７０２３として用いることができる。そして発光層７０２４は、図１９（Ａ）と同様に、単数の層で構成されていても、複数の層が積層されるように構成されていてもどちらでも良い。陽極７０２５は、図１９（Ａ）と同様に、光を透過する透光性を有する導電性材料を用いて形成することができる。

【０１８４】

陰極７０２３と、発光層７０２４と、陽極７０２５とが重なっている部分が発光素子７０２２に相当する。図１９（Ｃ）に示した画素の場合、発光素子７０２２から発せられる光は、矢印で示すように陽極７０２５側と陰極７０２３側の両方に射出する。

【０１８５】

なお、ここでは、発光素子として有機ＥＬ素子について述べたが、発光素子として無機ＥＬ素子を設けることも可能である。

【０１８６】
なお本実施の形態では、発光素子の駆動を制御する薄膜トランジスタ（駆動用ＴＦＴ）と発光素子が電気的に接続されている例を示したが、駆動用ＴＦＴと発光素子との間に電流制御用ＴＦＴが接続されている構成であってもよい。
【０１８７】
なお本実施の形態で示す半導体装置は、図１９（Ａ）、図１９（Ｂ）、図１９（Ｃ）に示した構成に限定されるものではなく、開示した技術的思想に基づく各種の変形が可能である。
【０１８８】
次に、半導体装置の一形態に相当する発光表示パネル（発光パネルともいう）の上面及び断面について、図２０（Ａ）、図２０（Ｂ）を用いて説明する。図２０（Ａ）は、第１の基板上に形成された薄膜トランジスタ及び発光素子を、第２の基板との間にシール材によって封止した、パネルの上面図であり、図２０（Ｂ）は、図２０（Ａ）のＨ－Ｉにおける断面図に相当する。
【０１８９】
第１の基板４５０１上に設けられた画素部４５０２、信号線駆動回路４５０３ａ、４５０３ｂ、及び走査線駆動回路４５０４ａ、４５０４ｂを囲むようにして、シール材４５０５が設けられている。また画素部４５０２、信号線駆動回路４５０３ａ、４５０３ｂ、及び走査線駆動回路４５０４ａ、４５０４ｂの上に第２の基板４５０６が設けられている。よって画素部４５０２、信号線駆動回路４５０３ａ、４５０３ｂ、及び走査線駆動回路４５０４ａ、４５０４ｂは、第１の基板４５０１とシール材４５０５と第２の基板４５０６とによって、充填材４５０７と共に密封されている。このように外気に曝されないように気密性が高く、脱ガスの少ない保護フィルム（貼り合わせフィルム、紫外線硬化樹脂フィルム等）やカバー材でパッケージング（封入）することが好ましい。
【０１９０】
また第１の基板４５０１上に設けられた画素部４５０２、信号線駆動回路４５０３ａ、４５０３ｂ、及び走査線駆動回路４５０４ａ、４５０４ｂは、薄膜トランジスタを複数有しており、図２０（Ｂ）では、画素部４５０２に含まれる薄膜トランジスタ４５１０と、信号線駆動回路４５０３ａに含まれる薄膜トランジスタ４５０９とを例示している。
【０１９１】
薄膜トランジスタ４５０９、４５１０は、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を半導体層として含む信頼性の高い実施の形態１に示す薄膜トランジスタを適用することができる。
【０１９２】
また４５１１は発光素子に相当し、発光素子４５１１が有する画素電極である第１の電極層４５１７は、薄膜トランジスタ４５１０のソース電極層またはドレイン電極層と電気的に接続されている。なお発光素子４５１１の構成は、第１の電極層４５１７、電界発光層４５１２、第２の電極層４５１３の積層構造であるが、本実施の形態に示した構成に限定されない。発光素子４５１１から取り出す光の方向などに合わせて、発光素子４５１１の構成は適宜変えることができる。
【０１９３】
隔壁４５２０は、有機樹脂膜、無機絶縁膜または有機ポリシロキサンを用いて形成する。特に感光性の材料を用い、第１の電極層４５１７上に開口部を形成し、その開口部の側壁が連続した曲率を持って形成される傾斜面となるように形成することが好ましい。
【０１９４】
電界発光層４５１２は、単数の層で構成されていても、複数の層が積層されるように構成されていてもどちらでも良い。
【０１９５】
発光素子４５１１に酸素、水素、水分、二酸化炭素等が侵入しないように、第２の電極層４５１３及び隔壁４５２０上に保護膜を形成してもよい。保護膜としては、窒化珪素膜、窒化酸化珪素膜、ＤＬＣ膜等を形成することができる。

【０１９６】
また、信号線駆動回路４５０３ａ、４５０３ｂ、走査線駆動回路４５０４ａ、４５０４ｂ、または画素部４５０２に与えられる各種信号及び電位は、ＦＰＣ４５１８ａ、４５１８ｂから供給されている。
【０１９７】
本実施の形態では、接続端子電極４５１５が、発光素子４５１１が有する第１の電極層４５１７と同じ導電膜から形成され、端子電極４５１６は、薄膜トランジスタ４５０９、４５１０が有するソース電極層及びドレイン電極層と同じ導電膜から形成されている。
【０１９８】
接続端子電極４５１５は、ＦＰＣ４５１８ａが有する端子と、異方性導電膜４５１９を介して電気的に接続されている。
【０１９９】
発光素子４５１１からの光の取り出し方向に位置する基板には、第２の基板は透光性でなければならない。その場合には、ガラス板、プラスチック板、ポリエステルフィルムまたはアクリルフィルムのような透光性を有する材料を用いる。
【０２００】
また、充填材４５０７としては窒素やアルゴンなどの不活性な気体の他に、紫外線硬化樹脂または熱硬化樹脂を用いることができ、ＰＶＣ（ポリビニルクロライド）、アクリル、ポリイミド、エポキシ樹脂、シリコン樹脂、ＰＶＢ（ポリビニルブチラル）またはＥＶＡ（エチレンビニルアセテート）を用いることができる。
【０２０１】
また、必要であれば、発光素子の射出面に偏光板、又は円偏光板（楕円偏光板を含む）、位相差板（λ／４板、λ／２板）、カラーフィルタなどの光学フィルムを適宜設けてもよい。また、偏光板又は円偏光板に反射防止膜を設けてもよい。例えば、表面の凹凸により反射光を拡散し、映り込みを低減できるアンチグレア処理を施すことができる。
【０２０２】
信号線駆動回路４５０３ａ、４５０３ｂ、及び走査線駆動回路４５０４ａ、４５０４ｂは、別途用意された単結晶半導体基板、或いは絶縁基板上に単結晶半導体膜又は多結晶半導体膜によって形成された駆動回路で実装されていてもよい。また、信号線駆動回路のみ、或いは一部、又は走査線駆動回路のみ、或いは一部のみを別途形成して実装しても良く、本実施の形態は図２０（Ａ）及び図２０（Ｂ）の構成に限定されない。
【０２０３】
以上の工程により、製造コストを低減した発光表示装置（表示パネル）を作製することができる。
【０２０４】
本実施の形態は、実施の形態１、実施の形態２、または実施の形態３に記載した構成と適宜組み合わせて実施することが可能である。
【０２０５】
（実施の形態７）
本実施の形態では、半導体装置の一形態に相当する液晶表示パネルの上面及び断面について、図２１（Ａ１）、図２１（Ａ２）、図２１（Ｂ）を用いて説明する。図２１（Ａ１）、図２１（Ａ２）は、第１の基板４００１上に形成された実施の形態１で示したＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を半導体層として含む薄膜トランジスタ４０１０、４０１１、及び液晶素子４０１３を、第２の基板４００６との間にシール材４００５によって封止した、パネルの上面図であり、図２１（Ｂ）は、図２１（Ａ１）、図２１（Ａ２）のＭ－Ｎにおける断面図に相当する。
【０２０６】
第１の基板４００１上に設けられた画素部４００２と、走査線駆動回路４００４とを囲むようにして、シール材４００５が設けられている。また画素部４００２と、走査線駆動回路４００４の上に第２の基板４００６が設けられている。よって画素部４００２と、走査

線駆動回路４００４とは、第１の基板４００１とシール材４００５と第２の基板４００６とによって、液晶層４００８と共に封止されている。また第１の基板４００１上のシール材４００５によって囲まれている領域とは異なる領域に、別途用意された基板上に単結晶半導体膜又は多結晶半導体膜で形成された信号線駆動回路４００３が実装されている。

【０２０７】

なお、別途形成した駆動回路の接続方法は、特に限定されるものではなく、ＣＯＧ方法、ワイヤボンディング方法、或いはＴＡＢ方法などを用いることができる。図２１（Ａ１）は、ＣＯＧ方法により信号線駆動回路４００３を実装する例であり、図２１（Ａ２）は、ＴＡＢ方法により信号線駆動回路４００３を実装する例である。

【０２０８】

また第１の基板４００１上に設けられた画素部４００２と、走査線駆動回路４００４は、薄膜トランジスタを複数有しており、図２１（Ｂ）では、画素部４００２に含まれる薄膜トランジスタ４０１０と、走査線駆動回路４００４に含まれる薄膜トランジスタ４０１１とを例示している。薄膜トランジスタ４０１０、４０１１上には絶縁層４０２０、４０２１が設けられている。

【０２０９】

薄膜トランジスタ４０１０、４０１１は、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を半導体層として含む実施の形態１に示す薄膜トランジスタを適用することができる。薄膜トランジスタ４０１１は、実施の形態１の図１に示した薄膜トランジスタ１７０に相当する。

【０２１０】

また、液晶素子４０１３が有する画素電極層４０３０は、薄膜トランジスタ４０１０と電気的に接続されている。そして液晶素子４０１３の対向電極層４０３１は第２の基板４００６上に形成されている。画素電極層４０３０と対向電極層４０３１と液晶層４００８とが重なっている部分が、液晶素子４０１３に相当する。なお、画素電極層４０３０、対向電極層４０３１はそれぞれ配向膜として機能する絶縁層４０３２、４０３３が設けられ、絶縁層４０３２、４０３３を介して液晶層４００８を挟持している。

【０２１１】

なお、第１の基板４００１、第２の基板４００６としては、ガラス、金属（代表的にはステンレス）、セラミックス、プラスチックを用いることができる。プラスチックとしては、ＦＲＰ（Ｆｉｂｅｒｇｌａｓｓ－Ｒｅｉｎｆｏｒｃｅｄ　Ｐｌａｓｔｉｃｓ）板、ＰＶＦ（ポリビニルフルオライド）フィルム、ポリエステルフィルムまたはアクリル樹脂フィルムを用いることができる。また、アルミニウムホイルをＰＶＦフィルムやポリエステルフィルムで挟んだ構造のシートを用いることもできる。

【０２１２】

また４０３５は絶縁膜を選択的にエッチングすることで得られる柱状のスペーサであり、画素電極層４０３０と対向電極層４０３１との間の距離（セルギャップ）を制御するために設けられている。なお球状のスペーサを用いていても良い。また、対向電極層４０３１は、薄膜トランジスタ４０１０と同一基板上に設けられる共通電位線と電気的に接続される。共通接続部を用いて、一対の基板間に配置される導電性粒子を介して対向電極層４０３１と共通電位線とを電気的に接続することができる。なお、導電性粒子はシール材４００５に含有させる。

【０２１３】

また、配向膜を用いないブルー相を示す液晶を用いてもよい。ブルー相は液晶相の一つであり、コレステリック液晶を昇温していくと、コレステリック相から等方相へ転移する直前に発現する相である。ブルー相は狭い温度範囲でしか発現しないため、温度範囲を改善するために５重量％以上のカイラル剤を混合させた液晶組成物を用いて液晶層４００８に用いる。ブルー相を示す液晶とカイラル剤とを含む液晶組成物は、応答速度が１０μｓ～１００μｓと短く、光学的等方性であるため配向処理が不要であり、視野角依存性が小さい。

【０２１４】

なお本実施の形態は透過型液晶表示装置の例であるが、反射型液晶表示装置でも半透過型液晶表示装置でも適用できる。

【０２１５】

また、本実施の形態の液晶表示装置では、基板の外側（視認側）に偏光板を設け、内側に着色層、表示素子に用いる電極層という順に設ける例を示すが、偏光板は基板の内側に設けてもよい。また、偏光板と着色層の積層構造も本実施の形態に限定されず、偏光板及び着色層の材料や作製工程条件によって適宜設定すればよい。また、ブラックマトリクスとして機能する遮光膜を設けてもよい。

【０２１６】

また、本実施の形態では、薄膜トランジスタの表面凹凸を低減するため、及び薄膜トランジスタの信頼性を向上させるため、実施の形態１で得られた薄膜トランジスタを保護膜や平坦化絶縁膜として機能する絶縁層（絶縁層４０２０、絶縁層４０２１）で覆う構成となっている。なお、保護膜は、大気中に浮遊する有機物や金属物、水蒸気などの汚染不純物の侵入を防ぐためのものであり、緻密な膜が好ましい。保護膜は、スパッタ法を用いて、酸化珪素膜、窒化珪素膜、酸化窒化珪素膜、窒化酸化珪素膜、酸化アルミニウム膜、窒化アルミニウム膜、酸化窒化アルミニウム膜、又は窒化酸化アルミニウム膜の単層、又は積層で形成すればよい。本実施の形態では保護膜をスパッタ法で形成する例を示すが、特に限定されずＰＣＶＤ法などの種々の方法で形成すればよい。

【０２１７】

ここでは、保護膜として積層構造の絶縁層４０２０を形成する。ここでは、絶縁層４０２０の一層目として、スパッタ法を用いて酸化珪素膜を形成する。保護膜として酸化珪素膜を用いると、ソース電極層及びドレイン電極層として用いるアルミニウム膜のヒロック防止に効果がある。

【０２１８】

また、保護膜の二層目として絶縁層を形成する。ここでは、ここでは、絶縁層４０２０の二層目として、スパッタ法を用いて窒化珪素膜を形成する。保護膜として窒化珪素膜を用いると、ナトリウム等のイオンが半導体領域中に侵入して、ＴＦＴの電気特性を変化させることを抑制することができる。

【０２１９】

また、保護膜を形成した後に、半導体層のアニール（３００℃～４００℃）を行ってもよい。

【０２２０】

また、平坦化絶縁膜として絶縁層４０２１を形成する。絶縁層４０２１としては、ポリイミド、アクリル、ポリイミド、ベンゾシクロブテン、ポリアミド、エポキシ等の、耐熱性を有する有機材料を用いることができる。また上記有機材料の他に、低誘電率材料（ｌｏｗ－ｋ材料）、シロキサン系樹脂、ＰＳＧ（リンガラス）、ＢＰＳＧ（リンボロンガラス）等を用いることができる。なお、これらの材料で形成される絶縁膜を複数積層させることで、絶縁層４０２１を形成してもよい。

【０２２１】

なおシロキサン系樹脂とは、シロキサン系材料を出発材料として形成されたＳｉ－Ｏ－Ｓｉ結合を含む樹脂に相当する。シロキサン系樹脂は置換基としては有機基（例えばアルキル基やアリール基）やフルオロ基を用いても良い。また、有機基はフルオロ基を有していても良い。

【０２２２】

絶縁層４０２１の形成法は、特に限定されず、その材料に応じて、スパッタ法、ＳＯＧ法、スピンコート、ディップ、スプレー塗布、液滴吐出法（インクジェット法、スクリーン印刷、オフセット印刷等）、ドクターナイフ、ロールコーター、カーテンコーター、ナイフコーター等を用いることができる。絶縁層４０２１を材料液を用いて形成する場合、ベークする工程で同時に、半導体層のアニール（３００℃～４００℃）を行ってもよい。絶縁層４０２１の焼成工程と半導体層のアニールを兼ねることで効率よく半導体装置を作製

することが可能となる。
【０２２３】
画素電極層４０３０、対向電極層４０３１は、酸化タングステンを含むインジウム酸化物、酸化タングステンを含むインジウム亜鉛酸化物、酸化チタンを含むインジウム酸化物、酸化チタンを含むインジウム錫酸化物、インジウム錫酸化物（以下、ＩＴＯと示す。）、インジウム亜鉛酸化物、酸化ケイ素を添加したインジウム錫酸化物などの透光性を有する導電性材料を用いることができる。
【０２２４】
また、画素電極層４０３０、対向電極層４０３１として、導電性高分子（導電性ポリマーともいう）を含む導電性組成物を用いて形成することができる。導電性組成物を用いて形成した画素電極は、シート抵抗が１００００Ω／□以下、波長５５０ｎｍにおける透光率が７０％以上であることが好ましい。また、導電性組成物に含まれる導電性高分子の抵抗率が０．１Ω・ｃｍ以下であることが好ましい。
【０２２５】
導電性高分子としては、いわゆるπ電子共役系導電性高分子が用いることができる。例えば、ポリアニリンまたはその誘導体、ポリピロールまたはその誘導体、ポリチオフェンまたはその誘導体、若しくはこれらの２種以上の共重合体などがあげられる。
【０２２６】
また別途形成された信号線駆動回路４００３と、走査線駆動回路４００４または画素部４００２に与えられる各種信号及び電位は、ＦＰＣ４０１８から供給されている。
【０２２７】
本実施の形態では、接続端子電極４０１５が、液晶素子４０１３が有する画素電極層４０３０と同じ導電膜から形成され、端子電極４０１６は、薄膜トランジスタ４０１０、４０１１のソース電極層及びドレイン電極層と同じ導電膜で形成されている。
【０２２８】
接続端子電極４０１５は、ＦＰＣ４０１８が有する端子と、異方性導電膜４０１９を介して電気的に接続されている。
【０２２９】
また図２１（Ａ１）、図２１（Ａ２）においては、信号線駆動回路４００３を別途形成し、第１の基板４００１に実装している例を示しているが、本実施の形態はこの構成に限定されない。走査線駆動回路を別途形成して実装しても良いし、信号線駆動回路の一部または走査線駆動回路の一部のみを別途形成して実装しても良い。
【０２３０】
図２２は、ＴＦＴ基板２６００を用いて半導体装置として液晶表示モジュールを構成する一例を示している。
【０２３１】
図２２は液晶表示モジュールの一例であり、ＴＦＴ基板２６００と対向基板２６０１がシール材２６０２により固着され、その間にＴＦＴ等を含む画素部２６０３、液晶層を含む表示素子２６０４、着色層２６０５、偏光板２６０６が設けられ表示領域を形成している。着色層２６０５はカラー表示を行う場合に必要であり、ＲＧＢ方式の場合は、赤、緑、青の各色に対応した着色層が各画素に対応して設けられている。ＴＦＴ基板２６００と対向基板２６０１の外側には偏光板２６０６、偏光板２６０７、拡散板２６１３が配設されている。光源は冷陰極管２６１０と反射板２６１１により構成され、回路基板２６１２は、フレキシブル配線基板２６０９によりＴＦＴ基板２６００の配線回路部２６０８と接続され、コントロール回路や電源回路などの外部回路が組みこまれている。また偏光板と、液晶層との間に位相差板を有した状態で積層してもよい。
【０２３２】
液晶表示モジュールには、ＴＮ（Ｔｗｉｓｔｅｄ　Ｎｅｍａｔｉｃ）モード、ＩＰＳ（Ｉｎ－Ｐｌａｎｅ－Ｓｗｉｔｃｈｉｎｇ）モード、ＦＦＳ（Ｆｒｉｎｇｅ　Ｆｉｅｌｄ　Ｓｗｉｔｃｈｉｎｇ）モード、ＭＶＡ（Ｍｕｌｔｉ－ｄｏｍａｉｎ　Ｖｅｒｔｉｃａｌ　Ａ

ｌｉｇｎｍｅｎｔ）モード、ＰＶＡ（Ｐａｔｔｅｒｎｅｄ　Ｖｅｒｔｉｃａｌ　Ａｌｉｇｎｍｅｎｔ）、ＡＳＭ（Ａｘｉａｌｌｙ　Ｓｙｍｍｅｔｒｉｃ　ａｌｉｇｎｅｄ　Ｍｉｃｒｏ－ｃｅｌｌ）モード、ＯＣＢ（Ｏｐｔｉｃａｌ　Ｃｏｍｐｅｎｓａｔｅｄ　Ｂｉｒｅｆｒｉｎｇｅｎｃｅ）モード、ＦＬＣ（Ｆｅｒｒｏｅｌｅｃｔｒｉｃ　Ｌｉｑｕｉｄ　Ｃｒｙｓｔａｌ）モード、ＡＦＬＣ（ＡｎｔｉＦｅｒｒｏｅｌｅｃｔｒｉｃ　Ｌｉｑｕｉｄ　Ｃｒｙｓｔａｌ）などを用いることができる。

【０２３３】

以上の工程により、半導体装置として製造コストを低減した液晶表示パネルを作製することができる。

【０２３４】

本実施の形態は、実施の形態１、実施の形態２、または実施の形態３に記載した構成と適宜組み合わせて実施することが可能である。

【０２３５】

（実施の形態８）

電子ペーパーは、情報を表示するものであればあらゆる分野の電子機器に用いることが可能である。例えば、電子ペーパーを用いて、電子書籍（電子ブック）、ポスター、電車などの乗り物の車内広告、クレジットカード等の各種カードにおける表示等に適用することができる。電子機器の一例を図２３、図２４に示す。

【０２３６】

図２３（Ａ）は、電子ペーパーで作られたポスター２６３１を示している。広告媒体が紙の印刷物である場合には、広告の交換は人手によって行われるが、本実施の形態３を適用した電子ペーパーを用いれば短時間で広告の表示を変えることができる。また、表示も崩れることなく安定した画像が得られる。なお、ポスターは無線で情報を送受信できる構成としてもよい。

【０２３７】

また、図２３（Ｂ）は、電車などの乗り物の車内広告２６３２を示している。広告媒体が紙の印刷物である場合には、広告の交換は人手によって行われるが、本実施の形態３を適用した電子ペーパーを用いれば人手を多くかけることなく短時間で広告の表示を変えることができる。また表示も崩れることなく安定した画像が得られる。なお、ポスターは無線で情報を送受信できる構成としてもよい。

【０２３８】

また、図２４は、電子書籍２７００の一例を示している。例えば、電子書籍２７００は、筐体２７０１および筐体２７０３の２つの筐体で構成されている。筐体２７０１および筐体２７０３は、軸部２７１１により一体とされており、該軸部２７１１を軸として開閉動作を行うことができる。このような構成により、紙の書籍のような動作を行うことが可能となる。

【０２３９】

筐体２７０１には表示部２７０５が組み込まれ、筐体２７０３には表示部２７０７が組み込まれている。表示部２７０５および表示部２７０７は、続き画面を表示する構成としてもよいし、異なる画面を表示する構成としてもよい。異なる画面を表示する構成とすることで、例えば右側の表示部（図２４では表示部２７０５）に文章を表示し、左側の表示部（図２４では表示部２７０７）に画像を表示することができる。

【０２４０】

また、図２４では、筐体２７０１に操作部などを備えた例を示している。例えば、筐体２７０１において、電源２７２１、操作キー２７２３、スピーカ２７２５などを備えている。操作キー２７２３により、頁を送ることができる。なお、筐体の表示部と同一面にキーボードやポインティングディバイスなどを備える構成としてもよい。また、筐体の裏面や側面に、外部接続用端子（イヤホン端子、ＵＳＢ端子、またはＡＣアダプタおよびＵＳＢケーブルなどの各種ケーブルと接続可能な端子など）、記録媒体挿入部などを備える構成としてもよい。さらに、電子書籍２７００は、電子辞書としての機能を持たせた構成とし

てもよい。
【０２４１】
また、電子書籍２７００は、無線で情報を送受信できる構成としてもよい。無線により、電子書籍サーバから、所望の書籍データなどを購入し、ダウンロードする構成とすることも可能である。
【０２４２】
（実施の形態９）
半導体装置は、さまざまな電子機器（遊技機も含む）に適用することができる。電子機器としては、例えば、テレビジョン装置（テレビ、またはテレビジョン受信機ともいう）、コンピュータ用などのモニタ、デジタルカメラ、デジタルビデオカメラ、デジタルフォトフレーム、携帯電話機（携帯電話、携帯電話装置ともいう）、携帯型ゲーム機、携帯情報端末、音響再生装置、パチンコ機などの大型ゲーム機などが挙げられる。
【０２４３】
図２５（Ａ）は、テレビジョン装置９６００の一例を示している。テレビジョン装置９６００は、筐体９６０１に表示部９６０３が組み込まれている。表示部９７０３により、映像を表示することが可能である。また、ここでは、スタンド９６０５により筐体９６０１を支持した構成を示している。
【０２４４】
テレビジョン装置９６００の操作は、筐体９６０１が備える操作スイッチや、別体のリモコン操作機９６１０により行うことができる。リモコン操作機９６１０が備える操作キー９６０９により、チャンネルや音量の操作を行うことができ、表示部９６０３に表示される映像を操作することができる。また、リモコン操作機９６１０に、当該リモコン操作機９６１０から出力する情報を表示する表示部９６０７を設ける構成としてもよい。
【０２４５】
なお、テレビジョン装置９６００は、受信機やモデムなどを備えた構成とする。受信機により一般のテレビ放送の受信を行うことができ、さらにモデムを介して優先または無線による通信ネットワークに接続することにより、一方向（送信者から受信者）または双方向（送信者と受信者間、あるいは受信者間同士など）の情報通信を行うことも可能である。
【０２４６】
図２５（Ｂ）は、デジタルフォトフレーム９７００の一例を示している。例えば、デジタルフォトフレーム９７００は、筐体９７０１に表示部９７０３が組み込まれている。表示部９７０３は、各種画像を表示することが可能であり、例えばデジタルカメラなどで撮影した画像データを表示させることで、通常の写真立てと同様に機能させることができる。
【０２４７】
なお、デジタルフォトフレーム９７００は、操作部、外部接続用端子（ＵＳＢ端子、ＵＳＢケーブルなどの各種ケーブルと接続可能な端子など）、記録媒体挿入部などを備える構成とする。これらの構成は、表示部と同一面に組み込まれていてもよいが、側面や裏面に備えるとデザイン性が向上するため好ましい。例えば、デジタルフォトフレームの記録媒体挿入部に、デジタルカメラで撮影した画像データを記憶したメモリを挿入して画像データを取り込み、取り込んだ画像データを表示部９７０３に表示させることができる。
【０２４８】
また、デジタルフォトフレーム９７００は、無線で情報を送受信出来る構成としてもよい。無線により、所望の画像データを取り込み、表示させる構成とすることもできる。
【０２４９】
図２６（Ａ）は携帯型遊技機であり、筐体９８８１と筐体９８９１の２つの筐体で構成されており、連結部９８９３により、開閉可能に連結されている。筐体９８８１には表示部９８８２が組み込まれ、筐体９８９１には表示部９８８３が組み込まれている。また、図２６（Ａ）に示す携帯型遊技機は、その他、スピーカ部９８８４、記録媒体挿入部９８８６、ＬＥＤランプ９８９０、入力手段（操作キー９８８５、接続端子９８８７、センサ９８８８（力、変位、位置、速度、加速度、角速度、回転数、距離、光、液、磁気、温度、

化学物質、音声、時間、硬度、電場、電流、電圧、電力、放射線、流量、湿度、傾度、振動、におい又は赤外線を測定する機能を含むもの）、マイクロフォン９８８９）等を備えている。もちろん、携帯型遊技機の構成は上述のものに限定されず、少なくとも実施の形態１または実施の形態２に示す薄膜トランジスタを有する半導体装置を備えた構成であればよく、その他付属設備が適宜設けられた構成とすることができる。図２６（Ａ）に示す携帯型遊技機は、記録媒体に記録されているプログラム又はデータを読み出して表示部に表示する機能や、他の携帯型遊技機と無線通信を行って情報を共有する機能を有する。なお、図２６（Ａ）に示す携帯型遊技機が有する機能はこれに限定されず、様々な機能を有することができる。

【０２５０】
図２６（Ｂ）は大型遊技機であるスロットマシン９９００の一例を示している。スロットマシン９９００は、筐体９９０１に表示部９９０３が組み込まれている。また、スロットマシン９９００は、その他、スタートレバーやストップスイッチなどの操作手段、コイン投入口、スピーカなどを備えている。もちろん、スロットマシン９９００の構成は上述のものに限定されず、少なくとも実施の形態１または実施の形態２に示す薄膜トランジスタを有する半導体装置を備えた構成であればよく、その他付属設備が適宜設けられた構成とすることができる。

【０２５１】
図２７は、携帯電話機１０００の一例を示している。携帯電話機１０００は、筐体１００１に組み込まれた表示部１００２の他、操作ボタン１００３、外部接続ポート１００４、スピーカ１００５、マイク１００６などを備えている。

【０２５２】
図２７に示す携帯電話機１０００は、表示部１００２を指などで触れることで、情報を入力ことができる。また、電話を掛ける、或いはメールを打つなどの操作は、表示部１００２を指などで触れることにより行うことができる。

【０２５３】
表示部１００２の画面は主として３つのモードがある。第１は、画像の表示を主とする表示モードであり、第２は、文字等の情報の入力を主とする入力モードである。第３は表示モードと入力モードの２つのモードが混合した表示＋入力モードである。

【０２５４】
例えば、電話を掛ける、或いはメールを作成する場合は、表示部１００２を文字の入力を主とする文字入力モードとし、画面に表示させた文字の入力操作を行えばよい。この場合、表示部１００２の画面のほとんどにキーボードまたは番号ボタンを表示させることが好ましい。

【０２５５】
また、携帯電話機１０００内部に、ジャイロ、加速度センサ等の傾きを検出するセンサを有する検出装置を設けることで、携帯電話機１０００の向き（縦か横か）を判断して、表示部１００２の画面表示を自動的に切り替えるようにすることができる。

【０２５６】
また、画面モードの切り替えは、表示部１００２を触れること、又は筐体１００１の操作ボタン１００３の操作により行われる。また、表示部１００２に表示される画像の種類によって切り替えるようにすることもできる。例えば、表示部に表示する画像信号が動画のデータであれば表示モード、テキストデータであれば入力モードに切り替える。

【０２５７】
また、入力モードにおいて、表示部１００２の光センサで検出される信号を検知し、表示部１００２のタッチ操作による入力が一定期間ない場合には、画面のモードを入力モードから表示モードに切り替えるように制御してもよい。

【０２５８】
表示部１００２は、イメージセンサとして機能させることもできる。例えば、表示部１００２に掌や指を触れることで、掌紋、指紋等を撮像することで、本人認証を行うことがで

きる。また、表示部に近赤外光を発光するバックライトまたは近赤外光を発光するセンシング用光源を用いれば、指静脈、掌静脈などを撮像することもできる。
【０２５９】
（実施の形態１０）
実施の形態１または実施の形態２においては、バッファ層を設ける例を示したが、本実施の形態ではバッファ層を設けない例を示す。また、２つのｎチャネル型の薄膜トランジスタを用いてインバータ回路を構成する例を以下に説明する。
【０２６０】
画素部を駆動するための駆動回路は、インバータ回路、容量、抵抗などを用いて構成する。２つのｎチャネル型ＴＦＴを組み合わせてインバータ回路を形成する場合、エンハンスメント型トランジスタとデプレッション型トランジスタとを組み合わせて形成する場合（以下、ＥＤＭＯＳ回路という）と、エンハンスメント型ＴＦＴ同士で形成する場合（以下、ＥＥＭＯＳ回路という）がある。なお、ｎチャネル型ＴＦＴのしきい値電圧が正の場合は、エンハンスメント型トランジスタと定義し、ｎチャネル型ＴＦＴのしきい値電圧が負の場合は、デプレッション型トランジスタと定義し、本明細書を通してこの定義に従うものとする。
【０２６１】
画素部と駆動回路は、同一基板上に形成し、画素部においては、マトリクス状に配置したエンハンスメント型トランジスタを用いて画素電極への電圧印加のオンオフを切り替える。この画素部に配置するエンハンスメント型トランジスタは、酸化物半導体を用いており、その電気特性は、ゲート電圧±２０Ｖにおいて、オンオフ比が$１０^{９}$以上であるため、リーク電流が少なく、低消費電力駆動を実現することができる。
【０２６２】
駆動回路のインバータ回路の断面構造を図３２（Ａ）に示す。図３２（Ａ）において、基板１４００上に第１のゲート電極１４０１及び第２のゲート電極１４０２を設ける。第１のゲート電極１４０１及び第２のゲート電極１４０２の材料は、モリブデン、チタン、クロム、タンタル、タングステン、アルミニウム、銅、ネオジム、スカンジウム等の金属材料又はこれらを主成分とする合金材料を用いて、単層で又は積層して形成することができる。
【０２６３】
例えば、第１のゲート電極１４０１及び第２のゲート電極１４０２の２層の積層構造としては、アルミニウム層上にモリブデン層が積層された二層の積層構造、または銅層上にモリブデン層を積層した二層構造、または銅層上に窒化チタン層若しくは窒化タンタルを積層した二層構造、窒化チタン層とモリブデン層とを積層した二層構造とすることが好ましい。２層の積層構造としては、タングステン層または窒化タングステンと、アルミニウムとシリコンの合金またはアルミニウムとチタンの合金と、窒化チタンまたはチタン層とを積層した積層とすることが好ましい。
【０２６４】
また、第１のゲート電極１４０１及び第２のゲート電極１４０２を覆うゲート絶縁層１４０３上には、第１配線１４０９、第２配線１４１０、及び第３配線１４１１を設け、第２の配線１４１０は、ゲート絶縁層１４０３に形成されたコンタクトホール１４０４を介して第２のゲート電極１４０２と直接接続する。
【０２６５】
また、第１のゲート電極１４０１と重なる位置に第１配線１４０９及び第２配線１４１０上に接する第１の酸化物半導体層１４０５と、第２のゲート電極１４０２と重なる位置に第２配線１４１０及び第３配線１４１１上に接する第２の酸化物半導体層１４０７とを設ける。
【０２６６】
第１の薄膜トランジスタ１４３０は、第１のゲート電極１４０１と、ゲート絶縁層１４０３を介して第１のゲート電極１４０１と重なる第１の酸化物半導体層１４０５とを有し、

第１配線１４０９は、接地電位の電源線（接地電源線）である。この接地電位の電源線は、負の電圧ＶＤＬが印加される電源線（負電源線）としてもよい。
【０２６７】
また、第２の薄膜トランジスタ１４３１は、第２のゲート電極１４０２と、ゲート絶縁層１４０３を介して第２のゲート電極１４０２と重なる第２の酸化物半導体層１４０７とを有し、第３配線１４１１は、正の電圧ＶＤＤが印加される電源線（正電源線）である。
【０２６８】
第１の酸化物半導体層１４０５を挟んで対向する第１配線１４０９の側面と第２配線１４１０の側面とをテーパ形状とすることで、酸化物半導体層におけるソース電極層の側面及びドレイン電極層の側面と重なる領域は、電界集中緩和領域として機能させる。
【０２６９】
また、第２の酸化物半導体層１４０７を挟んで対向する第２配線１４１０の側面と第３配線１４１１の側面とをテーパ形状とすることで、酸化物半導体層におけるソース電極層の側面及びドレイン電極層の側面と重なる領域は、電界集中緩和領域として機能させる。
【０２７０】
図３２（Ａ）に示すように、第１の酸化物半導体層１４０５と第２の酸化物半導体層１４０７の両方に電気的に接続する第２の配線１４１０は、ゲート絶縁層１４０３に形成されたコンタクトホール１４０４を介して第２の薄膜トランジスタ１４３１の第２のゲート電極１４０２と直接接続する。第２の配線１４１０と第２のゲート電極１４０２とを直接接続させることにより、良好なコンタクトを得ることができ、接触抵抗を低減することができる。第２のゲート電極１４０２と第２配線１４１０を他の導電膜、例えば透明導電膜を介して接続する場合に比べて、コンタクトホールの数の低減、コンタクトホールの数の低減による占有面積の縮小を図ることができる。
【０２７１】
また、駆動回路のインバータ回路の上面図を図３２（Ｃ）に示す。図３２（Ｃ）において、鎖線Ｚ１－Ｚ２で切断した断面が図３２（Ａ）に相当する。
【０２７２】
また、ＥＤＭＯＳ回路の等価回路を図３２（Ｂ）に示す。図３２（Ａ）及び図３２（Ｃ）示す回路接続は、図３２（Ｂ）に相当し、第１の薄膜トランジスタ１４３０をエンハンスメント型のｎチャネル型トランジスタとし、第２の薄膜トランジスタ１４３１をデプレッション型のｎチャネル型トランジスタとする例である。
【０２７３】
また、本実施の形態ではＥＤＭＯＳ回路の例を示したが、どちらもエンハンスメント型のｎチャネル型トランジスタとするＥＥＭＯＳ回路を用いて駆動回路を構成してもよい。
【０２７４】
また、本実施の形態においては、バッファ層を設けない例を示したが、特に限定されず、実施の形態１と同様に、第１配線１４０９の上面、第２配線１４１０上面、及び第３配線１４１１上面にバッファ層を設けてもよい。
【０２７５】
また、本実施の形態は、実施の形態１乃至９のいずれか一と組み合わせることができる。
【０２７６】
以上の構成でなる実施の形態について、以下に示す実施例でもってさらに詳細な説明を行うこととする。
【実施例１】
【０２７７】
本実施例では、酸化物半導体層を用いて作製された薄膜トランジスタの特性に関して示す。
【０２７８】
以下に、本実施例で用いたトランジスタの作製方法について説明する。
【０２７９】

まず、基板上に第１の導電膜を形成した後、当該第１の導電膜をフォトリソグラフィ法を用いてパターニングすることによりゲート電極５０２を形成した。続いて、当該ゲート電極５０２上にゲート絶縁層５０３を形成した。続いて、ゲート絶縁層５０３上に第２の導電膜とバッファ層を形成した。なお、基板を大気に曝すことなく連続して第２の導電膜とバッファ層を形成した。続いて、当該第２の導電膜及びバッファ層をフォトリソグラフィ法を用いてパターニングすることにより、一部がゲート電極と重なるソース電極層５０６ａ及びドレイン電極層５０６ｂを形成した。続いて、ゲート絶縁層、ソース電極層及びドレイン電極層上に酸化物半導体層を形成した後、当該酸化物半導体層をフォトリソグラフィ法を用いてパターニングすることにより、チャネル形成領域として機能する島状の酸化物半導体層５１０を形成した。続いて、窒素雰囲気下で３５０℃、１時間の熱処理を行った。

【０２８０】

基板として、旭ガラス社製のガラス基板（商品名ＡＮ１００）を用いた。

【０２８１】

ゲート電極５０２となる第１の導電膜として、スパッタ法を用いて膜厚１００ｎｍのタングステン膜を形成した。

【０２８２】

ゲート絶縁層５０３として、プラズマＣＶＤ法を用いて膜厚１００ｎｍの酸化窒化シリコン膜を形成した。

【０２８３】

ソース電極層５０６ａ及びドレイン電極層５０６ｂとなる第２の導電膜として、スパッタ法を用いて膜厚１００ｎｍのタングステン膜を形成した。

【０２８４】

バッファ層は、スパッタ法によって５～１０ｎｍのＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を形成した。成膜条件は、アルゴンガスのみを用い、ターゲットは、In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１としたターゲットを用いた。

【０２８５】

酸化物半導体層は、スパッタ法によって１５０ｎｍのＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を成膜した。成膜条件は、圧力を０．４Ｐａとし、電力を５００Ｗとし、成膜温度を２５℃とし、アルゴンガス流量を１０ｓｃｃｍとし、酸素流量を５ｓｃｃｍとし、ガラス基板とターゲット間の距離を１７０ｍｍとし、直流（ＤＣ（Ｄｉｒｅｃｔ　Ｃｕｒｒｅｎｔ））で行った。ターゲットは、In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：１としたターゲット（Ｉｎ：Ｇａ：Ｚｎ＝１：１：０．５）を用いた。また、プラズマ処理を行った後、基板５００を大気に曝すことなく連続して酸化物半導体層を形成した。なお、この成膜条件で得られた酸化物半導体層の組成を誘導結合プラズマ質量分析法（Ｉｎｄｕｃｔｉｖｅｌｙ　Ｃｏｕｐｌｅｄ　Ｐｌａｓｍａ　Ｍａｓｓ　Ｓｐｅｃｔｒｏｍｅｔｒｙ：ＩＣＰ－ＭＳ分析法）により測定した結果は、$InGa_{0.94}Zn_{0.40}O_{3.31}$であった。

【０２８６】

図２８に薄膜トランジスタのＶｇ－Ｉｇ曲線を示す。なお、本実施例では、トランジスタの測定は、ドレイン電圧（ソースの電圧に対するドレインの電圧）を１Ｖに設定して行った。

【０２８７】

また、本実施例では、トランジスタの構造を図２９に示すように形成した。具体的には、トランジスタのチャネル長Ｗを１００μｍ、チャネル幅Ｗを１００μｍ、ソース電極層５０６ａとゲート電極５０２が重なる長さＬｓを５μｍ、ドレイン電極層５０６ｂとゲート電極５０２が重なる長さＬｄを５μｍ、チャネル幅方向と平行な方向において酸化物半導体層５１０がソース電極層５０６ａ及びドレイン電極層５０６ｂと重ならない領域の長さＡを５μｍとした。

【０２８８】

以上により、基板を大気に曝すことなく連続して第２の導電膜とバッファ層を形成したことによって、トランジスタのオン・オフ比を高くし、電界効果移動度を高くすることができることがわかった。
【実施例２】
【０２８９】
また、本実施例では、エッチング後の電極形状の一例を示す。まず、サンプルを作製するプロセスについて図３０を用いて説明する。なお、実施例１とは、ソース電極層及びドレイン電極層の断面形状が異なっている点とバッファ層を形成しない点で異なっているだけであるため、同一の箇所には同一の符号を用いて説明する。
【０２９０】
まず、基板上に第１の導電膜を形成した後、当該第１の導電膜をフォトリソグラフィ法を用いてパターニングすることによりゲート電極５０２を形成した。続いて、当該ゲート電極５０２上にゲート絶縁層５０３を形成した（図３０（Ａ）参照）。続いて、ゲート絶縁層５０３上に第２の導電膜を形成した。続いて、当該第２の導電膜をフォトリソグラフィ法を用いてパターニングすることにより、一部がゲート電極と重なるソース電極層５０６ａ及びドレイン電極層５０６ｂを形成した（図３０（Ｂ）参照）。続いて、ゲート絶縁層、ソース電極層及びドレイン電極層上に酸化物半導体層を形成した後、当該酸化物半導体層をフォトリソグラフィ法を用いてパターニングすることにより、チャネル形成領域として機能する島状の酸化物半導体層５１０を形成した（図３０（Ｃ）参照）。
【０２９１】
基板として、旭ガラス社製のガラス基板（商品名ＡＮ１００）を用いた。
【０２９２】
ゲート電極５０２となる第１の導電膜として、スパッタ法を用いて膜厚１００ｎｍのタングステン膜を形成した。
【０２９３】
ゲート絶縁層５０３として、プラズマＣＶＤ法を用いて膜厚１００ｎｍの酸化窒化シリコン膜を形成した。
【０２９４】
ソース電極層６０６ａ及びドレイン電極層６０６ｂとなる第２の導電膜として、スパッタ法を用いて膜厚１００ｎｍのタングステン膜を形成した。
【０２９５】
酸化物半導体層は、スパッタ法によって１５０ｎｍのＩｎ－Ｇａ－Ｚｎ－Ｏ系非単結晶膜を成膜した。成膜条件は、実施例１と同じである。
【０２９６】
ソース電極層６０６ａ及びドレイン電極層６０６ｂのエッチングは、コイル状アンテナを用いるＩＣＰエッチング装置を用いて行った。CF_4のガス流量を２５（ｓｃｃｍ）、Cl_3のガス流量を２５（ｓｃｃｍ）、O_2のガス流量を１０（ｓｃｃｍ）とし、１．５Ｐａの圧力でコイル型の電極に５００ＷのＲＦ（１３．５６ＭＨｚ）電力を投入してプラズマを生成してエッチングを行う。基板側（試料ステージ）にも１０ＷのＲＦ（１３．５６ＭＨｚ）電力を投入し、実質的に負の自己バイアス電圧を印加する。少なくともゲート絶縁膜５０３がある程度露呈した段階で、このエッチングを途中で停止することにより、段差を有する電極側面が形成される。
【０２９７】
上記エッチング条件により、ソース電極層６０６ａの断面形状は、基板の基板面とソース電極層６０６ａの下端部側面とがなす角度θ１が２０°以上９０°未満とすることができる。図３０（Ｃ）中に示す点線で囲まれた部分の断面写真を図３１（Ａ）に示す。なお、図３１（Ｂ）は図３１（Ａ）の模式図である。図３１（Ａ）に示すように、θ１は約４０°である。また、図３１（Ａ）に示すように、基板の基板面とソース電極層６０６ａの上端部側面とがなす角度は約９０°である。なお、酸化物半導体層６１０を挟んで対向するソース電極層６０６ａ側面とドレイン電極層６０６ｂ側面の断面形状は同じエッチング工

程を経るため、ほぼ同一である。

【０２９８】

本実施例により、実施の形態２に示すソース電極層及びドレイン電極層の断面形状を作製することを示唆することができたと言える。

【図面の簡単な説明】

【０２９９】

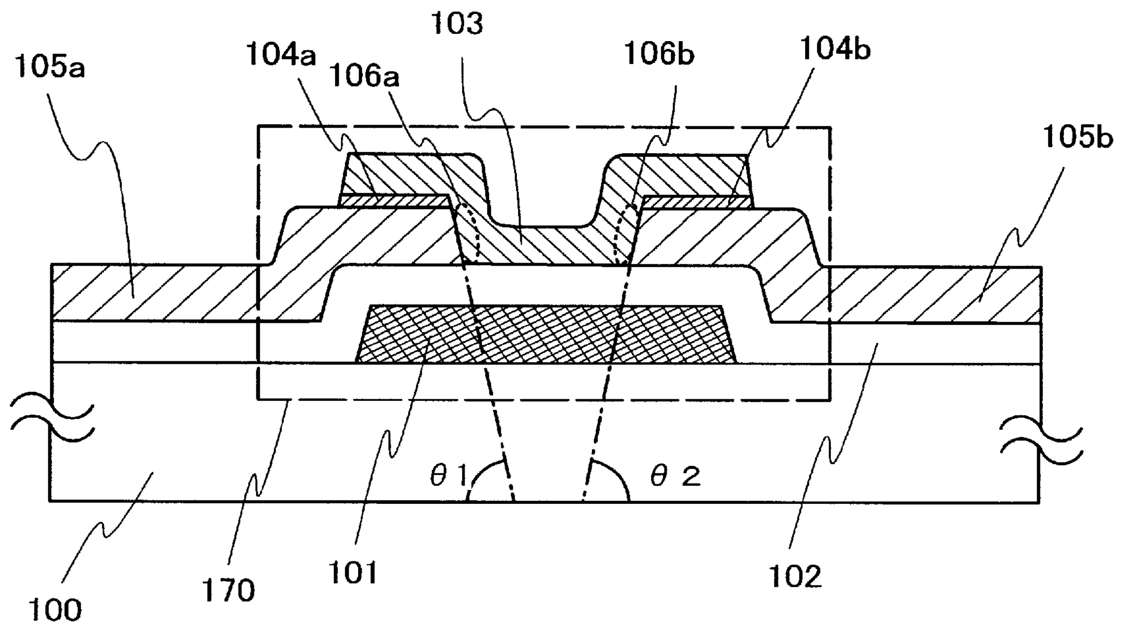
【図１】半導体装置の一例を説明する断面図である。
【図２】半導体装置の一例を説明する断面図である。
【図３】半導体装置の作製方法の一例を説明する断面図である。
【図４】半導体装置の作製方法の一例を説明する断面図である。
【図５】半導体装置の作製方法の一例を説明する上面図である。
【図６】半導体装置の作製方法の一例を説明する上面図である。
【図７】半導体装置の作製方法の一例を説明する上面図である。
【図８】半導体装置の作製方法の一例を説明する上面図である。
【図９】端子部の断面図の一例及び上面図の一例を示す図である。
【図１０】半導体装置の作製方法の一例を説明する上面図である。
【図１１】半導体装置の一例を説明する断面図である。
【図１２】半導体装置のブロック図の一例を説明する図である。
【図１３】信号線駆動回路の構成の一例を説明する図である。
【図１４】信号線駆動回路の動作の一例を説明するタイミングチャートである。
【図１５】信号線駆動回路の動作の一例を説明するタイミングチャートである。
【図１６】シフトレジスタの構成の一例を説明する図である。
【図１７】図１６に示すフリップフロップの接続構成を説明する図である。
【図１８】半導体装置の画素等価回路の一例を説明する図である。
【図１９】半導体装置の一例を説明する断面図である。
【図２０】半導体装置の一例を説明する断面図及び上面図である。
【図２１】半導体装置の一例を説明する断面図である。
【図２２】半導体装置の一例を説明する断面図及び上面図である。
【図２３】電子ペーパーの使用形態の例を説明する図である。
【図２４】電子書籍の一例を示す外観図である。
【図２５】テレビジョン装置およびデジタルフォトフレームの例を示す外観図である。
【図２６】遊技機の例を示す外観図である。
【図２７】携帯電話機の一例を示す外観図である。
【図２８】薄膜トランジスタの電気特性の一例を示す図である。
【図２９】電気特性を得るために作製した薄膜トランジスタの上面図である。
【図３０】サンプルを作製する工程を示す断面図である。
【図３１】サンプルの断面一部を示す写真である。
【図３２】（Ａ）半導体装置の断面構造の一例を示す図、（Ｂ）等価回路図、（Ｃ）上面図。

【符号の説明】

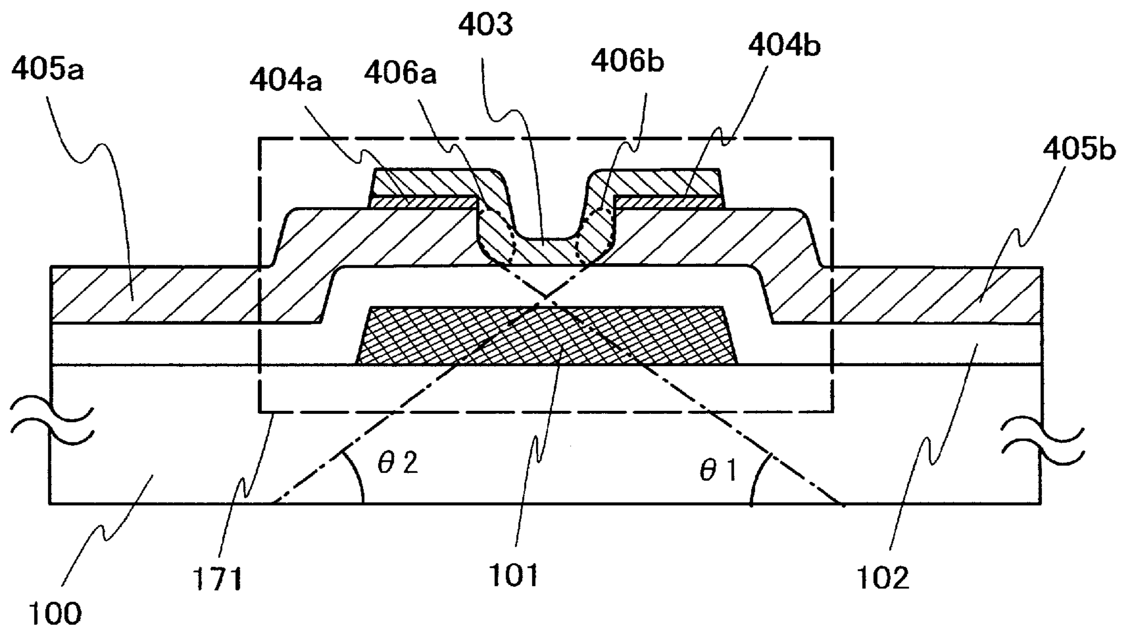
【０３００】

１００：基板
１０１：ゲート電極
１０２：ゲート絶縁層
１０３：酸化物半導体層
１０４ａ：第１のバッファ層
１０４ｂ：第２のバッファ層
１０５ａ：ソース電極層
１０５ｂ：ドレイン電極層

【書類名】図面
【図１】



【図２】



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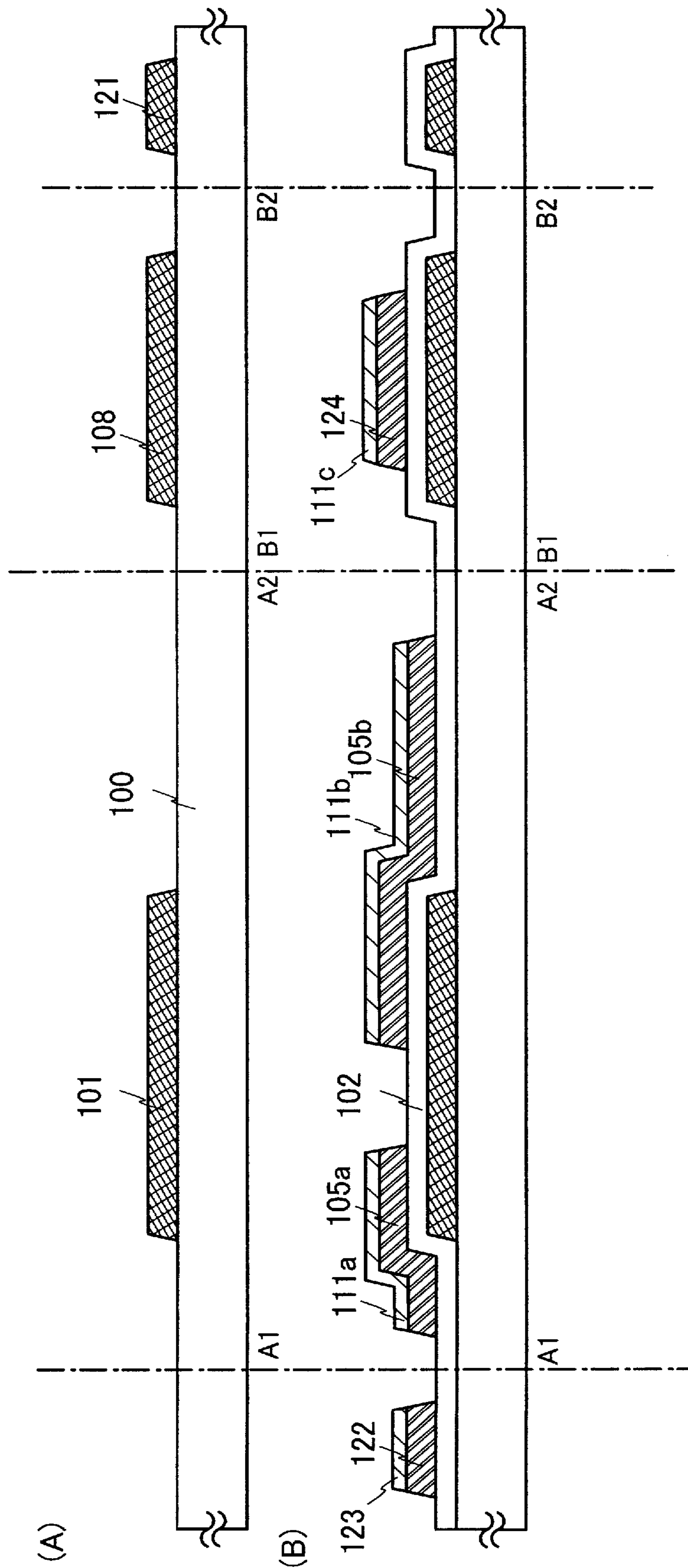

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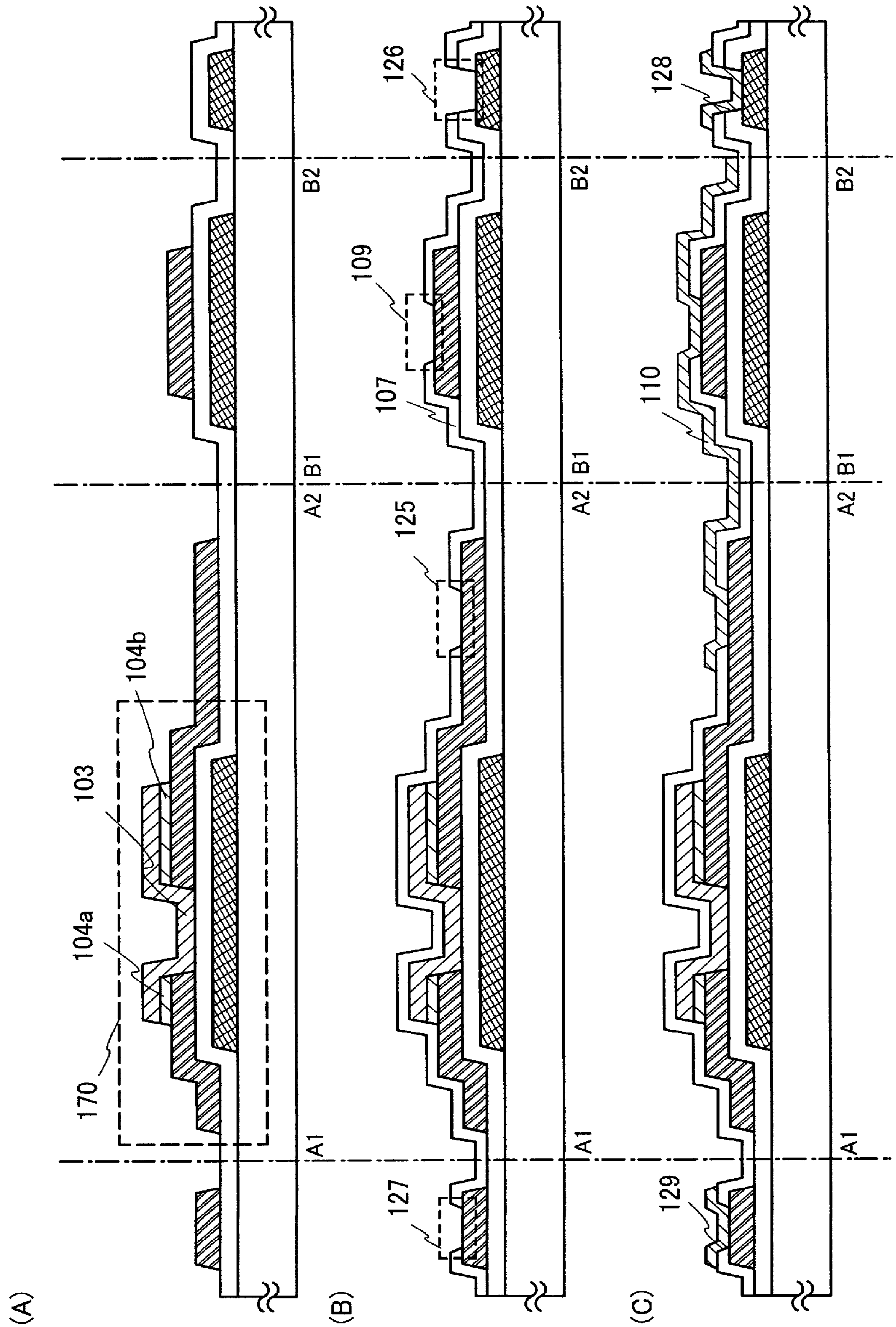

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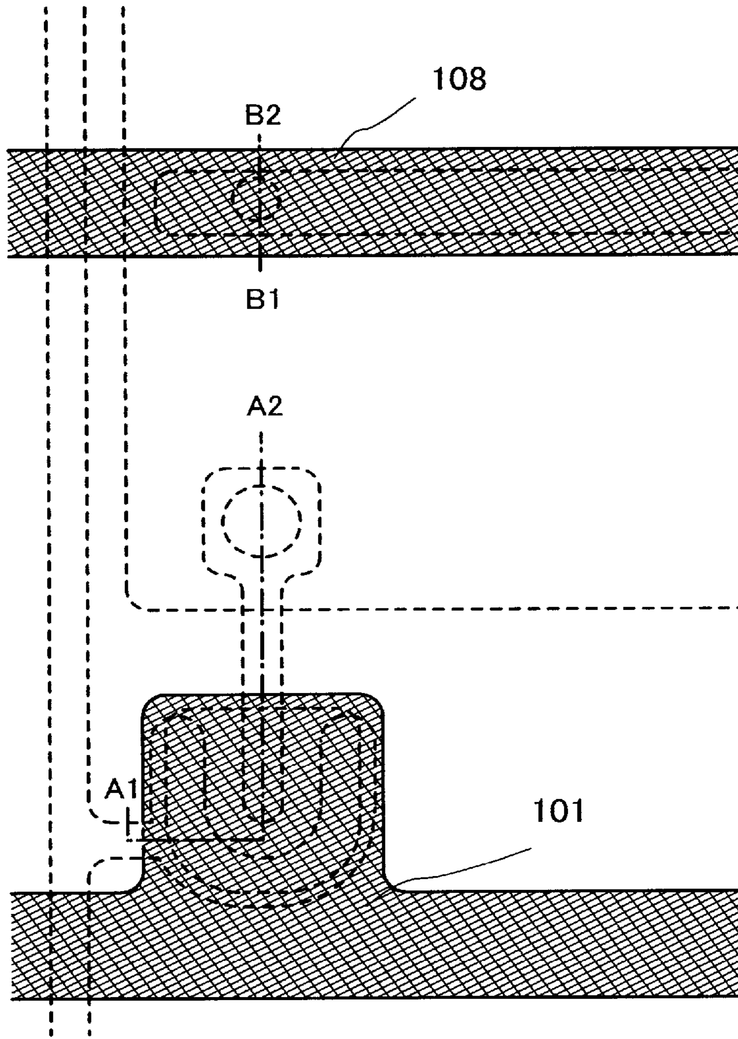

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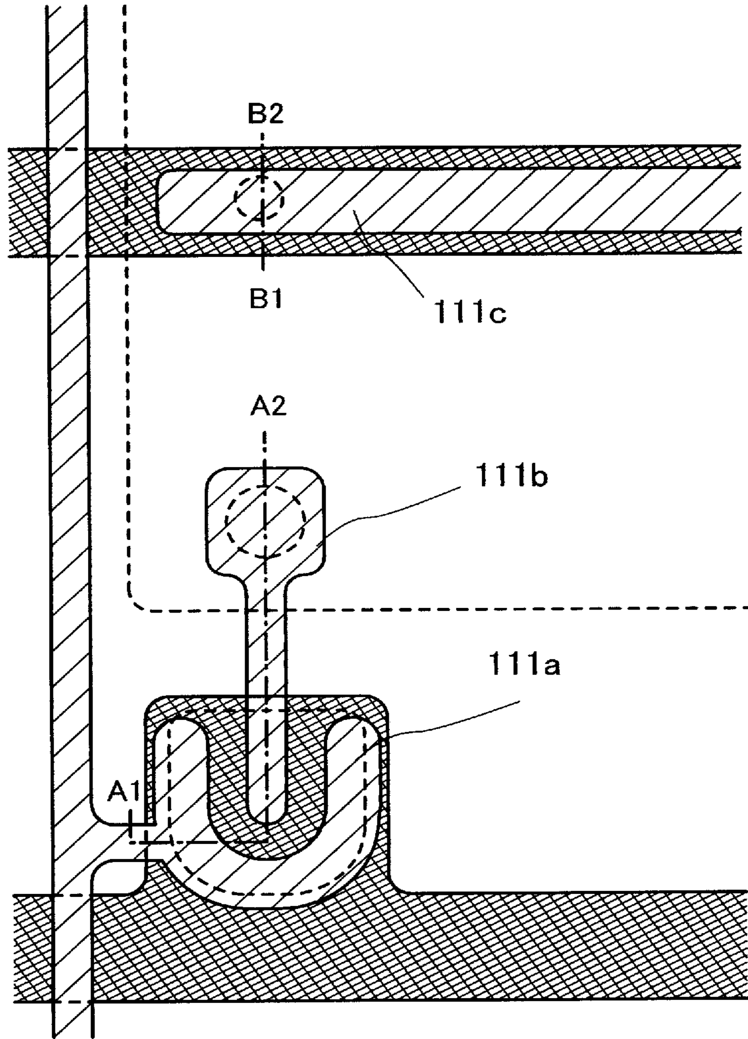

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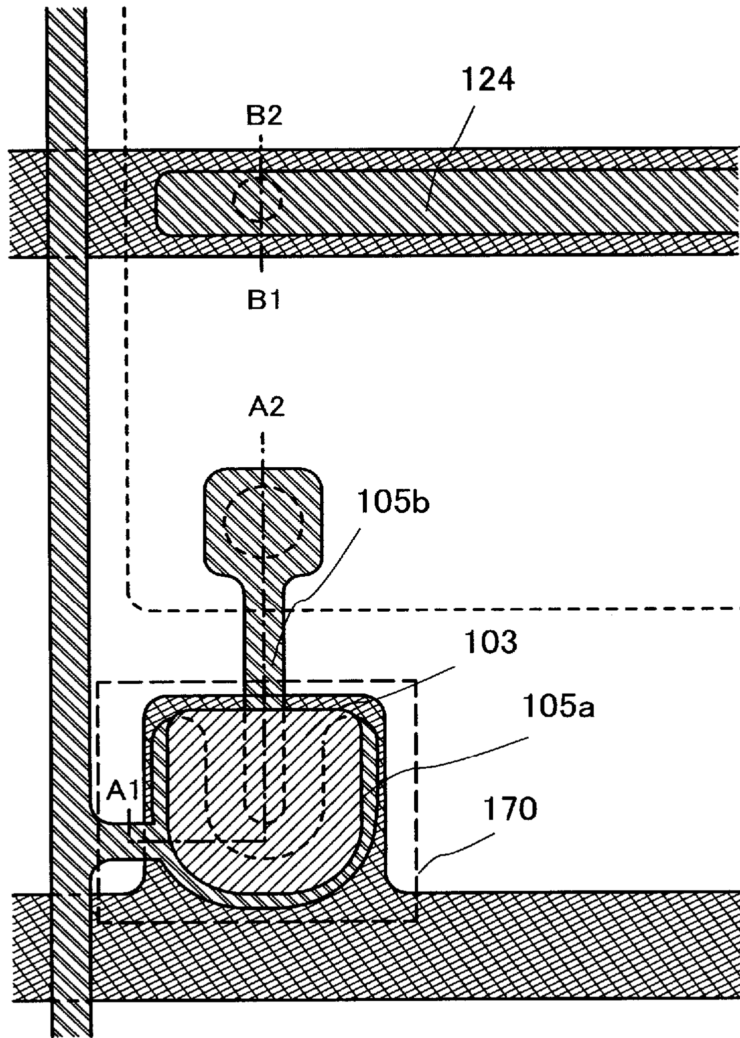

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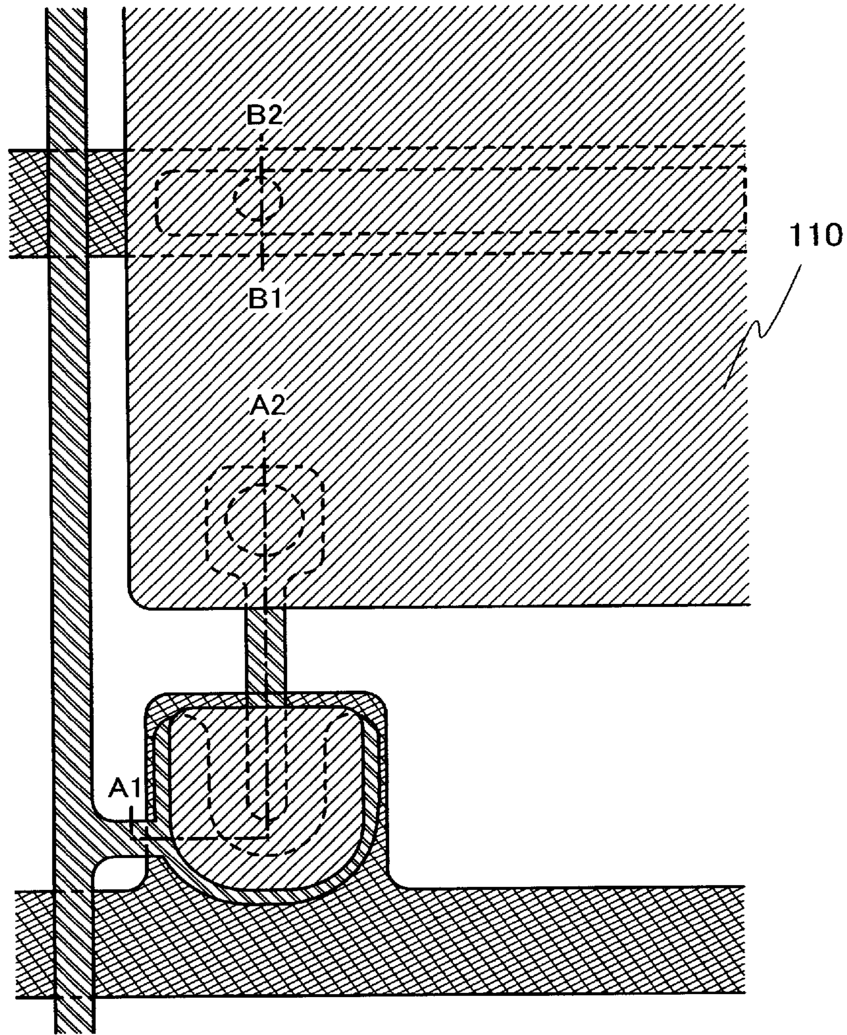
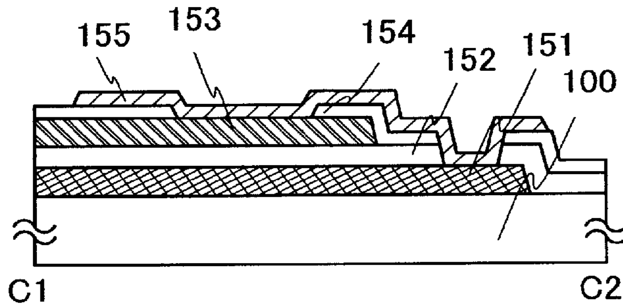


【図９】

(A1)



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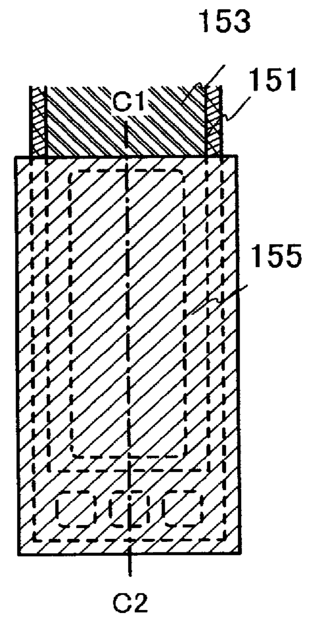

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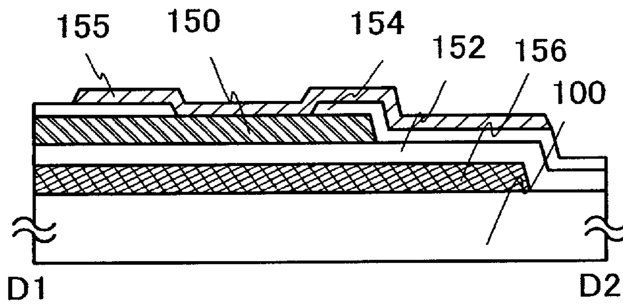

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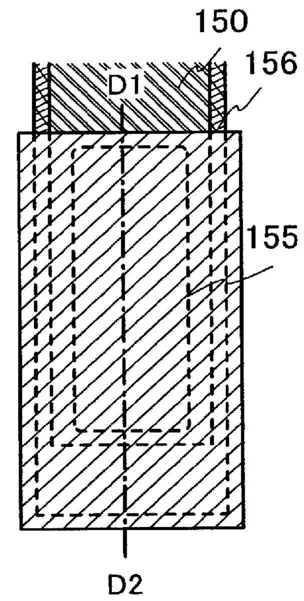

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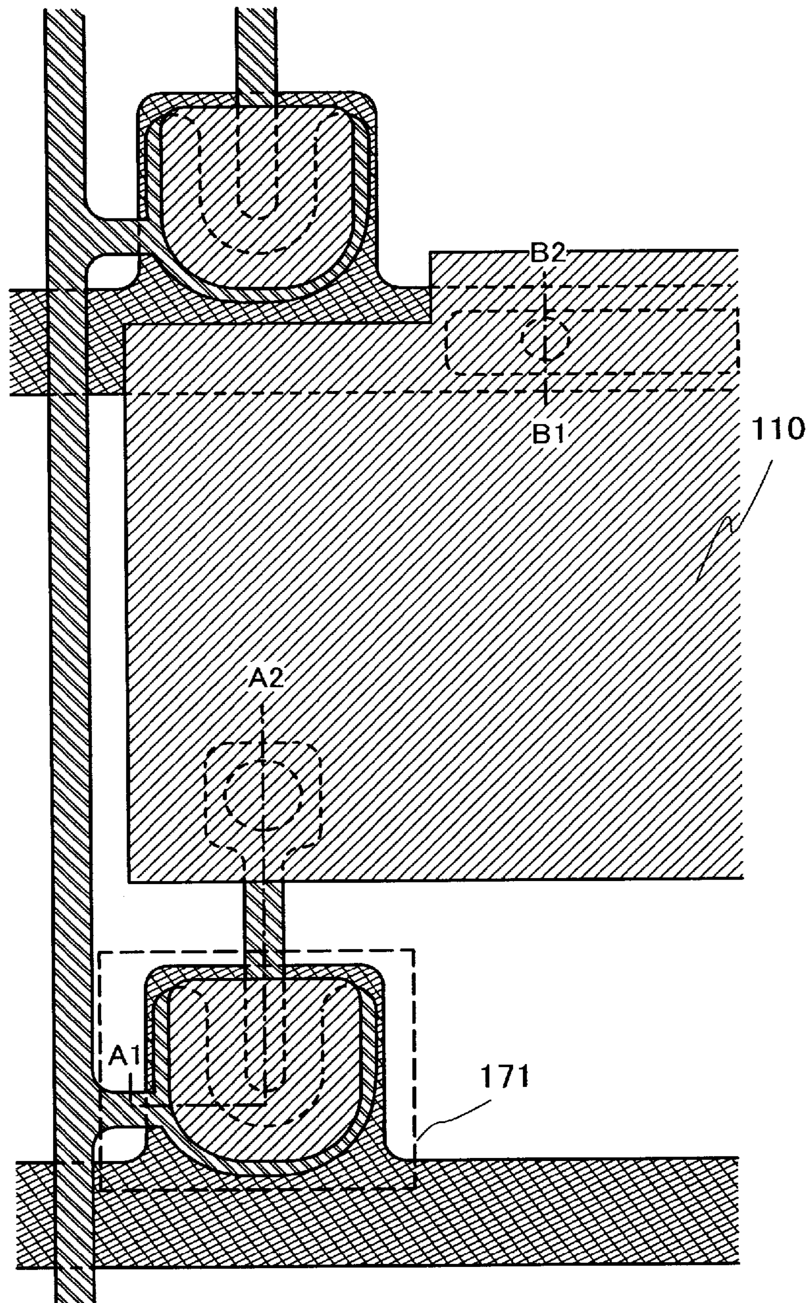
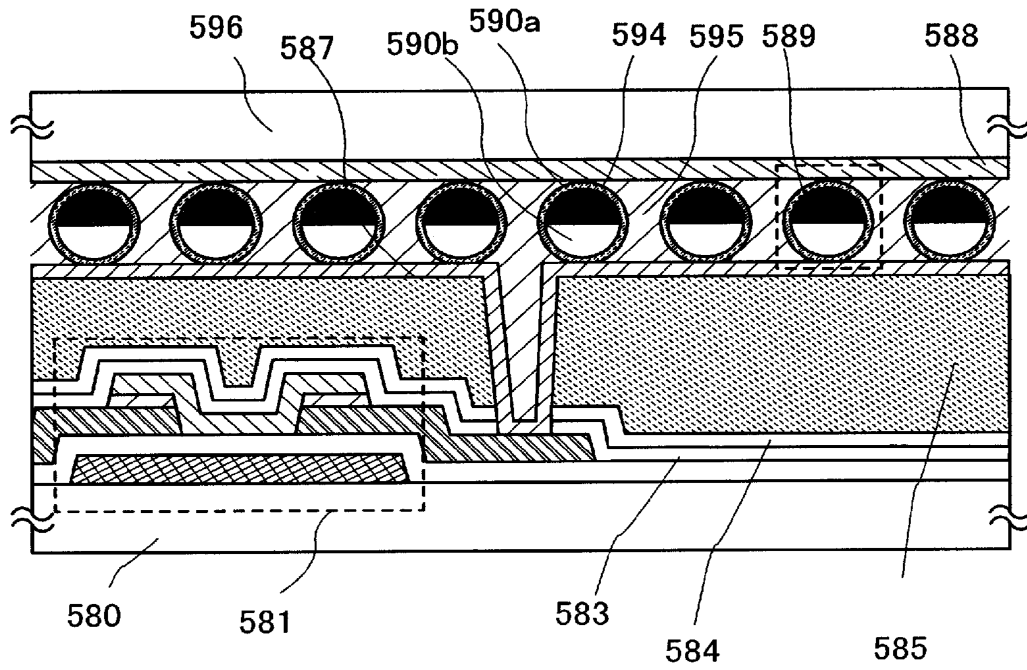
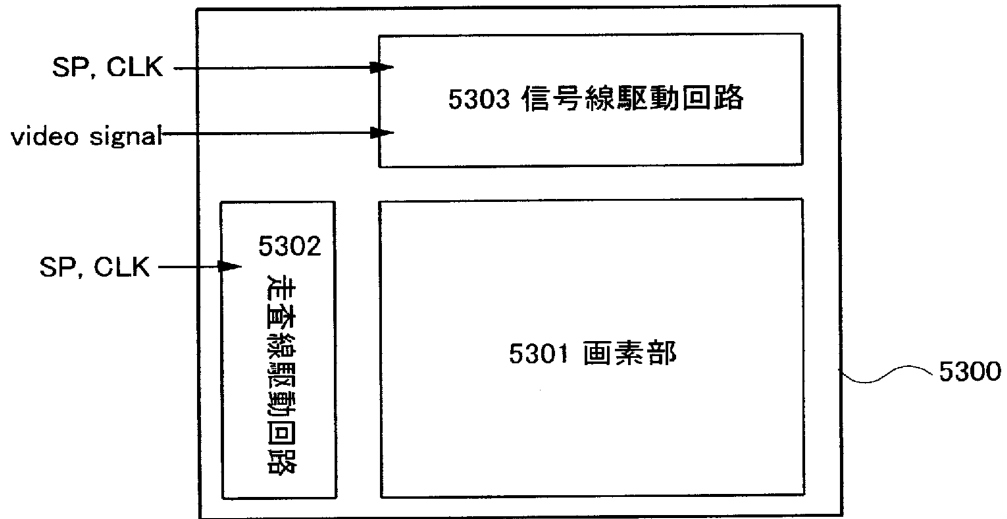


【図１１】

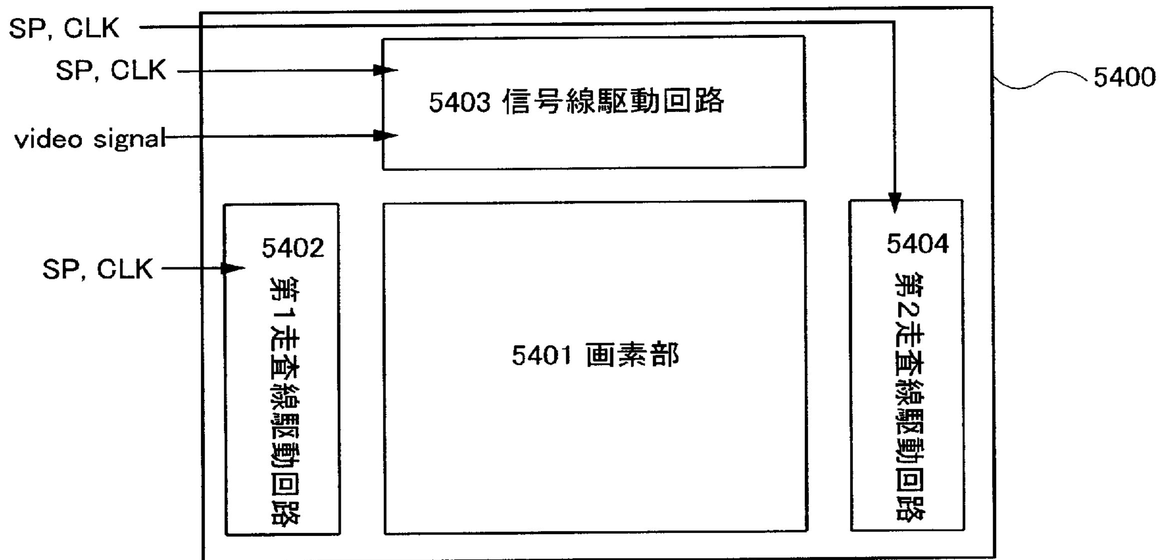


【図１２】

（A）



（B）



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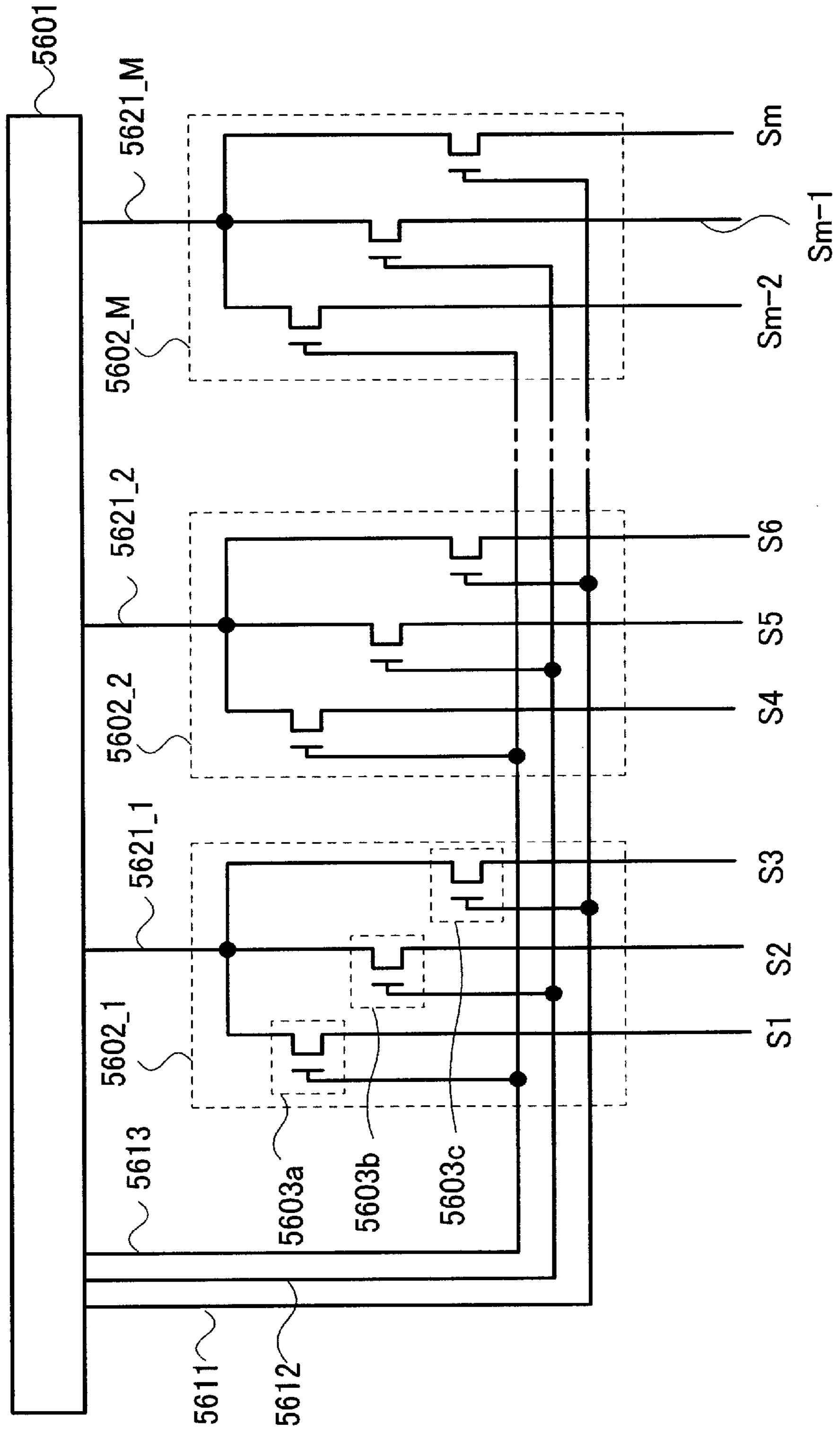

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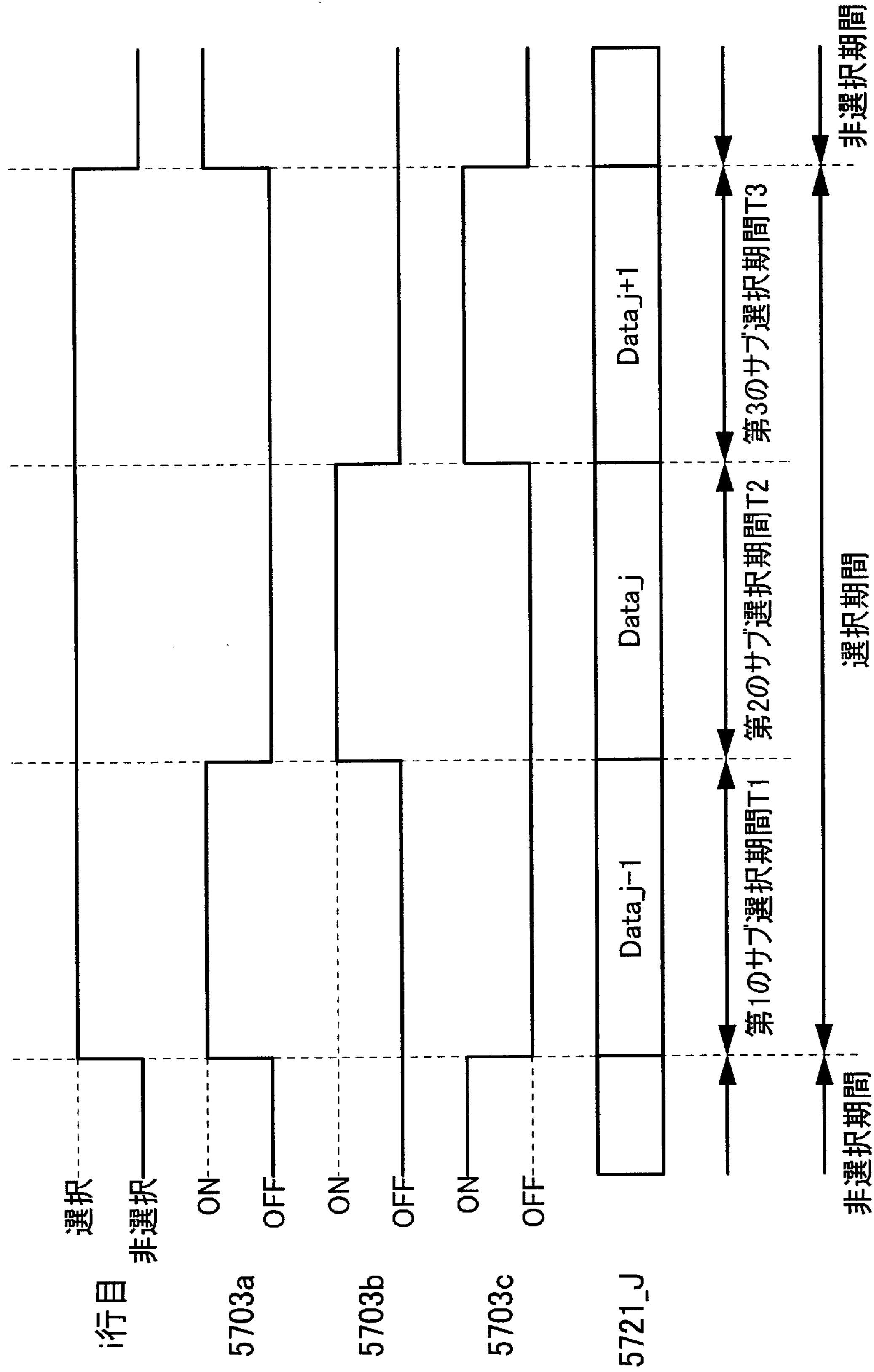

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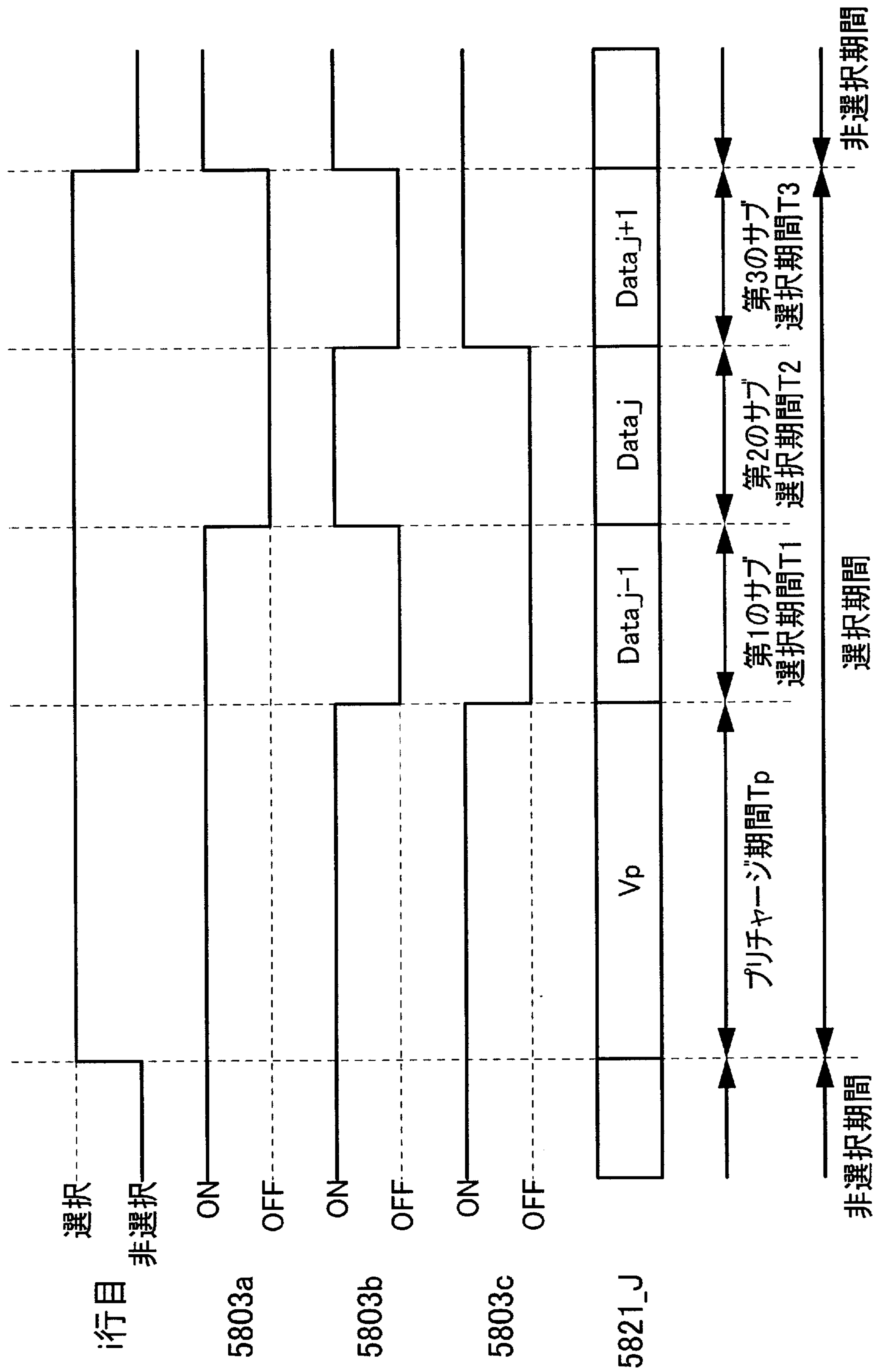

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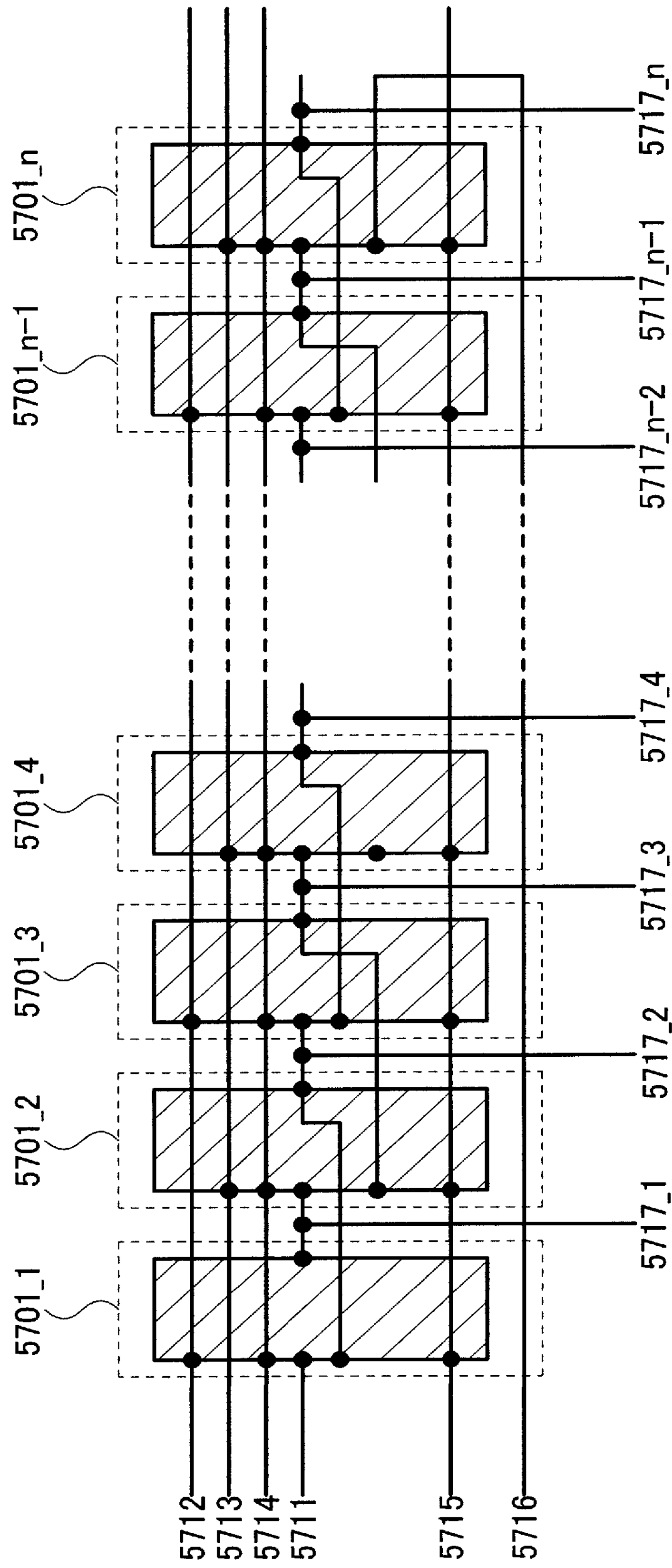

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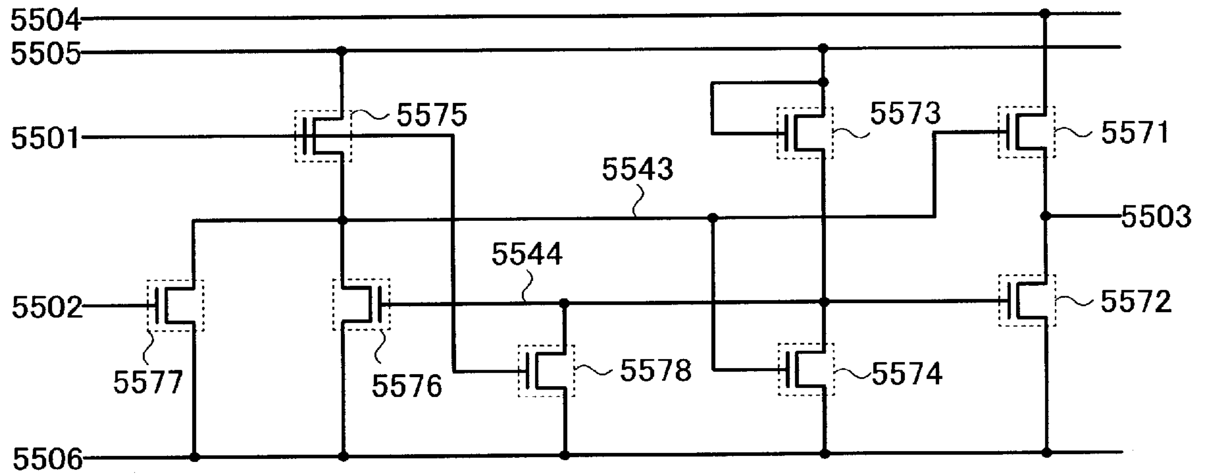

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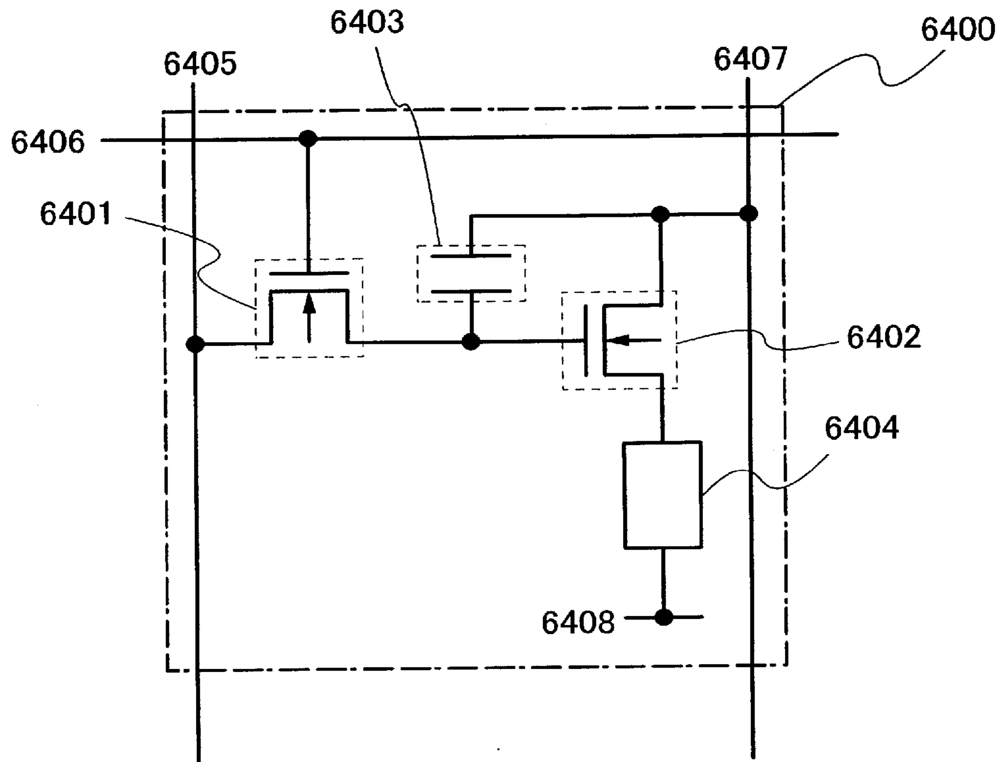

【図１９】

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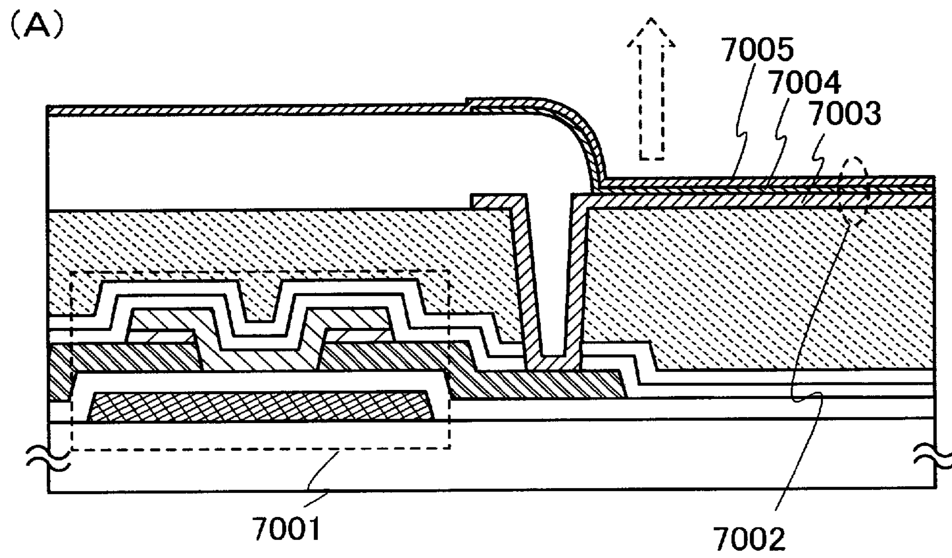
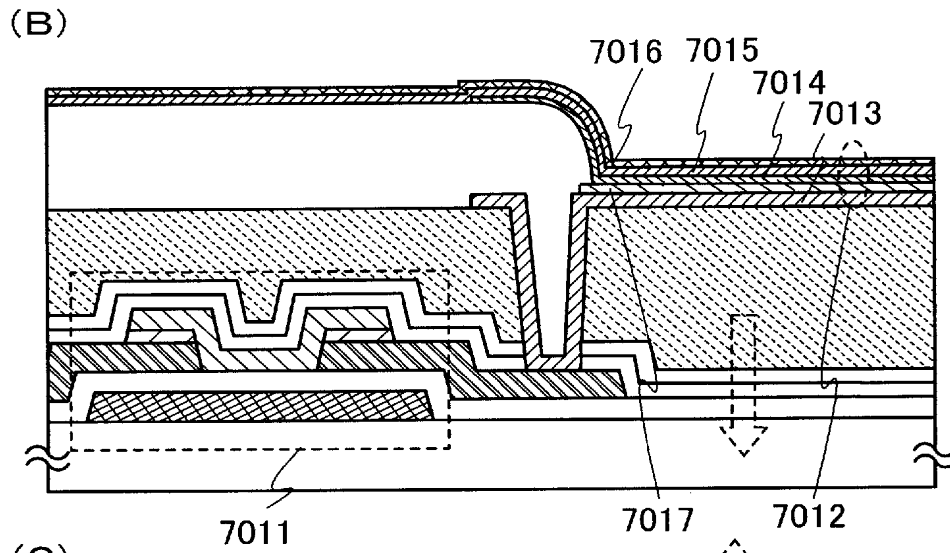


(B)



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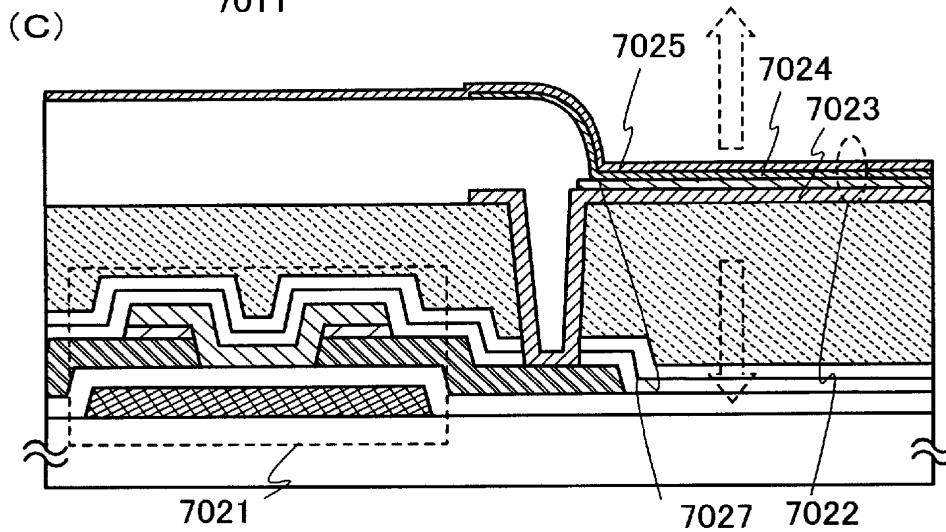

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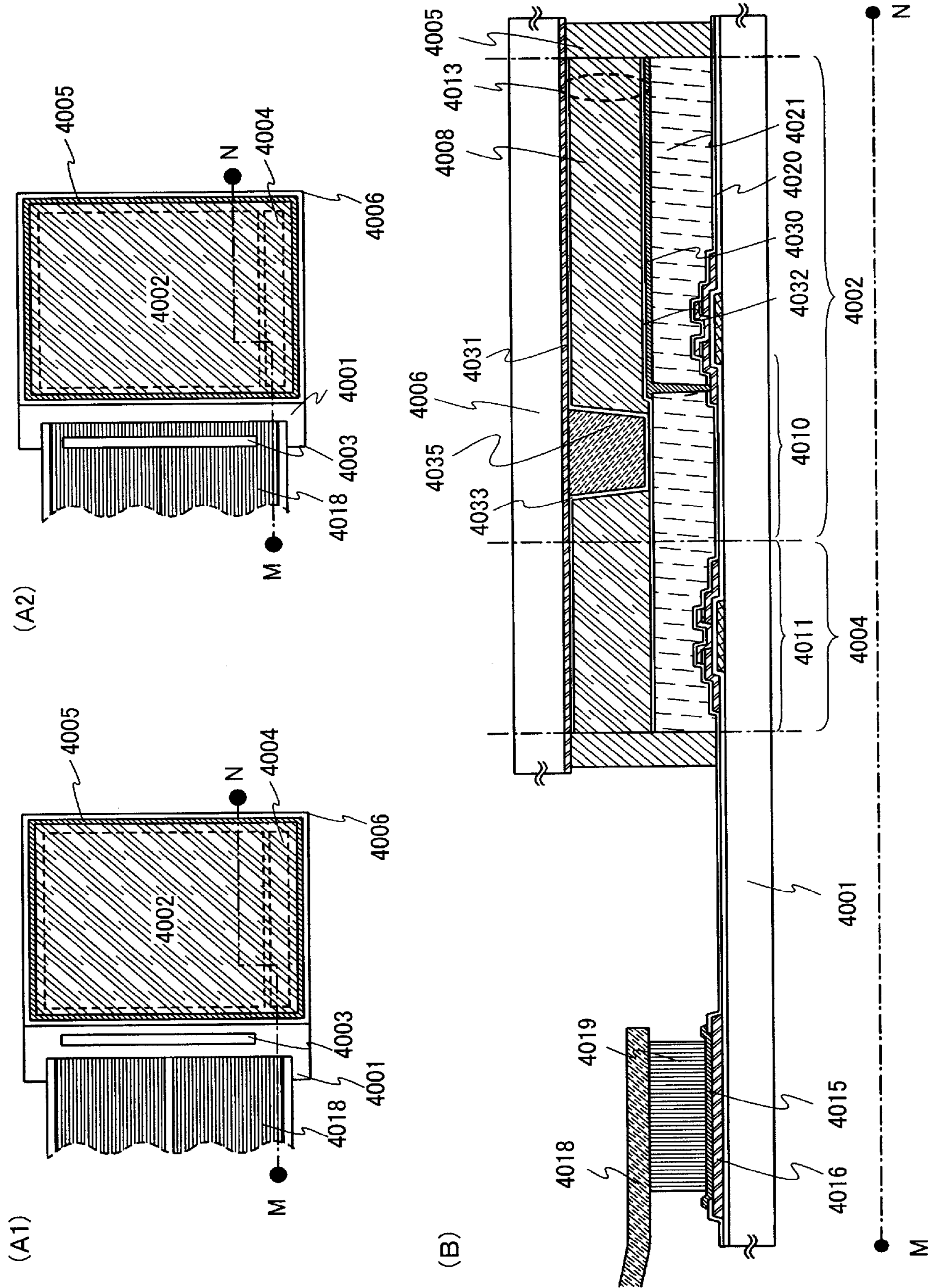

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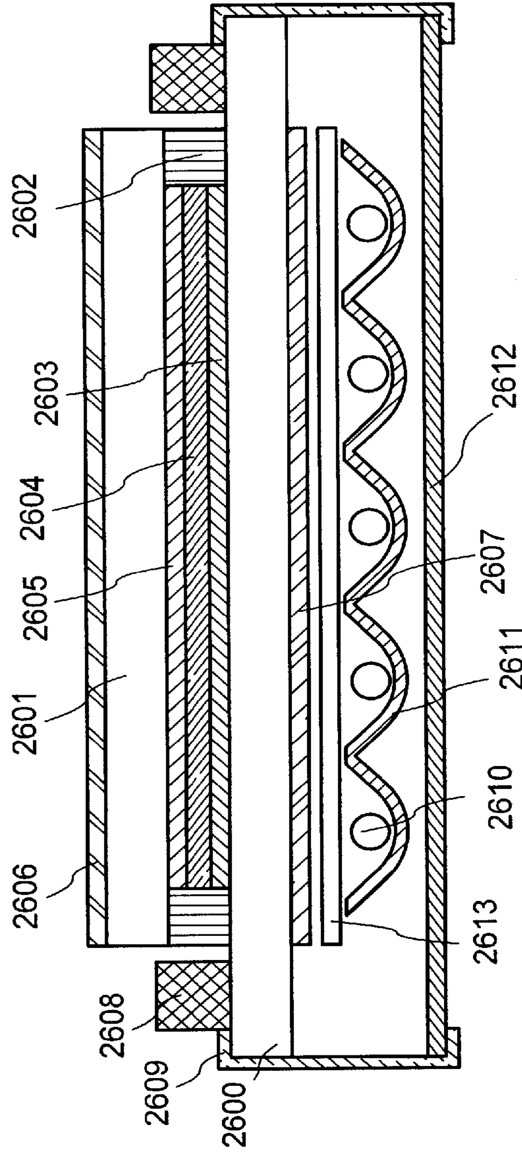

【図２２】

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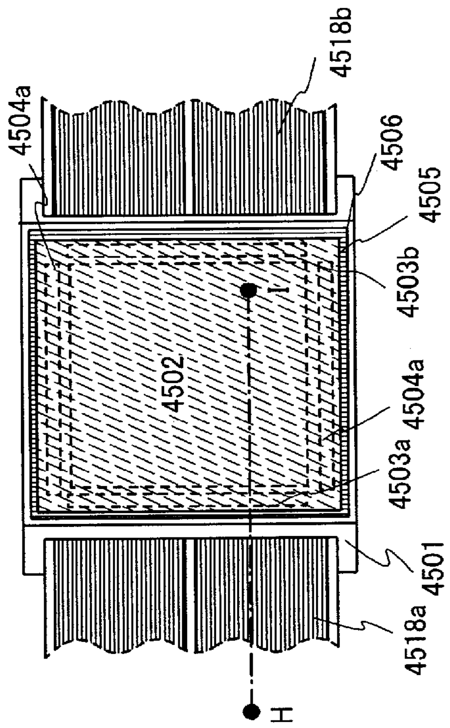

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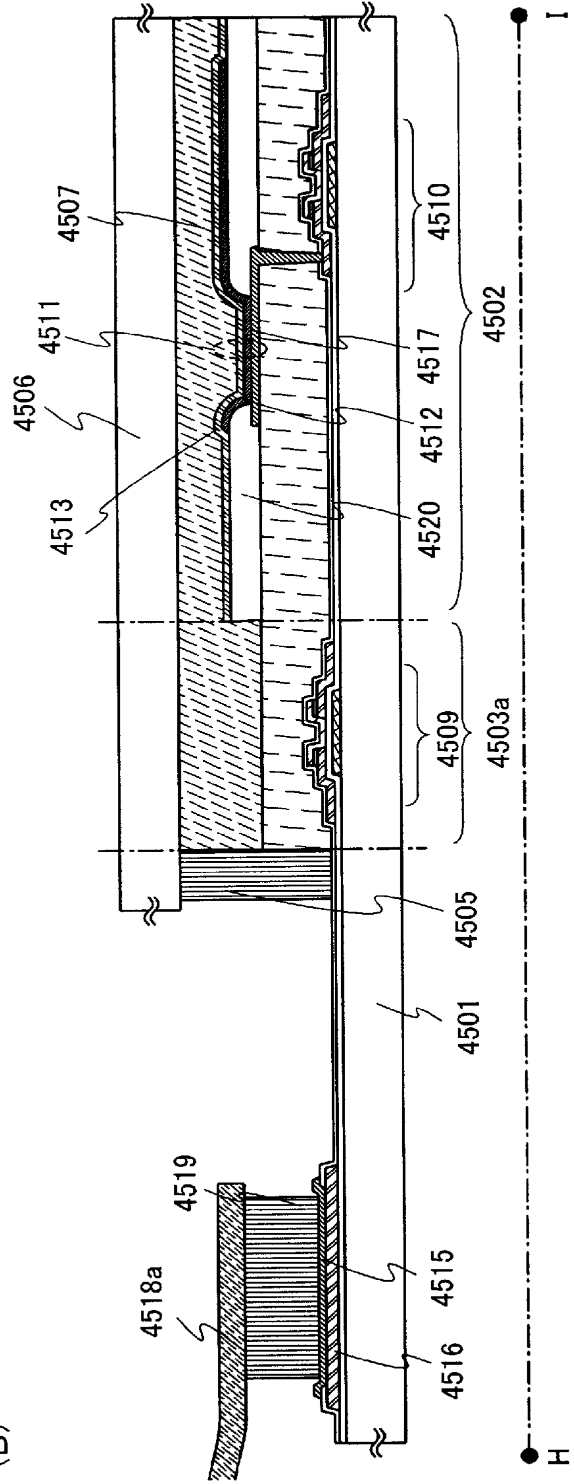

【図２３】

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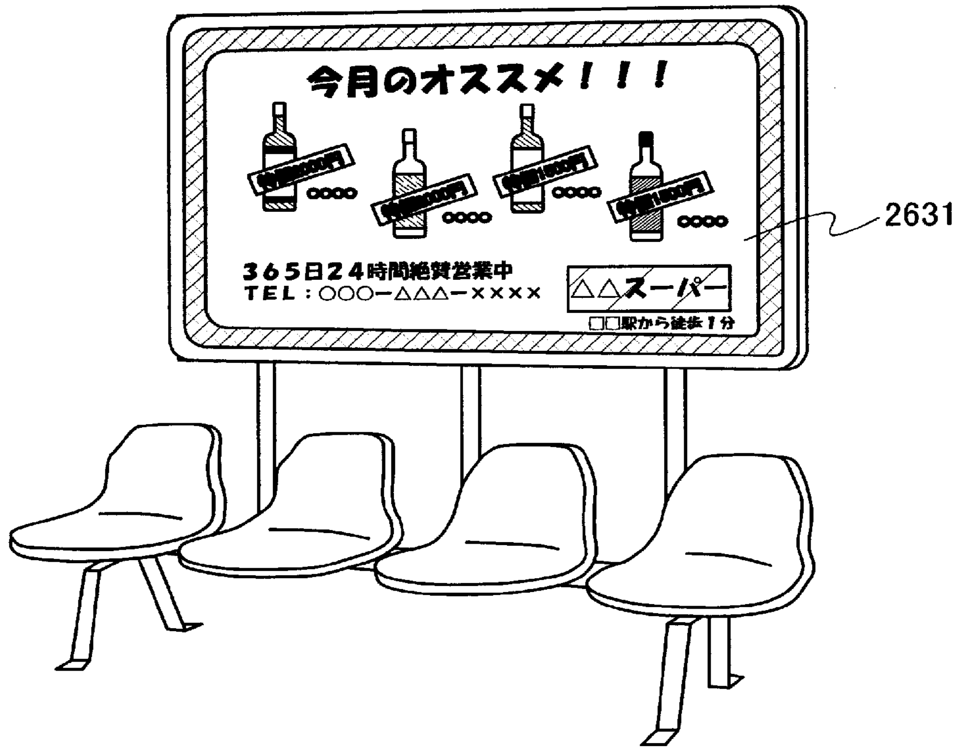
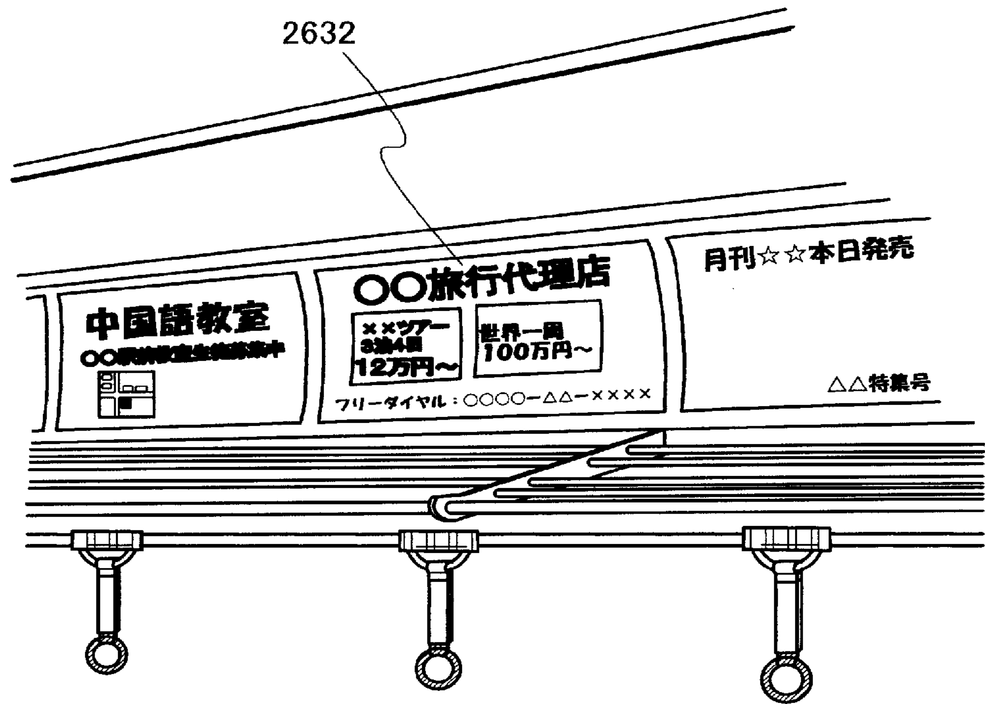


（B）



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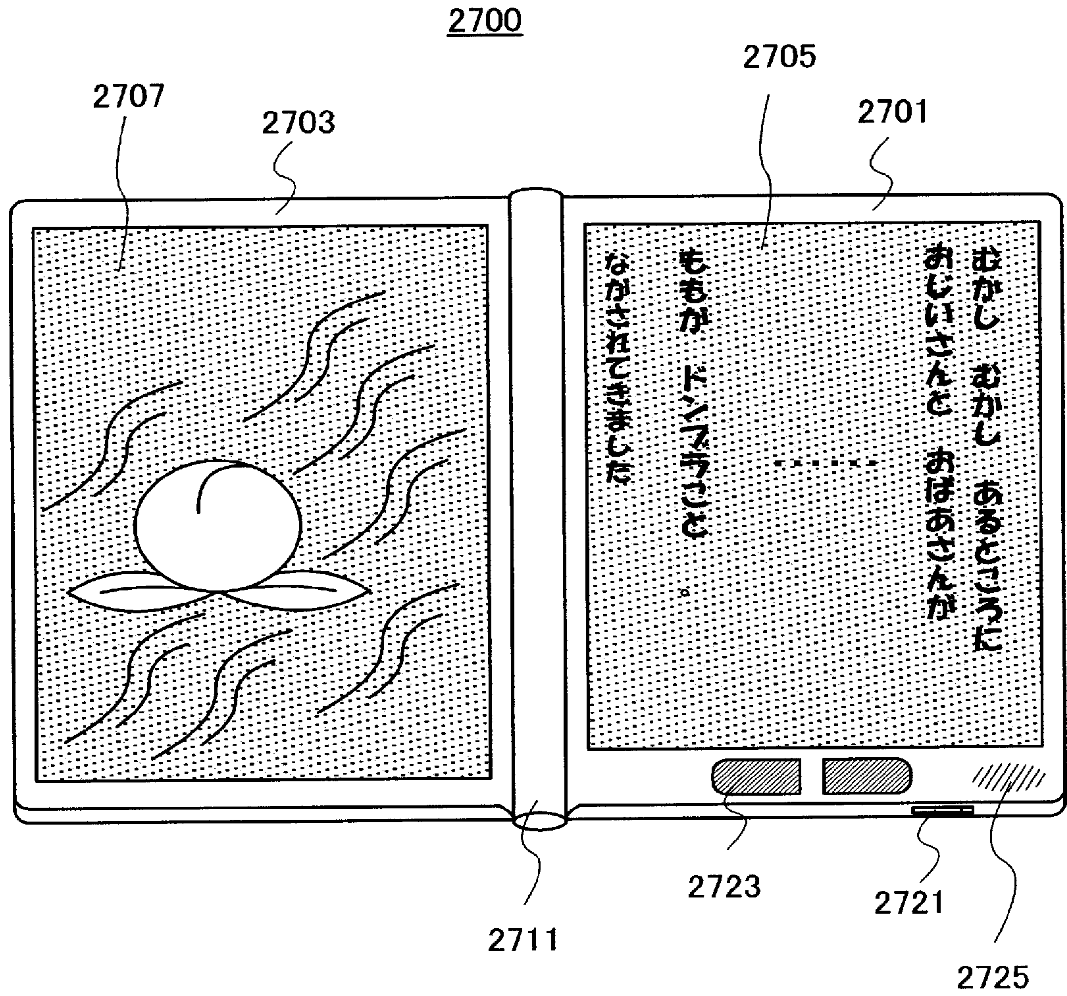

【図２５】

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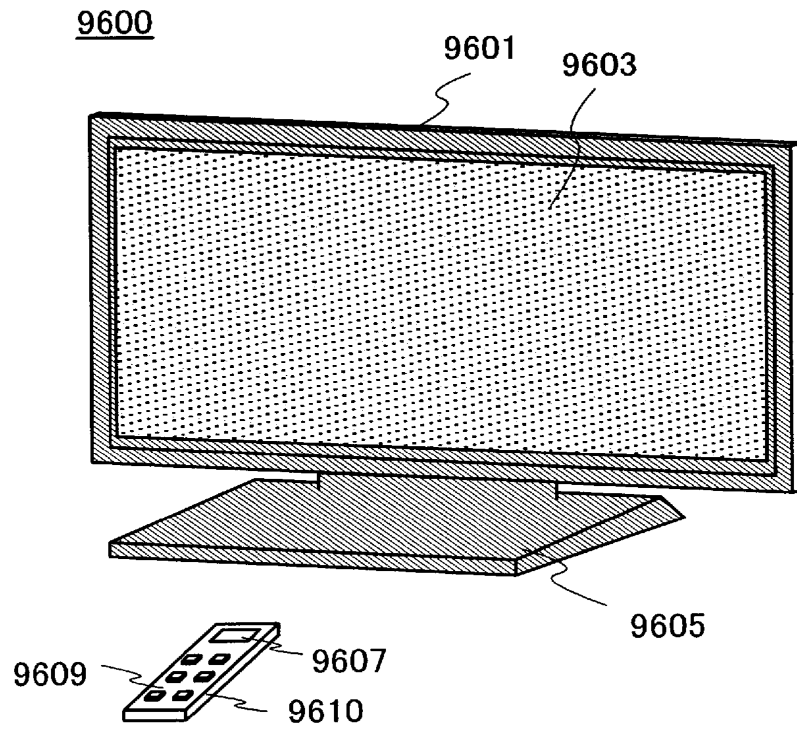

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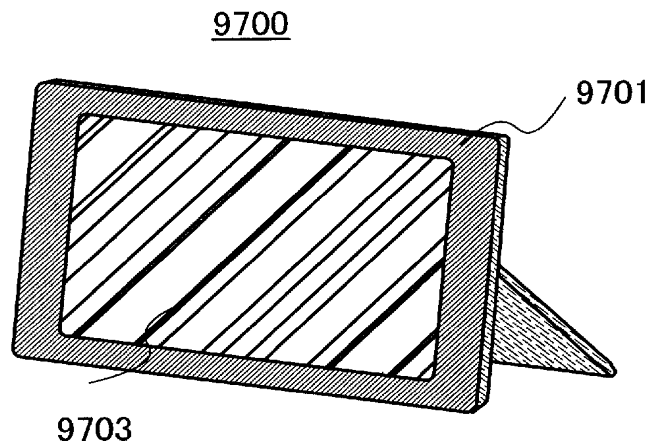
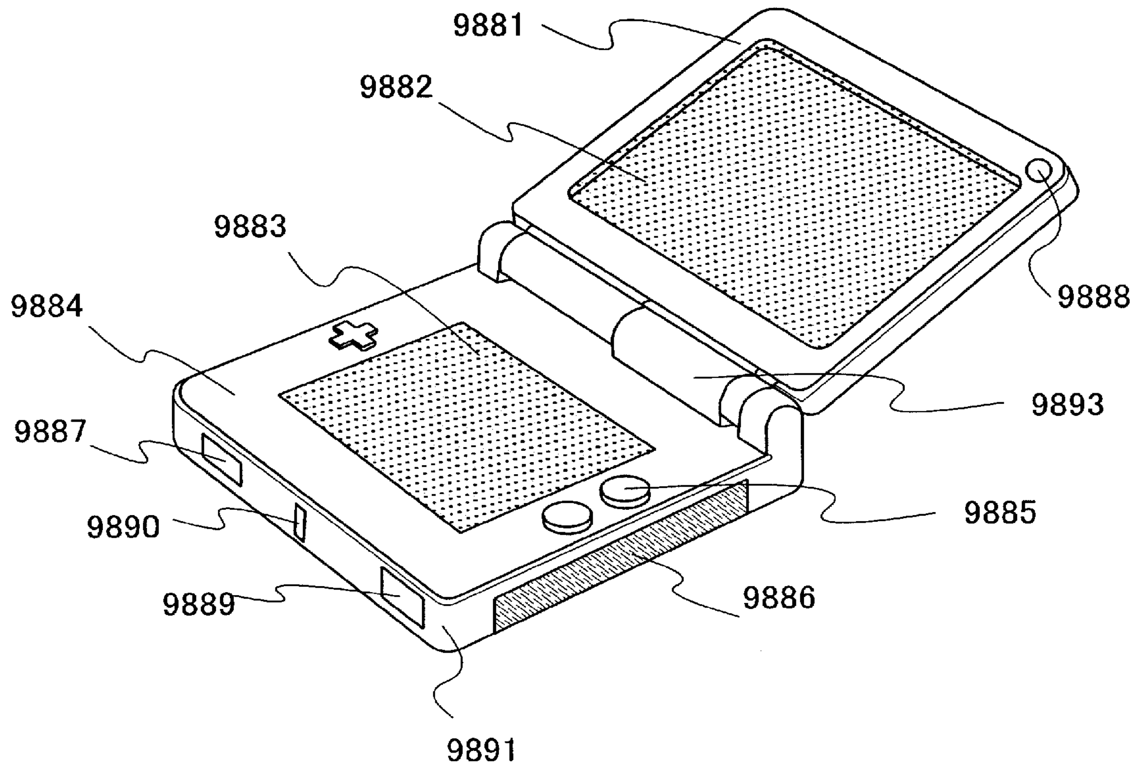


【図２６】

(A)



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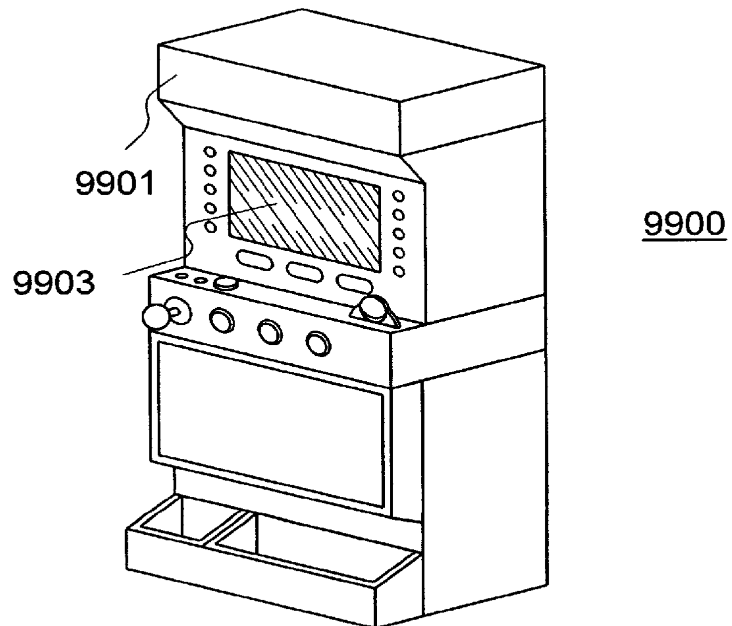

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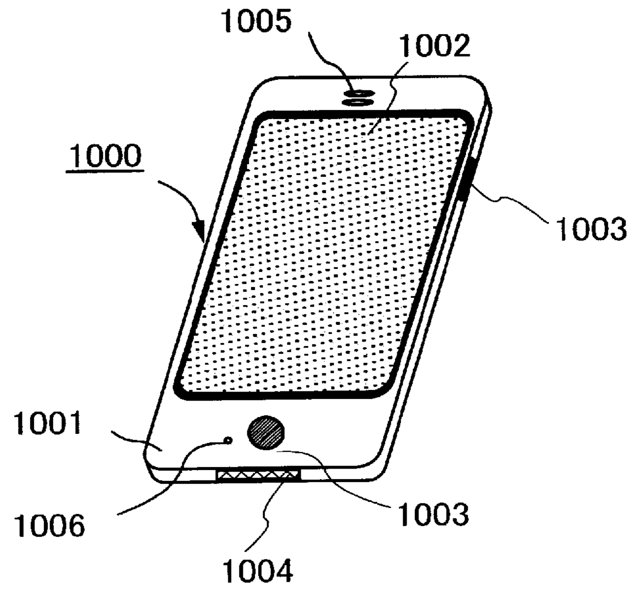

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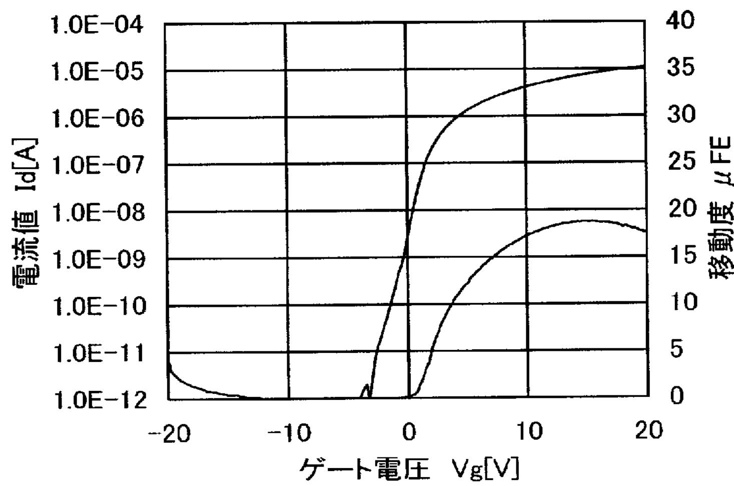
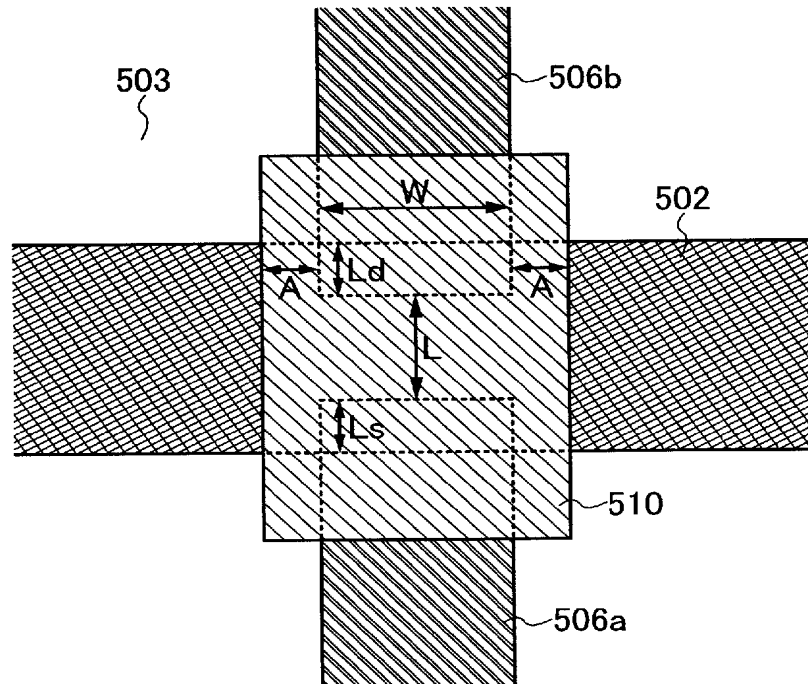
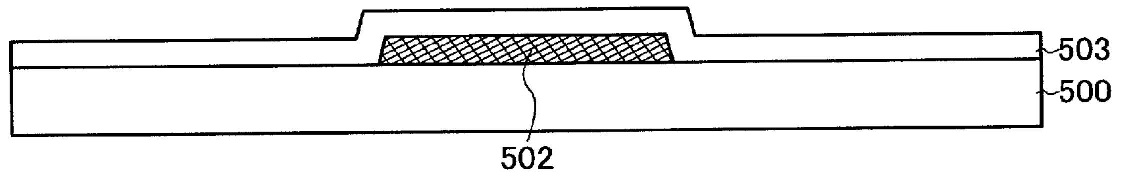


【図２９】



【図３０】

（A）



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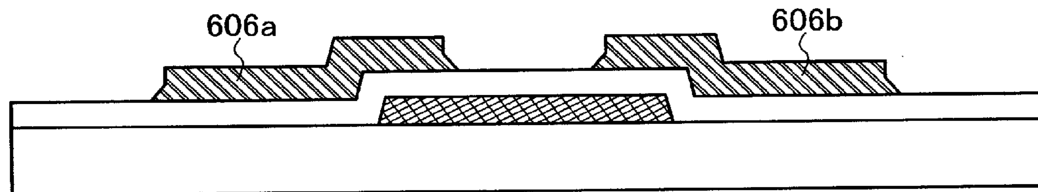

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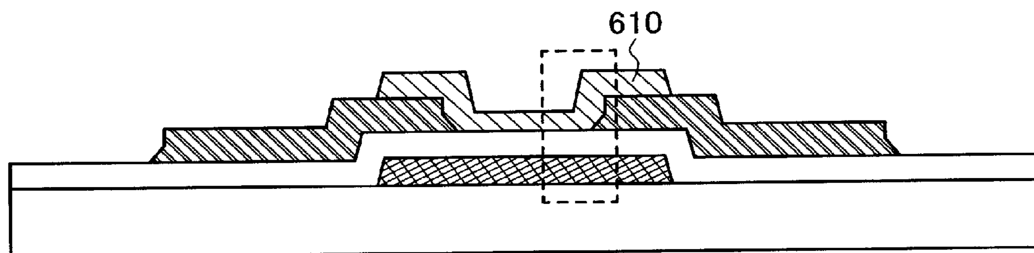
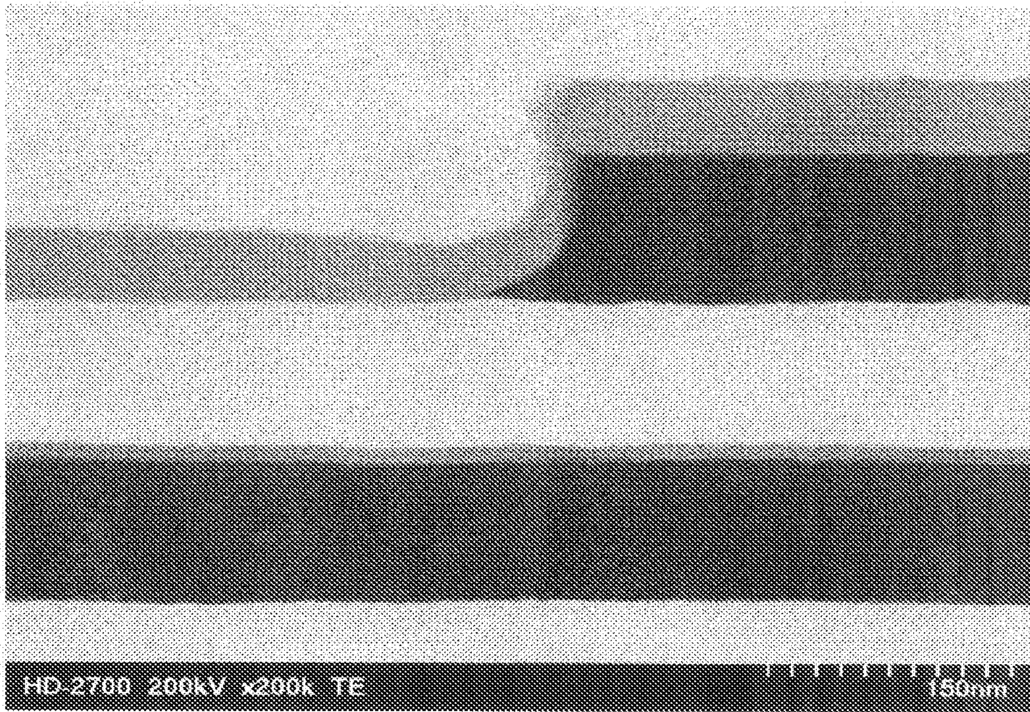
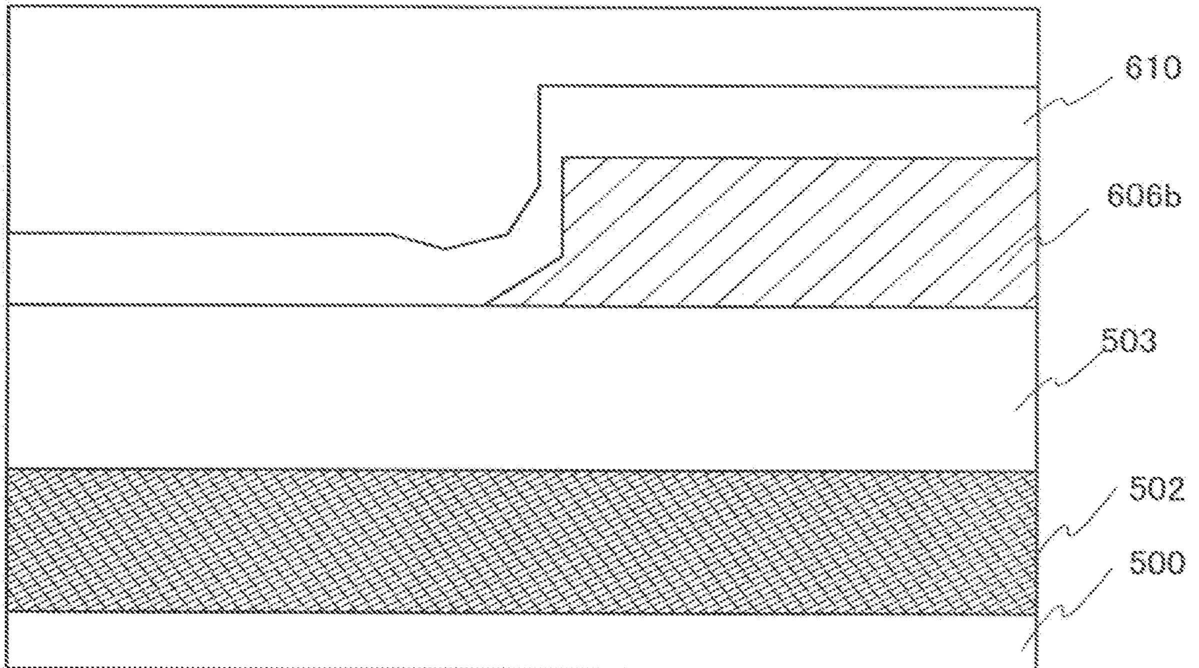


【図３１】

（Ａ）

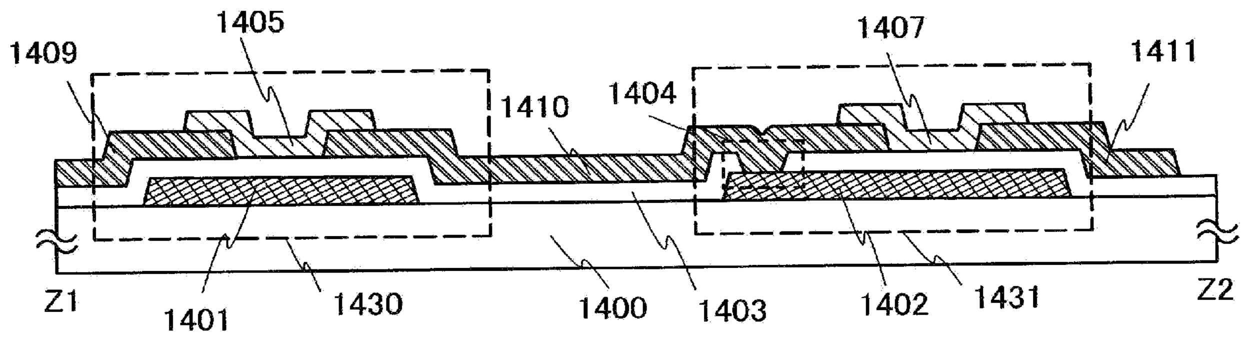


（Ｂ）



【図３２】

(A)



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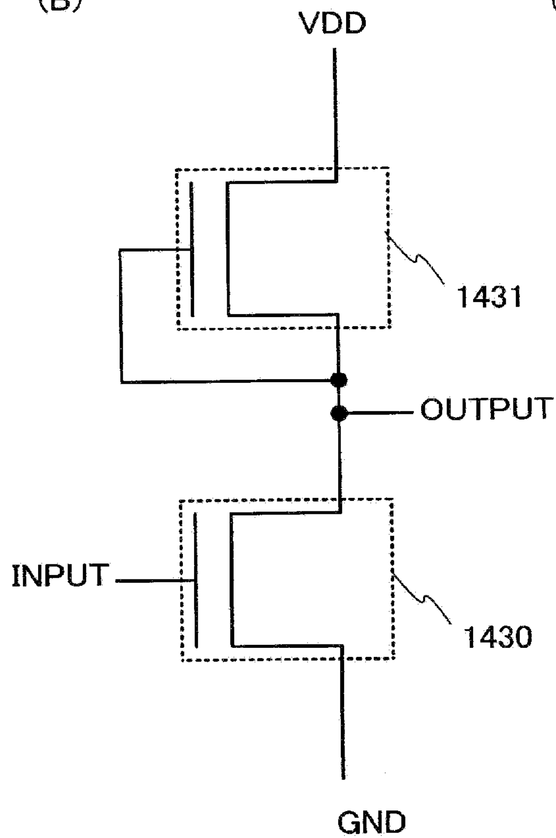

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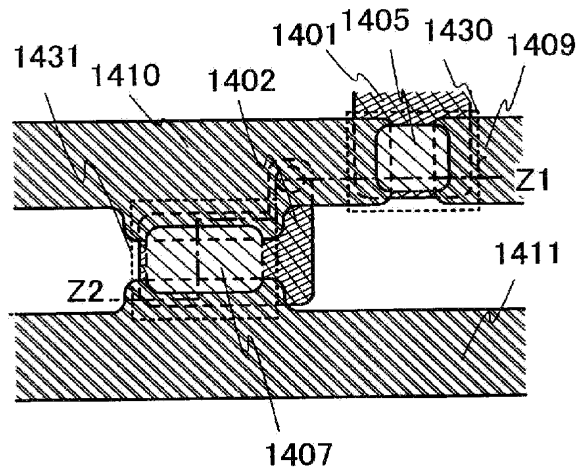


【書類名】要約書
【要約】
【課題】ボトムゲート型の薄膜トランジスタにおいて、ソース電極とドレイン電極間に生じる恐れのある電界集中を緩和し、スイッチング特性の劣化を抑える構造及びその作製方法を提供する。
【解決手段】ソース電極及びドレイン電極上に酸化物半導体層を有するボトムゲート型の薄膜トランジスタとし、酸化物半導体層と接するソース電極の側面の角度θ１及びドレイン電極の側面の角度θ２を２０°以上９０°未満とすることで、ソース電極及びドレイン電極の側面における電極上端から電極下端までの距離を大きくする。
【選択図】図１

出願人履歴

０００１５３８７８

19900817

新規登録

神奈川県厚木市長谷３９８番地

株式会社半導体エネルギー研究所

Attorney Docket No. 0756-10566

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 5776
Shunpei YAMAZAKI et al.	)	
Serial No. 14/451,680	)	
Filed: August 5, 2014	)	
For: SEMICONDUCTOR DEVICE	)	
AND MANUFACTURING	)	
METHOD THEREOF	)	

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Please consider the following amendments and remarks in connection with the above-identified application.

Amendments to the Claims are reflected in the listing of claims, which begin on page 2 of this paper.

Remarks begin on page 6 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (New) A semiconductor device comprising:
a glass substrate;
a gate electrode over the glass substrate;
a gate insulating film over the gate electrode;
a source electrode and a drain electrode over the gate insulating film; and
an oxide semiconductor film in contact with the source electrode and the drain electrode,
wherein a side surface of the source electrode faces a side surface of the drain electrode, and
wherein each of the side surface of the source electrode and the side surface of the drain electrode has a step in a lower end portion thereof.

3. (New) The semiconductor device according to claim 2, wherein the oxide semiconductor film is positioned on the source electrode and the drain electrode.

4. (New) The semiconductor device according to claim 2, wherein the source electrode and the drain electrode are in contact with the gate insulating film.

5. (New) The semiconductor device according to claim 2, wherein the oxide semiconductor film comprises indium, gallium, and zinc.

6. (New) The semiconductor device according to claim 2,

wherein a first angle of the step that is made between the side surface of the source electrode and an upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°, and

wherein a second angle of the step that is made between the side surface of the drain electrode and the upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°.

7. (New) The semiconductor device according to claim 2, comprising:

a first buffer layer between the oxide semiconductor film and the source electrode; and

a second buffer layer between the oxide semiconductor film and the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor film.

8. (New) A display device comprising:

a pixel portion comprising:

the semiconductor device according to claim 2; and

a display element electrically connected to one of the source electrode and the drain electrode.

9. (New) The display device according to claim 8, wherein the display element is a liquid crystal element.

10. (New) The display device according to claim 8, wherein the display element is a light-emitting element.

11. (New) A semiconductor device comprising:

a glass substrate;

a gate electrode over the glass substrate;

a gate insulating film over the gate electrode;

a source electrode and a drain electrode over the gate insulating film; and

an oxide semiconductor film in contact with the source electrode and the drain electrode,

wherein a side surface of the source electrode faces a side surface of the drain electrode,

wherein each of the side surface of the source electrode and the side surface of the drain electrode has a step in a lower end portion thereof,

wherein each of the source electrode and the drain electrode comprises a first layer and a second layer, and

wherein the first layer and the second layer comprises different material from each other.

12. (New) The semiconductor device according to claim 11, wherein the oxide semiconductor film is positioned on the source electrode and the drain electrode.

13. (New) The semiconductor device according to claim 11, wherein the source electrode and the drain electrode are in contact with the gate insulating film.

14. (New) The semiconductor device according to claim 11, wherein the oxide semiconductor film comprises indium, gallium, and zinc.

15. (New) The semiconductor device according to claim 11,

wherein a first angle of the step that is made between the side surface of the source electrode and an upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°, and

wherein a second angle of the step that is made between the side surface of the drain electrode and the upper surface of the glass substrate is greater than or equal to 20° and smaller than or equal to 90°.

16. (New) The semiconductor device according to claim 11, comprising:

a first buffer layer between the oxide semiconductor film and the source electrode; and

a second buffer layer between the oxide semiconductor film and the drain electrode,

wherein each of the first buffer layer and the second buffer layer has lower resistivity than the oxide semiconductor film.

17. (New) A display device comprising:

a pixel portion comprising:

the semiconductor device according to claim 11; and

a display element electrically connected to one of the source electrode and the drain electrode.

18. (New) The display device according to claim 17, wherein the display element is a liquid crystal element.

19. (New) The display device according to claim 17, wherein the display element is a light-emitting element.

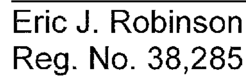
REMARKS

Claim 1 was pending in the present application prior to amendment. The present *Preliminary Amendment* is submitted to cancel claim 1 and add new claims 2-19 to recite additional protection to which the Applicant is entitled. Accordingly, claims 2-19 are pending in the present application, of which claims 2 and 11 are independent.

No new matter has been added. Examination on the merits is requested.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

Electronic Acknowledgement Receipt

EFS ID:	19861962
Application Number:	14451680
International Application Number:	
Confirmation Number:	5776
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Sue Ann Carr
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10566
Receipt Date:	14-AUG-2014
Filing Date:	05-AUG-2014
Time Stamp:	07:33:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	PAM.pdf	150332 7d8f65252e4402ccc675d78ff9b2fdff2e4e9ae6	no	6

Warnings:

Information:

Total Files Size (in bytes):	150332

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/451,680	Filing Date 08/05/2014	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 08/14/2014	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	x $80 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	x $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**0**

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DEBORAH POLLARD/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/451,680

APPLICATION AS FILED - PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
			TOTAL			TOTAL	1600

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

AMENDMENT A

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/451,680	08/05/2014	2812	1600	0756-10566	1	1

CONFIRMATION NO. 5776

31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

FILING RECEIPT

Date Mailed: 08/13/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Shunpei YAMAZAKI, Setagaya, JAPAN;
Kengo AKIMOTO, Atsugi, JAPAN;
Daisuke KAWAE, Yamato, JAPAN;

Applicant(s)

Semiconductor Energy Laboratory Co., Ltd., Atsugi-shi, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 31780

Domestic Priority data as claimed by applicant

This application is a CON of 13/763,874 02/11/2013 PAT 8803146
which is a CON of 12/613,769 11/06/2009 PAT 8373164
which is a CON of 12/606,262 10/27/2009 ABN

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
JAPAN 2008-287187 11/07/2008

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 08/13/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/451,680**

Projected Publication Date: 11/20/2014

Non-Publication Request: No

Early Publication Request: No
Title

SEMICONDUCTOR DEVICE

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

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PTO/AIA/15 (03-13)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	0756-10566
First Named Inventor	Shunpei YAMAZAKI et al.
Title	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

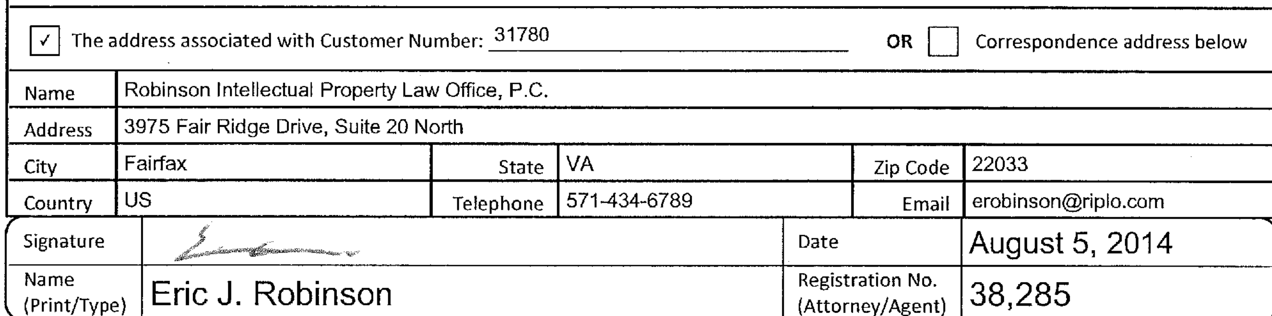
ADDRESS TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

1. ☐ **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. ☐ **Applicant asserts small entity status.** See 37 CFR 1.27
3. ☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. ☑ **Specification** [*Total Pages* 78]
   Both the claims and abstract must start on a new page.
   (See MPEP § 608.01(a) for information on the preferred arrangement)
5. ☑ **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 37]
6. **Inventor's Oath or Declaration** [*Total Pages* 6]
   (including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))
   a. ☐ Newly executed (original or copy)
   b. ☑ A copy from a prior application (37 CFR 1.63(d))
7. ☑ **Application Data Sheet** ** See note below.*
   See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R**
   in duplicate, large table, or Computer Program (*Appendix*)
   ☐ Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission**
   (*if applicable, items a. – c. are required*)
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PAPERS

10. ☐ **Assignment Papers** (cover sheet & document(s))
    Name of Assignee ____________
11. ☑ **37 CFR 3.73(c) Statement** *(when there is an assignee)* ☑ **Power of Attorney**
12. ☐ **English Translation Document** *(if applicable)*
13. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations attached
14. ☐ **Preliminary Amendment**
15. ☐ **Return Receipt Postcard** *(MPEP § 503) (Should be specifically itemized)*
16. ☐ **Certified Copy of Priority Document(s)** *(if foreign priority is claimed)*
17. ☐ **Nonpublication Request**
    Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. ☐ **Other:** ____________

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).



19. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 31780 **OR** ☐ Correspondence address below

Name	Robinson Intellectual Property Law Office, P.C.				
Address	3975 Fair Ridge Drive, Suite 20 North				
City	Fairfax	State	VA	Zip Code	22033
Country	US	Telephone	571-434-6789	Email	erobinson@riplo.com

Signature	[signature]	Date	August 5, 2014
Name (Print/Type)	Eric J. Robinson	Registration No. (Attorney/Agent)	38,285

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Semiconductor Energy Laboratory Co., Ltd.

Application No./Patent No.: ____________ Filed/Issue Date: August 5, 2014

Titled: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

Semiconductor Energy Laboratory Co., Ltd., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is ________%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 023662, Frame 0270, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: ____________ To: ____________

   The document was recorded in the United States Patent and Trademark Office at

   Reel ________, Frame ________, or for which a copy thereof is attached.

2. From: ____________ To: ____________

   The document was recorded in the United States Patent and Trademark Office at

   Reel ________, Frame ________, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: ______________________ To: ______________________

The document was recorded in the United States Patent and Trademark Office at

Reel __________, Frame __________, or for which a copy thereof is attached.

4. From: ______________________ To: ______________________

The document was recorded in the United States Patent and Trademark Office at

Reel __________, Frame __________, or for which a copy thereof is attached.

5. From: ______________________ To: ______________________

The document was recorded in the United States Patent and Trademark Office at

Reel __________, Frame __________, or for which a copy thereof is attached.

6. From: ______________________ To: ______________________

The document was recorded in the United States Patent and Trademark Office at

Reel __________, Frame __________, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

August 5, 2014

Date

Eric J. Robinson

Printed or Typed Name

Reg. No. 38,285

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☑ Practitioners associated with Customer Number: 31780

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications a ssigned only to the undersigned according to the USPTO assignment records or assignments docu ments attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 31780

OR

☐

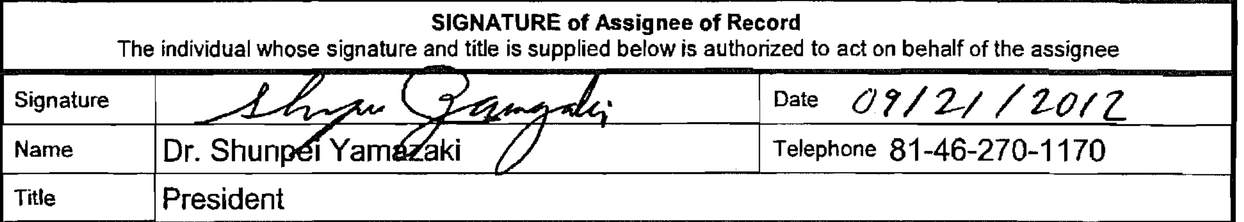
Firm or Individual Name			
Address			
City			
Country			
Telephone		Email	

Assignee Name and Address: SEMICONDUCTOR ENERGY LABORATORY CO., LTD.
398, HASE, ATSUGI-SHI
KANAGAWA-KEN 243-0036
JAPAN

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee



Signature	[signature]	Date	09/21/2012
Name	Dr. Shunpei Yamazaki	Telephone	81-46-270-1170
Title	President		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10566
	Application Number	

Title of Invention	SEMICONDUCTOR DEVICE

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove
Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shunpei		YAMAZAKI	

Residence Information (Select One) ◯ US Residency ◉ Non US Residency ◯ Active US Military Service

City	Setagaya	Country of Residence i	JP

Mailing Address of Inventor:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	State/Province	
Postal Code	243-0036	Country i	JP

Inventor 2 Remove
Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kengo		AKIMOTO	

Residence Information (Select One) ◯ US Residency ◉ Non US Residency ◯ Active US Military Service

City	Atsugi	Country of Residence i	JP

Mailing Address of Inventor:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	State/Province	
Postal Code	243-0036	Country i	JP

Inventor 3 Remove
Legal Name

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10566
	Application Number	

Title of Invention	SEMICONDUCTOR DEVICE

Prefix	Given Name	Middle Name	Family Name	Suffix
	Daisuke		KAWAE	

Residence Information (Select One) ◯ US Residency ◉ Non US Residency ◯ Active US Military Service

City	Yamato	Country of Residence i	JP

Mailing Address of Inventor:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country** i	JP

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	31780	
Email Address	erobinson@riplo.com	Add Email Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE		
Attorney Docket Number	0756-10566	**Small Entity Status Claimed** ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	37	**Suggested Figure for Publication (if any)**	

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country i

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10566
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE	

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	**Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	◯ US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	31780		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	13763874	2013-02-11

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13763874	Continuation of	12613769	2009-11-06	8373164	2013-02-12

Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12613769	Continuation of	12606262	2009-10-27

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10566
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) i the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country i	Filing Date (YYYY-MM-DD)	Access Code i (if applicable)
2008-287187	JP	2008-11-07	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10566
	Application Number	

Title of Invention	SEMICONDUCTOR DEVICE

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(●) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. [X]

Organization Name	Semiconductor Energy Laboratory Co., Ltd.

Mailing Address Information:

Address 1	398, Hase		
Address 2			
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Country i	JP	Postal Code	243-0036
Phone Number		Fax Number	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10566
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE	

Email Address	

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Eric J. Robinson/			Date (YYYY-MM-DD)	2014-08-05
First Name	Eric J.	Last Name	Robinson	Registration Number	38285

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-10566
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

発明の名称 Title of Invention	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

下記発明者である私は、つぎのことがらを宣誓します。
As the below named inventor, I hereby declare that:

本宣誓は
This declaration is directed to:

☐ 添付されている、あるいは
The attached application, or

■ 米国出願、あるいは____________に出願されたPCT国際願番号____________として出願されているものに宛てられています。
United States application or PCT international application number 13/763,874 filed on February 11, 2013, and amended on May 7, 2013.

上記の出願は私自身、あるいは私が権限を授与したものによって行われたものです。
The above-identified application was made or authorized to be made by me.

私は本出願書中にあらわれるもともとの発明者、あるいはもともとの共同発明者です。
I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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発明者の正式氏名
LEGAL NAME OF INVENTOR

発明者:
Inventor: Shunpei YAMAZAKI

日付(任意):
Date (Optional): 07/18/2013

署名:
Signature:

備考: 出願データシート(PTO/AIA/14 あるいはその同等用紙)は、発明の自主独立体全体の命名を含め、本用紙に添付すること。なお残余の発明者ごとに PTO/SB/AIA01 用紙を使用する。
Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

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プライバシー保護法声明書

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2. 本記録システムの記録は通常使用目的として、示談交渉手順における反対側弁護士への開示を含め、証拠の提示として法廷、予審判事、あるいは行政裁判所に開示される場合があります。
3. 本記録システム中の記録は通常使用目的として、記録に関する個人が該当する記録に関して、米国会議員に支援を要請する場合、個人の関与を要請する米国会議員に開示される場合があります。
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5. 特許協力条約のもとで出願された国際出願に関する本記録システム内の記録は、通常使用目的として、特許協力条約に基づき、世界知的所有権機関に開示される場合があります。
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

発明の名称 Title of Invention	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

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本宣誓は
This declaration is directed to:

☐ 添付されている、あるいは
The attached application, or

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発明者の正式氏名
LEGAL NAME OF INVENTOR

発明者:
Inventor: Kengo AKIMOTO

日付(任意):
Date (Optional): 07/22/2013

署名:
Signature: Kengo AKIMOTO

備考: 出願データシート(PTO/AIA/14 あるいはその同等用紙) は、発明の自主独立体全体の命名を含め、本用紙に添付すること。なお残余の発明者ごとに PTO/SB/AIA01 用紙を使用する。
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SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

[0001]

The present invention relates to a display device using an oxide semiconductor and a method for manufacturing the same.

2. Description of the Related Art

10 [0002]

As typically seen in liquid crystal display devices, a thin film transistor formed over a flat plate such as a glass substrate is manufactured using amorphous silicon or polycrystalline silicon. A thin film transistor manufactured using amorphous silicon has low field effect mobility, but can be formed over a larger glass substrate. In
15 contrast, a thin film transistor manufactured using crystalline silicon has high field effect mobility, but due to the necessity of a crystallization step such as laser annealing, such a transistor is not always suitable for being formed over a larger glass substrate.

[0003]

In view of the foregoing, attention has been drawn to a technique in which a
20 thin film transistor is manufactured using an oxide semiconductor and applied to electronic appliances or optical devices. For example, Patent Document 1 and Patent Document 2 disclose a technique in which a thin film transistor is manufactured using zinc oxide or an In-Ga-Zn-O-based oxide semiconductor for forming an oxide semiconductor film and such a transistor is used as a switching element or the like of an
25 image display device.

[0004]

Patent Document 1: Japanese Published Patent Application No. 2007-123861

Patent Document 2: Japanese Published Patent Application No. 2007-096055

30 ## SUMMARY OF THE INVENTION

[0005]

It is one object of the present invention to provide a structure by which

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electric-field concentration which might occur between a source electrode and a drain electrode in a bottom-gate thin film transistor is relaxed and deterioration of the switching characteristics is suppressed, and a manufacturing method thereof.

[0006]

5 Further, it is one object of the present invention to provide a structure by which coverage by an oxide semiconductor layer is improved and a manufacturing method thereof.

[0007]

In accordance with the present invention, a bottom-gate thin film transistor in
10 which an oxide semiconductor layer is provided over a source and drain electrodes is manufactured, and angle θ1 of the side surface of the source electrode which is in contact with the oxide semiconductor layer and angle θ2 of the side surface of the drain electrode which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the distance from the top edge to
15 the bottom edge in the side surface of each electrode is increased.

[0008]

One embodiment of the present invention disclosed in this specification is a semiconductor device wherein a gate electrode is formed over a substrate having an insulating surface, an insulating layer is formed over the gate electrode, a source and
20 drain electrodes are formed over the insulating layer, an oxide semiconductor layer is formed between their respective side surfaces of the source and drain electrodes, which face each other, so as to overlap with the gate electrode with the insulating layer interposed therebetween, and the angle formed between the surface of the substrate and the side surface of the source electrode and the angle formed between the surface of the
25 substrate and the side surface of the drain electrode are each greater than or equal to 20° and less than 90°.

[0009]

With the above embodiment, at least one of the objects can be achieved.

[0010]

30 A native oxide film is formed at least on the side surfaces of the source and drain electrodes, which depends on a metal material of the source and drain electrodes.

This native oxide film is formed by exposure to an atmosphere containing oxygen, such as the air, after etching for forming the source and drain electrodes. The native oxide film is also formed with oxygen contained in the atmosphere for deposition of the oxide semiconductor layer after etching for forming the source and drain electrodes.

5 [0011]

In order to prevent formation of the native oxide film on the electrodes, it is preferable that a buffer layer (also called an n^+ layer) is formed successively without exposure to the air on and in contact with a metal film formed by a sputtering method. This buffer layer is an oxide semiconductor layer which has lower resistance than the
10 oxide semiconductor layer which is formed thereover, and functions as a source and drain regions.

[0012]

In the above-described embodiment, the buffer layer is provided on the top surfaces of the source and drain electrodes and the oxide semiconductor layer is
15 provided on the buffer layer. The buffer layer (also called the n^+ layer) is formed successively without exposure to the air, which prevents a native oxide film from being formed on the top surfaces of the source and drain electrodes.

[0013]

Further, in the bottom-gate thin film transistor, the pathway of a drain current
20 (current pathway in the channel length direction) when the transistor is turned on by applying a voltage which is sufficiently higher than the threshold voltage to the gate electrode starts from the drain electrode and leads to the source electrode through the oxide semiconductor layer in the vicinity of the interface with the gate insulating film.

[0014]

25 Note that here the channel length of the bottom-gate thin film transistor in which the oxide semiconductor layer is provided over the source and drain electrodes corresponds to the shortest distance between the source and drain electrodes, and is the distance of the part of the oxide semiconductor layer in the vicinity of the interface with the gate insulating film, positioned between the source and drain electrodes.

30 [0015]

In the case where the n^+ layer is formed on and in contact with the top surface of each of the drain and source electrodes, when the conductivity of the native oxide

film formed on the side surface of each electrode is low, a main pathway of a drain current starts from the drain electrode and leads through the n^+ layer, a part of the oxide semiconductor layer in the vicinity of the interface with the side surface of the drain electrode, a part of the oxide semiconductor layer in the vicinity of the interface with the
5 gate insulating film, a part of the oxide semiconductor layer in the vicinity of the interface with the side surface of the source electrode, and the n^+ layer to the source electrode. As for the oxide semiconductor layer formed by a sputtering method, the film quality in the vicinity of the interface with a surface on which the film is formed tends to be affected by the material of the surface on which the film is formed. The
10 oxide semiconductor layer here has at least three interfaces with different materials: the interface with the n^+ layer, the interface with the side surface of each of the source and drain electrodes, and the interface with the gate insulating film. Therefore, in the oxide semiconductor layer, the interfacial state with the native oxide film on the side surface of the drain electrode is different from the interfacial state with the gate
15 insulating film, so that a part of the oxide semiconductor layer, which is in the vicinity of the interface with the side surface of the drain electrode functions as a first electric-field relaxation region. Similarly, in the oxide semiconductor layer, the interfacial state with the native oxide film on the side surface of the source electrode is different from the interfacial state with the gate insulating film, so that a part of the
20 oxide semiconductor layer, which is in the vicinity of the interface with the side surface of the source electrode functions as a second electric-field relaxation region.

[0016]

As described above, the regions of the oxide semiconductor layer, which overlap with the side surfaces of the source electrode and the drain electrode function as
25 electric-field relaxation regions.

[0017]

With an oxide semiconductor used in this specification, a thin film of a material described as $InMO_3(ZnO)_m$ ($m > 0$) is formed, and a thin film transistor in which the thin film is used as a semiconductor layer is manufactured. Note that M denotes a
30 single metal element or a plurality of metal elements selected from Ga, Fe, Ni, Mn, and Co. For example, M is Ga in some cases, and M includes another metal element in addition to Ga, such as either Ga and Ni or Ga and Fe, in some cases. Moreover, in the

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oxide semiconductor, in some cases, a transition metal element such as Fe or Ni or an oxide of the transition metal is contained as an impurity element in addition to the metal element contained as M. In this specification, this thin film is also referred to as an In-Ga-Zn-O-based non-single-crystal film.

5 [0018]

An amorphous structure is observed by X-ray diffraction (XRD), as the crystal structure of the In-Ga-Zn-O-based non-single-crystal film. Note that heat treatment is performed on the In-Ga-Zn-O non-single-crystal film to be observed at 200 to 500 °C, typically 300 to 400 °C, for 10 minutes to 100 minutes after the film deposition by a

10 sputtering method.

[0019]

The angle θ1 of the side surface of the source electrode which is in contact with the oxide semiconductor layer and the angle θ2 of the side surface of the drain electrode which is in contact with the oxide semiconductor layer are each set to be greater than or

15 equal to 20° and less than 90°, so that the distance from the top edge to the bottom edge of the electrode in the side surface of each electrode is increased, thereby increasing the lengths of the first and second electric-field relaxation regions to relax the electric-field concentration. Moreover, the distance from the top edge to the bottom edge of the electrode in the side surface of each electrode can also be increased by increasing the

20 thickness of the electrode.

[0020]

Further, in the case where the oxide semiconductor layer is formed by a sputtering method, if the side surface of the electrode is vertical to the substrate surface, the thickness of a part of the oxide semiconductor layer, which is formed on the side

25 surface of the electrode might be smaller than that of a part of the same, which is formed on the top surface of the electrode. Therefore, the angle θ1 of the side surface of the source electrode which is in contact with the oxide semiconductor layer and the angle θ2 of the side surface of the drain electrode which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so

30 that the thickness uniformity of the oxide semiconductor layer can be improved even over the side surface of each electrode and electric-field concentration can be relaxed.

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[0021]

Further, in the case where the straight line which connects the top edge of the side surface of the source electrode to the bottom edge of the side surface of the source electrode substantially coincides with the slope of the side surface of the source electrode as shown in FIG. 1, it can be said that the source electrode has a tapered shape, and the angle $\theta 1$ of the side surface of the source electrode with respect to the surface of the substrate can also be called a first taper angle. Similarly, in the case where the straight line which connects the top edge of the side surface of the drain electrode to the bottom edge of the side surface of the drain electrode substantially coincides with the slope of the slope of the side surface of the drain electrode, it can be said that the drain electrode has a tapered shape, and the angle $\theta 2$ of the side surface of the drain electrode with respect to the surface of the substrate can also be called a second taper angle.

[0022]

Further, the present invention is not limited to the shape in which the side surface of the electrode has only one angle, the side surface of the electrode may have a step as long as the angle $\theta 1$ of the side surface of the bottom edge of the source electrode and the angle $\theta 2$ of the side surface of the bottom edge of the drain electrode each are greater than or equal to 20° and less than 90°.

[0023]

Another embodiment of the present invention is a semiconductor device wherein a gate electrode is formed over a substrate having an insulating surface, an insulating layer is formed over the gate electrode, a source and drain electrodes are formed over the insulating layer, an oxide semiconductor layer is formed between their respective side surfaces of the source and drain electrodes, which face each other, so as to overlap with the gate electrode with the insulating layer interposed therebetween, and the angle formed between the surface of the substrate and the side surface of a bottom edge of the source electrode and the angle formed between the surface of the substrate and the side surface of a bottom edge of the drain electrode each are greater than or equal to 20° and less than 90°.

[0024]

In the above embodiment, the angle formed between the surface of the

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substrate and the side surface of the bottom edge of the source electrode is made to be different from the angle formed between the surface of the substrate and the side surface at a top edge of the source electrode. In addition, the angle formed between the surface of the substrate and the side surface of the bottom edge of the drain electrode is
5 made to be different from the angle formed between the surface of the substrate and the side surface at a top edge of the drain electrode. The cross section of the side surface of the source electrode and that of the side surface of the drain electrode, which face each other with the oxide semiconductor layer interposed therebetween, have substantially the same shape as each other because the same etching step is performed
10 thereon.

[0025]

For example, their respective angles of the side surfaces of the top edges of the source electrode and the drain electrode may be set to 90° so that their respective angles of the side surfaces of the bottom edges of the source electrode and the drain electrode
15 are different from their respective angles of the side surfaces of the top edges of the source electrode and the drain electrode. By increasing their respective angles of the side surfaces of the top edges of the source electrode and the drain electrode to be greater than their respective angles of the side surfaces of the bottom edges of the source electrode and the drain electrodes, the interval between masks for forming the
20 source and drain electrodes can be designed to be small, which can result in shorter design of the channel length, for example, a channel length of 1 to 10 μm.

[0026]

The side surface of each of the source and drain electrodes may have a curved surface; for example, in the cross-sectional shape of each of the source and drain
25 electrodes, the bottom edge portion of the electrode may have one curved surface at least partly which originates from a center of a curvature radius, which is positioned outside the electrode. The side surface of each of the source and drain electrodes may have a cross-sectional shape which spreads toward the substrate from the top surface of each electrode.
30 [0027]

The electrodes, which can have various cross-sectional shapes as described

above, are formed by dry etching or wet etching. As an etching apparatus used for the dry etching, an etching apparatus using a reactive ion etching method (an RIE method), or a dry etching apparatus using a high-density plasma source such as ECR (electron cyclotron resonance) or ICP (inductively coupled plasma) can be used. As a dry
5 etching apparatus by which uniform electric discharge can be obtained over a wider area as compared to an ICP etching apparatus, there is an ECCP (enhanced capacitively coupled plasma) mode apparatus in which an upper electrode is grounded, a high-frequency power source at 13.56 MHz is connected to a lower electrode, and further a low-frequency power source at 3.2 MHz is connected to the lower electrode.
10 This ECCP mode etching apparatus can be applied even when, as the substrate, a substrate, the size of which exceeds 3 m of the tenth generation, is used, for example.

[0028]

Each of the source and drain electrodes may be a single layer or a stacked layer of at least two layers formed using two different materials.

15 [0029]

Another embodiment of the present invention, which relates to the manufacturing method to realize the above structure, is a method for manufacturing a semiconductor device, wherein a gate electrode is formed over a substrate having an insulating surface, a gate insulating layer is formed to cover the gate electrode, a
20 conductive layer and a buffer layer are formed to be stacked over the gate insulating layer without exposure to the air, the conductive layer and the buffer layer are selectively etched to form a source and drain electrodes each having a side surface which forms an angle greater than or equal to 20° and less than 90° with respect to the surface of the substrate, and an oxide semiconductor layer is formed over the gate
25 insulating layer, the source electrode, and the drain electrode.

[0030]

In the above-described embodiment which relates to the manufacturing method, the buffer layer contains indium, gallium, and zinc, and can be used using the same target as a target used for the oxide semiconductor layer formed over the buffer layer.
30 The buffer layer and the oxide semiconductor layer can be separately formed by changing the film deposition atmosphere, and the manufacturing cost can be decreased by using the same target.

[0031]

According to the above-described embodiment which relates to the manufacturing method, the conductive layer and the buffer layer are formed to be stacked over the gate insulating layer without exposure to the air, that is, successive film deposition is performed.

[0032]

In the above-described embodiment which relates to the manufacturing method, the conductive layer, which forms the source and drain electrodes, is formed using a metal material such as aluminum, tungsten, chromium, tantalum, titanium, or molybdenum, or an alloy material thereof. The conductive layer may be a stacked layer of at least two layers; for example, a stacked layer in which an aluminum layer as a bottom layer and a titanium layer as an upper layer are stacked, a stacked layer in which a tungsten layer as a bottom layer and a molybdenum layer as an upper layer are stacked, a stacked layer in which an aluminum layer as a bottom layer and a molybdenum layer as an upper layer are stacked, or the like can be used.

[0033]

Successive film deposition in this specification means that a series of steps from a first film deposition step by a sputtering method to a second film deposition step by a sputtering method are performed by controlling an atmosphere in which a process substrate is disposed so that it is constantly in vacuum or an inert gas atmosphere (a nitrogen atmosphere or a rare gas atmosphere) without being exposed to a contaminated atmosphere such as the air. By the successive film deposition, film deposition can be performed on the process substrate which has been cleaned, without further adhesion of moisture or the like.

[0034]

Performing the series of steps from the first deposition step to the second deposition step in the same chamber is within the scope of the successive film deposition in this specification.

[0035]

In addition, the following is also within the scope of the successive film deposition in this specification: in the case of performing the series of steps from the first film deposition step to the second film deposition step in different chambers, the

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process substrate is transferred to another chamber without being exposed to the air after the first film deposition step and subjected to the second film deposition.

[0036]

Further, the following is also within the scope of the successive film deposition in this specification: a substrate transfer step, an alignment step, a slow-cooling step, a step of heating or cooling the substrate to a temperature which is necessary for the second film deposition step, or the like is provided between the first film deposition step and the second film deposition step.

[0037]

However, the case in which a step in which liquid is used, such as a cleaning step, wet etching, or resist formation, is provided between the first film deposition step and the second film deposition step is not within the scope of the successive film deposition in this specification.

[0038]

In this specification, a word which expresses a direction, such as "over", "below", "side", "horizontal", or "vertical", indicates a direction based on the substrate surface in the case where a device is provided over the surface of the substrate.

[0039]

Note that the ordinal numerals such as "first" and "second" in this specification are used for convenience and do not denote the order of steps or the stacking order of layers. In addition, the ordinal numbers in this specification do not denote particular names which specify the present invention.

[0040]

The angle formed by the surface of the substrate and the side surface of the source electrode and the angle formed by the surface of the substrate and the side surface of the drain electrode are adjusted, so that the coverage by the oxide semiconductor layer provided over the source and drain electrodes is improved.

[0041]

An electric-field relaxation region is provided, so that electric-field concentration which might occur between the source and drain electrodes is relaxed and degradation of the switching characteristics of the thin film transistor is suppressed.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0042]

FIG. 1 is a cross-sectional view showing one example of a semiconductor device.

5 FIG. 2 is a cross-sectional view showing one example of a semiconductor device.

FIGS. 3A and 3B are cross-sectional views showing one example of a method for manufacturing a semiconductor device.

FIGS. 4A to 4C are cross-sectional views showing one example of a method
10 for manufacturing a semiconductor device.

FIG. 5 is a top view showing one example of a method for manufacturing a semiconductor device.

FIG. 6 is a top view showing one example of a method for manufacturing a semiconductor device.

15 FIG. 7 is a top view showing one example of a method for manufacturing a semiconductor device.

FIG. 8 is a top view showing one example of a method for manufacturing a semiconductor device.

FIGS. 9A1 and 9B1 are views showing one example of a cross-sectional view
20 of a terminal portion and FIGS. 9A2 and 9B2 are views showing one example of a top view of the terminal portion.

FIG. 10 is a top view showing one example of a method for manufacturing a semiconductor device.

FIG. 11 is a cross-sectional view showing one example of a semiconductor
25 device.

FIGS. 12 A and 12B are views showing examples of a block diagram of semiconductor device.

FIG. 13 is a diagram showing one example of a structure of a signal line driver circuit.

30 FIG. 14 is a timing chart showing an operation of a signal line driver circuit.

FIG. 15 is a timing chart showing one example of an operation of a signal line driver circuit.

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FIG. 16 is a diagram showing one example of a structure of a shift register.

FIG. 17 is a diagram showing a connection structure of the flip-flop shown in FIG. 16.

FIG. 18 is a diagram showing one example of a pixel equivalent circuit of a
5 semiconductor device.

FIGS. 19A to 19C are cross-sectional views showing examples of a semiconductor device.

FIG. 20A1 and 20A2 are top views showing examples of a semiconductor device, and FIG. 20B is a cross-sectional view showing one example of a semiconductor
10 device.

FIG. 21 is a cross-sectional view showing one example of a semiconductor device.

FIGS. 22A and 22B are a top view and a cross-sectional view showing one example of a semiconductor device.

15 FIGS. 23A and 23B are views showing examples of a usage pattern of electronic paper.

FIG. 24 is an external view of one example of an electronic book reader.

FIGS. 25A and 25B are external views showing respective examples of a television device and a digital photo frame.

20 FIGS. 26A and 26B are external views showing examples of an amusement machine.

FIG. 27 is an external view showing one example of a mobile phone.

FIG. 28 is a graph showing one example of electrical characteristics of a thin film transistor.

25 FIG. 29 is a top view of a thin film transistor manufactured to measure the electrical characteristics.

FIGS. 30A to 30C are cross-sectional views showing a process for manufacturing a sample.

FIGS. 31A and 31B are a photograph and a cross-sectional view showing a part
30 of the cross-section of a sample.

FIG. 32A is a view showing one example of a cross-sectional structure of a semiconductor device, FIG. 32B is an equivalent circuit diagram thereof, and FIG. 32C

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is a top view thereof.

FIGS. 33A to 33C are cross-sectional views showing structures of a calculation model.

FIG. 34 is a graph showing calculation results.

5 FIG. 35 is a graph showing calculation results.

FIG. 36 is a graph showing calculation results.

FIGS. 37A and 37B are graphs showing calculation results (comparative examples).

10 DETAILED DESCRIPTION OF THE INVENTION

[0043]

Embodiments and examples of the present invention will be hereinafter described.

[Embodiment 1]

15 [0044]

The case in which a thin film transistor 170 is provided over a substrate is illustrated in FIG. 1. FIG. 1 is one example of a cross-sectional view of a thin film transistor.

[0045]

20 A gate electrode 101 provided over a substrate 100 having an insulating surface is covered with a gate insulating layer 102, and a first wiring and a second wiring are provided over the gate insulating layer 102 which overlaps with the gate electrode 101. A buffer layer is provided over each of the first wiring and the second wiring which function as a source electrode layer 105a and a drain electrode layer 105b. A first 25 buffer layer 104a is provided over the source electrode layer 105a, and a second buffer layer 104b is provided over the drain electrode layer 105b. An oxide semiconductor layer 103 is provided over the first buffer layer 104a and the second buffer layer 104b.

[0046]

In FIG. 1, as the substrate 100 having a light-transmitting property, a glass 30 substrate of barium borosilicate glass, aluminoborosilicate glass, or the like typified by 7059 glass, 1737 glass, or the like manufactured by Corning, Inc. can be used.

[0047]

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The gate electrode 101 is a single layer or a stacked layer made of different metal materials. As a material of the gate electrode 101, a metal material (an element selected from aluminum (Al), copper (Cu), titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc), or an alloy
5 including the element as a component) is used. The angle of the side surface of the gate electrode 101 is set to be greater than or equal to 20° and less than 90°. The gate electrode 101 is formed by etching so as to have a tapered shape at least in the edge portion thereof.

[0048]

10 The gate insulating layer 102 may be formed to have a single-layer structure or a stacked-layer structure using an insulating film obtained by a sputtering method or a plasma CVD method, such as a silicon oxide film, a silicon oxynitride film, a silicon nitride film, an aluminum oxide film, or a tantalum oxide film. It is preferable to select a material which can provide an etching selectivity which is high enough for the
15 etching for forming the source electrode layer 105a and the drain electrode layer 105b which are formed over the gate insulating layer 102. In etching the source electrode layer 105a and the drain electrode layer 105b, the surface of the gate insulating layer 102 may be etched off by about 20 nm at a maximum; and it is preferable to etch off the superficial layer of the gate insulating layer 102 by a small thickness in order to remove
20 an etching residue of the metal material.

[0049]

The source electrode layer 105a and the drain electrode layer 105b each are a single layer or a stacked layer made of different metal materials. As a material of each of the source electrode layer 105a and the drain electrode layer 105b, a metal material
25 (an element selected from aluminum (Al), copper (Cu), titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc), or an alloy including the element as a component) is used.

[0050]

With respect to the cross-sectional shape of the source electrode layer 105a, as
30 shown in FIG. 1, angle $\theta 1$ formed between the surface of the substrate and the side surface of the source electrode layer 105a is set to be greater than or equal to 20° and

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less than 90°. Similarly, with respect to the cross-sectional shape of the drain electrode layer 105b, as shown in FIG. 1, angle θ2 formed between the surface of the substrate and the side surface of the drain electrode layer 105b is set to be greater than or equal to 20° and less than 90°. The angle θ1 and the angle θ2 are substantially the same as
5 each other because the same etching step (dry etching or wet etching) is performed thereon. The angle θ1 of the side surface of the source electrode layer 105a which is in contact with the oxide semiconductor layer and the angle θ2 of the side surface of the drain electrode layer 105b which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the distance from
10 the top edge to the bottom edge in the side surface of each of the source electrode layer 105a and the drain electrode layer 105b is increased.

[0051]

Although the angles θ1 and θ2 are described when it is assumed that the plane of the back surface of the substrate is the substrate surface in FIG. 1, the present
15 invention is not limited thereto, and the angles θ1 and θ2 are not changed even when it is assumed that the plane of the front surface of the substrate is the substrate surface because the plane of the back surface of the substrate is in parallel to the plane of the front surface of the substrate.

[0052]

20 The oxide semiconductor layer 103 is formed over the source electrode layer 105a and the drain electrode layer 105b having the above-described shapes. The oxide semiconductor layer 103 is formed as follows: film deposition is performed using an oxide semiconductor target including In, Ga, and Zn (In_2O_3:Ga_2O_3:ZnO = 1:1:1), under a condition in which the distance between the substrate and the target is 170 mm, the
25 pressure is 0.4 Pa, and the direct-current (DC) power source is 0.5 kW, in an argon atmosphere containing oxygen, and a resist mask is formed and the deposited film is selectively etched off to remove the unnecessary portion thereof. Note that it is preferable to use a pulsed direct-current (DC) power source with which dust can be reduced and thickness distribution can be evened. The thickness of the oxide
30 semiconductor film is set to be 5 to 200 nm. In this embodiment, the thickness of the oxide semiconductor film is 100 nm.

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[0053]

It is preferable to provide the first buffer layer 104a between the source electrode layer 105a and the oxide semiconductor layer 103. It is preferable to provide the second buffer layer 104b between the drain electrode layer 105b and the oxide semiconductor layer 103.

[0054]

The first buffer layer 104a and the second buffer layer 104b each are an oxide semiconductor layer (n^+ layer) which have lower resistance than the oxide semiconductor layer 103, and function as a source and drain regions.

[0055]

In this embodiment, the n^+ layers are each formed as follows: film deposition is performed by a sputtering method using a target in which In_2O_3:Ga_2O_3:ZnO = 1:1:1, under a condition in which the pressure is 0.4 Pa, the power is 500 W, the deposition temperature is room temperature, and the argon-gas flow rate is 40 sccm. Despite the use of the target in which In_2O_3:Ga_2O_3:ZnO = 1:1:1, an In-Ga-Zn-O-based non-single-crystal film including crystal grains with a size of 1 to 10 nm may be formed immediately after the start of the film deposition. Note that it can be said that the presence or absence of crystal grains or the density of crystal grains can be adjusted and the diameter size can be adjusted within the range of 1 to 10 nm by appropriate adjustment of the composition ratio in the target, the film deposition pressure (0.1 to 2.0 Pa), the power (250 to 3000 W: 8 inches ø), the temperature (room temperature to 100 °C), the reactive sputtering deposition conditions, and/or the like. The second In-Ga-Zn-O-based non-single-crystal film has a thickness of 5 to 20 nm. Needless to say, when the film includes crystal grains, the size of each crystal grain does not exceed the thickness of the film. In this embodiment, the thickness of the second In-Ga-Zn-O-based non-single-crystal film is 5 nm.

[0056]

By forming and stacking the conductive film which forms the source electrode layer 105a and the drain electrode layer 105b and the oxide semiconductor film which forms the n^+ layers without exposing to the air, by a sputtering method, the source and drain electrode layers can be prevented from being exposed to the air during the manufacturing process, so that dust can be prevented from attaching thereto.

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[0057]

As for the oxide semiconductor layer 103 formed by a sputtering method, the film quality in the vicinity of the interface with a surface on which the film is formed tends to be affected by the material of the surface on which the film is formed. The oxide semiconductor layer here has at least three interfaces with different materials: the interface with the n^+ layer, the interface with the side surface of each of the source and drain electrodes, and the interface with the gate insulating film. Therefore, in the oxide semiconductor layer 103, the interfacial state with the native oxide film on the side surface of the drain electrode layer is different from the interfacial state with the gate insulating film, so that a part of the oxide semiconductor layer, which is in the vicinity of the interface with the side surface of the drain electrode layer functions as the first electric-field relaxation region 106a. Similarly, in the oxide semiconductor layer, the interfacial state with the native oxide film on the side surface of the source electrode is different from the interfacial state with the gate insulating film, so that a part of the oxide semiconductor layer, which is in the interface vicinity with the side surface of the source electrode functions as the second electric-field relaxation region 106b. The angle θ1 of the side surface of the source electrode which is in contact with the oxide semiconductor layer and the angle θ2 of the side surface of the drain electrode which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the distance from the top edge to the bottom edge of the electrode in the side surface of each electrode is increased, thereby increasing length L1 of the first electric-field relaxation region 106a and length L2 of the second electric-field relaxation region 106b to relax the electric-field concentration. The distance from the top edge to the bottom edge of the electrode in the side surface of each electrode can also be increased by increasing the thickness of the electrode.

[0058]

Further, in the case where the oxide semiconductor layer 103 is formed by a sputtering method, if the side surface of the electrode is vertical to the substrate surface, the thickness of a part of the oxide semiconductor layer 103, which is formed on the side surface of the electrode might be smaller than that of a part of the same, which is formed on the top surface of the electrode. Therefore, the angle θ1 of the side surface

of the source electrode which is in contact with the oxide semiconductor layer and the angle θ2 of the side surface of the drain electrode which is in contact with the oxide semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the thickness uniformity of the oxide semiconductor layer can be improved even over the side surface of each electrode, a partial reduction in the thickness of the oxide semiconductor layer 103 can be suppressed, and electric-field concentration can be relaxed.

[Embodiment 2]

[0059]

The case where the straight line which connects the top edge of the side surface of the source electrode layer (or the drain electrode layer) to the bottom edge of the side surface of the source electrode layer (or the drain electrode layer) substantially coincides with the slope of the side surface of the source electrode layer (or the drain electrode layer) is illustrated in FIG. 1. In Embodiment 2, the case where the side surface of a source electrode layer (or a drain electrode layer) has a step will be described using FIG. 2. The side surface of the electrode may have a step as long as angle θ1 of the side surface of the bottom edge of the source electrode layer and angle θ2 of the side surface of the bottom edge of the drain electrode layer each are greater than or equal to 20° and less than 90°. Note that, in FIG. 2, the same reference numerals are used for the portions that are common to those in FIG. 1.

[0060]

A gate electrode 101 provided over a substrate 100 having an insulating surface is covered with a gate insulating layer 102, and a first wiring and a second wiring are provided over the gate insulating layer 102 which overlaps with the gate electrode 101. A buffer layer is provided over each of the first wiring and the second wiring which function as a source electrode layer 405a and a drain electrode layer 405b. A first buffer layer 404a is provided over the source electrode 405a, and a second buffer layer 404b is provided over the drain electrode layer 405b. An oxide semiconductor layer 403 is provided over the first buffer layer 404a and the second buffer layer 404b.

[0061]

The substrate 100 having an insulating surface, the gate electrode 101, and the

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gate insulating layer 102 are the same as in Embodiment 1, and specific description thereof is omitted in this embodiment.

[0062]

The source electrode layer 405a and the drain electrode layer 405b each are a single layer or a stacked layer made of different metal materials. As a material of each of the source electrode layer 405a and the drain electrode layer 405b, a metal material (an element selected from aluminum (Al), copper (Cu), titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc), or an alloy including the element as a component) is used.

[0063]

Described in this embodiment is the case where a single layer of a tungsten film with a thickness of 100 nm is used as the source electrode layer 405a and the drain electrode layer 405b, and the side surface shapes of the source electrode layer 405a and the drain electrode layer 405b shown in FIG. 2 are formed by using an ICP etching apparatus using a coiled antenna.

[0064]

In this embodiment, etching is performed by generating plasma under the following condition: the gas flow rate of CF_4 is 25 sccm, the gas flow rate of Cl_3 is 25 sccm, the gas flow rate of O_2 is 10 sccm, and an RF (13.56 MHz) power of 500 W is applied to a coiled electrode at a pressure of 1.5 Pa. An RF (13.56 MHz) power of 10 W is applied to the substrate side (sample stage), which means that a negative self-bias voltage is substantially applied thereto. This etching is stopped when at least the gate insulating film 102 is exposed to some extent, thereby forming the side surface of the electrode, which has a step.

[0065]

By the above etching condition, with respect to the cross-sectional shape of the source electrode layer 405a, the angle θ1 formed between the surface of the substrate and the bottom edge of the side surface of the source electrode layer 405a can be made to be greater than or equal to 20° and less than 90°; and as shown in FIG. 2, θ1 is about 40°. Further, the angle formed between the surface of the substrate and the top edge of the side surface of the source electrode layer 405a is about 90°. The cross section of

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the side surface of the source electrode layer 405a and that of the side surface of the drain electrode layer 405b, which face each other with the oxide semiconductor layer 403 interposed therebetween, have substantially the same shape as each other because the same etching step is performed thereon.

5 [0066]

By increasing their respective angles of the side surfaces of the top edges of the source electrode layer 405a and the drain electrode layer 405b to be greater than their respective angles of the side surfaces of the bottom edges of the source electrode layer 405a and the drain electrode layer 405b, the interval between masks for forming the 10 source and drain electrode layers 405a and 405b can be designed to be small, which can result in shorter design of the channel length, for example, a channel length of 1 to 10 μm.

[0067]

The present invention is not limited to the above-described method, and a step 15 can also be formed in the side surface of each electrode by the following: materials having different etching rates of an etching gas, which form the source electrode layer 405a and the drain electrode layer 405b, are stacked such that a material layer having a low etching rate and a material layer having a high etching rate are stacked as a lower layer and an upper layer respectively, and etching is performed thereon.

20 [0068]

The two side surfaces of the electrodes which face each other with the oxide semiconductor layer 403 interposed therebetween each have a step, so that the distance from the top edge to the bottom edge of the electrode in the side surface of each electrode is increased, thereby increasing length L3 of a first electric-field relaxation 25 region 406a and length L4 of a second electric-field relaxation region to relax the electric-field concentration.

[0069]

In order to further increase the distance from the top edge to the bottom edge of the electrode in the side surface of each of the source electrode layer and the drain 30 electrode layer, wet etching may be performed after the above-described dry etching to provide a curved surface partly for the side surfaces of the electrodes which face each other with the oxide semiconductor layer 403 interposed therebetween.

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[0070]

Alternatively, instead of the above-described dry etching, the source electrode layer and the drain electrode layer may be formed by wet etching so that the angle $\theta 1$ of the side surface of the bottom edge of the source electrode layer and the angle $\theta 2$ of the side surface of the bottom edge of the drain electrode layer each are greater than or equal to 20° and less than 90°. The side surface of each of the source and drain electrode layers may have a cross-sectional shape which spreads toward the substrate from the top surface of each electrode layer.

[0071]

This embodiment can be combined with Embodiment 1, as appropriate.

[Embodiment 3]

[0072]

In this embodiment, a thin film transistor and a manufacturing process thereof are described with reference to FIGS. 3A and 3B, 4A to 4C, 5 to 8, and FIGS. 9A1 and 9A2 and 9B1 and 9B2.

[0073]

In FIG. 3A, as a substrate 100 having a light-transmitting property, a glass substrate of barium borosilicate glass, aluminoborosilicate glass, or the like can be used.

[0074]

Then, a conductive layer is formed over the entire surface of the substrate 100, a first photolithography step is performed to form a resist mask, and an unnecessary portion is removed by etching to form wirings and an electrode (a gate wiring including a gate electrode 101, a capacitor wiring 108, and a first terminal 121). At this time, the etching is performed so that at least the edge portion of the gate electrode 101 is tapered. FIG. 3A is a cross-sectional view at this stage. A top view at this stage corresponds to FIG. 5.

[0075]

The gate wiring including the gate electrode 101, the capacitor wiring 108, and the first terminal 121 in a terminal portion are each formed using an element selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), aluminum (Al), and copper (Cu), or an alloy including the element as

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a component, an alloy film in which the elements are combined, or a nitride including the element as a component. Among these, it is preferable to use a low-resistance conductive material such as aluminum (Al) or copper (Cu), but however, since aluminum itself has disadvantages such as low heat resistance and a tendency to be
5 corroded, the following is used to form them: an element selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), and neodymium (Nd), aluminum (Al), and copper (Cu), an alloy film including a combination of any or all of these elements, or a nitride including the element as a component.

[0076]

10 Then, a gate insulating layer 102 is formed entirely over the gate electrode 101. The gate insulating layer 102 is formed with a thickness of 50 to 250 nm by a sputtering method or the like.

[0077]

For example, as the gate insulating layer 102, a 100-nm-thick silicon oxide film
15 is formed by a sputtering method. The gate insulating layer 102 is not limited to such a silicon oxide film and may be a single layer or a stacked layer using another insulating film such as a silicon oxynitride film, a silicon nitride film, an aluminum oxide film, or a tantalum oxide film.

[0078]

20 Next, a conductive film is formed using a metal material over the gate insulating layer 102 by a sputtering method or a vacuum evaporation method. As the material of the conductive film, there are an element selected from Al, Cr, Ta, Ti, Mo, and W, an alloy including any of these elements as a component, an alloy film including a combination of any or all of these elements, and the like. In this embodiment, the
25 conductive film is formed by stacking an aluminum (Al) film and a titanium (Ti) film in this order. Alternatively, the conductive film may have a three-layer structure in which a titanium film is stacked over a tungsten film. Further alternatively, the conductive film may have a single-layer structure of a titanium film or an aluminum film including silicon.

30 [0079]

Next, a first oxide semiconductor film (a first In-Ga-Zn-O-based non-single-crystal film) is formed over the conductive film by a sputtering method. In

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this embodiment, the first oxide semiconductor film is formed as follows: film deposition is performed by a sputtering method using a target in which In_2O_3:Ga_2O_3:ZnO = 1:1:1, under a condition in which the pressure is 0.4 Pa, the power is 500 W, the deposition temperature is room temperature, and the argon-gas flow rate is
5 40 sccm. Despite the use of the target in which In_2O_3:Ga_2O_3:ZnO = 1:1:1, an In-Ga-Zn-O-based non-single-crystal film including crystal grains with a size of 1 to 10 nm may be formed immediately after the start of the film deposition. Note that it can be said that the presence or absence of crystal grains or the density of crystal grains can be adjusted and the diameter size can be adjusted within the range of 1 to 10 nm by
10 appropriate adjustment of the composition ratio in the target, the film deposition pressure (0.1 to 2.0 Pa), the power (250 to 3000 W: 8 inches ø), the temperature (room temperature to 100 °C), the reactive sputtering deposition conditions, and/or the like. The first In-Ga-Zn-O-based non-single-crystal film has a thickness of 5 to 20 nm. Needless to say, when the film includes crystal grains, the size of the crystal grains does
15 not exceed the thickness of the film. In this embodiment, the thickness of the first In-Ga-Zn-O-based non-single-crystal film is 5 nm.

[0080]

Next, a second photolithography step is performed to form a resist mask, and the first In-Ga-Zn-O-based non-single-crystal film is etched. In this embodiment, wet
20 etching using ITO07N (manufactured by Kanto Chemical Co., Inc.) is performed to remove an unnecessary portion in a pixel portion, so that first In-Ga-Zn-O-based non-single-crystal films 111a and 111b are formed. The etching here is not limited to wet etching and may be dry etching.

[0081]

25 Next, with use of the same resist mask as used for the etching of the first In-Ga-Zn-O-based non-single-crystal film, an unnecessary portion is removed by etching to form a source electrode layer 105a and a drain electrode layer 105b. Wet etching or dry etching is used as the etching method at this time. Here, dry etching using a mixed gas of $SiCl_4$, Cl_2, and BCl_3 is performed to etch the conductive film in
30 which the Al film and the Ti film are stacked, so that a source electrode layer 105a and a drain electrode layer 105b are formed. The cross-section at this stage is illustrated in FIG. 3B. FIG. 6 is a top view at this stage.

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[0082]

By this etching, angle θ1 of the side surface of the source electrode layer 105a and angle θ2 of the side surface of the drain electrode layer 105b which are in contact with an oxide semiconductor layer formed later are made to be greater than or equal to 5 20° and less than 90°. Tapered shapes of the side surfaces of the electrodes which face each other with the oxide semiconductor layer interposed therebetween enable respective regions of the oxide semiconductor layer, which overlap with the side surfaces of the source electrode layer and the drain electrode layer to function as electric-field relaxation regions.

10 [0083]

In the second photolithography process, a second terminal 122 formed using the same material as the material of the source electrode layer 105a and the drain electrode layer 105b remains in a terminal portion. Note that the second terminal 122 is electrically connected to a source wiring (a source wiring including the source 15 electrode layer 105a). In the terminal portion, a first In-Ga-Zn-O-based non-single-crystal film 123 remains over the second terminal 122 to overlap with the second terminal 122.

[0084]

In a capacitor portion, a capacitor electrode layer 124 which is made from the 20 same material as the material of the source electrode layer 105a and the drain electrode layer 105b remains. In addition, in the capacitor portion, a first In-Ga-Zn-O-based non-single-crystal film 111c remains over the capacitor electrode layer 124 to overlap with capacitor electrode layer 124.

[0085]

25 Next, the resist mask is removed, and then, a second oxide semiconductor film (a second In-Ga-Zn-O-based non-single-crystal film in this embodiment) formed without exposure to the air. Formation of the second In-Ga-Zn-O-based non-single-crystal film without exposure to the air after the plasma treatment is effective in preventing dust and the like from attaching to the interface between the gate 30 insulating layer and the semiconductor film. In this embodiment, the second In-Ga-Zn-O-based non-single-crystal film is formed in an argon or oxygen atmosphere

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using an oxide semiconductor target having a diameter of 8 inches and containing In, Ga, and Zn (In_2O_3:Ga_2O_3:ZnO = 1:1:1), with the distance between the substrate and the target set to 170 mm, under a pressure of 0.4 Pa, and with a direct-current (DC) power source of 0.5 kW. Note that it is preferable to use a pulsed direct-current (DC) power
5 source with which dust can be reduced and thickness distribution can be evened. The second In-Ga-Zn-O-based non-single-crystal film is formed to have a thickness of 5 to 200 nm. In this embodiment, the thickness of the second In-Ga-Zn-O-based non-single-crystal film is 100 nm.

[0086]

10 The film deposition condition of the second In-Ga-Zn-O-based non-single-crystal film is different from that of the first In-Ga-Zn-O-based non-single-crystal film, thereby forming the second In-Ga-Zn-O-based non-single-crystal film to have a higher electrical resistance than the first In-Ga-Zn-O-based non-single-crystal film. For example, the second
15 In-Ga-Zn-O-based non-single-crystal film is formed under a condition where the ratio of an oxygen gas flow rate to argon gas flow rate is higher than the ratio of an oxygen gas flow rate to an argon gas flow rate under the deposition condition of the first In-Ga-Zn-O-based non-single-crystal film. Specifically, the first In-Ga-Zn-O-based non-single-crystal film is formed in a rare gas (e.g., argon or helium) atmosphere (or an
20 atmosphere, less than or equal to 10 % of which is an oxygen gas and greater than or equal to 90 % of which is an argon gas), and the second In-Ga-Zn-O-based non-single-crystal film is formed in an oxygen atmosphere (or an atmosphere in which the ratio of an oxygen gas flow rate to an argon gas flow rate is 1:1 or higher).

[0087]

25 Then, heat treatment is preferably performed at 200 to 600 °C, typically, 300 to 500 °C. In this embodiment, heat treatment is performed under a nitrogen atmosphere or the air in a furnace at 350 °C for 1 hour. Through this heat treatment, rearrangement at the atomic level occurs in the In-Ga-Zn-O-based non-single-crystal film. Because strain energy which inhibits carrier movement is released by the heat treatment, the heat
30 treatment (including optical annealing) is important. There is no particular limitation on the timing of heat treatment as long as it is performed after formation of the second

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In-Ga-Zn-O-based non-single-crystal film, and for example, heat treatment may be performed after formation of a pixel electrode.

[0088]

Next, a third photolithography process is performed to form a resist mask, and an unnecessary portion is removed by etching, so that a semiconductor layer 103 is formed. In this embodiment, wet etching using ITO07N (manufactured by Kanto Chemical Co., Inc.) is performed to remove the second In-Ga-Zn-O-based non-single-crystal film, so that the semiconductor layer 103 is formed. In the case of the removal by wet etching, an oxide semiconductor can be reproduced using a waste solution of the etching to use for manufacturing a target again.

[0089]

Indium or gallium contained in an oxide semiconductor, which is known as a rare metal, can achieve resource saving and cost reduction of a product formed using an oxide semiconductor by recycle of it.

[0090]

The same etchant is used for the first In-Ga-Zn-O-based non-single-crystal film and the second In-Ga-Zn-O-based non-single-crystal film, and therefore, the first In-Ga-Zn-O-based non-single-crystal film is removed by this etching. Therefore, a side surface of the first In-Ga-Zn-O-based non-single-crystal film, which is covered with the second In-Ga-Zn-O-based non-single-crystal film is protected whereas parts of the first In-Ga-Zn-O-based non-single-crystal films 111a and 111b, which are exposed to the outside are etched, so that a first buffer layer 104a and a second buffer layer 104b are formed. The etching of the semiconductor layer 103 is not limited to wet etching and may be dry etching. Through the above steps, a thin film transistor 170 including the semiconductor layer 103 as a channel formation region can be manufactured. A cross-sectional view at this stage is FIG. 4A. A top view at this stage is FIG. 7.

[0091]

Next, the resist mask is removed, and a protective insulating film 107 is formed to cover the semiconductor layer. The protective insulating film 107 can be formed using a silicon nitride film, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, a tantalum oxide film, or the like by a sputtering method or the like.

[0092]

Then, a fourth photolithography step is performed to form a resist mask, so that the protective insulating film 107 is etched to form a contact hole 125 reaching the drain electrode layer 105b. In addition, a contact hole 127 reaching the second terminal 122 is also formed in the same etching step. In addition, a contact hole 109 reaching the capacitor electrode layer 124 is also formed in the same etching step. In order to reduce the number of masks, the gate insulating layer is preferably etched using the same resist mask so that a contact hole 126 reaching the gate electrode is formed using the same resist mask. A cross-sectional view at this stage is FIG. 4B.

[0093]

Then, the resist mask is removed, and a transparent conductive film is formed. The transparent conductive film is formed using indium oxide (In_2O_3), an alloy of indium oxide and tin oxide (In_2O_3-SnO_2, abbreviated as ITO), or the like by a sputtering method, a vacuum evaporation method, or the like. Etching treatment of such a material is performed with a hydrochloric acid based solution. Instead, because a residue tends to be generated particularly in etching of ITO, an alloy of indium oxide and zinc oxide (In_2O_3-ZnO) may be used in order to improve etching processability.

[0094]

Next, a fifth photolithography step is performed to form a resist mask, so that an unnecessary portion is removed by etching to form a pixel electrode 110.

[0095]

In the fifth photolithography step, a storage capacitor is formed by the capacitor electrode layer 124 and the pixel electrode layer 110 with the gate insulating layer 102 in the capacitor portion, used as a dielectric. The capacitor wiring 108 is electrically connected to the capacitor electrode layer 124 through the contact hole 109.

[0096]

Furthermore, in the fifth photolithography step, the first terminal and the second terminal are covered with the resist mask so that transparent conductive films 128 and 129 remain in the terminal portion. The transparent conductive films 128 and 129 serve as electrodes or wirings that are used for connection with an FPC. The transparent conductive film 129 formed over the second terminal 122 serves as a terminal electrode for connection which functions as an input terminal for the source

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wiring.

[0097]

Then, the resist mask is removed, and a cross-sectional view at this stage is FIG. 4C. A top view at this stage is FIG. 8A.

5 [0098]

FIGS. 9A1 and 9A2 are a cross-sectional view and a top view of a gate wiring terminal portion at this stage, respectively. FIG. 9A1 is a cross-sectional view along line C1-C2 in FIG. 9A2. In FIG. 9A1, a transparent conductive film 155 formed over a protective insulating film 154 is a connecting terminal electrode which functions as an
10 input terminal. Furthermore, in a terminal portion of FIG. 9A1, a first terminal 151 formed using the same material as the material of a gate wiring and a connection electrode 153 formed using the same material as the material of a source wiring overlap each other with a gate insulating layer 152 interposed therebetween, and are electrically connected to each other through the transparent conductive film 155. Note that a
15 portion where the transparent conductive film 128 and the first terminal 121 shown in FIG. 4C are in contact with each other corresponds to a portion where the transparent conductive film 155 and the first terminal 151 are in contact with each other in FIG. 9A1.

[0099]

20 FIGS. 9B1 and 9B2 are a cross-sectional view and a top view of a source wiring terminal portion which is different from the source wiring terminal portion shown in FIG. 4C, respectively. FIG. 9B1 is a cross-sectional view along line D1-D2 in FIG. 9B2. In FIG. 9B1, a transparent conductive film 155 formed over a protective insulating film 154 is a connection terminal electrode which functions as an input
25 terminal. In a terminal portion in FIG. 9B1, an electrode 156 formed using the same material as the material of a gate wiring is located under and overlaps with a second terminal 150 electrically connected to a source wiring with a gate insulating layer 102 interposed therebetween. The electrode 156 is not electrically connected to the second terminal 150. When the electrode 156 is set to, for example, floating, GND, or 0 V
30 such that the potential the electrode 156 is different from the potential of the second terminal 150, a capacitor for preventing noise or static electricity can be formed. In addition, the second terminal 150 is electrically connected to the transparent conductive

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film 155 with the protective insulating film 154 interposed therebetween.

[0100]

A plurality of gate wirings, source wirings, and capacitor wirings are provided depending on the pixel density. Also in the terminal portion, the first terminal at the same potential as the gate wiring, the second terminal at the same potential as the source wiring, the third terminal at the same potential as the capacitor wiring, and the like are each arranged in plurality. There is no particular limitation on the number of each of the terminals, and the number of the terminals may be determined, as appropriate.

[0101]

Through these five photolithography steps, a pixel thin film transistor portion including the thin film transistor 170 which is a bottom-gate n-channel thin film transistor, and the storage capacitor can be completed using the five photomasks. When these pixel thin film transistor portion and storage capacitor are arranged in a matrix corresponding to respective pixels, a pixel portion can be formed and one of the substrates for manufacturing an active matrix display device can be obtained. In this specification, such a substrate is referred to as an active matrix substrate for convenience.

[0102]

When an active matrix liquid crystal display device is manufactured, an active matrix substrate and a counter substrate provided with a counter electrode are bonded to each other with a liquid crystal layer interposed therebetween. Note that a common electrode electrically connected to the counter electrode on the counter substrate is provided over the active matrix substrate, and a fourth terminal electrically connected to the common electrode is provided in the terminal portion. This fourth terminal is provided so that the common electrode is fixed to a predetermined potential such as GND or 0 V.

[0103]

One embodiment of the present invention is not limited to the pixel structure of FIG. 8, and an example of a top view different from FIG. 8 is illustrated in FIG. 10. FIG. 10 illustrates the example in which a capacitor wiring is not provided and a pixel electrode overlaps with a gate wiring of an adjacent pixel with a protective insulating film and a gate insulating layer interposed therebetween to form a storage capacitor. In

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that case, the capacitor wiring and a third terminal connected to the capacitor wiring can be omitted. Note that in FIG. 10, the same portions as those in FIG. 8 are denoted by the same reference numerals.

[0104]

5 In an active matrix liquid crystal display device, display patterns are formed on a screen by driving pixel electrodes arranged in a matrix. Specifically, when voltage is applied between a selected pixel electrode and a counter electrode that corresponds to the selected pixel electrode, a liquid crystal layer provided between the pixel electrode and the counter electrode is optically modulated, and this optical modulation is 10 recognized as a display pattern.

[0105]

In displaying moving images, a liquid crystal display device has a problem that a long response time of liquid crystal molecules themselves causes afterimages or blurring of moving images. In order to improve the moving-image characteristics of a 15 liquid crystal display device, a driving method called black insertion is employed in which black is displayed on the whole screen every other frame period.

[0106]

Alternatively, a driving method called double-frame rate driving may be employed in which the vertical cycle is 1.5 or 2 times as long as usual to improve the 20 moving-image characteristics.

[0107]

Further alternatively, in order to improve the moving-image characteristics of a liquid crystal display device, a driving method may be employed in which a plurality of LEDs (light-emitting diodes) or a plurality of EL light sources are used to form a 25 surface light source as a backlight, and each light source of the surface light source is independently driven in a pulsed manner in one frame period. As the surface light source, three or more kinds of LEDs may be used and an LED emitting white light may be used. Since a plurality of LEDs can be controlled independently, the light emission timing of LEDs can be synchronized with the timing at which a liquid crystal layer is 30 optically modulated. According to this driving method, LEDs can be partly turned off; therefore, an effect of reducing power consumption can be obtained particularly in the case of displaying an image having a large part on which black is displayed.

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[0108]

By combining these driving methods, the display characteristics of a liquid crystal display device, such as moving-image characteristics, can be improved as compared to those of conventional liquid crystal display devices.

5 [0109]

The n-channel transistor obtained in Embodiment 3 includes an In-Ga-Zn-O-based non-single-crystal semiconductor film in a channel formation region and has good dynamic characteristics. Thus, these driving methods can be applied in combination to the n-channel transistor of this embodiment.

10 [0110]

When a light-emitting display device is manufactured, one electrode (also referred to as a cathode) of an organic light-emitting element is set to a low power supply potential such as GND or 0 V; therefore, a terminal portion is provided with a fourth terminal for setting the cathode to a low power supply potential such as GND or 15 0 V. In addition, when a light-emitting display device is manufactured, a power supply line is provided in addition to a source wiring and a gate wiring. Therefore, a terminal portion is provided with a fifth terminal electrically connected to the power supply line.

[0111]

According to this embodiment, the thin film transistor has a stacked-layer 20 structure in which a gate electrode layer, a gate insulating layer, a source and drain electrode layers, a source and drain regions (an oxide semiconductor layer containing In, Ga, and Zn), and a semiconductor layer (an oxide semiconductor layer containing In, Ga, and Zn), and the quality of the surface of the gate insulating layer is changed by plasma treatment, so that the semiconductor film is kept to be thin and parasitic capacitance can 25 be suppressed. Note that the parasitic capacitance is sufficiently suppressed even when the semiconductor layer is thin, because the thickness is sufficient with respect to that of the gate insulating layer.

[0112]

According to this embodiment, a thin film transistor with high on-off ratio can 30 be obtained, so that a thin film transistor having high dynamic characteristics can be manufactured. Thus, a semiconductor device including a thin film transistor with high electrical characteristics and high reliability can be provided.

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[Embodiment 4]

[0113]

In this embodiment, an example of electronic paper will be described as a semiconductor device.

5 [0114]

FIG. 11 illustrates active-matrix electronic paper as an example of a semiconductor device, which is different from a liquid crystal display device. A thin film transistor 581 used in a pixel portion of the semiconductor device can be manufactured in a manner similar to the manner of the thin film transistor in the pixel
10 portion described in Embodiment 3 and is a thin film transistor including an In-Ga-Zn-O-based non-single-crystal film as a semiconductor layer. Further, as described in Embodiment 1, tapered shapes of side surfaces of two electrodes which face each other with an oxide semiconductor layer interposed therebetween enables electronic paper including a highly reliable thin film transistor provided with an
15 electric-field relaxation region to be manufactured.

[0115]

The electronic paper in FIG. 11 is an example of a display device using a twisting ball display system. A twisting ball display method employs a method in which display is performed by arranging spherical particles each of which is colored
20 separately in black and white between the first electrode layer and the second electrode layer which are electrode layers used for display elements, and generating a potential difference between the first electrode layer and the second electrode layer so as to control the directions of the spherical particles.

[0116]

25 The thin film transistor 581 is a bottom-gate thin film transistor, and a source or drain electrode layer thereof is in contact with a first electrode layer 587 through an opening formed in an insulating layer 585, whereby the thin film transistor 581 is electrically connected to the first electrode layer 587. Between the first electrode layer 587 and a second electrode layer 588, spherical particles 589 each having a black region
30 590a, a white region 590b, and a cavity 594 around the regions which is filled with liquid are provided. A space around the spherical particles 589 is filled with a filler 595 such as a resin (see FIG. 11).

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[0117]

Instead of the twisting ball, an electrophoretic element can also be used. A microcapsule having a diameter of approximately 10 μm to 200 μm, in which a transparent liquid and positively charged white microparticles and negatively charged
5 black microparticles are encapsulated, is used. In the microcapsule that is provided between the first electrode layer and the second electrode layer, when an electric field is applied by the first electrode layer and the second electrode layer, the white microparticles and the black microparticles migrate to opposite sides to each other, so that white or black can be displayed. A display element using this principle is an
10 electrophoretic display element, and is generally called an electronic paper. The electrophoretic display element has higher reflectivity than a liquid crystal display element; thus, an auxiliary light is unnecessary, less power is consumed, and a display portion can be recognized even in a dusky place. In addition, even when power is not supplied to the display portion, an image which has been displayed once can be
15 maintained; accordingly, a displayed image can be stored even if a semiconductor device having a display function (which may simply be referred to as a display device or a semiconductor device provided with a display device) is distanced from an electric wave source.

[0118]

20 Through the above process, electronic paper as a semiconductor device can be manufactured at reduced cost.

[0119]

This embodiment can be implemented in appropriate combination with any of the structures described in Embodiments 1 to 3.

25 [Embodiment 5]

[0120]

In this embodiment, an example will be described below, in which at least part of a driver circuit and a thin film transistor arranged in a pixel portion are formed over one substrate in a display device which is one example of a semiconductor device.

30 [0121]

The thin film transistor arranged in the pixel portion is formed according to Embodiment 1 or 2. Further, the thin film transistor described in Embodiment 1 or 2 is

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an n-channel TFT, and thus a part of a driver circuit that can include an n-channel TFT among driver circuits is formed over the same substrate as the substrate of the thin film transistor of the pixel portion.

[0122]

5 FIG. 12A illustrates an example of a block diagram of an active-matrix liquid crystal display device which is an example of a semiconductor device. The display device illustrated in FIG. 12A includes, over a substrate 5300, a pixel portion 5301 including a plurality of pixels that are each provided with a display element; a scan line driver circuit 5302 that selects a pixel; and a signal line driver circuit 5303 that controls 10 a video signal input to the selected pixel.

[0123]

The pixel portion 5301 is connected to the signal line driver circuit 5303 by a plurality of signal lines S1 to Sm (not shown) which extend in a column direction from the signal line driver circuit 5303, and to the scan line driver circuit 5302 by a plurality 15 of scan lines G1 to Gn (not shown) that extend in a row direction from the scan line driver circuit 5302. The pixel portion 5301 includes a plurality of pixels (not shown) arranged in matrix so as to correspond to the signal lines S1 to Sm and the scan lines G1 to Gn. Each pixel is connected to a signal line Sj (one of the signal lines S1 to Sm) and a scan line Gj (one of the scan lines G1 to Gn).

20 [0124]

The thin film transistor described in Embodiment 1 or 2 is an n-channel TFT, and a signal line driver circuit including the n-channel TFT is described with reference to FIG. 13.

[0125]

25 The signal line driver circuit illustrated in FIG. 13 includes a driver IC 5601, switch groups 5602_1 to 5602_M, a first wiring 5611, a second wiring 5612, a third wiring 5613, and wirings 5621_1 to 5621_M. Each of the switch groups 5602_1 to 5602_M includes a first thin film transistor 5603a, a second thin film transistor 5603b, and a third thin film transistor 5603c.

30 [0126]

The driver IC 5601 is connected to the first wiring 5611, the second wiring 5612, the third wiring 5613, and the wirings 5621_1 to 5621_M. Each of the switch

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groups 5602_1 to 5602_M is connected to the first wiring 5611, the second wiring 5612, the third wiring 5613, and the wirings 5621_1 to 5621_M corresponding to the switch groups 5602_1 to 5602_M, respectively. Each of the wirings 5621_1 to 5621_M is connected to three signal lines via the first thin film transistor 5603a, the second thin
5 film transistor 5603b, and the third thin film transistor 5603c. For example, the wiring 5621_J of the J-th column (one of the wirings 5621_1 to 5621_M) is connected to a signal line Sj−1, a signal line Sj, and a signal line Sj+1 via the first thin film transistor 5603a, the second thin film transistor 5603b, and the third thin film transistor 5603c which are included in the switch group 5602_J.

10 [0127]

A signal is input to each of the first wiring 5611, the second wiring 5612, and the third wiring 5613.

[0128]

Note that the driver IC 5601 is preferably formed over a single crystalline
15 semiconductor substrate. Further, the switch groups 5602_1 to 5602_M are preferably formed over the same substrate as the substrate of the pixel portion. Therefore, the driver IC 5601 and the switch groups 5602_1 to 5602_M are preferably connected through an FPC or the like.

[0129]

20 Next, operation of the signal line driver circuit illustrated in FIG. 13 is described with reference to a timing chart in FIG. 14. The timing chart in FIG. 14 illustrates the case where the scan line Gi of the i-th row is selected. A selection period of the scan line Gi of the i-th row is divided into a first sub-selection period T1, a second sub-selection period T2, and a third sub-selection period T3. The signal line
25 driver circuit in FIG. 13 operates similarly to that in FIG. 14 even when a scan line of another row is selected.

[0130]

Note that the timing chart in FIG. 14 shows the case where the wiring 5621_J of the J-th column is connected to the signal line Sj−1, the signal line Sj, and the signal
30 line Sj+1 via the first thin film transistor 5603a, the second thin film transistor 5603b, and the third thin film transistor 5603c.

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[0131]

The timing chart in FIG. 14 shows timing at which the scan line Gi of the i-th row is selected, timing 5703a of on/off of the first thin film transistor 5603a, timing 5703b of on/off of the second thin film transistor 5603b, timing 5703c of on/off of the third thin film transistor 5603c, and a signal 5721_J input to the wiring 5621_J of the J-th column.

[0132]

In the first sub-selection period T1, the second sub-selection period T2, and the third sub-selection period T3, different video signals are input to the wirings 5621_1 to 5621_M. For example, a video signal input to the wiring 5621_J in the first sub-selection period T1 is input to the signal line Sj−1, a video signal input to the wiring 5621_J in the second sub-selection period T2 is input to the signal line Sj, and a video signal input to the wiring 5621_J in the third sub-selection period T3 is input to the signal line Sj+1. The video signals input to the wiring 5621_J in the first sub-selection period T1, the second sub-selection period T2, and the third sub-selection period T3 are denoted by Data_j−1, Data_j, and Data_j+1, respectively.

[0133]

As shown in FIG. 14, in the first sub-selection period T1, the first thin film transistor 5603a is turned on, and the second thin film transistor 5603b and the third thin film transistor 5603c are turned off. At this time, Data_j−1 input to the wiring 5621_J is input to the signal line Sj−1 via the first thin film transistor 5603a. In the second sub-selection period T2, the second thin film transistor 5603b is turned on, and the first thin film transistor 5603a and the third thin film transistor 5603c are turned off. At this time, Data_j input to the wiring 5621_J is input to the signal line Sj via the second thin film transistor 5603b. In the third sub-selection period T3, the third thin film transistor 5603c is turned on, and the first thin film transistor 5603a and the second thin film transistor 5603b are turned off. At this time, Data_j+1 input to the wiring 5621_J is input to the signal line Sj+1 via the third thin film transistor 5603c.

[0134]

As described above, in the signal line driver circuit in FIG. 13, by dividing one gate selection period into three, video signals can be input to three signal lines from one

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wiring 5621 in one gate selection period. Therefore, in the signal line driver circuit in FIG. 13, the number of connections between the substrate provided with the driver IC 5601 and the substrate provided with the pixel portion can be about 1/3 of the number of signal lines. The number of connections is reduced to about 1/3 of the number of
5 the signal lines, so that reliability, yield, etc., of the signal line driver circuit in FIG. 13 can be improved.

[0135]

Note that there are no particular limitations on the arrangement, the number, a driving method, and the like of the thin film transistors, as long as one gate selection
10 period is divided into a plurality of sub-selection periods and video signals are input to a plurality of signal lines from one wiring in the respective sub-selection periods as shown in FIG. 13.

[0136]

For example, when video signals are input to three or more signal lines from
15 one wiring in each of three or more sub-selection periods, it is necessary to add a thin film transistor and a wiring for controlling the thin film transistor. Note that when one selection period is divided into four or more sub-selection periods, one sub-selection period becomes short. Therefore, one selection period is preferably divided into two or three sub-selection periods.

20 [0137]

As another example, one gate selection period may be divided into a precharge period Tp, the first sub-selection period T1, the second sub-selection period T2, and the third sub-selection period T3 as illustrated in a timing chart in FIG. 15. The timing chart in FIG. 15 illustrates timing at which the scan line Gi of the i-th row is selected,
25 timing 5803a of on/off of the first thin film transistor 5603a, timing 5803b of on/off of the second thin film transistor 5603b, timing 5803c of on/off of the third thin film transistor 5603c, and a signal 5821_J input to the wiring 5621_J of the J-th column. As shown in FIG. 15, the first thin film transistor 5603a, the second thin film transistor 5603b, and the third thin film transistor 5603c are tuned on in the precharge period Tp.
30 At this time, precharge voltage Vp input to the wiring 5621_J is input to each of the signal line Sj−1, the signal line Sj, and the signal line Sj+1 via the first thin film

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transistor 5603a, the second thin film transistor 5603b, and the third thin film transistor 5603c. In the first sub-selection period T1, the first thin film transistor 5603a is turned on, and the second thin film transistor 5603b and the third thin film transistor 5603c are turned off. At this time, Data_j−1 input to the wiring 5621_J is input to the signal line
5 Sj−1 via the first thin film transistor 5603a. In the second sub-selection period T2, the second thin film transistor 5603b is turned on, and the first thin film transistor 5603a and the third thin film transistor 5603c are turned off. At this time, Data_j input to the wiring 5621_J is input to the signal line Sj via the second thin film transistor 5603b. In the third sub-selection period T3, the third thin film transistor 5603c is turned on, and
10 the first thin film transistor 5603a and the second thin film transistor 5603b are turned off. At this time, Data_j+1 input to the wiring 5621_J is input to the signal line Sj+1 via the third thin film transistor 5603c.

[0138]

As described above, in the signal line driver circuit in FIG. 13 to which the
15 timing chart in FIG. 15 is applied, the video signal can be written to the pixel at high speed because the signal line can be precharged by providing a precharge selection period before a sub-selection period. Note that portions in FIG. 15 which are similar to those of FIG. 14 are denoted by common reference numerals and detailed description of the same portions and portions which have similar functions is omitted.

20 [0139]

Further, a structure of a scan line driver circuit is described. The scan line driver circuit includes a shift register and a buffer. Also, a level shifter may be included in some cases. In the scan line driver circuit, when the clock signal (CLK) and the start pulse signal (SP) are input to the shift register, a selection signal is
25 generated. The generated selection signal is buffered and amplified by the buffer, and the resulting signal is supplied to a corresponding scan line. Gate electrodes of transistors in pixels of one line are connected to the scan line. Since the transistors in the pixels of one line have to be turned on all at once, a buffer which can supply a large current is used.

30 [0140]

One mode of a shift register which is used in a part of a scan line driver circuit

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is described with reference to FIGS. 16 and 17.

[0141]

FIG. 16 illustrates a circuit configuration of the shift register. The shift register illustrated in FIG. 16 includes a plurality of flip-flops 5701-i (one of flip-flops 5701-1 to 5701-n). Further, the shift register operates by inputting a first clock signal, a second clock signal, a start pulse signal, and a reset signal.

[0142]

The connection relation of the shift register in FIG. 16 is described below. In the i-th stage flip-flop 5701_i (one of the flip-flops 5701_1 to 5701_n) in the shift register of FIG. 16, a first wiring 5501 illustrated in FIG. 17 is connected to a seventh wiring 5717_i–1; a second wiring 5502 illustrated in FIG. 17 is connected to a seventh wiring 5717_i+1; a third wiring 5503 illustrated in FIG. 17 is connected to a seventh wiring 5717_i; and a sixth wiring 5506 illustrated in FIG. 17 is connected to a fifth wiring 5715.

[0143]

Further, a fourth wiring 5504 shown in FIG. 17 is connected to a second wiring 5712 in flip-flops of odd-numbered stages, and is connected to a third wiring 5713 in flip-flops of even-numbered stages. A fifth wiring 5505 shown in FIG. 17 is connected to a fourth wiring 5714.

[0144]

Note that the first wiring 5501 of the first stage flip-flop 5701_1 shown in FIG. 17 is connected to a first wiring 5711, and the second wiring 5502 of the n-th stage flip-flop 5701_n shown in FIG. 17 is connected to a sixth wiring 5716.

[0145]

Note that the first wiring 5711, the second wiring 5712, the third wiring 5713, and the sixth wiring 5716 may be referred to as a first signal line, a second signal line, a third signal line, and a fourth signal line, respectively. The fourth wiring 5714 and the fifth wiring 5715 may be referred to as a first power supply line and a second power supply line, respectively.

[0146]

Next, FIG. 17 illustrates details of the flip-flop shown in FIG. 16. A flip-flop

illustrated in FIG. 17 includes a first thin film transistor 5571, a second thin film transistor 5572, a third thin film transistor 5573, a fourth thin film transistor 5574, a fifth thin film transistor 5575, a sixth thin film transistor 5576, a seventh thin film transistor 5577, and an eighth thin film transistor 5578. Each of the first thin film
5 transistor 5571, the second thin film transistor 5572, the third thin film transistor 5573, the fourth thin film transistor 5574, the fifth thin film transistor 5575, the sixth thin film transistor 5576, the seventh thin film transistor 5577, and the eighth thin film transistor 5578 is an n-channel transistor and is turned on when the gate-source voltage (V_{gs}) exceeds the threshold voltage (V_{th}).

10 [0147]

Next, the connection structure of the flip-flop illustrated in FIG. 16 is described below.

[0148]

A first electrode (one of a source electrode and a drain electrode) of the first
15 thin film transistor 5571 is connected to the fourth wiring 5504. A second electrode (the other of the source electrode and the drain electrode) of the first thin film transistor 5571 is connected to the third wiring 5503.

[0149]

A first electrode of the second thin film transistor 5572 is connected to the sixth
20 wiring 5506, and a second electrode of the second thin film transistor 5572 is connected to the third wiring 5503.

[0150]

A first electrode of the third thin film transistor 5573 is connected to the fifth wiring 5505; a second electrode of the third thin film transistor 5573 is connected to a
25 gate electrode of the second thin film transistor 5572; and a gate electrode of the third thin film transistor 5573 is connected to the fifth wiring 5505.

[0151]

A first electrode of the fourth thin film transistor 5574 is connected to the sixth wiring 5506; a second electrode of the fourth thin film transistor 5574 is connected to a
30 gate electrode of the second thin film transistor 5572; and a gate electrode of the fourth thin film transistor 5574 is connected to a gate electrode of the first thin film transistor 5571.

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[0152]

A first electrode of the fifth thin film transistor 5575 is connected to the fifth wiring 5505; a second electrode of the fifth thin film transistor 5575 is connected to the gate electrode of the first thin film transistor 5571; and a gate electrode of the fifth thin film transistor 5575 is connected to the first wiring 5501.

[0153]

A first electrode of the sixth thin film transistor 5576 is connected to the sixth wiring 5506; a second electrode of the sixth thin film transistor 5576 is connected to the gate electrode of the first thin film transistor 5571; and a gate electrode of the sixth thin film transistor 5576 is connected to the gate electrode of the second thin film transistor 5572.

[0154]

A first electrode of the seventh thin film transistor 5577 is connected to the sixth wiring 5506; a second electrode of the seventh thin film transistor 5577 is connected to the gate electrode of the first thin film transistor 5571; and a gate electrode of the seventh thin film transistor 5577 is connected to the second wiring 5502. A first electrode of the eighth thin film transistor 5578 is connected to the sixth wiring 5506; a second electrode of the eighth thin film transistor 5578 is connected to the gate electrode of the second thin film transistor 5572; and a gate electrode of the eighth thin film transistor 5578 is connected to the first wiring 5501.

[0155]

Note that the points at which the gate electrode of the first thin film transistor 5571, the gate electrode of the fourth thin film transistor 5574, the second electrode of the fifth thin film transistor 5575, the second electrode of the sixth thin film transistor 5576, and the second electrode of the seventh thin film transistor 5577 are connected are each referred to as a node 5543. The points at which the gate electrode of the second thin film transistor 5572, the second electrode of the third thin film transistor 5573, the second electrode of the fourth thin film transistor 5574, the gate electrode of the sixth thin film transistor 5576, and the second electrode of the eighth thin film transistor 5578 are connected are each referred to as a node 5544.

[0156]

Note that the first wiring 5501, the second wiring 5502, the third wiring 5503,

and the fourth wiring 5504 may be referred to as a first signal line, a second signal line, a third signal line, and a fourth signal line, respectively. The fifth wiring 5505 and the sixth wiring 5506 may be referred to as a first power supply line and a second power supply line, respectively.

5 [0157]

The signal line driver circuit and the scan line driver circuit can be formed using only the n-channel TFTs described in Embodiment 1 or 2. In that case, the drive frequency of the driver circuit can be increased because the mobility of a transistor using an oxide semiconductor layer is high. Further, since the parasitic capacitance is
10 reduced by the source and drain regions in each of the n-channel TFTs described in Embodiment 1 or 2, the frequency characteristic (also called f characteristic) is high. For example, a scan line driver circuit using the n-channel TFT described in Embodiment 1 or 2 can operate at high speed, and thus a frame frequency can be increased and insertion of black images can be realized.

15 [0158]

In addition, by increasing the channel width of the transistor in the scan line driver circuit or providing a plurality of scan line driver circuits, for example, higher frame frequency can be realized. When a plurality of scan line driver circuits are provided, a scan line driver circuit for driving even-numbered scan lines is provided on
20 one side and a scan line driver circuit for driving odd-numbered scan lines is provided on the opposite side; thus, increase in frame frequency can be realized.

[0159]

Further, when an active-matrix light-emitting display device which is an example of a semiconductor device is manufactured, a plurality of thin film transistors
25 are arranged in at least one pixel, and thus a plurality of scan line driver circuits are preferably arranged. FIG. 12B is a block diagram illustrating an example of an active-matrix light-emitting display device.

[0160]

The light-emitting display device illustrated in FIG. 12B includes, over a
30 substrate 5400, a pixel portion 5401 having a plurality of pixels each provided with a display element, a first scan line driver circuit 5402 and a second scan line driver circuit 5404 that select a pixel, and a signal line driver circuit 5403 that controls input of a

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video signal to the selected pixel.

[0161]

When the video signal input to a pixel of the light-emitting display device illustrated in FIG. 12B is a digital signal, a pixel is in a light-emitting state or in a
5 non-light-emitting state by switching of ON/OFF of a transistor. Thus, grayscale can be displayed using an area ratio grayscale method or a time ratio grayscale method. An area ratio grayscale method refers to a driving method by which one pixel is divided into a plurality of subpixels and the respective subpixels are driven separately based on video signals so that grayscale is displayed. Further, a time ratio grayscale method
10 refers to a driving method by which a period during which a pixel is in a light-emitting state is controlled so that grayscale is displayed.

[0162]

Since the response speed of light-emitting elements is faster than that of liquid crystal elements or the like, the light-emitting elements are suitable for a time ratio
15 grayscale method. Specifically, in the case of performing display with a time ratio grayscale method, one frame period is divided into a plurality of subframe periods. Then, in accordance with video signals, the light-emitting element in the pixel is set in a light-emitting state or a non-light-emitting state in each subframe period. By dividing one frame period into a plurality of subframe periods, the total length of time, in which
20 a pixel actually emits light in one frame period, can be controlled by video signals so that grayscale can be displayed.

[0163]

In the example of the light-emitting display device illustrated in FIG. 12B, in the case where two TFTs, a switching TFT and a current control TFT, are arranged in
25 one pixel, the first scan line driver circuit 5402 generates a signal which is input to a first scan line serving as a gate wiring of the switching TFT, and the second scan line driver circuit 5404 generates a signal which is input to a second scan line serving as a gate wiring of the current control TFT; however, one scan line driver circuit may generate both the signal which is input to the first scan line and the signal which is input
30 to the second scan line. In addition, for example, there is a possibility that a plurality of first scan lines used for controlling the operation of the switching element be provided in each pixel depending on the number of transistors included in the switching

element. In that case, signals which are input to the plurality of first scan lines may be all generated by one scan line driver circuit or by an individual plurality of scan line driver circuits.

[0164]

5 Also in the light-emitting display device, a part of a driver circuit that can include n-channel TFTs among driver circuits can be formed over the same substrate as the substrate of the thin film transistors of the pixel portion. The signal line driver circuit and the scan line driver circuit can be formed using only the n-channel TFTs described in Embodiment 1 or 2.

10 [0165]

Through the above process, a highly reliable display device can be manufactured as a semiconductor device.

[0166]

This embodiment can be implemented in appropriate combination with any of 15 the structures disclosed in the other embodiments.

[Embodiment 6]

[0167]

In this embodiment, an example of a light-emitting display device will be described as a semiconductor device. As a display element included in a display 20 device, a light-emitting element utilizing electro luminescence is described in this embodiment. Light-emitting elements utilizing electroluminescence are classified according to the type of a light emitting material, that is, an organic compound or an inorganic compound. In general, the former is referred to as an organic EL element, the latter as an inorganic EL element.

25 [0168]

In an organic EL element, voltage is applied to the light-emitting element, so that electrons are injected from an electrode into a layer including a light-emitting organic compound, and holes are injected from the other electrode into the layer including the light-emitting organic compound, and there flows electric current. Then, 30 by recombination of these carriers (electrons and holes), the organic compound having a light-emitting property gets in an excited state, and light is emitted when the excited state returns to a ground state. From such a mechanism, such a light emitting element

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is referred to as a current-excitation-type light-emitting element.

[0169]

Inorganic EL elements are classified in a dispersive inorganic EL element and a thin-film inorganic EL element. A dispersive inorganic EL element includes a light-emitting layer in which particles of a light-emitting material are dispersed in a binder, and light emission mechanism thereof is donor-acceptor recombination light emission, in which a donor level and an acceptor level are utilized. In a thin film inorganic EL element, a light-emitting layer is sandwiched between dielectric layers, and the dielectric layers are sandwiched between electrodes. Light emission mechanism of the thin film inorganic EL element is local light emission, in which inner-shell electron transition of a metal ion is utilized. In this embodiment, description will be made using an organic EL element as a light-emitting element.

[0170]

FIG. 18 illustrates an example of a pixel structure to which digital time grayscale driving can be applied, as an example of a semiconductor device.

[0171]

A structure and an operation of the pixel to which digital time grayscale driving can be applied are described below. An example is described in this embodiment in which one pixel includes two n-channel transistors using an oxide semiconductor layer (an In-Ga-Zn-O-based non-single-crystal film) in a channel formation region.

[0172]

A pixel 6400 includes a switching transistor 6401, a driving transistor 6402, a light-emitting element 6404, and a capacitor 6403. A gate of the switching transistor 6401 is connected to a scan line 6406, a first electrode (one of a source electrode and a drain electrode) of the switching transistor 6401 is connected to a signal line 6405, and a second electrode (the other of the source electrode and the drain electrode) of the switching transistor 6401 is connected to a gate of the driving transistor 6402. The gate of the driving transistor 6402 is connected to a power supply line 6407 through the capacitor 6403, a first electrode of the driving transistor 6402 is connected to the power supply line 6407, and a second electrode of the driving transistor 6402 is connected to a first electrode (pixel electrode) of the light-emitting element 6404. A second electrode of the light-emitting element 6404 corresponds to a common electrode 6408.

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[0173]

The second electrode of the light-emitting element 6404 (the common electrode 6408) is set to a low power supply potential. The low power supply potential is a potential satisfying the low power supply potential < a high power supply potential with the high power supply potential set to the power supply line 6407 as a reference. As the low power supply potential, GND, 0 V, or the like may be employed, for example. A potential difference between the high power supply potential and the low power supply potential is applied to the light-emitting element 6404, and a current is supplied to the light-emitting element 6404. Here, in order to make the light-emitting element 6404 emit light, each potential is set so that the potential difference between the high power supply potential and the low power supply potential is a forward threshold voltage or higher.

[0174]

Gate capacitance of the driving transistor 6402 may be used as a substitute for the capacitor 6403, so that the capacitor 6403 can be omitted. The gate capacitance of the driving transistor 6402 may be formed between a channel region and a gate electrode.

[0175]

In the case of voltage-input voltage-driving method, a video signal is input to the gate of the driving transistor 6402 so that the driving transistor 6402 is in either of two states of being sufficiently turned on and turned off. That is, the driving transistor 6402 operates in a linear region. Since the driving transistor 6402 operates in a linear region, a voltage higher than the voltage of the power supply line 6407 is applied to the gate of the driving transistor 6402. Note that a voltage greater than or equal to the sum voltage of the power supply line voltage and V_{th} of the driving transistor 6402 is applied to the signal line 6405.

[0176]

In the case of performing analog grayscale driving instead of digital time grayscale driving, the same pixel structure as that in FIG. 18 can be used by changing signal input.

[0177]

In the case of performing the analog grayscale driving, a voltage greater than or

equal to the sum of the forward voltage of the light-emitting element 6404 and V_{th} of the driving transistor 6402 is applied to the gate of the driving transistor 6402. The forward voltage of the light-emitting element 6404 refers to a voltage to obtain a desired luminance, and includes at least a forward threshold voltage. The video signal such
5 that the driving transistor 6402 operates in a saturation region is input, so that a current can be supplied to the light-emitting element 6404. In order that the driving transistor 6402 can operate in the saturation region, the potential of the power supply line 6407 is higher than the gate potential of the driving transistor 6402. Since the video signal is an analog signal, a current in accordance with the video signal flows in the
10 light-emitting element 6404, and the analog grayscale driving can be performed.

[0178]

Note that the pixel structure illustrated in FIG. 18 is not limited thereto. For example, a switch, a resistor, a capacitor, a transistor, a logic circuit, or the like may be added to the pixel illustrated in FIG. 18.

15 [0179]

Next, structures of a light-emitting element will be described using FIGS. 19A to 19C. In this embodiment, cross-sectional structures of pixels are described taking the case where a driving TFT is the thin film transistor 170, as an example. Driving TFTs 7001, 7011, and 7021 used in semiconductor devices illustrated in FIGS. 19A to
20 19C can be manufactured in a manner similar to that of the thin film transistor 170 described in Embodiment 1 and are thin film transistors having high electrical characteristics, each including an In-Ga-Zn-O-based non-single-crystal film as a semiconductor layer.

[0180]

25 In order to extract light emission from the light-emitting element, at least one of the anode and the cathode of the light-emitting element is required to be transparent. The thin film transistors and the light-emitting element are formed over the substrate. A light-emitting element can have a top emission structure in which light is extracted through the surface opposite to the substrate; a bottom emission structure in which light
30 is extracted through the surface on the substrate side; or a dual emission structure in which light is extracted through the surface opposite to the substrate and the surface on the substrate side. The pixel structure illustrated in FIG. 18 can be applied to a

light-emitting element having any of these emission structures.

[0181]

A light-emitting element having a top emission structure is described with reference to FIG. 19A.

5 [0182]

FIG. 19A is a cross-sectional view of a pixel in the case where a driving TFT 7001 is the thin film transistor 170 shown in FIG. 1B and light emission from a light-emitting element 7002 passes to an anode 7005 side. In FIG. 19A, a cathode 7003 of the light-emitting element 7002 is electrically connected to the driving TFT 10 7001, and a light-emitting layer 7004 and the anode 7005 are stacked in this order over the cathode 7003. The cathode 7003 can be formed using various conductive materials as long as they have a low work function and reflect light. For example, Ca, Al, CaF, MgAg, AlLi, or the like is preferably used. The light-emitting layer 7004 may be formed using either a single layer or a stacked layer of a plurality of layers. If the 15 light-emitting layer 7004 is formed using a plurality of layers, the light-emitting layer 7004 is formed by stacking an electron-injecting layer, an electron-transporting layer, a light-emitting layer, a hole-transporting layer, and a hole-injecting layer in this order over the cathode 7003. It is not necessary to form all of these layers. The anode 7005 is formed using a light-transmitting conductive film such as a film of indium oxide 20 including tungsten oxide, indium zinc oxide including tungsten oxide, indium oxide including titanium oxide, indium tin oxide including titanium oxide, indium tin oxide (hereinafter, referred to as ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added.

[0183]

25 A region where the light-emitting layer 7004 is sandwiched between the cathode 7003 and the anode 7005 corresponds to the light-emitting element 7002. In the case of the pixel illustrated in FIG. 19A, light emitted from the light-emitting element 7002 is ejected to the anode 7005 side as indicated by an arrow.

[0184]

30 A light-emitting element having a bottom emission structure is described next with reference to FIG. 19B. FIG. 19B is a cross-sectional view of a pixel in the case where a driving TFT 7011 is the thin film transistor 170 shown in FIG. 1A and light

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emission from a light-emitting element 7012 passes to a cathode 7013 side. In FIG. 19B, the cathode 7013 of the light-emitting element 7012 is formed over a light-transmitting conductive film 7017 that is electrically connected to the driving TFT 7011, and a light-emitting layer 7014 and an anode 7015 are stacked in this order over
5 the cathode 7013. A blocking film 7016 for reflecting or blocking light may be formed so as to cover the anode 7015 when the anode 7015 has a light-transmitting property. For the cathode 7013, a variety of materials can be used as in the case of FIG. 19A as long as they are conductive materials having a low work function. The cathode 7013 has a thickness that can transmit light (preferably, about 5 to 30 nm). For example, an
10 aluminum film with a thickness of 20 nm can be used as the cathode 7013. In a manner similar to that of FIG. 19A, the light-emitting layer 7014 may be formed using either a single-layer structure or a layered structure of a plurality of layers. Although the anode 7015 does not need to transmit light, the anode 7015 can be formed using a light-transmitting conductive material in a manner similar to that of FIG. 19A. For the
15 blocking film 7016, a metal or the like that reflects light can be used; however, it is not limited to a metal film. For example, a resin or the like to which black pigments are added can be used.

[0185]

A region where the light-emitting layer 7014 is sandwiched between the
20 cathode 7013 and the anode 7015 corresponds to the light-emitting element 7012. In the case of the pixel illustrated in FIG. 19B, light emitted from the light-emitting element 7012 is ejected to the cathode 7013 side as indicated by an arrow.

[0186]

Next, a light-emitting element having a dual emission structure is described
25 with reference to FIG. 19C. In FIG. 19C, a cathode 7023 of a light-emitting element 7022 is formed over a light-transmitting conductive film 7027 which is electrically connected to the driving TFT 7021, and a light-emitting layer 7024 and an anode 7025 are stacked in this order over the cathode 7023. As in the case of FIG. 19A, the cathode 7023 can be formed using a variety of conductive materials as long as they have
30 a low work function. The cathode 7023 has a thickness that can transmit light. For example, an Al film having a thickness of 20 nm can be used as the cathode 7023. In a manner similar to that of FIG. 19A, the light-emitting layer 7024 may be formed using

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either a single-layer structure or a layered structure of a plurality of layers. In a manner similar to that of FIG. 19A, the anode 7025 can be formed using a light-transmitting conductive material.

[0187]

5 A region where the cathode 7023, the light-emitting layer 7024, and the anode 7025 overlap with each other corresponds to the light-emitting element 7022. In the case of the pixel illustrated in FIG. 19C, light emitted from the light-emitting element 7022 is ejected to both an anode 7025 side and a cathode 7023 side as indicated by arrows.

10 [0188]

Although an organic EL element is described as a light-emitting element in this embodiment, an inorganic EL element may be provided as a light-emitting element.

[0189]

This embodiment describes the example in which a thin film transistor for 15 controlling the drive of a light-emitting element (the driving TFT) is electrically connected to the light-emitting element. However, a current control TFT may be connected between the driving TFT and the light-emitting element.

[0190]

A semiconductor device described in this embodiment is not limited to the 20 structures illustrated in FIGS. 19A to 19C and can be modified in various ways based on the spirit of techniques according to the present invention disclosed in this specification.

[0191]

Next, a top surface and a cross section of a light-emitting display panel (also referred to as a light-emitting panel), which is one embodiment of the semiconductor 25 device will be described with reference to FIGS. 22A and 22B. FIG. 22A is a top view of a panel in which a thin film transistor and a light-emitting element are sealed between a first substrate and a second substrate with a sealant. FIG. 22B is a cross-sectional view taken along line H-I of FIG. 22A.

[0192]

30 A sealant 4505 is provided to surround a pixel portion 4502, signal line driver circuits 4503a and 4503b, and scan line driver circuits 4504a and 4504b, which are provided over a first substrate 4501. In addition, a second substrate 4506 is provided

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over the pixel portion 4502, the signal line driver circuits 4503a and 4503b, and the scan line driver circuits 4504a and 4504b. Accordingly, the pixel portion 4502, the signal line driver circuits 4503a and 4503b, and the scan line driver circuits 4504a and 4504b are sealed together with a filler 4507, by the first substrate 4501, the sealant 4505, and
5 the second substrate 4506. It is preferable that a display device be thus packaged (sealed) with a protective film (such as a bonding film or an ultraviolet curable resin film) or a cover material with high air-tightness and little degasification so that the display device is not exposed to the outside air.

[0193]

10 The pixel portion 4502, the signal line driver circuits 4503a and 4503b, and the scan line driver circuits 4504a and 4504b formed over the first substrate 4501 each include a plurality of thin film transistors, and a thin film transistor 4510 included in the pixel portion 4502 and a thin film transistor 4509 included in the signal line driver circuit 4503a are illustrated as an example in FIG. 20B.

15 [0194]

As the thin film transistors 4509 and 4510, the highly reliable thin film transistors described in Embodiment 1, each including an In-Ga-Zn-O-based non-single-crystal film as a semiconductor layer can be used.

[0195]

20 Moreover, reference numeral 4511 denotes a light-emitting element. A first electrode layer 4517 that is a pixel electrode included in the light-emitting element 4511 is electrically connected to a source electrode layer or a drain electrode layer of the thin film transistor 4510. Note that a structure of the light-emitting element 4511 which includes the first electrode layer 4517, an electroluminescent layer 4512, and the second
25 electrode layer 4513 is not limited to the structure described in Embodiment 6. The structure of the light-emitting element 4511 can be changed as appropriate depending on the direction in which light is extracted from the light-emitting element 4511, or the like.

[0196]

30 A bank 4520 is formed using an organic resin film, an inorganic insulating film, or organic polysiloxane. It is particularly preferable that the bank 4520 be formed using a photosensitive material to have an opening over the first electrode layer 4517 so

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that a sidewall of the opening is formed as an inclined surface with continuous curvature.

[0197]

The electroluminescent layer 4512 may be formed as a single layer or a
5 plurality of layers stacked.

[0198]

A protective film may be formed over the second electrode layer 4513 and the bank 4520 in order to prevent oxygen, hydrogen, moisture, carbon dioxide, or the like from entering into the light-emitting element 4511. As the protective film, a silicon
10 nitride film, a silicon nitride oxide film, a DLC film, or the like can be formed.

[0199]

A variety of signals and potentials are supplied to the signal line driver circuits 4503a and 4503b, the scan line driver circuits 4504a and 4504b, or the pixel portion 4502 from FPCs 4518a and 4518b.

15 [0200]

In Embodiment 6, a connection terminal electrode 4515 is formed from the same conductive film as the first electrode layer 4517 included in the light-emitting element 4511, and a terminal electrode 4516 is formed from the same conductive film as the source and drain electrode layers included in the thin film transistors 4509 and 4510.

20 [0201]

The connection terminal electrode 4515 is electrically connected to a terminal of the FPC 4518a through an anisotropic conductive film 4519.

[0202]

As the second substrate located in the direction in which light is extracted from
25 the light-emitting element 4511 needs to have a light-transmitting property. In that case, a material with a light-transmitting property, such as a glass plate, a plastic sheet, a polyester film, or an acrylic film is used.

[0203]

As the filler 4507, an ultraviolet curable resin or a thermosetting resin can be
30 used, in addition to an inert gas such as nitrogen or argon. For example, PVC (polyvinyl chloride), acrylic, polyimide, an epoxy resin, a silicone resin, PVB (polyvinyl butyral), or EVA (ethylene vinyl acetate) can be used.

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[0204]

If necessary, an optical film such as a polarizing plate, a circularly polarizing plate (including an elliptically polarizing plate), a retardation plate (a quarter-wave plate or a half-wave plate), or a color filter may be provided as appropriate for a
5 light-emitting surface of the light-emitting element. Further, the polarizing plate or the circularly polarizing plate may be provided with an anti-reflection film. For example, anti-glare treatment may be carried out by which reflected light can be diffused by projections and depressions on the surface so as to reduce the glare.

[0205]

10 The signal line driver circuits 4503a and 4503b and the scan line driver circuits 4504a and 4504b may be mounted as driver circuits formed using a single crystal semiconductor film or polycrystalline semiconductor film over a single crystal semiconductor substrate or an insulating substrate separately prepared. Alternatively, only the signal line driver circuits or part thereof, or the scan line driver circuits or part
15 thereof may be separately formed and mounted. This embodiment is not limited to the structure illustrated in FIGS. 22A and 22B.

[0206]

Through the above process, a light-emitting display device (display panel) can be manufactured at low cost.

20 [0207]

This embodiment can be implemented in appropriate combination with any of the structures described in Embodiments 1 to 3.

[Embodiment 7]

[0208]

25 In this embodiment, top surfaces and a cross section each of a liquid crystal display panel which corresponds to one example of the semiconductor device will be described using FIGS. 20A1, 20A2, and 20B. FIGS. 20A1 and 20A2 are each a top view of a panel in which thin film transistors 4010 and 4011 formed over a first substrate 4001 and a liquid crystal element 4013 are sealed between the first substrate
30 4001 and a second substrate 4006 with a sealant 4005. The thin film transistors 4010 and 4011 are according to Embodiment 1 and each includes an In-Ga-Zn-O-based non-single-crystal film as a semiconductor layer. FIG. 20B is a cross-sectional view

along line M-N of each of FIGS. 20A1 and 20A2.

[0209]

The sealant 4005 is provided so as to surround a pixel portion 4002 and a scan line driver circuit 4004 that are provided over the first substrate 4001. The second substrate 4006 is provided over the pixel portion 4002 and the scan line driver circuit 4004. Therefore, the pixel portion 4002 and the scan line driver circuit 4004 are sealed together with a liquid crystal layer 4008, by the first substrate 4001, the sealant 4005, and the second substrate 4006. A signal line driver circuit 4003 that is formed using a single crystal semiconductor film or a polycrystalline semiconductor film over a substrate separately prepared is mounted in a region different from the region surrounded by the sealant 4005 over the first substrate 4001.

[0210]

Note that there is no particular limitation on the connection method of a driver circuit which is separately formed, and a COG method, a wire bonding method, a TAB method, or the like can be used. FIG. 20A1 illustrates an example of mounting the signal line driver circuit 4003 by a COG method, and FIG. 20A2 illustrates an example of mounting the signal line driver circuit 4003 by a TAB method.

[0211]

The pixel portion 4002 and the scan line driver circuit 4004 provided over the first substrate 4001 each include a plurality of thin film transistors. FIG. 20B illustrates the thin film transistor 4010 included in the pixel portion 4002 and the thin film transistor 4011 included in the scanning line driver circuit 4004. Insulating layers 4020 and 4021 are provided over the thin film transistors 4010 and 4011.

[0212]

As each of the thin film transistors 4010 and 4011, the thin film transistor including an In-Ga-Zn-O-based non-single-crystal film as a semiconductor layer, which is described in Embodiment 1 can be employed. The thin film transistor 4011 corresponds to the thin film transistor 170 shown in FIG. 1 of Embodiment 1.

[0213]

A pixel electrode layer 4030 included in the liquid crystal element 4013 is electrically connected to the thin film transistor 4010. A counter electrode layer 4031 of the liquid crystal element 4013 is formed over the second substrate 4006. A portion

where the pixel electrode layer 4030, the counter electrode layer 4031, and the liquid crystal layer 4008 overlap with one another corresponds to the liquid crystal element 4013. Note that the pixel electrode layer 4030 and the counter electrode layer 4031 are provided with an insulating layer 4032 and an insulating layer 4033, respectively, each
5 of which functions as an alignment film. The liquid crystal layer 4008 is sandwiched between the pixel electrode layer 4030 and the counter electrode layer 4031 with the insulating layers 4032 and 4033 interposed therebetween.

[0214]

The first substrate 4001 and the second substrate 4006 can be formed using
10 glass, metal (typically, stainless steel), ceramic, or plastic. As for plastic, an FRP (fiberglass-reinforced plastics) plate, a PVF (polyvinyl fluoride) film, a polyester film, or an acrylic resin film can be used. Further, sheet in which aluminum foil is sandwiched by PVF films or polyester films can also be used.

[0215]

15 A columnar spacer denoted by reference numeral 4035 is obtained by selective etching of an insulating film and is provided in order to control the distance (a cell gap) between the pixel electrode layer 4030 and the counter electrode layer 4031. Note that a spherical spacer may be used. The counter electrode layer 4031 is electrically connected to a common potential line provided over the same substrate as the substrate
20 of the thin film transistor 4010. With the use of the common connection portion, the counter electrode layer 4031 can be electrically connected to the common potential line through conductive particles provided between the pair of substrates. Note that the conductive particles are contained in the sealant 4005.

[0216]

25 Alternatively, a liquid crystal showing a blue phase for which an alignment film is unnecessary may be used. A blue phase is one of the liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase while temperature of cholesteric liquid crystal is increased. Since the blue phase is only generated within a narrow range of temperatures, a liquid crystal composition
30 containing a chiral agent at 5 wt% or more is used for the liquid crystal layer 4008 in order to improve the temperature range. The liquid crystal composition which includes a liquid crystal showing a blue phase and a chiral agent has a small response

time of 10 to 100 μs, has optical isotropy, which makes the alignment process unneeded, and has a small viewing angle dependence.

[0217]

Although an example of a transmissive liquid crystal display device is described in this embodiment, the present invention can also be applied to a reflective liquid crystal display device or a transflective liquid crystal display device.

[0218]

In Embodiment 7, an example of the liquid crystal display device is described in which a polarizing plate is provided on the outer surface of the substrate (on the viewer side) and a coloring layer and an electrode layer used for a display element are provided on the inner surface of the substrate in this order; however, the polarizing plate may be provided on the inner surface of the substrate. The stack structure of the polarizing plate and the coloring layer is not limited to that described in Embodiment 7 and may be set as appropriate depending on materials of the polarizing plate and the coloring layer or conditions of manufacturing steps. Furthermore, a light-blocking film serving as a black matrix may be provided.

[0219]

In this embodiment, in order to reduce surface roughness of the thin film transistor and to improve reliability of the thin film transistor, the thin film transistor obtained by Embodiment 1 is covered with the insulating layers (the insulating layer 4020 and the insulating layer 4021) each functioning as a protective film or a planarizing insulating film. The protective film is provided to prevent entry of impurities floating in air, such as an organic substance, a metal substance, or moisture, and is preferably a dense film. The protective film may be formed by a sputtering method to be a single-layer film or a stack of a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, and/or an aluminum nitride oxide film. Although an example in which the protective film is formed by a sputtering method is described in this embodiment, the present invention is not limited to this example, and the protective film may be formed by a variety of methods such as a PCVD method.

[0220]

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In this embodiment, the insulating layer 4020 having a stack structure is formed as the protective film. As a first layer of the insulating layer 4020, a silicon oxide film is formed by a sputtering method. The use of the silicon oxide film as the protective film has the effect of preventing a hillock of an aluminum film used for the
5 source and drain electrode layers.

[0221]

In addition, an insulating layer is formed as a second layer of the protective film. In this embodiment, as the second layer of the insulating layer 4020, a silicon nitride film is formed by a sputtering method. The use of the silicon nitride film as the
10 protective film can prevent the entry of mobile ions of sodium or the like to a semiconductor region so that variation in electrical characteristics of the TFT can be suppressed.

[0222]

After the protective film is formed, the semiconductor layer may be subjected
15 to annealing (at 300 to 400 °C).

[0223]

Then, the insulating layer 4021 is formed as the planarizing insulating film. The insulating layer 4021 can be formed using an organic material having heat resistance, such as polyimide, acrylic, benzocyclobutene, polyamide, or epoxy. Other
20 than such organic materials, it is also possible to use a low-dielectric constant material (a low-k material), a siloxane-based resin, PSG (phosphosilicate glass), BPSG (borophosphosilicate glass), or the like. Note that the insulating layer 4021 may be formed by stacking a plurality of insulating films formed using any of these materials.

[0224]

25 Note that a siloxane resin is a resin formed from a siloxane material as a starting material and having the bond of Si-O-Si. A siloxane-based resin may use, as a substituent, an organic group (e.g., an alkyl group, and an aryl group) or a fluoro group. The organic group may have a fluoro group.

[0225]

30 There is no particular limitation on the method for forming the insulating layer 4021, and the insulating layer 4021 can be formed, depending on the material, by a sputtering method, an SOG method, a spin coating method, a dipping method, a spray

coating method, a droplet discharge method (e.g., an inkjet method, screen printing, offset printing, or the like), a doctor knife, a roll coater, a curtain coater, a knife coater, or the like. In the case where the insulating layer 4021 is formed using a material solution, the semiconductor layer may be annealed (at 300 to 400 °C) at the same time
5 as a baking step. The baking step of the insulating layer 4021 also serves as the annealing step of the semiconductor layer, whereby a semiconductor device can be manufactured efficiently.

[0226]

The pixel electrode layer 4030 and the counter electrode layer 4031 can be
10 made of a light-transmitting conductive material such as indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium tin oxide (hereinafter referred to as ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added..

15 [0227]

A conductive composition containing a conductive high molecule (also referred to as a conductive polymer) can be used for forming the pixel electrode layer 4030 and the counter electrode layer 4031.It is preferable that the pixel electrode formed using a conductive composition have sheet resistance of 10000 Ω/square or less, and light
20 transmittance of greater than or equal to 70 % at a wavelength of 550 nm. Further, it is preferable that the conductive high molecule contained in the conductive composition have resistance of less than or equal to 0.1 Ω·cm.

[0228]

As the conductive high molecule, a so-called π electron conjugated conductive
25 high molecule can be used. For example, polyaniline and/or a derivative thereof, polypyrrole and/or a derivative thereof, polythiophene and/or a derivative thereof, and a copolymer of two or more kinds of those materials can be given.

[0229]

The variety of signals and potentials are supplied to the signal line driver
30 circuit 4003 that is formed separately, and the scan line driver circuit 4004 or the pixel portion 4002 from an FPC 4018.

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[0230]

In Embodiment 7, a connection terminal electrode 4015 is formed from the same conductive film as the pixel electrode layer 4030 included in the liquid crystal element 4013, and a terminal electrode 4016 is formed from the same conductive film
5 as source and drain electrode layers of the thin film transistors 4010 and 4011.

[0231]

The connection terminal electrode 4015 is electrically connected to a terminal included in the FPC 4018 through an anisotropic conductive film 4019.

[0232]

10 Although FIGS. 20A1 and 20A2 illustrate an example in which the signal line driver circuit 4003 is formed separately and mounted on the first substrate 4001, this embodiment is not limited to this structure. The scan line driver circuit may be formed separately and then mounted, or only a part of the signal line driver circuit or a part of the scan line driver circuit may be formed separately and then mounted.

15 [0233]

FIG. 21 illustrates an example of a liquid crystal display module which is formed as a semiconductor device by using a TFT substrate 2600.

[0234]

FIG. 21 shows an example of a liquid crystal display module, in which the TFT
20 substrate 2600 and a counter substrate 2601 are fixed to each other with a sealant 2602, and a pixel portion 2603 including a TFT and the like, a display element 2604 including a liquid crystal layer, a coloring layer 2605, and a polarizing plate 2606 are provided between the substrates to form a display region. A coloring layer 2605 is necessary to perform color display. In the case of the RGB system, respective coloring layers for
25 red, green, and blue colors are provided for respective pixels. Polarizing plates 2606 and 2607 and a diffuser plate 2613 are provided outside the TFT substrate 2600 and the counter substrate 2601. A light source includes a cold cathode tube 2610 and a reflective plate 2611, and a circuit substrate 2612 is connected to a wiring circuit portion 2608 of the TFT substrate 2600 through a flexible wiring board 2609 and includes an
30 external circuit such as a control circuit and a power source circuit. The polarizing plate and the liquid crystal layer may be stacked with a retardation film interposed therebetween.

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[0235]

The liquid crystal display module can use any of the following modes: a TN (Twisted Nematic) mode, an IPS (In-Plane-Switching) mode, an FFS (Fringe Field Switching) mode, an MVA (Multi-domain Vertical Alignment) mode, a PVA (Patterned 5 Vertical Alignment) mode, an ASM (Axially Symmetric aligned Micro-cell) mode, an OCB (Optical Compensated Birefringence) mode, an FLC (Ferroelectric Liquid Crystal) mode, an AFLC (AntiFerroelectric Liquid Crystal) mode, and the like.

[0236]

Through the above process, a liquid crystal display panel as a semiconductor 10 device can be manufactured at reduced cost.

[0237]

This embodiment can be implemented in appropriate combination with any of the structures described in Embodiments 1 to 3.

[Embodiment 8]

15 [0238]

Electronic paper can be used for electronic devices of a variety of fields as long as they display data. For example, an electronic paper can be applied to an e-book reader (electronic book), a poster, an advertisement in a vehicle such as a train, or displays of various cards such as a credit card. Examples of the electronic devices are 20 illustrated in FIGS. 23A and 23B and FIG. 24.

[0239]

FIG. 23A illustrates a poster 2631 formed using electronic paper. In the case where an advertising medium is printed paper, the advertisements are replaced by hands; however, by using electronic paper to which Embodiment 3 is applied, the 25 advertisements can be changed in a short period of time. Further, stable images can be obtained without display defects. The poster may have a configuration capable of wirelessly transmitting and receiving data.

[0240]

FIG. 23B illustrates an advertisement 2632 in a vehicle such as a train. In the 30 case where an advertising medium is printed paper, the advertisement is replaced by hands; however, by using electronic paper to which Embodiment 3 is applied, the advertising display can be changed in a short period of time with less manpower.

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Furthermore, stable images can be obtained without display defects. The poster may have a configuration capable of wirelessly transmitting and receiving data.

[0241]

FIG. 24 illustrates an example of an e-book reader 2700. For example, the e-book reader 2700 includes two housings, a housing 2701 and a housing 2703. The housing 2701 and the housing 2703 are combined with a hinge 2711 so that the e-book reader 2700 can be opened and closed with the hinge 2711 as an axis. With such a structure, the e-book reader 2700 can operate like a paper book.

[0242]

A display portion 2705 and a display portion 2707 are incorporated in the housing 2701 and the housing 2703, respectively. The display portion 2705 and the display portion 2707 may display one image or different images. In the case where the display portion 2705 and the display portion 2707 display different images, for example, a display portion on the right side (the display portion 2705 in FIG. 24) can display text and a display portion on the left side (the display portion 2707 in FIG. 24) can display graphics.

[0243]

FIG. 24 illustrates an example in which the housing 2701 is provided with an operation portion and the like. For example, the housing 2701 is provided with a power switch 2721, an operation key 2723, a speaker 2725, and the like. With the operation key 2723, pages can be turned. Note that a keyboard, a pointing device, and the like may be provided on the same surface as the display portion of the housing. Furthermore, an external connection terminal (an earphone terminal, a USB terminal, a terminal that can be connected to various cables such as an AC adapter and a USB cable, or the like), a recording medium insertion portion, and the like may be provided on the back surface or the side surface of the housing. Moreover, the e-book reader 2700 may have a function of an electronic dictionary.

[0244]

The e-book reader 2700 may have a configuration capable of wirelessly transmitting and receiving data. Through wireless communication, desired book data or the like can be purchased and downloaded from an electronic book server.

[Embodiment 9]

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[0245]

A semiconductor device according to one embodiment of the present invention can be applied to a variety of electronic devices (including an amusement machine). Examples of electronic devices include: television sets (also referred to as televisions or television receivers), monitor of computers or the like, cameras such as digital cameras or digital video cameras, digital photo frames, cellular phones (also referred to as mobile phones or mobile phone sets), portable game consoles, portable information terminals, audio reproducing devices, large-sized game machines such as pachinko machines, and the like.

[0246]

FIG. 25A illustrates an example of a television set 9600. In the television set 9600, a display portion 9603 is incorporated in a housing 9601. The display portion 9603 can display images. In FIG. 25A, the housing 9601 is supported by a stand 9605.

[0247]

The television set 9600 can be operated with an operation switch of the housing 9601 or a separate remote controller 9610. Channels and volume can be controlled with an operation key 9609 of the remote controller 9610 so that an image displayed on the display portion 9603 can be controlled. Furthermore, the remote controller 9610 may be provided with a display portion 9607 for displaying data output from the remote controller 9610.

[0248]

Note that the television set 9600 is provided with a receiver, a modem, and the like. With the use of the receiver, general television broadcasting can be received. Moreover, when the display device is connected to a communication network with or without wires via the modem, one-way (from a sender to a receiver) or two-way (between a sender and a receiver or between receivers) information communication can be performed.

[0249]

FIG. 25B illustrates an example of a digital photo frame 9700. For example, in the digital photo frame 9700, a display portion 9703 is incorporated in a housing 9701. Various images can be displayed on the display portion 9703.For example, the display portion 9703 can display data of an image shot by a digital camera or the like to

function as a normal photo frame.

[0250]

Note that the digital photo frame 9700 is provided with an operation portion, an external connection portion (a USB terminal, a terminal that can be connected to various cables such as a USB cable, or the like), a recording medium insertion portion, and the like. Although they may be provided on the same surface as the display portion, it is preferable to provide them on the side surface or the back surface for the design of the digital photo frame 9700. For example, a memory storing data of an image shot by a digital camera is inserted in the recording medium insertion portion of the digital photo frame, whereby the image data can be downloaded and displayed on the display portion 9703.

[0251]

The digital photo frame 9700 may transmit and receive data wirelessly. Through wireless communication, desired image data can be downloaded to be displayed.

[0252]

FIG. 26A is a portable game machine and includes two housings, a housing 9881 and a housing 9891, which are connected with a joint portion 9893 so that the portable game machine can be opened or folded. A display portion 9882 and a display portion 9883 are incorporated in the housing 9881 and the housing 9891, respectively. In addition, the portable game machine illustrated in FIG. 26A is provided with a speaker portion 9884, a recording medium insert portion 9886, an LED lamp 9890, input means (operation keys 9885, a connection terminal 9887, a sensor 9888 (having a function of measuring force, displacement, position, speed, acceleration, angular velocity, rotation number, distance, light, liquid, magnetism, temperature, chemical substance, sound, time, hardness, electric field, current, voltage, electric power, radial ray, flow rate, humidity, gradient, vibration, odor, or infrared ray), and a microphone 9889), and the like. It is needless to say that the structure of the portable amusement machine is not limited to the above as long as the structure is provided with at least a semiconductor device including the thin film transistor described in Embodiment 1 or 2. The portable amusement machine may include other accessory equipment as appropriate. The portable game machine illustrated in FIG. 26A has a function of

reading a program or data stored in a recording medium to display it on the display portion, and a function of sharing information with another portable game machine by wireless communication. Note that the function of the portable game machine illustrated in FIG. 26A is not limited to those described above, and the portable game
5 machine can have a variety of functions.

[0253]

FIG. 26B illustrates an example of a slot machine 9900 which is a large-sized amusement machine. In the slot machine 9900, a display portion 9903 is incorporated in a housing 9901. In addition, the slot machine 9900 includes an operation means
10 such as a start lever or a stop switch, a coin slot, a speaker, and the like. It is needless to say that the structure of the slot machine 9900 is not limited to the above as long as the structure is provided with at least a semiconductor device including the thin film transistor described in Embodiment 1 or 2. The slot machine 9900 may include other accessory equipment as appropriate.

15 [0254]

FIG. 27 illustrates an example of a mobile phone 1000. The mobile phone 1000 is provided with a display portion 1002 incorporated in a housing 1001, operation buttons 1003, an external connection port 1004, a speaker 1005, a microphone 1006, and the like.

20 [0255]

When the display portion 1002 of the mobile phone 1000 illustrated in FIG. 27 is touched with a finger or the like, data can be input into the mobile phone 1000. Furthermore, operations such as making calls and composing mails can be performed by touching the display portion 1002 with a finger or the like.

25 [0256]

There are mainly three screen modes of the display portion 1002. The first mode is a display mode mainly for displaying an image. The second mode is an input mode mainly for inputting information such as text. The third mode is a display-and-input mode in which two modes of the display mode and the input mode
30 are mixed.

[0257]

For example, in the case of making a call or composing a mail, a text input

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mode mainly for inputting text is selected for the display portion 1002 so that text displayed on a screen can be input. In that case, it is preferable to display a keyboard or number buttons on almost all the area of the screen of the display portion 1002.

[0258]

5 When a detection device including a sensor for detecting inclination, such as a gyroscope or an acceleration sensor, is provided inside the mobile phone 1000, display on the screen of the display portion 1002 can be automatically switched by determining the direction of the mobile phone 1000 (whether the mobile phone 1000 is placed horizontally or vertically for a landscape mode or a portrait mode).

10 [0259]

The screen mode is switched by touching the display portion 1002 or operating the operation buttons 1003 of the housing 1001. Alternatively, the screen modes can be switched depending on kinds of images displayed in the display portion 1002. For example, when a signal for an image displayed in the display portion is data of moving

15 images, the screen mode is switched to the display mode, and whereas when the signal is text data, the screen mode is switched to the input mode.

[0260]

Moreover, in the input mode, when input by touching the display portion 1002 is not performed within a specified period while a signal detected by the optical sensor

20 in the display portion 1002 is detected, the screen mode may be controlled so as to be switched from the input mode to the display mode.

[0261]

The display portion 1002 can also function as an image sensor. For example, an image of a palm print, a fingerprint, or the like is taken by touching the display

25 portion 1002 with the palm or the finger, whereby personal authentication can be performed. Furthermore, by providing a backlight or a sensing light source emitting a near-infrared light for the display portion, an image of a finger vein, a palm vein, or the like can also be taken.

[Embodiment 10]

30 [0262]

The examples in which a buffer layer is provided are described in Embodiments 1 and 2. In this embodiment, an example in which a buffer layer is not

provided will be described. Further, an example in which an inverter circuit is formed using two n-channel thin film transistors will be described below.

[0263]

A driver circuit for driving a pixel portion is formed using an inverter circuit, a capacitor, a resistor, and the like. When two n-channel TFTs are combined to form an inverter circuit, there are two types of combinations: a combination of an enhancement type transistor and a depletion type transistor (hereinafter, a circuit formed by such a combination is referred to as an "EDMOS circuit") and a combination of enhancement type TFTs (hereinafter, a circuit formed by such a combination is referred to as an "EEMOS circuit"). Note that when the threshold voltage of the n-channel TFT is positive, the n-channel TFT is defined as an enhancement type transistor, while when the threshold voltage of the n-channel TFT is negative, the n-channel TFT is defined as a depletion type transistor, and this specification follows the above definitions.

[0264]

The pixel portion and the driver circuit are formed over the same substrate. In the pixel portion, ON/OFF of voltage application to a pixel electrode is switched using enhancement type transistors arranged in a matrix. An oxide semiconductor is used for these enhancement type transistors arranged in the pixel portion. Since the enhancement type transistor has electric characteristics such as an on/off ratio of greater than or equal to 10^9 at a gate voltage of $\pm$ 20 V, leakage current is small and low power consumption drive can be realized.

[0265]

FIG. 32A illustrates a cross-sectional structure of the inverter circuit of the driver circuit. In FIG. 32A, a first gate electrode 1401 and a second gate electrode 1402 are provided over a substrate 1400. The first gate electrode 1401 and the second gate electrode 1402 each can be formed to have a single-layer structure or a stacked-layer structure using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material containing any of these materials as its main component.

[0266]

For example, as a two-layer structure of each of the first gate electrode 1401 and the second gate electrode 1402, the following structures are preferable: a two-layer

structure of an aluminum layer and a molybdenum layer stacked thereover, a two-layer structure of a copper layer and a molybdenum layer stacked thereover, a two-layer structure of a copper layer and a titanium nitride layer or a tantalum nitride layer stacked thereover, and a two-layer structure of a titanium nitride layer and a molybdenum layer. As a three-layer structure, a stack of a tungsten layer or a tungsten nitride layer, a layer of an alloy of aluminum and silicon or an alloy of aluminum and titanium, and a titanium nitride layer or a titanium layer is preferable.

[0267]

Further, a first wiring 1409, a second wiring 1410, and a third wiring 1411 are provided over a gate insulating layer 1403 that covers the first gate electrode 1401 and the second gate electrode 1402. The second wiring 1410 is directly connected to the second gate electrode 1402 through a contact hole 1404 formed in the gate insulating layer 1403.

[0268]

Further, a first oxide semiconductor layer 1405 which is on and in contact with the first wiring 1409 and the second wiring 1410 is provided at a position overlapping with the first gate electrode 1401, and a second oxide semiconductor layer 1407 which is on and in contact with the second wiring 1410 and the third wiring 1411 is provided at a position overlapping with the second gate electrode 1402.

[0269]

A first thin film transistor 1430 includes the first gate electrode 1401 and the first oxide semiconductor layer 1405 that overlaps with the first gate electrode 1401 with the gate insulating layer 1403 interposed therebetween, and the first wiring 1409 is a power supply line at a ground potential (a ground power supply line). This power supply line at a ground potential may be a power supply line to which a negative voltage VDL is applied (a negative power supply line).

[0270]

In addition, the second thin film transistor 1431 includes the second gate electrode 1402 and the second oxide semiconductor layer 1407 overlapped with the second gate electrode 1402 with the gate insulating layer 1403 interposed therebetween, and the third wiring 1411 is a power supply line to which a positive voltage VDD is applied (a positive power supply line).

[0271]

Tapered shapes of the side surfaces of the first wiring 1409 and the second wiring 1410 which face each other with the first oxide semiconductor layer 1405 interposed therebetween enable respective regions of the oxide semiconductor layer, 5 which overlap with the side surfaces of the source electrode layer and the drain electrode layer to function as electric-field relaxation regions.

[0272]

Further, tapered shapes of the side surfaces of the second wiring 1410 and the third wiring 1411 which face each other with the second oxide semiconductor layer 10 1407 interposed therebetween enable respective regions of the oxide semiconductor layer, which overlap with the side surfaces of the source electrode layer and the drain electrode layer to function as electric-field relaxation regions.

[0273]

As illustrated in FIG. 32A, the second wiring 1410 which is electrically 15 connected to both the first oxide semiconductor layer 1405 and the second oxide semiconductor layer 1407 is directly connected to the second gate electrode 1402 of the second thin film transistor 1431 through the contact hole 1404 formed in the gate insulating layer 1403. The second wiring 1410 and the second gate electrode 1402 are directly connected to each other, whereby favorable contact can be obtained, which 20 leads to reduction in contact resistance. In comparison with the case where the second gate electrode 1402 and the second wiring 1410 are connected to each other with another conductive film, e.g., a transparent conductive film interposed therebetween, a reduction in the number of contact holes and a reduction in an area occupied by the driver circuit by the reduction in the number of contact holes can be achieved.

25 [0274]

Further, FIG. 32C is a top view of the inverter circuit of the driver circuit. A cross section taken along chain line Z1-Z2 of FIG. 32C corresponds to FIG. 32A.

[0275]

Further, FIG. 32B illustrates an equivalent circuit of the EDMOS circuit. The 30 circuit connection illustrated in FIGS. 32A and 32C corresponds to that illustrated in FIG. 32B. Illustrated is an example in which the first thin film transistor 1430 is an enhancement-type n-channel transistor and the second thin film transistor 1431 is a

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depletion-type n-channel transistor.

[0276]

Although the example of an EDMOS circuit is described in this embodiment, the driver circuit may be formed using an EEMOS circuit in which enhancement-type n-channel transistors are used.

[0277]

Further, although the example in which a buffer layer is not provided is described in this embodiment, the present invention is not limited thereto and a buffer layer may be provided over the first wiring 1409, the second wiring 1410, and the third wiring 1411 like in Embodiment 1.

[0278]

This embodiment can be freely combined with any one of Embodiments 1 to 9.

[Embodiment 11]

[0279]

In Embodiment 11, the degradation of electrical characteristics of thin film transistors having model structures shown in FIGS. 33A to 33C when stress is applied was calculated.

[0280]

In a structure shown in FIG. 33A, a gate electrode layer 302 and a gate insulating layer 303 are stacked over a glass substrate 301 in this order, and a source electrode layer 304 and a drain electrode layer 305 are formed thereover. An oxide layer 307 and an oxide layer 308 are provided on the side surface of the source electrode layer 304 and the side surface of the drain electrode layer 305 respectively. The oxide layers 307 and 308 here are respective native oxide films of the source electrode layer 304 and the drain electrode layer 305. An oxide semiconductor layer 306 is formed to cover the source electrode layer 304, the drain electrode layer 305, and the oxide layers 307 and 308.

[0281]

In this embodiment, the gate electrode layer 302 was formed using molybdenum, and the source electrode layer 304 and the drain electrode layer 305 were formed using the same material as the gate electrode layer 302. The gate insulating layer 303 was a silicon oxide film, and thickness thereof was 100 nm and relative

permittivity εr thereof was 4.1. The thickness of the oxide semiconductor layer 306 was 50 nm and a material thereof was an In-Ga-Zn-O-based non-single-crystal film. Channel length L of the thin film transistor was 10 μm and channel width W thereof was 10 μm.

5 [0282]

As for the stress which was applied to the thin film transistor, gate voltage Vgs was set to 2 V and source-drain voltage Vds was set to 20 V. The period of time during which the stress is applied was 1000 seconds, and the electrical characteristics before and after the stress application were compared to each other.

10 [0283]

Device simulator "Atlas" made by Silvaco was used for the calculation.

[0284]

Further, the calculation was performed in the respective cases where the taper angles θ1 of the source electrode layer 304 are 27°, 45°, and 63°. The taper angle θ1

15 of the source electrode layer 304 was set to be the same angle as the taper angle θ2 of the drain electrode layer 305.

[0285]

Calculation results in the case where the taper angle θ1 of the source electrode layer 304 is 27° are shown in FIG. 34.

20 [0286]

Calculation results in the case where the taper angle θ1 of the source electrode layer 304 is 45° are shown in FIG. 35.

[0287]

Calculation results in the case where the taper angle θ1 of the source electrode

25 layer 304 is 63° are shown in FIG. 36.

[0288]

From these results of FIGS. 34 to 36, such result that the degradation becomes smaller as the taper angle θ1 of the source electrode layer 304 is smaller can be obtained.

30 [0289]

For comparison, the result of the calculation which was performed in the

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similar manner on a structure shown in FIG. 33B where taper angle θ1 is 90° is shown in FIG. 37A. The structure shown in FIG. 33B is the same as the structure shown in FIG. 33A except that the taper angle θ1 is different from that in FIG. 33A.

[0290]

5 Furthermore, for comparison, the result of the calculation which was performed in the similar manner on a structure shown in FIG. 33C where taper angle θ1 is 27° and no oxide layer is formed on the side surface of each of a source electrode layer 304 and a drain electrode layer 305 is shown in FIG. 37B. Changing of the taper angle θ1 made no difference in the results as long as there is no oxide layer on the side surface of each 10 electrode layer. In the case where there is no oxide layer on the side surface of each electrode layer, the interface between the gate insulating layer 303 and the oxide semiconductor layer 306 corresponds to a current path, and therefore, the taper angle of the side surface of the source electrode layer 304 does not affect the current path.

[0291]

15 From these results, it can be said that degradation of the electrical characteristics of the thin film transistor can be suppressed by providing the oxide layer 307 and the oxide layer 308 on the respective side surfaces of the source electrode layer 304 and the drain electrode layer 305 and setting the taper angle θ1 to be smaller than 90°.

20 [0292]

The embodiments described above will be described in more detail in examples below.

[Example 1]

[0293]

25 In this example, characteristics of a thin film transistor manufactured using an oxide semiconductor layer will be described.

[0294]

The method for manufacturing a transistor used in this example will be described below.

30 [0295]

First, a first conductive film was formed over a substrate and patterned by a

photolithography method to form a gate electrode 502. Then, a gate insulating layer 503 was formed over the gate electrode 502. Then, a second conductive film and a buffer layer were formed over the gate insulating layer 503. The second conductive film and the buffer layer were formed successively without exposing the substrate to the
5 air. Then, the second conductive film and the buffer layer were patterned by a photolithography method, so that a source electrode layer 506a and a drain electrode layer 506b respective parts of which overlap with the gate electrode were formed. Then, an oxide semiconductor layer was formed over the gate insulating layer, the source electrode layer, and the drain electrode layer and patterned by a photolithography
10 method to form an island-shaped oxide semiconductor layer 510 which functions as a channel formation region. Then, thermal treatment at 350 °C for 1 hour was performed under a nitrogen atmosphere.

[0296]

As the substrate, a glass substrate manufactured by ASAHI GLASS CO., LTD.
15 (product name: AN 100) was used.

[0297]

As the first conductive film for forming the gate electrode 502, a tungsten film with a thickness of 100 nm was formed by a sputtering method.

[0298]

20 As the gate insulating layer 503, a silicon oxynitride film with a thickness of 100 nm was formed by a plasma CVD method.

[0299]

As the second conductive film for forming the source electrode layer 506a and the drain electrode layer 506b, a tungsten film with a thickness of 100 nm was formed
25 by a sputtering method.

[0300]

As the buffer layer, an In-Ga-Zn-O-based non-single-crystal film with a thickness of 5 to 10 nm was formed by a sputtering method. As for the film deposition condition, only an argon gas was used and a target in which In_2O_3:Ga_2O_3:ZnO = 1:1:1
30 was used.

[0301]

As the oxide semiconductor layer, an In-Ga-Zn-O-based non-single-crystal film

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with a thickness of 150 nm was formed by a sputtering method. The film deposition condition was as follows: the pressure was 0.4 Pa, the power was 500 W, the film deposition temperature was 25 °C, the argon gas flow rate was 10 sccm, the oxygen flow rate was 5 sccm, the distance between the glass substrate and the target was 170
5 mm, and a direct-current (DC) power source was used. As the target, a target in which $In_2O_3:Ga_2O_3:ZnO$ = 1:1:1 (In:Ga:Zn = 1:1:0.5) was used. After a plasma treatment was performed, the oxide semiconductor layer was formed successively without exposing a substrate 500 to the air. From the measurement with inductively coupled plasma mass spectrometry (ICP-MS), the composition of the oxide semiconductor layer
10 obtained by this film deposition condition was $InGa_{0.94}Zn_{0.40}O_{3.31}$.

[0302]

FIG. 28 is a graph showing a V_g-I_d curve of a thin film transistor. In this example, the drain voltage (a voltage which is applied to the drain with respect to a voltage which is applied to the source) was set to 1 V for the measurement.

15 [0303]

In this example also, the structure of the transistor was as follows, which is shown in FIG. 29. In specific, channel length L of the transistor was set to 100 μm, channel width W of the transistor was set to 100 μm, length Ls where the source electrode layer 506a and the gate electrode 502 overlap with each other was set to 5 μm,
20 length Ld where the drain electrode layer 506b and the gate electrode 502 overlap with each other was set to 5 μm, and each length A where the oxide semiconductor layer 510 does not overlap with either the source electrode layer 506a or the drain electrode layer 506b in the direction which is parallel to the channel width was set to 5 μm.

[0304]

25 Through the above, it was found that the successive formation of the second conductive film and the buffer layer without exposing the substrate to the air enables the on/off ratio of the transistor to be increased and the electron field-effect mobility to be increased.

[Example 2]

30 [0305]

In this example, one example of the electrode shape after etching will be

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described. First, the process for manufacturing a sample will be described using FIGS. 30A to 30C. The sample is different from the thin film transistor described in Example 1 only in the cross-sectional shape of each of a source electrode layer and a drain electrode layer and in that a buffer layer is not formed, and will be described using the
5 same reference numerals for the same portions as those of the thin film transistor described in Example 1.

[0306]

First, a first conductive film was formed over a substrate and patterned by a photolithography method to form a gate electrode 502. Then, a gate insulating layer
10 503 was formed over the gate electrode 502 (see FIG. 30A). Then, a second conductive film was formed over the gate insulating layer 503. Then, the second conductive film was patterned by a photolithography method, so that a source electrode layer 606a and a drain electrode layer 606b respective parts of which overlap with the gate electrode were formed (see FIG. 30B). Then, an oxide semiconductor layer was
15 formed over the gate insulating layer, the source electrode layer, and the drain electrode layer and patterned by a photolithography method to form an island-shaped oxide semiconductor layer 610 which functions as a channel formation region was formed (see FIG. 30C).

[0307]

20 As the substrate, a glass substrate manufactured by ASAHI GLASS CO., LTD. (product name: AN 100) was used.

[0308]

As the first conductive film for forming the gate electrode 502, a tungsten film with a thickness of 100 nm was formed by a sputtering method.

25 [0309]

As the gate insulating layer 503, a silicon oxynitride film with a thickness of 100 nm was formed by a plasma CVD method.

[0310]

As the second conductive film for forming the source electrode layer 606a and
30 the drain electrode layer 606b, a tungsten film with a thickness of 100 nm was formed by a sputtering method.

[0311]

As the oxide semiconductor layer, an In-Ga-Zn-O-based non-single-crystal film with a thickness of 150 nm was formed by a sputtering method. The film deposition condition thereof was the same as that in Example 1.

[0312]

5 The source electrode layer 606a and the drain electrode layer 606b were etched by using an ICP etching apparatus using a coiled antenna. The etching was performed by generating plasma under the following condition: the gas flow rate of CF_4 was set to 25 sccm, the gas flow rate of Cl_3 was set to 25 sccm, the gas flow rate of O_2 was set to 10 sccm, and an RF (13.56 MHz) power of 500 W was applied to a coiled electrode at a

10 pressure of 1.5 Pa. An RF (13.56 MHz) power of 10 W was applied to the substrate side (sample stage), which means that a negative self-bias voltage was substantially applied thereto. This etching was stopped when at least the gate insulating film 503 is exposed to some extent, thereby forming the side surface of the electrode, which has a step.

15 [0313]

By the above etching condition, with respect to the cross-sectional shape of the source electrode layer 606a, the angle θ1 formed between the surface of the substrate and the bottom edge of the side surface of the source electrode layer 606a can be made to be greater than or equal to 20° and less than 90°. The cross-sectional photograph of

20 the portion surrounded by a dotted line in FIG. 30C is FIG. 31A. FIG. 31B is a pattern diagram of FIG. 31A. As shown in FIG. 31A, θ1 was about 40°. Further, as shown in FIG. 31A, the angle formed between the surface of the substrate and the top edge of the side surface of the source electrode layer 606a was about 90°. The cross section of the side surface of the source electrode layer 606a and that of the side surface of the drain

25 electrode layer 606b, which face each other with the oxide semiconductor layer 610 interposed therebetween have substantially the same shape as each other because the same etching step is performed thereon.

[0314]

From this example, it can be said that it can be suggested that the

30 cross-sectional shape of each of the source electrode layer and the drain electrode layer described in Embodiment 2 is manufactured.

This application is based on Japanese Patent Application serial no. 2008-287187 filed with Japan Patent Office on November 7, 2008, the entire contents of which are hereby incorporated by reference.

BLUEHOUSE EXHIBIT 1002 CONTINUED
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WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a gate electrode formed over a substrate having an insulating surface;

5 an insulating layer formed over the gate electrode;

a source and drain electrodes formed over the insulating layer; and

an oxide semiconductor layer formed between a side surface of the source electrode and a side surface of the drain electrode, which face each other, so as to overlap with the gate electrode with the insulating layer interposed therebetween,

10 wherein the oxide semiconductor layer is in contact with at least the respective side surfaces of the source and drain electrodes, and

wherein a first angle formed between a surface of the substrate and the side surface of the source electrode and a second angle formed between the surface of the substrate and the side surface of the drain electrode are each greater than or equal to 20°

15 and less than 90°.

ABSTRACT OF THE DISCLOSURE

A structure by which electric-field concentration which might occur between a source electrode and a drain electrode in a bottom-gate thin film transistor is relaxed and
5 deterioration of the switching characteristics is suppressed, and a manufacturing method thereof. A bottom-gate thin film transistor in which an oxide semiconductor layer is provided over a source and drain electrodes is manufactured, and angle $\theta 1$ of the side surface of the source electrode which is in contact with the oxide semiconductor layer and angle $\theta 2$ of the side surface of the drain electrode which is in contact with the oxide
10 semiconductor layer are each set to be greater than or equal to 20° and less than 90°, so that the distance from the top edge to the bottom edge in the side surface of each electrode is increased.

FIG. 1

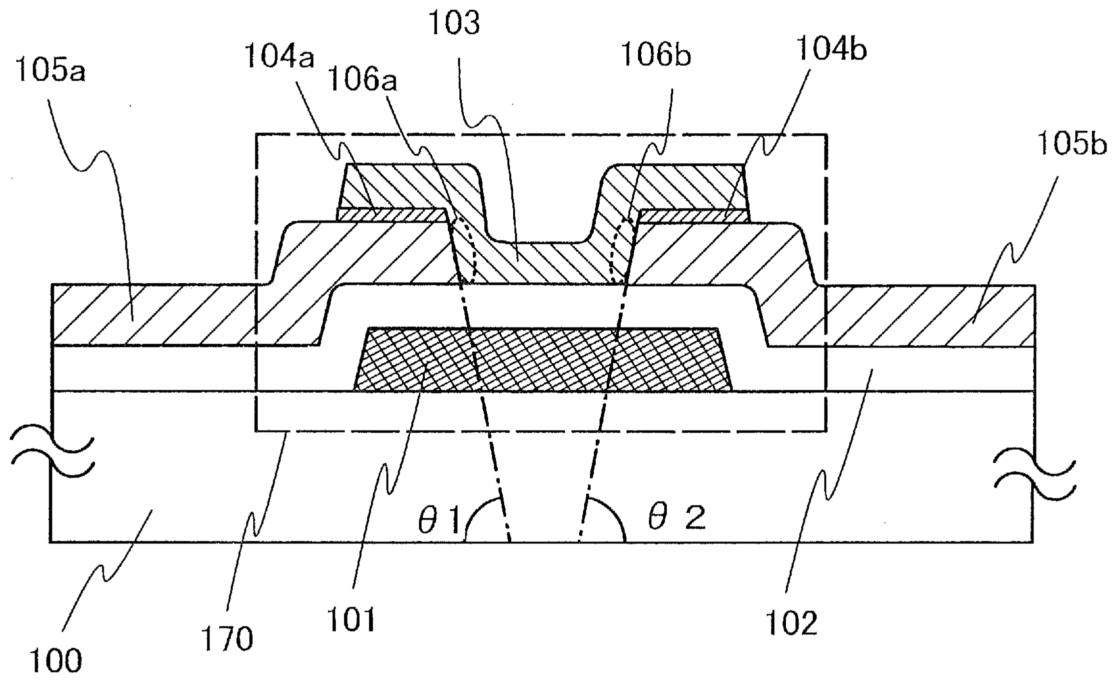
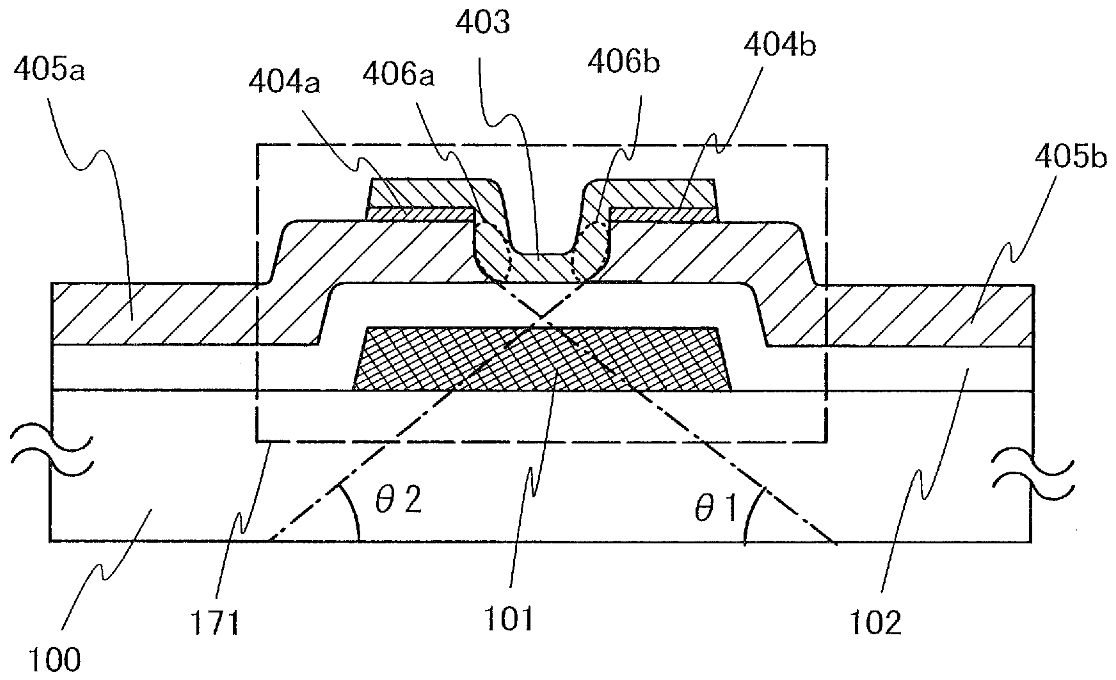


FIG. 2



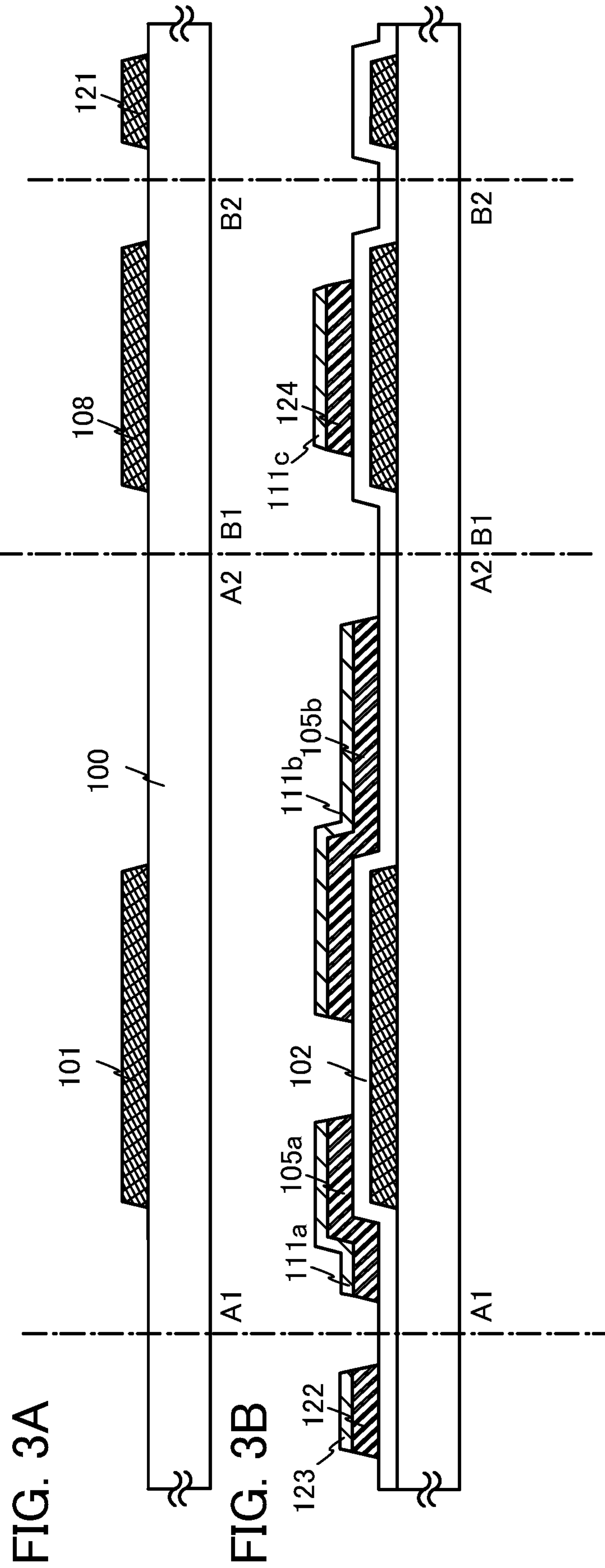


FIG. 3A
FIG. 3B
100
101
108
121
A1
A2
B1
B2
102
105a
105b
111a
111b
111c
122
123
124

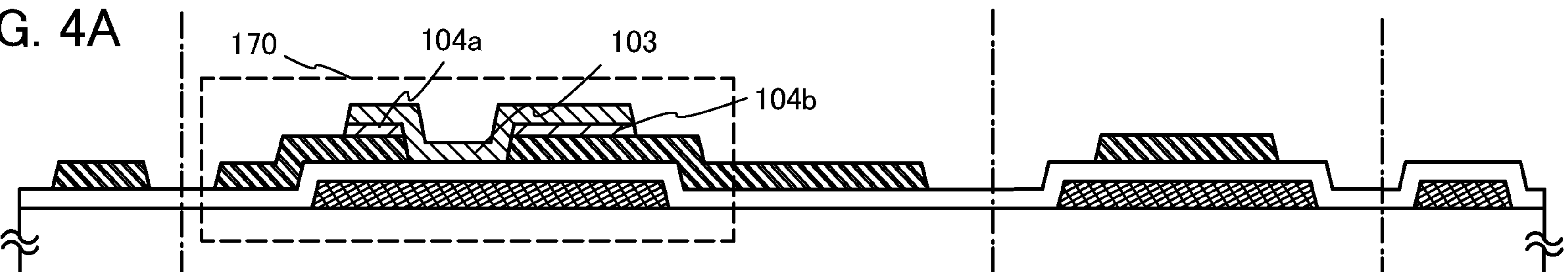


FIG. 4A
170
104a
103
104b
A1
A2
B1
B2

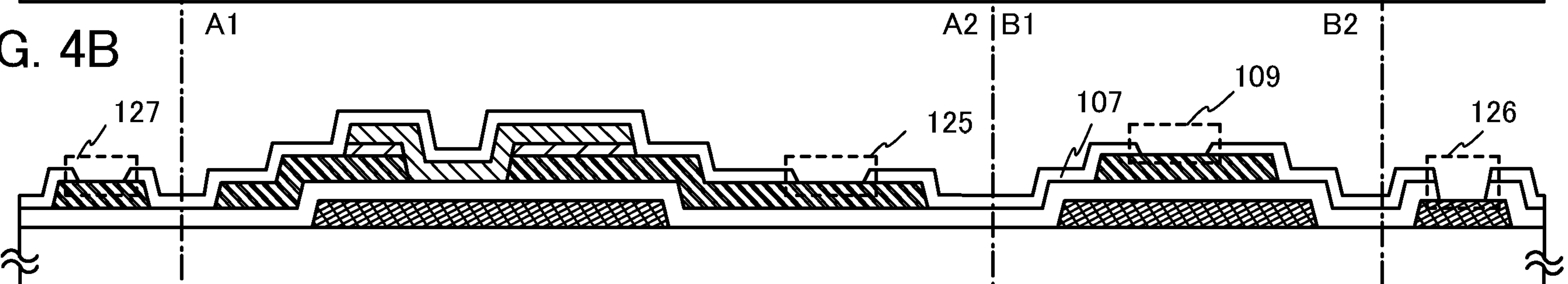


FIG. 4B
127
125
107
109
126
A1
A2
B1
B2

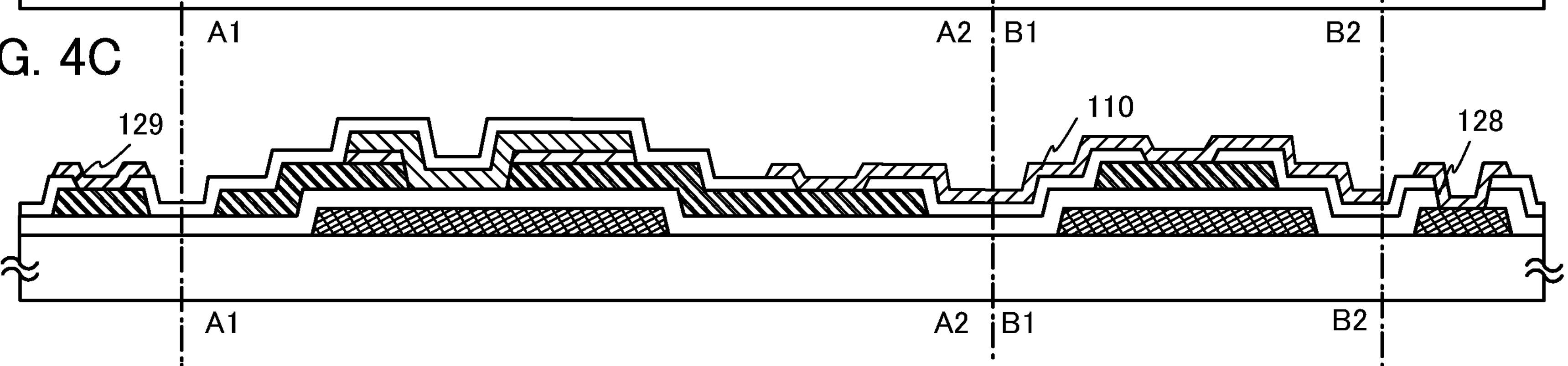


FIG. 4C
129
110
128
A1
A2
B1
B2

FIG. 5

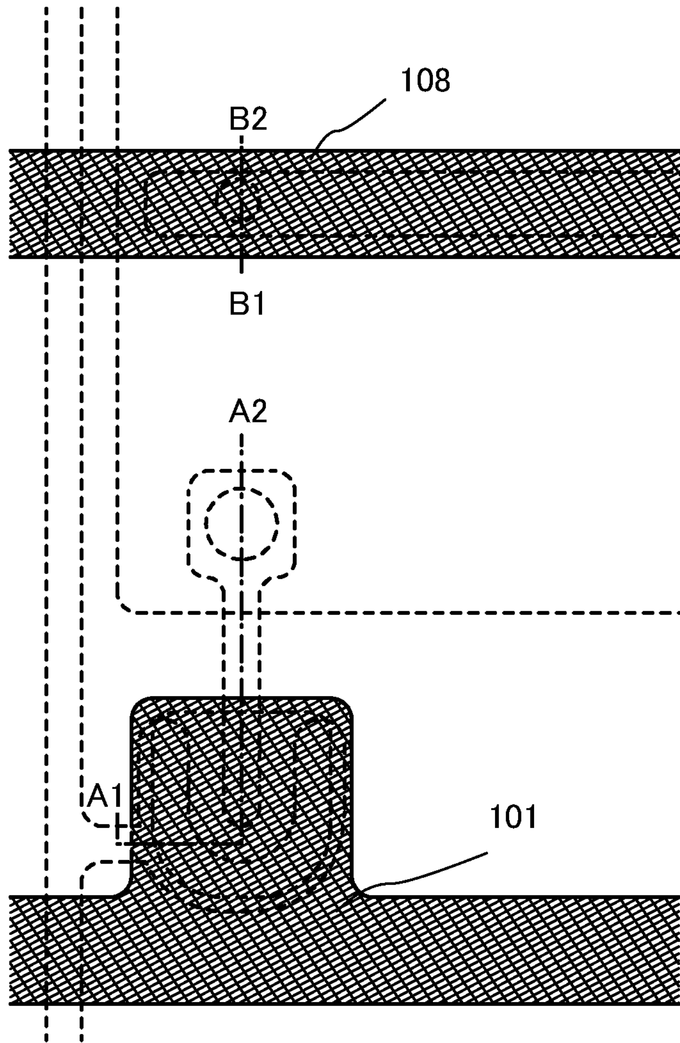


FIG. 6

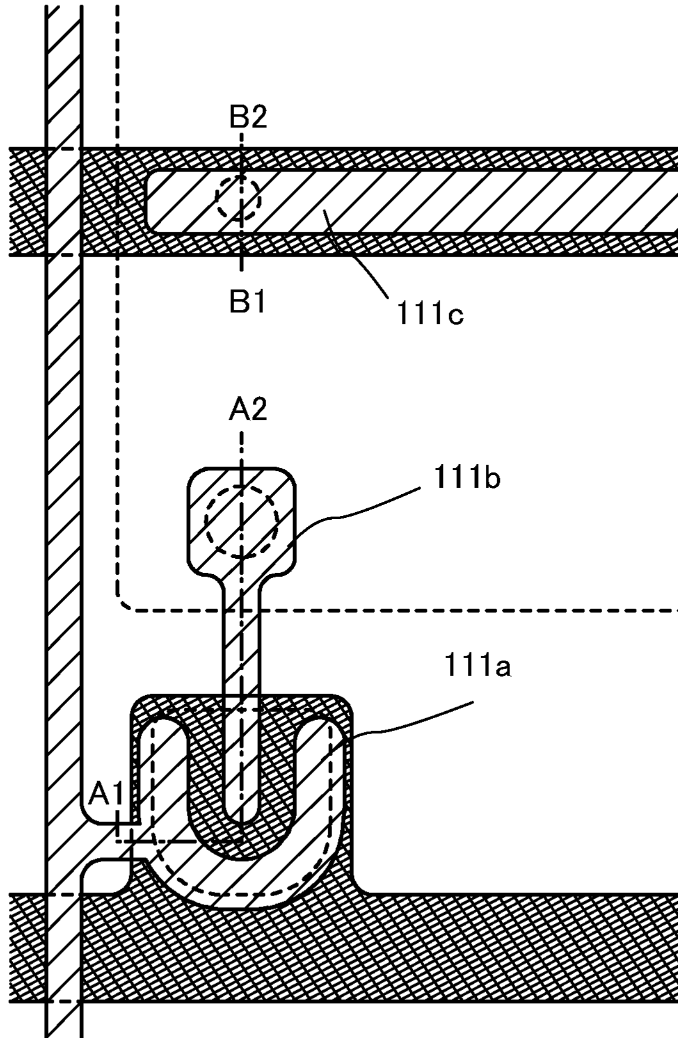


FIG. 7

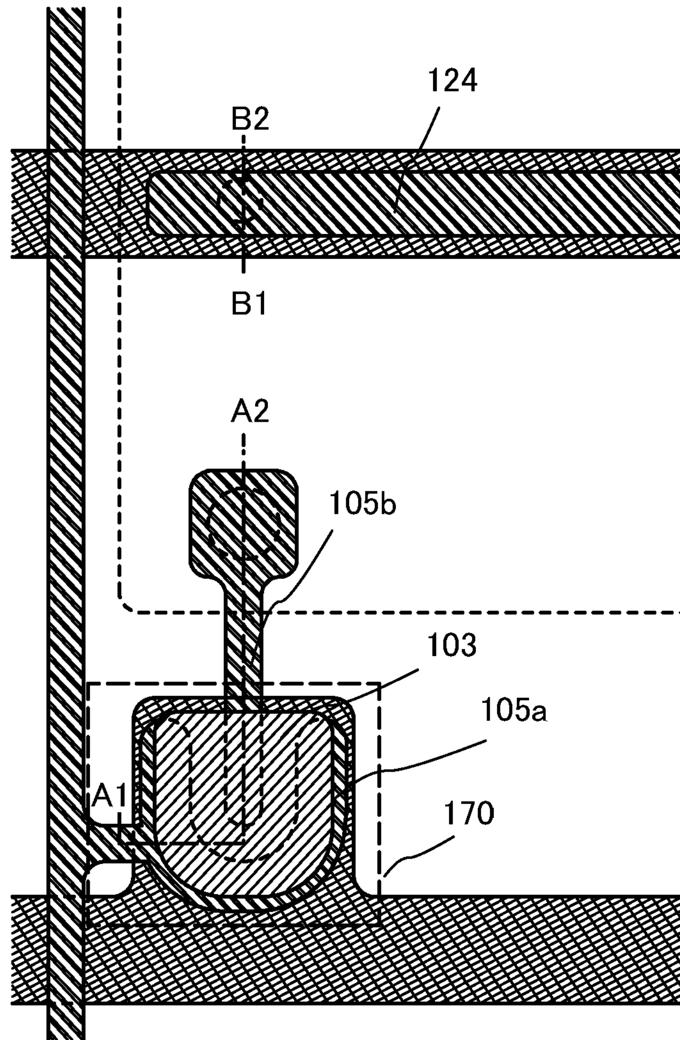


FIG. 8

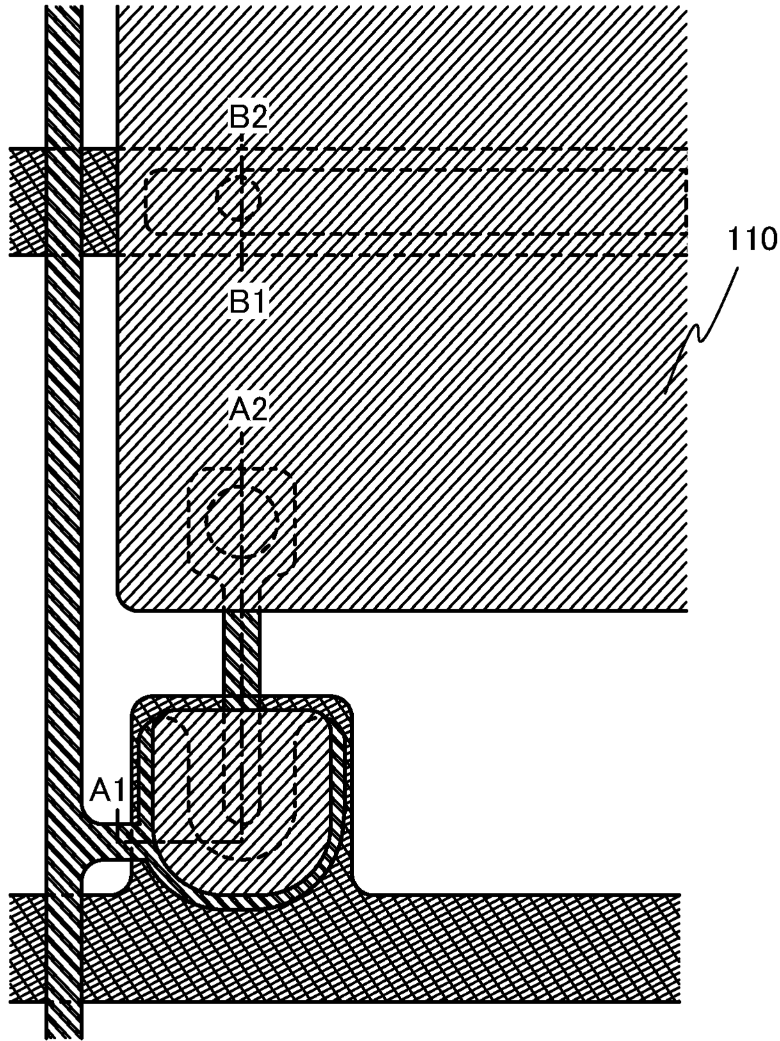


FIG. 9A1

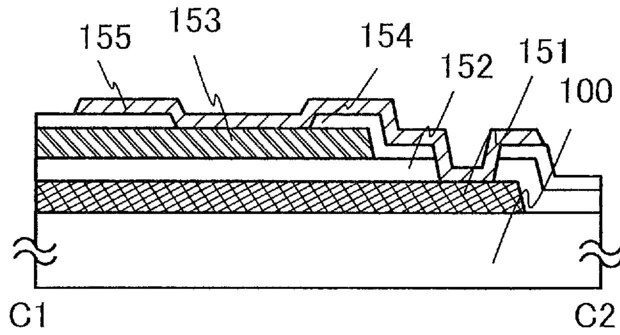


FIG. 9A2

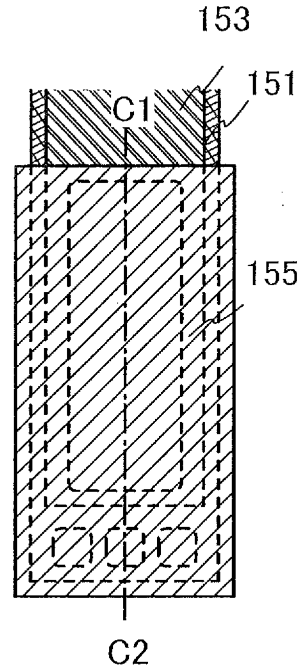


FIG. 9B1

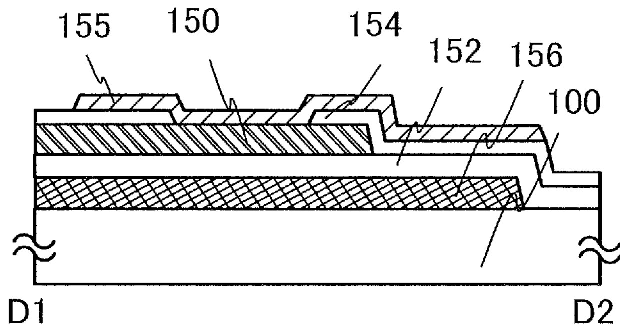


FIG. 9B2

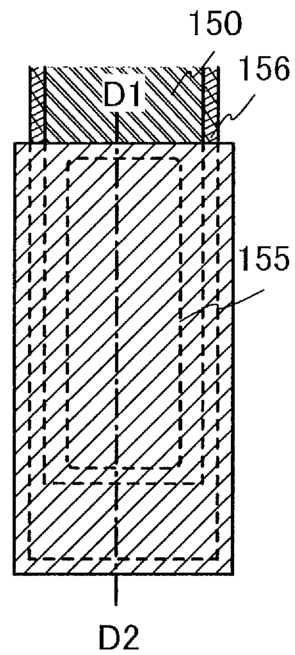


FIG. 10

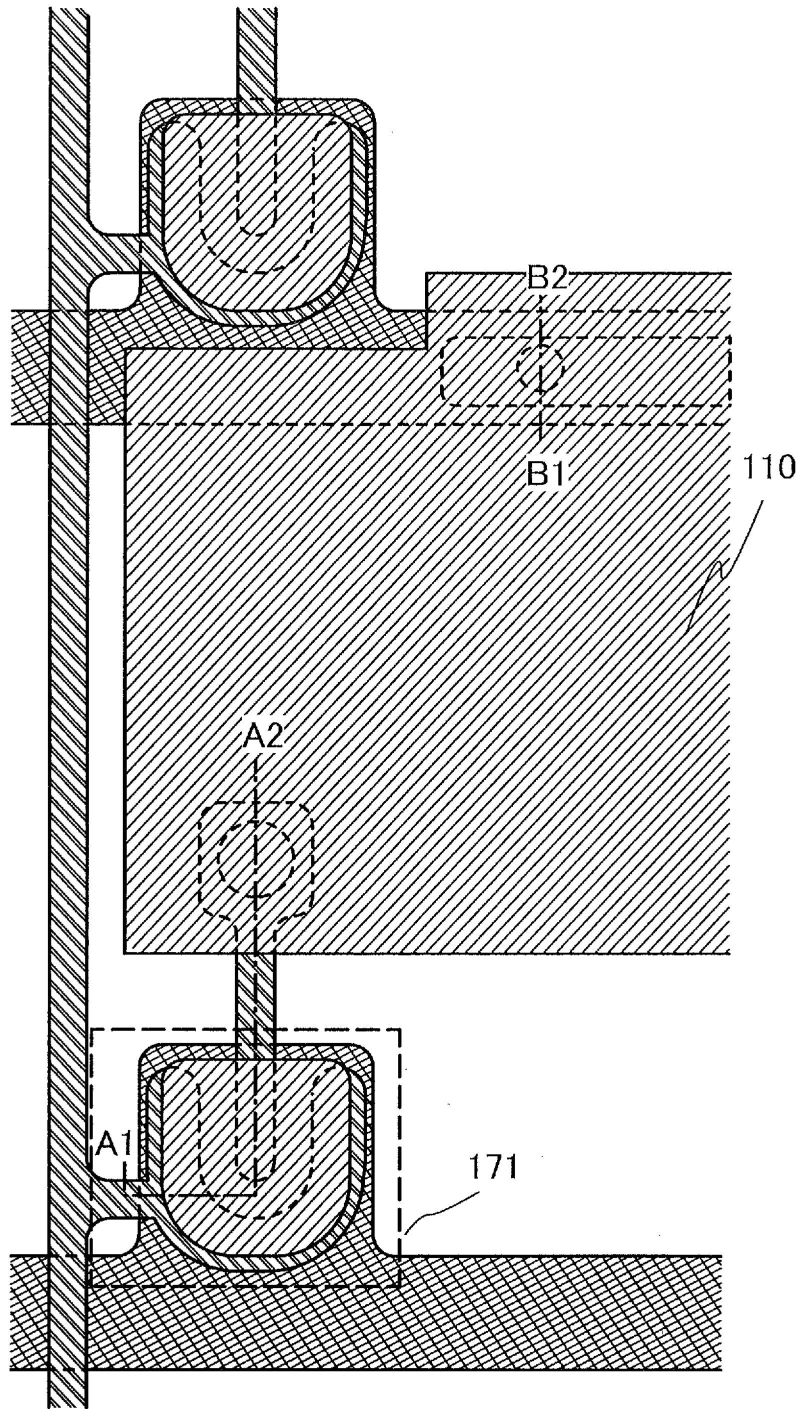


FIG. 11

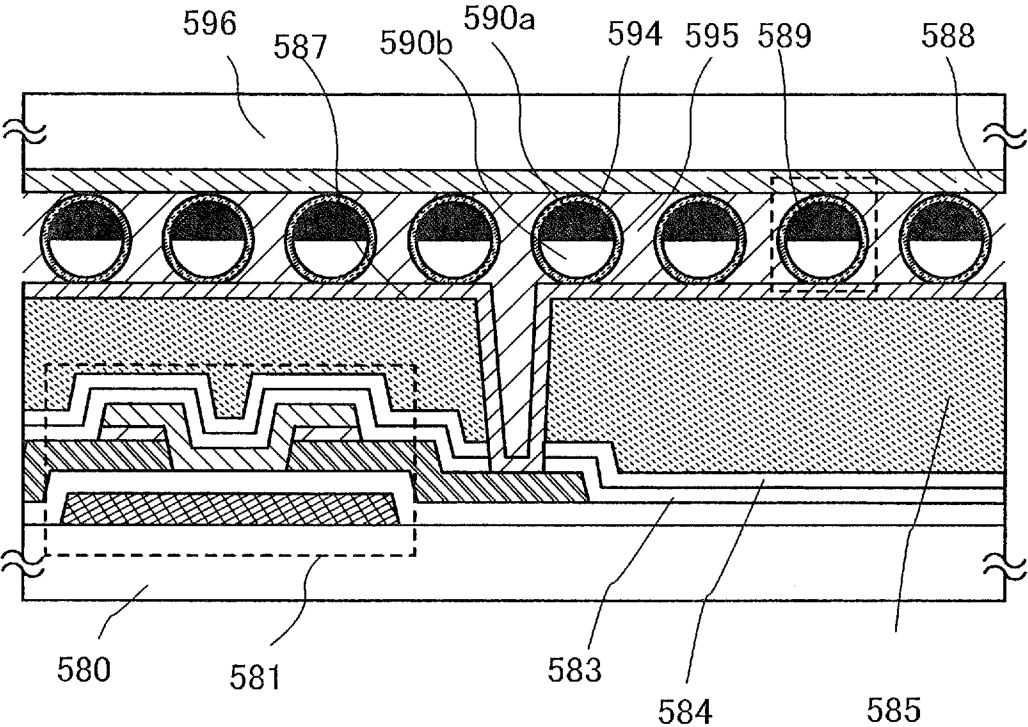


FIG. 12A

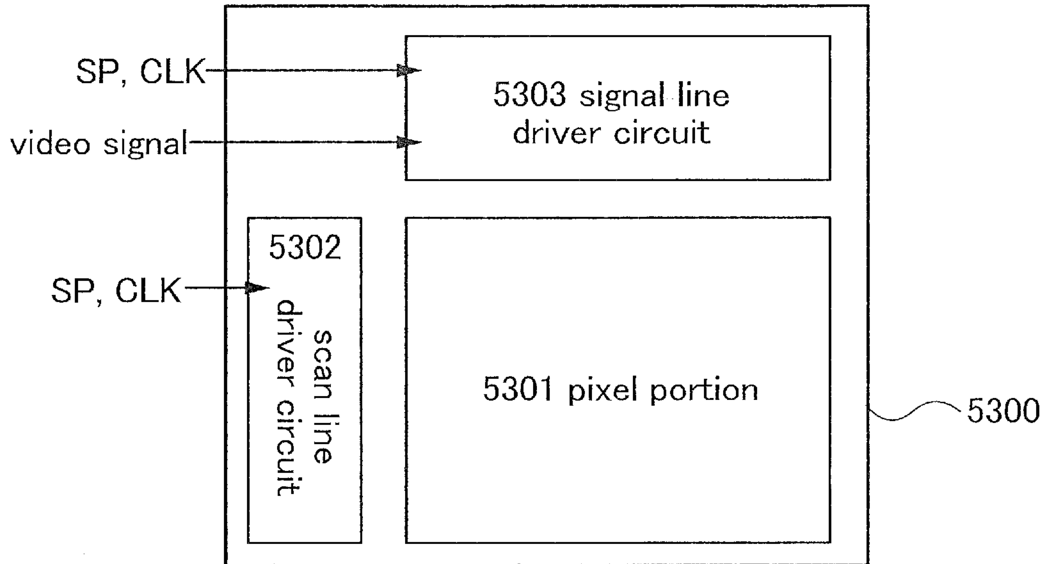


FIG. 12B

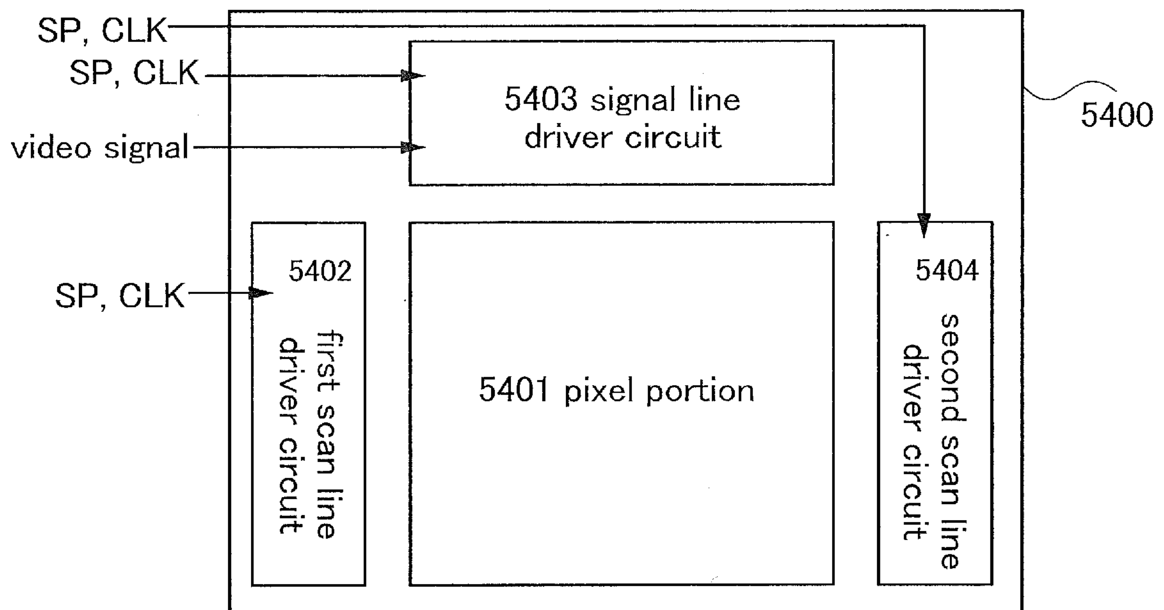
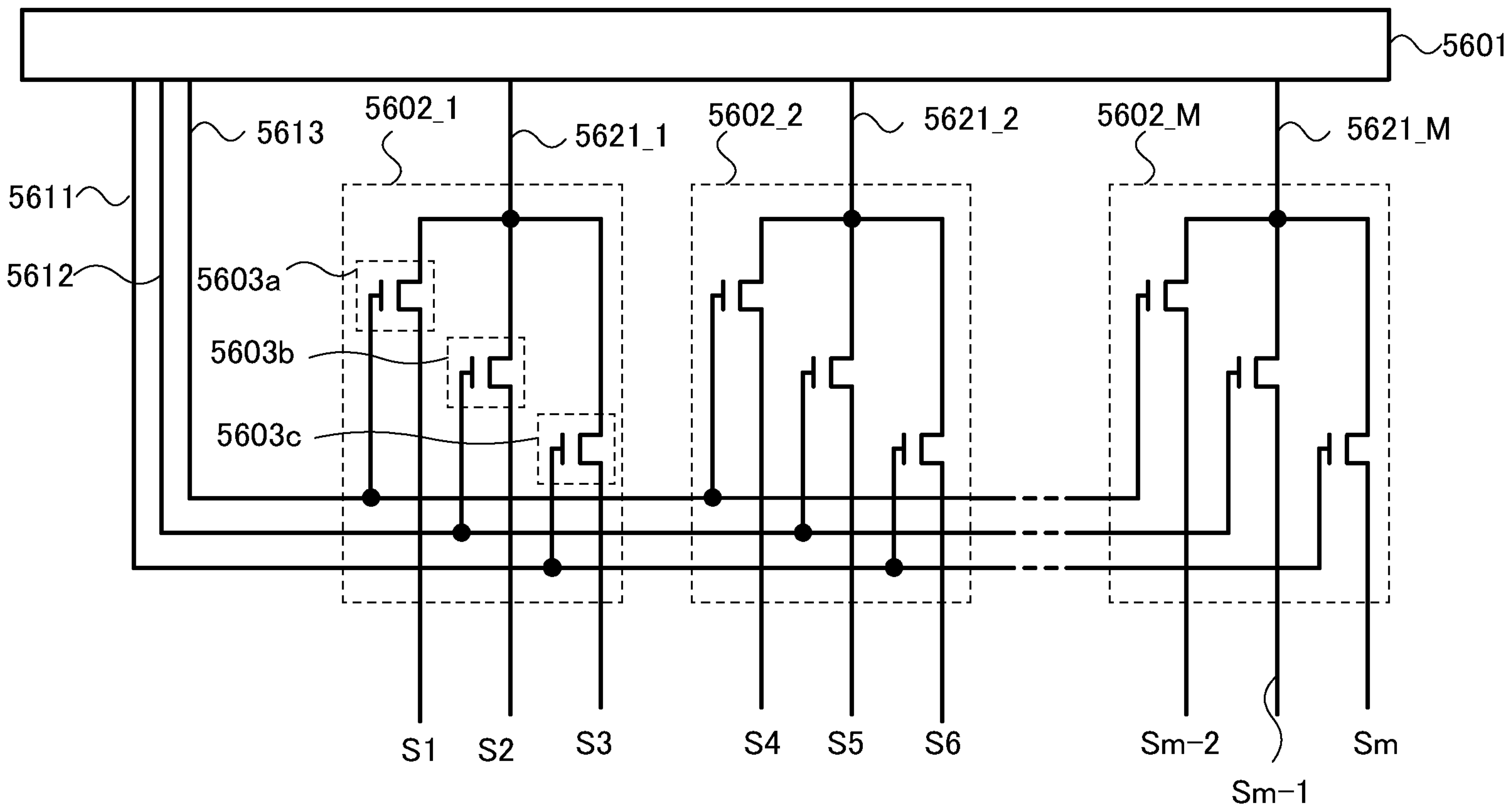


FIG. 13



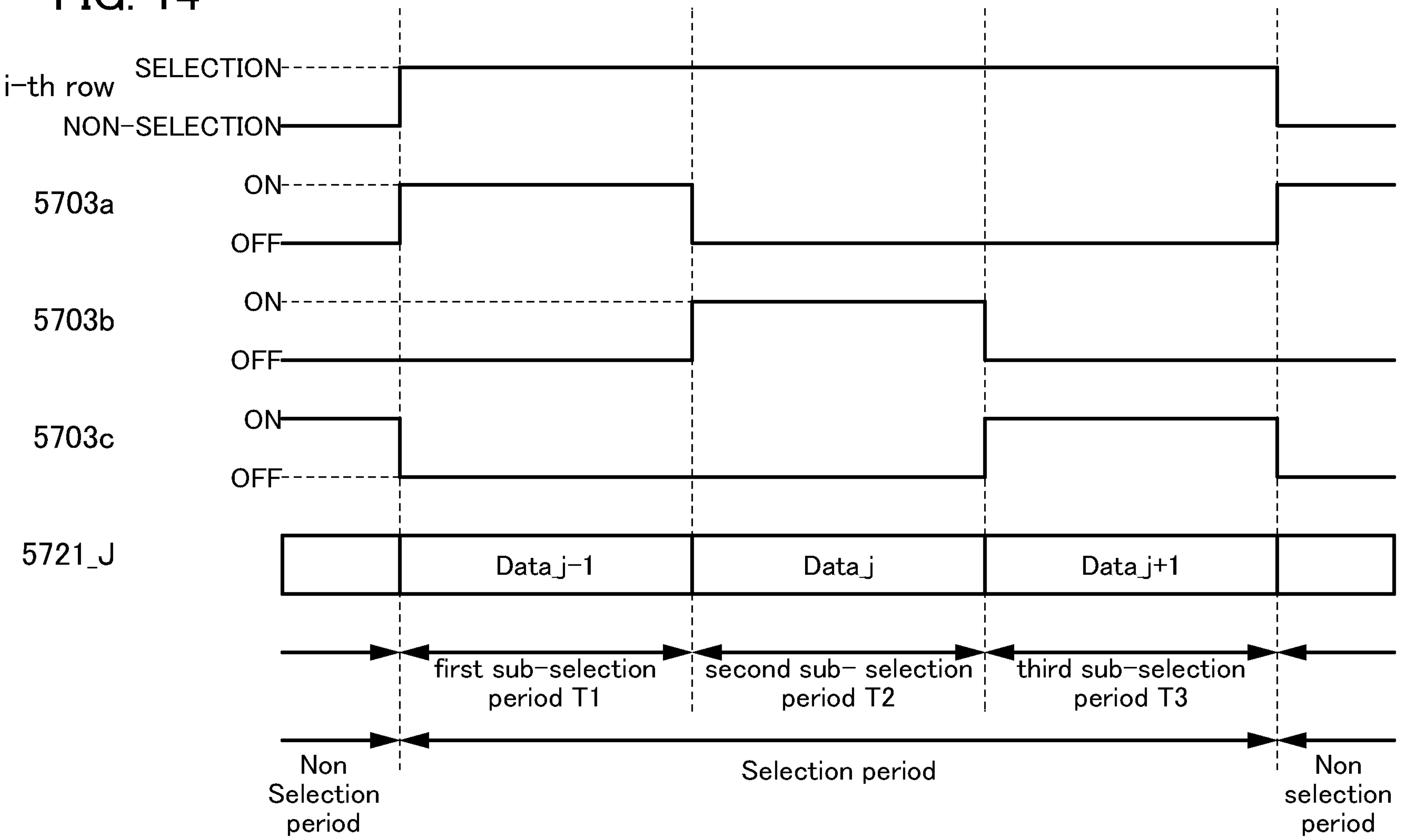


FIG. 14
i-th row
SELECTION
NON-SELECTION
5703a
ON
OFF
5703b
ON
OFF
5703c
ON
OFF
5721_J
Data j-1
Data j
Data j+1
first sub-selection period T1
second sub- selection period T2
third sub-selection period T3
Non Selection period
Selection period
Non selection period

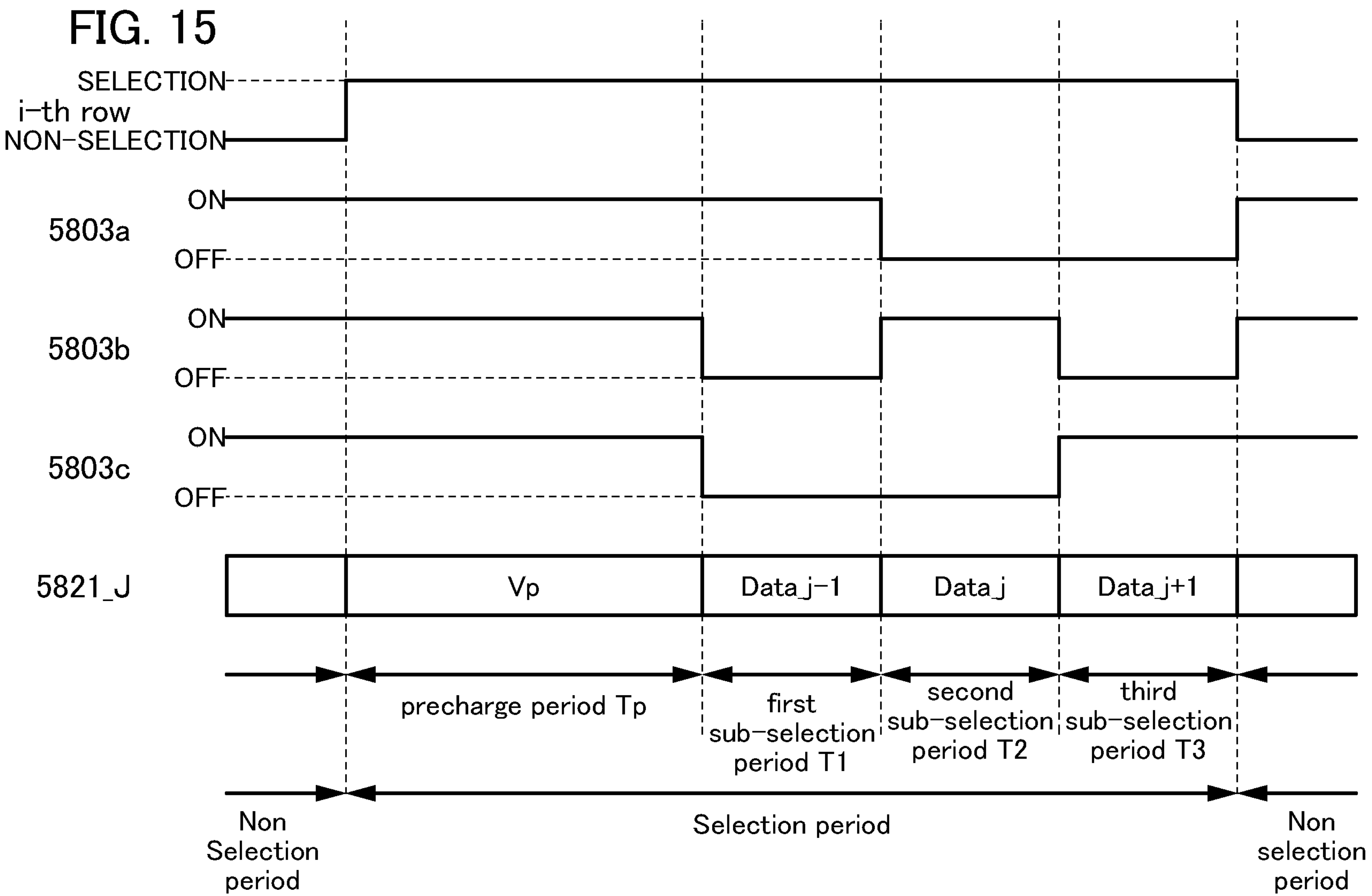


FIG. 15
SELECTION
i-th row
NON-SELECTION
5803a
5803b
5803c
ON
OFF
5821_J
Vp
Data j-1
Data j
Data j+1
precharge period Tp
first
sub-selection
period T1
second
sub-selection
period T2
third
sub-selection
period T3
Non
Selection
period
Selection period
Non
selection
period

FIG. 16

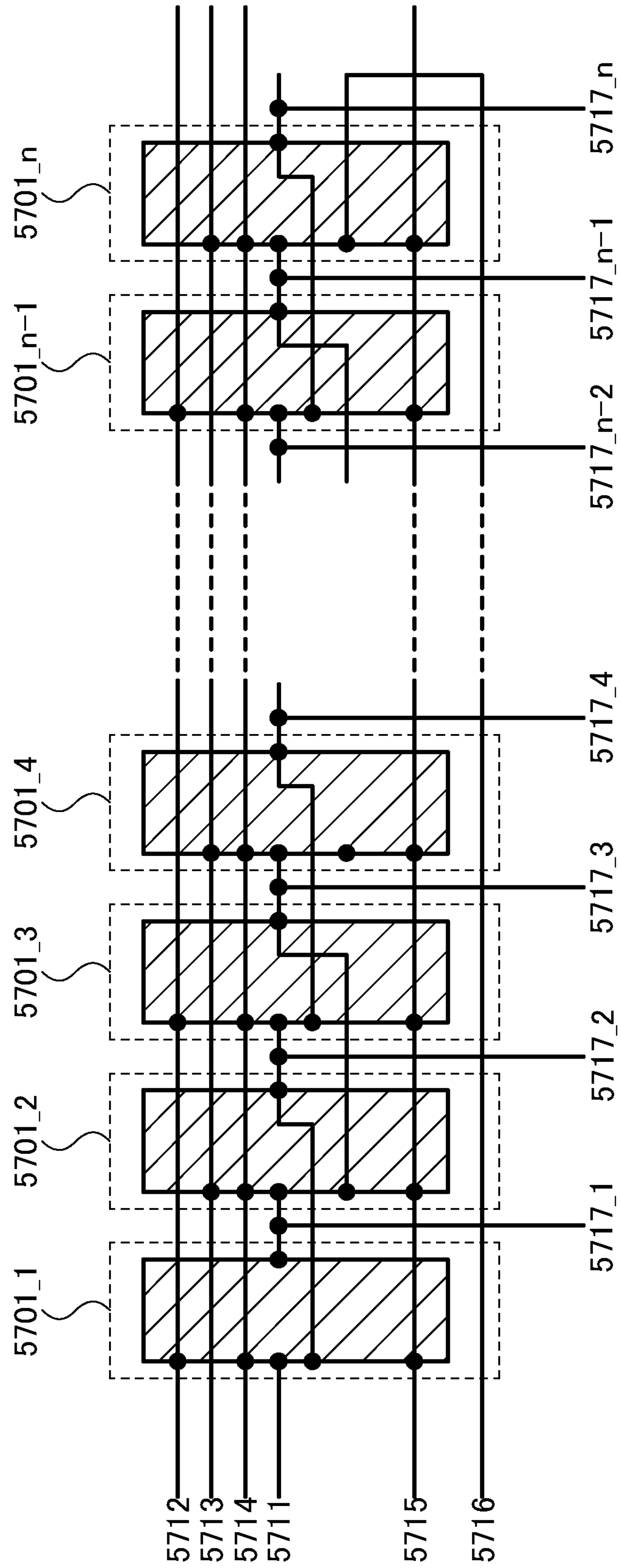


FIG. 17

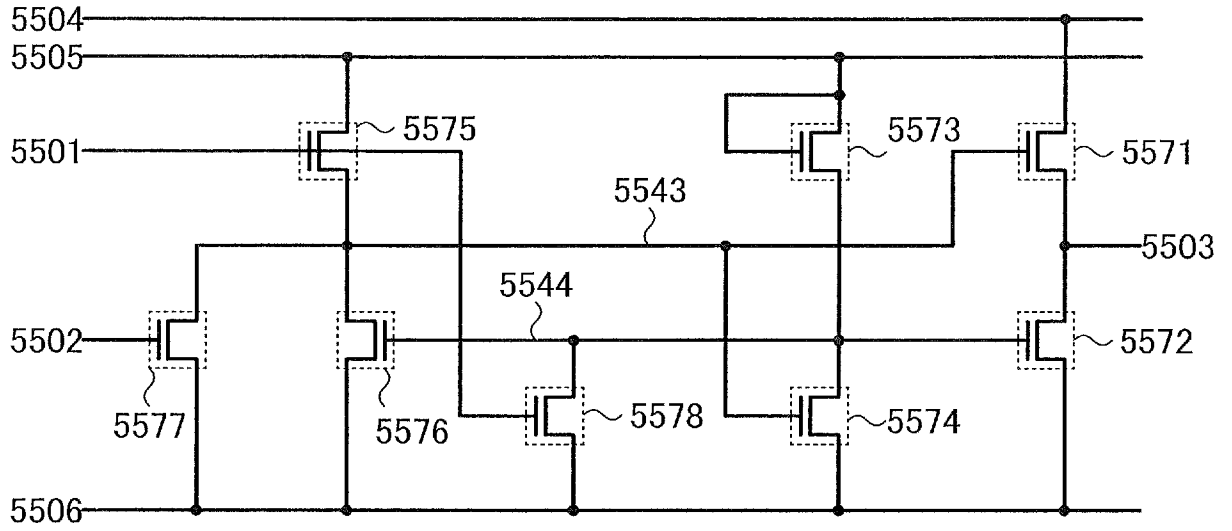


FIG. 18

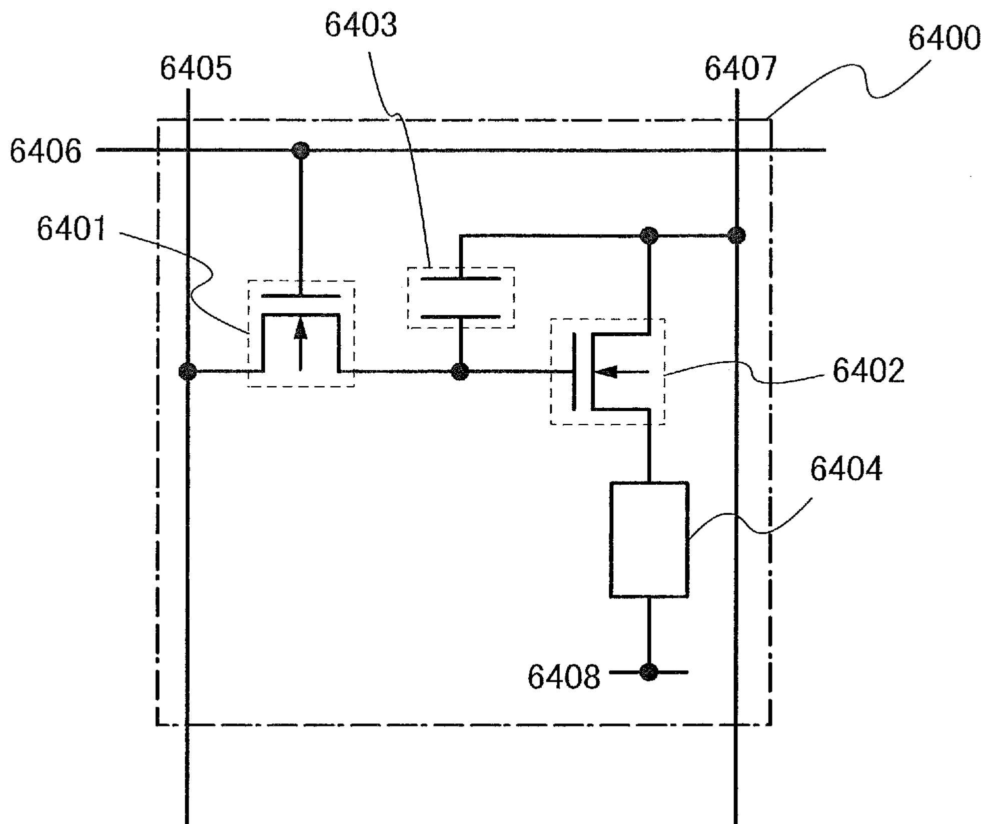


FIG. 19A

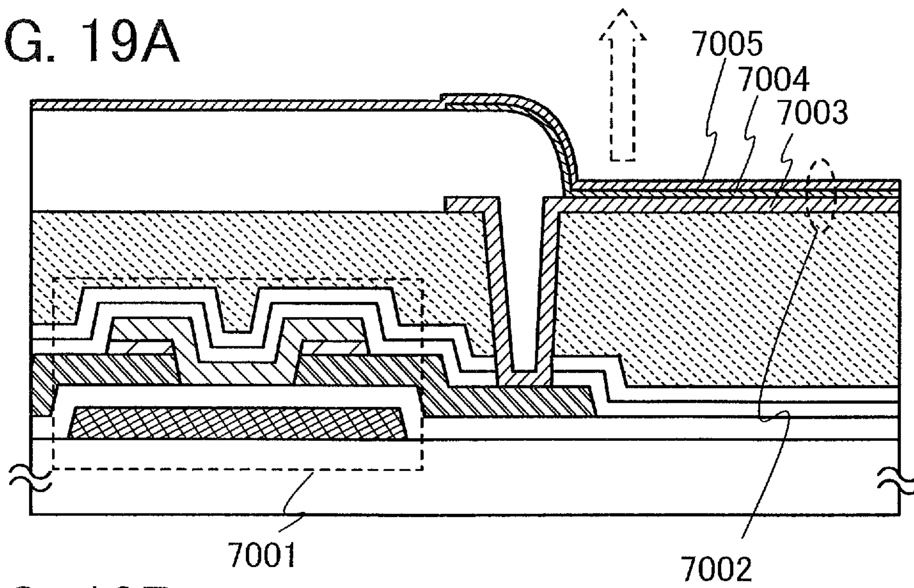


FIG. 19B

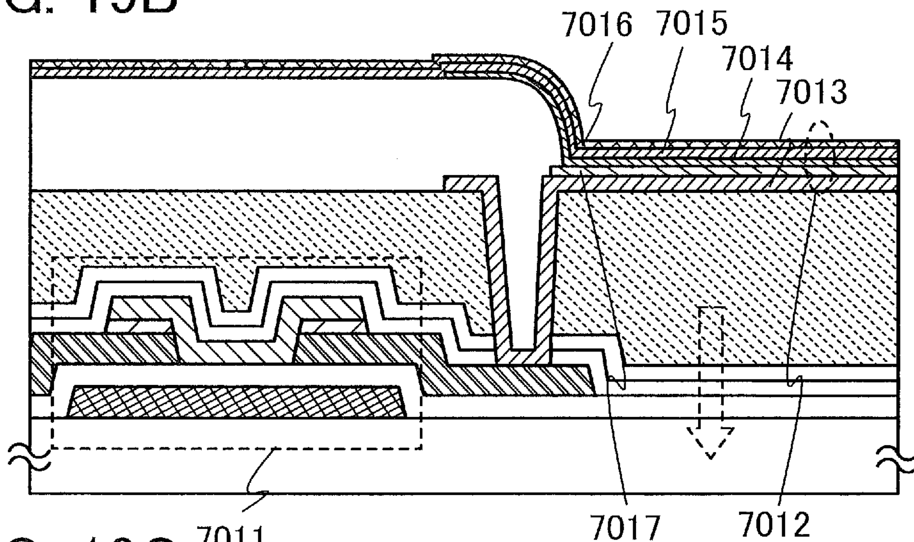


FIG. 19C

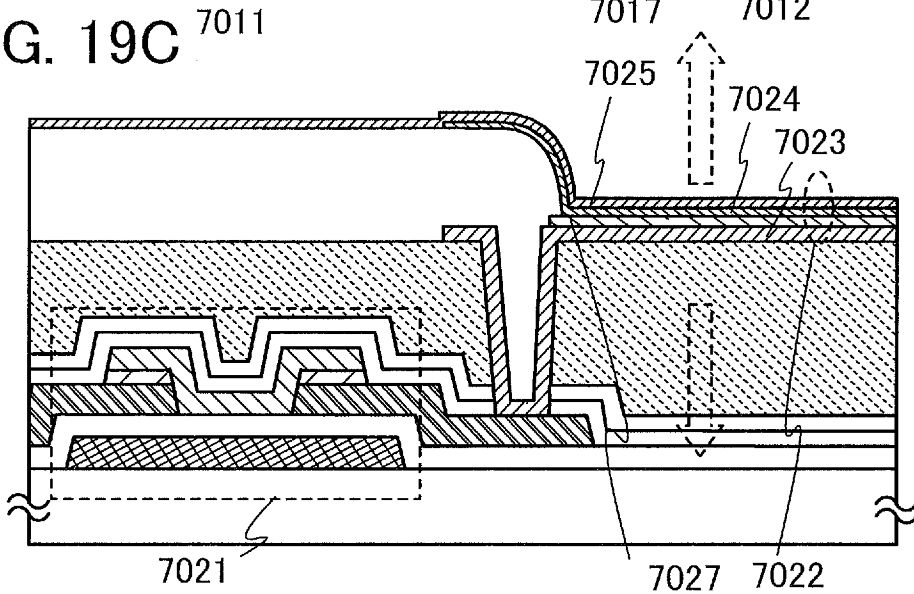


FIG. 20A1

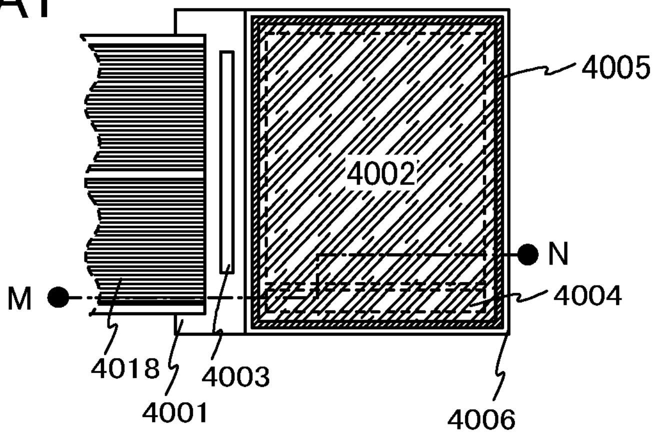


FIG. 20A2

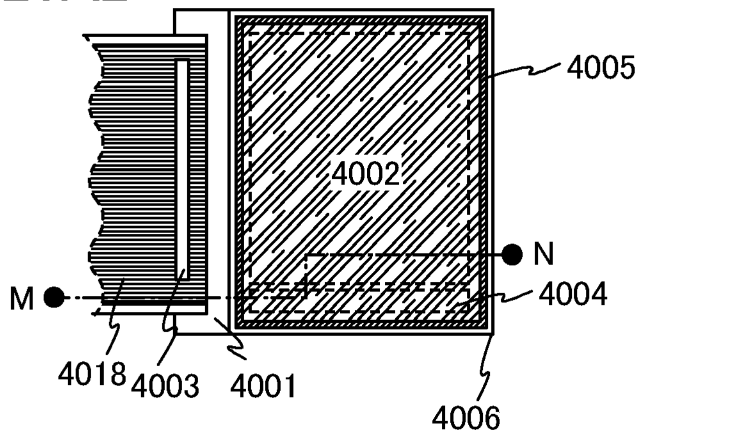


FIG. 20B

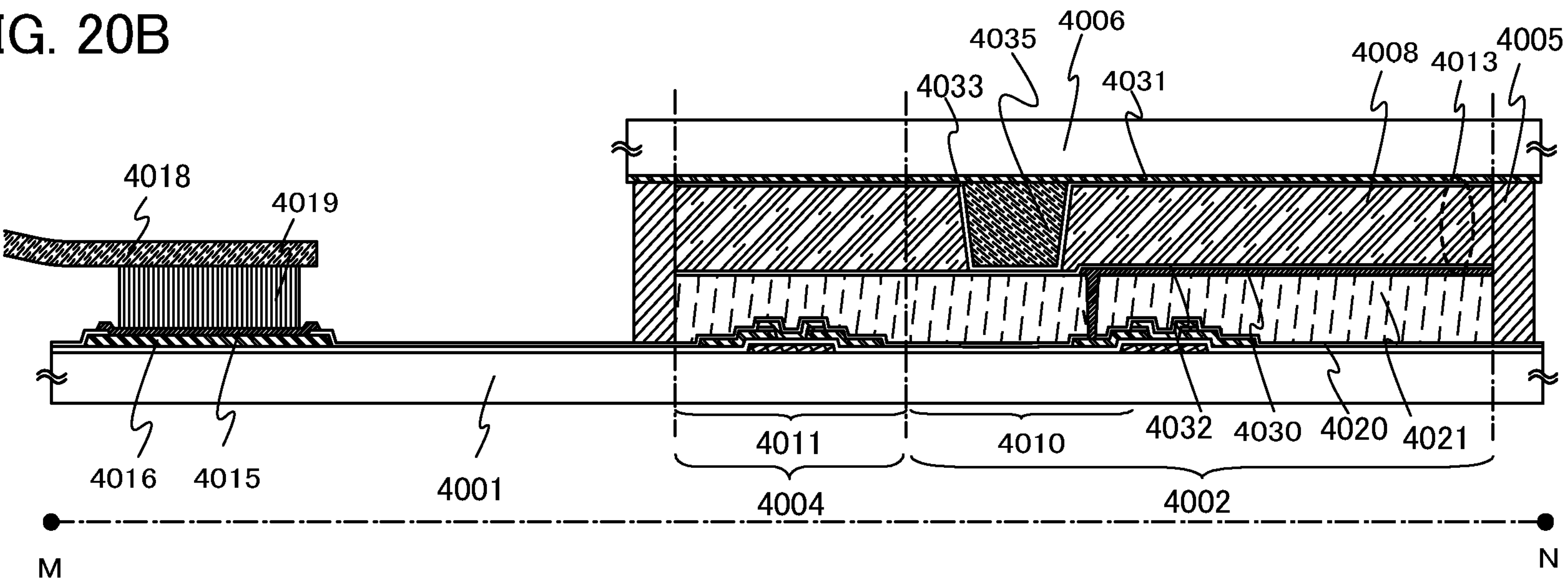


FIG. 21

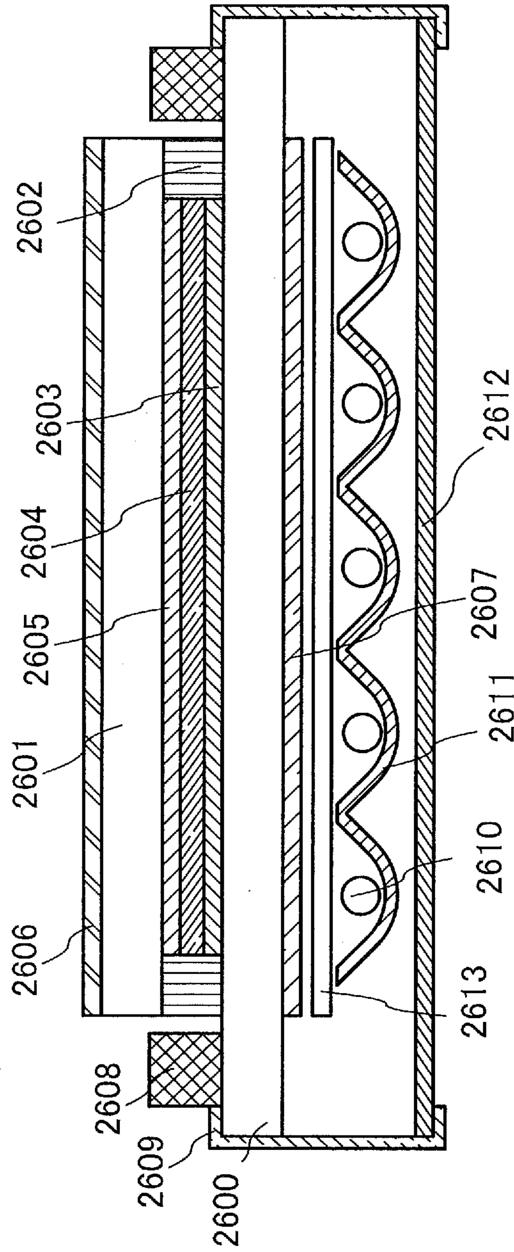


FIG. 22A

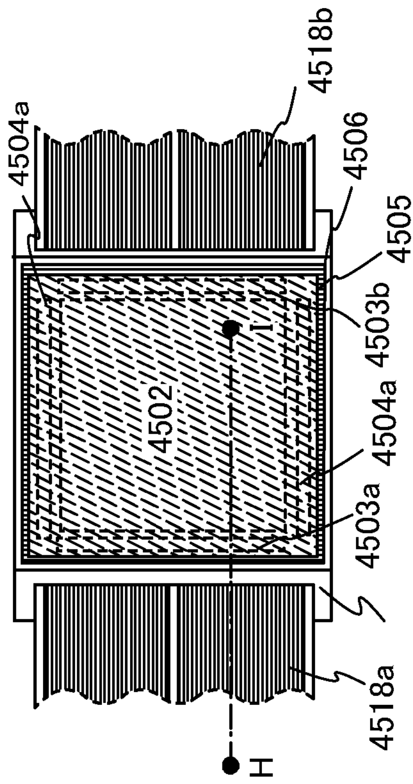


FIG. 22B

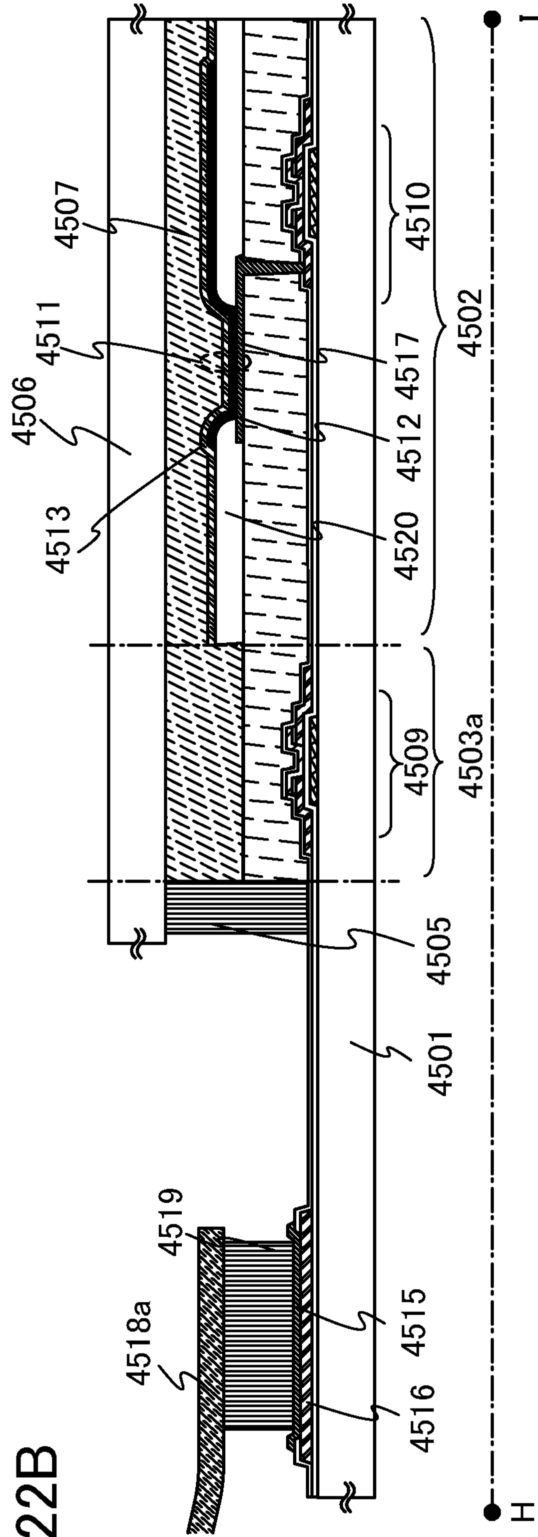


FIG. 23A

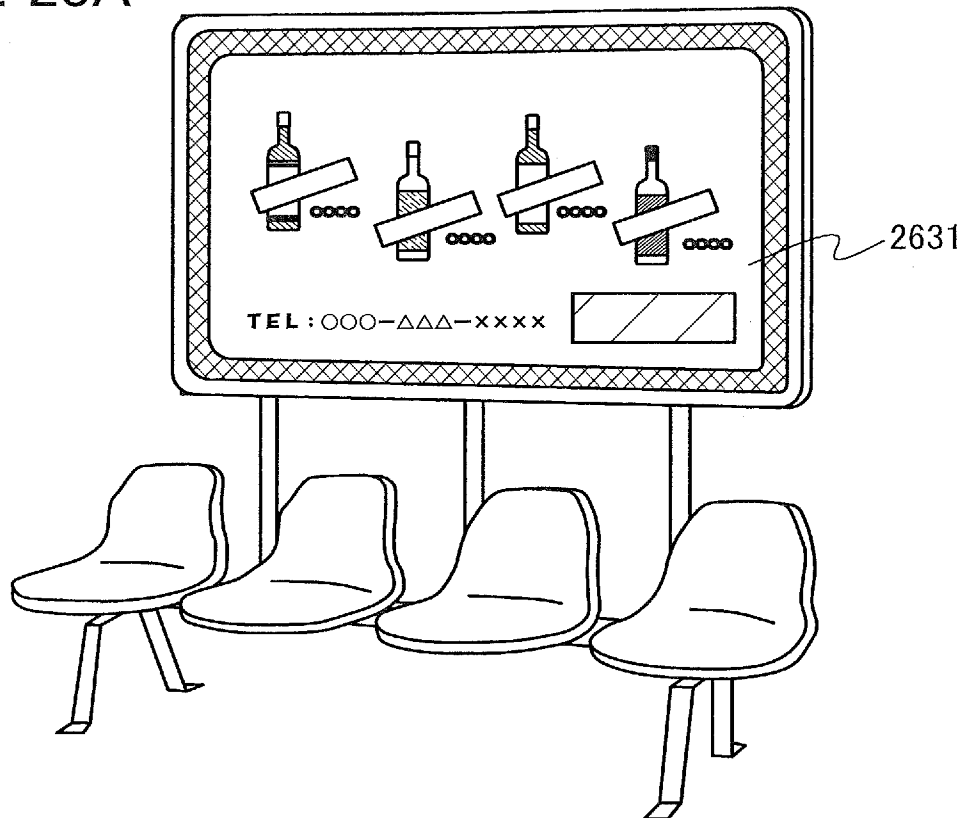


FIG. 23B

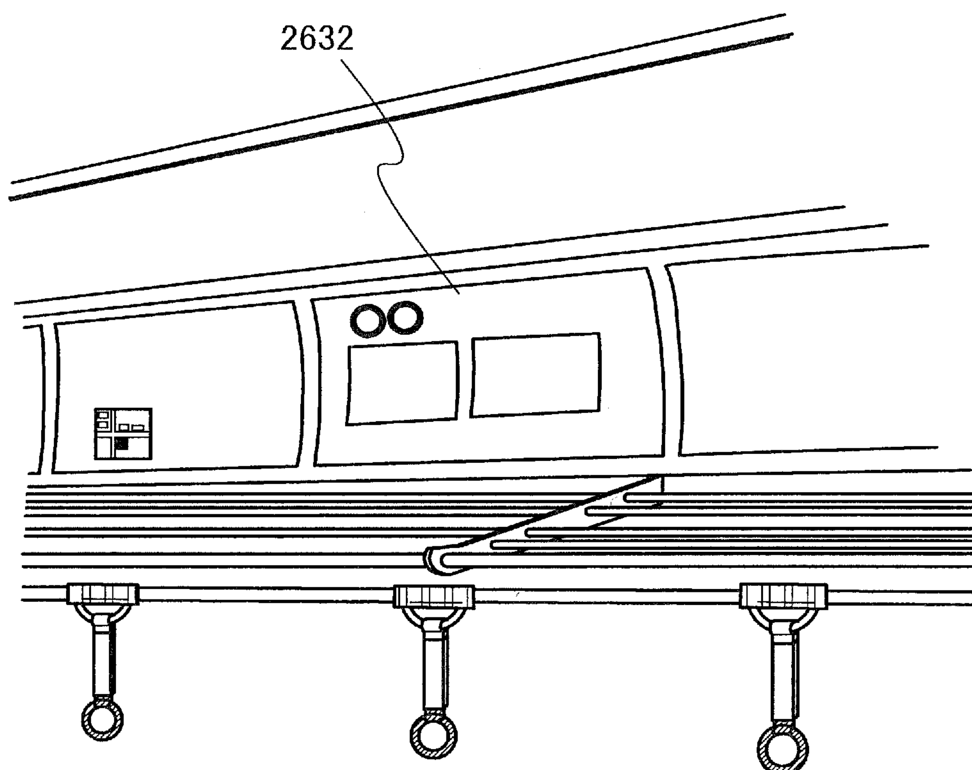


FIG. 24

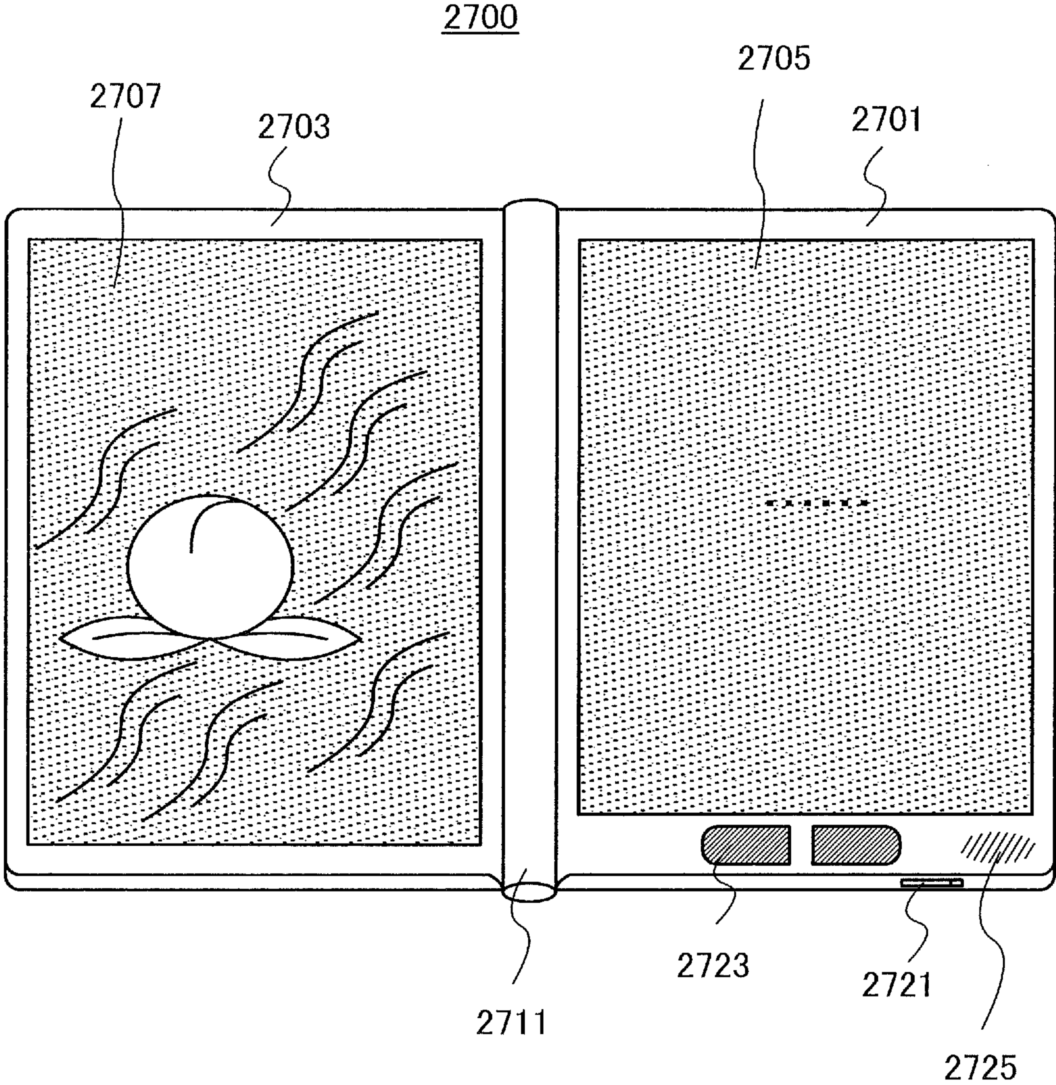


FIG. 25A

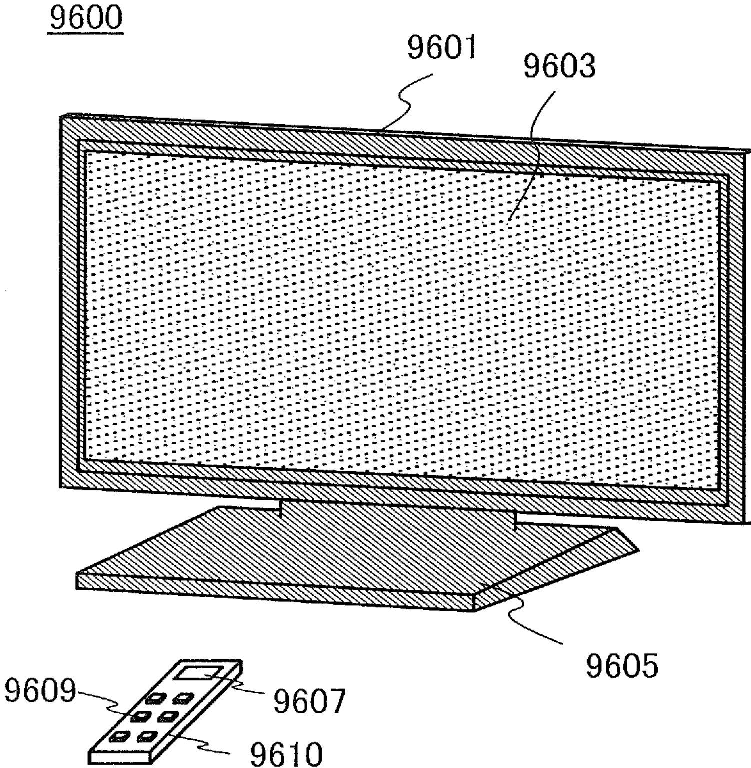


FIG. 25B

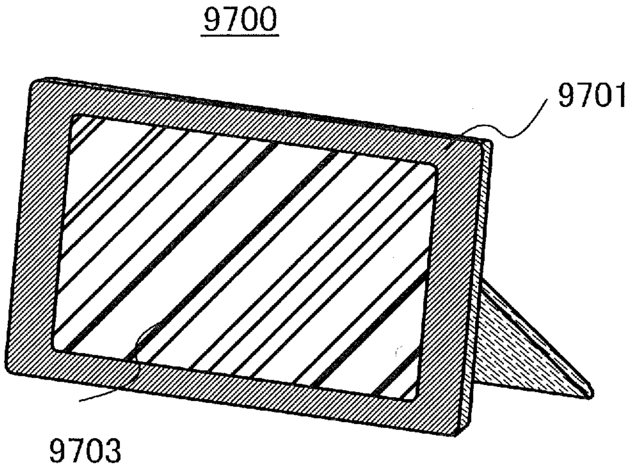


FIG. 26A

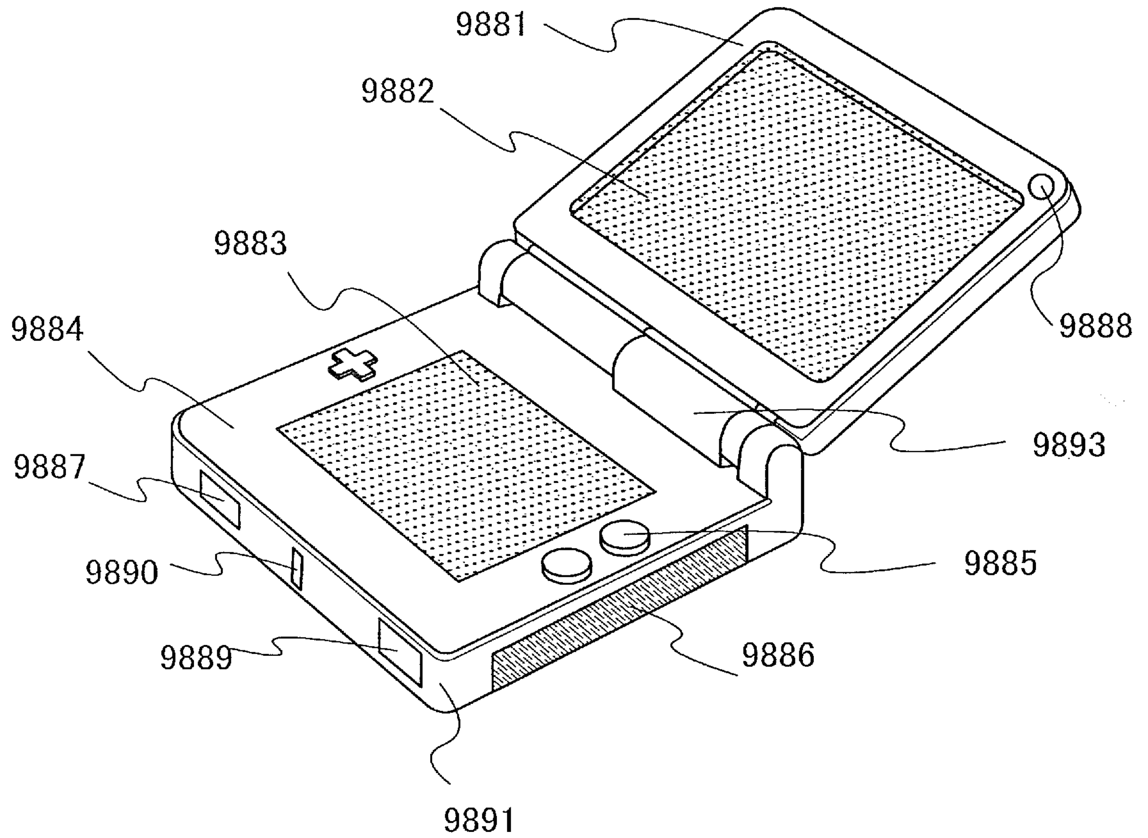


FIG. 26B

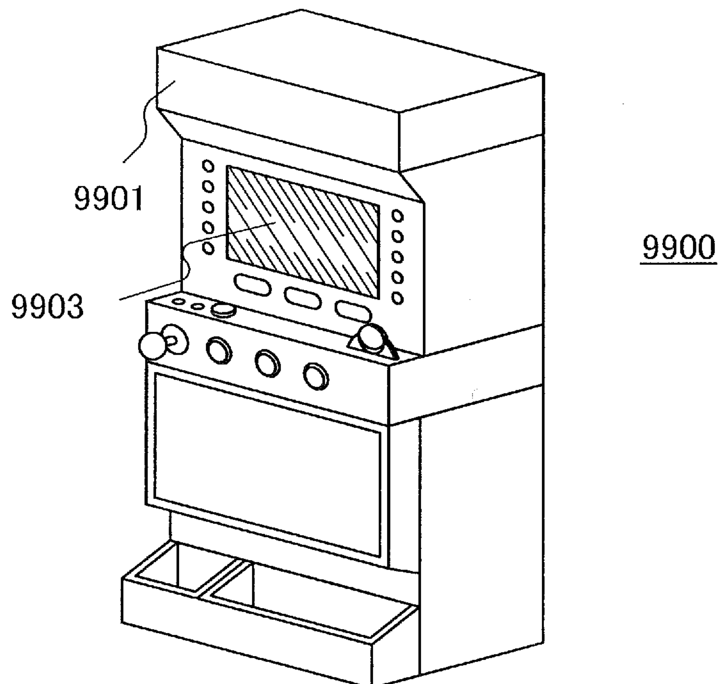


FIG. 27

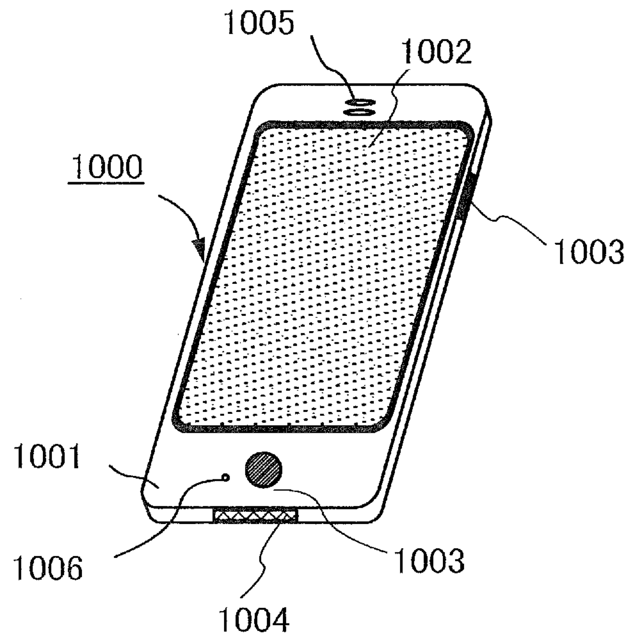


FIG. 28

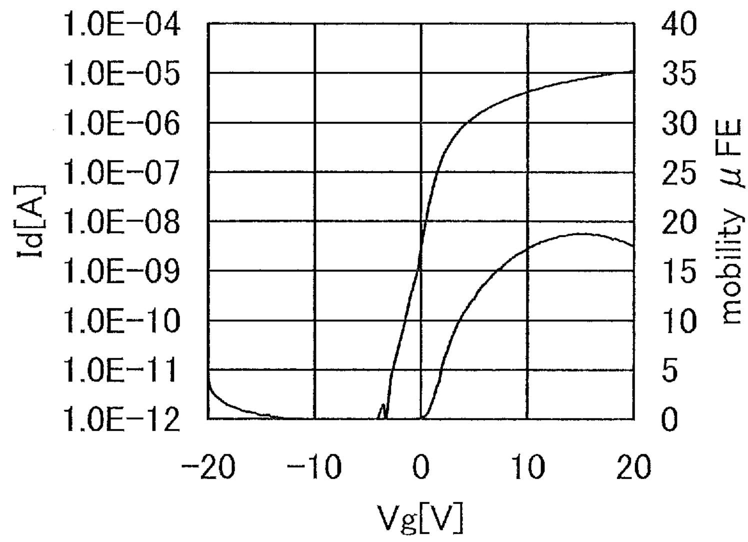


FIG. 29

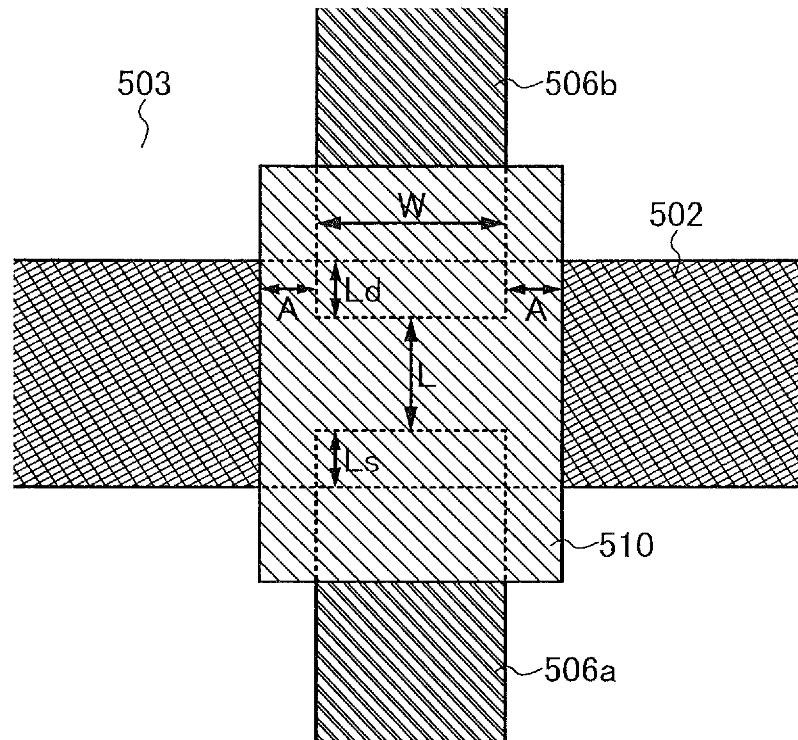


FIG. 30A

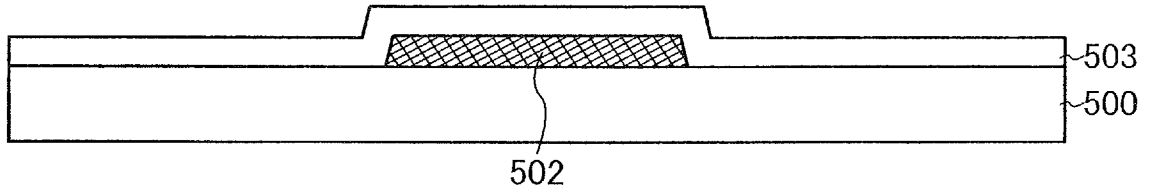


FIG. 30B

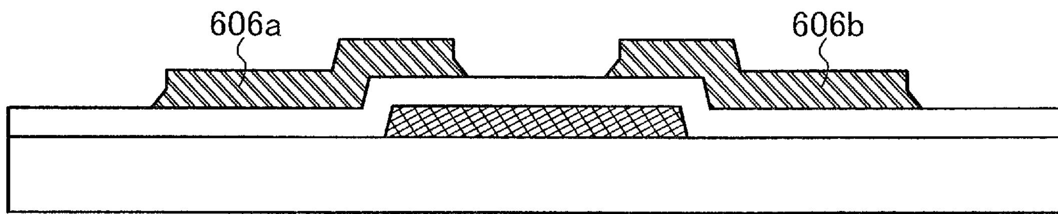


FIG. 30C

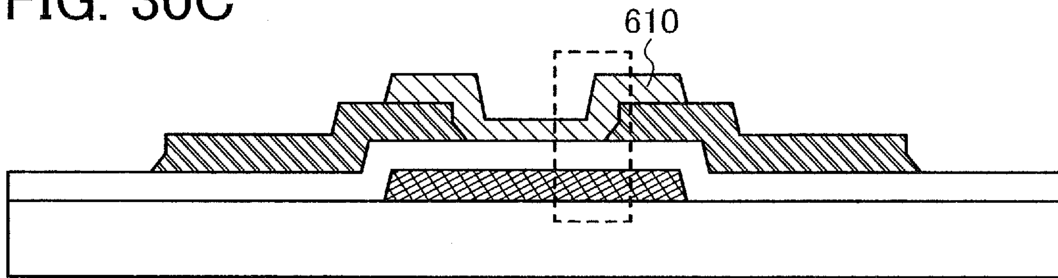


FIG. 31A

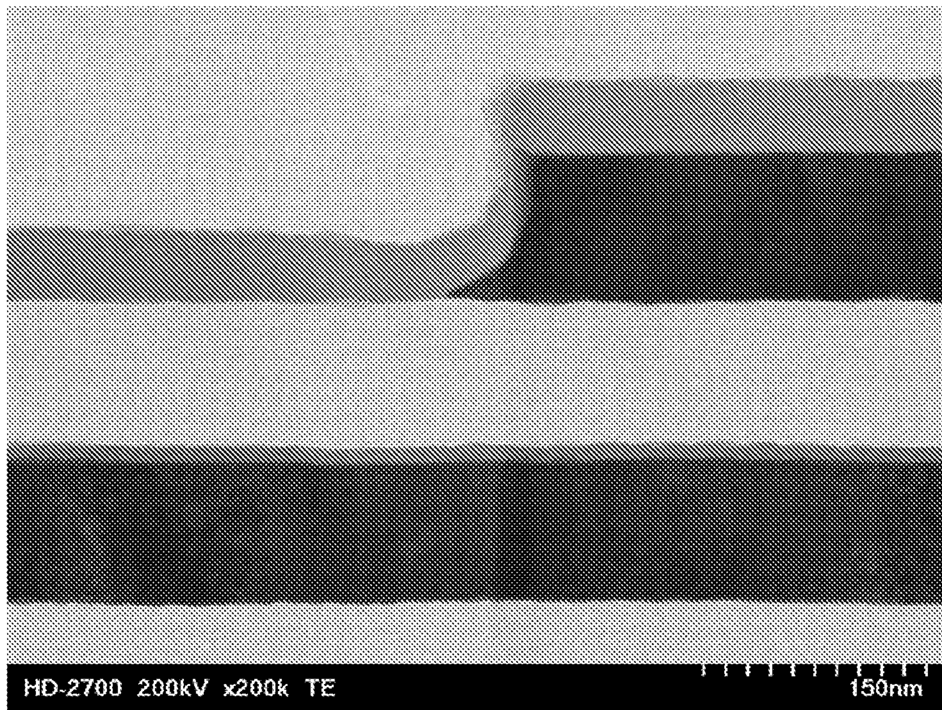


FIG. 31B

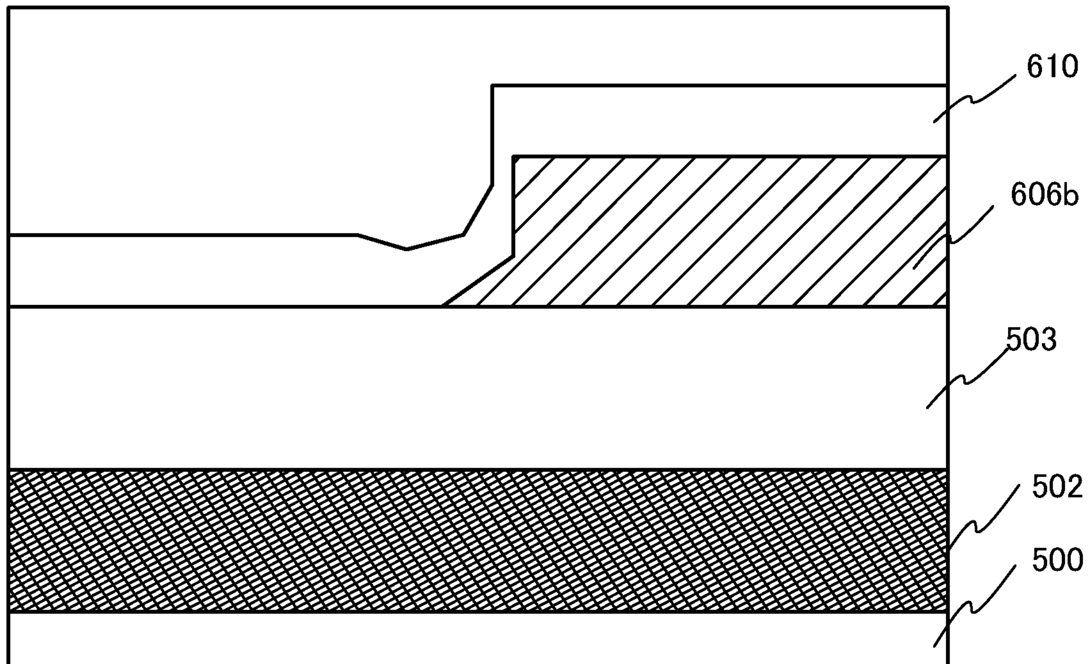


FIG. 32A

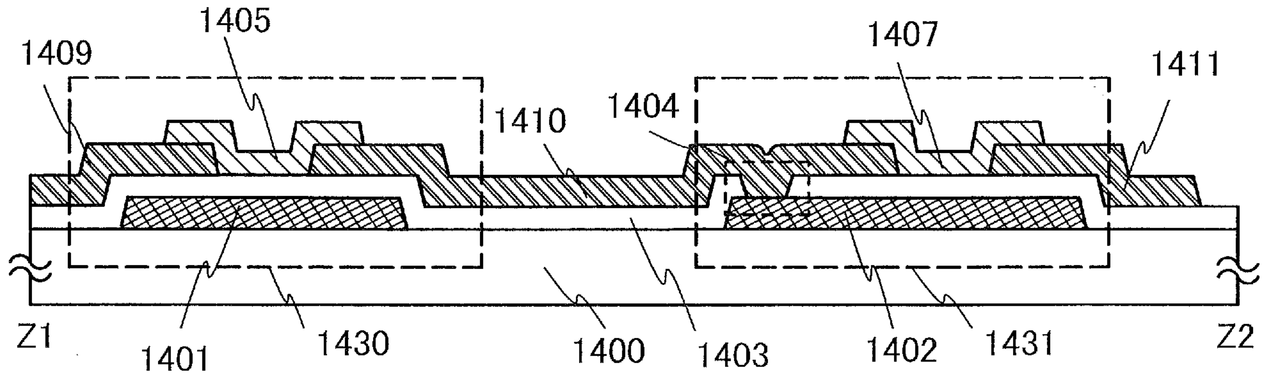


FIG. 32B

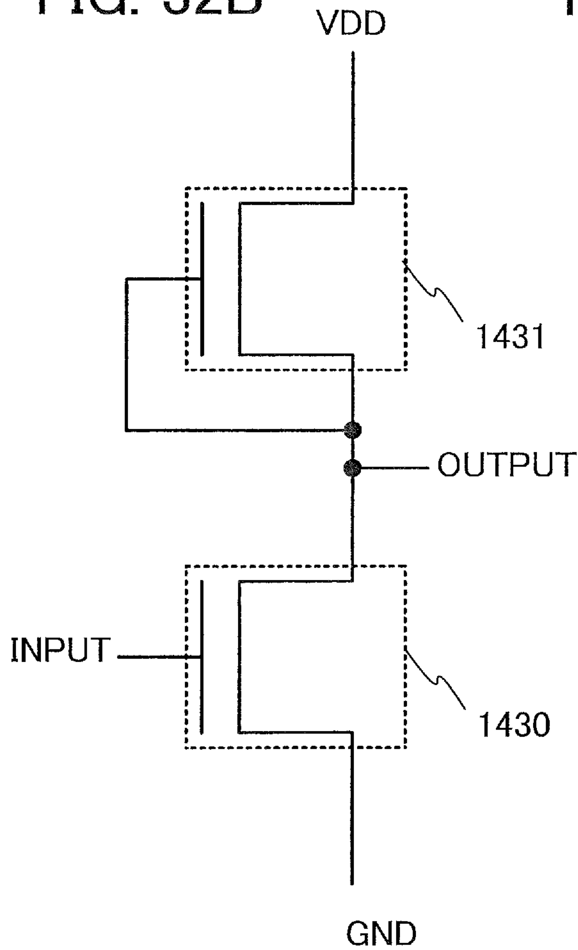


FIG. 32C

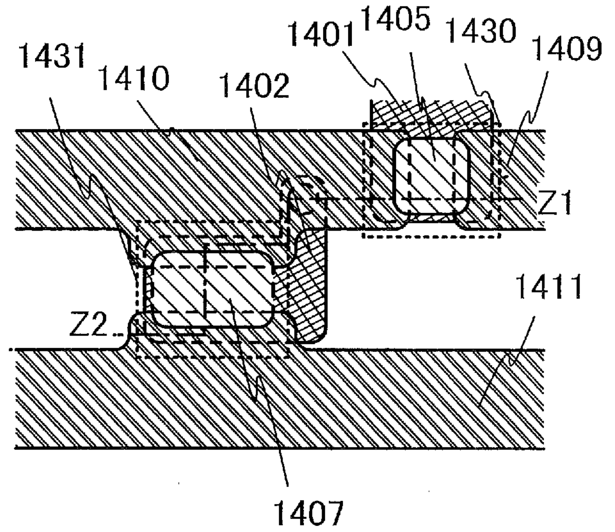


FIG. 33A

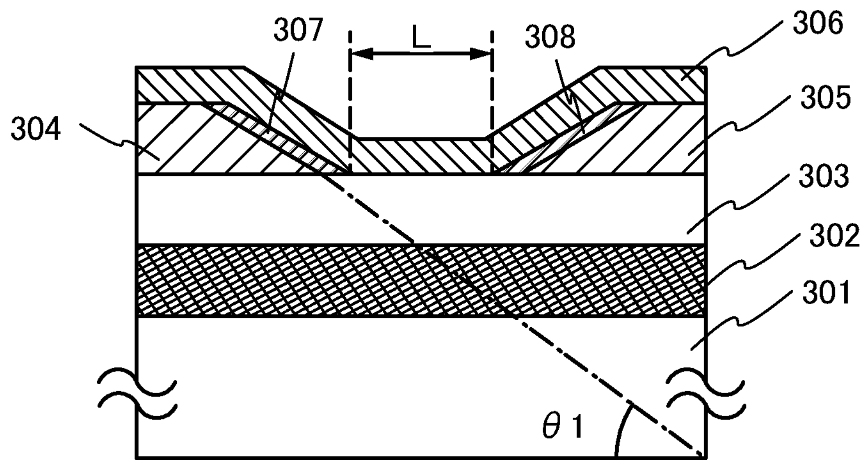


FIG. 33B

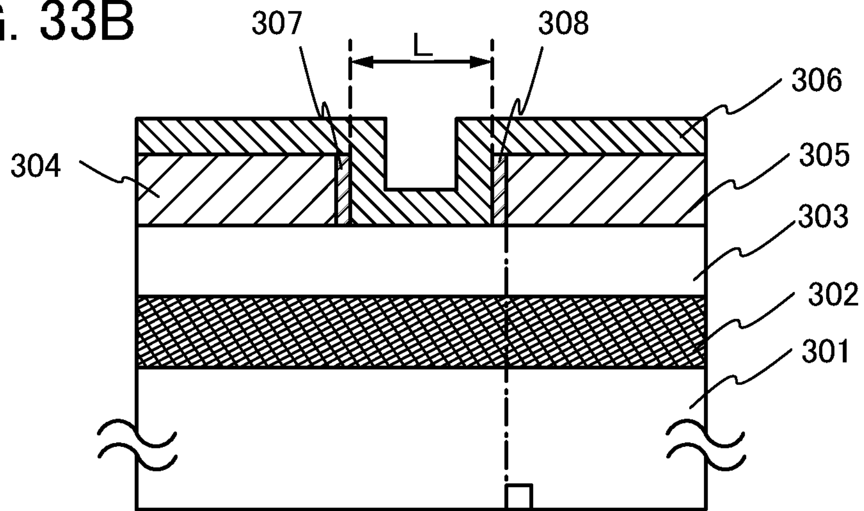


FIG. 33C

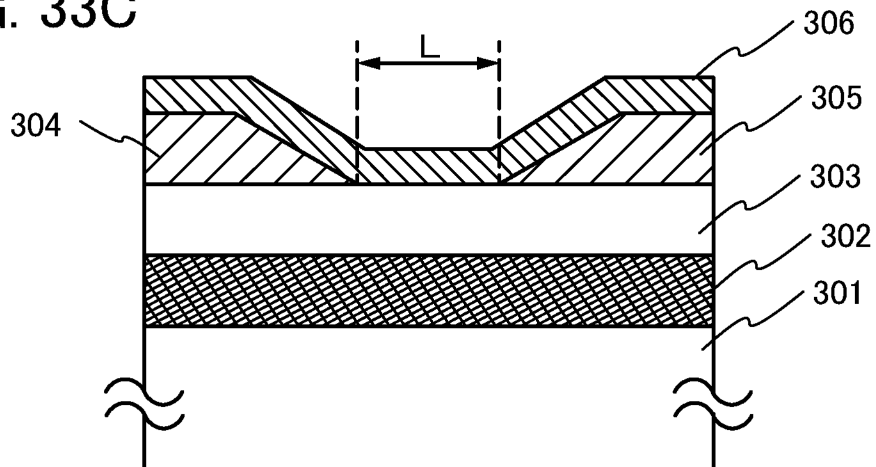


FIG. 34

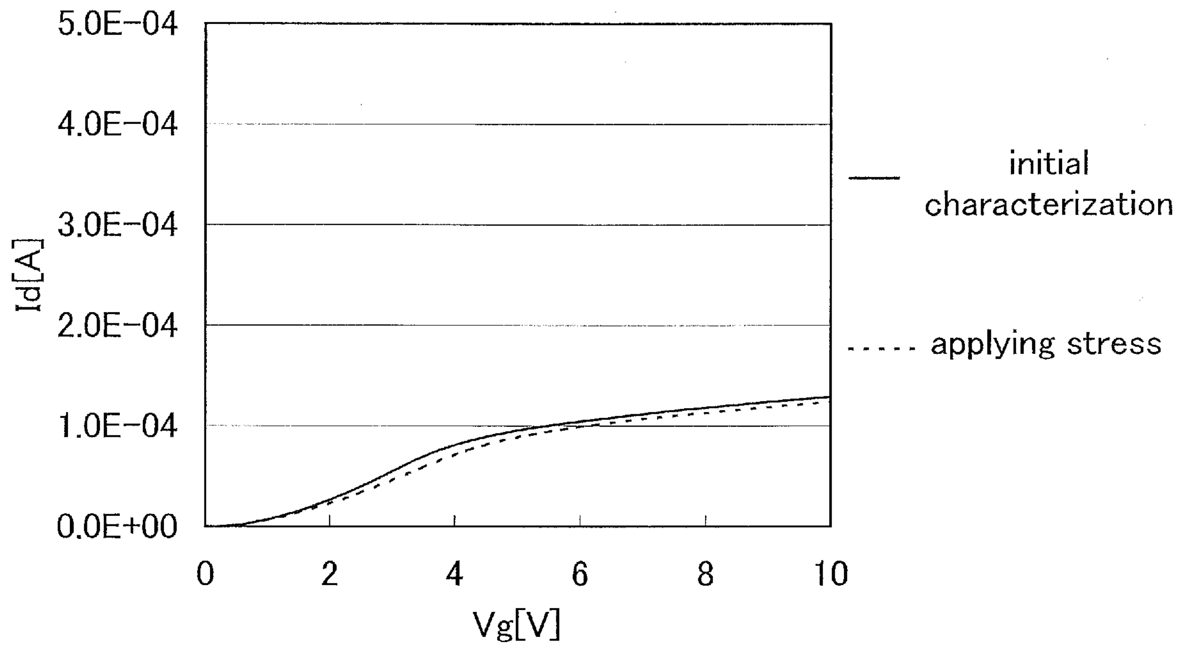


FIG. 35

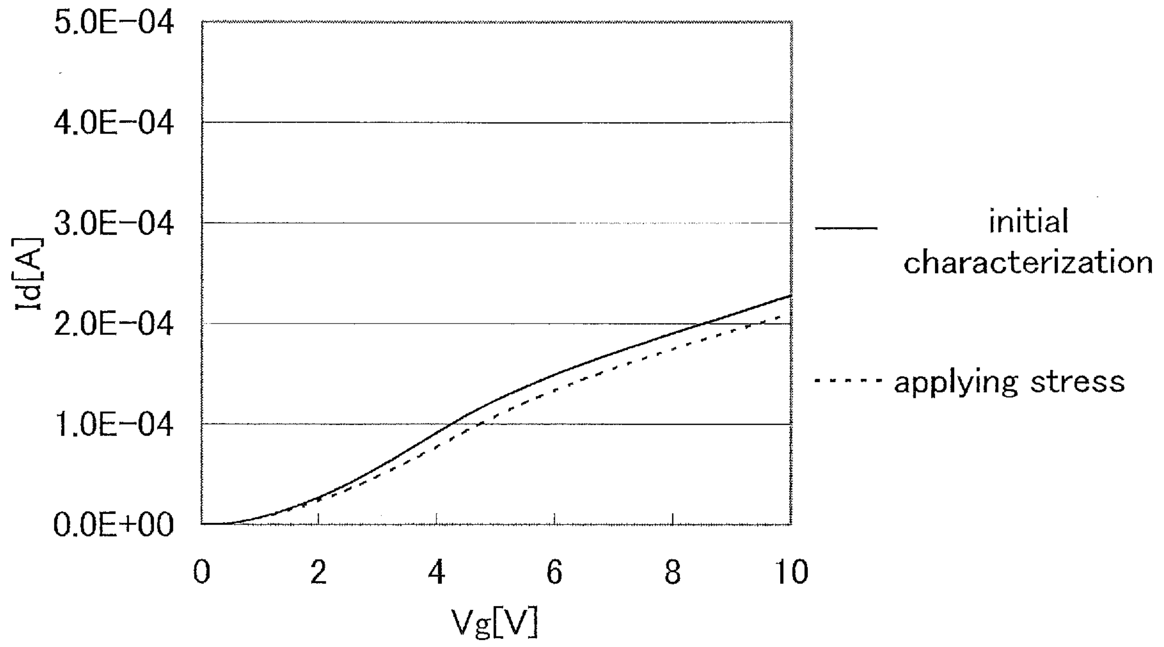


FIG. 36

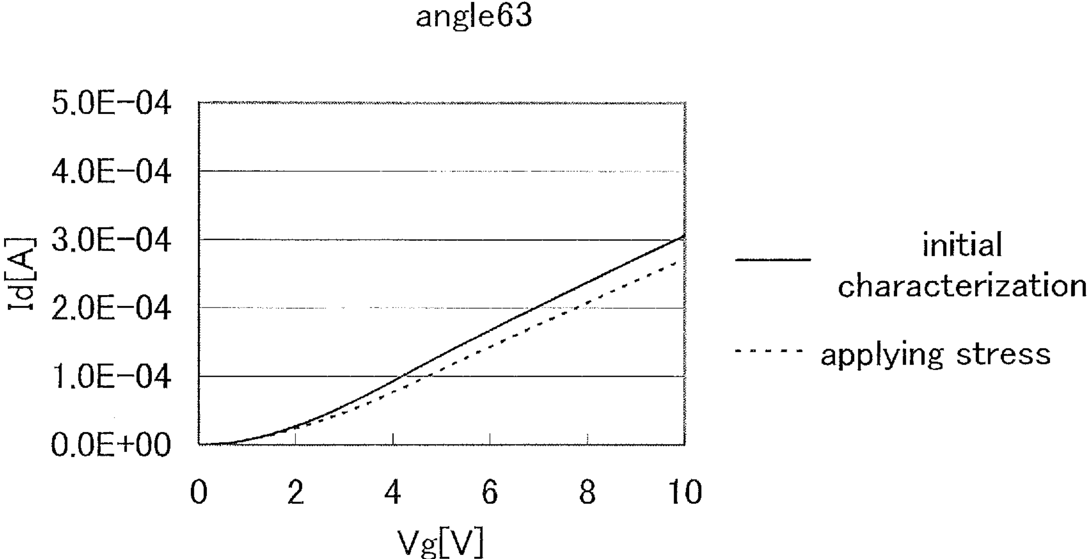


FIG. 37A

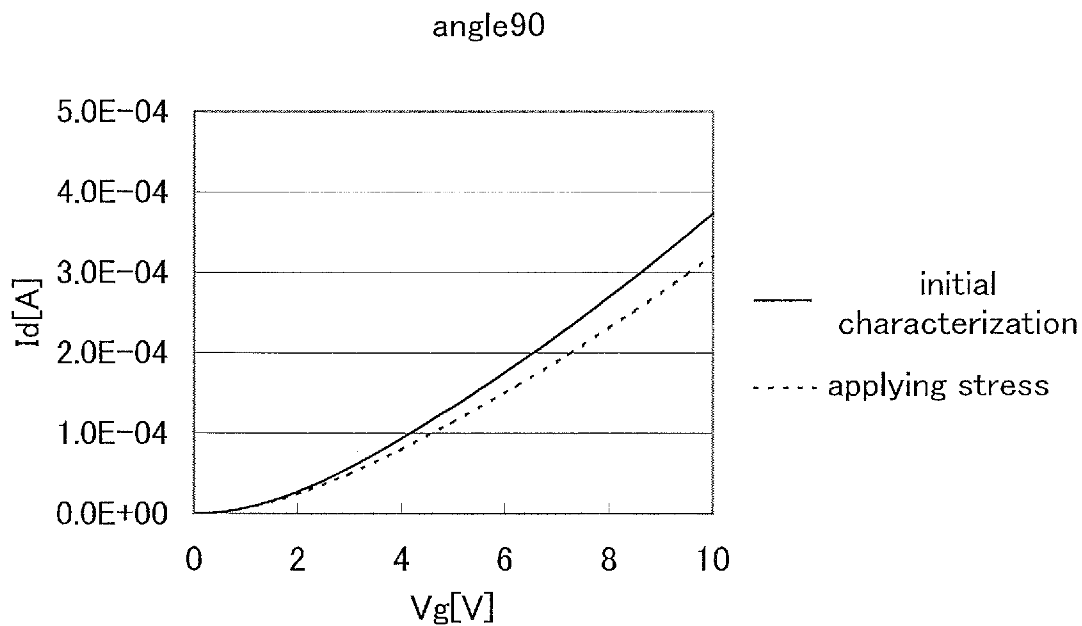
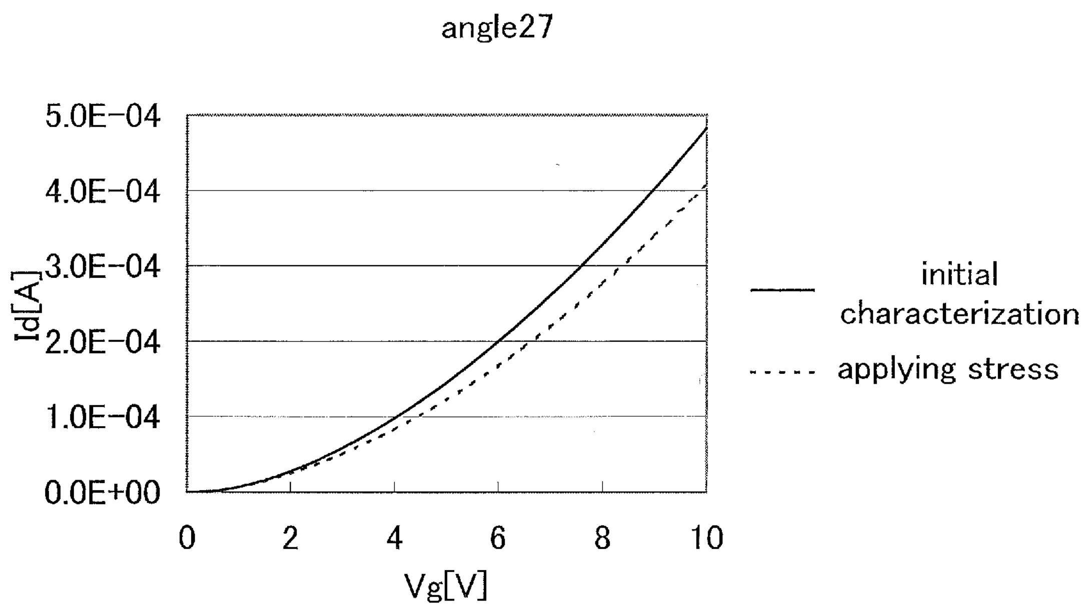


FIG. 37B



Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Shunpei Yamazaki
Filer:	Eric J. Robinson/Sue Ann Carr
Attorney Docket Number:	0756-10566

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt

EFS ID:	19775610
Application Number:	14451680
International Application Number:	
Confirmation Number:	5776
Title of Invention:	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Shunpei Yamazaki
Customer Number:	31780
Filer:	Eric J. Robinson/Sue Ann Carr
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-10566
Receipt Date:	05-AUG-2014
Filing Date:	
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Payment was successfully received in RAM	$1600
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Transmittal of New Application	TRNA.pdf	426333 abaeae62e4e9a923964bb9c078f534eeb596cba7	no	2
Warnings:					
Information:					
2	Assignee showing of ownership per 37 CFR 3.73.	373c_STATEMENT.pdf	550314 c872fd0a50cdab75fa68b2730f2559206b14370c	no	3
Warnings:					
Information:					
3	Power of Attorney	POA.pdf	196278 45ffba535bb2bc9ba5112ae39715d358079619cb	no	2
Warnings:					
Information:					
4	Application Data Sheet	ADS_05AUG2014.pdf	1561786 dd4fc824d3c896a5c1ba0ab4e553844b7d013ebb	no	8
Warnings:					
Information:					
5	Oath or Declaration filed	DEC.pdf	1401091 cd1b7fc5d748100af0c7f732b932a6d9d9313c86	no	6
Warnings:					
Information:					
6		SPEC.pdf	2882796 51608550f3718274135af2234223fd7055ebec3b	yes	115

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	76
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Warnings:					
Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	33145 73d750255f01945d0a9543eba277cc61b414dd8c	no	2
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