**Petitioner Bluehouse Global Ltd.**

**Ex. 1002**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | ISSUE DATE | PATENT NO. | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 14/337,583 | 03/08/2016 | 9281405 | 0756-10540 | 7546 |

31780 7590 02/17/2016

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

# ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Shinya SASAGAWA, Chigasaki, JAPAN;
Semiconductor Energy Laboratory Co., Ltd., Atsugi-shi, JAPAN;
Hideomi SUZAWA, Atsugi, JAPAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Document Description: Issue Fee Payment (PTO-85B)

# Issue Fee Transmittal Form

| Application Number | Filing Date | First Named Inventor | Atty. Docket No. | Confirmation No. |
|---|---|---|---|---|
| 14337583 | 22-Jul-2014 | Shinya SASAGAWA | 0756-10540 | 7546 |

**TITLE OF INVENTION :**

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

| Entity Status | Application Type | Art Unit | Class - Subclass | EXAMINER |
|---|---|---|---|---|
| Regular Undiscounted | Utility under 35 USC 111(a) | 2813 | 043000 | DAVID BLUM |

| Issue Fee Due | Publication Due | Total Fee(s) Due | Date Due | Prev. Paid Fee |
|---|---|---|---|---|
| $960 | $0 | $960 | 27-Jan-2016 | $0 |

## 1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

| Current Correspondence Address: | Current Indicated Fee Address : |
|---|---|
| 31780<br>Robinson Intellectual Property Law Office, P.C.<br><br>3975 Fair Ridge Drive<br>Suite 20 North<br>Fairfax VA 22033<br>UNITED STATES<br>571-434-6789<br>erobinson@riplo.com | |
| ☐ Change of correspondence address requested, system generated AIA/122-EFS form attached | ☐ Fee Address indication requested, system generated SB/47-EFS form attached |

## 2.Entity Status

### Change in Entity Status

○ Applicant certifying micro entity status; system generated Micro Entity certification form attached. See 37 CFR 1.29.
Note: Absent a valid certification of micro entity status, issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. If this box is checked, you will be prompted to choose a micro entity status on the gross income basis (37 CFR 1.29(a)) or the institution of higher education basis (37 CFR 1.29(d)), and make the applicable certification online.

○ Applicant asserting small entity status. See 37 CFR 1.27.
Note: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

◉ Applicant changing to regular undiscounted fee status.
Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

Document Description: Issue Fee Payment (PTO-85B)

**3.The Following Fee(s) Are Submitted:**

| | |
|---|---|
| ☒ Issue Fee | ☐ I authorize USPTO to apply my previously paid issue fee to the current fees due |
| ☐ Publication Fee | ☐ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number ________ |
| ☒ Advance Order - # of copies 2 | ☒ If i**n addition to** the payment of the issue fee amount submitted with this form, there are any discrepancies in any amount(s) due, the Director is authorized to charge any deficiency, or credit any overpayment, to Deposit Account Number 50-2280 . The **issue fee must be submitted** with this form. **If payment of the issue fee does not accompany this form, checking this box and providing a deposit account number will NOT be effective to satisfy full payment of the fee(s) due.** |

**4.Firm and/or Attorney Names To Be Printed**

**NOTE: If no name is listed, no name will be printed**
For printing on the patent front page, list to be displayed as entered

1. ROBINSON INTELLECTUAL PROPERTY LAW OFFICE
2. ERIC J. ROBINSON
3.

**5.Assignee Name(s) and Residence Data To Be Printed**

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

| Name | City | State | Country | Category |
|---|---|---|---|---|
| Semiconductor Energy Laboratory Co., Ltd. | Kanagawa-ken | | japan | corporation |

**6.Signature**

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

| | | | |
|---|---|---|---|
| **Signature** | /Eric J. Robinson/ | **Date** | 01-27-2016 |
| **Name** | Eric J. Robinson | **Registration Number** | 38285 |

# Electronic Patent Application Fee Transmittal

| | |
|---|---|
| **Application Number:** | 14337583 |
| **Filing Date:** | 22-Jul-2014 |
| **Title of Invention:** | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME |
| **First Named Inventor/Applicant Name:** | Shinya SASAGAWA |
| **Filer:** | Eric J. Robinson/Sue Ann Carr |
| **Attorney Docket Number:** | 0756-10540 |

Filed as Large Entity

**Filing Fees for** **Utility under 35 USC 111(a)**

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| Utility Appl Issue Fee | 1501 | 1 | 960 | 960 |
| Publ. Fee- Early, Voluntary, or Normal | 1504 | 1 | 0 | 0 |
| Printed Copy of Patent - No Color | 8001 | 2 | 3 | 6 |
| **Pages:** | | | | |
| **Claims:** | | | | |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Post-Allowance-and-Post-Issuance:** | | | | |
| **Extension-of-Time:** | | | | |
| **Miscellaneous:** | | | | |
| | | **Total in USD ($)** | | **966** |

# Electronic Acknowledgement Receipt

| | |
|---|---|
| **EFS ID:** | 24721062 |
| **Application Number:** | 14337583 |
| **International Application Number:** | |
| **Confirmation Number:** | 7546 |
| **Title of Invention:** | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME |
| **First Named Inventor/Applicant Name:** | Shinya SASAGAWA |
| **Customer Number:** | 31780 |
| **Filer:** | Eric J. Robinson/Sue Ann Carr |
| **Filer Authorized By:** | Eric J. Robinson |
| **Attorney Docket Number:** | 0756-10540 |
| **Receipt Date:** | 27-JAN-2016 |
| **Filing Date:** | 22-JUL-2014 |
| **Time Stamp:** | 08:30:20 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | yes |
| Payment Type | Electronic Funds Transfer |
| Payment was successfully received in RAM | $966 |
| RAM confirmation Number | 6659,6660 |
| Deposit Account | |
| Authorized User | |

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Issue Fee Payment (PTO-85B) | Web85b.pdf | 46339<br>37ee72e5a71bda709138c75b3b0c44063d605b3a | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | Fee Worksheet (SB06) | fee-info.pdf | 35686<br>4f8e635aa61fc408b658562adfba9325a6731507 | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | | **Total Files Size (in bytes):** | 82025 | |

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**
**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

# NOTICE OF ALLOWANCE AND FEE(S) DUE

31780 7590 10/27/2015
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

| EXAMINER | |
|---|---|
| BLUM, DAVID S | |
| ART UNIT | PAPER NUMBER |
| 2813 | |

DATE MAILED: 10/27/2015

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 14/337,583 | 07/22/2014 | Shinya SASAGAWA | 0756-10540 | 7546 |

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | UNDISCOUNTED | $960 | $0 | $0 | $960 | 01/27/2016 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

## HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

## PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail** **Mail Stop ISSUE FEE**
**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, Virginia 22313-1450**
**or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31780 7590 10/27/2015
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 14/337,583 | 07/22/2014 | Shinya SASAGAWA | 0756-10540 | 7546 |

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | UNDISCOUNTED | $960 | $0 | $0 | $960 | 01/27/2016 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| BLUM, DAVID S | 2813 | 257-043000 |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
   (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
   1 ____________________
   2 ____________________
   3 ____________________

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies ____________________

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number ____________ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature ______________________ Date ______________________

Typed or printed name ______________________ Registration No. ______________________

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 14/337,583 | 07/22/2014 | Shinya SASAGAWA | 0756-10540 | 7546 |

31780 7590 10/27/2015

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

| EXAMINER | |
|---|---|
| BLUM, DAVID S | |
| ART UNIT | PAPER NUMBER |
| 2813 | |

DATE MAILED: 10/27/2015

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

## OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

## Privacy Act Statement

**The Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

| **Notice of Allowability** | **Application No.**<br>14/337,583 | **Applicant(s)**<br>SASAGAWA ET AL. | |
|---|---|---|---|
| | **Examiner**<br>DAVID S. BLUM | **Art Unit**<br>2813 | **AIA (First Inventor to File) Status**<br>No |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 9/21/15.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on______.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-16 and 18-23. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   **Certified copies:**

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. ______ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/DAVID S BLUM/
Primary Examiner, Art Unit 2813

This action is in response to the amendment filed 9/21/15.

## ***Notice of Pre-AIA or AIA Status***

1. The present application is being examined under the pre-AIA first to invent provisions.

## EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In the Specification, on page 1, after the title and before Technical Field, please insert the following.

## CROSS-REFERENCE TO RELATED APPLICATIONS

This is a divisional application and claims the benefit of an Application Serial No. 13/716891, now U. s. Patent No. 8,790,961, filed December 17, 2012, which is based upon and claims priority from Japanese Patent Application Nos. 2011-282438 and 2011-282511, filed 12/23/2011 and 12/23/2011, the entire contents of which are incorporated herein by reference.

## ***Reasons for Allowance***

3. Claims 1-16 and 18-23 are allowed.

4. The following is an examiner's statement of reasons for allowance:

Claims 1 and 9 were allowed by the examiner in the action of 6/23/15. The reasoning is repeated below.

Claim 1 recites "A semiconductor device comprising:

a gate electrode layer;

a gate insulating layer on one surface of the gate electrode layer;

a semiconductor layer on one surface of the gate insulating layer;

a first conductive layer over the semiconductor layer;

a second conductive layer over the first conductive layer;

a first insulating layer over the second conductive layer; and

a hard mask layer over the first insulating layer,

wherein the hard mask layer comprises an opening which overlaps with a channel formation region of the semiconductor layer.

This is not taught or suggested by the prior art of record. Yamazaki (US 2011/0114943) does not form all the layers required. Yamazaki does not form an insulating layer between the electrode and the first conductive layer. Also, there is no teaching of the

formation of a hard mask and a resist. Layer 108 can be referred to as either the hard mask or the protective layer, but it cannot be both. Similarly, Yoshimoto ((US 2008/0062344) does not form all the required layers.

Claims 2-8 and 21 are allowed as being properly dependent upon allowed claim 1.

Claim 9 recites, "A semiconductor device comprising:

a gate electrode layer;

a gate insulating layer over the gate electrode layer;

a semiconductor layer over the gate insulating layer;

a first conductive layer and a second conductive layer over the semiconductor layer;

a third conductive layer over the first conductive layer;

a fourth conductive layer over the second conductive layer; and

a first insulating layer over the third conductive layer and the fourth conductive layer,

wherein a distance between the first conductive layer and the second conductive layer is shorter than a distance between the third conductive layer and the fourth conductive layer, and

wherein the first conductive layer and the third conductive layer serve as a source

electrode and the second conductive layer and the fourth conductive layer serve as a drain electrode.

This is not taught or suggested by the prior art of record. Yamazaki (US 2011/0114943) does not form all the layers required. Yamazaki does not form an insulating layer between the electrode and the first conductive layer. Also, there is no teaching of the formation of a hard mask and a resist. Layer 108 can be referred to as either a hard mask or a protective layer, but it cannot be both. Similarly, Yoshimoto ((US 2008/0062344) does not form all the required layers.

Claims 10-14 and 22 are allowed as being properly dependent upon allowed claim 9.

Claim 15 is allowed for reasons set forth by the applicant in the paper filed 9/21/15. In particular, “With respect to independent claim 15, the prior art to Yamazaki has not been shown to necessarily teach or suggest all the features of the independent claim, as amended. Specifically, the Patent Office alleges that FIG. 1 of Yamazaki teaches a transistor structure as recited in claim 15, except for exact dimensions. However, claim 15 as amended now recites a hard mask layer over the first conductive layer and the second conductive layer, wherein an entire upper surface of the hard mask layer is flat. These features are supported, for example, by at least Applicant's FIG. 1B (e.g., element 495). Claim 17 has been accordingly canceled. Applicant's paragraph [0091] provides the following advantage for the flatness: *"The surface of the hard mask layer*

*495 is flat. Therefore, even a resist as thin as about 30 nm can be uniformly applied on the surface where the resist is to be applied."*

Claims 16, 18-20, and 23 are allowed as being properly dependent upon allowed claim 15.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

### *Conclusion*

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, William Kraig, can be reached at (571)-272-8660. Our facsimile number all patent correspondence to be entered into an application is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/David S Blum/

Primary Examiner, Art Unit 2813

October 26, 2015

**EAST Search History**

**EAST Search History (Prior Art)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L4 | 16332 | H01L29/78.cpc. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 12:10 |
| L5 | 3138 | H01L29/66477.cpc. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 12:10 |
| L6 | 4596 | (257/43).CCLS. | US-PGPUB; USPAT | OR | OFF | 2015/10/19 12:10 |
| L7 | 4574 | L6 not L5 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 12:12 |
| L8 | 15134 | L4 not L6 not L5 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 12:12 |
| S1 | 652 | semiconductor and (gate adj electrode) and (gate adj insulat$4) and conductive and protective and ((hard adj mask) and resist same etch$3) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 10:02 |
| S2 | 454 | (Shinya near2 Sasagawa).in. or (Hideom near2 Suzawa).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 10:20 |
| S3 | 1051 | (Shinya near2 Sasagawa).in. or (Hideomi near2 Suzawa).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 10:21 |
| S4 | 19370 | Semiconductor adj energy adj Laboratory | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 10:45 |
| S5 | 3335 | S4 and (oxide adj semiconductor) and (channel adj length) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 10:45 |
| S6 | 3242 | S5 and (gate adj electrode) | US-PGPUB; USPAT; USOCR; | ADJ | ON | 2015/10/19 10:46 |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | FPRS; EPO; JPO; DERWENT; IBM_TDB | | | |

**EAST Search History (Interference)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L9 | 265 | semiconductor and (gate adj electrode) and (gate adj insulat$4) and conductive and protective and ((hard adj mask) and resist same etch$3) | USPAT | ADJ | ON | 2015/10/19 12:13 |
| L10 | 651 | semiconductor and (gate adj electrode) and (gate adj insulat$4) and conductive and protective and ((hard adj mask) and resist same etch$3) | US-PGPUB; USPAT | ADJ | ON | 2015/10/19 12:13 |

**10/19/2015 12:14:17 PM**

## EAST Search History

### EAST Search History (Prior Art)

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L2 | 13157 | H01L29/7869.cpc. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 17:27 |
| L3 | 16332 | H01L29/78.cpc. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 17:28 |
| L4 | 3138 | H01L29/66477.cpc. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 17:28 |
| L5 | 4596 | (257/43).CCLS. | US-PGPUB; USPAT | OR | OFF | 2015/10/19 17:28 |
| L6 | 10560 | L2 not L3 not L4 not L5 | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/10/19 17:28 |

### EAST Search History (Interference)

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 1 | "14337583" | US-PGPUB; USPAT | ADJ | ON | 2015/10/19 17:25 |

**10/19/2015 5:29:08 PM**

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

# BIB DATA SHEET

**CONFIRMATION NO. 7546**

| SERIAL NUMBER | FILING or 371(c) DATE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 14/337,583 | 07/22/2014<br>RULE | 438 | 2813 | 0756-10540 |

**APPLICANTS**
Semiconductor Energy Laboratory Co., Ltd., Atsugi-shi, JAPAN;

**INVENTORS**
Shinya SASAGAWA, Chigasaki, JAPAN;
Hideomi SUZAWA, Atsugi, JAPAN;

** **CONTINUING DATA** *************************
This application is a DIV of 13/716,891 12/17/2012 PAT 8790961

** **FOREIGN APPLICATIONS** *************************
JAPAN 2011-282438 12/23/2011
JAPAN 2011-282511 12/23/2011

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** **
07/31/2014

| Foreign Priority claimed ☑ Yes ☐ No<br>35 USC 119(a-d) conditions met ☑ Yes ☐ No<br>Verified and Acknowledged /DAVID S BLUM/ Examiner's Signature | ☐ Met after Allowance<br>Initials | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|
| | | JAPAN | 17 | 20 | 3 |

**ADDRESS**

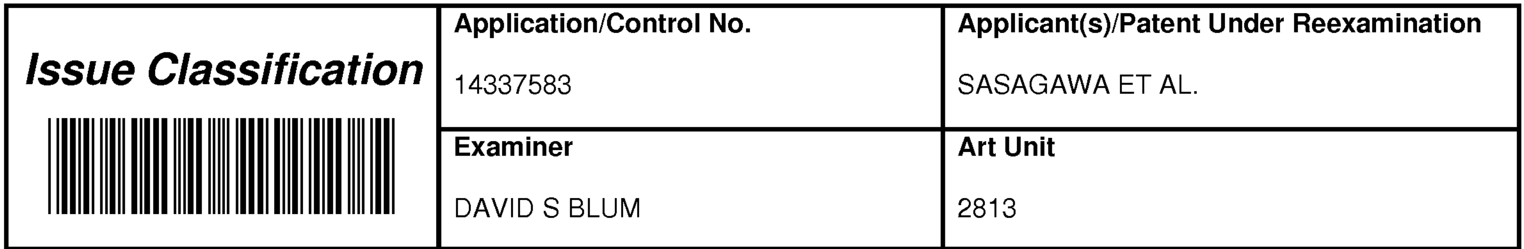
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033
UNITED STATES

**TITLE**

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

| FILING FEE RECEIVED | FEES: Authority has been given in Paper | |
|---|---|---|
| 1760 | No.____________ to charge/credit DEPOSIT ACCOUNT<br>No.____________ for following: | ☐ All Fees<br>☐ 1.16 Fees (Filing)<br>☐ 1.17 Fees (Processing Ext. of time)<br>☐ 1.18 Fees (Issue)<br>☐ Other ________________<br>☐ Credit |

BIB (Rev. 05/07).



| *Issue Classification* | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 14337583 | SASAGAWA ET AL. |
| | **Examiner** | **Art Unit** |
| | DAVID S BLUM | 2813 |

**CPC**

| Symbol | | | | | Type | Version |
|---|---|---|---|---|---|---|
| H01L | | 29 | / | 7869 | F | 2013-01-01 |
| H01L | | 29 | / | 66477 | I | 2013-01-01 |
| H01L | | 29 | / | 78 | I | 2013-01-01 |
| H01L | | 27 | / | 1156 | A | 2013-01-01 |
| H01L | | 29 | / | 41733 | I | 2013-01-01 |
| H01L | | 29 | / | 78606 | I | 2013-01-01 |
| H01L | | 29 | / | 78636 | I | 2013-01-01 |
| H01L | | 29 | / | 78696 | I | 2013-01-01 |
| H01L | | 29 | / | 66969 | I | 2013-01-01 |
| H01L | | 29 | / | 1033 | I | 2013-01-01 |
| H01L | | 29 | / | 24 | I | 2013-01-01 |
| H01L | | 29 | / | 42356 | I | 2013-01-01 |
| | | | / | | | |
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**CPC Combination Sets**

| Symbol | | | | | Type | Set | Ranking | Version |
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| | | | / | | | | | |
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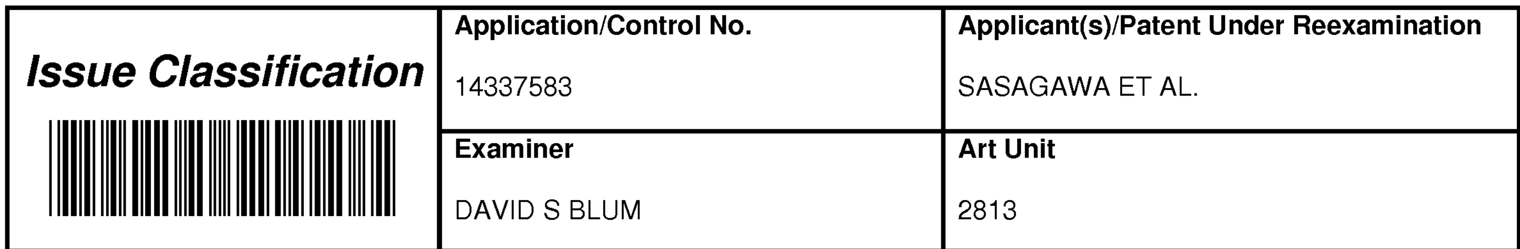
|---|---|---|---|
| NONE<br><br>(Assistant Examiner) | (Date) | **Total Claims Allowed:**<br><br>22 | |
| /DAVID S BLUM/<br>Primary Examiner.Art Unit 2813<br><br>(Primary Examiner) | 10/19/15<br><br>(Date) | O.G. Print Claim(s)<br><br>1 | O.G. Print Figure<br><br>1B |



| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 14337583 | SASAGAWA ET AL. |
| | **Examiner** | **Art Unit** |
| | DAVID S BLUM | 2813 |

| US ORIGINAL CLASSIFICATION | | INTERNATIONAL CLASSIFICATION | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CLASS | SUBCLASS | CLAIMED | | | | | NON-CLAIMED | | | | |
| 257 | 43 | H | 0 | 1 | L | 29 / 80 (2006.01.01) | | | | | |
| CROSS REFERENCE(S) | | H | 0 | 1 | L | 31 / 0288 (2006.01.01) | | | | | |
| | | H | 0 | 1 | L | 31 / 112 (2006.01.01) | | | | | |
| CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) | | | | | | | | | | |

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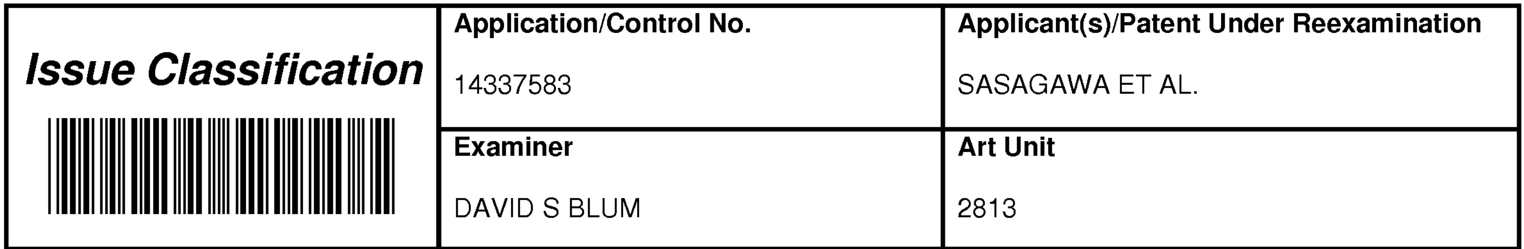
|---|---|---|
| NONE<br><br>(Assistant Examiner) | (Date) | **Total Claims Allowed:**<br>22 |
| /DAVID S BLUM/<br>Primary Examiner.Art Unit 2813<br><br>(Primary Examiner) | 10/19/15<br><br>(Date) | O.G. Print Claim(s): 1 / O.G. Print Figure: 1B |



| **Issue Classification** | **Application/Control No.** | **Applicant(s)/Patent Under Reexamination** |
|---|---|---|
| | 14337583 | SASAGAWA ET AL. |
| | **Examiner** | **Art Unit** |
| | DAVID S BLUM | 2813 |

☐ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

| Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | | 17 | | | | | | | | | | | | |
| 2 | 2 | 19 | 18 | | | | | | | | | | | | |
| 3 | 3 | 20 | 19 | | | | | | | | | | | | |
| 4 | 4 | 21 | 20 | | | | | | | | | | | | |
| 5 | 5 | 9 | 21 | | | | | | | | | | | | |
| 6 | 6 | 16 | 22 | | | | | | | | | | | | |
| 7 | 7 | 22 | 23 | | | | | | | | | | | | |
| 8 | 8 | | | | | | | | | | | | | | |
| 10 | 9 | | | | | | | | | | | | | | |
| 11 | 10 | | | | | | | | | | | | | | |
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| 15 | 14 | | | | | | | | | | | | | | |
| 17 | 15 | | | | | | | | | | | | | | |
| 18 | 16 | | | | | | | | | | | | | | |

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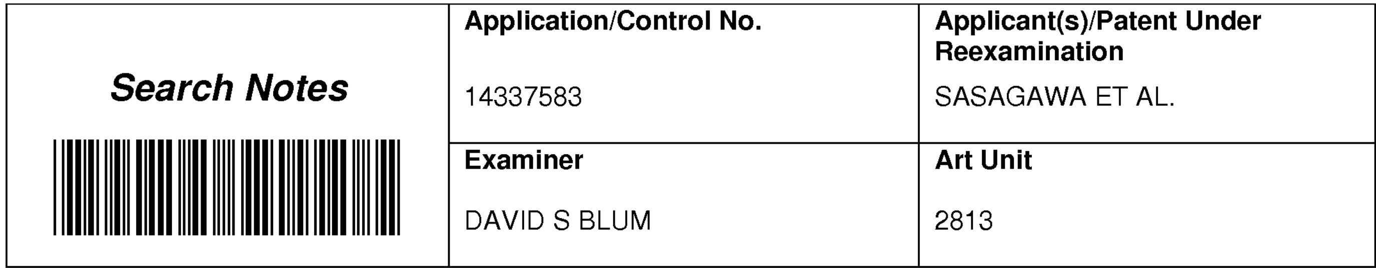
|---|---|---|---|
| NONE<br><br>(Assistant Examiner) | (Date) | **Total Claims Allowed:**<br><br>22 | |
| /DAVID S BLUM/<br>Primary Examiner.Art Unit 2813<br><br>(Primary Examiner) | 10/19/15<br><br>(Date) | O.G. Print Claim(s)<br><br>1 | O.G. Print Figure<br><br>1B |



| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 14337583 | SASAGAWA ET AL. |
| | **Examiner** | **Art Unit** |
| | DAVID S BLUM | 2813 |

## CPC- SEARCHED

| Symbol | Date | Examiner |
|---|---|---|
| H01L 29/78, 29/166477 | 6/11/15 | DSB |
| H01L 29/78, 29/166477 | 10/19/15 | DSB |
| H01L 29/7869 | 10/19/15 | DSB |

## CPC COMBINATION SETS - SEARCHED

| Symbol | Date | Examiner |
|---|---|---|
| | | |

## US CLASSIFICATION SEARCHED

| Class | Subclass | Date | Examiner |
|---|---|---|---|
| 257 | 43 | 6/11/15 | DSB |
| 257 | 43 | 10/19/15 | DSB |

## SEARCH NOTES

| Search Notes | Date | Examiner |
|---|---|---|
| 13/716891 | 6/11/15 | DSB |
| EAST (attached) | 6/11/15 | DSB |
| Inventor name search | 6/11/15 | DSB |
| Company name search | 6/11/15 | DSB |
| 13/716891 | 10/19/15 | DSB |
| EAST (attached) | 10/19/15 | DSB |
| Inventor name search | 10/19/15 | DSB |
| Company name search | 10/19/15 | DSB |

## INTERFERENCE SEARCH

| US Class/ CPC Symbol | US Subclass / CPC Group | Date | Examiner |
|---|---|---|---|
| H01L | 29/78, 29/166477 | 10/19/15 | DSB |
| H01L | 29/7869 | 10/19/15 | DSB |

| | /DAVID S BLUM/<br>Primary Examiner.Art Unit 2813 |
|---|---|

## INTERFERENCE SEARCH

| US Class/ CPC Symbol | US Subclass / CPC Group | Date | Examiner |
|---|---|---|---|
| 257 | 43 | 10/19/15 | DSB |

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|---|---|
| | /DAVID S BLUM/<br>Primary Examiner.Art Unit 2813 |

Attorney Docket No. 0756-10540

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | |
|---|---|---|
| In re Patent Application of: | ) | Confirmation No. 7546 |
| Shinya SASAGAWA et al. | ) | Group Art Unit: 2813 |
| Serial No. 14/337,583 | ) | Examiner: David S. Blum |
| Filed: July 22, 2014 | ) | |
| For: SEMICONDUCTOR DEVICE AND | ) | |
| METHOD FOR MANUFACTURING | ) | |
| THE SAME | ) | |

## AMENDMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action dated June 23, 2015, please consider the following amendments and remarks in connection with the above-identified application.

**Amendments to the Claims** are reflected in the listing of claims, which begins on page 2 of this paper.

**Remarks** begin on page 7 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A semiconductor device comprising:

a gate electrode layer;

a gate insulating layer ~~on one surface of~~ over the gate electrode layer;

a semiconductor layer ~~on one surface of~~ over the gate insulating layer;

a first conductive layer over the semiconductor layer;

a second conductive layer over the first conductive layer;

a ~~protective~~ first insulating layer over the second conductive layer; and

a hard mask layer over the ~~protective~~ first insulating layer,

wherein the hard mask layer comprises an opening which overlaps with a channel formation region of the semiconductor layer.

2. (Original) The semiconductor device according to claim 1,

wherein the semiconductor layer includes an oxide including In, an element *M*, and Zn, and

wherein the element *M* is at least one element selected from the group consisting of Ga, Sn, Hf, Al, Zr, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu.

3. (Original) The semiconductor device according to claim 1, wherein the hard mask layer comprises amorphous silicon.

4. (Original) The semiconductor device according to claim 1, wherein a thickness of the semiconductor layer is greater than or equal to 5 nm and less than or equal to 30 nm.

5. (Original) The semiconductor device according to claim 1, wherein a channel length of a transistor including the semiconductor layer is greater than or equal to 20 nm and less than or equal to 100 nm.

6. (Original) The semiconductor device according to claim 1, wherein a length of the semiconductor layer in a channel length direction is larger than a length of the gate electrode layer in the channel length direction.

7. (Original) The semiconductor device according to claim 1, wherein a width of the opening is substantially the same as a length of the semiconductor layer in a channel length direction.

8. (Original) The semiconductor device according to claim 1, wherein the semiconductor layer is located over the gate electrode layer.

9. (Currently Amended) A semiconductor device comprising:

a gate electrode layer;

a gate insulating layer ~~on one surface of~~ over the gate electrode layer;

a semiconductor layer ~~on one surface of~~ over the gate insulating layer;

a first conductive layer and a second conductive layer over the semiconductor layer;

a third conductive layer over the first conductive layer;

a fourth conductive layer over the second conductive layer; and

a ~~protective~~ first insulating layer over the third conductive layer and the fourth conductive layer,

wherein a distance between the first conductive layer and the second conductive layer is shorter than a distance between the third conductive layer and the fourth conductive layer, and

wherein the first conductive layer and the third conductive layer serve as a source electrode and the second conductive layer and the fourth conductive layer serve as a drain electrode.

10. (Original) The semiconductor device according to claim 9,

wherein the semiconductor layer includes an oxide including In, an element *M*, and Zn, and

wherein the element *M* is at least one element selected from the group consisting of Ga, Sn, Hf, Al, Zr, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu.

11. (Original) The semiconductor device according to claim 9, wherein a thickness of the semiconductor layer is greater than or equal to 5 nm and less than or equal to 30 nm.

12. (Original) The semiconductor device according to claim 9, wherein a channel length of a transistor including the semiconductor layer is greater than or equal to 20 nm and less than or equal to 100 nm.

13. (Original) The semiconductor device according to claim 9, wherein a length of the semiconductor layer in a channel length direction is larger than a length of the gate electrode layer in the channel length direction.

14. (Original) The semiconductor device according to claim 9, wherein the semiconductor layer is located over the gate electrode layer.

15. (Currently Amended) A semiconductor device comprising:

a gate electrode layer adjacent to an oxide semiconductor layer;

the oxide semiconductor layer comprising a channel formation region;

a first conductive layer over and in contact with a first portion of the oxide semiconductor layer;

a second conductive layer over and in contact with a second portion of the oxide semiconductor layer; [[and]]

a hard mask layer over the first conductive layer and the second conductive layer, wherein an entire upper surface of the hard mask layer is flat; and

a silicon oxynitride film over the hard mask layer ~~first conductive layer and the second conductive layer~~,

wherein the silicon oxynitride film is in contact with a third portion of the oxide semiconductor layer between the first portion and the second portion, and

wherein the third portion includes the channel formation region[[, and]]

~~wherein a channel length of a transistor including the oxide semiconductor layer is less than or equal to 30 nm with use of a photolithography process using an electron beam~~.

16. (Original) The semiconductor device according to claim 15,

wherein the oxide semiconductor layer includes In, an element *M*, and Zn, and

wherein the element *M* is at least one element selected from the group consisting of Ga, Sn, Hf, Al, Zr, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu.

17. (Canceled)

18. (Currently Amended) The semiconductor device according to claim 15 [[17]], wherein the hard mask layer comprises amorphous silicon.

19. (Original) The semiconductor device according to claim 15, wherein a thickness of the oxide semiconductor layer is greater than or equal to 5 nm and less than or equal to 30 nm.

20. (Original) The semiconductor device according to claim 15, wherein the oxide semiconductor layer is formed over the gate electrode layer.

21. (New) The semiconductor device according to claim 1, wherein the first insulating layer is a protective layer.

22. (New) The semiconductor device according to claim 9, wherein the first insulating layer is a protective layer.

23. (New) The semiconductor device according to claim 15, wherein a channel length of a transistor including the oxide semiconductor layer is less than or equal to 30 nm.

## REMARKS

The Official Action mailed June 23, 2015, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statement filed on August 18, 2014.

Claims 1-20 were pending in the present application prior to the above amendment. The Applicant notes with appreciation the indication of the allowability of claims 18 and 20, and the allowance of claims 1-14. Claim 17 has been canceled without prejudice or disclaimer, claims 1, 9, 15 and 18 have been amended to better recite the features of the present invention and new claims 21-23 have been added to recite additional protection to which the Applicant is entitled. Accordingly, claims 1-16 and 18-23 are now pending in the present application, of which claims 1, 9 and 15 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Allowed independent claims 1 and 9 have been revised to clarify "over" relationships and to rephrase "protective layer" as a "first insulating layer." Claims 1-14 are believed to remain allowable for reasons already of record.

Paragraph 4 of the Official Action rejects claims 15-17 and 19 as obvious based on U.S. Publication No. 2011/0114943 to Yamazaki. The Applicant respectfully traverses the rejection because a *prima facie* case of obviousness cannot be maintained against independent claim 15 of the present application, as amended.

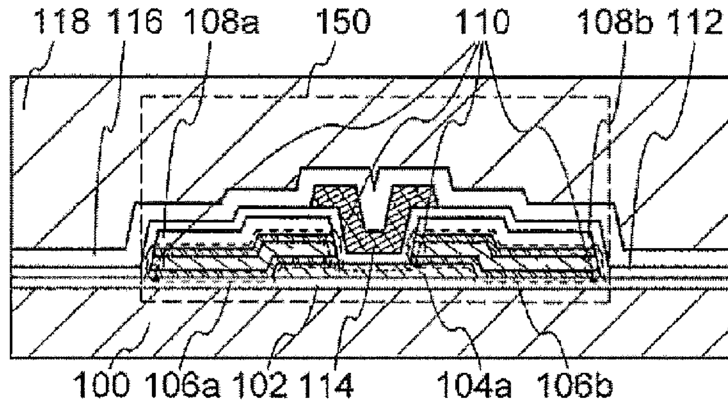
As stated in MPEP §§ 2142-2144.04, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or

references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some reason to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

With respect to independent claim 15, the prior art to Yamazaki has not been shown to necessarily teach or suggest all the features of the independent claim, as amended. Specifically, the Patent Office alleges that FIG. 1 of Yamazaki teaches a transistor structure as recited in claim 15, except for exact dimensions. However, claim 15 as amended now recites a hard mask layer over the first conductive layer and the second conductive layer, wherein an entire upper surface of the hard mask layer is flat. These features are supported, for example, by at least Applicant's FIG. 1B (e.g., element 495). Claim 17 has been accordingly canceled. Applicant's paragraph [0091] provides the following advantage for the flatness: *"The surface of the hard mask layer 495 is flat. Therefore, even a resist as thin as about 30 nm can be uniformly applied on the surface where the resist is to be applied."*

In rejecting dependent claim 17, which recited a hard mask layer generally, the Patent Office asserted insulating layers 108ab of Yamazaki as the corresponding hard mask layer. However, when viewed in light of FIG. 1 of Yamazaki (below), one skilled in the art would understand that the alleged insulating layers 108ab of Yamazaki are formed over a level difference caused by an island-shaped oxide semiconductor layer 104a. Thus, the prior art appears to be silent with respect to the clarified "flat" hard mask layer claim feature.

FIG. 1



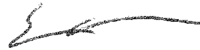

Because Yamazaki has not been shown to teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained with respect to independent claim 15. Therefore, Applicant believes the rejection of claim 15 and claims dependent therefrom is not proper. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are in order and respectfully requested.

New claims 21-23 have been added to recite additional protection to which the Applicant is entitled. The features of claims 21-22 are supported by previous claims 1 and 9. The features of claim 23 relate to a feature redacted from pending claim 15. For the reasons stated above, the Applicant respectfully submits that new claims 21-23 are in condition for allowance.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



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# Electronic Patent Application Fee Transmittal

| | |
|---|---|
| **Application Number:** | 14337583 |
| **Filing Date:** | 22-Jul-2014 |
| **Title of Invention:** | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME |
| **First Named Inventor/Applicant Name:** | Shinya SASAGAWA |
| **Filer:** | Eric J. Robinson/Jennifer Rosenfeld |
| **Attorney Docket Number:** | 0756-10540 |

Filed as Large Entity

**Filing Fees for** **Utility under 35 USC 111(a)**

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| **Pages:** | | | | |
| **Claims:** | | | | |
| Claims in Excess of 20 | 1202 | 2 | 80 | 160 |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
| --- | --- | --- | --- | --- |
| **Extension-of-Time:** | | | | |
| **Miscellaneous:** | | | | |
| | | **Total in USD ($)** | | **160** |

# Electronic Acknowledgement Receipt

| | |
|---|---|
| **EFS ID:** | 23552428 |
| **Application Number:** | 14337583 |
| **International Application Number:** | |
| **Confirmation Number:** | 7546 |
| **Title of Invention:** | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME |
| **First Named Inventor/Applicant Name:** | Shinya SASAGAWA |
| **Customer Number:** | 31780 |
| **Filer:** | Eric J. Robinson/Jennifer Rosenfeld |
| **Filer Authorized By:** | Eric J. Robinson |
| **Attorney Docket Number:** | 0756-10540 |
| **Receipt Date:** | 21-SEP-2015 |
| **Filing Date:** | 22-JUL-2014 |
| **Time Stamp:** | 15:14:50 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | yes |
| Payment Type | Electronic Funds Transfer |
| Payment was successfully received in RAM | $160 |
| RAM confirmation Number | 1731 |
| Deposit Account | |
| Authorized User | |

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Amendment/Req. Reconsideration-After Non-Final Reject | AMENDMENT_21SEP2015.pdf | 1228163<br>1638847b219253e0573c8c8e852d2336b00db8fd | no | 10 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | Fee Worksheet (SB06) | fee-info.pdf | 30602<br>4b907319239d3b05e760829a5936706cf8fa377e | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | **Total Files Size (in bytes):** | 1258765 | | |

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**New Applications Under 35 U.S.C. 111**
**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

| **PATENT APPLICATION FEE DETERMINATION RECORD** Substitute for Form PTO-875 | Application or Docket Number 14/337,583 | Filing Date 07/22/2014 | ☐ To be Mailed |
|---|---|---|---|

**ENTITY**: ☒ LARGE ☐ SMALL ☐ MICRO

## APPLICATION AS FILED – PART I

| FOR | NUMBER FILED (Column 1) | NUMBER EXTRA (Column 2) | RATE ($) | FEE ($) |
|---|---|---|---|---|
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | X $ = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | X $ = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| AMENDMENT | 09/21/2015 | CLAIMS REMAINING AFTER AMENDMENT (Column 1) | | HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2) | PRESENT EXTRA (Column 3) | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * 22 | Minus | ** 20 | = 2 | x $80 = | 160 |
| | Independent (37 CFR 1.16(h)) | * 3 | Minus | ***3 | = 0 | x $420 = | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | |
| | | | | | | TOTAL ADD'L FEE | **160** |

| AMENDMENT | | CLAIMS REMAINING AFTER AMENDMENT (Column 1) | | HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2) | PRESENT EXTRA (Column 3) | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | X $ = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | |
| | | | | | | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/PAMELA YOUNG/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 14/337,583 | 07/22/2014 | Shinya SASAGAWA | 0756-10540 | 7546 |

31780 7590 06/23/2015
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

| EXAMINER | |
|---|---|
| BLUM, DAVID S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2813 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 06/23/2015 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| *Office Action Summary* | **Application No.**<br>14/337,583 | **Applicant(s)**<br>SASAGAWA ET AL. | |
|---|---|---|---|
| | **Examiner**<br>DAVID S. BLUM | **Art Unit**<br>2813 | **AIA (First Inventor to File) Status**<br>No |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *7/22/14*.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims***

5)☒ Claim(s) *1-20* is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *1-14* is/are allowed.

7)☒ Claim(s) *15-17 and 19* is/are rejected.

8)☒ Claim(s) *18 and 20* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

**Application Papers**

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *7/22/14* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

a)☒ All b)☐ Some** c)☐ None of the:

1.☒ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date *8/18/14*.

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.


BLUEHOUSE EXHIBIT 1002

This action is in response to the application filed 7/22/14.

### *Notice of Pre-AIA or AIA Status*

1. The present application is being examined under the pre-AIA first to invent provisions.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

2. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

3. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 15-17 and 19 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US 2011/0114943).

Yamazaki teaches the device of claims 15-17 and 19 except for exact dimensions.

Regarding claim 15, Yamazaki teaches

A semiconductor device comprising:

a gate electrode layer (114) adjacent to an oxide semiconductor layer (104);

the oxide semiconductor layer comprising a channel formation region (paragraph 0142 indicates the oxide semiconductor is the channel, see figure 1);

a first conductive layer (106a) over and in contact with a first portion of the oxide semiconductor layer;

a second conductive layer (106b) over and in contact with a second portion of the oxide semiconductor layer; and

a silicon oxynitride film (112) over the first conductive layer and the second conductive layer,

wherein the silicon oxynitride film is in contact with a third portion of the oxide semiconductor layer between the first portion and the second portion (figure 1),

wherein the third portion includes the channel formation region (figure 1), and

wherein a channel length of a transistor including the oxide semiconductor layer is less than or equal to 30 nm with use of a photolithography process using an electron beam.

The limitation, “with use of a photolithography process using an electron beam” refers to a process method for making the device (product by process) and is given patentable weight only as to how it reads on the structure.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production.” MPEP 2113

Yamazaki does not teach the dimensions as claimed, teaching larger channel lengths. However, Yamazaki also teaches the channel length is based upon the threshold voltage, therefore one making transistors meant for lower voltages would know to and know how to determine an appropriate channel length. This is easily determined by one skilled in the art by usage of equations or routine experimentation.

These ranges are considered to involve routine optimization while it has been held to be within the level of ordinary skill in the art. As noted in In re Aller (105 USPQ233), the selection of reaction parameters such as temperature and concentration would have been obvious:

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art. Such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ

372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

One skilled in the requisite art at the time of the invention would have used any ranges or exact figures suitable to the transistor device regarding dimensions using prior knowledge, experimentation, and observation with the apparatus used in order to optimize the process and produce the transistor structure desired to the parameters desired.

Regarding clam 16, the oxide semiconductor layer includes In, an element M, and Zn, and wherein the element M is at least one element selected from the group consisting of Ga, Sn, Hf, Al, Zr, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu (paragraph 0069).

Regarding claim 17, a hard mask layer over the first conductive layer and the second conductive layer (108, paragraph 0109 refers to layer 108 as a mask as it prevents oxidation of conductive layers 106a and 106b. The function of the layers reads toward the structure as for location).

Regarding claim 19, wherein a thickness of the oxide semiconductor layer is greater than or equal to 5 nm and less than or equal to 30 nm (paragraph 0075, 2-200 nm).

5. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 18 recites “The semiconductor device according to claim 17, wherein the hard mask layer comprises amorphous silicon.” This is not taught or suggested by the prior art of record. Yamazaki (US 2011/0114943) teaches the mask layer to be silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide, hafnium oxide, tantalum oxide or the like, but does not teach or suggest the layer may be amorphous silicon.

6. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 20 recites, “The semiconductor device according to claim 15, wherein the oxide semiconductor layer is formed over the gate electrode layer.” This is not taught or suggested by the prior art of record. Yamazaki (US 2011/0114943) does not form all the layers required. Yamazaki does not form an insulating layer between the electrode and the first conductive layer. Also, there is no teaching of the formation of a hard mask and a resist. Layer 108 can be referred to as either a hard mask or a protective layer, but it cannot be both. Similarly, Yoshimoto ((US 2008/0062344) does not form all the required layers.

7. Claims 1-14 are allowed.

Claim 1 recites “A semiconductor device comprising:

a gate electrode layer;

a gate insulating layer on one surface of the gate electrode layer;

a semiconductor layer on one surface of the gate insulating layer;

a first conductive layer over the semiconductor layer;

a second conductive layer over the first conductive layer;

a protective layer over the second conductive layer; and

a hard mask layer over the protective layer,

wherein the hard mask layer comprises an opening which overlaps with a channel formation region of the semiconductor layer.

This is not taught or suggested by the prior art of record. Yamazaki (US 2011/0114943) does not form all the layers required. Yamazaki does not form an insulating layer between the electrode and the first conductive layer. Also, there is no teaching of the formation of a hard mask and a resist. Layer 108 can be referred to as either a hard mask or a protective layer, but it cannot be both. Similarly, Yoshimoto ((US 2008/0062344) does not form all the required layers.

Claims 2-8 are allowed as being properly dependent upon allowed claim 1.

Claim 9 recites, “A semiconductor device comprising:

a gate electrode layer;

a gate insulating layer on one surface of the gate electrode layer;

a semiconductor layer on one surface of the gate insulating layer;

a first conductive layer and a second conductive layer over the semiconductor layer;

a third conductive layer over the first conductive layer;

a fourth conductive layer over the second conductive layer; and

a protective layer over the third conductive layer and the fourth conductive layer,

wherein a distance between the first conductive layer and the second conductive layer is shorter than a distance between the third conductive layer and the fourth conductive layer, and

wherein the first conductive layer and the third conductive layer serve as a source electrode and the second conductive layer and the fourth conductive layer serve as a drain electrode.

This is not taught or suggested by the prior art of record. Yamazaki (US 2011/0114943) does not form all the layers required. Yamazaki does not form an insulating layer between the electrode and the first conductive layer. Also, there is no teaching of the formation of a hard mask and a resist. Layer 108 can be referred to as either a hard mask or a protective layer, but it cannot be both. Similarly, Yoshimoto ((US 2008/0062344) does not form all the required layers.

Claims 10-14 are allowed as being properly dependent upon allowed claim 9.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Kraig, can be reached at (571)-272-8660. Our facsimile number all patent correspondence to be entered into an application is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/David S Blum/

Primary Examiner, Art Unit 2813

June 19, 2015

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**APPLICANTS**
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**INVENTORS**
Shinya SASAGAWA, Chigasaki, JAPAN;
Hideomi SUZAWA, Atsugi, JAPAN;

** **CONTINUING DATA** *************************
This application is a DIV of 13/716,891 12/17/2012 PAT 8790961

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07/31/2014

| Foreign Priority claimed ☑ Yes ☐ No<br>35 USC 119(a-d) conditions met ☑ Yes ☐ No<br>Verified and Acknowledged /DAVID S BLUM/ Examiner's Signature | ☐ Met after Allowance<br>Initials | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|
| | | JAPAN | 17 | 20 | 3 |

**ADDRESS**

Robinson Intellectual Property Law Office, P.C.
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**TITLE**

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

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| Examiner Signature | /David S. Blum/ | Date Considered | 06/11/2015 |
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| Examiner Signature | /David S. Blum/ | Date Considered | 06/11/2015 |
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Sheet 6 of 15

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| Application Number | 14/337,583 |
| Filing Date | July 22, 2014 |
| First Named Inventor | Shinya SASAGAWA |
| Art Unit | 2813 |
| Examiner Name | BLUM |
| Attorney Docket Number | 0756-10540 |

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| | | | | Filing Date | July 22, 2014 |
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| Sheet | 9 | of | 15 | Attorney Docket Number | 0756-10540 |

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| **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** | | | | Application Number | 14/337,583 |
| | | | | Filing Date | July 22, 2014 |
| | | | | First Named Inventor | Shinya SASAGAWA |
| (Use as many sheets as necessary) | | | | Art Unit | 2813 |
| | | | | Examiner Name | BLUM |
| Sheet | 11 | of | 15 | Attorney Docket Number | 0756-10540 |

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| Examiner Signature | /David S. Blum/ | Date Considered | 06/11/2015 |
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| Examiner Name | BLUM |
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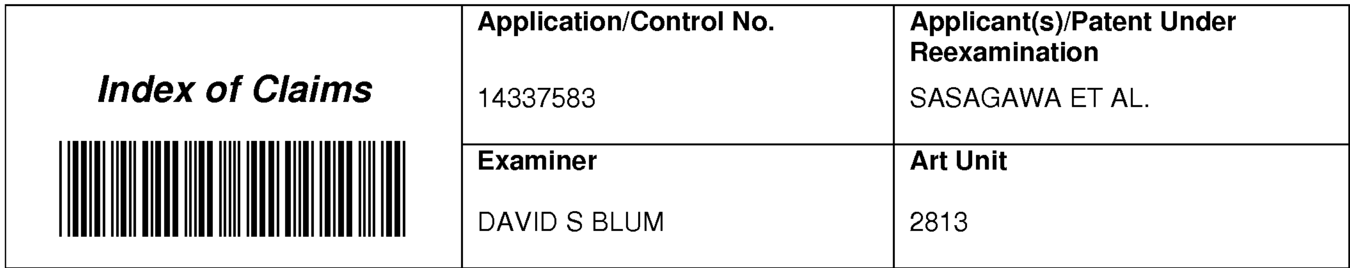

| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 14337583 | SASAGAWA ET AL. |
| | **Examiner** | **Art Unit** |
| | DAVID S BLUM | 2813 |

| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal |
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| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
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| | 17 | ✓ | | | | | | | | |
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| | 19 | ✓ | | | | | | | | |
| | 20 | O | | | | | | | | |

**EAST Search History**

**EAST Search History (Prior Art)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 2 | "20110114943" | US-PGPUB; USPAT | ADJ | ON | 2015/06/11 10:25 |
| L2 | 3 | "13716891" | US-PGPUB; USPAT | ADJ | ON | 2015/06/11 10:48 |
| L3 | 463 | "L3" and (hard adj mask) | US-PGPUB; USPAT | ADJ | ON | 2015/06/11 10:48 |
| L4 | 3 | L2 and (hard adj mask) | US-PGPUB; USPAT | ADJ | ON | 2015/06/11 10:49 |
| L5 | 610 | semiconductor and (gate adj electrode) and (gate adj insulat$4) and conductive and protective and ((hard adj mask) and resist same etch$3) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/06/11 11:06 |
| L6 | 1018 | (Shinya near2 Sasagawa).in. or (Hideomi near2 Suzawa).in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/06/11 11:13 |
| L7 | 18572 | Semiconductor adj energy adj Laboratory | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/06/11 11:14 |
| L8 | 5128 | L7 and (oxide adj semiconductor) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/06/11 11:14 |
| L9 | 4971 | L8 and channel | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/06/11 11:14 |
| L10 | 2878 | L9 and (channel adj length) and (gate adj electrode) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | ADJ | ON | 2015/06/11 11:15 |
| L11 | 4307 | (257/43).CCLS. | US-PGPUB; USPAT | OR | OFF | 2015/06/11 11:16 |
| L12 | 6544 | H01L29/78.cpc. | US-PGPUB; USPAT | ADJ | ON | 2015/06/11 11:16 |
| L13 | 1324 | H01L29/66477.cpc. | US-PGPUB; USPAT | ADJ | ON | 2015/06/11 11:17 |
| L14 | 4307 | L11 not "L13." | US-PGPUB; USPAT | ADJ | ON | 2015/06/11 11:17 |
| L15 | 6074 | L12 not L11 not L13 | US-PGPUB; USPAT | ADJ | ON | 2015/06/11 11:18 |

**EAST Search History (Interference)**

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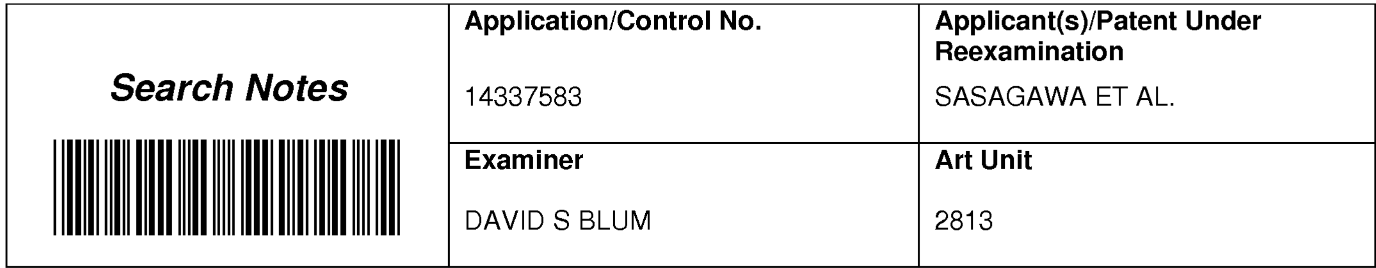

| Search Notes | Application/Control No. 14337583 | Applicant(s)/Patent Under Reexamination SASAGAWA ET AL. |
|---|---|---|
| | Examiner DAVID S BLUM | Art Unit 2813 |

## CPC- SEARCHED

| Symbol | Date | Examiner |
|---|---|---|
| H01L 29/78, 29/166477 | 6/11/15 | DSB |

## CPC COMBINATION SETS - SEARCHED

| Symbol | Date | Examiner |
|---|---|---|
| | | |

## US CLASSIFICATION SEARCHED

| Class | Subclass | Date | Examiner |
|---|---|---|---|
| 257 | 43 | 6/11/15 | DSB |

## SEARCH NOTES

| Search Notes | Date | Examiner |
|---|---|---|
| 13/716891 | 6/11/15 | DSB |
| EAST (attached) | 6/11/15 | DSB |
| Inventor nmae search | 6/11/15 | DSB |
| Company name search | 6/11/15 | DSB |

## INTERFERENCE SEARCH

| US Class/ CPC Symbol | US Subclass / CPC Group | Date | Examiner |
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| APPLICATION NUMBER | FILING OR 371(C) DATE | FIRST NAMED APPLICANT | ATTY. DOCKET NO./TITLE |
|---|---|---|---|
| 14/337,583 | 07/22/2014 | Shinya SASAGAWA | 0756-10540 |

**CONFIRMATION NO. 7546**

**PUBLICATION NOTICE**

*OC000000071832613*

31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

**Title:**SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

**Publication No.**US-2014-0332801-A1
**Publication Date:**11/13/2014

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The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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| Application Number | 14/337,583 |
| Filing Date | July 22, 2014 |
| First Named Inventor | Shinya SASAGAWA |
| Art Unit | 2813 |
| Examiner Name | |
| Attorney Docket Number | 0756-10540 |

Sheet 1 of 15

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Sheet 2 of 15

| Complete if Known | |
|---|---|
| Application Number | 14/337,583 |
| Filing Date | July 22, 2014 |
| First Named Inventor | Shinya SASAGAWA |
| Art Unit | 2813 |
| Examiner Name | |
| Attorney Docket Number | 0756-10540 |

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| | | | | Filing Date | July 22, 2014 |
| | | | | First Named Inventor | Shinya SASAGAWA |
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| Sheet | 3 | of | 15 | Attorney Docket Number | 0756-10540 |

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| Filing Date | July 22, 2014 |
| First Named Inventor | Shinya SASAGAWA |
| Art Unit | 2813 |
| Examiner Name | |
| Attorney Docket Number | 0756-10540 |

Sheet 5 of 15

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| | | | | Filing Date | July 22, 2014 |
| | | | | First Named Inventor | Shinya SASAGAWA |
| (Use as many sheets as necessary) | | | | Art Unit | 2813 |
| | | | | Examiner Name | |
| Sheet | 11 | of | 15 | Attorney Docket Number | 0756-10540 |

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| **First Named Inventor/Applicant Name:** | Shinya SASAGAWA |
| **Customer Number:** | 31780 |
| **Filer:** | Eric J. Robinson/Adele Stamper |
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**New Applications Under 35 U.S.C. 111**
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**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

Attorney Docket No. 0756-10540

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| In re Patent Application of: | ) | Confirmation No. 7546 |
| Shinya SASAGAWA et al. | ) | Group Art Unit: 2813 |
| Serial No. 14/337,583 | ) | Examiner: Unassigned |
| Filed: July 22, 2014 | ) | |
| For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME | ) | |

## INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application.

The references listed on the attached Form PTO-1449 were cited in parent Application Serial No. 13/716,891 and copies of the references can be found in this application (37 C.F.R. § 1.98(d)(1)-(2)).

U.S. Patent Nos. 5,648,662; 5,811,328; 6,124,155; 6,166,399; 6,335,213; 6,756,258; 6,797,548; 6,847,064; 7,507,991 and 7,923,311 and U.S. Publication No. 2011/0101362 are in the family of JP 06-045354.

U.S. Patent No. 8,183,099 and U.S. Publication Nos. 2012/0223307 and 2010/0159639 and WO2010/071034 and CN102257621 and KR2011-0104057 and TW201041049 are in the family of JP 2010-166030.

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U.S. Patent Nos. 6,727,522 and 7,064,346 are in the family of JP 2000-150900.

U.S. Patent No. 7,061,014 is in the family of JP 2004-103957.

U.S. Patent No. 5,744,864 is in the family of JP 11-505377.

U.S. Patent No. 6,563,174 is in the family of JP 2003-086808.

U.S. Publication No. 2006/0244107 is in the family of WO 2004/114391.

This Information Disclosure Statement is being submitted before the issuance of a first Office Action on the merits, therefore, no fee is required. However, the Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

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## JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

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特許庁長官
Commissioner,
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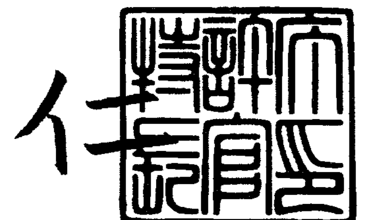

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【書類名】明細書
【発明の名称】半導体装置およびその作製方法
【技術分野】
【０００１】
本発明は、トランジスタに代表される半導体装置およびその作製方法に関する。
【背景技術】
【０００２】
絶縁表面を有する基板上に半導体材料を堆積して、その半導体材料を活性層として用いるトランジスタ（以下、堆積膜トランジスタと呼ぶ）が研究されてきた。従来は、活性層としてアモルファスシリコンなどのシリコン系半導体材料が用いられてきたが、近年、活性層に酸化物半導体材料を用いるトランジスタの研究が注目を集めている。というのは、酸化物半導体材料を活性層に用いたトランジスタ（以下、酸化物半導体トランジスタと呼ぶ）は、アモルファスシリコンを用いたトランジスタに比べ、オン電流が大きく、オフ電流が小さいという特徴を有するからである。
【０００３】
また、上記のような特徴を有する酸化物半導体トランジスタを、単結晶シリコンを用いたトランジスタ等が形成されている階層とは別の階層に形成して、メモリ機能等を有する半導体装置を開発する試みがなされている（特許文献１、非特許文献１）。このような半導体装置の構成では、上の階層に作製するトランジスタは、ボトムゲート型トランジスタが好ましい。というのは、下層に形成したトランジスタを電気的につなげている配線を、上層に形成するトランジスタのゲート電極に流用できるからである。
【先行技術文献】
【特許文献】
【０００４】
【特許文献１】特開２０１１－２３８３３３号公報
【非特許文献】
【０００５】
【非特許文献１】Ｋ．　Ｋａｎｅｋｏ　ｅｔ　ａｌ．，”Ｈｉｇｈｌｙ　Ｒｅｌｉａｂｌｅ　ＢＥＯＬ－Ｔｒａｎｓｉｓｔｏｒ　ｗｉｔｈ　Ｏｘｙｇｅｎ－ｃｏｎｔｒｏｌｌｅｄ　ＩｎＧａＺｎＯ　ａｎｄ　Ｇａｔｅ／Ｄｒａｉｎ　Ｏｆｆｓｅｔ　Ｄｅｓｉｇｎ　ｆｏｒ　Ｈｉｇｈ／Ｌｏｗ　Ｖｏｌｔａｇｅ　Ｂｒｉｄｇｉｎｇ　Ｉ／Ｏ　Ｏｐｅｒａｔｉｏｎｓ”　ＩＥＤＭ２０１１，　ｐｐ．１５５－１５８
【発明の概要】
【発明が解決しようとする課題】
【０００６】
上述した複数の階層に複数のトランジスタを有する半導体装置のうち、上層に形成されるボトムゲート型トランジスタは、堆積膜トランジスタが好ましい。堆積膜により容易に活性層を形成できるからであり、当該半導体装置の作製も容易になるからである。
【０００７】
ボトムゲート型トランジスタを上層に形成した、従来の複数の階層に複数のトランジスタを有する半導体装置は、作製が容易であるが、半導体装置の性能として十分ではない。上層に形成したボトムゲート型トランジスタの電気特性が十分でないからである。たとえば、複数の階層に複数のトランジスタを有する半導体装置を用いたメモリにおいて、メモリの書き込みを行うトランジスタを、堆積膜トランジスタで構成すると、メモリの書き込み能力等が十分ではない。というのは、上層に形成されるボトムゲート型トランジスタの電気特性が十分でなく、特にオン電流がバルクシリコンを活性層に用いたトランジスタに比べ小さいためである。そのため、堆積膜トランジスタのオン電流を大きくする必要がある。その方法のひとつとして、当該ボトムゲート型トランジスタのチャネル長を短くした（たとえば３０ｎｍ程度まで）トランジスタを用いる方法がある。なお、チャネル長を３０ｎｍ未満まで微細化するには電子線を用いたフォトリソグラフィ工程が必要である。

【０００８】
フォトリソグラフィ工程を用いて、一の導電層を分断してソース電極とドレイン電極を形成するボトムゲート型のトランジスタにおいて、そのチャネル長を短くするには、レジストの厚さをそのチャネル長以下とする必要がある。ところで、一の導電層のエッチング工程においてレジストの厚さは減少する。そのため、一の導電層の厚さを、当該エッチング工程でレジストが消失してしまわない程度の条件で分断できる厚さとしなければならない。
【０００９】
一方、トランジスタのソース電極とドレイン電極の電気抵抗は低い方が好ましく、その厚さはどこまでも薄くできるものではない。
【００１０】
以上のことから、ボトムゲート型のトランジスタのソース電極とドレイン電極の電気抵抗を抑制しつつ、そのチャネル長を短くすることは難しい。
【００１１】
本発明は、チャネル長の短いボトムゲート型のトランジスタを提供することを課題の一とする。または、チャネル長の短いボトムゲート型のトランジスタの作製方法を提供することを課題の一とする。
【課題を解決するための手段】
【００１２】
ボトムゲート型のトランジスタのソース電極およびドレイン電極の構成に着目した。そして、ソース電極およびドレイン電極のチャネル形成領域に近接する部分の厚さが、他の部分より薄い構成に想到した。
【００１３】
また、ソース電極およびドレイン電極のチャネル形成領域に近接する部分を、他の部分より後の工程で形成する方法に想到した。
【００１４】
また、ソース電極およびドレイン電極の上記他の部分（言い換えるとチャネル形成領域に近接する部分以外の部分）を形成した後に、チャネル形成領域に近接する部分と当該他の部分の間に生じる段差が、チャネル形成領域に近接するソース電極およびドレイン電極を形成する際に、レジストで被覆できない現象に着目した。そして、当該段差を絶縁膜層で覆い、当該絶縁層を平坦化し、当該平坦化された絶縁層上にハードマスク層を形成し、当該ハードマスク層を用いて、ソース電極およびドレイン電極のチャネル形成領域に近接する部分を分断して、チャネル長の短いボトムゲート型のトランジスタを作製する方法に想到した。
【００１５】
すなわち、本発明に係る半導体装置の作製方法の一態様は、絶縁表面上にゲート電極層を形成する工程と、ゲート電極層の上に接するようにゲート絶縁層を形成する工程と、ゲート絶縁層の上に接して、かつゲート電極層と重なるように、酸化物半導体層を形成する工程と、酸化物半導体層の上に接して、かつ酸化物半導体層を覆うように、導電膜を形成する工程と、導電膜の上に接しゲート電極層を挟んで離間する、第１低抵抗材料層と第２低抵抗材料層を形成する工程と、第１低抵抗材料層および第２低抵抗材料層ならびに導電膜の上に接するように、第１保護層を形成する工程と、第１保護層を平坦化する工程と、平坦化した第１保護層の上に接するように、ハードマスク層を形成する工程と、ハードマスク層の表面において、第１低抵抗材料層と第２低抵抗材料層の間で、かつ酸化物半導体層と重なる領域に、開口パターン部を有するレジストパターンを形成する工程と、レジストパターンを用いて、ハードマスク層をエッチングして開口パターンを形成する工程と、開口パターンを有するハードマスク層をマスクとして用いて、第１保護層を導電層が露出するまでエッチングする工程と、開口パターンを有するハードマスク層と第１保護層をマスクとして用いて、導電膜をエッチングして、第１導電層と第２導電層に分離して形成する工程と、第１保護層の開口部を第２絶縁層で充填する工程と、を有する半導体装置の作製

方法である。
【００１６】
ソース電極およびドレイン電極の、チャネル形成領域に近接する部分と他の部分の間に生じる段差を絶縁層で平坦化した後に、ハードマスク層を形成し、当該ハードマスク層に開口部を形成するレジストを塗布する。当該レジストを塗布する面が平坦であるため、レジストを均一に形成できるので、被覆されない領域が生じにくい。また、薄いレジストを均一に形成できる。よって、ハードマスク層の上に線幅が微細なレジストの開口パターンを形成することができる。
【００１７】
上記のように、ハードマスク層を用いて導電膜を加工して、微細なチャネル長のトランジスタを形成することができる。ハードマスク層があるので、加工中にレジストが消失しても、その後の工程で加工ができないという問題は生じない。というのは、ハードマスク層は、第１保護層および導電膜の加工の際のマスクとなるからである。なお、ハードマスク層は、第１保護層および導電膜をエッチングする条件でエッチングされにくい膜で構成することができる。
【００１８】
以上の工程により、ソース電極層、ドレイン電極層となる導電膜を、微細なパターンに開口することができる。よって、ボトムゲート型のトランジスタにおいて、チャネル長が微細なトランジスタを作製することができる。
【００１９】
また、本発明の一態様は、ゲート電極層と、ゲート電極層の上に接するゲート絶縁層と、ゲート絶縁層の上に接し、かつゲート電極層と重なるように設けられた酸化物半導体層と、酸化物半導体層の上に接しゲート電極層を挟んで離間する、第１導電層と第２導電層と、第１導電層の上に接する第１低抵抗材料層と、第２導電層の上に接する第２低抵抗材料層と、第１保護層は、第１導電層および第１低抵抗材料層ならびに第２導電層および第２低抵抗材料層の上に接するように設けられ、第２絶縁層は、酸化物半導体層と一部に接するように設けられ、第１導電層と第２導電層の間隔は、第１低抵抗材料層と第２低抵抗材料層の間隔よりも狭く、第１導電層および第１低抵抗材料層はソース電極であり、第２導電層および第２低抵抗材料層はドレイン電極であることを特徴とする半導体装置である。
【００２０】
酸化物半導体層を用いたボトムゲート型トランジスタに上記構造を採用すると、チャネル長を微細にすることができるので、オン電流の大きいトランジスタを得ることが出来る。また、酸化物半導体はアモルファスシリコンより電子移動度が高いため、オン電流の大きい半導体装置を得ることができる。
【００２１】
また、ゲート絶縁層が、平坦である半導体装置が好ましい。
【００２２】
下地絶縁層およびゲート電極層を平坦にすると、酸化物半導体層がゲート電極層により生じる段差により、被覆されないことを防止することができる。とくに、酸化物半導体の膜厚が５ｎｍ以上３０ｎｍ以下であるときに、平坦化するメリットがある。
【００２３】
また、酸化物半導体層のチャネル長方向の幅は、ゲート電極層のチャネル長方向の幅よりも広いことを特徴とする半導体装置であることが好ましい。
【００２４】
酸化物半導体層とゲート電極層の接する面積が大きくなるので、酸化物半導体層よりも下方に設けられている絶縁層からの酸素を酸化物半導体層に供給しやすくできる。その結果、トランジスタの初期の電気特性（閾値など）および電気特性（閾値など）の信頼性を向上させることができる。
【００２５】
また、島状の酸化物半導体層の端は酸素欠陥を生じやすく、キャリアをその他の領域より

発生しやすい。活性層である酸化物半導体層において、局所的にキャリアが発生するとトランジスタの電気特性（閾値など）を劣化させる。

【００２６】

仮に、酸化物半導体層のチャネル長方向の幅が、ゲート電極層のチャネル長方向の幅よりも狭い場合、すなわち、島状の酸化物半導体層の端がゲート電極層の端の内側にある場合、ゲート電極層とソース電極間に電圧を印加したとき、島状の酸化物半導体層の端に電界が集中する。キャリアを発生しやすい島状の酸化物半導体層の端に電界が集中すると、トランジスタの電気特性（閾値など）を劣化させる。一方、本発明のように、酸化物半導体層のチャネル長方向の幅を、ゲート電極層のチャネル長方向の幅よりも広くすると、島状の酸化物半導体層の端がゲート電極層の端の外側に位置するので、ゲート電極層とソース電極間に電圧を印加したとき、酸化物半導体層の端に電界は集中しない。そのため、トランジスタの電気特性（閾値等）を劣化させにくくできる。

【発明の効果】

【００２７】

本発明により、チャネル長が微細な（たとえば３０ｎｍ）、酸化物半導体層を活性層に用いたボトムゲート型トランジスタを作製することができる。また、当該トランジスタを構成要素の一つとした半導体装置を実現できる。

【図面の簡単な説明】

【００２８】

【図１】本発明の一態様を示す断面図および平面図である。
【図２】本発明の一態様の作製方法を説明するための断面模式図である。
【図３】本発明の一態様の作製方法を説明するための断面模式図である。
【図４】本発明の一態様の作製方法を説明するための断面模式図である。
【図５】本発明の一態様の作製方法を説明するための断面模式図である。
【図６】本発明の一態様の作製方法を説明するための断面模式図である。
【図７】本発明の一態様を示す断面図および平面図である。
【図８】本発明の一態様を示す回路図である。
【図９】記憶装置の例を説明するための図である。
【図１０】記憶装置の例を説明するための図である。
【図１１】記憶装置の例を説明するための図である。
【図１２】電子機器の例を説明するための図である。

【発明を実施するための形態】

【００２９】

以下では、本発明の実施の形態について図面を用いて詳細に説明する。ただし、本発明は以下の説明に限定されず、その形態および詳細を様々に変更し得ることは、当業者であれば容易に理解される。また、本発明は以下に示す実施の形態の記載内容に限定して解釈されるものではない。

【００３０】

（実施の形態１）

本実施の形態では、本発明で作製することのできる半導体装置の一態様を図１（Ａ）から（Ｃ）を用いて説明する。図１（Ａ）は、トランジスタ４２０の平面図であり、図１（Ｂ）は、図１（Ａ）のＡ－Ａ’における断面図、図１（Ｃ）は、図１（Ａ）のＢ－Ｂ’における断面図である。

【００３１】

図１に示すトランジスタ４４０は、ボトムゲート型のトランジスタである。図１に示すトランジスタ４４０は、基板４００表面に形成された下地絶縁層４３６上に、絶縁層４３２に埋め込まれるようにして設けられたゲート電極層４０１と、ゲート電極層４０１上にゲート絶縁層４０２と、ゲート絶縁層４０２の上に酸化物半導体層４０３と、酸化物半導体層４０３の上に第１導電層４５４ａおよび第２導電層４５４ｂと、第１導電層４５４ａの上に接する第１低抵抗材料層４０５ａと、第２導電層４５４ｂの上に接する第２低抵抗材

料層４０５ｂと、第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂならびに第１導電層４５４ａおよび第２導電層４５４ｂと接するように第１保護層４０６と、第１保護層４０６に接するハードマスク層４９５と、ハードマスク層４９５の上に第２保護層４０７、を有する。

【００３２】

まず、各構成要素について説明する。

【００３３】

＜当該半導体装置の構成要素＞

（基板と下地絶縁層）

基板４００としては、絶縁表面を有する基板を用いることができ、少なくとも、後の熱処理に耐えうる程度の耐熱性を有する基板を用いることが好ましい。基板４００としては、例えばガラス基板、セラミック基板、石英基板、サファイア基板などを用いることができる。また、シリコンや炭化シリコンなどの単結晶半導体基板、多結晶半導体基板、シリコンゲルマニウムなどの化合物半導体基板、ＳＯＩ基板などを適用することもでき、これらの基板上に半導体素子が設けられたものを、基板４００として用いてもよい。なお、基板４００中の水素または水などの不純物濃度は、低いことが好ましい。酸化物半導体層４０３に水素または水が拡散し、当該半導体装置の電気特性を劣化させないようにするためである。

【００３４】

下地絶縁層４３６としては、例えば酸化シリコン、酸化窒化シリコン、酸化アルミニウム、酸化窒化アルミニウムなどの酸化物絶縁層、窒化シリコン、窒化酸化シリコン、窒化アルミニウム、窒化酸化アルミニウムなどの窒化物絶縁層を用いることができる。

【００３５】

（ゲート電極層）

ゲート電極層４０１としては、例えばモリブデン、チタン、タングステン、アルミニウム、銅等の金属材料を用いることができる。また、ゲート電極層４０１としてリン等の不純物元素をドーピングした多結晶シリコン層に代表される半導体層、ニッケルシリサイドなどのシリサイド層を用いてもよい。また、ゲート電極層４０１を単層構造としてもよいし、積層構造としてもよい。

【００３６】

（ゲート絶縁層）

ゲート絶縁層４０２は、酸化シリコン、酸窒化シリコン、窒化シリコン等を用いることができる。ゲート絶縁層４０２は、化学量論比を満たす酸素よりも多くの酸素を含む酸化シリコン層が好ましい。ゲート絶縁層４０２は、上記に示した膜を単層で形成しても良いし、２層で構成しても良い。たとえば、窒化シリコンと酸窒化シリコン、窒化シリコンと酸化シリコンを用いることができる。

【００３７】

（ソース電極層およびドレイン電極層）

ソース電極層およびドレイン電極層は、第１導電層４５４ａと第１低抵抗材料層４０５ａで構成されている。第１導電層４５４ａは、タングステン、モリブデン等の金属を用いることができる。特にタングステンが好ましい。第１保護層４０６とエッチングレートの比を高くすることができるからである。第１低抵抗材料層４０５ａは、アルミニウムとチタンの積層構造、または銅などを用いることができる。アルミニウムとチタンの積層構造は、チタン／アルミニウム／チタンを用いてもよい。第１低抵抗材料層４０５ａに銅を用いる場合、銅が隣接する層に拡散しないように窒化チタン等を設けることが好ましい。

【００３８】

（酸化物半導体層）

次に、本実施の形態に用いることができる酸化物半導体層４０３について説明する。酸化物半導体層４０３は、少なくとも禁制帯幅がシリコンの１．１ｅＶよりも大きい半導体を用いることが出来る。たとえば、酸化物半導体を用いることができる。

【００３９】
酸化物半導体層４０３の膜厚は、５ｎｍ以上１００ｎｍ以下とし、好ましくは５ｎｍ以上３０ｎｍ以下とする。というのは、ショートチャネル効果を抑えながら、トランジスタのチャネル長を微細化するためである。
【００４０】
酸化物半導体層４０３には酸化物半導体が好ましい。酸化物半導体として用いることのできる材料は、少なくともインジウム（Ｉｎ）を含む。特にＩｎと亜鉛（Ｚｎ）を含むことが好ましい。また、当該酸化物半導体を用いたトランジスタの電気特性のばらつきを減らすためのスタビライザーとして、それらに加えてガリウム（Ｇａ）を有することが好ましい。また、スタビライザーとしてスズ（Ｓｎ）を有することが好ましい。また、スタビライザーとしてハフニウム（Ｈｆ）を有することが好ましい。また、スタビライザーとしてアルミニウム（Ａｌ）を有することが好ましい。また、スタビライザーとしてジルコニウム（Ｚｒ）を有することが好ましい。
【００４１】
また、他のスタビライザーとして、ランタノイドである、ランタン（Ｌａ）、セリウム（Ｃｅ）、プラセオジム（Ｐｒ）、ネオジム（Ｎｄ）、サマリウム（Ｓｍ）、ユウロピウム（Ｅｕ）、ガドリニウム（Ｇｄ）、テルビウム（Ｔｂ）、ジスプロシウム（Ｄｙ）、ホルミウム（Ｈｏ）、エルビウム（Ｅｒ）、ツリウム（Ｔｍ）、イッテルビウム（Ｙｂ）、ルテチウム（Ｌｕ）のいずれか一種あるいは複数種を有してもよい。
【００４２】
また、酸化物半導体として、酸化インジウム、酸化スズ、酸化亜鉛、２元系金属の酸化物であるＩｎ－Ｚｎ系酸化物、Ｉｎ－Ｍｇ系酸化物、Ｉｎ－Ｇａ系酸化物、３元系金属の酸化物であるＩｎ－Ｇａ－Ｚｎ系酸化物（ＩＧＺＯとも表記する）、Ｉｎ－Ａｌ－Ｚｎ系酸化物、Ｉｎ－Ｓｎ－Ｚｎ系酸化物、Ｉｎ－Ｈｆ－Ｚｎ系酸化物、Ｉｎ－Ｌａ－Ｚｎ系酸化物、Ｉｎ－Ｃｅ－Ｚｎ系酸化物、Ｉｎ－Ｐｒ－Ｚｎ系酸化物、Ｉｎ－Ｎｄ－Ｚｎ系酸化物、Ｉｎ－Ｓｍ－Ｚｎ系酸化物、Ｉｎ－Ｅｕ－Ｚｎ系酸化物、Ｉｎ－Ｇｄ－Ｚｎ系酸化物、Ｉｎ－Ｔｂ－Ｚｎ系酸化物、Ｉｎ－Ｄｙ－Ｚｎ系酸化物、Ｉｎ－Ｈｏ－Ｚｎ系酸化物、Ｉｎ－Ｅｒ－Ｚｎ系酸化物、Ｉｎ－Ｔｍ－Ｚｎ系酸化物、Ｉｎ－Ｙｂ－Ｚｎ系酸化物、Ｉｎ－Ｌｕ－Ｚｎ系酸化物、４元系金属の酸化物であるＩｎ－Ｓｎ－Ｇａ－Ｚｎ系酸化物、Ｉｎ－Ｈｆ－Ｇａ－Ｚｎ系酸化物、Ｉｎ－Ａｌ－Ｇａ－Ｚｎ系酸化物、Ｉｎ－Ｓｎ－Ａｌ－Ｚｎ系酸化物、Ｉｎ－Ｓｎ－Ｈｆ－Ｚｎ系酸化物、Ｉｎ－Ｈｆ－Ａｌ－Ｚｎ系酸化物を用いることができる。
【００４３】
なお、ここで、例えば、Ｉｎ－Ｇａ－Ｚｎ系酸化物とは、ＩｎとＧａとＺｎを主成分として有する酸化物という意味であり、ＩｎとＧａとＺｎの比率は問わない。また、ＩｎとＧａとＺｎ以外の金属元素が入っていてもよい。
【００４４】
また、酸化物半導体として、$InMO_3$（ＺｎＯ）ｍ（ｍ＞０、且つ、ｍは整数でない）で表記される材料を用いてもよい。なお、Ｍは、Ｇａ、Ｆｅ、ＭｎおよびＣｏから選ばれた一の金属元素または複数の金属元素を示す。また、酸化物半導体として、$In_2SnO_5$（ＺｎＯ）ｎ（ｎ＞０、且つ、ｎは整数）で表記される材料を用いてもよい。
【００４５】
また、酸化物半導体として、Ｉｎ：Ｇａ：Ｚｎ＝１：１：１（＝１／３：１／３：１／３）、Ｉｎ：Ｇａ：Ｚｎ＝２：２：１（＝２／５：２／５：１／５）、あるいはＩｎ：Ｇａ：Ｚｎ＝３：１：２（＝１／２：１／６：１／３）の原子数比のＩｎ－Ｇａ－Ｚｎ系酸化物やその組成の近傍の酸化物を用いることができる。あるいは、Ｉｎ：Ｓｎ：Ｚｎ＝１：１：１（＝１／３：１／３：１／３）、Ｉｎ：Ｓｎ：Ｚｎ＝２：１：３（＝１／３：１／６：１／２）あるいはＩｎ：Ｓｎ：Ｚｎ＝２：１：５（＝１／４：１／８：５／８）の原子数比のＩｎ－Ｓｎ－Ｚｎ系酸化物やその組成の近傍の酸化物を用いるとよい。
【００４６】

しかし、インジウムを含む酸化物半導体は、これらに限られず、必要とする半導体特性（移動度、閾値等の電気特性とそれらのばらつき）に応じて適切な組成のものを用いればよい。また、必要とする半導体特性を得るために、キャリア濃度や不純物濃度、欠陥密度、金属元素と酸素の原子数比、原子間結合距離、密度等を適切なものとすることが好ましい。

【００４７】
例えば、Ｉｎ－Ｓｎ－Ｚｎ系酸化物では比較的容易に高い移動度が得られる。しかしながら、Ｉｎ－Ｇａ－Ｚｎ系酸化物でも、バルク内欠陥密度を低くすることにより移動度を上げることができる。

【００４８】
また、酸化物半導体層４０３は、単結晶、多結晶（ポリクリスタルともいう。）または非晶質などの状態をとる。

【００４９】
また、酸化物半導体層４０３に、銅、アルミニウム、塩素などの不純物がほとんど含まれない高純度化されたものであることが望ましい。トランジスタの製造工程において、これらの不純物が混入または酸化物半導体層４０３の表面に付着する恐れのない工程を適宜選択することが好ましく、酸化物半導体層４０３に付着した場合には、シュウ酸や希フッ酸などに曝す、またはプラズマ処理（$Ｎ_2Ｏ$プラズマ処理など）を行うことにより、酸化物半導体層４０３の不純物を除去することが好ましい。具体的には、酸化物半導体中の銅濃度は$１×１０^{18}$ａｔｏｍｓ／$ｃｍ^3$以下、好ましくは$１×１０^{17}$ａｔｏｍｓ／$ｃｍ^3$以下とする。また、酸化物半導体中のアルミニウム濃度は$１×１０^{18}$ａｔｏｍｓ／$ｃｍ^3$以下とする。また、酸化物半導体中の塩素濃度は$２×１０^{18}$ａｔｏｍｓ／$ｃｍ^3$以下とする。

【００５０】
また、酸化物半導体は成膜直後において、化学量論的組成より酸素が多い過飽和の状態とすることが好ましい。例えば、スパッタリング法を用いて酸化物半導体を成膜する場合、成膜ガスの酸素の占める割合が多い条件で成膜することが好ましく、特に酸素雰囲気（酸素ガス１００％）で成膜を行うことが好ましい。成膜ガスの酸素の占める割合が多い条件、特に酸素ガス１００％の雰囲気で成膜すると、例えば成膜温度を３００℃以上としても、膜中からのＺｎの放出が抑えられる。

【００５１】
酸化物半導体は、水素などの不純物が十分に除去され、その酸化物半導体に十分な酸素が供給されて酸素が過飽和の状態となっていることが望ましい。具体的には、酸化物半導体の水素濃度は$５×１０^{19}$ａｔｏｍｓ／$ｃｍ^3$以下、望ましくは$５×１０^{18}$ａｔｏｍｓ／$ｃｍ^3$以下、より望ましくは$５×１０^{17}$ａｔｏｍｓ／$ｃｍ^3$以下とする。なお、上述の酸化物半導体の水素濃度は、二次イオン質量分析法（ＳＩＭＳ：Ｓｅｃｏｎｄａｒｙ　Ｉｏｎ　Ｍａｓｓ　Ｓｐｅｃｔｒｏｓｃｏｐｙ）で測定されるものである。

【００５２】
（保護層）
第１保護層４０６は、酸化物半導体層４０３を、外部から浸入する水分等から守る役割を有する。第１保護層４０６は、酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウムを用いることできる。第１保護層４０６は、膜中に酸素を多く含ませた酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウムを用いることが好ましい。また、多くの過剰酸素を上記保護層に含ませたい場合には、イオン注入法やイオンドーピング法やプラズマ処理によって、上記保護層に酸素を適宜添加すればよい。

【００５３】
第２保護層４０７は、酸化物半導体層４０３を、外部から浸入する水分等から守る役割を有する。第２保護層４０７は、酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウムを用いることできる。第２保護層４０７は、膜中に酸素を多く含ませた酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウムを用いることが好ましい。また、第２保護層４０

７は、第３保護層４０７ａと第４保護層４０７ｂの２層で構成しても良い。第３保護層４０７ａは、酸化物半導体に接して形成すればよい。第３保護層４０７ａは、成膜条件を適宜設定して膜中に酸素を多く含ませたガリウム（Ｇａ）を有する酸化物半導体、酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウムを用いることできる。第４保護層４０７ｂは、第３保護層４０７ａに接して形成すればよい。第４保護層４０７ｂは、膜中に酸素を多く含ませた酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウムを用いることできる。また、多くの過剰酸素を上記保護層に含ませたい場合には、イオン注入法やイオンドーピング法やプラズマ処理によって、上記保護層に酸素を適宜添加すればよい。

【００５４】

（ハードマスク層）

ハードマスク層４９５は、第１保護層４０６をエッチングする条件でエッチングされにくい膜であることが好ましい。というのは、第１保護層４０６をエッチングするときに、ハードマスク層４９５をマスクとして利用するためである。ハードマスク層４９５には、アモルファスシリコンを用いることが好ましく、アモルファスシリコンは、ＰＣＶＤ法または、スパッタリング法で成膜することができる。

【００５５】

＜半導体装置の作製方法＞

本発明の一態様である半導体装置の作製方法について、図２から図６を用いて説明する。

【００５６】

図２にゲート電極層４０１の形成工程から、酸化物半導体層４０３への酸素ドーピング工程までを示す。

【００５７】

まず、基板４００を準備し、基板４００の上に下地絶縁層４３６を形成し、下地絶縁層４３６の上にゲート電極層４０１を形成する（図２（Ａ－１）から（Ａ－３））。

【００５８】

ゲート電極層４０１は、ゲート電極として使用できる材料をたとえばスパッタリング成膜し、一部を選択的にエッチングして形成する。なお、エッチングは、ドライエッチングでもウェットエッチングでもよく、両方を用いてもよい。また、ゲート電極層４０１形成後に、基板４００、およびゲート電極層４０１に熱処理を行ってもよい。

【００５９】

次に、下地絶縁層４３６およびゲート電極層４０１の上に絶縁層４３２を形成する。絶縁層４３２を平坦化して、ゲート電極層４０１を露出させ、絶縁層４３２およびゲート電極層４０１を平坦にすることが好ましい。（図２（Ｂ－１）から（Ｂ－３）参照）。平坦化処理としては、化学的機械研磨（Ｃｈｅｍｉｃａｌ　Ｍｅｃｈａｎｉｃａｌ　Ｐｏｌｉｓｈｉｎｇ：ＣＭＰ）処理などを行えばよい。

【００６０】

後述する酸化物半導体層４０３が、ゲート電極層４０１により生じる段差により、被覆されないことを防止することができるため、絶縁層４３２およびゲート電極層４０１を平坦化することが好ましい。

【００６１】

次に、ゲート電極層４０１上にゲート絶縁層４０２を形成し、ゲート絶縁層４０２上に酸化物半導体層４０３を形成する（図２（Ｃ－１）から（Ｃ－３）参照）。

【００６２】

例えば、ＰＣＶＤ法を用いてゲート絶縁層４０２に適用可能な材料の膜を成膜してゲート絶縁層４０２を形成できる。

【００６３】

なお、酸化物半導体層４０３を形成する前に熱処理を行い、ゲート絶縁層４０２の脱水化または脱水素化を行ってもよい。例えば３５０℃以上４５０℃以下の熱処理を行ってもよい。

【００６４】

また、脱水化または脱水素化されたゲート絶縁層４０２に酸素ドープ処理を行い、酸素をゲート絶縁層４０２に供給して、ゲート絶縁層４０２中、またはゲート絶縁層４０２中および該界面近傍に酸素を過剰に含有させてもよい。脱水化または脱水素化した後にゲート絶縁層４０２に酸素を供給することにより、酸素の放出を抑制でき、ゲート絶縁層４０２の酸素濃度を高くできる。

【００６５】

なお、ゲート絶縁層４０２から酸化物半導体への酸素の供給のための熱処理を、酸化物半導体が島状に加工される前に行うと、ゲート絶縁層４０２に含まれる酸素が熱処理によって放出されるのを防止することができるため好ましい。

【００６６】

例えば、３５０℃以上基板の歪み点未満の温度、好ましくは、３５０℃以上４５０℃以下で熱処理を行う。さらに、その後の工程において熱処理を行ってもよい。このとき、上記熱処理を行う熱処理装置としては、例えば電気炉、または抵抗発熱体などの発熱体からの熱伝導または熱輻射により被処理物を加熱する装置を用いることができ、例えばＧＲＴＡ（Ｇａｓ　Ｒａｐｉｄ　Ｔｈｅｒｍａｌ　Ａｎｎｅａｌｉｎｇ）装置またはＬＲＴＡ（Ｌａｍｐ　Ｒａｐｉｄ　Ｔｈｅｒｍａｌ　Ａｎｎｅａｌｉｎｇ）装置などのＲＴＡ（Ｒａｐｉｄ　Ｔｈｅｒｍａｌ　Ａｎｎｅａｌｉｎｇ）装置を用いることができる。

【００６７】

また、上記熱処理を行った後、その加熱温度を維持しながらまたはその加熱温度から降温する過程で該熱処理を行った炉と同じ炉に高純度の酸素ガス、高純度の$N_2O$ガス、または超乾燥エア（露点が－４０℃以下、好ましくは－４０℃以下の雰囲気）を導入してもよい。このとき、酸素ガスまたは$N_2O$ガスは、水、水素などを含まないことが好ましい。また、熱処理装置に導入する酸素ガスまたは$N_2O$ガスの純度を、６Ｎ以上、好ましくは７Ｎ以上、すなわち、酸素ガスまたは$N_2O$ガス中の不純物濃度を１ｐｐｍ以下、好ましくは０．１ｐｐｍ以下とすることが好ましい。酸素ガスまたは$N_2O$ガスの作用により、酸化物半導体に酸素が供給され、酸化物半導体中の酸素欠乏に起因する欠陥を低減できる。なお、上記高純度の酸素ガス、高純度の$N_2O$ガス、または超乾燥エアの導入は、上記熱処理時に行ってもよい。

【００６８】

さらに、酸化物半導体に酸素ドーピング４５１を行う（図２（Ｃ－１）から（Ｃ－３）参照）。酸化物半導体へ酸素を供給することにより、酸化物半導体中の酸素欠損を補填するためである。酸素欠損を補填することにより、当該半導体装置は、初期の電気特性（閾値など）に異常値が生じにくくなり、電気特性（閾値など）の信頼性も向上する。

【００６９】

酸素ドーピング４５１は、イオン注入法、イオンドーピング法、プラズマイマージョンイオンインプランテーション法、プラズマ処理などを用いることができる。これら方法により、酸素（酸素ラジカル、酸素原子、酸素分子、オゾン、酸素イオン（酸素分子イオン）および／または酸素クラスタイオン）を酸化物半導体にドープすることができる。

【００７０】

図３に酸化物半導体層４０３を島状に形成する工程から、第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂの形成するための、レジスト４５３の形成工程までを示す。

【００７１】

酸化物半導体層４０３をフォトリソグラフィ工程により加工して、島状の酸化物半導体層４０３を形成する（図３（Ａ－１）から（Ａ－３）参照）。

【００７２】

酸化物半導体層４０３のエッチングは、ドライエッチングでもウェットエッチングでもよく、両方を用いてもよい。

【００７３】

なお、酸化物半導体層のチャネル長方向の幅は、ゲート電極層のチャネル長方向の幅よりも広いことが好ましい。酸化物半導体層とゲート電極層の接する面積が大きくなるので、

酸化物半導体層よりも下方に設けられている絶縁層からの酸素を酸化物半導体層に供給しやすくできる。その結果、トランジスタの初期の電気特性（閾値など）および電気特性（閾値など）の信頼性を向上させることができるからである。

【００７４】

次に、導電膜４５４を、酸化物半導体層４０３に接するように形成する。導電膜４５４は、スパッタリング法などを用いて形成すればよい。（図３（Ｂ－１）から（Ｂ－３）参照）。

【００７５】

次に、導電膜４５４に接するように、低抵抗材料層４０５を、形成する。低抵抗材料層４０５は、スパッタリング法などを用いて形成すればよい。

【００７６】

次に、フォトリソグラフィ工程によりレジスト４５３を形成する（図３（Ｃ－１）から（Ｃ－３）参照）。

【００７７】

図４に低抵抗材料層４０５の形成工程から、第１保護層４０６の平坦化工程までを示す。

【００７８】

レジスト４５３をマスクとして低抵抗材料層４０５を選択的にエッチングし、第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂを形成する（図４（Ａ－１）から（Ａ－３）参照）。低抵抗材料層４０５をエッチングする条件は、導電膜４５４がエッチングされにくい条件で行う。後に行うハードマスク層４９５をマスクとして用いて、導電膜４５４を開口するためである。

【００７９】

次に、酸化物半導体層４０３と接していない領域の導電膜４５４をエッチングする（図４（Ｂ－１）から（Ｂ－３）参照）。

【００８０】

次に、第１保護層４０６を形成した後、ＣＭＰで平坦化を行う。（図４（Ｃ－１）から（Ｃ－３）参照）。第１保護層４０６の表面を平坦して、３０ｎｍ前後の薄膜レジストを塗布しても、レジストを塗布する面にある段差により、レジストが被覆されない領域を生じさせないためである。

【００８１】

図５にハードマスク層４９５の形成工程を示す。

【００８２】

平坦化した第１保護層４０６の上に、ハードマスク層４９５を形成する（図５（Ａ－１）から（Ａ－３）参照）。ハードマスク層４９５は、第１保護層４０６をエッチングする条件でエッチングされにくい膜であることが好ましい。ハードマスク層４９５を、第１保護層４０６をエッチングするときにマスクとして使用するためである。

【００８３】

次に、ハードマスク層４９５上にレジストを形成し、該レジストに対して電子ビームを用いた露光を行い、レジスト４５５を形成する（図５（Ｂ－１）から（Ｂ－３）参照）。

【００８４】

このときのレジストの膜厚は、作製するパターンの幅と１：１～１：２の関係になることが好ましい。例えば、パターンの幅が３０ｎｍの場合には、レジストの厚さを３０ｎｍから６０ｎｍとする。

【００８５】

また、トランジスタが形成されるハードマスク層４９５の表面は、平坦である。そのため、レジストの厚さが３０ｎｍ前後であっても、レジストを塗布する面にレジストを均一に塗布することができる。

【００８６】

次に、ハードマスク層４９５のエッチングを行う（図５（Ｃ－１）から（Ｃ－３）参照）。エッチング方法はドライエッチングが好ましい。ハードマスク層４９５をエッチングし

たのち、レジスト剥離を行ってもよい。
【００８７】
図６に第１保護層４０６の開口工程から、導電膜４５４の開口工程までを示す。
【００８８】
第１保護層４０６のエッチングを行う（図６（Ａ－１）から（Ａ－３）参照）。第１保護層４０６のエッチングの条件は、第１保護層４０６のエッチングレートとハードマスク層４９５のエッチングレートの比が大きいエッチング条件であることが好ましい。ハードマスク層４９５をマスクとして、第１保護層４０６を３０ｎｍ前後に開口するためである。
【００８９】
次に、導電膜４５４のエッチングを行い、第１導電層４５４ａと第２導電層を形成する。第１導電層４５４ａと第２導電層の間はチャネルが形成される領域になる（図６（Ｂ－１）から（Ｂ－３）参照）。導電膜４５４をエッチングする条件は、導電膜４５４のエッチングレートと酸化物半導体層４０３のエッチングレートの比が大きい条件であることが好ましい。酸化物半導体層４０３の表面にエッチングダメージを与えないためである。
【００９０】
３０ｎｍ前後の幅の開口を行う場合、レジスト４５５の膜厚は３０ｎｍから６０ｎｍと薄い。そのため、第１保護層４０６と、導電膜４５４とのエッチングを行っている途中にレジスト４５５が消失する。しかし、ハードマスク層４９５がマスクとして機能するため、レジスト４５５が消失しても、導電膜４５４に３０ｎｍ前後の幅の開口部を設けることができる。
【００９１】
次に、上記の工程で開口した導電膜４５４の開口部を、第２保護層４０７で覆う（図６（Ｃ－１）から（Ｃ－３）参照）。第２保護層４０７は、酸化物半導体層４０３に、水分、水素等の浸入を防止する膜が好ましい。たとえば、酸化シリコン膜、酸窒化シリコン膜、窒化シリコン膜、酸化アルミニウム等を用いることができる。
【００９２】
また、第２保護層４０７は、酸素を過剰に含む膜であることが好ましい。そのため、成膜段階で酸素を過剰に含む膜でもよい、また、第２保護層４０７に酸素ドーピングを行ってもよい。例えば、イオン注入法、イオンドーピング法、プラズマイマージョンイオンインプランテーション法、プラズマ処理などを用いて酸素（酸素ラジカル、酸素原子、酸素分子、オゾン、酸素イオン（酸素分子イオン）および／または酸素クラスタイオン）をドープできる。また、イオン注入法としてガスクラスタイオンビームを用いてもよい。
【００９３】
さらに、第２保護層４０７を成膜した後に熱処理を行ってもよい。例えば、窒素雰囲気下２５０℃で１時間熱処理を行う。
【００９４】
以上により、トランジスタ４４０が作製できる。このとき、作製されるトランジスタ４４０のチャネル長Ｌは、３０ｎｍ未満と短い。そのため、トランジスタ４４０はオン電流の大きいトランジスタとすることができる。
【００９５】
以上が本実施の一態様である半導体装置の作製方法である。
【００９６】
本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。
【００９７】
酸化物半導体層４０３を活性層に用いたボトムゲート型トランジスタにおいて、チャネル長が３０ｎｍ未満であるトランジスタを作製することができる。チャネル長を３０ｎｍ未満にすると、当該トランジスタのオン電流を大きくすることができる。
【００９８】
（実施の形態２）

本実施の形態では、半導体装置の一態様を図７（Ａ）および図７（Ｂ）を用いて説明する。図７（Ｂ）は、トランジスタ４２０の平面図であり、図７（Ａ）は、図７（Ｂ）のＸ－Ｙにおける断面図である。

【００９９】

図７（Ａ）および図７（Ｂ）に示すトランジスタ４２０は、基板４００表面に形成された下地絶縁層４３６上に、絶縁層４３２に埋め込まれるようにして設けられたゲート電極層４０１と、ゲート電極層４０１上にゲート絶縁層４０２と、ゲート絶縁層４０２の上に酸化物半導体層４０３と、酸化物半導体層４０３の上に第１導電層４５４ａおよび第２導電層４５４ｂと、第１導電層４５４ａの上に接する第１低抵抗材料層４０５ａと、第２導電層４５４ｂの上に接する第２低抵抗材料層４０５ｂと、第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂならびに第１導電層４５４ａおよび第２導電層４５４ｂと接するように第１保護層４０６と、第１保護層４０６に接するハードマスク層４９５と、ハードマスク層４９５の上に第２保護層４０７、を有する。

【０１００】

本実施例で示す半導体装置の構成、作製方法は、実施の形態１を参酌することができる。

【０１０１】

（基板４００に設けることができる回路について）

基板４００には半導体素子が設けられているが、ここでは簡略化のため省略している。また、基板４００上には、配線層４７４ａ、４７４ｂと、配線層４７４ａ、４７４ｂを覆う下地絶縁層４３６が設けられており、その一部が図８に示すメモリ構成の一つとなっている。図８にトランジスタ４２０と基板４００に設けられているトランジスタ４３１との接続を示す等価回路の一例を示す。

【０１０２】

また、容量４３０は、積層からなるドレイン電極層と、配線層４７４ａとを一対の電極とし、下地絶縁層４３６および積層からなるゲート絶縁層４０２を誘電体とする容量である。

【０１０３】

図８に示すメモリ構成において、メモリの書き込みは容量４３０に電荷を注入することにより行われる。本実施の形態で示すトランジスタは、チャネル長が３０ｎｍ未満と短いので、オン電流が大きい。そのためメモリの書き込みを早くすることができる。

【０１０４】

図８に示すメモリ構成は、電力が供給されない状況でも記憶内容の保持が可能で、かつ、書き込み回数にも制限が無いというメリットを有している。というのは、本実施の形態で示すトランジスタは、オフ電流が小さいため、容量４３０に蓄えられた電荷を逃しにくいからである。

【０１０５】

（実施の形態３）

本実施の形態では、実施の形態１で例示した酸化物半導体層４０３に用いることができる、ＣＡＡＣ－ＯＳ（Ｃ　Ａｘｉｓ　Ａｌｉｇｎｅｄ　Ｃｒｙｓｔａｌｌｉｎｅ　Ｏｘｉｄｅ　Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）膜について説明する。

【０１０６】

ＣＡＡＣ－ＯＳ膜は、完全な単結晶ではなく、完全な非晶質でもない。ＣＡＡＣ－ＯＳ膜は、非晶質相に結晶部を有する結晶－非晶質混相構造の酸化物半導体である。なお、当該結晶部は、一辺が１００ｎｍ未満の立方体内に収まる大きさであることが多い。また、透過型電子顕微鏡（ＴＥＭ：Ｔｒａｎｓｍｉｓｓｉｏｎ　Ｅｌｅｃｔｒｏｎ　Ｍｉｃｒｏｓｃｏｐｅ）による観察像では、ＣＡＡＣ－ＯＳ膜に含まれる非晶質部と結晶部との境界は明確ではない。また、ＴＥＭによってＣＡＡＣ－ＯＳ膜には粒界（グレインバウンダリーともいう）は確認できない。そのため、ＣＡＡＣ－ＯＳ膜は、粒界に起因する電子移動の低下が抑制される。

【０１０７】

ＣＡＡＣ－ＯＳ膜に含まれる結晶部は、ｃ軸がＣＡＡＣ－ＯＳ膜の被形成面または表面に垂直な方向に揃い、かつａｂ面に垂直な方向から見て三角形状または六角形状の原子配列を有し、ｃ軸に垂直な方向から見て金属原子が層状または金属原子と酸素原子とが層状に配列している。なお、異なる結晶部間で、それぞれａ軸およびｂ軸の向きが異なっていてもよい。本明細書等において、単に垂直と記載する場合、８５°以上９５°以下の範囲も含まれることとする。

【０１０８】

なお、ＣＡＡＣ－ＯＳ膜において、結晶部の分布が一様でなくてもよい。例えば、ＣＡＡＣ－ＯＳ膜の形成過程において、酸化物半導体膜の表面側から結晶成長させる場合、被形成面の近傍に対し表面の近傍では結晶部の占める割合が高くなることがある。

【０１０９】

ＣＡＡＣ－ＯＳ膜に含まれる結晶部のｃ軸は、ＣＡＡＣ－ＯＳ膜の被形成面または表面に垂直な方向に揃うため、ＣＡＡＣ－ＯＳ膜の形状（被形成面の断面形状または表面の断面形状）によっては互いに異なる方向を向くことがある。なお、結晶部のｃ軸の方向は、ＣＡＡＣ－ＯＳ膜が形成されたときの被形成面または表面に垂直な方向となる。結晶部は、成膜することにより、または成膜後に熱処理などの結晶化処理を行うことにより形成される。

【０１１０】

また、ＣＡＡＣ－ＯＳのように結晶部を有する酸化物半導体では、よりバルク内欠陥を低減することができ、表面の平坦性を高めればアモルファス状態の酸化物半導体以上の移動度を得ることができる。表面の平坦性を高めるためには、平坦な表面上に酸化物半導体を形成することが好ましく、具体的には、平均面粗さ（Ｒａ）が１ｎｍ以下、好ましくは０．３ｎｍ以下、より好ましくは０．１ｎｍ以下の表面上に形成するとよい。ただし、トランジスタ４４０は、ボトムゲート型であるため、上記平坦な表面を得るためにゲート電極層４０１および下地絶縁層４３６を形成した後、ＣＭＰ処理などの平坦化処理を行うことにより、酸化物半導体層４０３の被形成面の平坦性を向上させることができる。

【０１１１】

ＣＡＡＣ－ＯＳ膜を酸化物半導体層４０３として用いたトランジスタは、可視光や紫外光の照射によるトランジスタの電気特性（閾値など）の変動を低減させることが可能である。よって、当該トランジスタは信頼性が高い。

【０１１２】

（実施の形態４）

本実施の形態では、本明細書に示すトランジスタを使用し、電力が供給されない状況でも記憶内容の保持が可能で、かつ、書き込み回数にも制限が無い半導体装置（記憶装置）の一例を、図面を用いて説明する。

【０１１３】

図９は、半導体装置の構成の一例である。図９（Ａ）に、半導体装置の断面図を、図９（Ｂ）に半導体装置の回路図をそれぞれ示す。

【０１１４】

図９（Ａ）及び図９（Ｂ）に示す半導体装置は、下部に第１の半導体材料を用いたトランジスタ３２００を有し、上部に第２の半導体材料を用いたトランジスタ３２０２を有するものである。トランジスタ３２０２としては、実施の形態１で示すトランジスタ４４０の構造を適用する例である。

【０１１５】

ここで、第１の半導体材料と第２の半導体材料は異なる禁制帯幅を持つ材料とすることが望ましい。例えば、第１の半導体材料をワイドバンドギャップ半導体以外の半導体材料（シリコンなど）とし、第２の半導体材料をワイドバンドギャップ半導体とすることができる。一方で、ワイドバンドギャップ半導体を用いたトランジスタは、その特性により長時間の電荷保持を可能とする。

【０１１６】

なお、上記トランジスタは、いずれもｎチャネル型トランジスタであるものとして説明するが、ｐチャネル型トランジスタを用いることができるのはいうまでもない。また、情報を保持するためにワイドバンドギャップ半導体を用いた実施の形態１又は実施の形態２に示すようなトランジスタを用いる他は、半導体装置に用いられる材料や半導体装置の構造など、半導体装置の具体的な構成をここで示すものに限定する必要はない。

【０１１７】

図９（Ａ）におけるトランジスタ３２００は、半導体材料（例えば、シリコンなど）を含む基板３０００に設けられたチャネル形成領域と、チャネル形成領域を挟むように設けられた不純物領域と、不純物領域に接する金属化合物領域と、チャネル形成領域上に設けられたゲート絶縁膜と、ゲート絶縁膜上に設けられたゲート電極層と、を有する。なお、図において、明示的にはソース電極層やドレイン電極層を有しない場合があるが、便宜上、このような状態を含めてトランジスタと呼ぶ場合がある。また、この場合、トランジスタの接続関係を説明するために、ソース領域やドレイン領域を含めてソース電極層やドレイン電極層と表現することがある。つまり、本明細書において、ソース電極層との記載には、ソース領域が含まれうる。

【０１１８】

基板３０００上にはトランジスタ３２００を囲むように素子分離絶縁層３１０６が設けられており、トランジスタ３２００を覆うように絶縁層３２２０が設けられている。

【０１１９】

単結晶半導体基板を用いたトランジスタ３２００は、高速動作が可能である。このため、当該トランジスタを読み出し用のトランジスタとして用いることで、情報の読み出しを高速に行うことができる。トランジスタ３２０２および容量素子３２０４の形成前の処理として、トランジスタ３２００を覆う絶縁層３２２０にＣＭＰ処理を施して、絶縁層３２２０を平坦化すると同時にトランジスタ３２００のゲート電極層の上面を露出させる。

【０１２０】

図９（Ａ）に示すトランジスタ３２０２は、ワイドバンドギャップ半導体をチャネル形成領域に用いたボトムゲート型トランジスタである。ここで、トランジスタ３２０２に含まれる酸化物半導体層は、高純度化されたものであることが望ましい。高純度化された酸化物半導体層を用いることで、極めて優れたオフ特性のトランジスタ３２０２を得ることができる。

【０１２１】

図９（Ｂ）は、トランジスタ３２０２を用いた半導体記録装置の一例である。トランジスタ３２０２にオフ電流が小さいトランジスタ用いると、当該半導体記録装置は長期にわたり記憶内容を保持することが可能である。つまり、リフレッシュ動作を必要としない、或いは、リフレッシュ動作の頻度が極めて少ない半導体記憶装置とすることが可能となるため、消費電力を１０分に低減することができる。

【０１２２】

トランジスタ３２０２のソース電極層又はドレイン電極層の一方は、ゲート絶縁層に設けられた開口を介して、電極３２０８と電気的に接続され、電極３２０８を介してトランジスタ３２００のゲート電極層と電気的に接続されている。電極３２０８は、トランジスタ３２０２のゲート電極層と同様の工程で作製することができる。

【０１２３】

また、トランジスタ３２０２上には、絶縁層３２２２と絶縁層３２２３と絶縁層３２２３ａが設けられている。そして、絶縁層３２２２と絶縁層３２２３と絶縁層３２２３ａを介してトランジスタ３２０２のソース電極層又はドレイン電極層の一方と重畳する領域には、導電層３２１０ａが設けられており、トランジスタ３２０２のソース電極層又はドレイン電極層の一方と、絶縁層３２２２と導電層３２１０ａとによって、容量素子３２０４が構成される。すなわち、トランジスタ３２０２のソース電極層又はドレイン電極層の一方は、容量素子３２０４の一方の電極として機能し、導電層３２１０ａは、容量素子３２０４の他方の電極として機能する。なお、容量が不要の場合には、容量素子３２０４を設け

ない構成とすることもできる。また、容量素子３２０４は、別途、トランジスタ３２０２の上方に設けてもよい。

【０１２４】

容量素子３２０４上には絶縁層３２２４が設けられている。そして、絶縁層３２２４上にはトランジスタ３２０２と、他のトランジスタを接続するための配線３２１６が設けられている。配線３２１６は、絶縁層３２２４に形成された開口に設けられた３２１４、導電層３２１０ａと同じ層に設けられた導電層３２１０ｂ、及び、絶縁層３２２２に形成された開口に設けられた電極３２１２を介して、トランジスタ３２０２のソース電極層又はドレイン電極層の他方と電気的に接続される。

【０１２５】

図９（Ａ）及び図９（Ｂ）において、トランジスタ３２００と、トランジスタ３２０２とは、少なくとも一部が重畳するように設けられており、トランジスタ３２００のソース領域またはドレイン領域と、トランジスタ３２０２に含まれる酸化物半導体層の一部が重畳するように設けられているのが好ましい。また、トランジスタ３２０２及び容量素子３２０４が、トランジスタ３２００の少なくとも一部と重畳するように設けられている。例えば、容量素子３２０４の導電層３２１０ａは、トランジスタ３２００のゲート電極層と少なくとも一部が重畳して設けられている。このような平面レイアウトを採用することにより、半導体装置の占有面積の低減を図ることができるため、高集積化を図ることができる。

【０１２６】

次に、図９（Ａ）に対応する回路構成の一例を図９（Ｂ）に示す。

【０１２７】

図９（Ｂ）において、第１の配線（１ｓｔ　Ｌｉｎｅ）とトランジスタ３２００のソース電極層とは、電気的に接続され、第２の配線（２ｎｄ　Ｌｉｎｅ）とトランジスタ３２００のドレイン電極層とは、電気的に接続されている。また、第３の配線（３ｒｄ　Ｌｉｎｅ）とトランジスタ３２０２のソース電極層またはドレイン電極層の一方とは、電気的に接続され、第４の配線（４ｔｈ　Ｌｉｎｅ）と、トランジスタ３２０２のゲート電極層とは、電気的に接続されている。そして、トランジスタ３２００のゲート電極層と、トランジスタ３２０２のソース電極層またはドレイン電極層の一方は、容量素子３２０４の電極の他方と電気的に接続され、第５の配線（５ｔｈ　Ｌｉｎｅ）と、容量素子３２０４の電極の他方は電気的に接続されている。

【０１２８】

図９（Ｂ）に示す半導体装置では、トランジスタ３２００のゲート電極層の電位が保持可能という特徴を生かすことで、次のように、情報の書き込み、保持、読み出しが可能である。

【０１２９】

情報の書き込みおよび保持について説明する。まず、第４の配線の電位を、トランジスタ３２０２がオン状態となる電位にして、トランジスタ３２０２をオン状態とする。これにより、第３の配線の電位が、トランジスタ３２００のゲート電極層、および容量素子３２０４に与えられる。すなわち、トランジスタ３２００のゲート電極層には、所定の電荷が与えられる（書き込み）。ここでは、異なる二つの電位レベルを与える電荷（以下Ｌｏｗレベル電荷、Ｈｉｇｈレベル電荷という）のいずれかが与えられるものとする。その後、第４の配線の電位を、トランジスタ３２０２がオフ状態となる電位にして、トランジスタ３２０２をオフ状態とすることにより、トランジスタ３２００のゲート電極層に与えられた電荷が保持される（保持）。

【０１３０】

トランジスタ３２０２のオフ電流は極めて小さいため、トランジスタ３２００のゲート電極層の電荷は長時間にわたって保持される。

【０１３１】

次に情報の読み出しについて説明する。第１の配線に所定の電位（定電位）を与えた状態

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で、第５の配線に適切な電位（読み出し電位）を与えると、トランジスタ３２００のゲート電極層に保持された電荷量に応じて、第２の配線は異なる電位をとる。一般に、トランジスタ３２００をｎチャネル型とすると、トランジスタ３２００のゲート電極層にＨｉｇｈレベル電荷が与えられている場合の見かけの閾値Ｖｔｈ＿Ｈは、トランジスタ３２００のゲート電極層にＬｏｗレベル電荷が与えられている場合の見かけの閾値Ｖｔｈ＿Ｌより低くなるためである。ここで、見かけの閾値とは、トランジスタ３２００を「オン状態」とするために必要な第５の配線の電位をいうものとする。したがって、第５の配線の電位をＶｔｈ＿ＨとＶｔｈ＿Ｌの中間の電位$Ｖ_0$とすることにより、トランジスタ３２００のゲート電極層に与えられた電荷を判別できる。例えば、書き込みにおいて、Ｈｉｇｈレベル電荷が与えられていた場合には、第５の配線の電位が$Ｖ_0$（＞Ｖｔｈ＿Ｈ）となれば、トランジスタ３２００は「オン状態」となる。Ｌｏｗレベル電荷が与えられていた場合には、第５の配線の電位が$Ｖ_0$（＜Ｖｔｈ＿Ｌ）となっても、トランジスタ３２００は「オフ状態」のままである。このため、第２の配線の電位を見ることで、保持されている情報を読み出すことができる。

【０１３２】

なお、メモリセルをアレイ状に配置して用いる場合、所望のメモリセルの情報のみを読み出せることが必要になる。このように情報を読み出さない場合には、ゲート電極層の状態にかかわらずトランジスタ３２００が「オフ状態」となるような電位、つまり、Ｖｔｈ＿Ｈより小さい電位を第５の配線に与えればよい。または、ゲート電極層の状態にかかわらずトランジスタ３２００が「オン状態」となるような電位、つまり、Ｖｔｈ＿Ｌより大きい電位を第５の配線に与えればよい。

【０１３３】

本実施の形態に示す半導体装置では、チャネル形成領域にワイドバンドギャップ半導体を用いたオフ電流の極めて小さいトランジスタを適用することで、極めて長期にわたり記憶内容を保持することが可能である。つまり、リフレッシュ動作が不要となるか、または、リフレッシュ動作の頻度を極めて低くすることが可能となるため、消費電力を１０分に低減することができる。また、電力の供給がない場合（ただし、電位は固定されていることが望ましい）であっても、長期にわたって記憶内容を保持することが可能である。

【０１３４】

また、本実施の形態に示す半導体装置では、情報の書き込みに高い電圧を必要とせず、素子の劣化の問題もない。例えば、従来の不揮発性メモリのように、フローティングゲートへの電子の注入や、フローティングゲートからの電子の引き抜きを行う必要がないため、ゲート絶縁膜の劣化といった問題が全く生じない。すなわち、開示する発明に係る半導体装置では、従来の不揮発性メモリで問題となっている書き換え可能回数に制限はなく、信頼性が飛躍的に向上する。さらに、トランジスタのオン状態、オフ状態によって、情報の書き込みが行われるため、高速な動作も容易に実現しうる。

【０１３５】

以上のように、微細化及び高集積化を実現し、かつ高い電気的特性を付与された半導体装置、及び該半導体装置の作製方法を提供することができる。

【０１３６】

以上、本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。

【０１３７】

（実施の形態５）

本実施の形態では、実施の形態４と異なる構成の記憶装置の構造の一形態について説明する。

【０１３８】

図１０は、記憶装置の斜視図である。図１０に示す記憶装置は上部に記憶回路としてメモリセルを複数含む、メモリセルアレイ（メモリセルアレイ３４００ａからメモリセルアレイ３４００ｎ（ｎは２以上の整数））を複数層有し、下部にメモリセルアレイ３４００ａ

からメモリセルアレイ３４００ｎを動作させるために必要な論理回路３００４を有する。
【０１３９】
図１１に、図１０に示した記憶装置の部分拡大図を示す。図１１では、論理回路３００４、メモリセルアレイ３４００ａ及びメモリセルアレイ３４００ｂを図示しており、メモリセルアレイ３４００ａ又はメモリセルアレイ３４００ｂに含まれる複数のメモリセルのうち、メモリセル３１７０ａと、メモリセル３１７０ｂを代表で示す。メモリセル３１７０ａ及びメモリセル３１７０ｂとしては、例えば、上記に実施の形態において説明した回路構成と同様の構成とすることもできる。
【０１４０】
なお、メモリセル３１７０ａに含まれるトランジスタ３１７１ａを代表で示す。メモリセル３１７０ｂに含まれるトランジスタ３１７１ｂを代表で示す。トランジスタ３１７１ａ及びトランジスタ３１７１ｂは、酸化物半導体層にチャネル形成領域を有する。酸化物半導体層にチャネル形成領域が形成されるトランジスタの構成については、その他の実施の形態において説明した構成と同様であるため、説明は省略する。
【０１４１】
トランジスタ３１７１ａのゲート電極層と同じ層に形成された導電層３５０１ａは、電極３５０２ａによって、電極３００３ａと電気的に接続されている。トランジスタ３１７１ｂのゲート電極層と同じ層に形成された、導電層３５０１ｃは、電極３５０２ｃによって、電極３００３ｃと電気的に接続されている。
【０１４２】
また、論理回路３００４は、ワイドバンドギャップ半導体以外の半導体材料をチャネル形成領域として用いたトランジスタ３００１を有する。トランジスタ３００１は、半導体材料（例えば、シリコンなど）を含む基板３０００に素子分離絶縁層３１０６を設け、素子分離絶縁層３１０６に囲まれた領域にチャネル形成領域となる領域を形成することによって得られるトランジスタとすることができる。なお、トランジスタ３００１は、絶縁表面上に形成されたシリコン膜等の半導体膜や、ＳＯＩ基板のシリコン膜にチャネル形成領域が形成されるトランジスタであってもよい。トランジスタ３００１の構成については、公知の構成を用いることが可能であるため、説明は省略する。
【０１４３】
トランジスタ３１７１ａが形成された層と、トランジスタ３００１が形成された層との間には、配線３１００ａ及び配線３１００ｂが形成されている。配線３１００ａとトランジスタ３００１が形成された層との間には、絶縁膜３１４０ａが設けられ、配線３１００ａと配線３１００ｂとの間には、絶縁膜３１４１ａが設けられ、配線３１００ｂとトランジスタ３１７１ａが形成された層との間には、絶縁膜３１４２ａが設けられている。
【０１４４】
同様に、トランジスタ３１７１ｂが形成された層と、トランジスタ３１７１ａが形成された層との間には、配線３１００ｃ及び配線３１００ｄが形成されている。配線３１００ｃとトランジスタ３１７１ａが形成された層との間には、絶縁膜３１４０ｂが設けられ、配線３１００ｃと配線３１００ｄとの間には、絶縁膜３１４１ｂが設けられ、配線３１００ｄとトランジスタ３１７１ｂが形成された層との間には、絶縁膜３１４２ｂが設けられている。
【０１４５】
絶縁膜３１４０ａ、絶縁膜３１４１ａ、絶縁膜３１４２ａ、絶縁膜３１４０ｂ、絶縁膜３１４１ｂ、絶縁膜３１４２ｂは、層間絶縁膜として機能し、その表面は平坦化された構成とすることができる。
【０１４６】
配線３１００ａ、配線３１００ｂ、配線３１００ｃ、配線３１００ｄによって、メモリセル間の電気的接続や、論理回路３００４とメモリセルとの電気的接続等を行うことができる。
【０１４７】

論理回路３００４に含まれる電極３３０３は、上部に設けられた回路と電気的に接続することができる。
【０１４８】
例えば、図１１に示すように、電極３５０５によって電極３３０３は配線３１００ａと電気的に接続することができる。配線３１００ａは、電極３５０３ａによって、トランジスタ３１７１ａのゲート電極層と同じ層に形成された、導電層３５０１ｂと電気的に接続することができる。こうして、配線３１００ａ及び電極３３０３を、トランジスタ３１７１ａのソースまたはドレインと電気的に接続することができる。また、導電層３５０１ｂは、トランジスタ３１７１ａのソースまたはドレインと、電極３５０２ｂとによって、電極３００３ｂと電気的に接続することができる。電極３００３ｂは、電極３５０３ｂによって配線３１００ｃと電気的に接続することができる。
【０１４９】
図１１では、電極３３０３とトランジスタ３１７１ａとの電気的接続は、配線３１００ａを介して行われる例を示したがこれに限定されない。電極３３０３とトランジスタ３１７１ａとの電気的接続は、配線３１００ｂを介して行われてもよいし、配線３１００ａと配線３１００ｂの両方を介して行われてもよい。または、配線３１００ａも配線３１００ｂも介さず、他の電極を用いて行われてもよい。
【０１５０】
また、図１１では、トランジスタ３１７１ａが形成された層と、トランジスタ３００１が形成された層との間には、配線３１００ａが形成された配線層と、配線３１００ｂが形成された配線層との、２つの配線層が設けられた構成を示したがこれに限定されない。トランジスタ３１７１ａが形成された層と、トランジスタ３００１が形成された層との間に、１つの配線層が設けられていてもよいし、３つ以上の配線層が設けられていてもよい。
【０１５１】
また、図１１では、トランジスタ３１７１ｂが形成された層と、トランジスタ３１７１ａが形成された層との間には、配線３１００ｃが形成された配線層と、配線３１００ｄが形成された配線層との、２つの配線層が設けられた構成を示したがこれに限定されない。トランジスタ３１７１ｂが形成された層と、トランジスタ３１７１ａが形成された層との間に、１つの配線層が設けられていてもよいし、３つ以上の配線層が設けられていてもよい。
【０１５２】
以上、本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。
【０１５３】
（実施の形態６）
本明細書に開示する半導体装置は、さまざまな電子機器（遊技機も含む）に適用することができる。電子機器としては、テレビジョン装置（テレビ、またはテレビジョン受信機ともいう）、コンピュータ用などのモニタ、デジタルカメラ、デジタルビデオカメラ、デジタルフォトフレーム、携帯電話機、携帯型ゲーム機、携帯情報端末、音響再生装置、遊技機（パチンコ機、スロットマシン等）、ゲーム筐体が挙げられる。これらの電子機器の具体例を図１２に示す。
【０１５４】
図１２（Ａ）および図１２（Ｂ）は２つ折り可能なタブレット型端末である。図１２（Ａ）は、開いた状態であり、タブレット型端末は、筐体９６３０、表示部９６３１ａ、表示部９６３１ｂ、表示モード切り替えスイッチ９０３４、電源スイッチ９０３５、省電力モード切り替えスイッチ９０３６、留め具９０３３、操作スイッチ９０３８、を有する。
【０１５５】
実施の形態１および２のいずれかに示す半導体装置は、表示部９６３１ａ、表示部９６３１ｂに用いることが可能であり、信頼性の高いタブレット型端末とすることが可能となる。

【０１５６】
表示部９６３１ａは、一部をタッチパネルの領域９６３２ａとすることができ、表示された操作キー９６３８にふれることでデータ入力をすることができる。なお、表示部９６３１ａにおいては、一例として半分の領域が表示のみの機能を有する構成、もう半分の領域がタッチパネルの機能を有する構成を示しているが該構成に限定されない。表示部９６３１ａの全ての領域がタッチパネルの機能を有する構成としても良い。例えば、表示部９６３１ａの全面をキーボードボタン表示させてタッチパネルとし、表示部９６３１ｂを表示画面として用いることができる。
【０１５７】
また、表示部９６３１ｂにおいても表示部９６３１ａと同様に、表示部９６３１ｂの一部をタッチパネルの領域９６３２ｂとすることができる。また、タッチパネルのキーボード表示切り替えボタン９６３９が表示されている位置に指やスタイラスなどでふれることで表示部９６３１ｂにキーボードボタン表示することができる。
【０１５８】
また、タッチパネルの領域９６３２ａとタッチパネルの領域９６３２ｂに対して同時にタッチ入力することもできる。
【０１５９】
また、表示モード切り替えスイッチ９０３４は、縦表示または横表示などの表示の向きを切り替え、白黒表示やカラー表示の切り替えなどを選択できる。省電力モード切り替えスイッチ９０３６は、タブレット型端末に内蔵している光センサで検出される使用時の外光の光量に応じて表示の輝度を最適なものとすることができる。タブレット型端末は光センサだけでなく、ジャイロ、加速度センサ等の傾きを検出するセンサなどの他の検出装置を内蔵させてもよい。
【０１６０】
また、図１２（Ａ）では表示部９６３１ｂと表示部９６３１ａの表示面積が同じ例を示しているが特に限定されず、一方のサイズともう一方のサイズが異なっていてもよく、表示の品質も異なっていてもよい。例えば一方が他方よりも高精細な表示を行える表示パネルとしてもよい。
【０１６１】
図１２（Ｂ）は、閉じた状態であり、タブレット型端末は、筐体９６３０、太陽電池９６３３、充放電制御回路９６３４、バッテリー９６３５、ＤＣＤＣコンバータ９６３６を有する。なお、図１２（Ｂ）では充放電制御回路９６３４の一例としてバッテリー９６３５、ＤＣＤＣコンバータ９６３６を有する構成について示している。
【０１６２】
なお、タブレット型端末は２つ折り可能なため、未使用時に筐体９６３０を閉じた状態にすることができる。従って、表示部９６３１ａ、表示部９６３１ｂを保護できるため、耐久性に優れ、長期使用の観点からも信頼性の優れたタブレット型端末を提供できる。
【０１６３】
また、この他にも図１２（Ａ）および図１２（Ｂ）に示したタブレット型端末は、様々な情報（静止画、動画、テキスト画像など）を表示する機能、カレンダー、日付または時刻などを表示部に表示する機能、表示部に表示した情報をタッチ入力操作または編集するタッチ入力機能、様々なソフトウェア（プログラム）によって処理を制御する機能、等を有することができる。
【０１６４】
タブレット型端末の表面に装着された太陽電池９６３３によって、電力をタッチパネル、表示部、または映像信号処理部等に供給することができる。なお、太陽電池９６３３は、筐体９６３０の一面または二面に効率的なバッテリー９６３５の充電を行う構成とすることができるため好適である。なおバッテリー９６３５としては、リチウムイオン電池を用いると、小型化を図れる等の利点がある。
【０１６５】

また、図１２（Ｂ）に示す充放電制御回路９６３４の構成、および動作について図１２（Ｃ）にブロック図を示し説明する。図１２（Ｃ）には、太陽電池９６３３、バッテリー９６３５、ＤＣＤＣコンバータ９６３６、コンバータ９６３７、スイッチＳＷ１からＳＷ３、表示部９６３１について示しており、バッテリー９６３５、ＤＣＤＣコンバータ９６３６、コンバータ９６３７、スイッチＳＷ１からＳＷ３が、図１２（Ｂ）に示す充放電制御回路９６３４に対応する箇所となる。

【０１６６】

まず外光により太陽電池９６３３により発電がされる場合の動作の例について説明する。太陽電池で発電した電力は、バッテリー９６３５を充電するための電圧となるようＤＣＤＣコンバータ９６３６で昇圧または降圧がなされる。そして、表示部９６３１の動作に太陽電池９６３３からの電力が用いられる際にはスイッチＳＷ１をオンにし、コンバータ９６３７で表示部９６３１に必要な電圧に昇圧または降圧をすることとなる。また、表示部９６３１での表示を行わない際には、ＳＷ１をオフにし、ＳＷ２をオンにしてバッテリー９６３５の充電を行う構成とすればよい。

【０１６７】

なお太陽電池９６３３については、発電手段の一例として示したが、特に限定されず、圧電素子（ピエゾ素子）や熱電変換素子（ペルティエ素子）などの他の発電手段によるバッテリー９６３５の充電を行う構成であってもよい。例えば、無線（非接触）で電力を送受信して充電する無接点電力電送モジュールや、また他の充電手段を組み合わせて行う構成としてもよい。

【０１６８】

本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。

【符号の説明】

【０１６９】

４００　基板
４０１　ゲート電極層
４０２　ゲート絶縁層
４０３　酸化物半導体層
４０５　低抵抗材料層
４０５ａ　第１低抵抗材料層
４０５ｂ　第２低抵抗材料層
４０６　第１保護層
４０７　第２保護層
４０７ａ　第３保護層
４０７ｂ　第４保護層
４２０　トランジスタ
４３０　容量
４３１　トランジスタ
４３２　絶縁層
４３６　下地絶縁層
４４０　トランジスタ
４５１　酸素ドーピング
４５３　レジスト
４５４　導電膜
４５４ａ　第１導電層
４５４ｂ　第２導電層
４５５　レジスト
４７４ａ　配線層
４７４ｂ　配線層

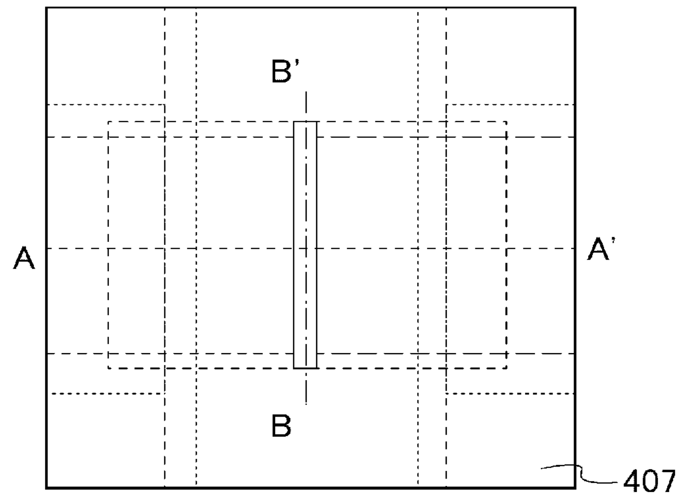
４９５　ハードマスク層
３０００　基板
３００１　トランジスタ
３００３ａ　電極
３００３ｂ　電極
３００３ｃ　電極
３００４　論理回路
３１００ａ　配線
３１００ｂ　配線
３１００ｃ　配線
３１００ｄ　配線
３１０６　素子分離絶縁層
３１４０ａ　絶縁膜
３１４０ｂ　絶縁膜
３１４１ａ　絶縁膜
３１４１ｂ　絶縁膜
３１４２ａ　絶縁膜
３１４２ｂ　絶縁膜
３１７０ａ　メモリセル
３１７０ｂ　メモリセル
３１７１ａ　トランジスタ
３１７１ｂ　トランジスタ
３２００　トランジスタ
３２０２　トランジスタ
３２０４　容量素子
３２０８　電極
３２１０ａ　導電層
３２１０ｂ　導電層
３２１２　電極
３２１６　配線
３２２０　絶縁層
３２２２　絶縁層
３２２３　絶縁層
３２２３ａ　絶縁層
３２２４　絶縁層
３３０３　電極
３４００ａ　メモリセルアレイ
３４００ｂ　メモリセルアレイ
３４００ｎ　メモリセルアレイ
３５０１ａ　導電層
３５０１ｂ　導電層
３５０１ｃ　導電層
３５０２ａ　電極
３５０２ｂ　電極
３５０２ｃ　電極
３５０３ａ　電極
３５０３ｂ　電極
３５０５　電極
９０３３　留め具
９０３４　スイッチ

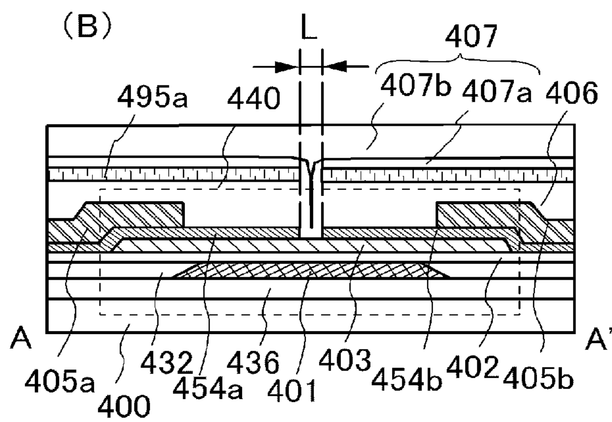
９０３５　　電源スイッチ
９０３６　　スイッチ
９０３８　　操作スイッチ
９６３０　　筐体
９６３１　　表示部
９６３１ａ　　表示部
９６３１ｂ　　表示部
９６３２ａ　　領域
９６３２ｂ　　領域
９６３３　　太陽電池
９６３４　　充放電制御回路
９６３５　　バッテリー
９６３６　　ＤＣＤＣコンバータ
９６３７　　コンバータ
９６３８　　操作キー
９６３９　　ボタン

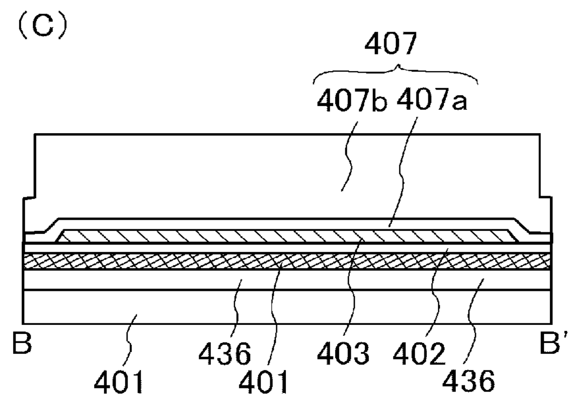
【書類名】特許請求の範囲
【請求項１】
絶縁表面上にゲート電極層を形成する工程と、
前記ゲート電極層の上に接するようにゲート絶縁層を形成する工程と、
前記ゲート絶縁層の上に接して、かつ前記ゲート電極層と重なるように、酸化物半導体層を形成する工程と、
前記酸化物半導体層の上に接して、かつ前記酸化物半導体層を覆うように、導電膜を形成する工程と、
前記導電膜の上に接し前記ゲート電極層を挟んで離間する、第１低抵抗材料層と第２低抵抗材料層を形成する工程と、
前記第１低抵抗材料層および前記第２低抵抗材料層ならびに前記導電膜の上に接するように、第１保護層を形成する工程と、
前記第１保護層を平坦化する工程と、
平坦化した前記第１保護層の上に接するように、ハードマスク層を形成する工程と、
前記ハードマスク層の表面において、前記第１低抵抗材料層と前記第２低抵抗材料層の間で、かつ前記酸化物半導体層と重なる領域に、開口パターン部を有するレジストパターンを形成する工程と、
前記レジストパターンを用いて、前記ハードマスク層をエッチングして開口パターンを形成する工程と、
前記開口パターンを有するハードマスク層をマスクとして用いて、前記第１保護層を導電層が露出するまでエッチングする工程と、
前記開口パターンを有するハードマスク層と前記第１保護層をマスクとして用いて、前記導電膜をエッチングして、第１導電層と第２導電層に分離して形成する工程と、
前記第１保護層の開口部を第２絶縁層で充填する工程と、
を有する半導体装置の作製方法。
【請求項２】
ゲート電極層と、
前記ゲート電極層の上に接するゲート絶縁層と、
前記ゲート絶縁層の上に接し、かつ前記ゲート電極層と重なるように設けられた酸化物半導体層と、
前記酸化物半導体層の上に接し前記ゲート電極層を挟んで離間する、第１導電層と第２導電層と、
前記第１導電層の上に接する第１低抵抗材料層と、
前記第２導電層の上に接する第２低抵抗材料層と、
第１保護層は、前記第１導電層および前記第１低抵抗材料層ならびに前記第２導電層および前記第２低抵抗材料層の上に接するように設けられ、
第２絶縁層は、前記酸化物半導体層と一部に接するように設けられ、
前記第１導電層と前記第２導電層の間隔は、前記第１低抵抗材料層と前記第２低抵抗材料層の間隔よりも狭く、
前記第１導電層および前記第１低抵抗材料層はソース電極であり、前記第２導電層および前記第２低抵抗材料層はドレイン電極であることを特徴とする半導体装置。
【請求項３】
請求項２において、前記ゲート絶縁層が、平坦であることを特徴とする半導体装置。
【請求項４】
請求項２または請求項３において、前記酸化物半導体層のチャネル長方向の幅は、前記ゲート電極層のチャネル長方向の幅よりも広いことを特徴とする半導体装置。

【書類名】要約書
【要約】
【課題】微細なチャネル長のボトムゲート型トランジスタを作製する方法、およびそのトランジスタを提供する。
【解決手段】ソース電極およびドレイン電極のチャネル形成領域に近接する部分を、他の部分より薄い構成にする微細なチャネル長のボトムゲート型トランジスタを創作した。また、ソース電極およびドレイン電極のチャネル形成領域に近接する部分を、他の部分より後の工程で形成する方法により、チャネル長が微細なボトムゲート型トランジスタ作製することができる。
【選択図】図１

【書類名】図面
【図１】



【図２】

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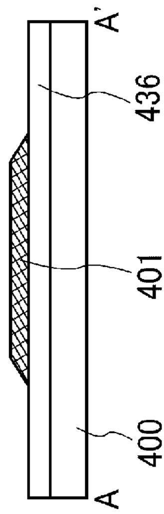


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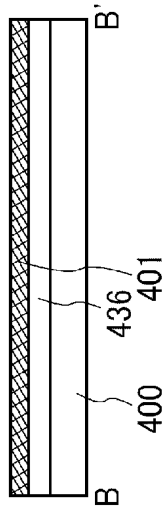


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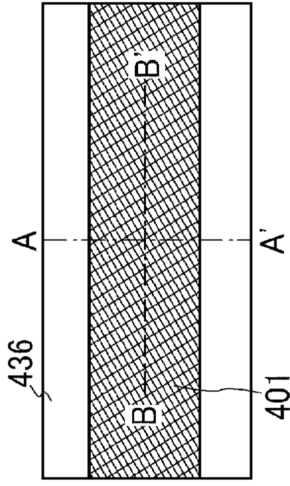


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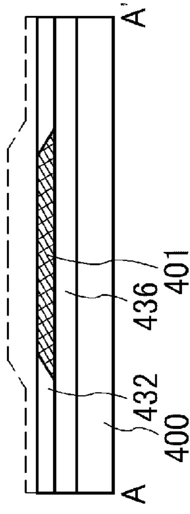


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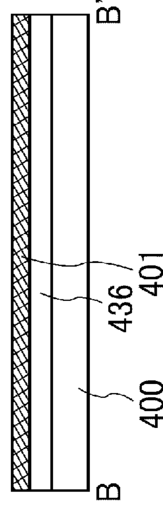


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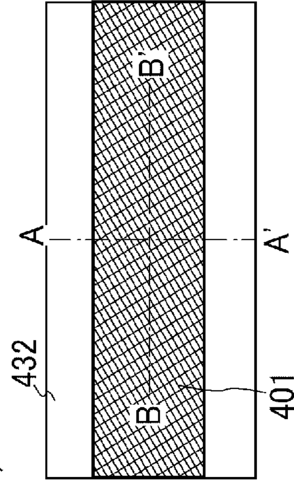


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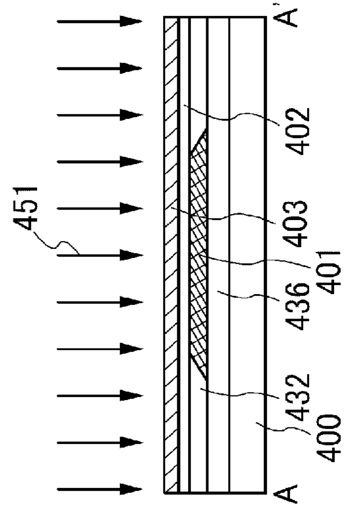


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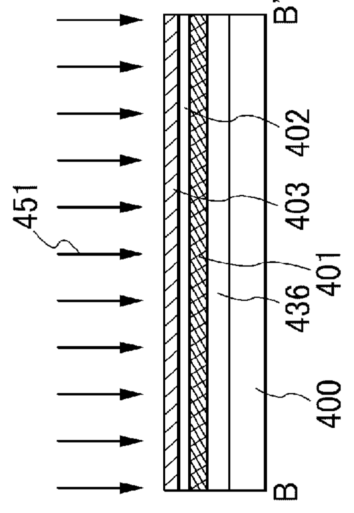


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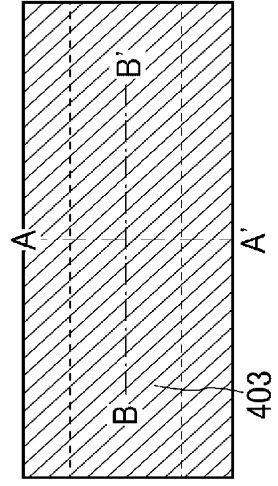

【図３】

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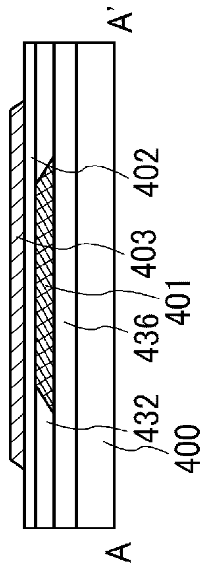


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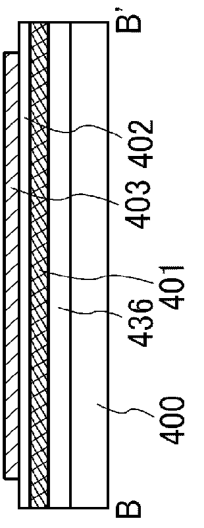


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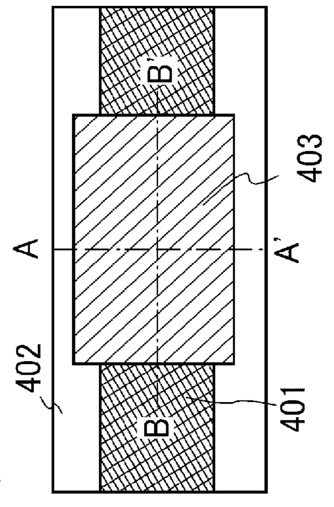


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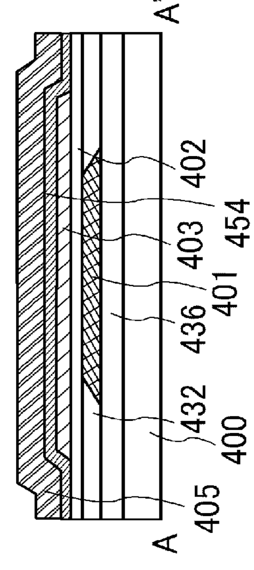


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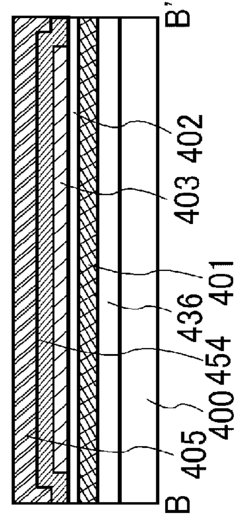


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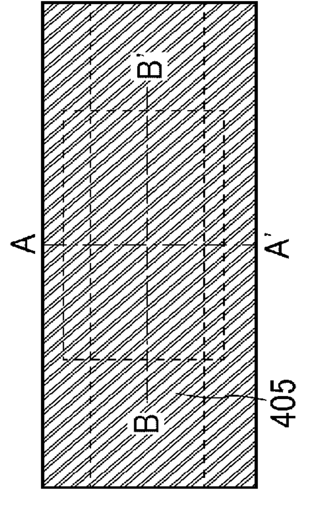


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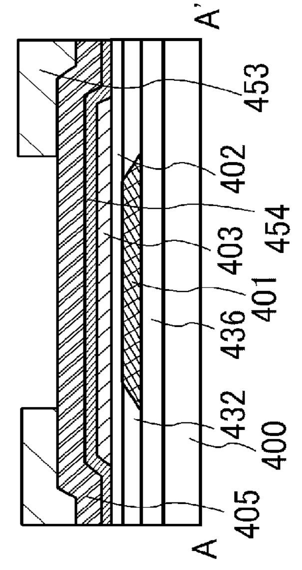


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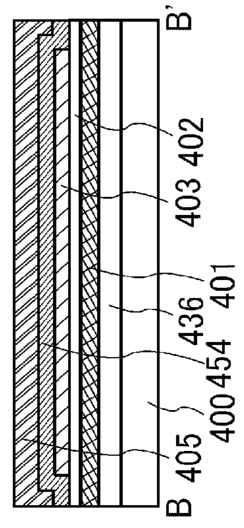


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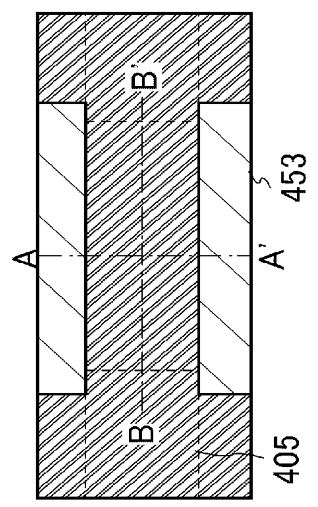

【図４】

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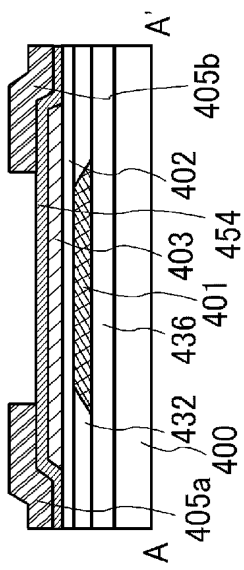


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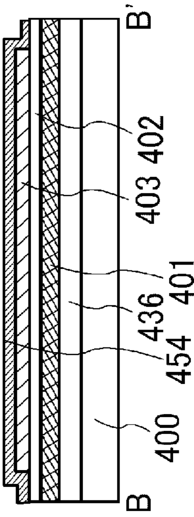


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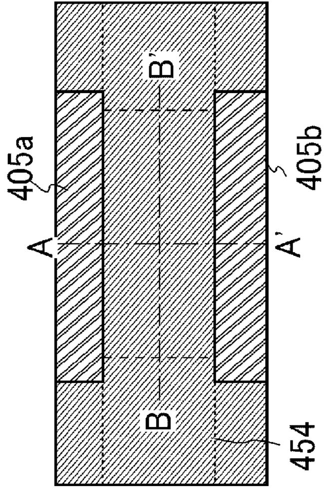


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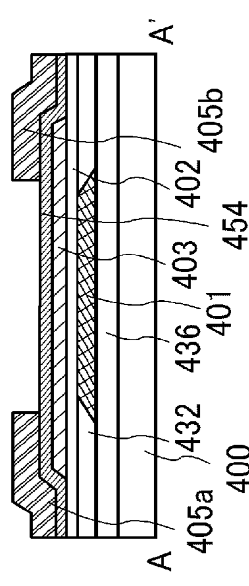


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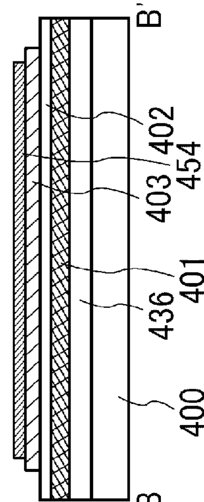


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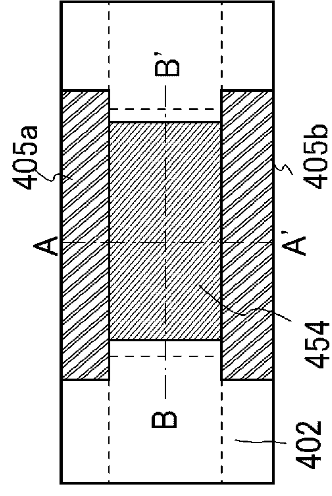


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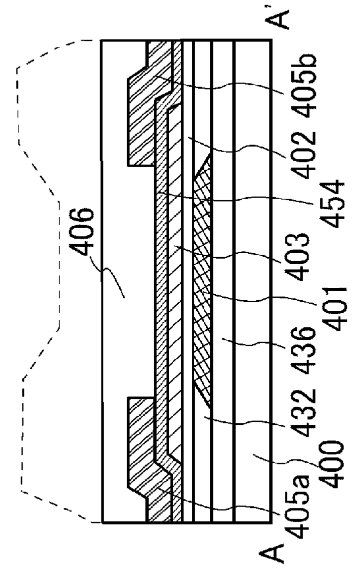


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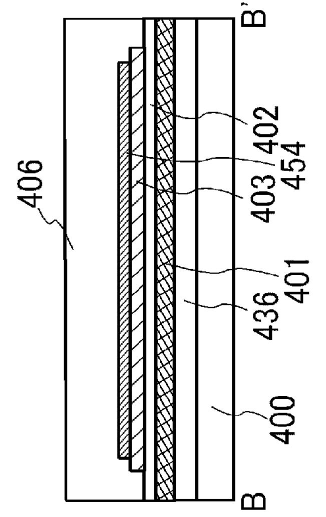


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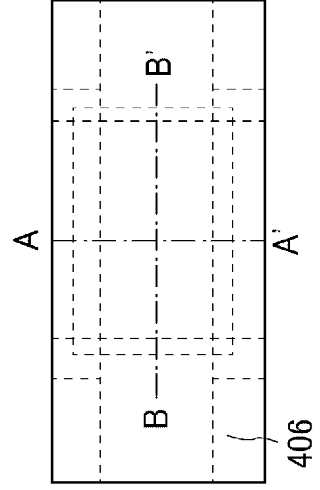

【図５】

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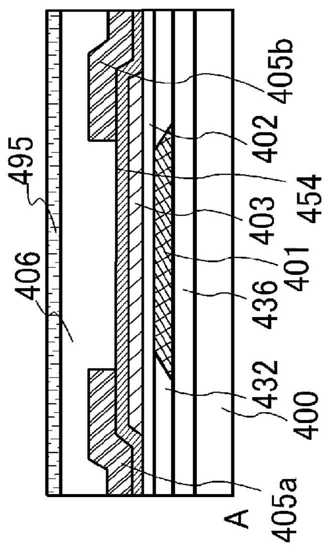


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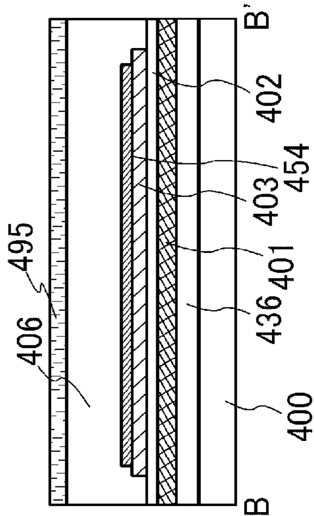


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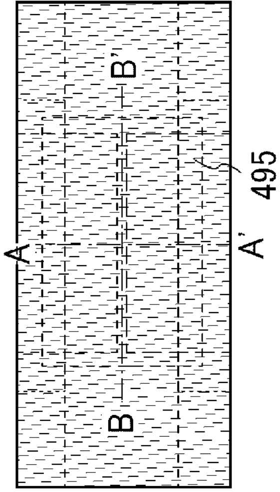


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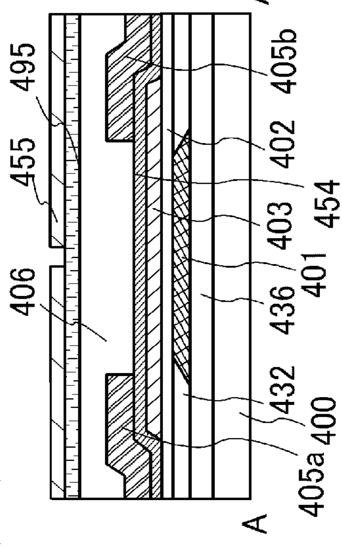


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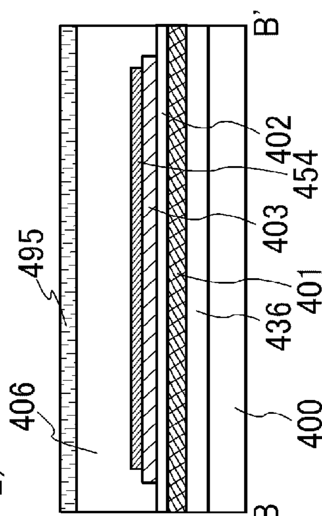


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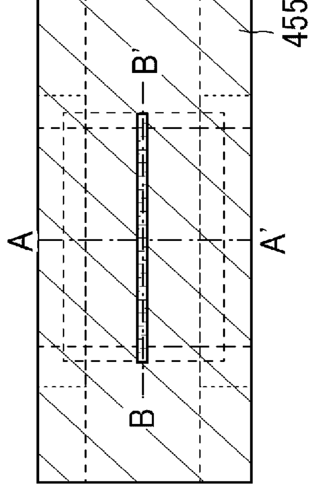


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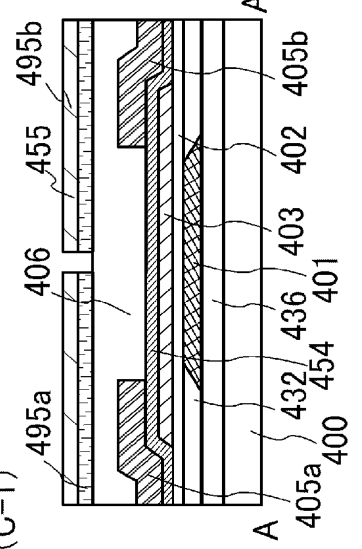


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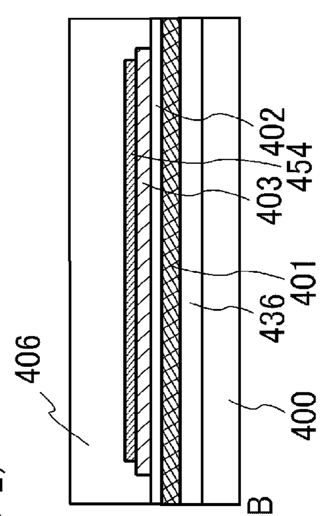


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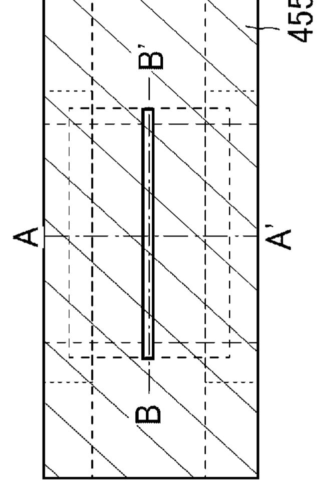

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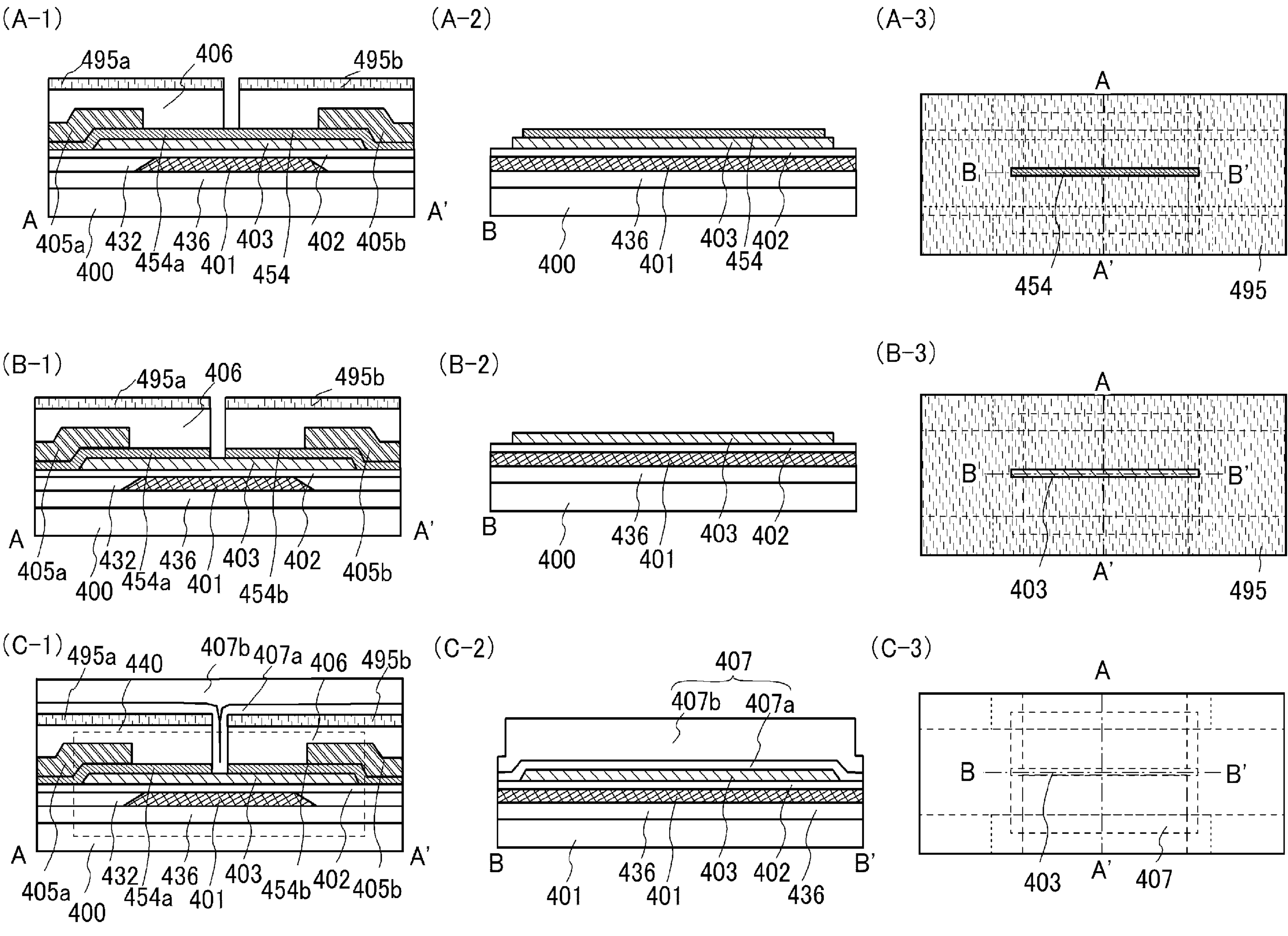
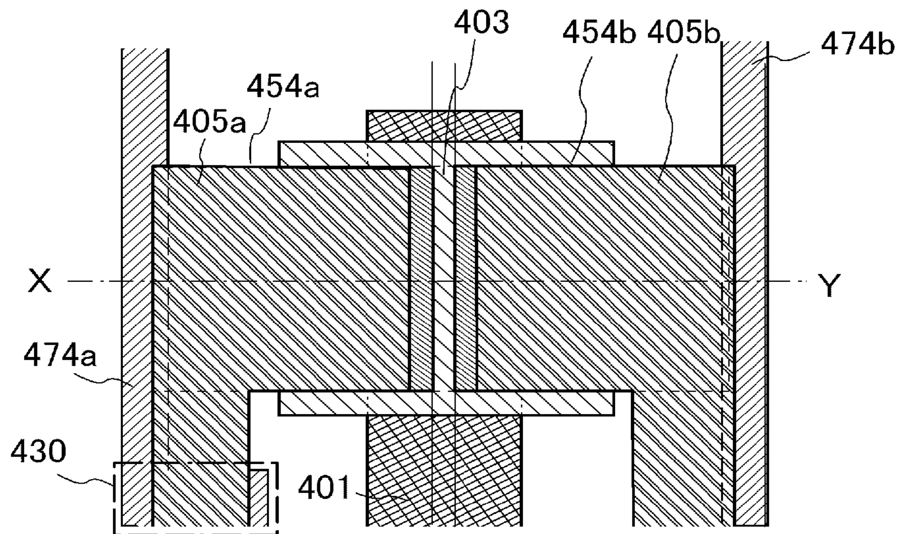


【図７】

（Ａ）

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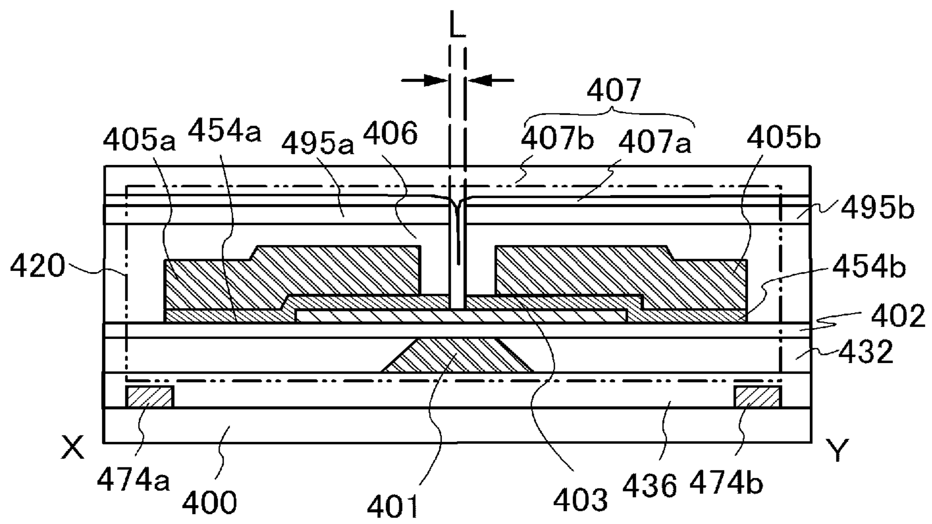


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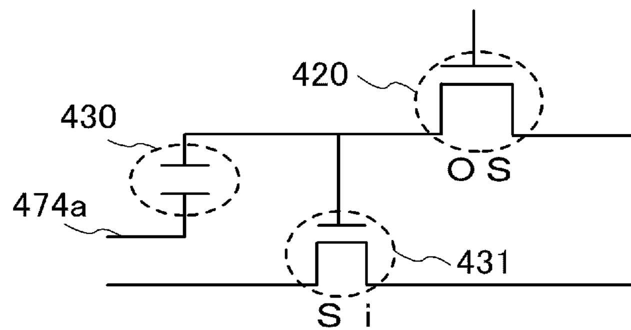

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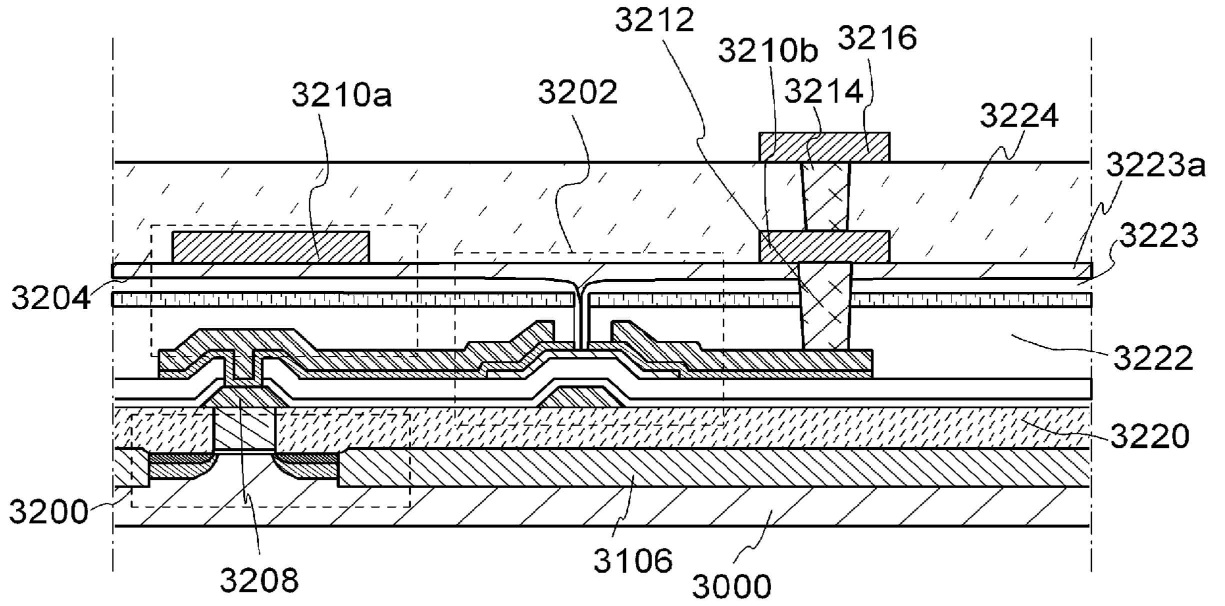


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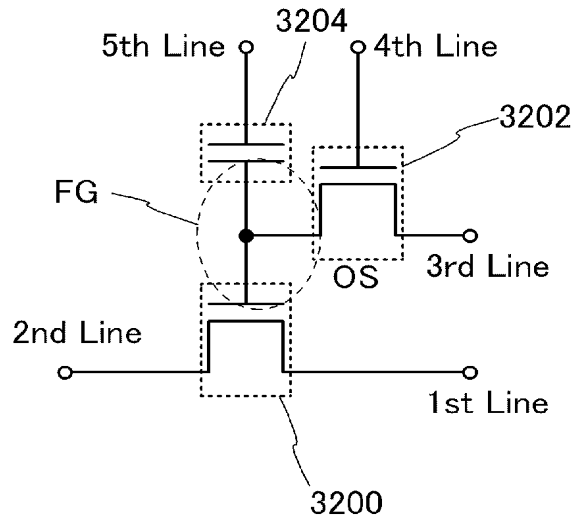

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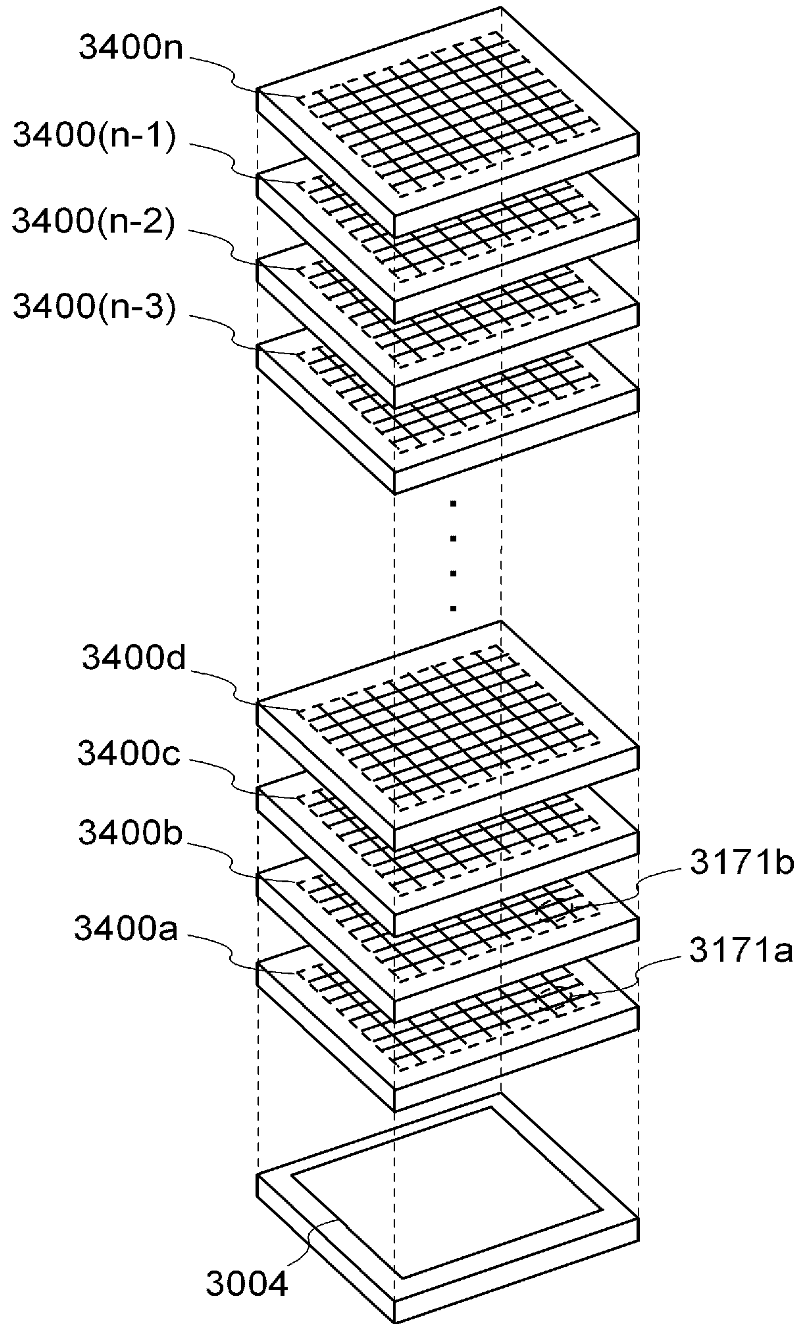

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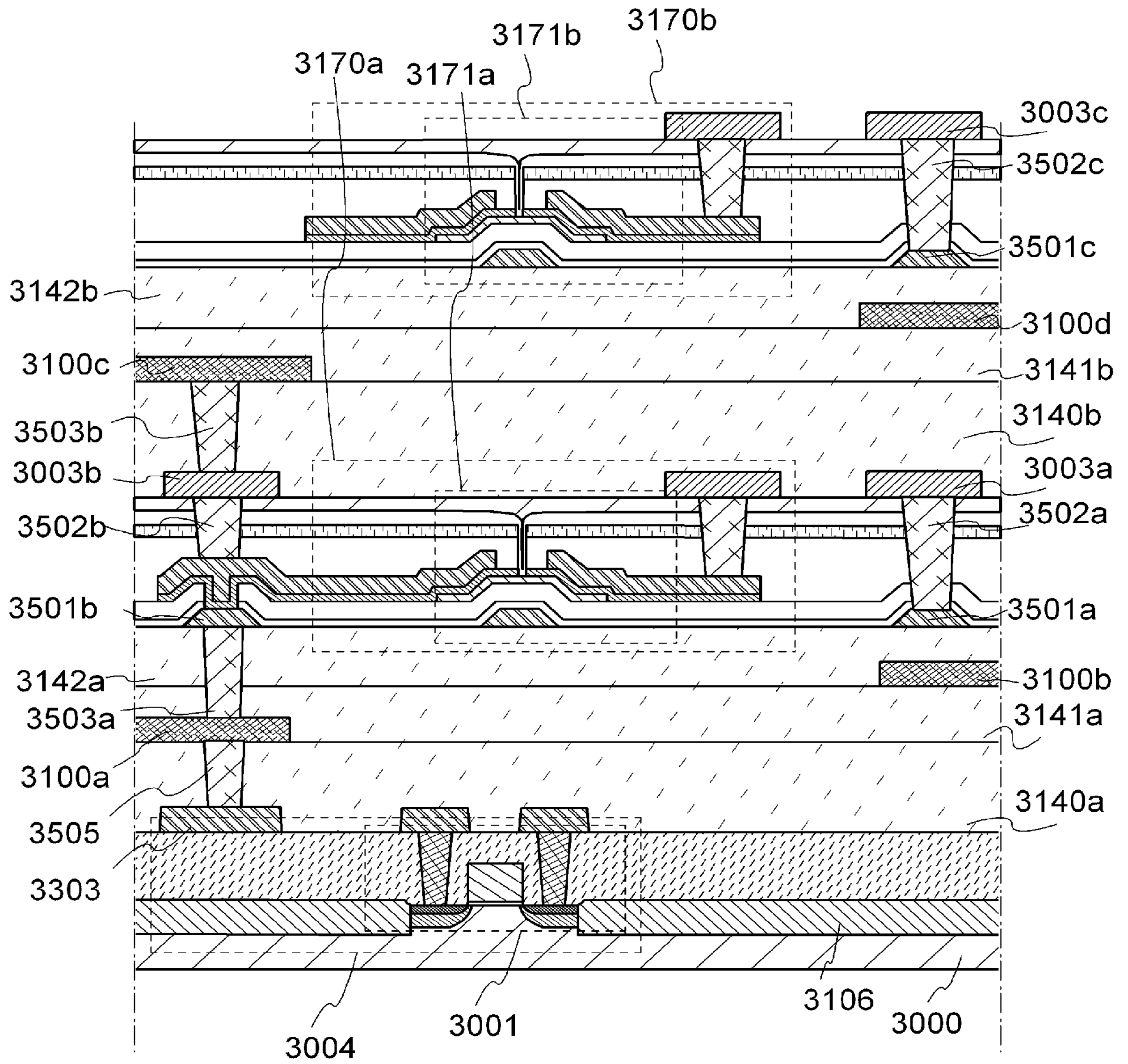
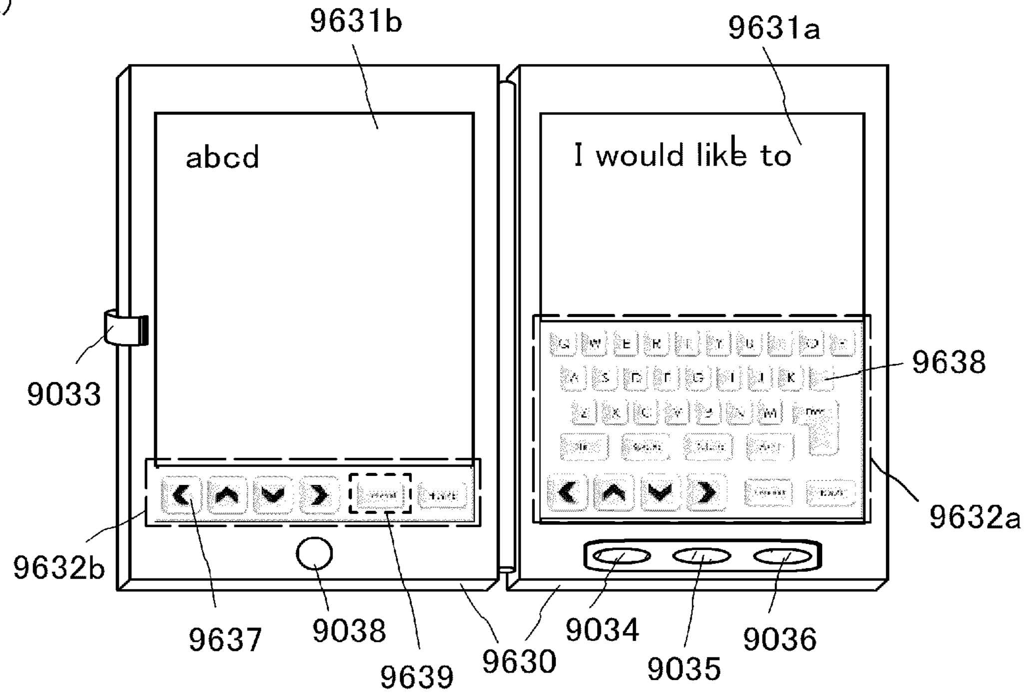


【図１２】

(A)

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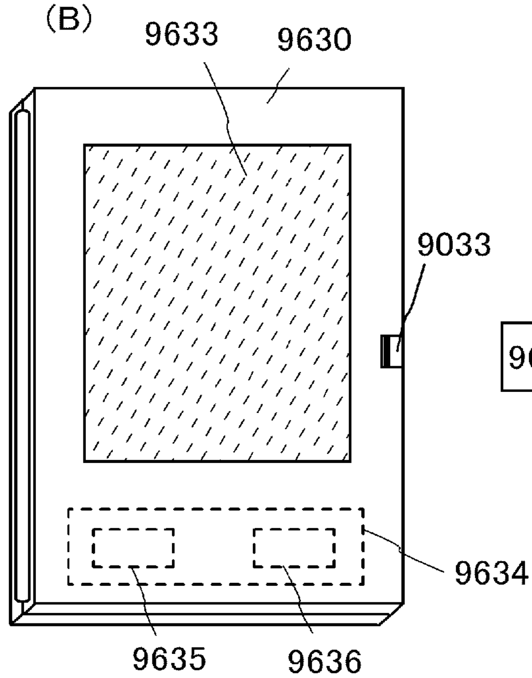
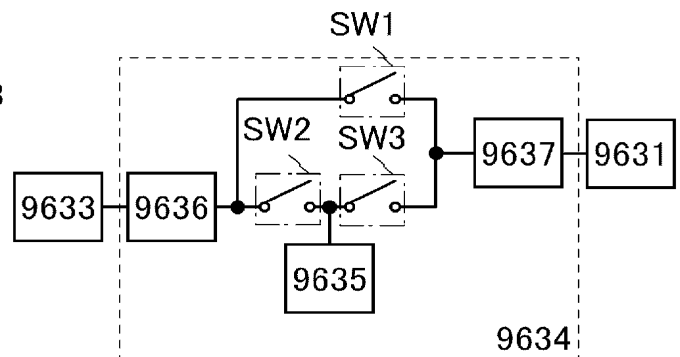



(C)



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Application Number: 特願２０１１－２８２５１１

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２０１４年　８月　５日

特許庁長官
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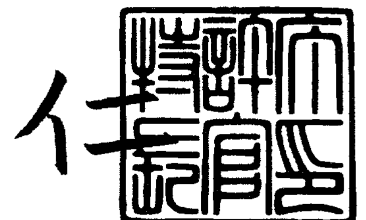

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【書類名】明細書
【発明の名称】半導体装置およびその作製方法
【技術分野】
【０００１】
本発明は、半導体装置およびその作製方法に関する。
【背景技術】
【０００２】
絶縁表面を有する基板上に半導体材料を堆積して、その半導体材料を活性層として用いるトランジスタ（以下、堆積膜トランジスタと呼ぶ）が研究されてきた。従来は、活性層としてアモルファスシリコンなどのシリコン系半導体材料が用いられてきたが、近年、活性層に酸化物半導体材料を用いるトランジスタの研究が注目を集めている。というのは、酸化物半導体材料を活性層に用いたトランジスタ（以下、酸化物半導体トランジスタと呼ぶ）は、アモルファスシリコンを用いたトランジスタに比べ、オン電流が大きく、オフ電流が小さいという特徴を有するからである。
【０００３】
また、上記のような特徴を有する酸化物半導体トランジスタを、単結晶シリコンを用いたトランジスタ等が形成されている階層とは別の階層に形成して、メモリ機能等を有する半導体装置を開発する試みがなされている（特許文献１、非特許文献１）。このような半導体装置の構成では、上の階層に作製するトランジスタは、ボトムゲート型トランジスタが好ましい。というのは、下層に形成したトランジスタを電気的につなげている配線を、上層に形成するトランジスタのゲート電極に流用できるからである。
【先行技術文献】
【特許文献】
【０００４】
【特許文献１】特開２０１１－２３８３３３号公報
【非特許文献】
【０００５】
【非特許文献１】Ｋ．　Ｋａｎｅｋｏ　ｅｔ　ａｌ．，”Ｈｉｇｈｌｙ　Ｒｅｌｉａｂｌｅ　ＢＥＯＬ－Ｔｒａｎｓｉｓｔｏｒ　ｗｉｔｈ　Ｏｘｙｇｅｎ－ｃｏｎｔｒｏｌｌｅｄ　ＩｎＧａＺｎＯ　ａｎｄ　Ｇａｔｅ／Ｄｒａｉｎ　Ｏｆｆｓｅｔ　Ｄｅｓｉｇｎ　ｆｏｒ　Ｈｉｇｈ／Ｌｏｗ　Ｖｏｌｔａｇｅ　Ｂｒｉｄｇｉｎｇ　Ｉ／Ｏ　Ｏｐｅｒａｔｉｏｎｓ”　ＩＥＤＭ２０１１，　ｐｐ１５５－１５８
【発明の概要】
【発明が解決しようとする課題】
【０００６】
上述した複数の階層に複数のトランジスタを有する半導体装置のうち、上層に形成されるボトムゲート型トランジスタは、堆積膜トランジスタが好ましい。堆積膜により容易に活性層を形成できるからであり、当該半導体装置の作製も容易になるからである。
【０００７】
ボトムゲート型トランジスタを上層に形成した、従来の複数の階層に複数のトランジスタを有する半導体装置は、作製することが容易であるが、半導体装置の性能として十分ではない。上層に形成したボトムゲート型トランジスタの電気特性が十分でないからである。たとえば、複数の階層に複数のトランジスタを有する半導体装置を用いたメモリにおいて、メモリの書き込みを行うトランジスタを、堆積膜トランジスタで構成すると、メモリの書き込み能力等が十分ではない。というのは、上層に形成されるボトムゲート型トランジスタの電気特性が十分でなく、特にオン電流がバルクシリコンを活性層に用いたトランジスタに比べ小さいためである。そのため、堆積膜トランジスタのオン電流を大きくする必要がある。その方法のひとつとして、当該ボトムゲート型トランジスタのチャネル長を短くした（たとえば３０ｎｍ程度まで）トランジスタを用いる方法がある。なお、チャネル長を３０ｎｍ未満まで微細化するには電子線を用いたフォトリソグラフィ工程が必要であ

る。
【０００８】
フォトリソグラフィ工程を用いて、一の導電層を分断してソース電極とドレイン電極を形成するボトムゲート型のトランジスタにおいて、そのチャネル長を短くするには、レジストの厚さをそのチャネル長以下とする必要がある。ところで、一の導電層のエッチング工程においてレジストの厚さは減少する。そのため、一の導電層の厚さを、当該エッチング工程でレジストが消失してしまわない程度の条件で分断できる厚さとしなければならない。
【０００９】
一方、トランジスタのソース電極とドレイン電極の電気抵抗は低い方が好ましく、その厚さはどこまでも薄くできるものではない。
【００１０】
以上のことから、ボトムゲート型のトランジスタのソース電極とドレイン電極の電気抵抗を抑制しつつ、そのチャネル長を短くすることは難しい。とくに、ボトムゲート型トランジスタにおいて、ソース電極とドレイン電極を、トランジスタ間を電気的につなげる配線に使用する場合、それらの電気抵抗を抑制する必要がある。
【００１１】
本発明は、チャネル長の短いボトムゲート型のトランジスタを提供することを課題の一とする。または、チャネル長の短いボトムゲート型のトランジスタの作製方法を提供することを課題の一とする。
【課題を解決するための手段】
【００１２】
ボトムゲート型のトランジスタのソース電極およびドレイン電極の構成に着目した。そして、ソース電極およびドレイン電極のチャネル形成領域に近接する部分の厚さが、他の部分より薄い構成に想到した。
【００１３】
また、ソース電極およびドレイン電極の上記他の部分（言い換えるとチャネル形成領域に近接する部分以外の部分）を形成した後に、チャネル形成領域に近接する部分と当該他の部分の間に生じる段差が、チャネル形成領域に近接するソース電極およびドレイン電極を形成する際に、レジストで被覆できない現象に着目した。そして、当該段差の表面を保護層で覆うことにより、チャネル形成時に段差部分の表面にダメージを与えないで、チャネル長の短いボトムゲート型のトランジスタを作製する方法に想到した。
【００１４】
すなわち、本発明に係る半導体装置の作製方法の一態様は、絶縁表面上にゲート電極層を形成する工程と、ゲート電極層の上に接するようにゲート絶縁層を形成する工程と、ゲート絶縁層の上に接してかつゲート電極層と重なるように酸化物半導体層を形成する工程と、酸化物半導体層の上に接してかつ酸化物半導体層を覆うように導電膜を形成する工程と、導電膜の上に接して低抵抗材料膜を形成する工程と、低抵抗材料膜の上に接して配線保護膜を形成する工程と、ゲート電極層を挟んで離間する第１配線保護層と第２配線保護層を形成する工程と、ゲート電極層を挟んで離間する第１配線保護層と接した第１低抵抗材料層と第２配線保護層と接した第２低抵抗材料層を形成する工程と、第１低抵抗材料層と第２低抵抗材料層の間でかつ酸化物半導体層と重なる領域に開口パターン部を有するレジストパターンを形成する工程と、レジストパターンを用いて導電膜をエッチングして第１導電層と第２導電層に分離して形成する工程と、導電膜の開口部を保護層で充填する工程と、を有する半導体装置の作製方法である。
【００１５】
以上の工程により、ソース電極層、ドレイン電極層となる導電膜の加工時に、低抵抗材料層を消失させないで、導電膜を微細なパターンに開口することができる。よって、微細なチャネル長を有するボトムゲート型のトランジスタを作製することができる。
【００１６】

本発明の半導体装置の作製方法では、ソース電極およびドレイン電極となる導電膜加工中に、低抵抗材料層の膜厚は減少せず、低抵抗材料層の表面は損傷しない。そのため、低抵抗材料層の配線抵抗が高くならない。低抵抗材料層はトランジスタとその他の半導体素子を電気的に接続する配線として用いることができる。よって、当該作製方法で作製した半導体装置で構成する集積回路は、配線抵抗が高いことにより生じる配線遅延を生じにくいので、高速動作をすることができる。

【００１７】

また、本発明の一態様は、ゲート電極層と、ゲート電極層の上に接するゲート絶縁層と、ゲート絶縁層の上に接し、かつゲート電極層と重なるように設けられた酸化物半導体層と、酸化物半導体層の上に接しゲート電極層を挟んで離間する、第１導電層と第２導電層と、第１導電層の上に接する第１低抵抗材料層と、第２導電層の上に接する第２低抵抗材料層と、第１低抵抗材料層の上に接する第１配線保護層と、第２低抵抗材料層の上に接する第２配線保護層と、保護層は、第１導電層および第１配線保護層ならびに第２導電層および第２配線保護層の上に接し、かつ酸化物半導体層と一部接するように設けられ、第１導電層と第２導電層の間隔は、第１低抵抗材料層と第２低抵抗材料層の間隔よりも狭く、第１導電層および第１低抵抗材料層はソース電極であり、第２導電層および第２低抵抗材料層はドレイン電極であることを特徴とする半導体装置である。

【００１８】

酸化物半導体層を用いたボトムゲート型トランジスタに上記構造を採用すると、チャネル長を微細にすることができるので、オン電流の大きいトランジスタを得ることが出来る。また、酸化物半導体はアモルファスシリコンより電子移動度が高いため、オン電流の大きい半導体装置を得ることができる。

【００１９】

導電層の加工後にチャネル側の配線保護層の端は、角が取れる場合がある。その角が取れない場合に比べ、保護層の被覆性を良くすることができる。保護層はパッシベーション膜として機能しており、保護層の被覆性が高まるとより外部からの水分等の浸入を防ぐことが出来る。外部から進入する水分等により電気特性に影響を受けやすい酸化物半導体を用いたトランジスタには、特に有効である。

【００２０】

また、ゲート絶縁層が、平坦である半導体装置が好ましい。

【００２１】

下地絶縁層およびゲート電極層を平坦にすると、酸化物半導体層がゲート電極層により生じる段差により、被覆されないことを防止することができる。とくに、酸化物半導体の膜厚が５ｎｍ以上３０ｎｍ以下であるときに、平坦化するメリットがある。

【００２２】

また、酸化物半導体層のチャネル長方向の幅は、ゲート電極層のチャネル長方向の幅よりも広いことを特徴とする半導体装置であることが好ましい。

【００２３】

酸化物半導体層とゲート電極層の接する面積が大きくなるので、酸化物半導体層よりも下方に設けられている絶縁層からの酸素を酸化物半導体層に供給しやすくできる。その結果、トランジスタの初期の電気特性（閾値など）および電気特性（閾値など）の信頼性を向上させることができる。

【００２４】

また、島状の酸化物半導体層の端は酸素欠陥を生じやすく、キャリアをその他の領域より発生しやすい。活性層である酸化物半導体層において、局所的にキャリアが発生するとトランジスタの電気特性（閾値など）を劣化させる。

【００２５】

仮に、酸化物半導体層のチャネル長方向の幅が、ゲート電極層のチャネル長方向の幅よりも狭い場合、すなわち、島状の酸化物半導体層の端がゲート電極層の端の内側にある場合、ゲート電極層とソース電極間に電圧を印加したとき、島状の酸化物半導体層の端に電界

が集中する。キャリアを発生しやすい島状の酸化物半導体層の端に電界が集中すると、トランジスタの電気特性（閾値など）を劣化させる。一方、本発明のように、酸化物半導体層のチャネル長方向の幅を、ゲート電極層のチャネル長方向の幅よりも広くすると、島状の酸化物半導体層の端がゲート電極層の端の外側に位置するので、ゲート電極層とソース電極間に電圧を印加したとき、酸化物半導体層の端に電界は集中しない。そのため、トランジスタの電気特性（閾値等）を劣化させにくくできる。

【発明の効果】

【００２６】

本発明により、酸化物半導体層を活性層に用いたボトムゲート型トランジスタにおいて、チャネル長の微細なボトムゲート型トランジスタを作製することができる。また、当該トランジスタを構成要素の一つとした半導体集積回路を実現できる。

【図面の簡単な説明】

【００２７】

【図１】本発明の一態様を示す断面図および平面図である。
【図２】本発明の一態様の作製方法を説明するための断面模式図である。
【図３】本発明の一態様の作製方法を説明するための断面模式図である。
【図４】本発明の一態様の作製方法を説明するための断面模式図である。
【図５】本発明の一態様の作製方法を説明するための断面模式図である。
【図６】本発明の一態様を示す断面図および平面図である。
【図７】本発明の一態様を示す回路図である。
【図８】記憶装置の例を説明するための図である。
【図９】記憶装置の例を説明するための図である。
【図１０】記憶装置の例を説明するための図である。
【図１１】電子機器の例を説明するための図である。

【発明を実施するための形態】

【００２８】

以下では、本発明の実施の形態について図面を用いて詳細に説明する。ただし、本発明は以下の説明に限定されず、その形態および詳細を様々に変更し得ることは、当業者であれば容易に理解される。また、本発明は以下に示す実施の形態の記載内容に限定して解釈されるものではない。

【００２９】

（実施の形態１）

本実施の形態では、本発明で作製することのできる半導体装置の一態様を図１（Ａ）から（Ｃ）を用いて説明する。図１（Ａ）は、トランジスタ４４０の平面図であり、図１（Ｂ）は、図１（Ａ）のＡ－Ａ’における断面図、図１（Ｃ）は、図１（Ａ）のＢ－Ｂ’における断面図である。

【００３０】

図１に示すトランジスタ４４０は、ボトムゲート型のトランジスタである。図１に示すトランジスタ４４０は、基板４００表面と、下地絶縁層４３６と、絶縁層４３２と、ゲート電極層４０１と、ゲート絶縁層４０２と、酸化物半導体層４０３と、第１導電層４５４ａおよび第２導電層４５４ｂと、第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂと、配線保護層４８５ａおよび配線保護層４８５ｂと、保護層４０６を有する。

【００３１】

下地絶縁層４３６は、基板４００表面に接するように設ける。絶縁層４３２は、下地絶縁層４３６に接している。ゲート電極層４０１は、絶縁層４３２に埋め込まれている。ゲート絶縁層４０２はゲート電極層４０１上に接するように設ける。酸化物半導体層４０３は、ゲート絶縁層４０２の上に接するように設ける。第１導電層４５４ａおよび第２導電層４５４ｂは、酸化物半導体層４０３の上に接するように設ける。第１低抵抗材料層４０５ａは、第１導電層４５４ａの上に接するように設ける。第２低抵抗材料層４０５ｂは、第２導電層４５４ｂの上に接するように設ける。配線保護層４８５ａは、第１低抵抗材料層

４０５ａの上に接するように設ける。配線保護層４８５ｂは、第２低抵抗材料層４０５ｂの上に接するように設ける。保護層４０６は、第１導電層４５４ａおよび第２導電層４５４ｂ、ならびに配線保護層４８５ａおよび配線保護層４８５ｂ、ならびに酸化物半導体層４０３と接するように設ける。

【００３２】

まず、各構成要素について説明する。

【００３３】

＜当該半導体装置の構成要素＞

（基板と下地絶縁層）

基板４００は、絶縁表面を有する基板を用いることができる。基板４００は、少なくとも、後の熱処理に耐えうる程度の耐熱性を有する基板を用いることが好ましい。基板４００としては、例えばガラス基板、セラミック基板、石英基板、サファイア基板などを用いることができる。また、シリコンや炭化シリコンなどの単結晶半導体基板、多結晶半導体基板、シリコンゲルマニウムなどの化合物半導体基板、ＳＯＩ基板などを適用することもでき、これらの基板上に半導体素子が設けられたものを、基板４００として用いてもよい。なお、基板４００中の水素または水などの不純物濃度は、低いことが好ましい。酸化物半導体層４０３に水素または水が拡散し、当該半導体装置の電気特性を劣化させないようにするためである。

【００３４】

下地絶縁層４３６としては、例えば酸化シリコン、酸化窒化シリコン、酸化アルミニウム、酸化窒化アルミニウムなどの酸化物絶縁層、窒化シリコン、窒化酸化シリコン、窒化アルミニウム、窒化酸化アルミニウムなどの窒化物絶縁層を用いることができる。

【００３５】

（ゲート電極層）

ゲート電極層４０１としては、例えばモリブデン、チタン、タングステン、アルミニウム、銅等の金属材料を用いることができる。また、ゲート電極層４０１としてリン等の不純物元素をドーピングした多結晶シリコン層に代表される半導体層、ニッケルシリサイドなどのシリサイド層を用いてもよい。また、ゲート電極層４０１を単層構造としてもよいし、積層構造としてもよい。

【００３６】

（ゲート絶縁層）

ゲート絶縁層４０２は、酸化シリコン、酸窒化シリコン、窒化シリコン等を用いることができる。ゲート絶縁層４０２は、化学量論比を満たす酸素よりも多くの酸素を含む酸化シリコン層が好ましい。

【００３７】

（ソース電極層およびドレイン電極層）

ソース電極層とドレイン電極層は、導電膜４５４と低抵抗材料膜４０５で構成する。第１導電層４５４ａは、タングステン、モリブデン等の金属を用いることができる。特にタングステンが好ましい。第１保護層４０６とエッチングレートの比を高くすることができるからである。第１低抵抗材料層４０５ａは、アルミニウムとチタンの積層構造、または銅などを用いることができる。アルミニウムとチタンの積層構造は、チタン／アルミニウム／チタンを用いてもよい。第１低抵抗材料層４０５ａに銅を用いる場合、銅が隣接する酸化物半導体層４０３に拡散しないように窒化チタン等を設けることが好ましい。

【００３８】

（酸化物半導体層）

次に、本実施の形態に用いることができる酸化物半導体層４０３について説明する。酸化物半導体層４０３は、少なくとも禁制帯幅がシリコンの１．１ｅＶよりも大きい半導体を用いることが出来る。たとえば、酸化物半導体を用いることができる。

【００３９】

酸化物半導体層４０３の膜厚は、５ｎｍ以上１００ｎｍ以下とし、好ましくは５ｎｍ以上

３０ｎｍ以下とする。というのは、ショートチャネル効果を抑えながら、トランジスタのチャネル長を微細化するためである。

【００４０】

酸化物半導体層４０３には酸化物半導体が好ましい。酸化物半導体として用いることのできる材料は、少なくともインジウム（Ｉｎ）を含む。特にＩｎと亜鉛（Ｚｎ）を含むことが好ましい。また、当該酸化物半導体を用いたトランジスタの電気特性のばらつきを減らすためのスタビライザーとして、それらに加えてガリウム（Ｇａ）を有することが好ましい。また、スタビライザーとしてスズ（Ｓｎ）を有することが好ましい。また、スタビライザーとしてハフニウム（Ｈｆ）を有することが好ましい。また、スタビライザーとしてアルミニウム（Ａｌ）を有することが好ましい。また、スタビライザーとしてジルコニウム（Ｚｒ）を有することが好ましい。

【００４１】

また、他のスタビライザーとして、ランタノイドである、ランタン（Ｌａ）、セリウム（Ｃｅ）、プラセオジム（Ｐｒ）、ネオジム（Ｎｄ）、サマリウム（Ｓｍ）、ユウロピウム（Ｅｕ）、ガドリニウム（Ｇｄ）、テルビウム（Ｔｂ）、ジスプロシウム（Ｄｙ）、ホルミウム（Ｈｏ）、エルビウム（Ｅｒ）、ツリウム（Ｔｍ）、イッテルビウム（Ｙｂ）、ルテチウム（Ｌｕ）のいずれか一種あるいは複数種を有してもよい。

【００４２】

また、酸化物半導体として、酸化インジウム、酸化スズ、酸化亜鉛、２元系金属の酸化物であるＩｎ－Ｚｎ系酸化物、Ｉｎ－Ｍｇ系酸化物、Ｉｎ－Ｇａ系酸化物、３元系金属の酸化物であるＩｎ－Ｇａ－Ｚｎ系酸化物（ＩＧＺＯとも表記する）、Ｉｎ－Ａｌ－Ｚｎ系酸化物、Ｉｎ－Ｓｎ－Ｚｎ系酸化物、Ｉｎ－Ｈｆ－Ｚｎ系酸化物、Ｉｎ－Ｌａ－Ｚｎ系酸化物、Ｉｎ－Ｃｅ－Ｚｎ系酸化物、Ｉｎ－Ｐｒ－Ｚｎ系酸化物、Ｉｎ－Ｎｄ－Ｚｎ系酸化物、Ｉｎ－Ｓｍ－Ｚｎ系酸化物、Ｉｎ－Ｅｕ－Ｚｎ系酸化物、Ｉｎ－Ｇｄ－Ｚｎ系酸化物、Ｉｎ－Ｔｂ－Ｚｎ系酸化物、Ｉｎ－Ｄｙ－Ｚｎ系酸化物、Ｉｎ－Ｈｏ－Ｚｎ系酸化物、Ｉｎ－Ｅｒ－Ｚｎ系酸化物、Ｉｎ－Ｔｍ－Ｚｎ系酸化物、Ｉｎ－Ｙｂ－Ｚｎ系酸化物、Ｉｎ－Ｌｕ－Ｚｎ系酸化物、４元系金属の酸化物であるＩｎ－Ｓｎ－Ｇａ－Ｚｎ系酸化物、Ｉｎ－Ｈｆ－Ｇａ－Ｚｎ系酸化物、Ｉｎ－Ａｌ－Ｇａ－Ｚｎ系酸化物、Ｉｎ－Ｓｎ－Ａｌ－Ｚｎ系酸化物、Ｉｎ－Ｓｎ－Ｈｆ－Ｚｎ系酸化物、Ｉｎ－Ｈｆ－Ａｌ－Ｚｎ系酸化物を用いることができる。

【００４３】

なお、ここで、例えば、Ｉｎ－Ｇａ－Ｚｎ系酸化物とは、ＩｎとＧａとＺｎを主成分として有する酸化物という意味であり、ＩｎとＧａとＺｎの比率は問わない。また、ＩｎとＧａとＺｎ以外の金属元素が入っていてもよい。

【００４４】

また、酸化物半導体として、$InMO_3$（ＺｎＯ）ｍ（ｍ＞０、且つ、ｍは整数でない）で表記される材料を用いてもよい。なお、Ｍは、Ｇａ、Ｆｅ、ＭｎおよびＣｏから選ばれた一の金属元素または複数の金属元素を示す。また、酸化物半導体として、$In_2SnO_5$（ＺｎＯ）ｎ（ｎ＞０、且つ、ｎは整数）で表記される材料を用いてもよい。

【００４５】

また、酸化物半導体として、Ｉｎ：Ｇａ：Ｚｎ＝１：１：１（＝１／３：１／３：１／３）、Ｉｎ：Ｇａ：Ｚｎ＝２：２：１（＝２／５：２／５：１／５）、あるいはＩｎ：Ｇａ：Ｚｎ＝３：１：２（＝１／２：１／６：１／３）の原子数比のＩｎ－Ｇａ－Ｚｎ系酸化物やその組成の近傍の酸化物を用いることができる。あるいは、Ｉｎ：Ｓｎ：Ｚｎ＝１：１：１（＝１／３：１／３：１／３）、Ｉｎ：Ｓｎ：Ｚｎ＝２：１：３（＝１／３：１／６：１／２）あるいはＩｎ：Ｓｎ：Ｚｎ＝２：１：５（＝１／４：１／８：５／８）の原子数比のＩｎ－Ｓｎ－Ｚｎ系酸化物やその組成の近傍の酸化物を用いるとよい。

【００４６】

しかし、インジウムを含む酸化物半導体は、これらに限られず、必要とする半導体特性（移動度、しきい値、ばらつき等）に応じて適切な組成のものを用いればよい。また、必要

とする半導体特性を得るために、キャリア濃度や不純物濃度、欠陥密度、金属元素と酸素の原子数比、原子間結合距離、密度等を適切なものとすることが好ましい。

【００４７】

例えば、Ｉｎ－Ｓｎ－Ｚｎ系酸化物では比較的容易に高い移動度が得られる。しかしながら、Ｉｎ－Ｇａ－Ｚｎ系酸化物でも、バルク内欠陥密度を低くすることにより移動度を上げることができる。

【００４８】

また、酸化物半導体層４０３は、単結晶、多結晶（ポリクリスタルともいう。）または非晶質などの状態をとる。

【００４９】

また、酸化物半導体層４０３に、銅、アルミニウム、塩素などの不純物がほとんど含まれない高純度化されたものであることが望ましい。トランジスタの製造工程において、これらの不純物が混入または酸化物半導体層４０３の表面に付着する恐れのない工程を適宜選択することが好ましく、酸化物半導体層４０３に付着した場合には、シュウ酸や希フッ酸などに曝す、またはプラズマ処理（$N_2O$プラズマ処理など）を行うことにより、酸化物半導体層４０３の不純物を除去することが好ましい。酸化物半導体層４０３に酸化物半導体を用いた場合、具体的には、酸化物半導体中の銅濃度は$1 \times 10^{18}$ ａｔｏｍｓ／ｃｍ$^3$以下、好ましくは$1 \times 10^{17}$ ａｔｏｍｓ／ｃｍ$^3$以下とする。また、酸化物半導体中のアルミニウム濃度は$1 \times 10^{18}$ ａｔｏｍｓ／ｃｍ$^3$以下とする。また、酸化物半導体中の塩素濃度は$2 \times 10^{18}$ ａｔｏｍｓ／ｃｍ$^3$以下とする。

【００５０】

また、酸化物半導体層４０３に酸化物半導体を用いた場合、酸化物半導体は成膜直後において、化学量論的組成より酸素が多い過飽和の状態とすることが好ましい。例えば、スパッタリング法を用いて酸化物半導体を成膜する場合、成膜ガスの酸素の占める割合が多い条件で成膜することが好ましく、特に酸素雰囲気（酸素ガス１００％）で成膜を行うことが好ましい。成膜ガスの酸素の占める割合が多い条件、特に酸素ガス１００％の雰囲気で成膜すると、例えば成膜温度を３００℃以上としても、膜中からのＺｎの放出が抑えられる。

【００５１】

酸化物半導体層４０３は、水素などの不純物が十分に除去され、その酸化物半導体に十分な酸素が供給されて酸素が過飽和の状態となっていることが望ましい。具体的には、酸化物半導体の水素濃度は$5 \times 10^{19}$ ａｔｏｍｓ／ｃｍ$^3$以下、望ましくは$5 \times 10^{18}$ ａｔｏｍｓ／ｃｍ$^3$以下、より望ましくは$5 \times 10^{17}$ ａｔｏｍｓ／ｃｍ$^3$以下とする。なお、上述の酸化物半導体の水素濃度は、二次イオン質量分析法（ＳＩＭＳ：Ｓｅｃｏｎｄａｒｙ　Ｉｏｎ　Ｍａｓｓ　Ｓｐｅｃｔｒｏｓｃｏｐｙ）で測定されるものである。

【００５２】

（配線保護層）

配線保護膜４８５は、導電膜４５４をエッチングする条件でエッチングされにくい膜であることが好ましい。というのは、第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂは、トランジスタ同士を連結する引き回し配線として使用するため、低抵抗材料膜４０５の膜厚は、１００ｎｍ以上の膜厚がある。よって、低抵抗材料膜４０５の表面と、導電膜４５４の表面との高さの差は、少なくとも１００ｎｍ以上になる。仮に配線保護膜４８５を設けない場合、低抵抗材料膜４０５の端はレジストが被覆されないか、または被覆されていてもレジストの膜厚は薄くなる。そのため、導電膜４５４の加工で低抵抗材料膜４０５はエッチングダメージを受ける。そのダメージを防止するため、導電膜４５４をエッチングする条件でエッチングされにくい配線保護膜４８５を低抵抗材料膜４０５の上に設け、低抵抗材料膜４０５がエッチングされないようにするためである。配線保護膜４８５には、酸化シリコン、窒化シリコン、酸窒化シリコン、酸化アルミニウムを用いることが好ましい。酸化シリコン、窒化シリコン、酸窒化シリコンは、ＰＣＶＤ法または、スパッタリング法で成膜することができる。酸化アルミニウムは、スパッタリング法で成膜す

ることができる。
【００５３】
（保護層）
保護層４０６は、酸化物半導体層４０３を、外部から浸入する水分等から守る役割を有する。第１保護層４０６は、酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウムを用いることできる。第１保護層４０６は、膜中に酸素を多く含ませた酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウムを用いることが好ましい。また、多くの過剰酸素を上記保護層に含ませたい場合には、イオン注入法やイオンドーピング法やプラズマ処理によって、上記保護層に酸素を適宜添加すればよい。
【００５４】
<半導体装置の作製方法>
本発明の一態様である半導体装置の作製方法について、図２から図５を用いて説明する。
【００５５】
図２にゲート電極層４０１の形成工程から、酸化物半導体層４０３への酸素ドーピング工程までを示す。
【００５６】
まず、基板４００を準備し、基板４００の上に下地絶縁層４３６を形成し、下地絶縁層４３６の上にゲート電極層４０１を形成する（図２（Ａ－１）から（Ａ－３））。
【００５７】
ゲート電極層４０１は、ゲート電極として使用できる材料をたとえばスパッタリング成膜し、一部を選択的にエッチングして形成する。なお、エッチングは、ドライエッチングでもウェットエッチングでもよく、両方を用いてもよい。また、ゲート電極層４０１形成後に、基板４００、およびゲート電極層４０１に熱処理を行ってもよい。
【００５８】
次に、下地絶縁層４３６およびゲート電極層４０１の上に絶縁層４３２を形成する。絶縁層４３２を平坦化して、ゲート電極層４０１を露出させ、絶縁層４３２およびゲート電極層４０１を平坦にすることが好ましい。（図２（Ｂ－１）から（Ｂ－３）参照）。平坦化処理としては、化学的機械研磨（Ｃｈｅｍｉｃａｌ　Ｍｅｃｈａｎｉｃａｌ　Ｐｏｌｉｓｈｉｎｇ：ＣＭＰ）処理などを行えばよい。
【００５９】
後述する酸化物半導体層４０３が、ゲート電極層４０１により生じる段差により、被覆されないことを防止することができるため、絶縁層４３２およびゲート電極層４０１を平坦化することが好ましい。
【００６０】
次に、ゲート電極層４０１上にゲート絶縁層４０２を形成し、ゲート絶縁層４０２上に酸化物半導体層４０３を形成する（図２（Ｃ－１）から（Ｃ－３）参照）。
【００６１】
例えば、ＰＣＶＤ法を用いてゲート絶縁層４０２に適用可能な材料の膜を成膜してゲート絶縁層４０２を形成できる。
【００６２】
なお、酸化物半導体層４０３を形成する前に熱処理を行い、ゲート絶縁層４０２の脱水化または脱水素化を行ってもよい。例えば３５０℃以上４５０℃以下の熱処理を行ってもよい。
【００６３】
また、脱水化または脱水素化されたゲート絶縁層４０２に、酸素を供給してもよい。酸素は、ゲート絶縁層４０２中、またはゲート絶縁層４０２中および該界面近傍に含有させてもよい。酸素の供給は酸素ドープ処理等により行うことができる。脱水化または脱水素化した後にゲート絶縁層４０２に酸素を供給することにより、酸素の放出を抑制でき、ゲート絶縁層４０２の酸素濃度を高くできる。
【００６４】

なお、ゲート絶縁層４０２から酸化物半導体への酸素の供給のための熱処理を、酸化物半導体が島状に加工される前に行うと、ゲート絶縁層４０２に含まれる酸素が熱処理によって放出されるのを防止することができるため好ましい。
【００６５】
例えば、３５０℃以上基板の歪み点未満の温度、好ましくは、３５０℃以上４５０℃以下で熱処理を行う。さらに、その後の工程において熱処理を行ってもよい。このとき、上記熱処理を行う熱処理装置としては、例えば電気炉、または抵抗発熱体などの発熱体からの熱伝導または熱輻射により被処理物を加熱する装置を用いることができ、例えばＧＲＴＡ（Ｇａｓ　Ｒａｐｉｄ　Ｔｈｅｒｍａｌ　Ａｎｎｅａｌｉｎｇ）装置またはＬＲＴＡ（Ｌａｍｐ　Ｒａｐｉｄ　Ｔｈｅｒｍａｌ　Ａｎｎｅａｌｉｎｇ）装置などのＲＴＡ（Ｒａｐｉｄ　Ｔｈｅｒｍａｌ　Ａｎｎｅａｌｉｎｇ）装置を用いることができる。
【００６６】
また、上記熱処理を行った後、その加熱温度を維持しながらまたはその加熱温度から降温する過程で該熱処理を行った炉と同じ炉に高純度の酸素ガス、高純度の$N_2O$ガス、または超乾燥エア（露点が－４０℃以下、好ましくは－４０℃以下の雰囲気）を導入してもよい。このとき、酸素ガスまたは$N_2O$ガスは、水、水素などを含まないことが好ましい。また、熱処理装置に導入する酸素ガスまたは$N_2O$ガスの純度を、６Ｎ以上、好ましくは７Ｎ以上、すなわち、酸素ガスまたは$N_2O$ガス中の不純物濃度を１ｐｐｍ以下、好ましくは０．１ｐｐｍ以下とすることが好ましい。酸素ガスまたは$N_2O$ガスの作用により、酸化物半導体に酸素が供給され、酸化物半導体中の酸素欠乏に起因する欠陥を低減できる。なお、上記高純度の酸素ガス、高純度の$N_2O$ガス、または超乾燥エアの導入は、上記熱処理時に行ってもよい。
【００６７】
さらに、酸化物半導体に酸素ドーピング４５１を行う（図２（Ｃ－１）から（Ｃ－３）参照）。酸化物半導体へ酸素を供給することにより、酸化物半導体中の酸素欠損を補填するためである。酸素欠損を補填することにより、当該半導体装置は、初期の電気特性（閾値電圧など）に異常値が生じにくくなり、電気特性（閾値電圧など）の信頼性も向上する。
【００６８】
酸素ドーピング４５１は、イオン注入法、イオンドーピング法、プラズマイマージョンイオンインプランテーション法、プラズマ処理などを用いることができる。これら方法により、酸素（酸素ラジカル、酸素原子、酸素分子、オゾン、酸素イオン（酸素分子イオン）および／または酸素クラスタイオン）を酸化物半導体にドープすることができる。
【００６９】
図３に酸化物半導体層４０３を島状に形成する工程から、低抵抗材料膜４０５および配線保護膜４８５を形成するためのレジスト４５３の形成工程までを示す。
【００７０】
酸化物半導体層４０３をフォトリソグラフィ工程により加工して、島状の酸化物半導体層４０３を形成する（図３（Ａ－１）から（Ａ－３）参照）。
【００７１】
酸化物半導体層４０３のエッチングは、ドライエッチングでもウェットエッチングでもよく、両方を用いてもよい。
【００７２】
なお、酸化物半導体層のチャネル長方向の幅は、ゲート電極層のチャネル長方向の幅よりも広いことが好ましい。酸化物半導体層とゲート電極層の接する面積が大きくなるので、酸化物半導体層よりも下方に設けられている絶縁層からの酸素を酸化物半導体層に供給しやすくできる。その結果、トランジスタの初期の電気特性（閾値など）および電気特性（閾値など）の信頼性を向上させることができるからである。
【００７３】
次に、導電膜４５４を、酸化物半導体層４０３に接するように形成する。導電膜４５４は、スパッタリング法などを用いて形成すればよい。次に、低抵抗材料膜４０５を、導電膜

４５４に接するように形成する。低抵抗材料膜４０５は、スパッタリング法などを用いて形成すればよい。次に、配線保護膜４８５を、低抵抗材料膜４０５に接するように形成する。配線保護膜４８５は、スパッタリング法などを用いて形成すればよい。（図３（Ｂ－１）から（Ｂ－３）参照）。

【００７４】

次に、フォトリソグラフィ工程によりレジスト４５３を形成する（図３（Ｃ－１）から（Ｃ－３）参照）。

【００７５】

図４に、配線保護膜４８５と低抵抗材料膜４０５の形成工程から、第１導電層４５４ａおよび第２導電層４５４ｂを形成するためのレジスト４５５の形成工程までを示す。

【００７６】

レジスト４５３をマスクとして、配線保護膜４８５および低抵抗材料膜４０５を選択的にエッチングし、第１配線保護層４８５ａおよび第２配線保護層４８５ｂならびに第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂを形成する（図４（Ａ－１）から（Ａ－３）参照）。配線保護膜４８５と低抵抗材料膜４０５の加工は、同じレジストパターンを用いて行ってもよいし、配線保護膜４８５の加工と低抵抗材料膜４０５の加工とで、それぞれレジストパターンを形成して、加工を行っても良い。配線保護膜４８５低抵抗材料膜４０５をエッチングする条件は、導電膜４５４がエッチングされにくい条件で行うことが好ましい。

【００７７】

次に、酸化物半導体層４０３と接していない領域の導電膜４５４をエッチングする（図４（Ｂ－１）から（Ｂ－３）参照）。

【００７８】

次に、導電膜４５４および配線保護膜４８５の上にレジストを形成する。このときのレジストの膜厚は、作製するパターンの幅と１：１～１：２の関係になることが好ましい。例えば、パターンの幅が３０ｎｍの場合には、レジストの厚さを３０ｎｍから６０ｎｍとする。該レジストに対して電子ビームを用いた露光を行い、レジスト４５５を形成する。（図４（Ｃ－１）から（Ｃ－３）参照）。第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂは、トランジスタ同士を連結する引き回し配線として使用するため、低抵抗材料膜４０５の膜厚は、１００ｎｍ以上の膜厚がある。低抵抗材料膜４０５の表面と、導電膜４５４の表面との高さの差は、少なくとも１００ｎｍ以上になる。仮に配線保護膜４８５を設けない場合、第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂの端はレジストが被覆されないか、または被覆されていてもレジストの膜厚は薄い。そのため、導電膜４５４の加工で低抵抗材料膜４０５はエッチングダメージを受ける。そのダメージを防止するため、導電膜４５４をエッチングする条件でエッチングされにくい配線保護膜４８５を低抵抗材料膜４０５の上に設け、低抵抗材料膜４０５がエッチングされないようにする。

【００７９】

第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂはトランジスタ同士を連結する引き回し配線として使用することができる。引き回し配線の配線抵抗が高いと集積回路において配線遅延の問題が生じるので、配線抵抗を下げる必要がある。そのため、一般的に低抵抗材料膜４０５の膜厚は１００ｎｍ以上の膜厚が必要となる。よって、低抵抗材料膜４０５の表面と導電膜４５４の表面との高さの差は、少なくとも１００ｎｍ以上になる。配線保護膜４８５を低抵抗材料膜４０５の上に設けない場合、第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂの端はレジストが被覆されないか、または被覆されていてもレジストの膜厚は薄くなる。そのため、導電膜４５４の加工において、第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂがエッチングされてしまう。しかし、本発明の作製方法は、導電膜４５４をエッチングする条件でエッチングされにくい配線保護膜４８５を第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂの上に接するように設けるので、導電膜加工中に低抵抗材料層の膜厚が減少せず、低抵抗材料層の表面は損

傷を受けないため、配線抵抗が高くならない。よって、当該作製方法で作製した半導体装置で構成する集積回路は、配線遅延を生じにくくすることができる。
【００８０】
図５に導電膜４５４の形成から、保護層４０６の形成工程までを示す。
【００８１】
図４Ｃで形成したレジスト４５５をマスクとして、導電膜４５４のエッチングを行い、第１導電層４５４ａと第２導電層４５４ｂを形成する。第１導電層４５４ａと第２導電層４５４ｂの間はチャネルが形成される領域になる（図５（Ａ－１）から（Ａ－３）参照）。
【００８２】
導電膜４５４をエッチングする条件は、導電膜４５４のエッチングレートと酸化物半導体層４０３のエッチングレートの比が大きい条件であることが好ましい。というのは、酸化物半導体層４０３の表面にエッチングダメージを与えないためである。
【００８３】
３０ｎｍ前後の幅の開口を行う場合、レジスト４５５の膜厚は３０ｎｍから６０ｎｍと薄く、たとえば、第１配線保護層４８５ａおよび第２配線保護層４８５ｂの端で、レジストが、被覆されていない領域も生じうる。そのため、導電膜４５４とのエッチングを行っている途中にレジスト４５５が消失する領域、または、レジストが被覆されずエッチングされる領域もある。しかし、レジストが被覆されにくい領域、たとえば、第１配線保護層４８５ａおよび第２配線保護層４８５ｂの端は、第１配線保護層４８５ａおよび第２配線保護層ｂが低抵抗材料層を保護するので、レジスト４５５が消失しても、第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂがエッチングされることはない。
【００８４】
次に、上記の工程で開口した導電膜４５４の開口部を、保護層４０６で覆う（図５（Ｂ－１）から（Ｂ－３）参照）。保護層４０６は、酸化物半導体層４０３に、水分、水素等の浸入を防止する膜が好ましい。たとえば、酸化シリコン膜、酸窒化シリコン膜、窒化シリコン膜、酸化アルミニウム等を用いることができる。
【００８５】
また、保護層４０６は、酸素を過剰に含む膜であることが好ましい。たとえば、膜中に酸素を多く含ませた酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウムを用いることが好ましい。また、保護層４０６は、２層で構成しても良い。酸化物半導体に接して設ける第１の層は、成膜条件を適宜設定して膜中に酸素を多く含ませたガリウム（Ｇａ）を有する酸化物半導体、酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウムを用いることできる。第２の層は、膜中に酸素を多く含ませた酸化シリコン膜、酸化窒化シリコン膜、酸化アルミニウムを用いることできる。また、多くの過剰酸素を上記保護層に含ませたい場合には、イオン注入法やイオンドーピング法やプラズマ処理によって、上記保護層４０６に酸素を適宜添加すればよい。
【００８６】
さらに、保護層４０６を成膜した後に熱処理を行ってもよい。例えば、窒素雰囲気下２５０℃で１時間熱処理を行う。
【００８７】
以上により、トランジスタ４４０が作製できる。このとき、作製されるトランジスタ４４０のチャネル長Ｌは、３０ｎｍ未満と短い。そのため、トランジスタ４４０はオン電流の大きいトランジスタとすることができる。
【００８８】
以上が本実施の一態様である半導体装置の作製方法である。
【００８９】
本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。
【００９０】
酸化物半導体層４０３を活性層に用いたボトムゲート型トランジスタにおいて、チャネル

長が３０ｎｍ未満であるトランジスタを作製することができる。チャネル長を３０ｎｍ未満にすると、当該トランジスタのオン電流を大きくすることができる。
【００９１】
（実施の形態２）
本実施の形態では、半導体装置の一態様を図６（Ａ）および図６（Ｂ）を用いて説明する。図６（Ｂ）は、トランジスタ４２０の平面図であり、図６（Ａ）は、図６（Ｂ）のＸ－Ｙにおける断面図である。
【００９２】
図６（Ａ）および図６（Ｂ）に示すトランジスタ４２０は、基板４００表面と、下地絶縁層４３６と、絶縁層４３２と、ゲート電極層４０１と、ゲート絶縁層４０２と、酸化物半導体層４０３と、第１導電層４５４ａおよび第２導電層４５４ｂと、第１低抵抗材料層４０５ａおよび第２低抵抗材料層４０５ｂと、第１配線保護層４８５ａおよび第２配線保護層４８５ｂと、保護層４０６を有する。
【００９３】
下地絶縁層４３６は、基板４００表面に接するように設ける。絶縁層４３２は、下地絶縁層４３６に接している。ゲート電極層４０１は、絶縁層４３２に埋め込まれている。ゲート絶縁層４０２はゲート電極層４０１上に接するように設ける。酸化物半導体層４０３は、ゲート絶縁層４０２の上に接するように設ける。第１導電層４５４ａおよび第２導電層４５４ｂは、酸化物半導体層４０３の上に接するように設ける。第１低抵抗材料層４０５ａは、第１導電層４５４ａの上に接するように設ける。第２低抵抗材料層４０５ｂは、第２導電層４５４ｂの上に接するように設ける。配線保護層４８５ａは、第１低抵抗材料層４０５ａの上に接するように設ける。配線保護層４８５ｂは、第２低抵抗材料層４０５ｂの上に接するように設ける。保護層４０６は、第１導電層４５４ａおよび第２導電層４５４ｂ、ならびに配線保護層４８５ａおよび配線保護層４８５ｂ、ならびに酸化物半導体層４０３と接するように設ける。
【００９４】
本実施例で示す半導体装置の構成、作製方法は、実施の形態１を参酌することができる。
【００９５】
（基板４００に設けることができる回路について）
基板４００には半導体素子が設けられているが、ここでは簡略化のため省略している。また、基板４００上には、配線層４７４ａ、４７４ｂと、配線層４７４ａ、４７４ｂを覆う下地絶縁層４３６が設けられており、その一部が図６に示すメモリ構成の一つとなっている。図７にトランジスタ４２０と基板４００に設けられているトランジスタ４３１との接続を示す等価回路の一例を示す。
【００９６】
また、容量４３０は、積層からなるドレイン電極層と、配線層４７４ａとを一対の電極とし、下地絶縁層４３６および積層からなるゲート絶縁層４０２を誘電体とする容量である。
【００９７】
図７に示すメモリ構成において、メモリの書き込みは容量４３０に電荷を注入することにより行われる。本実施の形態で示すトランジスタは、チャネル長が３０ｎｍ未満と短いので、オン電流が大きい。そのためメモリの書き込みを早くすることができる。
【００９８】
図７に示すメモリ構成は、電力が供給されない状況でも記憶内容の保持が可能で、かつ、書き込み回数にも制限が無いというメリットを有している。というのは、本実施の形態で示すトランジスタは、オフ電流が小さいため、容量４３０に蓄えられた電荷を逃しにくいからである。
【００９９】
（実施の形態３）
本実施の形態では、実施の形態１で例示した酸化物半導体層４０３に用いることができる

、ＣＡＡＣ－ＯＳ（Ｃ　Ａｘｉｓ　Ａｌｉｇｎｅｄ　Ｃｒｙｓｔａｌｌｉｎｅ　Ｏｘｉｄｅ　Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）膜について説明する。

【０１００】
ＣＡＡＣ－ＯＳ膜は、完全な単結晶ではなく、完全な非晶質でもない。ＣＡＡＣ－ＯＳ膜は、非晶質相に結晶部を有する結晶－非晶質混相構造の酸化物半導体である。なお、当該結晶部は、一辺が１００ｎｍ未満の立方体内に収まる大きさであることが多い。また、透過型電子顕微鏡（ＴＥＭ：Ｔｒａｎｓｍｉｓｓｉｏｎ　Ｅｌｅｃｔｒｏｎ　Ｍｉｃｒｏｓｃｏｐｅ）による観察像では、ＣＡＡＣ－ＯＳ膜に含まれる非晶質部と結晶部との境界は明確ではない。また、ＴＥＭによってＣＡＡＣ－ＯＳ膜には粒界（グレインバウンダリーともいう）は確認できない。そのため、ＣＡＡＣ－ＯＳ膜は、粒界に起因する電子移動の低下が抑制される。

【０１０１】
ＣＡＡＣ－ＯＳ膜に含まれる結晶部は、ｃ軸がＣＡＡＣ－ＯＳ膜の被形成面または表面に垂直な方向に揃い、かつａｂ面に垂直な方向から見て三角形状または六角形状の原子配列を有し、ｃ軸に垂直な方向から見て金属原子が層状または金属原子と酸素原子とが層状に配列している。なお、異なる結晶部間で、それぞれａ軸およびｂ軸の向きが異なっていてもよい。本明細書等において、単に垂直と記載する場合、８５°以上９５°以下の範囲も含まれることとする。

【０１０２】
なお、ＣＡＡＣ－ＯＳ膜において、結晶部の分布が一様でなくてもよい。例えば、ＣＡＡＣ－ＯＳ膜の形成過程において、酸化物半導体膜の表面側から結晶成長させる場合、被形成面の近傍に対し表面の近傍では結晶部の占める割合が高くなることがある。

【０１０３】
ＣＡＡＣ－ＯＳ膜に含まれる結晶部のｃ軸は、ＣＡＡＣ－ＯＳ膜の被形成面または表面に垂直な方向に揃うため、ＣＡＡＣ－ＯＳ膜の形状（被形成面の断面形状または表面の断面形状）によっては互いに異なる方向を向くことがある。なお、結晶部のｃ軸の方向は、ＣＡＡＣ－ＯＳ膜が形成されたときの被形成面または表面に垂直な方向となる。結晶部は、成膜することにより、または成膜後に熱処理などの結晶化処理を行うことにより形成される。

【０１０４】
また、ＣＡＡＣ－ＯＳのように結晶部を有する酸化物半導体では、よりバルク内欠陥を低減することができ、表面の平坦性を高めればアモルファス状態の酸化物半導体以上の移動度を得ることができる。表面の平坦性を高めるためには、平坦な表面上に酸化物半導体を形成することが好ましく、具体的には、平均面粗さ（Ｒａ）が１ｎｍ以下、好ましくは０．３ｎｍ以下、より好ましくは０．１ｎｍ以下の表面上に形成するとよい。ただし、トランジスタ４４０は、ボトムゲート型であるため、上記平坦な表面を得るためにゲート電極層４０１および下地絶縁層４３６を形成した後、ＣＭＰ処理などの平坦化処理を行うことにより、酸化物半導体層４０３の被形成面の平坦性を向上させることができる。

【０１０５】
ＣＡＡＣ－ＯＳ膜を酸化物半導体層４０３として用いたトランジスタは、可視光や紫外光の照射によるトランジスタの電気特性の変動を低減させることが可能である。よって、当該トランジスタは信頼性が高い。

【０１０６】
（実施の形態４）
本実施の形態では、本明細書に示すトランジスタを使用し、電力が供給されない状況でも記憶内容の保持が可能で、かつ、書き込み回数にも制限が無い半導体装置（記憶装置）の一例を、図面を用いて説明する。

【０１０７】
図８は、半導体装置の構成の一例である。図８（Ａ）に、半導体装置の断面図を、図８（Ｂ）に半導体装置の回路図をそれぞれ示す。

【０１０８】
図８（Ａ）及び図８（Ｂ）に示す半導体装置は、下部に第１の半導体材料を用いたトランジスタ３２００を有し、上部に第２の半導体材料を用いたトランジスタ３２０２を有するものである。トランジスタ３２０２としては、実施の形態１で示すトランジスタ４２０の構造を適用する例である。
【０１０９】
ここで、第１の半導体材料と第２の半導体材料は異なる禁制帯幅を持つ材料とすることが望ましい。例えば、第１の半導体材料をワイドバンドギャップ半導体以外の半導体材料（シリコンなど）とし、第２の半導体材料をワイドバンドギャップ半導体とすることができる。一方で、ワイドバンドギャップ半導体を用いたトランジスタは、その特性により長時間の電荷保持を可能とする。
【０１１０】
なお、上記トランジスタは、いずれもｎチャネル型トランジスタであるものとして説明するが、ｐチャネル型トランジスタを用いることができるのはいうまでもない。また、情報を保持するためにワイドバンドギャップ半導体を用いた実施の形態１又は実施の形態２に示すようなトランジスタを用いる他は、半導体装置に用いられる材料や半導体装置の構造など、半導体装置の具体的な構成をここで示すものに限定する必要はない。
【０１１１】
図８（Ａ）におけるトランジスタ３２００は、半導体材料（例えば、シリコンなど）を含む基板３０００に設けられたチャネル形成領域と、チャネル形成領域を挟むように設けられた不純物領域と、不純物領域に接する金属化合物領域と、チャネル形成領域上に設けられたゲート絶縁膜と、ゲート絶縁膜上に設けられたゲート電極層と、を有する。なお、図において、明示的にはソース電極層やドレイン電極層を有しない場合があるが、便宜上、このような状態を含めてトランジスタと呼ぶ場合がある。また、この場合、トランジスタの接続関係を説明するために、ソース領域やドレイン領域を含めてソース電極層やドレイン電極層と表現することがある。つまり、本明細書において、ソース電極層との記載には、ソース領域が含まれうる。
【０１１２】
基板３０００上にはトランジスタ３２００を囲むように素子分離絶縁層３１０６が設けられており、トランジスタ３２００を覆うように絶縁層３２２０が設けられている。
【０１１３】
単結晶半導体基板を用いたトランジスタ３２００は、高速動作が可能である。このため、当該トランジスタを読み出し用のトランジスタとして用いることで、情報の読み出しを高速に行うことができる。トランジスタ３２０２および容量素子３２０４の形成前の処理として、トランジスタ３２００を覆う絶縁層３２２０にＣＭＰ処理を施して、絶縁層３２２０を平坦化すると同時にトランジスタ３２００のゲート電極層の上面を露出させる。
【０１１４】
図８（Ａ）に示すトランジスタ３２０２は、ワイドバンドギャップ半導体をチャネル形成領域に用いたボトムゲート型トランジスタである。ここで、トランジスタ３２０２に含まれる酸化物半導体層は、高純度化されたものであることが望ましい。高純度化された酸化物半導体層を用いることで、極めて優れたオフ特性のトランジスタ３２０２を得ることができる。
【０１１５】
図８（Ｂ）は、トランジスタ３２０２を用いた半導体記録装置の一例である。トランジスタ３２０２にオフ電流が小さいトランジスタ用いると、当該半導体記録装置は長期にわたり記憶内容を保持することが可能である。つまり、リフレッシュ動作を必要としない、或いは、リフレッシュ動作の頻度が極めて少ない半導体記憶装置とすることが可能となるため、消費電力を１０分に低減することができる。
【０１１６】
トランジスタ３２０２のソース電極層又はドレイン電極層の一方は、ゲート絶縁層に設け

られた開口を介して、電極３２０８と電気的に接続され、電極３２０８を介してトランジスタ３２００のゲート電極層と電気的に接続されている。電極３２０８は、トランジスタ３２０２のゲート電極層と同様の工程で作製することができる。

【０１１７】

また、トランジスタ３２０２上には、絶縁層３２２２と絶縁層３２２３とが設けられている。そして、絶縁層３２２２と絶縁層３２２３を介してトランジスタ３２０２のソース電極層又はドレイン電極層の一方と重畳する領域には、導電層３２１０ａが設けられており、トランジスタ３２０２のソース電極層又はドレイン電極層の一方と、絶縁層３２２２と導電層３２１０ａとによって、容量素子３２０４が構成される。すなわち、トランジスタ３２０２のソース電極層又はドレイン電極層の一方は、容量素子３２０４の一方の電極として機能し、導電層３２１０ａは、容量素子３２０４の他方の電極として機能する。なお、容量が不要の場合には、容量素子３２０４を設けない構成とすることもできる。また、容量素子３２０４は、別途、トランジスタ３２０２の上方に設けてもよい。

【０１１８】

容量素子３２０４上には絶縁層３２２４が設けられている。そして、絶縁層３２２４上にはトランジスタ３２０２と、他のトランジスタを接続するための配線３２１６が設けられている。配線３２１６は、絶縁層３２２４に形成された開口に設けられた３２１４、導電層３２１０ａと同じ層に設けられた導電層３２１０ｂ、及び、絶縁層３２２２に形成された開口に設けられた電極３２１２を介して、トランジスタ３２０２のソース電極層又はドレイン電極層の他方と電気的に接続される。

【０１１９】

図８（Ａ）及び図８（Ｂ）において、トランジスタ３２００と、トランジスタ３２０２とは、少なくとも一部が重畳するように設けられており、トランジスタ３２００のソース領域またはドレイン領域と、トランジスタ３２０２に含まれる酸化物半導体層の一部が重畳するように設けられているのが好ましい。また、トランジスタ３２０２及び容量素子３２０４が、トランジスタ３２００の少なくとも一部と重畳するように設けられている。例えば、容量素子３２０４の導電層３２１０ａは、トランジスタ３２００のゲート電極層と少なくとも一部が重畳して設けられている。このような平面レイアウトを採用することにより、半導体装置の占有面積の低減を図ることができるため、高集積化を図ることができる。

【０１２０】

次に、図８（Ａ）に対応する回路構成の一例を図８（Ｂ）に示す。

【０１２１】

図８（Ｂ）において、第１の配線（１ｓｔ　Ｌｉｎｅ）とトランジスタ３２００のソース電極層とは、電気的に接続され、第２の配線（２ｎｄ　Ｌｉｎｅ）とトランジスタ３２００のドレイン電極層とは、電気的に接続されている。また、第３の配線（３ｒｄ　Ｌｉｎｅ）とトランジスタ３２０２のソース電極層またはドレイン電極層の一方とは、電気的に接続され、第４の配線（４ｔｈ　Ｌｉｎｅ）と、トランジスタ３２０２のゲート電極層とは、電気的に接続されている。そして、トランジスタ３２００のゲート電極層と、トランジスタ３２０２のソース電極層またはドレイン電極層の一方は、容量素子３２０４の電極の他方と電気的に接続され、第５の配線（５ｔｈ　Ｌｉｎｅ）と、容量素子３２０４の電極の他方は電気的に接続されている。

【０１２２】

図８（Ｂ）に示す半導体装置では、トランジスタ３２００のゲート電極層の電位が保持可能という特徴を生かすことで、次のように、情報の書き込み、保持、読み出しが可能である。

【０１２３】

情報の書き込みおよび保持について説明する。まず、第４の配線の電位を、トランジスタ３２０２がオン状態となる電位にして、トランジスタ３２０２をオン状態とする。これにより、第３の配線の電位が、トランジスタ３２００のゲート電極層、および容量素子３２

０４に与えられる。すなわち、トランジスタ３２００のゲート電極層には、所定の電荷が与えられる（書き込み）。ここでは、異なる二つの電位レベルを与える電荷（以下Ｌｏｗレベル電荷、Ｈｉｇｈレベル電荷という）のいずれかが与えられるものとする。その後、第４の配線の電位を、トランジスタ３２０２がオフ状態となる電位にして、トランジスタ３２０２をオフ状態とすることにより、トランジスタ３２００のゲート電極層に与えられた電荷が保持される（保持）。

【０１２４】
トランジスタ３２０２のオフ電流は極めて小さいため、トランジスタ３２００のゲート電極層の電荷は長時間にわたって保持される。

【０１２５】
次に情報の読み出しについて説明する。第１の配線に所定の電位（定電位）を与えた状態で、第５の配線に適切な電位（読み出し電位）を与えると、トランジスタ３２００のゲート電極層に保持された電荷量に応じて、第２の配線は異なる電位をとる。一般に、トランジスタ３２００をｎチャネル型とすると、トランジスタ３２００のゲート電極層にＨｉｇｈレベル電荷が与えられている場合の見かけのしきい値Ｖｔｈ＿Ｈは、トランジスタ３２００のゲート電極層にＬｏｗレベル電荷が与えられている場合の見かけのしきい値Ｖｔｈ＿Ｌより低くなるためである。ここで、見かけのしきい値電圧とは、トランジスタ３２００を「オン状態」とするために必要な第５の配線の電位をいうものとする。したがって、第５の配線の電位をＶｔｈ＿ＨとＶｔｈ＿Ｌの中間の電位Ｖ０とすることにより、トランジスタ３２００のゲート電極層に与えられた電荷を判別できる。例えば、書き込みにおいて、Ｈｉｇｈレベル電荷が与えられていた場合には、第５の配線の電位がＶ０（＞Ｖｔｈ＿Ｈ）となれば、トランジスタ３２００は「オン状態」となる。Ｌｏｗレベル電荷が与えられていた場合には、第５の配線の電位がＶ０（＜Ｖｔｈ＿Ｌ）となっても、トランジスタ３２００は「オフ状態」のままである。このため、第２の配線の電位を見ることで、保持されている情報を読み出すことができる。

【０１２６】
なお、メモリセルをアレイ状に配置して用いる場合、所望のメモリセルの情報のみを読み出せることが必要になる。このように情報を読み出さない場合には、ゲート電極層の状態にかかわらずトランジスタ３２００が「オフ状態」となるような電位、つまり、Ｖｔｈ＿Ｈより小さい電位を第５の配線に与えればよい。または、ゲート電極層の状態にかかわらずトランジスタ３２００が「オン状態」となるような電位、つまり、Ｖｔｈ＿Ｌより大きい電位を第５の配線に与えればよい。

【０１２７】
本実施の形態に示す半導体装置では、チャネル形成領域にワイドバンドギャップ半導体を用いたオフ電流の極めて小さいトランジスタを適用することで、極めて長期にわたり記憶内容を保持することが可能である。つまり、リフレッシュ動作が不要となるか、または、リフレッシュ動作の頻度を極めて低くすることが可能となるため、消費電力を１０分に低減することができる。また、電力の供給がない場合（ただし、電位は固定されていることが望ましい）であっても、長期にわたって記憶内容を保持することが可能である。

【０１２８】
また、本実施の形態に示す半導体装置では、情報の書き込みに高い電圧を必要とせず、素子の劣化の問題もない。例えば、従来の不揮発性メモリのように、フローティングゲートへの電子の注入や、フローティングゲートからの電子の引き抜きを行う必要がないため、ゲート絶縁膜の劣化といった問題が全く生じない。すなわち、開示する発明に係る半導体装置では、従来の不揮発性メモリで問題となっている書き換え可能回数に制限はなく、信頼性が飛躍的に向上する。さらに、トランジスタのオン状態、オフ状態によって、情報の書き込みが行われるため、高速な動作も容易に実現しうる。

【０１２９】
以上のように、微細化及び高集積化を実現し、かつ高い電気的特性を付与された半導体装置、及び該半導体装置の作製方法を提供することができる。

【０１３０】
以上、本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。
【０１３１】
（実施の形態５）
本実施の形態では、実施の形態４と異なる構成の記憶装置の構造の一形態について説明する。
【０１３２】
図９は、記憶装置の斜視図である。図９に示す記憶装置は上部に記憶回路としてメモリセルを複数含む、メモリセルアレイ（メモリセルアレイ３４００ａからメモリセルアレイ３４００ｎ（ｎは２以上の整数））を複数層有し、下部にメモリセルアレイ３４００ａからメモリセルアレイ３４００ｎを動作させるために必要な論理回路３００４を有する。
【０１３３】
図１０に、図９に示した記憶装置の部分拡大図を示す。図１０では、論理回路３００４、メモリセルアレイ３４００ａ及びメモリセルアレイ３４００ｂを図示しており、メモリセルアレイ３４００ａ又はメモリセルアレイ３４００ｂに含まれる複数のメモリセルのうち、メモリセル３１７０ａと、メモリセル３１７０ｂを代表で示す。メモリセル３１７０ａ及びメモリセル３１７０ｂとしては、例えば、上記に実施の形態において説明した回路構成と同様の構成とすることもできる。
【０１３４】
なお、メモリセル３１７０ａに含まれるトランジスタ３１７１ａを代表で示す。メモリセル３１７０ｂに含まれるトランジスタ３１７１ｂを代表で示す。トランジスタ３１７１ａ及びトランジスタ３１７１ｂは、酸化物半導体層にチャネル形成領域を有する。酸化物半導体層にチャネル形成領域が形成されるトランジスタの構成については、その他の実施の形態において説明した構成と同様であるため、説明は省略する。
【０１３５】
トランジスタ３１７１ａのゲート電極層と同じ層に形成された導電層３５０１ａは、電極３５０２ａによって、電極３００３ａと電気的に接続されている。トランジスタ３１７１ｂのゲート電極層と同じ層に形成された、導電層３５０１ｃは、電極３５０２ｃによって、電極３００３ｃと電気的に接続されている。
【０１３６】
また、論理回路３００４は、ワイドバンドギャップ半導体以外の半導体材料をチャネル形成領域として用いたトランジスタ３００１を有する。トランジスタ３００１は、半導体材料（例えば、シリコンなど）を含む基板３０００に素子分離絶縁層３１０６を設け、素子分離絶縁層３１０６に囲まれた領域にチャネル形成領域となる領域を形成することによって得られるトランジスタとすることができる。なお、トランジスタ３００１は、絶縁表面上に形成されたシリコン膜等の半導体膜や、ＳＯＩ基板のシリコン膜にチャネル形成領域が形成されるトランジスタであってもよい。トランジスタ３００１の構成については、公知の構成を用いることが可能であるため、説明は省略する。
【０１３７】
トランジスタ３１７１ａが形成された層と、トランジスタ３００１が形成された層との間には、配線３１００ａ及び配線３１００ｂが形成されている。配線３１００ａとトランジスタ３００１が形成された層との間には、絶縁膜３１４０ａが設けられ、配線３１００ａと配線３１００ｂとの間には、絶縁膜３１４１ａが設けられ、配線３１００ｂとトランジスタ３１７１ａが形成された層との間には、絶縁膜３１４２ａが設けられている。
【０１３８】
同様に、トランジスタ３１７１ｂが形成された層と、トランジスタ３１７１ａが形成された層との間には、配線３１００ｃ及び配線３１００ｄが形成されている。配線３１００ｃとトランジスタ３１７１ａが形成された層との間には、絶縁膜３１４０ｂが設けられ、配線３１００ｃと配線３１００ｄとの間には、絶縁膜３１４１ｂが設けられ、配線３１００

ｄとトランジスタ３１７１ｂが形成された層との間には、絶縁膜３１４２ｂが設けられている。
【０１３９】
絶縁膜３１４０ａ、絶縁膜３１４１ａ、絶縁膜３１４２ａ、絶縁膜３１４０ｂ、絶縁膜３１４１ｂ、絶縁膜３１４２ｂは、層間絶縁膜として機能し、その表面は平坦化された構成とすることができる。
【０１４０】
配線３１００ａ、配線３１００ｂ、配線３１００ｃ、配線３１００ｄによって、メモリセル間の電気的接続や、論理回路３００４とメモリセルとの電気的接続等を行うことができる。
【０１４１】
論理回路３００４に含まれる電極３３０３は、上部に設けられた回路と電気的に接続することができる。
【０１４２】
例えば、図１０に示すように、電極３５０５によって電極３３０３は配線３１００ａと電気的に接続することができる。配線３１００ａは、電極３５０３ａによって、トランジスタ３１７１ａのゲート電極層と同じ層に形成された、導電層３５０１ｂと電気的に接続することができる。こうして、配線３１００ａ及び電極３３０３を、トランジスタ３１７１ａのソースまたはドレインと電気的に接続することができる。また、導電層３５０１ｂは、トランジスタ３１７１ａのソースまたはドレインと、電極３５０２ｂとによって、電極３００３ｂと電気的に接続することができる。電極３００３ｂは、電極３５０３ｂによって配線３１００ｃと電気的に接続することができる。
【０１４３】
図１０では、電極３３０３とトランジスタ３１７１ａとの電気的接続は、配線３１００ａを介して行われる例を示したがこれに限定されない。電極３３０３とトランジスタ３１７１ａとの電気的接続は、配線３１００ｂを介して行われてもよいし、配線３１００ａと配線３１００ｂの両方を介して行われてもよい。または、配線３１００ａも配線３１００ｂも介さず、他の電極を用いて行われてもよい。
【０１４４】
また、図１０では、トランジスタ３１７１ａが形成された層と、トランジスタ３００１が形成された層との間には、配線３１００ａが形成された配線層と、配線３１００ｂが形成された配線層との、２つの配線層が設けられた構成を示したがこれに限定されない。トランジスタ３１７１ａが形成された層と、トランジスタ３００１が形成された層との間に、１つの配線層が設けられていてもよいし、３つ以上の配線層が設けられていてもよい。
【０１４５】
また、図１０では、トランジスタ３１７１ｂが形成された層と、トランジスタ３１７１ａが形成された層との間には、配線３１００ｃが形成された配線層と、配線３１００ｄが形成された配線層との、２つの配線層が設けられた構成を示したがこれに限定されない。トランジスタ３１７１ｂが形成された層と、トランジスタ３１７１ａが形成された層との間に、１つの配線層が設けられていてもよいし、３つ以上の配線層が設けられていてもよい。
【０１４６】
以上、本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。
【０１４７】
（実施の形態６）
本明細書に開示する半導体装置は、さまざまな電子機器（遊技機も含む）に適用することができる。電子機器としては、テレビジョン装置（テレビ、またはテレビジョン受信機ともいう）、コンピュータ用などのモニタ、デジタルカメラ、デジタルビデオカメラ、デジタルフォトフレーム、携帯電話機、携帯型ゲーム機、携帯情報端末、音響再生装置、遊技

機（パチンコ機、スロットマシン等）、ゲーム筐体が挙げられる。これらの電子機器の具体例を図１１に示す。
【０１４８】
図１１（Ａ）および図１１（Ｂ）は２つ折り可能なタブレット型端末である。図１１（Ａ）は、開いた状態であり、タブレット型端末は、筐体９６３０、表示部９６３１ａ、表示部９６３１ｂ、表示モード切り替えスイッチ９０３４、電源スイッチ９０３５、省電力モード切り替えスイッチ９０３６、留め具９０３３、操作スイッチ９０３８、を有する。
【０１４９】
実施の形態1および２のいずれかに示す半導体装置は、表示部９６３１ａ、表示部９６３１ｂに用いることが可能であり、信頼性の高いタブレット型端末とすることが可能となる。
【０１５０】
表示部９６３１ａは、一部をタッチパネルの領域９６３２ａとすることができ、表示された操作キー９６３８にふれることでデータ入力をすることができる。なお、表示部９６３１ａにおいては、一例として半分の領域が表示のみの機能を有する構成、もう半分の領域がタッチパネルの機能を有する構成を示しているが該構成に限定されない。表示部９６３１ａの全ての領域がタッチパネルの機能を有する構成としても良い。例えば、表示部９６３１ａの全面をキーボードボタン表示させてタッチパネルとし、表示部９６３１ｂを表示画面として用いることができる。
【０１５１】
また、表示部９６３１ｂにおいても表示部９６３１ａと同様に、表示部９６３１ｂの一部をタッチパネルの領域９６３２ｂとすることができる。また、タッチパネルのキーボード表示切り替えボタン９６３９が表示されている位置に指やスタイラスなどでふれることで表示部９６３１ｂにキーボードボタン表示することができる。
【０１５２】
また、タッチパネルの領域９６３２ａとタッチパネルの領域９６３２ｂに対して同時にタッチ入力することもできる。
【０１５３】
また、表示モード切り替えスイッチ９０３４は、縦表示または横表示などの表示の向きを切り替え、白黒表示やカラー表示の切り替えなどを選択できる。省電力モード切り替えスイッチ９０３６は、タブレット型端末に内蔵している光センサで検出される使用時の外光の光量に応じて表示の輝度を最適なものとすることができる。タブレット型端末は光センサだけでなく、ジャイロ、加速度センサ等の傾きを検出するセンサなどの他の検出装置を内蔵させてもよい。
【０１５４】
また、図１１（Ａ）では表示部９６３１ｂと表示部９６３１ａの表示面積が同じ例を示しているが特に限定されず、一方のサイズともう一方のサイズが異なっていてもよく、表示の品質も異なっていてもよい。例えば一方が他方よりも高精細な表示を行える表示パネルとしてもよい。
【０１５５】
図１１（Ｂ）は、閉じた状態であり、タブレット型端末は、筐体９６３０、太陽電池９６３３、充放電制御回路９６３４、バッテリー９６３５、ＤＣＤＣコンバータ９６３６を有する。なお、図１１（Ｂ）では充放電制御回路９６３４の一例としてバッテリー９６３５、ＤＣＤＣコンバータ９６３６を有する構成について示している。
【０１５６】
なお、タブレット型端末は２つ折り可能なため、未使用時に筐体９６３０を閉じた状態にすることができる。従って、表示部９６３１ａ、表示部９６３１ｂを保護できるため、耐久性に優れ、長期使用の観点からも信頼性の優れたタブレット型端末を提供できる。
【０１５７】
また、この他にも図１１（Ａ）および図１１（Ｂ）に示したタブレット型端末は、様々な

情報（静止画、動画、テキスト画像など）を表示する機能、カレンダー、日付または時刻などを表示部に表示する機能、表示部に表示した情報をタッチ入力操作または編集するタッチ入力機能、様々なソフトウェア（プログラム）によって処理を制御する機能、等を有することができる。

【０１５８】

タブレット型端末の表面に装着された太陽電池９６３３によって、電力をタッチパネル、表示部、または映像信号処理部等に供給することができる。なお、太陽電池９６３３は、筐体９６３０の一面または二面に効率的なバッテリー９６３５の充電を行う構成とすることができるため好適である。なおバッテリー９６３５としては、リチウムイオン電池を用いると、小型化を図れる等の利点がある。

【０１５９】

また、図１１（Ｂ）に示す充放電制御回路９６３４の構成、および動作について図１１（Ｃ）にブロック図を示し説明する。図１１（Ｃ）には、太陽電池９６３３、バッテリー９６３５、ＤＣＤＣコンバータ９６３６、コンバータ９６３７、スイッチＳＷ１からＳＷ３、表示部９６３１について示しており、バッテリー９６３５、ＤＣＤＣコンバータ９６３６、コンバータ９６３７、スイッチＳＷ１からＳＷ３が、図１１（Ｂ）に示す充放電制御回路９６３４に対応する箇所となる。

【０１６０】

まず外光により太陽電池９６３３により発電がされる場合の動作の例について説明する。太陽電池で発電した電力は、バッテリー９６３５を充電するための電圧となるようＤＣＤＣコンバータ９６３６で昇圧または降圧がなされる。そして、表示部９６３１の動作に太陽電池９６３３からの電力が用いられる際にはスイッチＳＷ１をオンにし、コンバータ９６３７で表示部９６３１に必要な電圧に昇圧または降圧をすることとなる。また、表示部９６３１での表示を行わない際には、ＳＷ１をオフにし、ＳＷ２をオンにしてバッテリー９６３５の充電を行う構成とすればよい。

【０１６１】

なお太陽電池９６３３については、発電手段の一例として示したが、特に限定されず、圧電素子（ピエゾ素子）や熱電変換素子（ペルティエ素子）などの他の発電手段によるバッテリー９６３５の充電を行う構成であってもよい。例えば、無線（非接触）で電力を送受信して充電する無接点電力電送モジュールや、また他の充電手段を組み合わせて行う構成としてもよい。

【０１６２】

本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。

【符号の説明】

【０１６３】

４００　　基板
４０１　　ゲート電極層
４０２　　ゲート絶縁層
４０３　　酸化物半導体層
４０５　　低抵抗材料膜
４０５ａ　　低抵抗材料層
４０５ｂ　　低抵抗材料層
４０６　　保護層
４２０　　トランジスタ
４３０　　容量
４３１　　トランジスタ
４３２　　絶縁層
４３６　　下地絶縁層
４４０　　トランジスタ

４５１　　酸素ドーピング
４５３　　レジスト
４５４　　導電膜
４５４ａ　　導電層
４５４ｂ　　導電層
４５５　　レジスト
４７４ａ　　配線層
４７４ｂ　　配線層
４８５　　配線保護膜
４８５ａ　　配線保護層
４８５ｂ　　配線保護層
３０００　　基板
３００１　　トランジスタ
３００３ａ　　電極
３００３ｂ　　電極
３００３ｃ　　電極
３００４　　論理回路
３１００ａ　　配線
３１００ｂ　　配線
３１００ｃ　　配線
３１００ｄ　　配線
３１０６　　素子分離絶縁層
３１４０ａ　　絶縁膜
３１４０ｂ　　絶縁膜
３１４１ａ　　絶縁膜
３１４１ｂ　　絶縁膜
３１４２ａ　　絶縁膜
３１４２ｂ　　絶縁膜
３１７０ａ　　メモリセル
３１７０ｂ　　メモリセル
３１７１ａ　　トランジスタ
３１７１ｂ　　トランジスタ
３２００　　トランジスタ
３２０２　　トランジスタ
３２０４　　容量素子
３２０８　　電極
３２１０ａ　　導電層
３２１０ｂ　　導電層
３２１２　　電極
３２１６　　配線
３２２０　　絶縁層
３２２２　　絶縁層
３２２３　　絶縁層
３２２４　　絶縁層
３３０３　　電極
３４００ａ　　メモリセルアレイ
３４００ｂ　　メモリセルアレイ
３４００ｎ　　メモリセルアレイ
３５０１ａ　　導電層
３５０１ｂ　　導電層

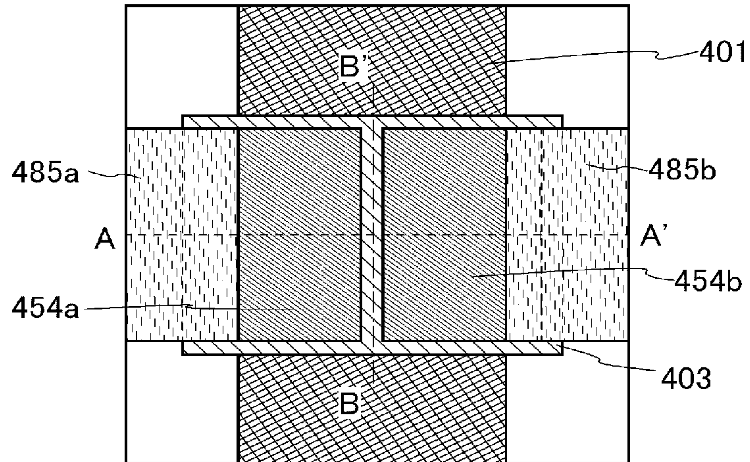
３５０１ｃ　　導電層
３５０２ａ　　電極
３５０２ｂ　　電極
３５０２ｃ　　電極
３５０３ａ　　電極
３５０３ｂ　　電極
３５０５　　電極
９０３３　　留め具
９０３４　　スイッチ
９０３５　　電源スイッチ
９０３６　　スイッチ
９０３８　　操作スイッチ
９６３０　　筐体
９６３１　　表示部
９６３１ａ　　表示部
９６３１ｂ　　表示部
９６３２ａ　　領域
９６３２ｂ　　領域
９６３３　　太陽電池
９６３４　　充放電制御回路
９６３５　　バッテリー
９６３６　　ＤＣＤＣコンバータ
９６３７　　コンバータ
９６３８　　操作キー
９６３９　　ボタン

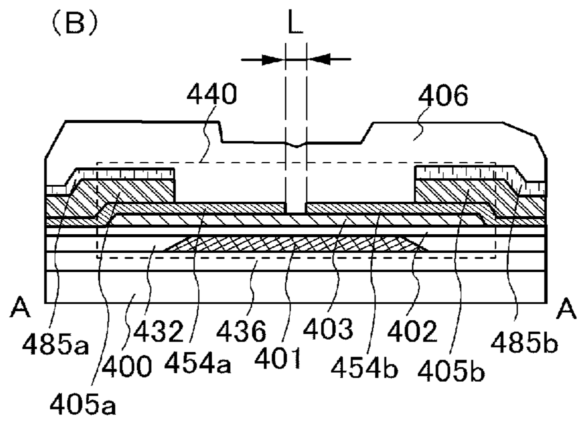
【書類名】特許請求の範囲
【請求項１】
絶縁表面上にゲート電極層を形成する工程と、
前記ゲート電極層の上に接するようにゲート絶縁層を形成する工程と、
前記ゲート絶縁層の上に接して、かつ前記ゲート電極層と重なるように、酸化物半導体層を形成する工程と、
前記酸化物半導体層の上に接して、かつ前記酸化物半導体層を覆うように、導電膜を形成する工程と、
前記導電膜の上に接して、低抵抗材料膜を形成する工程と、
前記低抵抗材料膜の上に接して、配線保護膜を形成する工程と、
前記ゲート電極層を挟んで離間する、第１配線保護層と第２配線保護層を形成する工程と、
前記ゲート電極層を挟んで離間する、前記第１配線保護層と接した第１低抵抗材料層と前記第２配線保護層と接した第２低抵抗材料層を形成する工程と、
前記第１低抵抗材料層と前記第２低抵抗材料層の間で、かつ前記酸化物半導体層と重なる領域に、開口パターン部を有するレジストパターンを形成する工程と、
前記レジストパターンを用いて、前記導電膜をエッチングして、第１導電層と第２導電層に分離して形成する工程と、
前記導電膜の開口部を保護層で充填する工程と、
を有する半導体装置の作製方法。
【請求項２】
ゲート電極層と、
前記ゲート電極層の上に接するゲート絶縁層と、
前記ゲート絶縁層の上に接し、かつ前記ゲート電極層と重なるように設けられた酸化物半導体層と、
前記酸化物半導体層の上に接し前記ゲート電極層を挟んで離間する、第１導電層と第２導電層と、
前記第１導電層の上に接する第１低抵抗材料層と、
前記第２導電層の上に接する第２低抵抗材料層と、
前記第１低抵抗材料層の上に接する第１配線保護層と、前記第２低抵抗材料層の上に接する第２配線保護層と、
保護層は、前記第１導電層および前記第１配線保護層ならびに前記第２導電層および前記第２配線保護層の上に接し、かつ前記酸化物半導体層と一部接するように設けられ、
前記第１導電層と前記第２導電層の間隔は、前記第１低抵抗材料層と前記第２低抵抗材料層の間隔よりも狭く、
前記第１導電層および前記第１低抵抗材料層はソース電極であり、前記第２導電層および前記第２低抵抗材料層はドレイン電極であることを特徴とする半導体装置。
【請求項３】
請求項２において、前記ゲート絶縁層が、平坦であることを特徴とする半導体装置。
【請求項４】
請求項２または請求項３において、前記酸化物半導体層のチャネル長方向の幅は、前記ゲート電極層のチャネル長方向の幅よりも広いことを特徴とする半導体装置。

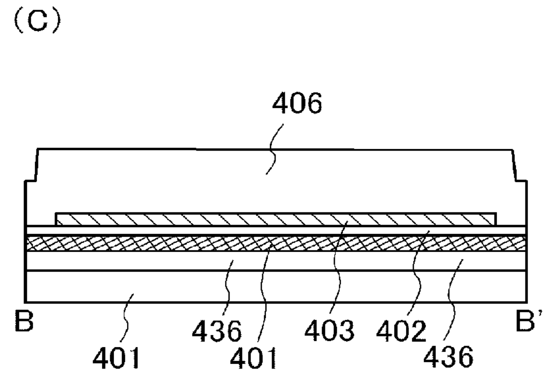
【書類名】要約書
【要約】
【課題】微細なチャネル長のボトムゲート型トランジスタを作製する方法、およびそのトランジスタを提供する。
【解決手段】ソース電極およびドレイン電極のチャネル形成領域に近接する部分を、他の部分より薄い構成にする、微細なチャネル長のボトムゲート型トランジスタを創作した。また、段差のある領域において、高さの高い低抵抗材料層の表面に保護層を有する微細なチャネル長のボトムゲート型トランジスタを創作した。また、ソース電極およびドレイン電極のチャネル形成領域に近接する部分を、他の部分より後の工程で形成し、段差のある領域において、高さの高い低抵抗材料層の表面に保護層を設けることにより、微細なチャネル長のボトムゲート型トランジスタを作製する方法を創作した。
【選択図】図１

【書類名】図面
【図１】

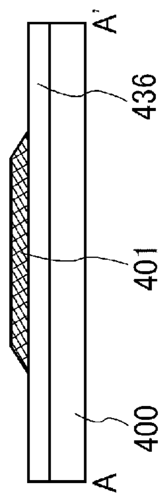
（A）



【図２】



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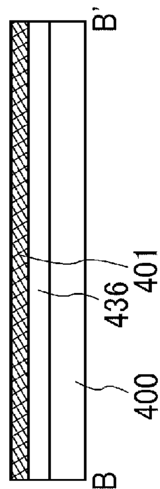

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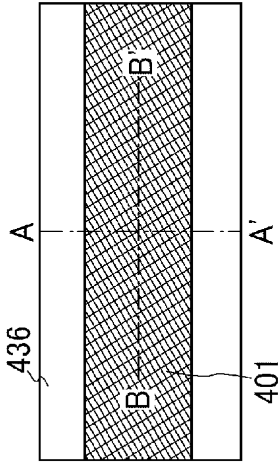

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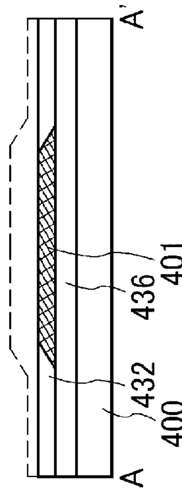

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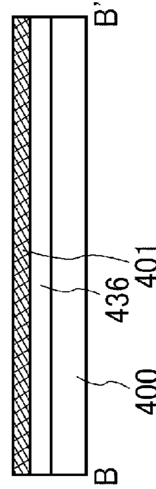

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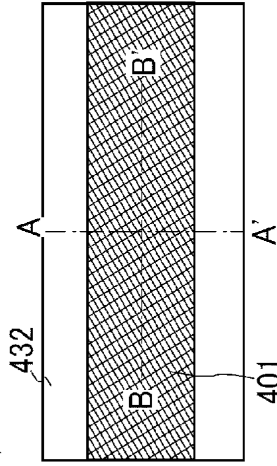

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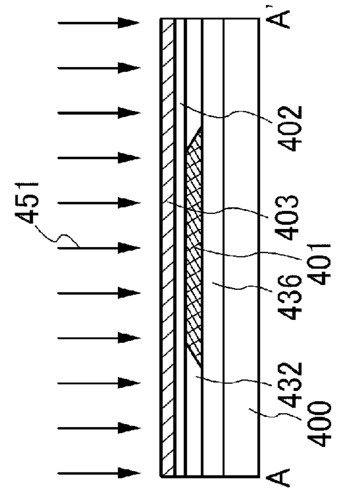

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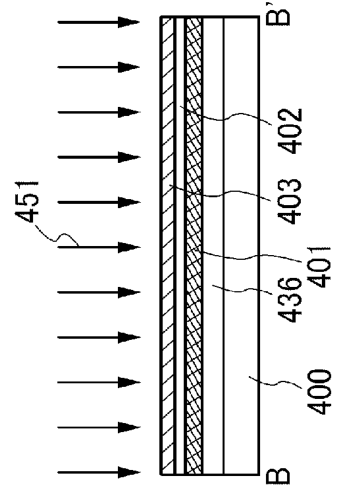

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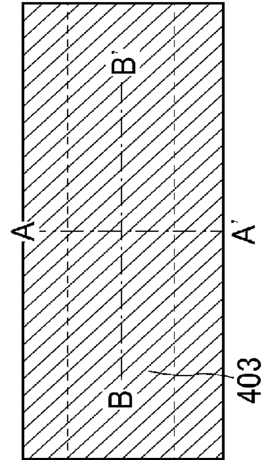
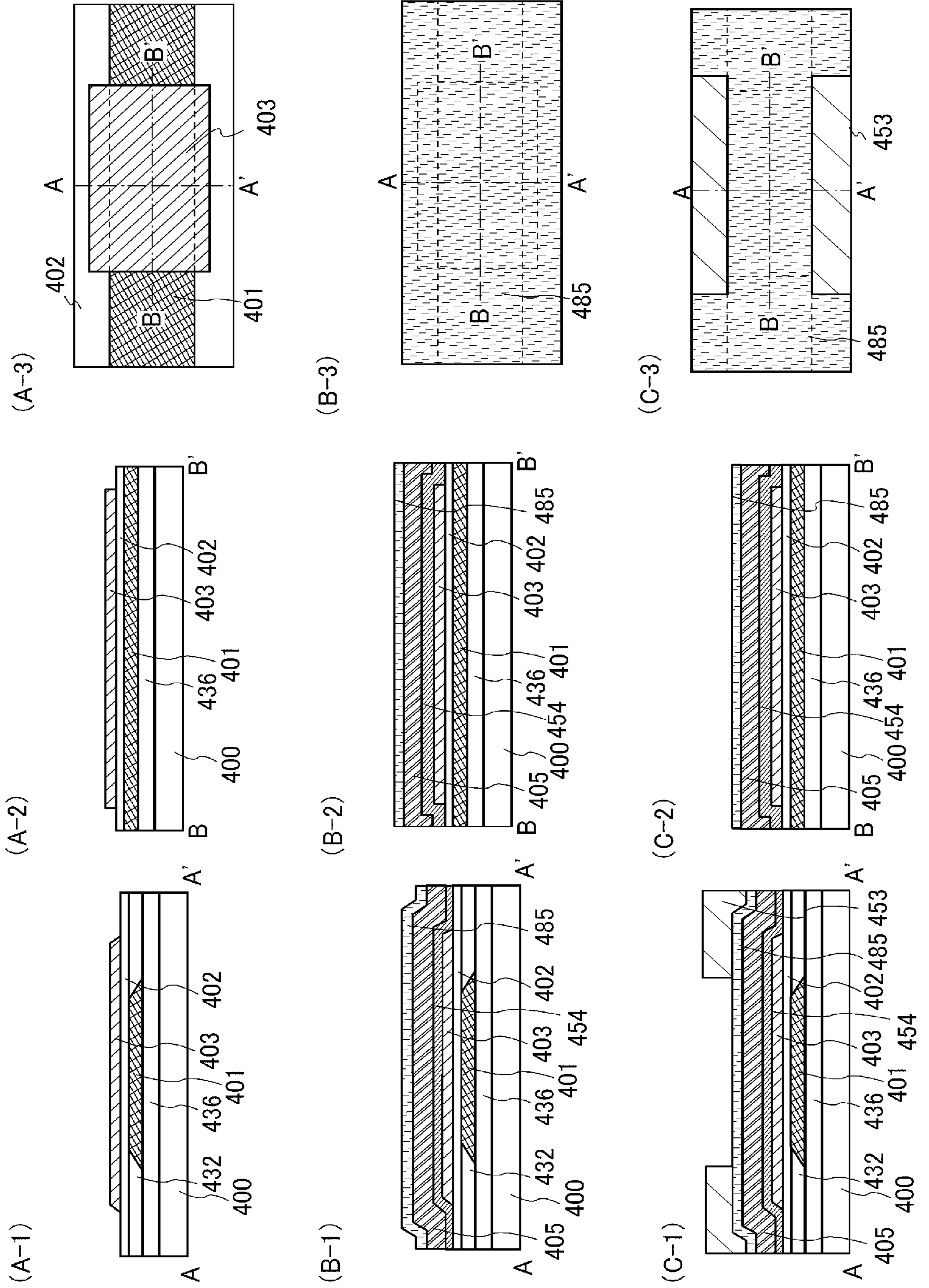


(C-3)

【図３】



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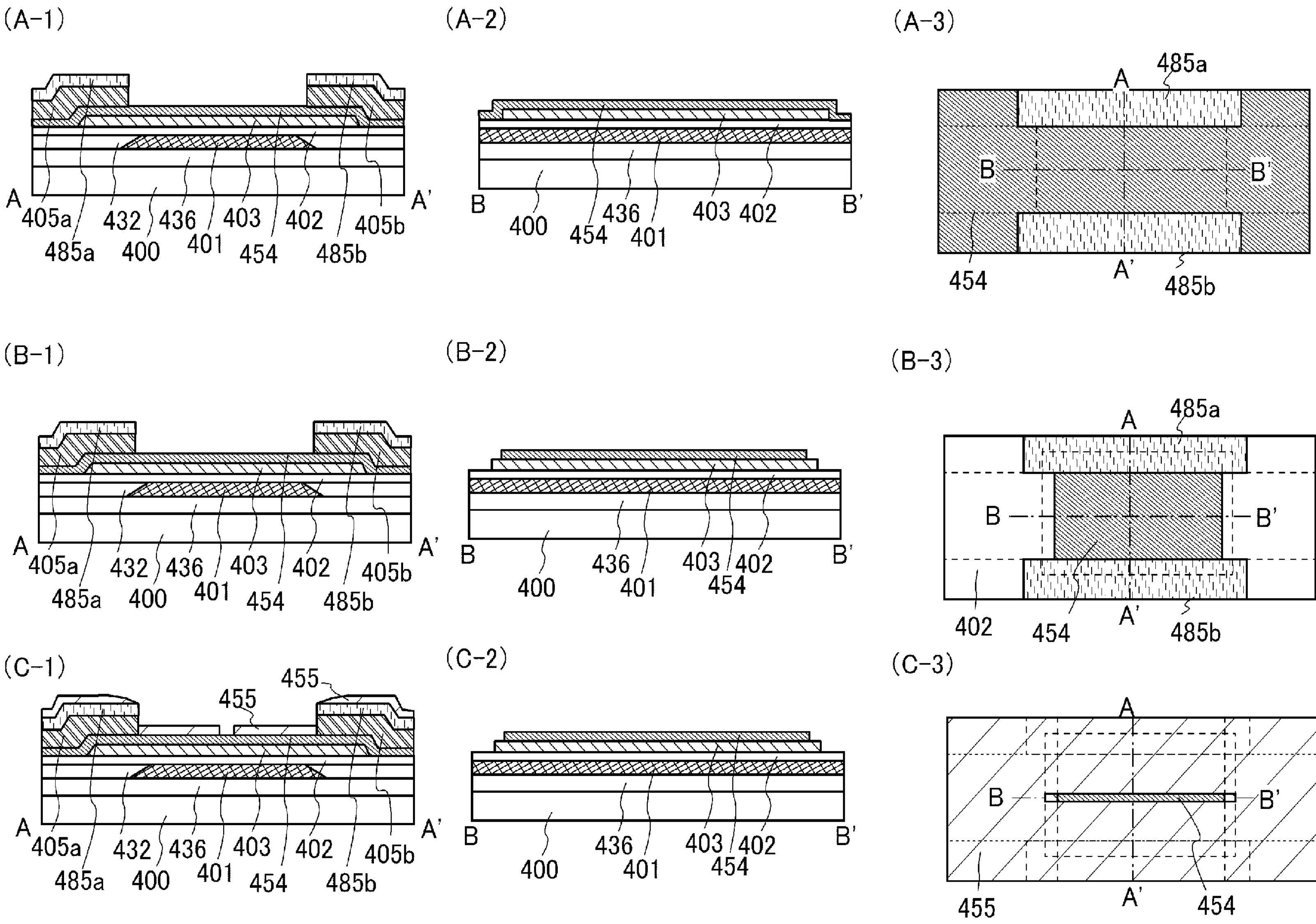

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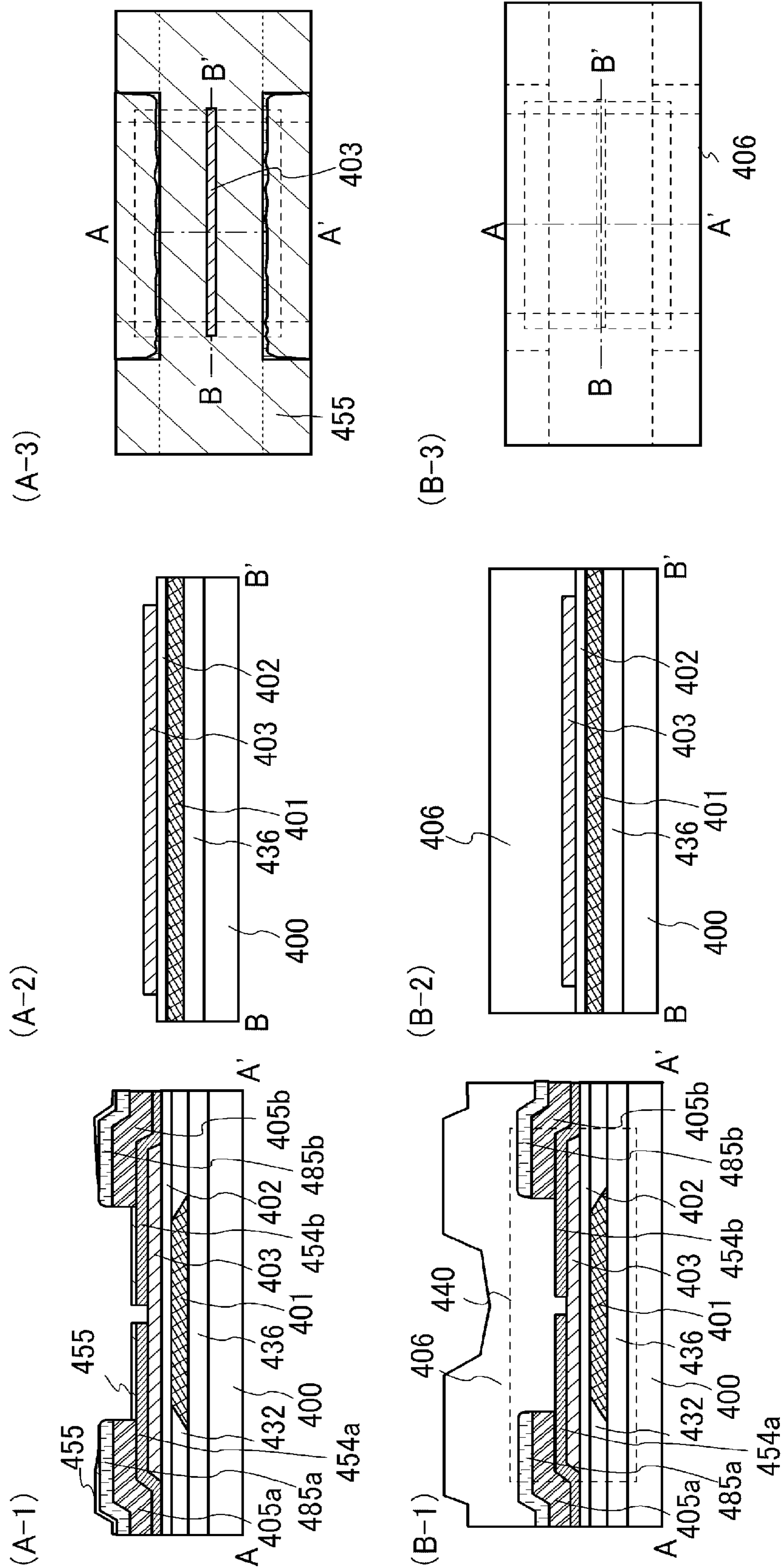
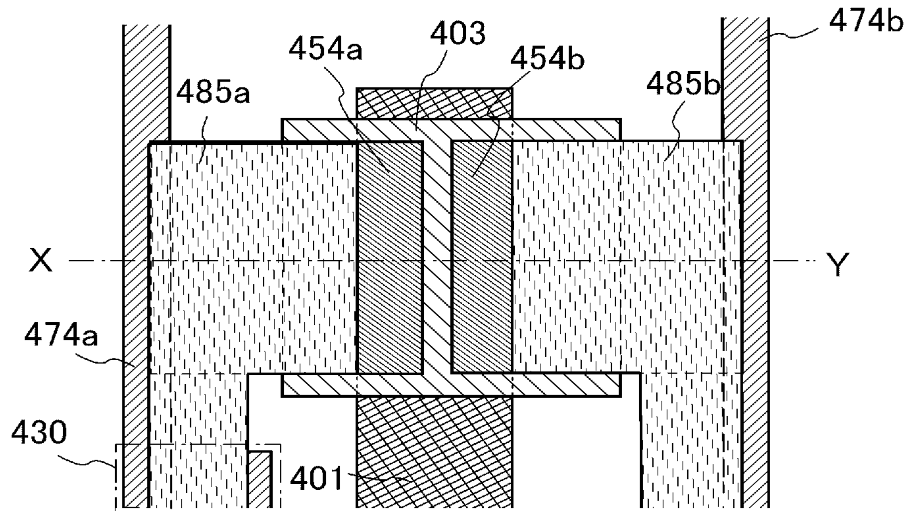
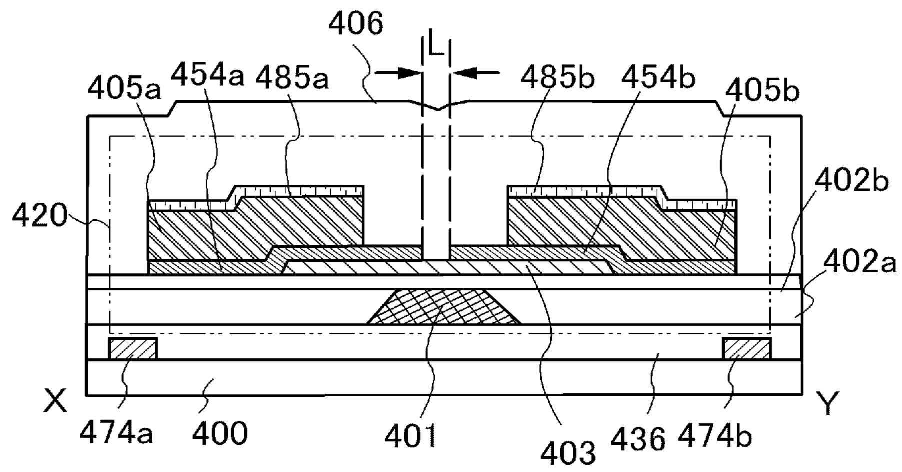


【図６】

（Ａ）




（Ｂ）

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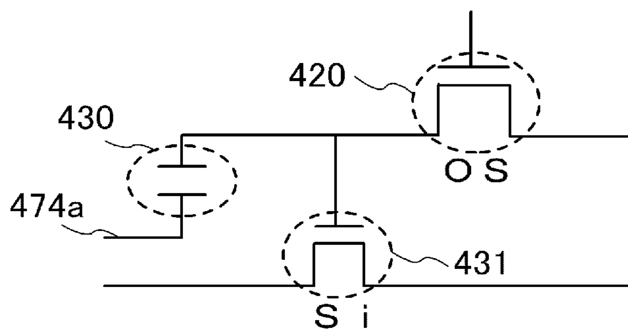
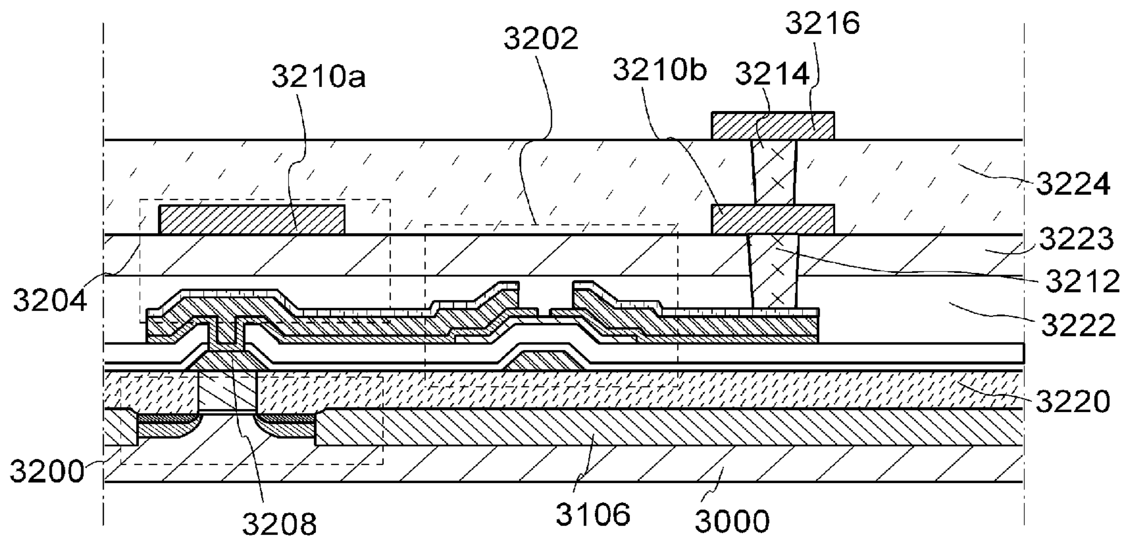
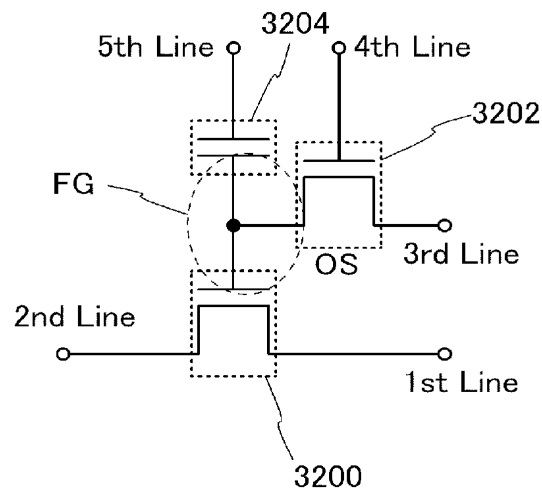


【図８】

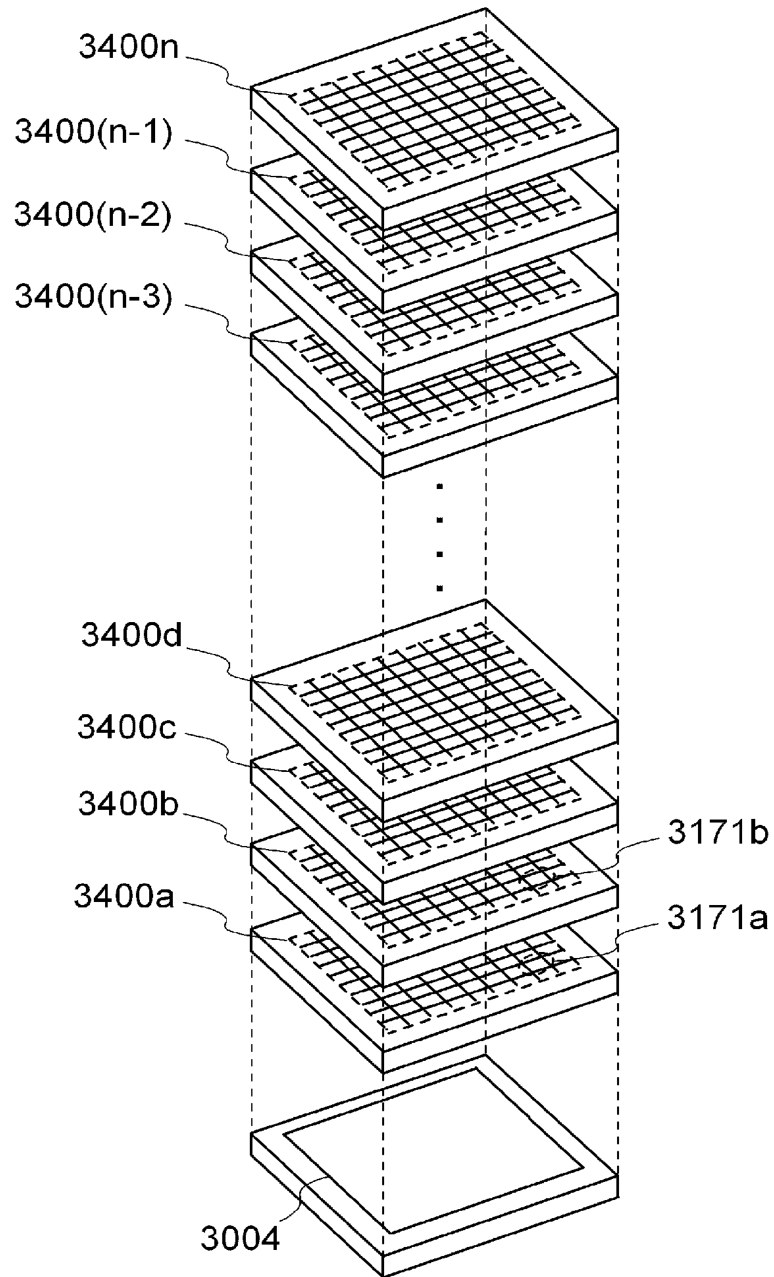
(A)



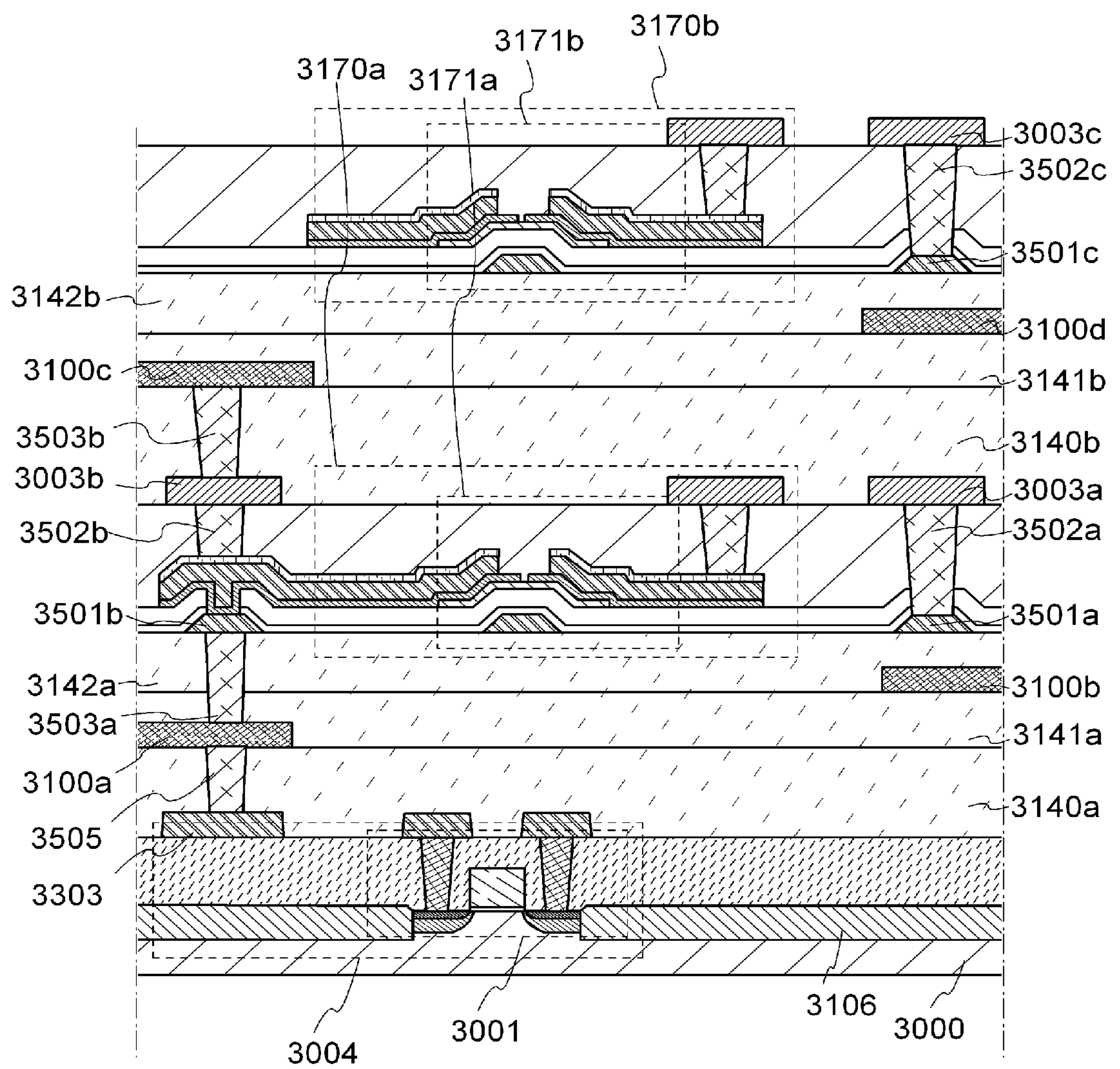

(B)



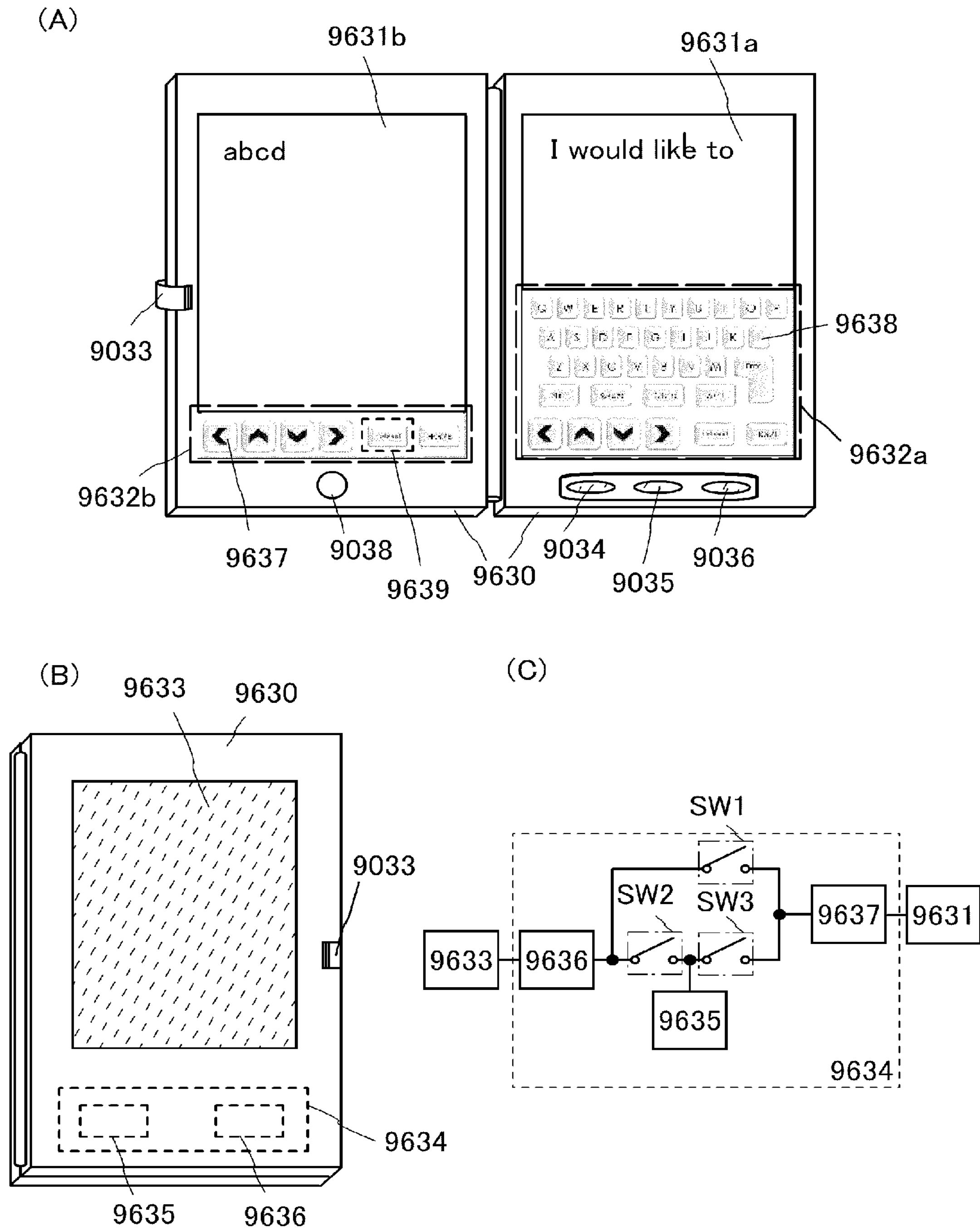
【図９】



【図１０】



【図１１】



出願人履歴

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新規登録

神奈川県厚木市長谷３９８番地

株式会社半導体エネルギー研究所

| PATENT APPLICATION FEE DETERMINATION RECORD<br>Substitute for Form PTO-875 | Application or Docket Number<br>14/337,583 |
|---|---|

APPLICATION AS FILED - PART I

| | (Column 1) | (Column 2) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE($) | FEE($) | | RATE($) | FEE($) |
| BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | 280 |
| SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | 600 |
| EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | 720 |
| TOTAL CLAIMS (37 CFR 1.16(i)) | 20 minus 20 = | * | | | OR | x 80 = | 0.00 |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | 3 minus 3 = | * | | | | x 420 = | 0.00 |
| APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | 0.00 |
| MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | 0.00 |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | 1600 |

APPLICATION AS AMENDED - PART II

| AMENDMENT A | | (Column 1) | | (Column 2) | (Column 3) | SMALL ENTITY | | OR | OTHER THAN SMALL ENTITY | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE($) | ADDITIONAL FEE($) | | RATE($) | ADDITIONAL FEE($) |
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | x = | | OR | x = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x = | | OR | x = | |
| | Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

| AMENDMENT B | | (Column 1) | | (Column 2) | (Column 3) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE($) | ADDITIONAL FEE($) | | RATE($) | ADDITIONAL FEE($) |
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | x = | | OR | x = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x = | | OR | x = | |
| | Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NUMBER | FILING or 371(c) DATE | GRP ART UNIT | FIL FEE REC'D | ATTY.DOCKET.NO | TOT CLAIMS | IND CLAIMS |
|---|---|---|---|---|---|---|
| 14/337,583 | 07/22/2014 | 2811 | 1600 | 0756-10540 | 20 | 3 |

**CONFIRMATION NO. 7546**

**FILING RECEIPT**

*OC000000069934911*

31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

Date Mailed: 08/01/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

**Inventor(s)**

Shinya SASAGAWA, Chigasaki, JAPAN;
Hideomi SUZAWA, Atsugi, JAPAN;

**Applicant(s)**

Semiconductor Energy Laboratory Co., Ltd., Atsugi-shi, JAPAN

**Power of Attorney:** The patent practitioners associated with Customer Number 31780

**Domestic Priority data as claimed by applicant**

This application is a DIV of 13/716,891 12/17/2012 PAT 8790961

**Foreign Applications** (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
JAPAN 2011-282438 12/23/2011
JAPAN 2011-282511 12/23/2011

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

**If Required, Foreign Filing License Granted:** 07/31/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/337,583**

**Projected Publication Date:** 11/13/2014

**Non-Publication Request:** No

**Early Publication Request:** No
**Title**

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

**Preliminary Class**

257

**Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:** No

## PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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## Title 35, United States Code, Section 184
## Title 37, Code of Federal Regulations, 5.11 & 5.15

**GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

**NOT GRANTED**

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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## *SelectUSA*

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PTO/AIA/15 (03-13)
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# UTILITY PATENT APPLICATION TRANSMITTAL

*(Only for new nonprovisional applications under 37 CFR 1.53(b))*

| | |
|---|---|
| *Attorney Docket No.* | 0756-10540 |
| *First Named Inventor* | Shinya SASAGAWA et al. |
| *Title* | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME; |
| *Express Mail Label No.* | |

## APPLICATION ELEMENTS

*See MPEP chapter 600 concerning utility patent application contents.*

*ADDRESS TO:* **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

1. ☐ **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. ☐ **Applicant asserts small entity status.** See 37 CFR 1.27
3. ☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. ☑ **Specification** [*Total Pages* 54 ]
   Both the claims and abstract must start on a new page.
   *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. ☑ **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 17 ]
6. **Inventor's Oath or Declaration** [*Total Pages* 4 ]
   *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. ☐ Newly executed (original or copy)
   b. ☑ A copy from a prior application (37 CFR 1.63(d))
7. ☑ **Application Data Sheet** ** See note below.*
   See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R**
   in duplicate, large table, or Computer Program (*Appendix*)
   ☐ Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission**
   (*if applicable, items a. – c. are required*)
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

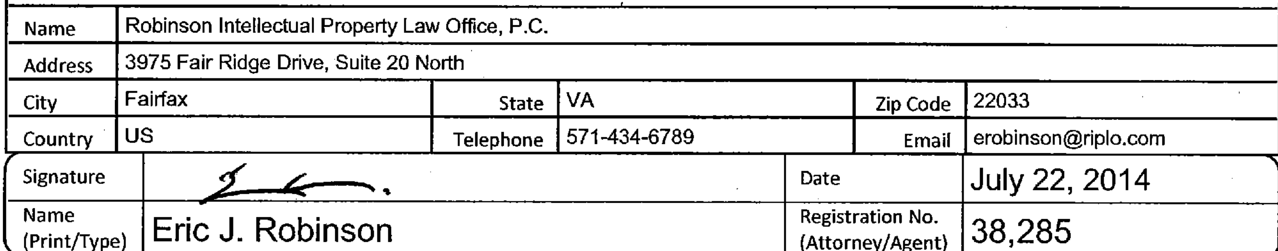
## ACCOMPANYING APPLICATION PAPERS

10. ☐ **Assignment Papers** (cover sheet & document(s))
    Name of Assignee ____________
11. ☑ **37 CFR 3.73(c) Statement** (*when there is an assignee*) ☑ **Power of Attorney**
12. ☐ **English Translation Document** (*if applicable*)
13. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations attached
14. ☐ **Preliminary Amendment**
15. ☐ **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. ☐ **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. ☐ **Nonpublication Request**
    Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. ☐ **Other:** ____________

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

## 19. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 31780 **OR** ☐ Correspondence address below



| | | | | | |
|---|---|---|---|---|---|
| Name | Robinson Intellectual Property Law Office, P.C. | | | | |
| Address | 3975 Fair Ridge Drive, Suite 20 North | | | | |
| City | Fairfax | State | VA | Zip Code | 22033 |
| Country | US | Telephone | 571-434-6789 | Email | erobinson@riplo.com |

| | | | |
|---|---|---|---|
| Signature | [signature] | Date | July 22, 2014 |
| Name (Print/Type) | Eric J. Robinson | Registration No. (Attorney/Agent) | 38,285 |

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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# Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
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## STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Semiconductor Energy Laboratory Co., Ltd.

Application No./Patent No.: ______________ Filed/Issue Date: July 22, 2014

Titled: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Semiconductor Energy Laboratory Co., Ltd., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is ________%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 029484, Frame 0026, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: ______________ To: ______________

   The document was recorded in the United States Patent and Trademark Office at

   Reel ________, Frame ________, or for which a copy thereof is attached.

2. From: ______________ To: ______________

   The document was recorded in the United States Patent and Trademark Office at

   Reel ________, Frame ________, or for which a copy thereof is attached.



This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

PTO/AIA/96 (08-12)
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## STATEMENT UNDER 37 CFR 3.73(c)

3. From: ______________________ To: ______________________

The document was recorded in the United States Patent and Trademark Office at

Reel ___________, Frame ___________, or for which a copy thereof is attached.

4. From: ______________________ To: ______________________

The document was recorded in the United States Patent and Trademark Office at

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5. From: ______________________ To: ______________________

The document was recorded in the United States Patent and Trademark Office at

Reel ___________, Frame ___________, or for which a copy thereof is attached.

6. From: ______________________ To: ______________________

The document was recorded in the United States Patent and Trademark Office at

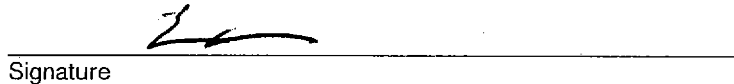
Reel ___________, Frame ___________, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.



Signature — Date: July 22, 2014

Printed or Typed Name: Eric J. Robinson — Title or Registration Number: Reg. No. 38,285

[Page 2 of 2]

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

# POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☑ Practitioners associated with Customer Number: 31780

**OR**

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

| Name | Registration Number | Name | Registration Number |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications a ssigned only to the undersigned according to the USPTO assignment records or assignments docu ments attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 31780

**OR**

☐

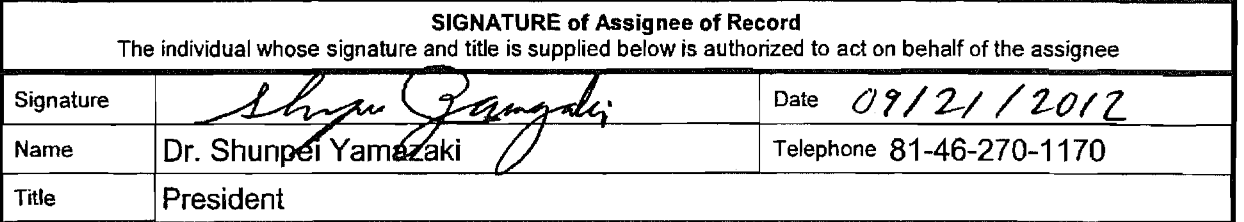
| Firm or Individual Name | | | |
|---|---|---|---|
| Address | | | |
| City | | | |
| Country | | | |
| Telephone | | Email | |

Assignee Name and Address: SEMICONDUCTOR ENERGY LABORATORY CO., LTD.
398, HASE, ATSUGI-SHI
KANAGAWA-KEN 243-0036
JAPAN

**A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.**

**SIGNATURE of Assignee of Record**

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee



| Signature | [signature] | Date 09/21/2012 |
|---|---|---|
| Name | Dr. Shunpei Yamazaki | Telephone 81-46-270-1170 |
| Title | President | |

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

## Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 0756-10540 |
|---|---|---|
| | Application Number | |

| Title of Invention | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME |
|---|---|

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

## Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

## Inventor Information:

**Inventor 1** [Remove]

**Legal Name**

| Prefix | Given Name | Middle Name | Family Name | Suffix |
|---|---|---|---|---|
| | Shinya | | SASAGAWA | |

**Residence Information (Select One)** ○ US Residency ◉ Non US Residency ○ Active US Military Service

| City | Chigasaki | Country of Residence i | JP |
|---|---|---|---|

**Mailing Address of Inventor:**

| Address 1 | c/o Semiconductor Energy Laboratory Co., Ltd. | | |
|---|---|---|---|
| Address 2 | 398, Hase | | |
| City | Atsugi-shi, Kanagawa-ken | State/Province | |
| Postal Code | 243-0036 | Country i | JP |

**Inventor 2** [Remove]

**Legal Name**

| Prefix | Given Name | Middle Name | Family Name | Suffix |
|---|---|---|---|---|
| | Hideomi | | SUZAWA | |

**Residence Information (Select One)** ○ US Residency ◉ Non US Residency ○ Active US Military Service

| City | Atsugi | Country of Residence i | JP |
|---|---|---|---|

**Mailing Address of Inventor:**

| Address 1 | c/o Semiconductor Energy Laboratory Co., Ltd. | | |
|---|---|---|---|
| Address 2 | 398, Hase | | |
| City | Atsugi-shi, Kanagawa-ken | State/Province | |
| Postal Code | 243-0036 | Country i | JP |

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. [Add]

## Correspondence Information:

| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 0756-10540 |
|---|---|---|
| | Application Number | |
| Title of Invention | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME | |

**Enter either Customer Number or complete the Correspondence Information section below.**
**For further information see 37 CFR 1.33(a).**

☐ **An Address is being provided for the correspondence Information of this application.**

| | | |
|---|---|---|
| **Customer Number** | 31780 | |
| **Email Address** | erobinson@riplo.com | Add Email / Remove Email |

## Application Information:

| | | | |
|---|---|---|---|
| **Title of the Invention** | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME | | |
| **Attorney Docket Number** | 0756-10540 | **Small Entity Status Claimed** | ☐ |
| **Application Type** | Nonprovisional | | |
| **Subject Matter** | Utility | | |
| **Total Number of Drawing Sheets (if any)** | 17 | **Suggested Figure for Publication (if any)** | |

## Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

| Application number of the previously filed application | Filing date (YYYY-MM-DD) | Intellectual Property Authority or Country i |
|---|---|---|
| | | |

## Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

## Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

| | | | |
|---|---|---|---|
| Please Select One: | ◉ Customer Number | ○ US Patent Practitioner | ○ Limited Recognition (37 CFR 11.9) |
| Customer Number | 31780 | | |

| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 0756-10540 |
|---|---|---|
| | Application Number | |
| Title of Invention | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME | |

## Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

| Prior Application Status | Pending | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) |
| | Division of | 13716891 | 2012-12-17 |

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

## Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) i the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

| Application Number | Country i | Filing Date (YYYY-MM-DD) | Access Code i (if applicable) |
|---|---|---|---|
| 2011-282438 | JP | 2011-12-23 | |

Remove

| Application Number | Country i | Filing Date (YYYY-MM-DD) | Access Code i (if applicable) |
|---|---|---|---|
| 2011-282511 | JP | 2011-12-23 | |

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 0756-10540 |
|---|---|---|
| | Application Number | |
| Title of Invention | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME | |

## Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

## Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

## Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 0756-10540 |
|---|---|---|
| | Application Number | |
| Title of Invention | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME | |

**Applicant 1** [Remove]

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section. [Clear]

- (●) Assignee
- ( ) Legal Representative under 35 U.S.C. 117
- ( ) Joint Inventor
- ( ) Person to whom the inventor is obligated to assign.
- ( ) Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. [X]

| Organization Name | Semiconductor Energy Laboratory Co., Ltd. | | |
|---|---|---|---|
| **Mailing Address Information:** | | | |
| **Address 1** | 398, Hase | | |
| Address 2 | | | |
| **City** | Atsugi-shi, Kanagawa-ken | **State/Province** | |
| **Country** i | JP | Postal Code | 243-0036 |
| Phone Number | | Fax Number | |
| Email Address | | | |

Additional Applicant Data may be generated within this form by selecting the Add button. [Add]

## Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

**Assignee 1**

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

[Remove]

If the Assignee or Non-Applicant Assignee is an Organization check here. [ ]

| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 0756-10540 |
|---|---|---|
| | Application Number | |

| Title of Invention | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME |
|---|---|

| Prefix | **Given Name** | Middle Name | **Family Name** | Suffix |
|---|---|---|---|---|
| | | | | |

**Mailing Address Information For Assignee including Non-Applicant Assignee:**

| **Address 1** | | | |
|---|---|---|---|
| Address 2 | | | |
| **City** | | **State/Province** | |
| **Country** i | | Postal Code | |
| Phone Number | | Fax Number | |
| Email Address | | | |

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

## Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

| **Signature** | /Eric J. Robinson/ | | | Date (YYYY-MM-DD) | 2014-07-22 |
|---|---|---|---|---|---|
| First Name | Eric J. | Last Name | Robinson | Registration Number | 38285 |

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/01 (06-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

# 申請データシート(37 CFR 1.76)を使った実用及び意匠登録出願宣誓書(37 CFR 1.63)
# DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

| 発明の名称 Title of Invention | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME |
|---|---|

下記発明者である私は、つぎのことがらを宣誓します。
As the below named inventor, I hereby declare that:

本宣誓は
This declaration is directed to:

☑ 添付されている、あるいは
The attached application, or

☐ 米国出願、あるいは__________に出願された PCT 国際願番号__________として出願されているものに宛てられています。
United States application or PCT international application number __________ filed on __________.

上記の出願は私自身、あるいは私が権限を授与したものによって行われたものです。
The above-identified application was made or authorized to be made by me.

私は本出願書中にあらわれるもともとの発明者、あるいはもともとの共同発明者です。
I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

本宣誓書において故意に虚偽の申し立てを行った場合は 18 U.S.C. 1001 により、罰金あるいは最高五(5)年の禁固刑、あるいはその両方による罰則の対象となることを認めます。
I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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# DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

| 発明の名称 Title of Invention | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME |
|---|---|

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The attached application, or

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DESCRIPTION

# SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

## TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device typified by a transistor and a method for manufacturing the semiconductor device.

## BACKGROUND ART

[0002]

Transistors in which a semiconductor material is deposited over a substrate having an insulating surface to be used as an active layer (hereinafter referred to as deposited-film transistors) have been researched. A silicon-based semiconductor material such as amorphous silicon has been conventionally used as an active layer; however, attention is focused in recent years on research on transistors in which an oxide semiconductor material is used as an active layer. This is because a transistor in which an oxide semiconductor material is used as an active layer (hereinafter referred to as an oxide semiconductor transistor) has higher on-state current and lower off-state current than a transistor in which amorphous silicon is used as an active layer.

[0003]

Further, there have been attempts to develop a semiconductor device which functions as a memory or the like by forming an oxide semiconductor transistor having the above features in a layer different from a transistor including single crystal silicon, and the like (Patent Document 1 and Non-Patent Document 1). In the structure of such a semiconductor device, the transistor in the upper layer is preferably a bottom-gate transistor. This is because a wiring which electrically connects the transistor in the lower layer can serve also as a gate electrode of the transistor in the upper layer.

[References]

[Patent Document]

[0004]

[Patent Document 1] Japanese Published Patent Application No. 2011-238333

[Non-Patent Document]

[0005]

[Non-Patent Document 1] K. Kaneko et al., "Highly Reliable BEOL-Transistor with
5 Oxygen-controlled InGaZnO and Gate/Drain Offset Design for High/Low Voltage Bridging I/O Operations", IEDM 2011, pp.155-158.

DISCLOSURE OF INVENTION

[0006]

10 In the above semiconductor device, which includes a plurality of transistors in a plurality of layers, the bottom-gate transistor formed in the upper layer is preferably a deposited-film transistor. This is because an active layer can be easily formed by deposition, which facilitates manufacture of the semiconductor device.

[0007]

15 Conventional semiconductor devices which include a plurality of transistors in a plurality of layers and in which a bottom-gate transistor is formed in the upper layer are easy to manufacture, but do not have sufficient performance capabilities as semiconductor devices. This is because the bottom-gate transistor in the upper layer does not have sufficient electric characteristics. For example, in a memory using a
20 semiconductor device which includes a plurality of transistors in a plurality of layers, a transistor which performs writing to the memory does not have sufficient writing capability or the like when the transistor is a deposited-film transistor. This is because the bottom-gate transistor in the upper layer does not have sufficient electric characteristics, particularly because the on-state current is lower than that of a transistor
25 in which bulk silicon is used as an active layer. Therefore, it is necessary to increase the on-state current of the deposited-film transistor. One method for achieving this is to use the bottom-gate transistor whose channel length is reduced (for example, to about 30 nm). Note that a photolithography process using an electron beam is necessary for reducing the channel length to less than 30 nm.

30 [0008]

In order to reduce the channel length of a bottom-gate transistor whose source electrode and drain electrode are formed by separating one conductive layer using a

photolithography process, the thickness of a resist needs to be less than or equal to the desired channel length. Meanwhile, the thickness of the resist is reduced during the etching step of the conductive layer. Therefore, the thickness of the conductive layer needs to be set such that the conductive layer can be separated before the resist is
5 removed in the etching step.

[0009]

On the other hand, there is a limitation on reduction in the thickness of the conductive layer because the source electrode and the drain electrode of the transistor preferably have low electric resistance.

10 [0010]

As described above, it is difficult to reduce the channel length of the bottom-gate transistor while suppressing the electric resistance between the source electrode and the drain electrode.

[0011]

15 An object of one embodiment of the present invention is to provide a bottom-gate transistor with a short channel length. Another object is to provide a method for manufacturing a bottom-gate transistor with a short channel length.

[0012]

The inventors have focused on the structure of the source electrode and the
20 drain electrode of the bottom-gate transistor. Thus, the inventors have devised a structure in which portions of the source electrode and the drain electrode which are proximate to a channel formation region are thinner than other portions thereof.

[0013]

The inventors have also devised a method in which the portions of the source
25 electrode and the drain electrode which are proximate to the channel formation region are formed in a later step than the other portions thereof.

[0014]

Further, the inventors focused on the following phenomenon: steps which are caused between a portion proximate to the channel formation region and the other
30 portions by the formation of the other portions (i.e., portions other than the portions proximate to the channel formation region) of the source electrode and the drain electrode cannot be covered with a resist at the time of the formation of the portions of

the source electrode and the drain electrode which are proximate to the channel formation region. Thus, the inventors have devised a method for manufacturing a bottom-gate transistor with a short channel length, which includes the steps of: covering the steps with an insulating layer, planarizing the insulating layer, forming a hard mask
5 layer over the planarized insulating layer, and separating the portion proximate to the channel formation region with the hard mask layer.

[0015]

Specifically, one embodiment of the present invention is a method for manufacturing a semiconductor device, including the steps of: forming a gate electrode
10 layer over an insulating surface; forming a gate insulating layer on and in contact with the gate electrode layer; forming an oxide semiconductor layer overlapping with the gate electrode layer on and in contact with the gate insulating layer; forming a conductive layer covering the oxide semiconductor layer on and in contact with the oxide semiconductor layer; forming, on and in contact with the conductive layer, a first
15 low-resistance material layer and a second low-resistance material layer apart from each other with the gate electrode layer provided therebetween; forming a first protective layer on and in contact with the first low-resistance material layer, the second low-resistance material layer, and the conductive layer; planarizing the first protective layer; forming a hard mask layer on and in contact with the planarized first protective
20 layer; forming, on a surface of the hard mask layer, a resist pattern including an opening pattern portion in a region that is between the first low-resistance material layer and the second low-resistance material layer and overlaps with the oxide semiconductor layer; etching the hard mask layer using the resist pattern to form an opening pattern; etching the first protective layer using the hard mask layer including the opening pattern as a
25 mask until the conductive layer is exposed; etching the conductive layer using the hard mask layer and the first protective layer including the opening pattern as masks to separate the conductive layer into a first conductive layer and a second conductive layer; and filling an opening in the first protective layer with a second protective layer.

[0016]

30 The steps between the portion proximate to the channel formation region and the other portions are planarized with an insulating layer, and then, a hard mask layer is formed and a resist for forming an opening is applied on the hard mask layer. Since

the surface on which the resist is to be applied is flat, the resist can be uniformly formed, which prevents a region which cannot be covered with the resist from being formed and enables the resist to be thinly and uniformly formed. Thus, an opening pattern with a small line width can be formed with the resist over the hard mask layer.

5 [0017]

As described above, a transistor with a short channel length can be formed by processing a conductive layer with the use of a hard mask layer. Even when the resist is removed during the processing, a problem in that processing cannot be performed after the removal is prevented owing to the hard mask layer. This is because the hard 10 mask layer serves as a mask for the processing of the first protective layer and the conductive layer. Note that the hard mask layer can be formed using a film which is not easily etched under conditions for etching the first protective layer and the conductive layer.

[0018]

15 Through the above steps, the conductive layer for forming the source electrode and the drain electrode can be provided with an opening with a minute pattern. Thus, a bottom-gate transistor with a short channel length can be manufactured.

[0019]

Another embodiment of the present invention is a method for manufacturing a 20 semiconductor device, including the steps of: forming a gate electrode layer over an insulating surface; forming a gate insulating layer on and in contact with the gate electrode layer; forming an oxide semiconductor layer overlapping with the gate electrode layer on and in contact with the gate insulating layer; forming a conductive layer covering the oxide semiconductor layer on and in contact with the oxide 25 semiconductor layer; forming a low-resistance material layer on and in contact with the conductive layer; forming a wiring protective layer on and in contact with the low-resistance material layer; forming a first wiring protective layer and a second wiring protective layer apart from each other with the gate electrode layer provided therebetween by processing the wiring protective layer; forming a first low-resistance 30 material layer and a second low-resistance material layer apart from each other with the gate electrode layer provided therebetween by processing the low-resistance material layer, the first low-resistance material layer being in contact with the first wiring

protective layer and the second low-resistance material layer being in contact with the second wiring protective layer; forming a resist pattern including an opening pattern portion in a region that is between the first low-resistance material layer and the second low-resistance material layer and overlaps with the oxide semiconductor layer; etching
5 the conductive layer using the resist pattern to separate the conductive layer into a first conductive layer and a second conductive layer; and filling an opening in the conductive layer with a protective layer.

[0020]

Through the above steps, the conductive layer for forming the source electrode
10 and the drain electrode can be provided with an opening with a minute pattern without the low-resistance material layer being removed during the processing of the conductive layer. Thus, a bottom-gate transistor with a short channel length can be manufactured.

[0021]

In the method for manufacturing a semiconductor device according to one
15 embodiment of the present invention, the thickness of the low-resistance material layer is not reduced and the surface of the low-resistance material layer is not damaged during the processing of the conductive layer for forming the source electrode and the drain electrode. Therefore, the wiring resistance of the low-resistance material layer is not increased. The low-resistance material layer can be used as a wiring for electrically
20 connecting the transistor to another semiconductor element. Thus, an integrated circuit which includes a semiconductor device manufactured by the method can operate at high speed because wiring delay due to high wiring resistance hardly occurs.

[0022]

Another embodiment of the present invention is a semiconductor device
25 including a gate electrode layer; a gate insulating layer on and in contact with the gate electrode layer; an oxide semiconductor layer being on and in contact with the gate insulating layer and overlapping with the gate electrode layer; a first conductive layer and a second conductive layer provided on and in contact with the oxide semiconductor layer apart from each other with the gate electrode layer provided therebetween; a first
30 low-resistance material layer on and in contact with the first conductive layer; a second low-resistance material layer on and in contact with the second conductive layer; a first protective layer on and in contact with the first conductive layer, the first low-resistance

material layer, the second conductive layer, and the second low-resistance material layer; and a second protective layer in contact with a part of the oxide semiconductor layer. In the semiconductor device, a distance between the first conductive layer and the second conductive layer is shorter than a distance between the first low-resistance
5 material layer and the second low-resistance material layer. The first conductive layer and the first low-resistance material layer serve as a source electrode and the second conductive layer and the second low-resistance material layer serve as a drain electrode.

[0023]

When the above structure is applied to a bottom-gate transistor including an
10 oxide semiconductor layer, the transistor can have a short channel length and thus can have high on-state current. Further, since an oxide semiconductor has higher electron mobility than amorphous silicon, a semiconductor device with high on-state current can be provided.

[0024]

15 Another embodiment of the present invention is a semiconductor device including a gate electrode layer; a gate insulating layer on and in contact with the gate electrode layer; an oxide semiconductor layer being on and in contact with the gate insulating layer and overlapping with the gate electrode layer; a first conductive layer and a second conductive layer provided on and in contact with the oxide semiconductor
20 layer apart from each other with the gate electrode layer provided therebetween; a first low-resistance material layer on and in contact with the first conductive layer; a second low-resistance material layer on and in contact with the second conductive layer; a first wiring protective layer on and in contact with the first low-resistance material layer; a second wiring protective layer on and in contact with the second low-resistance material
25 layer; and a protective layer on and in contact with the first conductive layer, the first wiring protective layer, the second conductive layer, and the second wiring protective layer and in contact with a part of the oxide semiconductor layer. In the semiconductor device, a distance between the first conductive layer and the second conductive layer is shorter than a distance between the first low-resistance material layer and the second
30 low-resistance material layer. The first conductive layer and the first low-resistance material layer serve as a source electrode and the second conductive layer and the second low-resistance material layer serve as a drain electrode.

[0025]

When the above structure is applied to a bottom-gate transistor including an oxide semiconductor layer, the transistor can have a short channel length and thus can have high on-state current. Further, since an oxide semiconductor has higher electron
5 mobility than amorphous silicon, a semiconductor device with high on-state current can be provided.

[0026]

The ends of the wiring protective layers on the channel side might be rounded through the processing for forming the conductive layers. In that case, the coverage
10 with the protective layer can be favorable as compared with the case where the ends are not rounded. The protective layer functions as a passivation film; thus, better coverage with the protective layer enables moisture or the like to be further prevented from entering from the outside. This is particularly effective in a transistor using an oxide semiconductor, whose electric characteristics are easily affected by moisture or the like
15 which enters from the outside.

[0027]

In any of the above semiconductor devices, the gate insulating layer is preferably flat.

[0028]

20 Planarization of a base insulating layer and the gate electrode layer can prevent non-coverage of the oxide semiconductor layer due to a step caused by the gate electrode layer. The planarization is particularly effective when the thickness of the oxide semiconductor layer is greater than or equal to 5 nm and less than or equal to 30 nm.

25 [0029]

In any of the above semiconductor devices, a width of the oxide semiconductor layer in a channel length direction is preferably larger than a width of the gate electrode layer in the channel length direction.

[0030]

30 In that case, the oxide semiconductor layer overlaps with the gate electrode layer in a large area, which enables the oxide semiconductor layer to be supplied with oxygen more easily from an insulating layer below the oxide semiconductor layer. As

a result, the initial electric characteristics (e.g., threshold voltage) and reliability in electric characteristics (e.g., threshold voltage) of the transistor can be improved.

[0031]

Moreover, oxygen vacancies are likely to be formed in the end of an island-shaped oxide semiconductor layer, and therefore carriers are more likely to be generated than in other regions thereof. Local generation of carriers in the oxide semiconductor layer, which is an active layer, causes degradation of electric characteristics (e.g., threshold voltage) of the transistor.

[0032]

Suppose that the width of the oxide semiconductor layer in the channel length direction is smaller than the width of the gate electrode layer in the channel length direction, that is, the end of the island-shaped oxide semiconductor layer is on the inner side than the end of the gate electrode layer, an electric field is concentrated on the end of the island-shaped oxide semiconductor layer upon application of a voltage between the gate electrode layer and the source electrode. Concentration of an electric field on the end of the island-shaped oxide semiconductor layer, where carriers are likely to be generated, leads to degradation of electric characteristics (e.g., threshold voltage) of the transistor. On the other hand, when the width of the oxide semiconductor layer in the channel length direction is larger than the width of the gate electrode layer in the channel length direction as in one embodiment of the present invention, the end of the island-shaped oxide semiconductor layer is on the outer side than the end of the gate electrode layer; thus, an electric field is not concentrated on the end of the island-shaped oxide semiconductor layer upon application of a voltage between the gate electrode layer and the source electrode. This can suppress degradation of electric characteristics (e.g., threshold voltage) of the transistor.

[0033]

According to one embodiment of the present invention, a bottom-gate transistor whose channel length is short (e.g., 30 nm) and in which an oxide semiconductor layer is used as an active layer can be manufactured. Further, a semiconductor device including the transistor as a component can be provided.

BRIEF DESCRIPTION OF DRAWINGS

[0034]

FIGS. 1A to 1C are a plan view and cross-sectional views illustrating one embodiment of the present invention.

FIGS. 2A-1 to 2A-3, 2B-1 to 2B-3, and 2C-1 to 2C-3 are plan views and cross-sectional views illustrating one embodiment of the present invention.

FIGS. 3A-1 to 3A-3, 3B-1 to 3B-3, and 3C-1 to 3C-3 are plan views and cross-sectional views illustrating one embodiment of the present invention.

FIGS. 4A-1 to 4A-3, 4B-1 to 4B-3, and 4C-1 to 4C-3 are plan views and cross-sectional views illustrating one embodiment of the present invention.

FIGS. 5A-1 to 5A-3, 5B-1 to 5B-3, and 5C-1 to 5C-3 are plan views and cross-sectional views illustrating one embodiment of the present invention.

FIGS. 6A-1 to 6A-3, 6B-1 to 6B-3, and 6C-1 to 6C-3 are plan views and cross-sectional views illustrating one embodiment of the present invention.

FIGS. 7A and 7B are a plan view and a cross-sectional view illustrating one embodiment of the present invention.

FIG. 8 is a circuit diagram illustrating one embodiment of the present invention.

FIGS. 9A to 9C are a plan view and cross-sectional views illustrating one embodiment of the present invention.

FIGS. 10A-1 to 10A-3, 10B-1 to 10B-3, and 10C-1 to 10C-3 are plan views and cross-sectional views illustrating one embodiment of the present invention.

FIGS. 11A-1 to 11A-3, 11B-1 to 11B-3, and 11C-1 to 11C-3 are plan views and cross-sectional views illustrating one embodiment of the present invention.

FIGS. 12A-1 to 12A-3 and 12B-1 to 12B-3 are plan views and cross-sectional views illustrating one embodiment of the present invention.

FIGS. 13A and 13B are a plan view and a cross-sectional view illustrating one embodiment of the present invention.

FIGS. 14A and 14B illustrate an example of a memory device.

FIG. 15 illustrates an example of a memory device.

FIG. 16 illustrates an example of a memory device.

FIGS. 17A to 17C illustrate an example of an electronic device.

BEST MODE FOR CARRYING OUT THE INVENTION

[0035]

Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the description below, and it is easily understood by those skilled in the art
5 that modes and details disclosed herein can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention is not construed as being limited to description of the embodiments.

[0036]

(Embodiment 1)

10 In this embodiment, one embodiment of a semiconductor device which can be manufactured according to the present invention will be described with reference to FIGS. 1A to 1C. FIG. 1A is a plan view of a transistor 440, FIG. 1B is a cross-sectional view taken along line A-A' in FIG. 1A, and FIG. 1C is a cross-sectional view taken along line B-B' in FIG. 1A. A channel length $L$ of the transistor 440 is greater than or
15 equal to 20 nm and less than or equal to 100 nm, preferably greater than or equal to 20 nm and less than or equal to 50 nm, more preferably greater than or equal to 20 nm and less than or equal to 30 nm. In this embodiment, the channel length $L$ is about 30 nm.

[0037]

The transistor 440 in FIGS. 1A to 1C is a bottom-gate transistor. The
20 transistor 440 illustrated in FIGS. 1A to 1C includes, over a base insulating layer 436 formed over a surface of a substrate 400, a gate electrode layer 401 provided so as to be buried in an insulating layer 432, a gate insulating layer 402 over the gate electrode layer 401, an oxide semiconductor layer 403 over the gate insulating layer 402, a first conductive layer 454a and a second conductive layer 454b over the oxide
25 semiconductor layer 403, a first low-resistance material layer 405a on and in contact with the first conductive layer 454a, a second low-resistance material layer 405b on and in contact with the second conductive layer 454b, a first protective layer 406 in contact with the first low-resistance material layer 405a, the second low-resistance material layer 405b, the first conductive layer 454a, and the second conductive layer 454b, a
30 hard mask layer 495 in contact with the first protective layer 406, and a second protective layer 407 over the hard mask layer 495.

[0038]

First, components will be described below.

[0039]

<Components of the Semiconductor Device>

(Substrate and base insulating layer)

5 As the substrate 400, a substrate having an insulating surface can be used; a substrate having at least heat resistance high enough to withstand heat treatment in a later step is preferable. For example, a glass substrate, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like can be used as the substrate 400. A single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of 10 silicon, silicon carbide, or the like; a compound semiconductor substrate made of silicon germanium or the like; an SOI substrate; or the like can be used as the substrate 400, or the substrate provided with a semiconductor element can be used as the substrate 400. Note that the concentration of impurities such as hydrogen or water in the substrate 400 is preferably low. This is for preventing diffusion of hydrogen or water into the oxide 15 semiconductor layer 403 so as to prevent degradation of the electric characteristics of the semiconductor device.

[0040]

As the base insulating layer 436, an oxide insulating layer of silicon oxide, silicon oxynitride, aluminum oxide, aluminum oxynitride, or the like or a nitride 20 insulating layer of silicon nitride, silicon nitride oxide, aluminum nitride, aluminum nitride oxide, or the like can be used, for example.

[0041]

(Gate electrode layer)

The gate electrode layer 401 can be formed using a metal material such as 25 molybdenum, titanium, tungsten, aluminum, or copper, for example. Alternatively, a semiconductor layer typified by a polycrystalline silicon layer doped with an impurity element such as phosphorus, or a silicide layer such as a nickel silicide layer may be used as the gate electrode layer 401. The gate electrode layer 401 may have either a single-layer structure or a stacked-layer structure.

30 [0042]

(Gate insulating layer)

The gate insulating layer 402 can be formed using silicon oxide, silicon

oxynitride, silicon nitride, or the like. The gate insulating layer 402 is preferably a silicon oxide layer containing oxygen in a proportion higher than that in the stoichiometric composition. The gate insulating layer 402 may be a single layer or a stack of two layers formed using any of the above materials. For example, silicon
5 nitride and silicon oxynitride, or silicon nitride and silicon oxide can be used.

[0043]

(Source electrode layer and drain electrode layer)

One of the source electrode layer and the drain electrode layer includes the first conductive layer 454a and the first low-resistance material layer 405a, and the other of
10 the source electrode layer and the drain electrode layer includes the second conductive layer 454b and the second low-resistance material layer 405b. The first conductive layer 454a and the second conductive layer 454b can be formed using a metal such as tungsten or molybdenum. Tungsten is especially preferred because the ratio of the etching rate of the first conductive layer 454a and the second conductive layer 454b to
15 that of the first protective layer 406 can be increased. A stack of aluminum and titanium, copper, or the like can be used for the first low-resistance material layer 405a and the second low-resistance material layer 405b. The stack of aluminum and titanium may be titanium, aluminum, and titanium stacked in this order. In the case of using copper for the first low-resistance material layer 405a and the second
20 low-resistance material layer 405b, titanium nitride or the like is preferably provided to prevent diffusion of copper into an adjacent layer.

[0044]

(Semiconductor layer)

A semiconductor that has a band gap wider than at least that of silicon, 1.1 eV,
25 can be used for a semiconductor layer of a transistor according to one embodiment of the present invention; an oxide semiconductor is preferably used. In this embodiment, the case where the oxide semiconductor layer 403 is used as the semiconductor layer is described.

[0045]

30 The thickness of the oxide semiconductor layer 403 is greater than or equal to 5 nm and less than or equal to 100 nm, preferably greater than or equal to 5 nm and less than or equal to 30 nm. The thickness is set such that the channel length of the

transistor is reduced while short-channel effect is suppressed.

[0046]

A material that can be used as the oxide semiconductor contains at least indium (In). In particular, In and zinc (Zn) are preferably contained. As a stabilizer for reducing variation in electric characteristics of a transistor using the oxide semiconductor, gallium (Ga) is preferably additionally contained. Tin (Sn) is preferably contained as a stabilizer. Hafnium (Hf) is preferably contained as a stabilizer. Aluminum (Al) is preferably contained as a stabilizer. Zirconium (Zr) is preferably contained as a stabilizer.

[0047]

As another stabilizer, one or plural kinds of lanthanoid such as lanthanum (La), cerium (Ce), praseodymium (Pr), neodymium (Nd), samarium (Sm), europium (Eu), gadolinium (Gd), terbium (Tb), dysprosium (Dy), holmium (Ho), erbium (Er), thulium (Tm), ytterbium (Yb), or lutetium (Lu) may be contained.

[0048]

As the oxide semiconductor, any of the following can be used: indium oxide, tin oxide, zinc oxide, an In-Zn-based oxide, an In-Mg-based oxide, an In-Ga-based oxide, an In-Ga-Zn-based oxide (also referred to as IGZO), an In-Al-Zn-based oxide, an In-Sn-Zn-based oxide, an In-Hf-Zn-based oxide, an In-La-Zn-based oxide, an In-Ce-Zn-based oxide, an In-Pr-Zn-based oxide, an In-Nd-Zn-based oxide, an In-Sm-Zn-based oxide, an In-Eu-Zn-based oxide, an In-Gd-Zn-based oxide, an In-Tb-Zn-based oxide, an In-Dy-Zn-based oxide, an In-Ho-Zn-based oxide, an In-Er-Zn-based oxide, an In-Tm-Zn-based oxide, an In-Yb-Zn-based oxide, an In-Lu-Zn-based oxide, an In-Sn-Ga-Zn-based oxide, an In-Hf-Ga-Zn-based oxide, an In-Al-Ga-Zn-based oxide, an In-Sn-Al-Zn-based oxide, an In-Sn-Hf-Zn-based oxide, or an In-Hf-Al-Zn-based oxide.

[0049]

Note that here, for example, an "In-Ga-Zn-based oxide" means an oxide containing In, Ga, and Zn as its main component and there is no particular limitation on the ratio of In: Ga: Zn. The In-Ga-Zn-based oxide may contain a metal element other than the In, Ga, and Zn.

[0050]

A material represented by $InMO_3(ZnO)_m$ ($m > 0$, where $m$ is not an integer) may be used as the oxide semiconductor. Note that M represents one or more metal elements selected from Ga, Fe, Mn, and Co. Alternatively, a material represented by $In_2SnO_5(ZnO)_n$ ($n > 0$, where $n$ is an integer) may be used as the oxide semiconductor.

5 [0051]

As the oxide semiconductor, an In-Ga-Zn-based oxide with an atomic ratio of In: Ga: Zn = 1:1:1 (= 1/3:1/3:1/3), In: Ga: Zn = 2:2:1 (= 2/5:2/5:1/5), or In: Ga: Zn = 3:1:2 (= 1/2:1/6:1/3), or an oxide with an atomic ratio close to the above atomic ratios can be used. Alternatively, an In-Sn-Zn-based oxide with an atomic ratio of In: Sn: Zn
10 = 1:1:1 (= 1/3:1/3:1/3), In: Sn: Zn = 2:1:3 (= 1/3:1/6:1/2), or In: Sn: Zn = 2:1:5 (= 1/4:1/8:5/8), or an oxide with an atomic ratio close to the above atomic ratios may be used.

[0052]

However, without limitation to the materials given above, a material with an
15 appropriate composition may be used as the oxide semiconductor containing indium depending on needed semiconductor characteristics (e.g., electric characteristics such as mobility and threshold voltage, and variation in the electric characteristics). In order to obtain the needed semiconductor characteristics, it is preferable that the carrier concentration, the impurity concentration, the defect density, the atomic ratio between a
20 metal element and oxygen, the interatomic distance, the density, and the like be set to appropriate values.

[0053]

For example, high mobility can be obtained relatively easily in the case of using an In-Sn-Zn-based oxide. However, mobility can be increased by reducing the
25 defect density in a bulk also in the case of using an In-Ga-Zn-based oxide.

[0054]

The oxide semiconductor layer 403 is in a single crystal state, a polycrystalline (also referred to as polycrystal) state, an amorphous state, or the like.

[0055]

30 It is preferable that the oxide semiconductor layer 403 be highly purified so as to hardly contain impurities such as copper, aluminum, or chlorine. In the process for

manufacturing the transistor, steps in which these impurities are not mixed or attached to the surface of the oxide semiconductor layer 403 are preferably selected as appropriate. In the case where the impurities are attached to the surface of the oxide semiconductor layer 403, the impurities on the surface of the oxide semiconductor layer 403 are preferably removed by exposure to oxalic acid, dilute hydrofluoric acid, or the like or by plasma treatment (such as $N_2O$ plasma treatment). Specifically, the copper concentration in the oxide semiconductor is lower than or equal to $1 \times 10^{18}$ atoms/cm$^3$, preferably lower than or equal to $1 \times 10^{17}$ atoms/cm$^3$. In addition, the aluminum concentration in the oxide semiconductor is lower than or equal to $1 \times 10^{18}$ atoms/cm$^3$. Further, the chlorine concentration in the oxide semiconductor is lower than or equal to $2 \times 10^{18}$ atoms/cm$^3$.

[0056]

The oxide semiconductor immediately after being deposited is preferably in a supersaturated state in which the proportion of oxygen is higher than that in the stoichiometric composition. For example, in the case where the oxide semiconductor is deposited using a sputtering method, the deposition is preferably performed under the condition where the proportion of oxygen in a deposition gas is high, in particular, in an oxygen atmosphere (oxygen gas: 100 %). When the deposition is performed under the condition where the proportion of oxygen in the deposition gas is high, particularly in a 100 % oxygen gas atmosphere, release of Zn from the film can be suppressed even at a deposition temperature higher than or equal to 300 °C, for example.

[0057]

The oxide semiconductor is preferably supersaturated with oxygen by sufficient removal of impurities such as hydrogen followed by sufficient supply with oxygen. Specifically, the hydrogen concentration in the oxide semiconductor is lower than or equal to $5 \times 10^{19}$ atoms/cm$^3$, preferably lower than or equal to $5 \times 10^{18}$ atoms/cm$^3$, further preferably lower than or equal to $5 \times 10^{17}$ atoms/cm$^3$. Note that the above hydrogen concentration in the oxide semiconductor is measured by secondary ion mass spectrometry (SIMS).

[0058]

(Protective layer)

The first protective layer 406 has a function of protecting the oxide semiconductor layer 403 from entry of moisture or the like from the outside. The first protective layer 406 can be formed using a silicon oxide film, a silicon oxynitride film, or an aluminum oxide film. The first protective layer 406 is preferably formed using a silicon oxide film, a silicon oxynitride film, or an aluminum oxide film containing much oxygen. In order to make the first protective layer contain much excess oxygen, oxygen may be added as appropriate to the first protective layer by an ion implantation method, an ion doping method, or plasma treatment.

[0059]

The second protective layer 407 has a function of protecting the oxide semiconductor layer 403 from entry of moisture or the like from the outside. The second protective layer 407 can be formed using a silicon oxide film, a silicon oxynitride film, or an aluminum oxide film. The second protective layer 407 is preferably formed using a silicon oxide film, a silicon oxynitride film, or an aluminum oxide film containing much oxygen. Alternatively, the second protective layer 407 may include two layers: a third protective layer 407a and a fourth protective layer 407b. The third protective layer 407a is formed in contact with the oxide semiconductor. The third protective layer 407a can be formed using an oxide semiconductor film containing gallium (Ga), a silicon oxide film, a silicon oxynitride film, or an aluminum oxide film which is deposited with conditions set as appropriate so as to contain much oxygen. The fourth protective layer 407b is formed in contact with the third protective layer 407a. The fourth protective layer 407b can be formed using a silicon oxide film, a silicon oxynitride film, or an aluminum oxide film containing much oxygen. In order to make the second protective layer contain much excess oxygen, oxygen may be added as appropriate to the second protective layer by an ion implantation method, an ion doping method, or plasma treatment.

[0060]

(Hard mask layer)

The hard mask layer 495 is preferably a film that is not easily etched under conditions for etching the first protective layer 406. This is because the hard mask layer 495 is used as a mask in the etching of the first protective layer 406. The hard mask layer 495 is preferably formed using amorphous silicon, which can be deposited

by a PCVD method or a sputtering method.

[0061]

<Method for Manufacturing Semiconductor Device>

A method for manufacturing the semiconductor device according to one
5 embodiment of the present invention is described with reference to FIGS. 2A-1 to 2A-3, 2B-1 to 2B-3, and 2C-1 to 2C-3; FIGS. 3A-1 to 3A-3, 3B-1 to 3B-3, and 3C-1 to 3C-3; FIGS. 4A-1 to 4A-3, 4B-1 to 4B-3, and 4C-1 to 4C-3; FIGS. 5A-1 to 5A-3, 5B-1 to 5B-3, and 5C-1 to 5C-3; and FIGS. 6A-1 to 6A-3, 6B-1 to 6B-3, and 6C-1 to 6C-3.

[0062]

10 FIGS. 2A-1 to 2A-3, 2B-1 to 2B-3, and 2C-1 to 2C-3 illustrate the steps from formation of the gate electrode layer 401 to oxygen doping of the oxide semiconductor layer 403.

[0063]

First, the substrate 400 is prepared, the base insulating layer 436 is formed over
15 the substrate 400, and the gate electrode layer 401 is formed over the base insulating layer 436 (see FIGS. 2A-1 to 2A-3).

[0064]

The gate electrode layer 401 is formed by depositing a material that can be used as a gate electrode using sputtering, for example, and then selectively etching part
20 of the material. Note that the etching may be dry etching, wet etching, or both dry etching and wet etching. The substrate 400 and the gate electrode layer 401 may be subjected to heat treatment after the formation of the gate electrode layer 401.

[0065]

Next, the insulating layer 432 is formed over the base insulating layer 436 and
25 the gate electrode layer 401. The insulating layer 432 is preferably planarized so that the gate electrode layer 401 is exposed and the insulating layer 432 and the gate electrode layer 401 are planarized (see FIGS. 2B-1 to 2B-3). As the planarization treatment, chemical mechanical polishing (CMP) treatment or the like may be performed.

30 [0066]

The insulating layer 432 and the gate electrode layer 401 are preferably planarized so that non-coverage of the oxide semiconductor layer 403, which is

described later, due to a step caused by the gate electrode layer 401 can be prevented.

[0067]

Next, the gate insulating layer 402 is formed over the gate electrode layer 401, and the oxide semiconductor layer 403 is formed over the gate insulating layer 402 (see
5 FIGS. 2C-1 to 2C-3).

[0068]

For example, for the gate insulating layer 402, a film of a material which can be used for the gate insulating layer 402 can be formed by a PCVD method.

[0069]

10 Note that before the oxide semiconductor layer 403 is formed, heat treatment may be performed for dehydration or dehydrogenation of the gate insulating layer 402. For example, heat treatment may be performed at a temperature higher than or equal to 350 °C and lower than or equal to 450 °C.

[0070]

15 In addition, oxygen may be supplied to the gate insulating layer 402 which has been dehydrated or dehydrogenated. Oxygen may be contained in the gate insulating layer 402, or in the gate insulating layer 402 and in the vicinity of an interface of the gate insulating layer 402. By the supply of oxygen to the gate insulating layer 402 after dehydration or dehydrogenation, the release of oxygen can be suppressed and the
20 concentration of oxygen in the gate insulating layer 402 can be increased. Oxygen can be supplied by oxygen doping treatment or the like.

[0071]

Note that in the case of performing heat treatment for supplying oxygen from the gate insulating layer 402 to the oxide semiconductor, the heat treatment is preferably
25 performed before the oxide semiconductor is processed into an island shape, in which case oxygen contained in the gate insulating layer 402 can be prevented from being released by the heat treatment.

[0072]

For example, the heat treatment is performed at a temperature higher than or
30 equal to 350 °C and lower than the strain point of the substrate, preferably higher than or equal to 350 °C and lower than or equal to 450 °C. Heat treatment may be further

performed in a later step. As a heat treatment apparatus for the heat treatment, for example, an electric furnace or an apparatus for heating an object by heat conduction or heat radiation from a heater such as a resistance heater can be used; for example, a rapid thermal annealing (RTA) apparatus such as a gas rapid thermal annealing (GRTA)
5 apparatus or a lamp rapid thermal annealing (LRTA) apparatus can be used.

[0073]

Further, after the heat treatment is performed and while the heating temperature is being maintained or being decreased, a high-purity oxygen gas, a high-purity $N_2O$ gas, or ultra-dry air (having a dew point of –40 °C or lower, preferably –60 °C or lower)
10 may be introduced into the furnace where the heat treatment has been performed. It is preferable that the oxygen gas or the $N_2O$ gas do not contain water, hydrogen, and the like. The purity of the oxygen gas or the $N_2O$ gas which is introduced into the heat treatment apparatus is preferably 6N or higher, further preferably 7N or higher; that is, the impurity concentration in the oxygen gas or the $N_2O$ gas is preferably 1 ppm or
15 lower, further preferably 0.1 ppm or lower. By the action of the oxygen gas or the $N_2O$ gas, oxygen is supplied to the oxide semiconductor, and defects due to oxygen vacancies in the oxide semiconductor can be reduced. Note that the high-purity oxygen gas, high-purity $N_2O$ gas, or ultra-dry air may be introduced during the heat treatment.

20 [0074]

Further, oxygen doping 451 is performed on the oxide semiconductor (see FIGS. 2C-1 to 2C-3). This is for supplying oxygen to the oxide semiconductor to fill oxygen vacancies in the oxide semiconductor. Filling the oxygen vacancies makes the semiconductor device less likely to exhibit abnormal initial electric characteristics (e.g.,
25 threshold voltage) and improves its reliability in electric characteristics (e.g., threshold voltage).

[0075]

The oxygen doping 451 can be performed by an ion implantation method, an ion doping method, a plasma immersion ion implantation method, plasma treatment, or
30 the like. By use of such methods, the oxide semiconductor can be doped with oxygen (an oxygen radical, an oxygen atom, an oxygen molecule, ozone, an oxygen ion (an oxygen molecular ion), and/or an oxygen cluster ion).

[0076]

FIGS. 3A-1 to 3A-3, 3B-1 to 3B-3, and 3C-1 to 3C-3 illustrate the steps from processing of the oxide semiconductor layer 403 into an island shape to formation of a resist 453 for forming the first low-resistance material layer 405a and the second low-resistance material layer 405b.

[0077]

The oxide semiconductor layer 403 is processed into an island-shaped oxide semiconductor layer 403 by a photolithography step (see FIGS. 3A-1 to 3A-3).

[0078]

The etching of the oxide semiconductor layer 403 may be dry etching, wet etching, or both dry etching and wet etching.

[0079]

Note that the width of the oxide semiconductor layer in the channel length direction is preferably larger than the width of the gate electrode layer in the channel length direction. In that case, the oxide semiconductor layer overlaps with the gate electrode layer in a large area, which enables the oxide semiconductor layer to be supplied with oxygen more easily from an insulating layer below the oxide semiconductor layer. As a result, the initial electric characteristics (e.g., threshold voltage) and reliability in electric characteristics (e.g., threshold voltage) of the transistor can be improved.

[0080]

Next, a conductive layer 454 is formed in contact with the oxide semiconductor layer 403. The conductive layer 454 may be formed by a sputtering method or the like (see FIGS. 3B-1 to 3B-3).

[0081]

Then, a low-resistance material layer 405 is formed in contact with the conductive layer 454. The low-resistance material layer 405 may be formed by a sputtering method or the like.

[0082]

Next, the resist 453 is formed by a photolithography step (see FIGS. 3C-1 to 3C-3).

[0083]

FIGS. 4A-1 to 4A-3, 4B-1 to 4B-3, and 4C-1 to 4C-3 illustrate the steps from processing of the low-resistance material layer 405 to planarization of the first protective layer 406.

[0084]

5 The low-resistance material layer 405 is selectively etched using the resist 453 as a mask; thus, the low-resistance material layer 405a and the low-resistance material layer 405b are formed (see FIGS. 4A-1 to 4A-3). The conditions for etching the low-resistance material layer 405 are set such that the conductive layer 454 is not easily etched. This is because an opening is formed in the conductive layer 454 in a later step 10 with the use of the hard mask layer 495 as a mask.

[0085]

Next, a region of the conductive layer 454 which is not in contact with the oxide semiconductor layer 403 is etched (see FIGS. 4B-1 to 4B-3).

[0086]

15 Then, the first protective layer 406 is formed and planarized by CMP (see FIGS. 4C-1 to 4C-3). The surface of the first protective layer 406 is planarized so that, even when a resist as thin as about 30 nm is applied thereon, no region is formed which cannot be covered with the resist owing to a step on the surface where the resist is to be applied.

20 [0087]

FIGS. 5A-1 to 5A-3, 5B-1 to 5B-3, and 5C-1 to 5C-3 illustrate the steps for forming the hard mask layer 495.

[0088]

The hard mask layer 495 is formed over the planarized first protective layer 25 406 (see FIGS. 5A-1 to 5A-3). The hard mask layer 495 is preferably a film that is not easily etched under conditions for etching the first protective layer 406. This is because the hard mask layer 495 is used as a mask in the etching of the first protective layer 406.

[0089]

30 Next, a resist is formed over the hard mask layer 495 and subjected to exposure to an electron beam; thus, a resist 455 is formed (see FIGS. 5B-1 to 5B-3).

[0090]

Here, the thickness of the resist is preferably set such that the ratio of the thickness of the resist to the width of the manufactured pattern becomes 1:1 to 1:2. For example, in the case where the width of the pattern is 30 nm, the thickness of the resist is set within 30 nm to 60 nm.

5 [0091]

The surface of the hard mask layer 495 is flat. Therefore, even a resist as thin as about 30 nm can be uniformly applied on the surface where the resist is to be applied.

[0092]

Next, the hard mask layer 495 is etched (see FIGS. 5C-1 to 5C-3). The etching method is preferably dry etching. The resist may be removed after the hard mask layer 495 is etched. In this embodiment, the hard mask layer 495 includes an opening which overlaps with a channel formation region of the oxide semiconductor layer 403.

10

[0093]

15

FIGS. 6A-1 to 6A-3, 6B-1 to 6B-3, and 6C-1 to 6C-3 illustrate the steps from formation of an opening in the first protective layer 406 to formation of an opening in the conductive layer 454.

[0094]

The first protective layer 406 is etched (see FIGS. 6A-1 to 6A-3). The conditions for etching the first protective layer 406 are preferably set such that the ratio of the etching rate of the first protective layer 406 to that of the hard mask layer 495 is high. This is for forming an opening with a width (width in the channel length direction) of about 30 nm in the first protective layer 406 with the use of the hard mask layer 495 as a mask.

20

25 [0095]

Next, the conductive layer 454 is etched, so that the first conductive layer 454a and the second conductive layer 454b are formed. A channel is to be formed between the first conductive layer 454a and the second conductive layer 454b (see FIGS. 6B-1 to 6B-3). The conditions for etching the conductive layer 454 are preferably set such that the ratio of the etching rate of the conductive layer 454 to that of the oxide semiconductor layer 403 is high. This is for preventing the surface of the oxide semiconductor layer 403 from being damaged by the etching.

30

[0096]

In the case of forming an opening with a width (width in the channel length direction) of about 30 nm, the resist 455 is as thin as 30 nm to 60 nm. Therefore, the resist 455 is removed during the etching of the first protective layer 406 and the conductive layer 454. However, since the hard mask layer 495 serves as a mask, an opening with a width of about 30 nm can be formed in the conductive layer 454 even though the resist 455 is removed.

[0097]

Next, the opening formed in the conductive layer 454 in the above step is covered with the second protective layer 407 (see FIGS. 6C-1 to 6C-3). A film which can prevent entry of moisture, hydrogen, or the like into the oxide semiconductor layer 403 is preferably used as the second protective layer 407. For example, a silicon oxide film, a silicon oxynitride film, a silicon nitride film, an aluminum oxide film, or the like can be used.

[0098]

The second protective layer 407 preferably contains excess oxygen. The as-deposited second protective layer 407 may contain excess oxygen, or the second protective layer 407 may be subjected to oxygen doping. For example, the doping with oxygen (an oxygen radical, an oxygen atom, an oxygen molecule, ozone, an oxygen ion (an oxygen molecular ion), and/or an oxygen cluster ion) can be performed by an ion implantation method, an ion doping method, a plasma immersion ion implantation method, plasma treatment, or the like. For the ion implantation method, a gas cluster ion beam may be used.

[0099]

After the second protective layer 407 is formed, heat treatment may be performed. For example, heat treatment is performed at 250 °C for one hour in a nitrogen atmosphere.

[0100]

Through the above steps, the transistor 440 can be manufactured. The channel length $L$ of the transistor 440 manufactured at that time is about 30 nm. Therefore, the transistor 440 can have high on-state current.

[0101]

The above is the method for manufacturing the semiconductor device according to one embodiment of the present invention.

[0102]

Through the above method for manufacturing a semiconductor device, a bottom-gate transistor in which the oxide semiconductor layer 403 is used as an active layer and whose channel length is about 30 nm can be manufactured.

[0103]

(Embodiment 2)

In this embodiment, one embodiment of a semiconductor device will be described with reference to FIGS. 7A and 7B. FIG. 7A is a plan view of a transistor 420, and FIG. 7B is a cross-sectional view taken along line X-Y in FIG. 7A. Note that in FIG. 7A, some components of the transistor 420 (e.g., the gate insulating layer 402) are not illustrated for simplicity. A channel length *L* of the transistor 420 is greater than or equal to 20 nm and less than or equal to 100 nm, preferably greater than or equal to 20 nm and less than or equal to 50 nm, more preferably greater than or equal to 20 nm and less than or equal to 30 nm. In this embodiment, the channel length *L* is about 30 nm.

[0104]

The transistor 420 illustrated in FIGS. 7A and 7B includes, over the base insulating layer 436 formed over a surface of the substrate 400, the gate electrode layer 401 provided so as to be buried in the insulating layer 432, the gate insulating layer 402 over the gate electrode layer 401, the oxide semiconductor layer 403 over the gate insulating layer 402, the first conductive layer 454a and the second conductive layer 454b over the oxide semiconductor layer 403, the first low-resistance material layer 405a on and in contact with the first conductive layer 454a, the second low-resistance material layer 405b on and in contact with the second conductive layer 454b, the first protective layer 406 in contact with the first low-resistance material layer 405a, the second low-resistance material layer 405b, the first conductive layer 454a, and the second conductive layer 454b, the hard mask layer 495 in contact with the first protective layer 406, and the second protective layer 407 over the hard mask layer 495.

[0105]

Embodiment 1 can be referred to for the structure and manufacturing method of

the semiconductor device described in this embodiment.

[0106]

(Circuit which can be provided over the substrate 400)

The substrate 400 is provided with a semiconductor element, which is not illustrated here for simplicity. Wiring layers 474a and 474b and the base insulating layer 436 covering the wiring layers 474a and 474b are provided over the substrate 400, part of which is a component of a memory illustrated in FIG. 8. FIG. 8 illustrates an example of an equivalent circuit, showing a connection between the transistor 420 and a transistor 431 formed using the substrate 400.

[0107]

A capacitor 430 is a capacitor in which the source electrode layer or the drain electrode layer, which includes stacked layers, and the wiring layer 474a serve as a pair of electrodes and the base insulating layer 436 and the gate insulating layer 402, which includes stacked layers, serve as a dielectric.

[0108]

In the memory configuration illustrated in FIG. 8, writing to the memory is performed by injection of charge into the capacitor 430. The transistor described in this embodiment has a channel length about 30 nm, and thus has high on-state current. Therefore, writing to the memory can be performed at high speed.

[0109]

The memory configuration illustrated in FIG. 8 has the advantages of being capable of holding stored data even when not powered and having an unlimited number of write cycles. This is because, since the transistor described in this embodiment has low off-state current, the charge stored in the capacitor 430 is not easily released.

[0110]

(Embodiment 3)

In this embodiment, one embodiment of a semiconductor device which can be manufactured according to the present invention will be described with reference to FIGS. 9A to 9C. FIG. 9A is a plan view of a transistor 441, FIG. 9B is a cross-sectional view taken along line A-A' in FIG. 9A, and FIG. 9C is a cross-sectional view taken along line B-B' in FIG. 9A. Note that in FIG. 9A, some components of the transistor 441 (e.g., the gate insulating layer 402) are not illustrated for simplicity. A channel

length $L$ of the transistor 441 is greater than or equal to 20 nm and less than or equal to 100 nm, preferably greater than or equal to 20 nm and less than or equal to 50 nm, more preferably greater than or equal to 20 nm and less than or equal to 30 nm. In this embodiment, the channel length $L$ is about 30 nm.

5 [0111]

The transistor 441 in FIGS. 9A to 9C is a bottom-gate transistor. The transistor 441 illustrated in FIGS. 9A to 9C includes the substrate 400, the base insulating layer 436, the insulating layer 432, the gate electrode layer 401, the gate insulating layer 402, the oxide semiconductor layer 403, the first conductive layer 454a, 10 the second conductive layer 454b, the first low-resistance material layer 405a, the second low-resistance material layer 405b, a first wiring protective layer 485a, a second wiring protective layer 485b, and the first protective layer 406.

[0112]

The base insulating layer 436 is provided in contact with a surface of the 15 substrate 400. The insulating layer 432 is in contact with the base insulating layer 436. The gate electrode layer 401 is buried in the insulating layer 432. The gate insulating layer 402 is provided on and in contact with the gate electrode layer 401. The oxide semiconductor layer 403 is provided on and in contact with the gate insulating layer 402. The first conductive layer 454a and the second conductive layer 454b are provided on 20 and in contact with the oxide semiconductor layer 403. The first low-resistance material layer 405a is provided on and in contact with the first conductive layer 454a. The second low-resistance material layer 405b is provided on and in contact with the second conductive layer 454b. The first wiring protective layer 485a is provided on and in contact with the first low-resistance material layer 405a. The second wiring 25 protective layer 485b is provided on and in contact with the second low-resistance material layer 405b. The first protective layer 406 is provided in contact with the first conductive layer 454a, the second conductive layer 454b, the first wiring protective layer 485a, the second wiring protective layer 485b, and the oxide semiconductor layer 403.

30 [0113]

First, components will be described below.

[0114]

<Components of the Semiconductor Device>

Embodiment 1 can be referred to for details of the substrate, the base insulating layer, the gate electrode layer, the gate insulating layer, the source electrode layer, the drain electrode layer, the oxide semiconductor layer, and the protective layer.

5 [0115]

(Wiring protective layer)

A wiring protective layer 485 is preferably a film that is not easily etched under conditions for etching the conductive layer 454. The first low-resistance material layer 405a and the second low-resistance material layer 405b are used as lead wirings for 10 connecting transistors; therefore, the low-resistance material layer 405 has a thickness greater than or equal to 100 nm. This means that the difference in height between the surface of the low-resistance material layer 405 and the surface of the conductive layer 454 is at least greater than or equal to 100 nm. Without the wiring protective layer 485, the end of the low-resistance material layer 405 is not covered with a resist, or covered 15 with a thin resist even if covered; thus, the low-resistance material layer 405 is damaged by the etching for processing the conductive layer 454. In order to prevent that damage, the wiring protective layer 485 which is not easily etched under conditions for etching the conductive layer 454 is provided over the low-resistance material layer 405 to prevent the low-resistance material layer 405 from being etched. The wiring 20 protective layer 485 is preferably formed using silicon oxide, silicon nitride, silicon oxynitride, or aluminum oxide. Silicon oxide, silicon nitride, and silicon oxynitride can be deposited by a PCVD method or a sputtering method. Aluminum oxide can be deposited by a sputtering method.

[0116]

25 <Method for Manufacturing Semiconductor Device>

A method for manufacturing the semiconductor device according to one embodiment of the present invention is described with reference to FIGS. 2A-1 to 2A-3, 2B-1 to 2B-3, and 2C-1 to 2C-3; FIGS. 10A-1 to 10A-3, 10B-1 to 10B-3, and 10C-1 to 10C-3; FIGS. 11A-1 to 11A-3, 11B-1 to 11B-3, and 11C-1 to 11C-3; and FIGS. 12A-1 30 to 12A-3 and 12B-1 to 12B-3.

[0117]

FIGS. 2A-1 to 2A-3, 2B-1 to 2B-3, and 2C-1 to 2C-3 illustrate the steps from

formation of the gate electrode layer 401 to oxygen doping of the oxide semiconductor layer 403. Embodiment 1 can be referred to for these steps.

[0118]

FIGS. 10A-1 to 10A-3, 10B-1 to 10B-3, and 10C-1 to 10C-3 illustrate the steps from processing of the oxide semiconductor layer 403 into an island shape to formation of the resist 453 for forming the low-resistance material layer 405 and the wiring protective layer 485.

[0119]

The oxide semiconductor layer 403 is processed into an island-shaped oxide semiconductor layer 403 by a photolithography step (see FIGS. 10A-1 to 10A-3). Refer to Embodiment 1 for details.

[0120]

Next, the conductive layer 454 is formed in contact with the oxide semiconductor layer 403. The conductive layer 454 may be formed by a sputtering method or the like. Then, the low-resistance material layer 405 is formed in contact with the conductive layer 454. The low-resistance material layer 405 may be formed by a sputtering method or the like. Then, the wiring protective layer 485 is formed in contact with the low-resistance material layer 405. The wiring protective layer 485 may be formed by a sputtering method or the like (see FIGS. 10B-1 to 10B-3).

[0121]

Next, the resist 453 is formed by a photolithography step (see FIGS. 10C-1 to 10C-3).

[0122]

FIGS. 11A-1 to 11A-3, 11B-1 to 11B-3, and 11C-1 to 11C-3 illustrate the steps from processing of the wiring protective layer 485 and the low-resistance material layer 405 to formation of the resist 455 for forming the first conductive layer 454a and the second conductive layer 454b.

[0123]

The wiring protective layer 485 and the low-resistance material layer 405 are selectively etched using the resist 453 as a mask; thus, the first wiring protective layer 485a, the second wiring protective layer 485b, the first low-resistance material layer 405a, and the second low-resistance material layer 405b are formed (see FIGS. 11A-1 to

11A-3). The wiring protective layer 485 and the low-resistance material layer 405 may be processed using the same resist pattern, or may be processed by forming their respective resist patterns. The wiring protective layer 485 and the low-resistance material layer 405 are preferably etched under conditions such that the conductive layer 5 454 is not easily etched.

[0124]

Next, a region of the conductive layer 454 which is not in contact with the oxide semiconductor layer 403 is etched (see FIGS. 11B-1 to 11B-3).

[0125]

10 Next, a resist is formed over the conductive layer 454, the first wiring protective layer 485a, and the second wiring protective layer 485b. Here, the thickness of the resist is preferably set such that the ratio of the thickness of the resist to the width of the manufactured pattern becomes 1:1 to 1:2. For example, in the case where the width of the pattern is 30 nm, the thickness of the resist is set within 30 nm to 60 nm. 15 The resist is subjected to exposure to an electron beam, so that the resist 455 is formed (see FIGS. 11C-1 to 11C-3).

[0126]

The first low-resistance material layer 405a and the second low-resistance material layer 405b can be used as lead wirings for connecting transistors. High 20 wiring resistance of a lead wiring causes a problem of wiring delay in an integrated circuit; thus, the wiring resistance needs to be lowered. Therefore, the low-resistance material layer 405 needs a thickness greater than or equal to 100 nm in general. This means that the difference in height between the surface of the low-resistance material layer 405 and the surface of the conductive layer 454 is at least greater than or equal to 25 100 nm. Without the wiring protective layer 485 over the low-resistance material layer 405, the ends of the first low-resistance material layer 405a and the second low-resistance material layer 405b are not covered with a resist, or covered with a thin resist even if covered; thus, the first low-resistance material layer 405a and the second low-resistance material layer 405b are etched at the time of processing the conductive 30 layer 454. However, in the manufacturing method according to one embodiment of the present invention, the wiring protective layer 485 which is not easily etched under conditions for etching the conductive layer 454 is provided on and in contact with the

low-resistance material layer 405, so that the first low-resistance material layer 405a and the second low-resistance material layer 405b are not reduced in thickness and the surfaces thereof are not damaged in the processing of the conductive layer 454; thus, an increase in wiring resistance is prevented. Therefore, wiring delay is less likely to
5 occur in an integrated circuit which includes a semiconductor device manufactured by the manufacturing method.

[0127]

FIGS. 12A-1 to 12A-3 and 12B-1 to 12B-3 illustrate the steps from processing of the conductive layer 454 to formation of the first protective layer 406.

10 [0128]

The conductive layer 454 is etched using the resist 455 as a mask, so that the first conductive layer 454a and the second conductive layer 454b are formed. A channel is to be formed between the first conductive layer 454a and the second conductive layer 454b (see FIGS. 12A-1 to 12A-3).

15 [0129]

The conditions for etching the conductive layer 454 are preferably set such that the ratio of the etching rate of the conductive layer 454 to that of the oxide semiconductor layer 403 is high. This is for preventing the surface of the oxide semiconductor layer 403 from being damaged by the etching.

20 [0130]

In the case of forming an opening with a width of about 30 nm, the resist 455 is as thin as 30 nm to 60 nm; thus, a region which cannot be covered with a resist may be formed at the ends of the first wiring protective layer 485a and the second wiring protective layer 485b, for example. Accordingly, there may be a region where the
25 resist 455 is removed during the etching of the conductive layer 454 or a region which is etched without being covered with a resist. However, in a region which is less likely to be covered with a resist, for example, at the ends of the first wiring protective layer 485a and the second wiring protective layer 485b, the first low-resistance material layer 405a and the second low-resistance material layer 405b are not etched even when the
30 resist 455 is removed because the first wiring protective layer 485a and the second wiring protective layer 485b protect the low-resistance material layers.

[0131]

Next, the opening formed in the conductive layer 454 in the above step is covered with the first protective layer 406 (see FIGS. 12B-1 to 12B-3). A film which can prevent entry of moisture, hydrogen, or the like into the oxide semiconductor layer 403 is preferably used as the first protective layer 406. For example, a silicon oxide film, a silicon oxynitride film, a silicon nitride film, an aluminum oxide film, or the like can be used.

[0132]

The first protective layer 406 preferably contains excess oxygen. For example, the first protective layer 406 is preferably formed using a silicon oxide film, a silicon oxynitride film, or an aluminum oxide film containing much oxygen. Alternatively, the first protective layer 406 may include two layers. The first layer provided in contact with the oxide semiconductor can be formed using an oxide semiconductor film containing gallium (Ga), a silicon oxide film, a silicon oxynitride film, or an aluminum oxide film which is deposited with conditions set as appropriate so as to contain much oxygen. The second layer can be formed using a silicon oxide film, a silicon oxynitride film, or an aluminum oxide film containing much oxygen. In order to make the first protective layer 406 contain much excess oxygen, oxygen may be added as appropriate to the first protective layer 406 by an ion implantation method, an ion doping method, or plasma treatment.

[0133]

After the first protective layer 406 is formed, heat treatment may be performed. For example, heat treatment is performed at 250 °C for one hour in a nitrogen atmosphere.

[0134]

Through the above steps, the transistor 441 can be manufactured. The channel length $L$ of the transistor 441 manufactured at that time is about 30 nm. Therefore, the transistor 441 can have high on-state current.

[0135]

The above is the method for manufacturing the semiconductor device according to one embodiment of the present invention.

[0136]

The structures, methods, and the like described in this embodiment can be

combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0137]

(Embodiment 4)

5 In this embodiment, one embodiment of a semiconductor device will be described with reference to FIGS. 13A and 13B. FIG. 13A is a plan view of a transistor 421, and FIG. 13B is a cross-sectional view taken along line X-Y in FIG. 13A. Note that in FIG. 13A, some components of the transistor 421 (e.g., the gate insulating layer 402) are not illustrated for simplicity. A channel length $L$ of the transistor 421 is 10 greater than or equal to 20 nm and less than or equal to 100 nm, preferably greater than or equal to 20 nm and less than or equal to 50 nm, more preferably greater than or equal to 20 nm and less than or equal to 30 nm. In this embodiment, the channel length $L$ is about 30 nm.

[0138]

15 The transistor 421 illustrated in FIGS. 13A and 13B includes the substrate 400, the base insulating layer 436, the insulating layer 432, the gate electrode layer 401, the gate insulating layer 402, the oxide semiconductor layer 403, the first conductive layer 454a, the second conductive layer 454b, the first low-resistance material layer 405a, the second low-resistance material layer 405b, the first wiring protective layer 485a, the 20 second wiring protective layer 485b, and the first protective layer 406.

[0139]

The base insulating layer 436 is provided in contact with a surface of the substrate 400. The insulating layer 432 is in contact with the base insulating layer 436. The gate electrode layer 401 is buried in the insulating layer 432. The gate insulating 25 layer 402 is provided on and in contact with the gate electrode layer 401. The oxide semiconductor layer 403 is provided on and in contact with the gate insulating layer 402. The first conductive layer 454a and the second conductive layer 454b are provided on and in contact with the oxide semiconductor layer 403. The first low-resistance material layer 405a is provided on and in contact with the first conductive layer 454a. 30 The second low-resistance material layer 405b is provided on and in contact with the second conductive layer 454b. The first wiring protective layer 485a is provided on and in contact with the first low-resistance material layer 405a. The second wiring

protective layer 485b is provided on and in contact with the second low-resistance material layer 405b. The first protective layer 406 is provided in contact with the first conductive layer 454a, the second conductive layer 454b, the first wiring protective layer 485a, the second wiring protective layer 485b, and the oxide semiconductor layer
5 403.

[0140]

Embodiment 3 can be referred to for the structure and manufacturing method of the semiconductor device described in this embodiment.

[0141]

10 (Embodiment 5)

In this embodiment, a c-axis aligned crystalline oxide semiconductor (CAAC-OS) film, which can be used as the oxide semiconductor layer 403 exemplified in Embodiments 1 and 3, will be described.

[0142]

15 The CAAC-OS film is not completely single crystal nor completely amorphous. The CAAC-OS film is an oxide semiconductor film with a crystal-amorphous mixed phase structure where crystal parts are included in an amorphous phase. Note that in most cases, the crystal part fits inside a cube whose one side is less than 100 nm. From an observation image obtained with a transmission electron microscope (TEM), a
20 boundary between an amorphous part and a crystal part in the CAAC-OS film is not clear. Further, with the TEM, a grain boundary in the CAAC-OS film is not found. Thus, in the CAAC-OS film, a reduction in electron mobility due to the grain boundary is suppressed.

[0143]

25 In each of the crystal parts included in the CAAC-OS film, the c-axis is aligned in a direction perpendicular to a surface where the CAAC-OS film is formed or a surface of the CAAC-OS film, triangular or hexagonal atomic arrangement which is seen from the direction perpendicular to the a-b plane is formed, and metal atoms are arranged in a layered manner or metal atoms and oxygen atoms are arranged in a
30 layered manner when seen from the direction perpendicular to the c-axis. Note that, among crystal parts, the directions of the a-axis and the b-axis of one crystal part may be different from those of another crystal part. In this specification and the like, a

simple term "perpendicular" includes a range from 85° to 95°.

[0144]

In the CAAC-OS film, distribution of crystal parts is not necessarily uniform. For example, in the formation process of the CAAC-OS film, in the case where crystal growth occurs from a surface side of the oxide semiconductor film, the proportion of crystal parts in the vicinity of the surface of the oxide semiconductor film is higher than that in the vicinity of the surface where the oxide semiconductor film is formed in some cases.

[0145]

Since the c-axes of the crystal parts included in the CAAC-OS film are aligned in the direction perpendicular to the surface where the CAAC-OS film is formed or a surface of the CAAC-OS film, the directions of the c-axes may be different from each other depending on the shape of the CAAC-OS film (the cross-sectional shape of the surface where the CAAC-OS film is formed or the cross-sectional shape of the surface of the CAAC-OS film). Note that when the CAAC-OS film is formed, the direction of the c-axis of the crystal part is the direction perpendicular to the surface where the CAAC-OS film is formed or the surface of the CAAC-OS film. The crystal part is formed by deposition or by performing treatment for crystallization such as heat treatment after deposition.

[0146]

In an oxide semiconductor having a crystal part such as the CAAC-OS, defects in the bulk can be further reduced and when the surface flatness of the oxide semiconductor is improved, mobility higher than that of an oxide semiconductor in an amorphous state can be obtained. In order to improve the surface flatness, the oxide semiconductor is preferably formed over a flat surface. Specifically, the oxide semiconductor may be formed over a surface with an average surface roughness ($R_a$) of less than or equal to 1 nm, preferably less than or equal to 0.3 nm, further preferably less than or equal to 0.1 nm. Since the transistor 440 is a bottom-gate transistor, it is possible to improve the planarity of the surface where the oxide semiconductor layer 403 is to be formed by performing planarization treatment such as CMP treatment after the formation of the gate electrode layer 401 and the base insulating layer 436 to obtain the above flat surface.

[0147]

When the CAAC-OS film is used as the oxide semiconductor layer 403 in a transistor, change in electric characteristics (e.g., threshold voltage) of the transistor due to irradiation with visible light or ultraviolet light can be reduced. Thus, the transistor
5 has high reliability.

[0148]

(Embodiment 6)

In this embodiment, an example of a semiconductor device (memory device) which includes the transistor described in this specification, which can hold stored data
10 even when not powered, and which has an unlimited number of write cycles will be described with reference to drawings.

[0149]

FIGS. 14A and 14B illustrate an example of a structure of the semiconductor device. FIG. 14A is a cross-sectional view of the semiconductor device, and FIG. 14B
15 is a circuit diagram of the semiconductor device.

[0150]

The semiconductor device illustrated in FIGS. 14A and 14B includes a transistor 3200 including a first semiconductor material in a lower portion, and a transistor 3202 including a second semiconductor material in an upper portion. The
20 structure of the transistor 440 described in Embodiment 1 is applied to the transistor 3202.

[0151]

Here, the first semiconductor material and the second semiconductor material are preferably materials having different band gaps. For example, the first
25 semiconductor material can be a semiconductor material (such as silicon) other than a wide band gap semiconductor, and the second semiconductor material can be a wide band gap semiconductor. A transistor including a material other than a wide band gap semiconductor can operate at high speed easily. On the other hand, a transistor including a wide band gap semiconductor enables charge to be held for a long time
30 owing to its characteristics.

[0152]

Although both of the above transistors are n-channel transistors in the

following description, it is needless to say that p-channel transistors can be used. The specific structure of the semiconductor device, such as the material used for the semiconductor device and the structure of the semiconductor device, is not necessarily limited to those described here except for the use of the transistor described in any of Embodiments 1 to 4, which is formed using a wide band gap semiconductor for holding data.

[0153]

The transistor 3200 in FIG. 14A includes a channel formation region provided in a substrate 3000 including a semiconductor material (such as silicon), impurity regions provided such that the channel formation region is sandwiched therebetween, intermetallic compound regions provided in contact with the impurity regions, a gate insulating layer provided over the channel formation region, and a gate electrode layer provided over the gate insulating layer. Note that a transistor whose source electrode layer and drain electrode layer are not illustrated in a drawing may be referred to as a transistor for the sake of convenience. Further, in such a case, in description of a connection of a transistor, a source region and a source electrode layer may be collectively referred to as a source electrode layer, and a drain region and a drain electrode layer may be collectively referred to as a drain electrode layer. That is, in this specification, the term "source electrode layer" may include a source region.

[0154]

Further, an element isolation insulating layer 3106 is formed on the substrate 3000 so as to surround the transistor 3200, and an insulating layer 3220 is formed so as to cover the transistor 3200.

[0155]

The transistor 3200 formed using a single crystal semiconductor substrate can operate at high speed. Thus, when the transistor is used as a reading transistor, data can be read at a high speed. As treatment prior to formation of the transistor 3202 and a capacitor 3204, CMP treatment is performed on the insulating layer 3220 covering the transistor 3200, whereby the insulating layer 3220 is planarized and, at the same time, an upper surface of the gate electrode layer of the transistor 3200 is exposed.

[0156]

The transistor 3202 shown in FIG. 14A is a bottom-gate transistor including a

wide band gap semiconductor in the channel formation region. Here, an oxide semiconductor layer included in the transistor 3202 is preferably highly purified. By using a highly purified oxide semiconductor layer, the transistor 3202 which has extremely favorable off-state characteristics can be obtained.

5 [0157]

FIG. 14B shows an example of a semiconductor memory device which includes the transistor 3202. When a transistor with low off-state current is used as the transistor 3202, stored data can be held for a long time in the semiconductor memory device. In other words, refresh operation becomes unnecessary or the frequency of the

10 refresh operation can be extremely lowered, which leads to a sufficient reduction in power consumption.

[0158]

One of source and drain electrode layers of the transistor 3202 is electrically connected to an electrode 3208 through an opening provided in a gate insulating layer

15 and is electrically connected to the gate electrode layer of the transistor 3200 via the electrode 3208. The electrode 3208 can be formed through a process similar to that for a gate electrode layer of the transistor 3202.

[0159]

Insulating layers 3222, 3223, and 3223a are provided over the transistor 3202.

20 In addition, a conductive layer 3210a is provided in a region overlapping with the one of the source and drain electrode layers of the transistor 3202 with the insulating layers 3222, 3223, and 3223a provided therebetween, and the one of the source and drain electrode layers of the transistor 3202, the insulating layer 3222, and the conductive layer 3210a form the capacitor 3204. That is, the one of the source and drain electrode

25 layers of the transistor 3202 functions as one electrode of the capacitor 3204, and the conductive layer 3210a functions as the other electrode of the capacitor 3204. Note that in the case where no capacitor is needed, a structure in which the capacitor 3204 is not provided is also possible. Alternatively, the capacitor 3204 may be separately provided above the transistor 3202.

30 [0160]

An insulating layer 3224 is provided over the capacitor 3204. In addition, a wiring 3216 for connecting the transistor 3202 to another transistor is provided over the

insulating layer 3224. The wiring 3216 is electrically connected to the other of the source and drain electrode layers of the transistor 3202 through an electrode 3214 provided in an opening formed in the insulating layer 3224, a conductive layer 3210b formed using the same layer as the conductive layer 3210a, and an electrode 3212 5 provided in an opening formed in the insulating layer 3222.

[0161]

In FIGS. 14A and 14B, the transistors 3200 and 3202 are provided so as to at least partly overlap each other, and the source region or the drain region of the transistor 3200 is preferably provided to partly overlap with the oxide semiconductor layer 10 included in the transistor 3202. In addition, the transistor 3202 and the capacitor 3204 are provided so as to overlap with at least part of the transistor 3200. For example, the conductive layer 3210a of the capacitor 3204 is provided so as to at least partly overlap with the gate electrode layer of the transistor 3200. When such a planar layout is employed, the area occupied by the semiconductor device can be reduced; thus, the 15 degree of integration can be increased.

[0162]

Next, an example of a circuit configuration corresponding to FIG. 14A is illustrated in FIG. 14B.

[0163]

20 In FIG. 14B, a first wiring (1st Line) is electrically connected to a source electrode layer of the transistor 3200. A second wiring (2nd Line) is electrically connected to a drain electrode layer of the transistor 3200. A third wiring (3rd Line) is electrically connected to one of the source and drain electrode layers of the transistor 3202, and a fourth wiring (4th Line) is electrically connected to the gate electrode layer 25 of the transistor 3202. The gate electrode layer of the transistor 3200 and the other of the source and drain electrode layers of the transistor 3202 are electrically connected to one electrode of the capacitor 3204. A fifth wiring (5th Line) is electrically connected to the other electrode of the capacitor 3204.

[0164]

30 The semiconductor device in FIG. 14B utilizes a characteristic in which the potential of the gate electrode layer of the transistor 3200 can be held, and thus enables data writing, holding, and reading as follows.

[0165]

Writing and holding of data will be described. First, the potential of the fourth wiring is set to a potential at which the transistor 3202 is turned on, so that the transistor 3202 is turned on. Accordingly, the potential of the third wiring is supplied
5 to the gate electrode layer of the transistor 3200 and to the capacitor 3204. That is, predetermined charge is supplied to the gate electrode layer of the transistor 3200 (writing). Here, one of two kinds of charges providing different potential levels (hereinafter referred to as a low-level charge and a high-level charge) is supplied. After that, the potential of the fourth wiring is set to a potential at which the transistor
10 3202 is turned off, so that the transistor 3202 is turned off. Thus, the charge supplied to the gate electrode layer of the transistor 3200 is held (holding).

[0166]

Since the off-state current of the transistor 3202 is significantly small, the charge of the gate electrode layer of the transistor 3200 is held for a long time.

15 [0167]

Next, reading of data will be described. By supplying an appropriate potential (a reading potential) to the fifth wiring while supplying a predetermined potential (a constant potential) to the first wiring, the potential of the second wiring varies depending on the amount of charge held at the gate electrode layer of the transistor 3200.
20 This is because in general, when the transistor 3200 is an n-channel transistor, an apparent threshold voltage $V_{th_H}$ in the case where the high-level charge is given to the gate electrode layer of the transistor 3200 is lower than an apparent threshold voltage $V_{th_L}$ in the case where the low-level charge is given to the gate electrode layer of the transistor 3200. Here, an apparent threshold voltage refers to the potential of the fifth
25 wiring which is needed to turn on the transistor 3200. Thus, the potential of the fifth wiring is set to a potential $V_0$ which is between $V_{th_H}$ and $V_{th_L}$, whereby charge supplied to the gate electrode layer of the transistor 3200 can be determined. For example, in the case where the high-level charge is supplied in writing, when the potential of the fifth wiring is $V_0$ ($> V_{th_H}$), the transistor 3200 is turned on. In the case
30 where the low-level charge is supplied in writing, even when the potential of the fifth wiring is $V_0$ ($< V_{th_L}$), the transistor 3200 remains off. Therefore, the data held can be

read by measuring the potential of the second wiring.

[0168]

Note that in the case where memory cells are arrayed, it is necessary that data of only a desired memory cell can be read. In that case, the fifth wirings of memory cells from which data is not read may be supplied with a potential at which the transistor 3200 is turned off regardless of the state of the gate electrode layer, that is, a potential lower than $V_{th_H}$. Alternatively, the fifth wirings may be supplied with a potential at which the transistor 3200 is turned on regardless of the state of the gate electrode layer, that is, a potential higher than $V_{th_L}$.

[0169]

When including a transistor having a channel formation region formed using a wide band gap semiconductor and having extremely low off-state current, the semiconductor device described in this embodiment can store data for an extremely long period. In other words, refresh operation becomes unnecessary or the frequency of the refresh operation can be extremely lowered, which leads to a sufficient reduction in power consumption. Moreover, stored data can be held for a long period even when power is not supplied (note that a potential is preferably fixed).

[0170]

Further, in the semiconductor device described in this embodiment, high voltage is not needed for writing data and there is no problem of deterioration of elements. For example, unlike a conventional nonvolatile memory, it is not necessary to inject and extract electrons into and from a floating gate, and thus a problem such as deterioration of a gate insulating layer does not arise at all. That is, the semiconductor device according to the disclosed invention does not have a limitation on the number of times data can be rewritten, which is a problem of a conventional nonvolatile memory, and the reliability thereof is drastically improved. Furthermore, since data are written by turning on or off the transistors, high-speed operation can be easily achieved.

[0171]

As described above, a miniaturized and highly integrated semiconductor device having favorable electric characteristics and a method for manufacturing the semiconductor device can be provided.

[0172]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

5 [0173]

(Embodiment 7)

In this embodiment, one embodiment of a structure of a memory device which is different from that in Embodiment 6 will be described.

[0174]

10 FIG. 15 is a perspective view of a memory device. The memory device illustrated in FIG. 15 includes a plurality of layers of memory cell arrays (memory cell arrays 3400(1) to 3400(*n*) (*n* is an integer greater than or equal to 2)) each including a plurality of memory cells as memory circuits in the upper portion, and a logic circuit 3004 in the lower portion which is necessary for operating the memory cell arrays 15 3400(1) to 3400(*n*).

[0175]

FIG. 16 is a partial enlarged view of the memory device illustrated in FIG. 15. FIG. 16 illustrates the logic circuit 3004, the memory cell array 3400(1), and the memory cell array 3400(2), and illustrates a memory cell 3170a and a memory cell 20 3170b as typical examples among the plurality of memory cells included in the memory cell array 3400(1) and the memory cell array 3400(2). The memory cell 3170a and the memory cell 3170b can have a configuration similar to the circuit configuration described in the above embodiment, for example.

[0176]

25 Note that a transistor 3171a included in the memory cell 3170a is illustrated as a typical example. A transistor 3171b included in the memory cell 3170b is illustrated as a typical example. Each of the transistors 3171a and 3171b includes a channel formation region in an oxide semiconductor layer. The structure of the transistor in which the channel formation region is formed in the oxide semiconductor layer is the 30 same as the structure described in any of the other embodiments, and thus the description of the structure is omitted.

[0177]

A conductive layer 3501a which is formed using the same layer as a gate electrode layer of the transistor 3171a is electrically connected to an electrode 3003a via an electrode 3502a. A conductive layer 3501c which is formed using the same layer as a gate electrode layer of the transistor 3171b is electrically connected to an electrode 3003c via an electrode 3502c.

[0178]

The logic circuit 3004 includes a transistor 3001 in which a semiconductor material other than a wide band gap semiconductor is used for a channel formation region. The transistor 3001 can be a transistor obtained in such a manner that an element isolation insulating layer 3106 is provided on a substrate 3000 including a semiconductor material (e.g., silicon) and a region serving as the channel formation region is formed in a region surrounded by the element isolation insulating layer 3106. Note that the transistor 3001 may be a transistor obtained in such a manner that the channel formation region is formed in a semiconductor film such as a silicon film formed on an insulating surface or in a silicon film of an SOI substrate. A known structure can be used as the structure of the transistor 3001 and thus the description is omitted.

[0179]

A wiring 3100a and a wiring 3100b are formed between layers in which the transistor 3171a is formed and layers in which the transistor 3001 is formed. An insulating film 3140a is provided between the wiring 3100a and the layers in which the transistor 3001 is formed. An insulating film 3141a is provided between the wiring 3100a and the wiring 3100b. An insulating film 3142a is provided between the wiring 3100b and the layers in which the transistor 3171a is formed.

[0180]

Similarly, a wiring 3100c and a wiring 3100d are formed between the layers in which the transistor 3171b is formed and the layers in which the transistor 3171a is formed. An insulating film 3140b is provided between the wiring 3100c and the layers in which the transistor 3171a is formed. An insulating film 3141b is provided between the wiring 3100c and the wiring 3100d. An insulating film 3142b is provided between the wiring 3100d and the layers in which the transistor 3171b is formed.

[0181]

The insulating films 3140a, 3141a, 3142a, 3140b, 3141b, and 3142b each function as an interlayer insulating film whose surface can be planarized.

[0182]

The wirings 3100a, 3100b, 3100c, and 3100d enable electrical connection between the memory cells, electrical connection between the logic circuit 3004 and the memory cells, and the like.

[0183]

An electrode 3303 included in the logic circuit 3004 can be electrically connected to a circuit provided in the upper portion.

[0184]

For example, as illustrated in FIG. 16, the electrode 3303 can be electrically connected to the wiring 3100a via an electrode 3505. The wiring 3100a can be electrically connected to a conductive layer 3501b which is formed using the same layer as the gate electrode layer of the transistor 3171a via an electrode 3503a. In this manner, the wiring 3100a and the electrode 3303 can be electrically connected to the source or the drain of the transistor 3171a. The conductive layer 3501b can be electrically connected to an electrode 3003b via the source or the drain of the transistor 3171a and an electrode 3502b. The electrode 3003b can be electrically connected to the wiring 3100c via an electrode 3503b.

[0185]

FIG. 16 illustrates an example in which the electrode 3303 and the transistor 3171a are electrically connected to each other via the wiring 3100a; however, one embodiment of the disclosed invention is not limited thereto. The electrode 3303 may be electrically connected to the transistor 3171a via the wiring 3100b, via both the wiring 3100a and the wiring 3100b, or via another electrode without using the wiring 3100a nor the wiring 3100b.

[0186]

FIG. 16 illustrates the structure where two wiring layers, i.e., a wiring layer in which the wiring 3100a is formed and a wiring layer in which the wiring 3100b is formed are provided between the layers in which the transistor 3171a is formed and the layers in which the transistor 3001 is formed; however, the number of wiring layers provided therebetween is not limited to two. One wiring layer or three or more wiring

layers may be provided between the layers in which the transistor 3171a is formed and the layers in which the transistor 3001 is formed.

[0187]

FIG. 16 illustrates the structure where two wiring layers, i.e., a wiring layer in which the wiring 3100c is formed and a wiring layer in which the wiring 3100d is formed are provided between the layers in which the transistor 3171b is formed and the layers in which the transistor 3171a is formed; however, the number of wiring layers provided therebetween is not limited to two. One wiring layer or three or more wiring layers may be provided between the layers in which the transistor 3171b is formed and the layers in which the transistor 3171a is formed.

[0188]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0189]

(Embodiment 8)

A semiconductor device disclosed in this specification can be applied to a variety of electronic devices (including game machines). Examples of electronic devices include a television device (also referred to as a television or a television receiver), a monitor of a computer or the like, a camera such as a digital camera or a digital video camera, a digital photo frame, a mobile phone, a portable game machine, a portable information terminal, an audio reproducing device, a game machine (such as a pachinko machine or a slot machine), a game console, and the like. FIGS. 17A to 17C illustrate a specific example of an electronic device.

[0190]

FIGS. 17A and 17B illustrate a tablet terminal that can be folded. In FIG. 17A, the tablet terminal is opened, and includes a housing 9630, a display portion 9631a, a display portion 9631b, a display-mode switching button 9034, a power button 9035, a power-saving-mode switching button 9036, a clip 9033, and an operation button 9038.

[0191]

The semiconductor device described in any of Embodiments 1 to 3 can be used for the display portion 9631a and the display portion 9631b, whereby the tablet terminal

can be provided with high reliability.

[0192]

Part of the display portion 9631a can be a touch panel region 9632a and data can be input when a displayed operation key 9638 is touched. Although a structure in which a half region in the display portion 9631a has only a display function and the other half region has a touch panel function is shown as an example, the display portion 9631a is not limited to the structure. The whole region in the display portion 9631a may have a touch panel function. For example, the display portion 9631a can display a keyboard in the whole region to be used as a touch panel, and the display portion 9631b can be used as a display screen.

[0193]

Like the display portion 9631a, a touch panel region 9632b can be formed in part of the display portion 9631b. When a keyboard display switching button 9639 displayed on the touch panel is touched with a finger, a stylus, or the like, a keyboard can be displayed on the display portion 9631b.

[0194]

Touch input can be performed concurrently on the touch panel regions 9632a and 9632b.

[0195]

The display-mode switching button 9034 allows switching between a landscape mode and a portrait mode, color display and black-and-white display, and the like. With the power-saving-mode switching button 9036, the luminance of display can be optimized in accordance with the amount of external light at the time when the tablet is in use, which is detected with an optical sensor incorporated in the tablet. The tablet terminal may include another detection device such as a sensor for detecting inclination (e.g., a gyroscope or an acceleration sensor) in addition to the optical sensor.

[0196]

Although the display portion 9631a and the display portion 9631b have the same display area in FIG. 17A, one embodiment of the present invention is not limited to this structure. The display portion 9631a and the display portion 9631b may have different areas or different display quality. For example, one of them may be a display panel that can display higher-definition images than the other.

[0197]

In FIG. 17B, the tablet terminal is folded, and includes the housing 9630, a solar battery 9633, a charge and discharge control circuit 9634, a battery 9635, and a DCDC converter 9636. FIG. 17B illustrates an example in which the charge and
5 discharge control circuit 9634 includes the battery 9635 and the DCDC converter 9636.

[0198]

Since the tablet terminal can be folded, the housing 9630 can be closed when the tablet terminal is not used. Thus, the display portions 9631a and 9631b can be protected, thereby providing the tablet terminal with high endurance and high reliability
10 for long-term use.

[0199]

In addition, the tablet terminal illustrated in FIGS. 17A and 17B can have a function of displaying a variety of kinds of data (e.g., a still image, a moving image, and a text image), a function of displaying a calendar, a date, the time, or the like on the
15 display portion, a touch-input function of operating or editing the data displayed on the display portion by touch input, a function of controlling processing by a variety of kinds of software (programs), and the like.

[0200]

The solar battery 9633, which is attached on the surface of the tablet terminal,
20 supplies electric power to a touch panel, a display portion, an image signal processor, and the like. Note that the solar battery 9633 can be provided on one or both surfaces of the housing 9630, so that the battery 9635 can be charged efficiently. The use of a lithium ion battery as the battery 9635 is advantageous in downsizing or the like.

[0201]

25 The structure and operation of the charge and discharge control circuit 9634 illustrated in FIG. 17B are described with reference to a block diagram of FIG. 17C. FIG. 17C illustrates the solar battery 9633, the battery 9635, the DCDC converter 9636, a converter 9637, switches SW1 to SW3, and the display portion 9631. The battery 9635, the DCDC converter 9636, the converter 9637, and the switches SW1 to SW3
30 correspond to the charge and discharge control circuit 9634 in FIG. 17B.

[0202]

First, an example of operation in the case where power is generated by the solar

battery 9633 using external light is described. The voltage of power generated by the solar battery 9633 is raised or lowered by the DCDC converter 9636 so that the power has a voltage for charging the battery 9635. When the display portion 9631 is operated with the power from the solar battery 9633, the switch SW1 is turned on and the voltage
5 of the power is raised or lowered by the converter 9637 to a voltage needed for operating the display portion 9631. In addition, when display on the display portion 9631 is not performed, the switch SW1 is turned off and a switch SW2 is turned on so that charge of the battery 9635 may be performed.

[0203]

10 Here, the solar battery 9633 is shown as an example of a power generation means; however, there is no particular limitation on a way of charging the battery 9635, and the battery 9635 may be charged with another power generation means such as a piezoelectric element or a thermoelectric conversion element (Peltier element). For example, the battery 9635 may be charged with a non-contact power transmission
15 module that transmits and receives power wirelessly (without contact) to charge the battery or with a combination of other charging means.

[0204]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in
20 the other embodiments.

EXPLANATION OF REFERENCE

[0205]

400: substrate, 401: gate electrode layer, 402: gate insulating layer, 403: oxide
25 semiconductor layer, 405: low-resistance material layer, 405a: low-resistance material layer, 405b: low-resistance material layer, 406: first protective layer, 407: second protective layer, 407a: third protective layer, 407b: fourth protective layer, 420: transistor, 421: transistor, 430: capacitor, 431: transistor, 432: insulating layer, 436: base insulating layer, 440: transistor, 441: transistor, 451: oxygen doping, 453: resist, 454:
30 conductive layer, 454a: first conductive layer, 454b: second conductive layer, 455: resist, 474a: wiring layer, 474b: wiring layer, 485: wiring protective layer, 485a: first wiring protective layer, 485b: second wiring protective layer, 495: hard mask layer, 3000:

substrate, 3001: transistor, 3003a: electrode, 3003b: electrode, 3003c: electrode, 3004: logic circuit, 3100a: wiring, 3100b: wiring, 3100c: wiring, 3100d: wiring, 3106: element isolation insulating layer, 3140a: insulating film, 3140b: insulating film, 3141a: insulating film, 3141b: insulating film, 3142a: insulating film, 3142b: insulating film,
5 3170a: memory cell, 3170b: memory cell, 3171a: transistor, 3171b: transistor, 3200: transistor, 3202: transistor, 3204: capacitor, 3208: electrode, 3210a: conductive layer, 3210b: conductive layer, 3212: electrode, 3214: electrode, 3216: wiring, 3220: insulating layer, 3222: insulating layer, 3223: insulating layer, 3223a: insulating layer, 3224: insulating layer, 3303: electrode, 3400(1): memory cell array, 3400(2): memory
10 cell array, 3400(n): memory cell array, 3501a: conductive layer, 3501b: conductive layer, 3501c: conductive layer, 3502a: electrode, 3502b: electrode, 3502c: electrode, 3503a: electrode, 3503b: electrode, 3505: electrode, 9033: clip, 9034: button, 9035: power button, 9036: button, 9038: operation button, 9630: housing, 9631: display portion, 9631a: display portion, 9631b: display portion, 9632a: region, 9632b: region, 9633:
15 solar battery, 9634: charge and discharge control circuit, 9635: battery, 9636: DCDC converter, 9637: converter, 9638: operation key, 9639: button.

This application is based on Japanese Patent Application serial no. 2011-282438 filed with Japan Patent Office on December 23, 2011 and Japanese Patent
20 Application serial no. 2011-282511 filed with Japan Patent Office on December 23, 2011, the entire contents of which are hereby incorporated by reference.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a gate electrode layer;

a gate insulating layer on one surface of the gate electrode layer;

a semiconductor layer on one surface of the gate insulating layer;

a first conductive layer over the semiconductor layer;

a second conductive layer over the first conductive layer;

a protective layer over the second conductive layer; and

a hard mask layer over the protective layer,

wherein the hard mask layer comprises an opening which overlaps with a channel formation region of the semiconductor layer.

2. The semiconductor device according to claim 1,

wherein the semiconductor layer includes an oxide including In, an element *M*, and Zn, and

wherein the element *M* is at least one element selected from the group consisting of Ga, Sn, Hf, Al, Zr, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu.

3. The semiconductor device according to claim 1, wherein the hard mask layer comprises amorphous silicon.

4. The semiconductor device according to claim 1, wherein a thickness of the semiconductor layer is greater than or equal to 5 nm and less than or equal to 30 nm.

5. The semiconductor device according to claim 1, wherein a channel length of a transistor including the semiconductor layer is greater than or equal to 20 nm and less than or equal to 100 nm.

6. The semiconductor device according to claim 1, wherein a length of the semiconductor layer in a channel length direction is larger than a length of the gate electrode layer in the channel length direction.

7. The semiconductor device according to claim 1, wherein a width of the opening is substantially the same as a length of the semiconductor layer in a channel length direction.

8. The semiconductor device according to claim 1, wherein the semiconductor layer is located over the gate electrode layer.

9. A semiconductor device comprising:

a gate electrode layer;

a gate insulating layer on one surface of the gate electrode layer;

a semiconductor layer on one surface of the gate insulating layer;

a first conductive layer and a second conductive layer over the semiconductor layer;

a third conductive layer over the first conductive layer;

a fourth conductive layer over the second conductive layer; and

a protective layer over the third conductive layer and the fourth conductive layer,

wherein a distance between the first conductive layer and the second conductive layer is shorter than a distance between the third conductive layer and the fourth conductive layer, and

wherein the first conductive layer and the third conductive layer serve as a source electrode and the second conductive layer and the fourth conductive layer serve as a drain electrode.

10. The semiconductor device according to claim 9,

wherein the semiconductor layer includes an oxide including In, an element *M*, and Zn, and

wherein the element $M$ is at least one element selected from the group consisting of Ga, Sn, Hf, Al, Zr, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu.

11. The semiconductor device according to claim 9, wherein a thickness of the semiconductor layer is greater than or equal to 5 nm and less than or equal to 30 nm.

12. The semiconductor device according to claim 9, wherein a channel length of a transistor including the semiconductor layer is greater than or equal to 20 nm and less than or equal to 100 nm.

13. The semiconductor device according to claim 9, wherein a length of the semiconductor layer in a channel length direction is larger than a length of the gate electrode layer in the channel length direction.

14. The semiconductor device according to claim 9, wherein the semiconductor layer is located over the gate electrode layer.

15. A semiconductor device comprising:

a gate electrode layer adjacent to an oxide semiconductor layer;

the oxide semiconductor layer comprising a channel formation region;

a first conductive layer over and in contact with a first portion of the oxide semiconductor layer;

a second conductive layer over and in contact with a second portion of the oxide semiconductor layer; and

a silicon oxynitride film over the first conductive layer and the second conductive layer,

wherein the silicon oxynitride film is in contact with a third portion of the oxide semiconductor layer between the first portion and the second portion,

wherein the third portion includes the channel formation region, and

wherein a channel length of a transistor including the oxide semiconductor layer is less than or equal to 30 nm with use of a photolithography process using an electron beam.

16. The semiconductor device according to claim 15,

wherein the oxide semiconductor layer includes In, an element *M*, and Zn, and

wherein the element *M* is at least one element selected from the group consisting of Ga, Sn, Hf, Al, Zr, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu.

17. The semiconductor device according to claim 15, further comprising a hard mask layer over the first conductive layer and the second conductive layer.

18. The semiconductor device according to claim 17, wherein the hard mask layer comprises amorphous silicon.

19. The semiconductor device according to claim 15, wherein a thickness of the oxide semiconductor layer is greater than or equal to 5 nm and less than or equal to 30 nm.

20. The semiconductor device according to claim 15, wherein the oxide semiconductor layer is formed over the gate electrode layer.

ABSTRACT

A bottom-gate transistor with a short channel length and a method for manufacturing the transistor are provided. A bottom-gate transistor with a short channel length in which portions of a source electrode and a drain electrode which are proximate to a channel formation region are thinner than other portions thereof was devised. In addition, the portions of the source electrode and the drain electrode which are proximate to the channel formation region are formed in a later step than the other portions thereof, whereby a bottom-gate transistor with a short channel length can be manufactured.

FIG. 1A

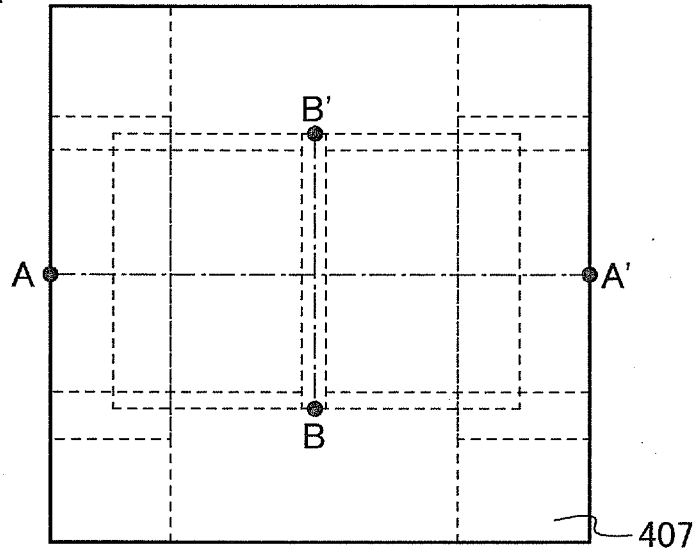



FIG. 1B

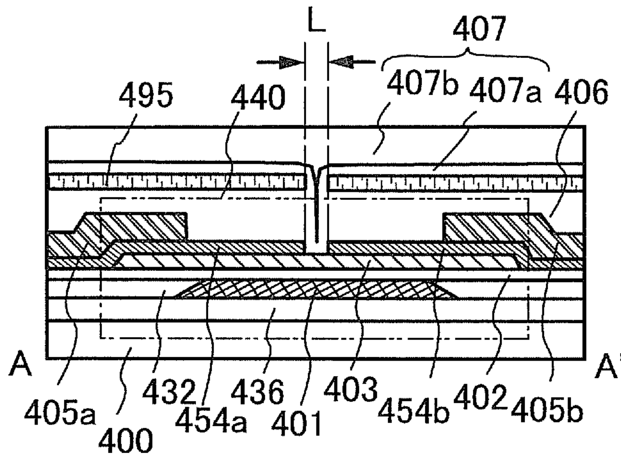
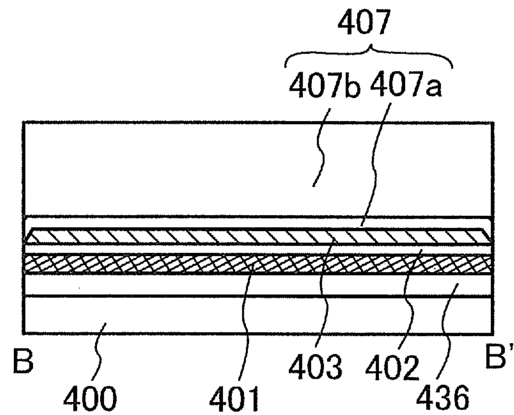



FIG. 1C



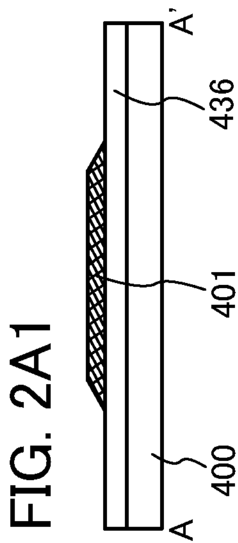


FIG. 2A1

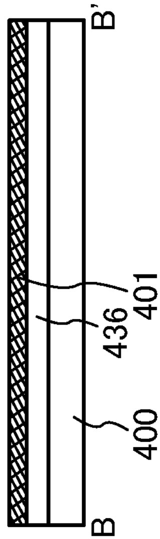


FIG. 2A2

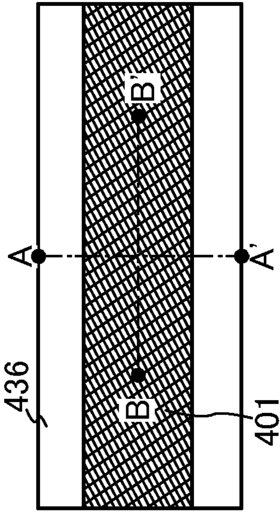


FIG. 2A3

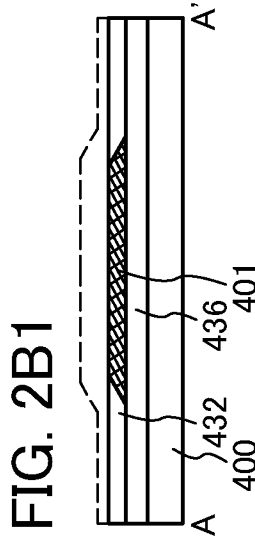


FIG. 2B1

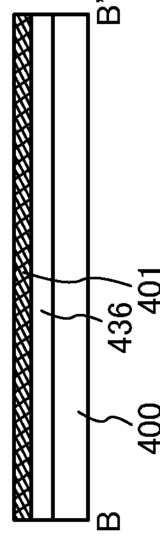


FIG. 2B2

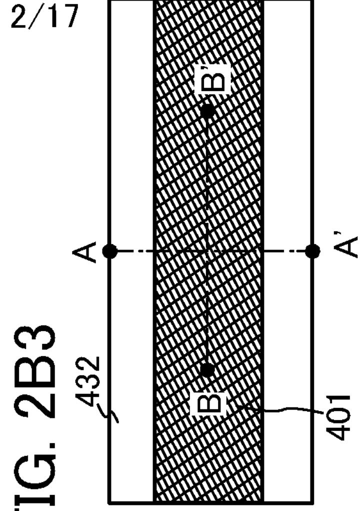


FIG. 2B3

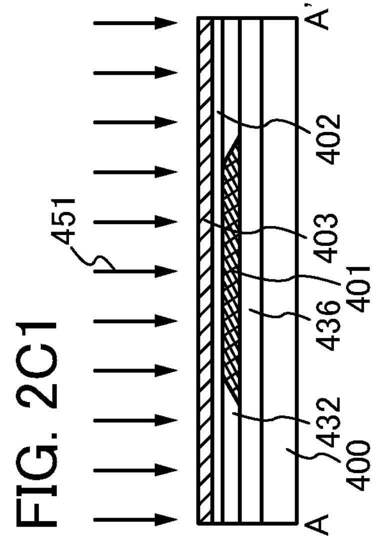


FIG. 2C1

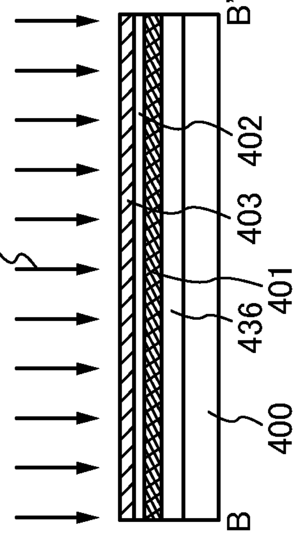


FIG. 2C2

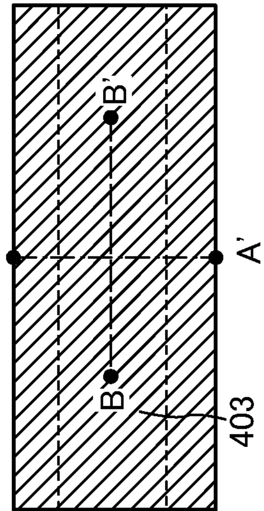


FIG. 2C3

FIG. 3A1

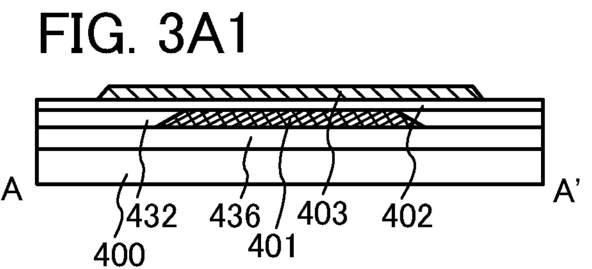



FIG. 3A2

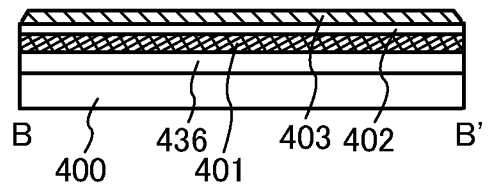



FIG. 3A3

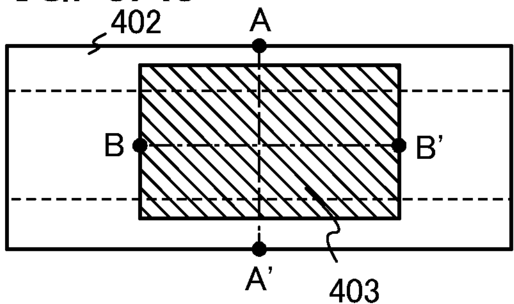



FIG. 3B1

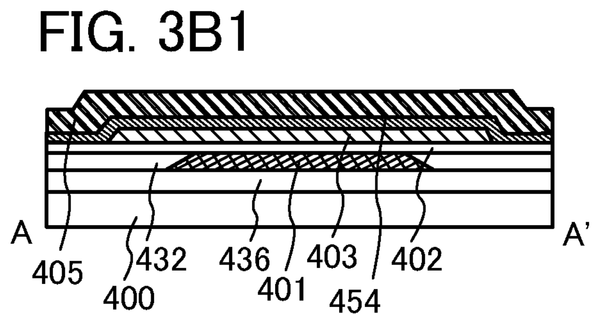



FIG. 3B2

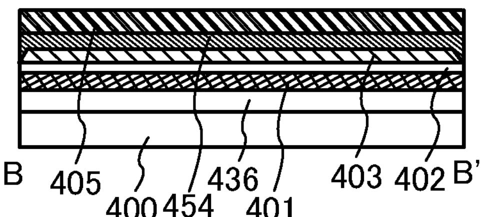



FIG. 3B3

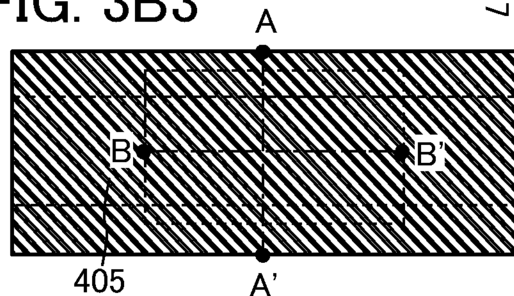



FIG. 3C1

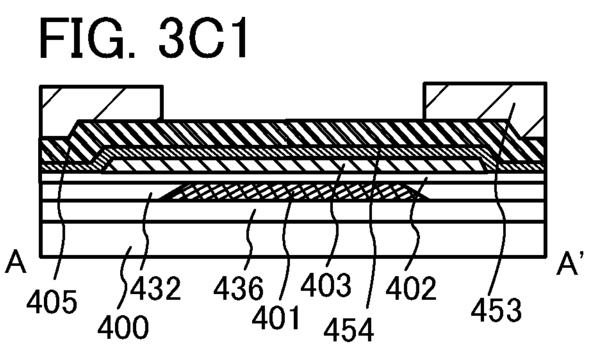



FIG. 3C2

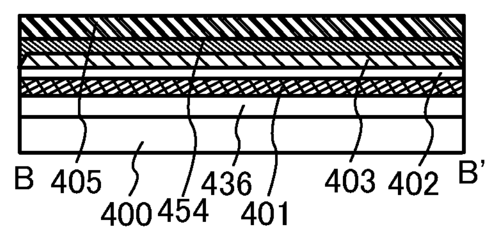
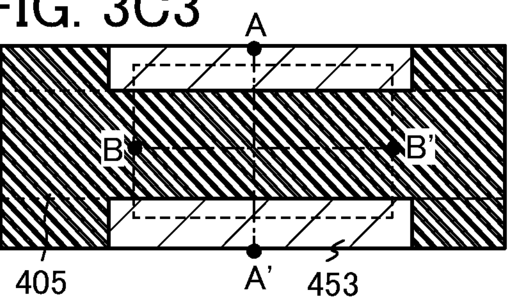



FIG. 3C3



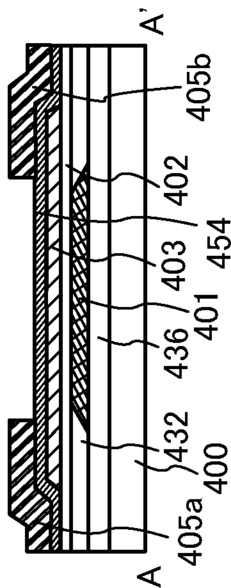


FIG. 4A1

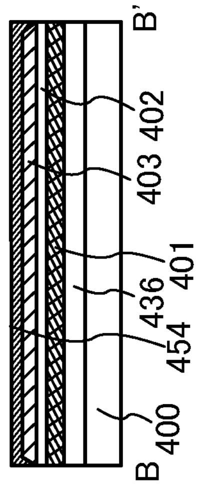


FIG. 4A2

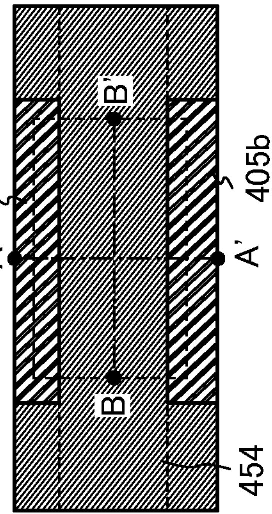


FIG. 4A3

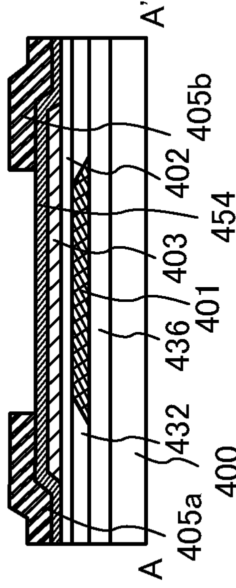


FIG. 4B1

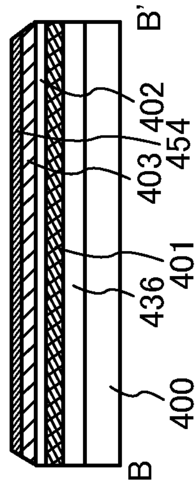


FIG. 4B2

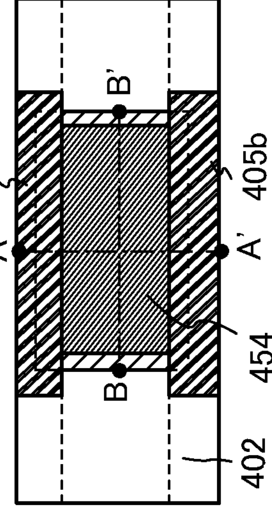


FIG. 4B3

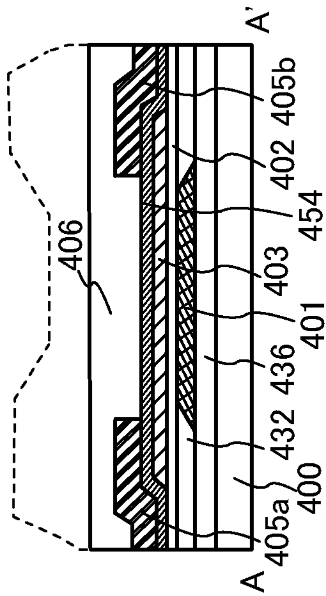


FIG. 4C1

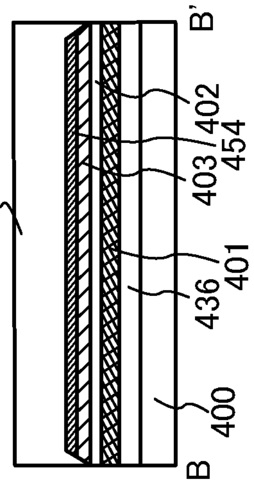


FIG. 4C2

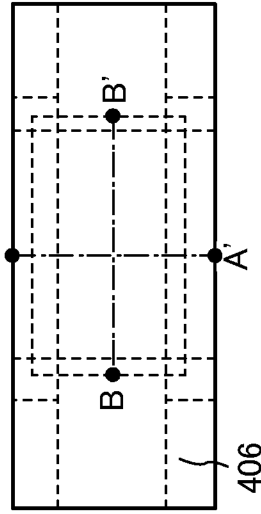


FIG. 4C3

FIG. 5A1

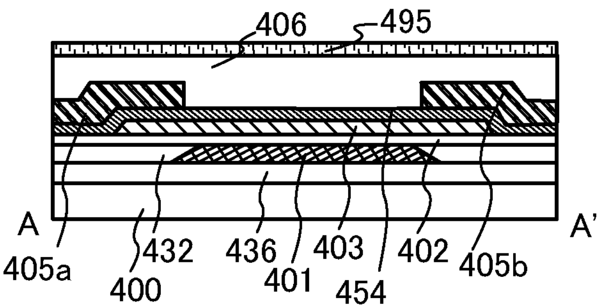



FIG. 5A2

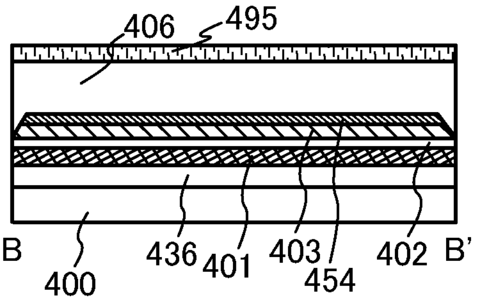



FIG. 5A3

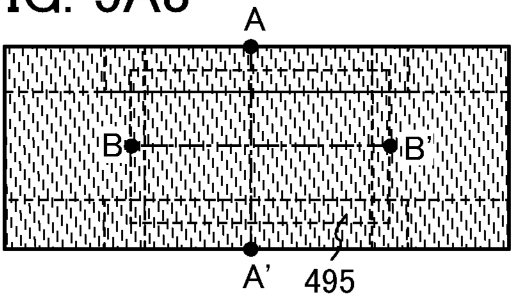



FIG. 5B1

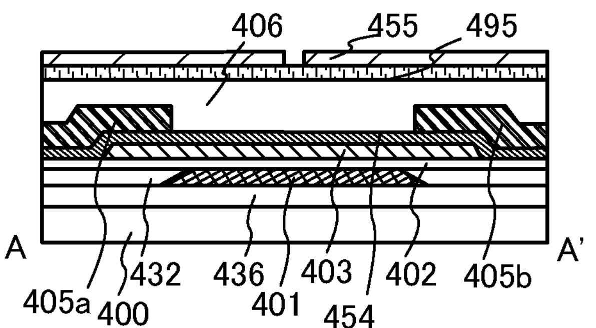



FIG. 5B2

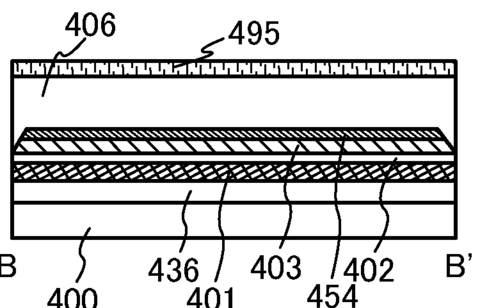



FIG. 5B3

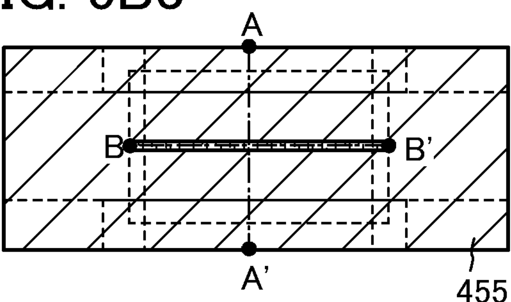



FIG. 5C1

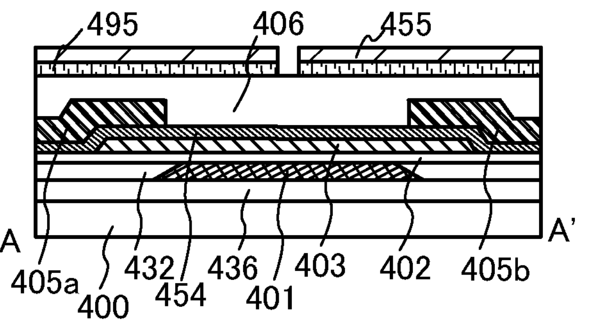



FIG. 5C2

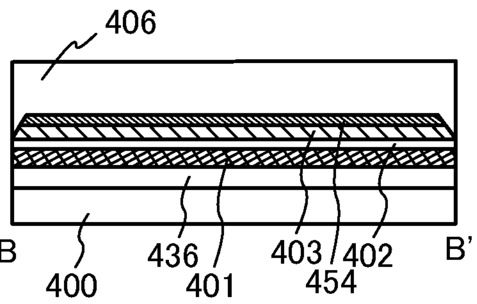



FIG. 5C3

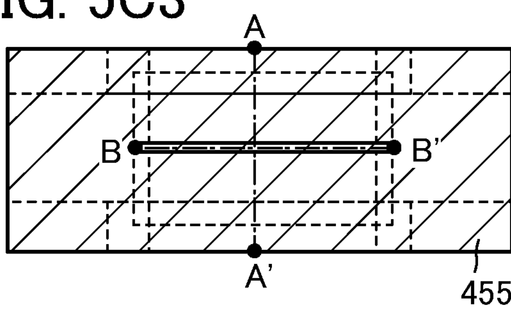


FIG. 6A1

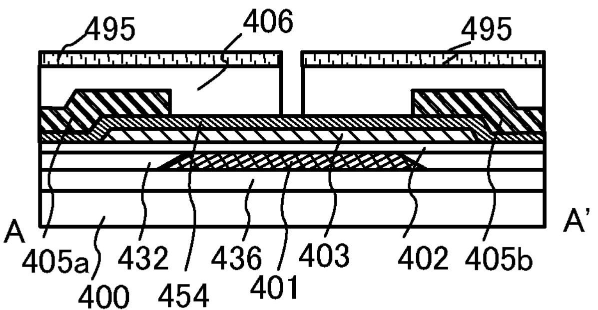



FIG. 6A2

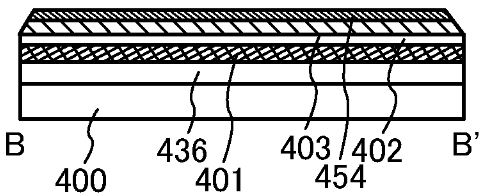



FIG. 6A3

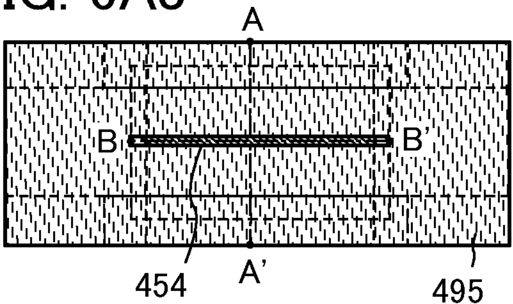



FIG. 6B1

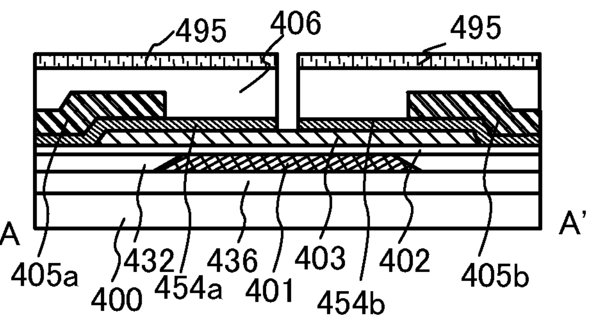



FIG. 6B2



FIG. 6B3

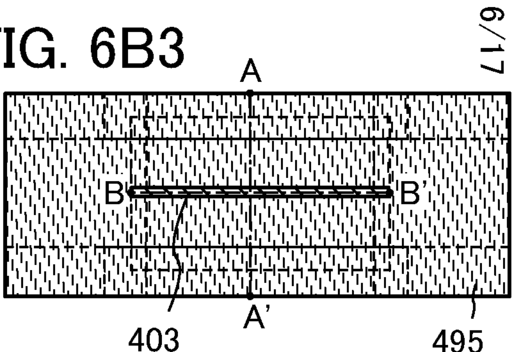



FIG. 6C1

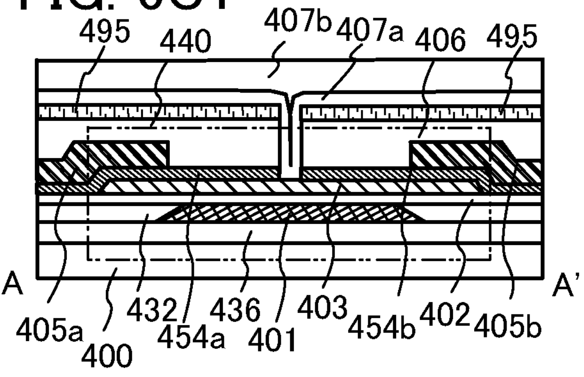
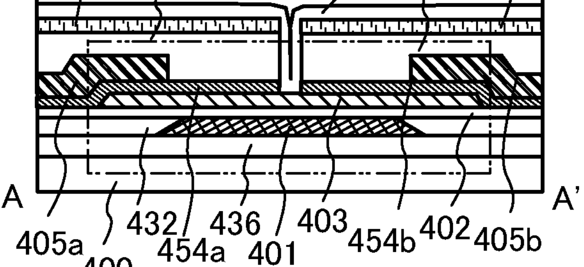




FIG. 6C2

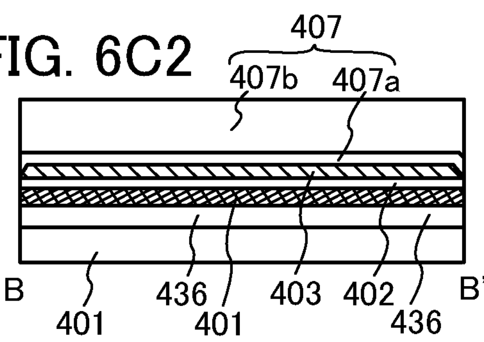
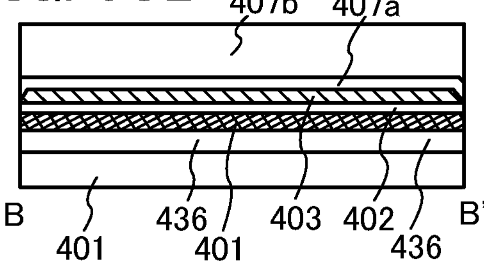




FIG. 6C3

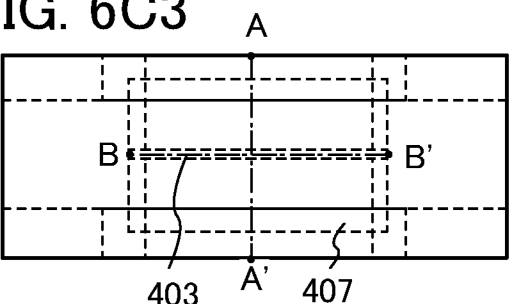


FIG. 7A

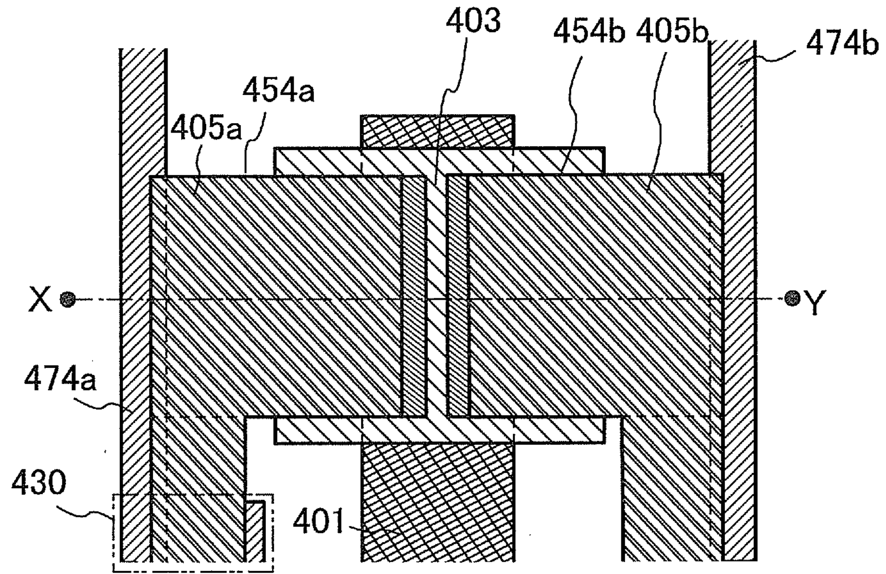



FIG. 7B

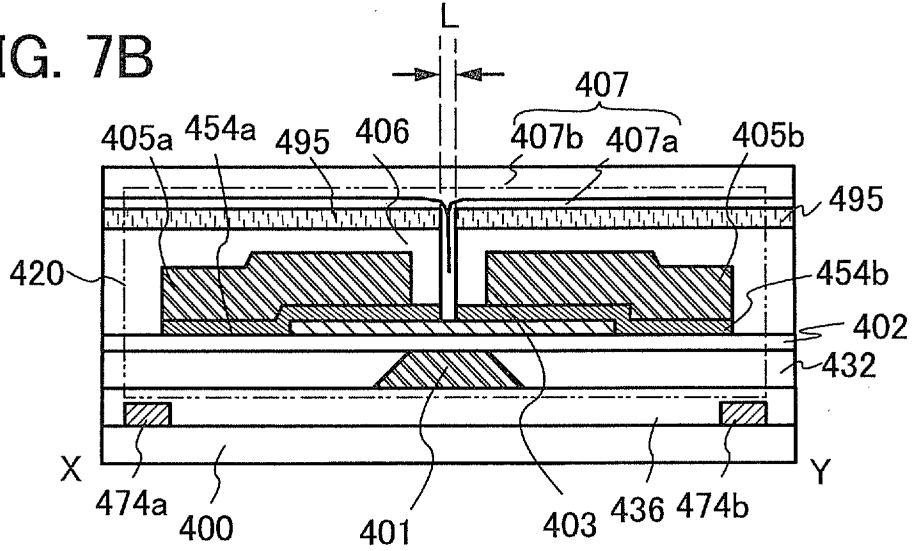


FIG. 8

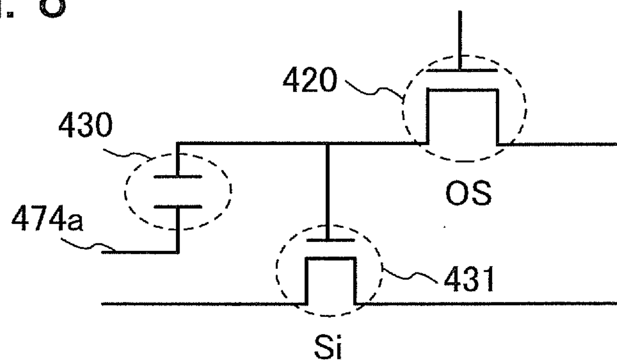


FIG. 9A

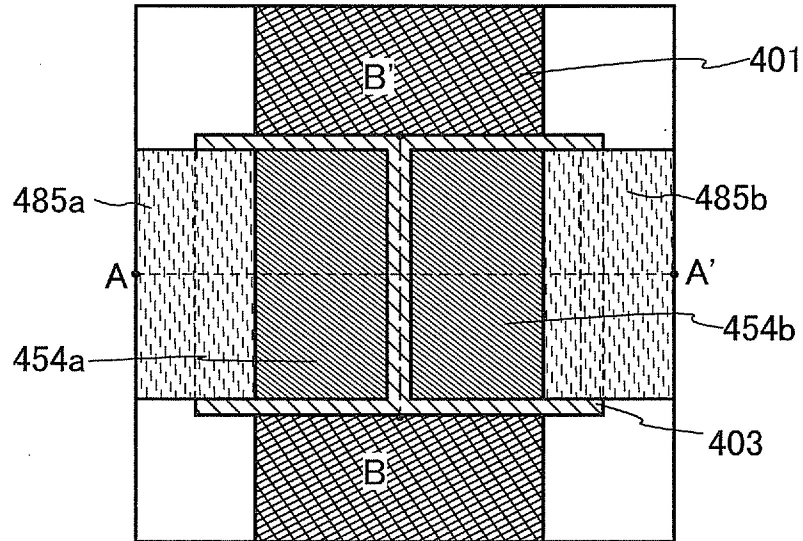



FIG. 9B

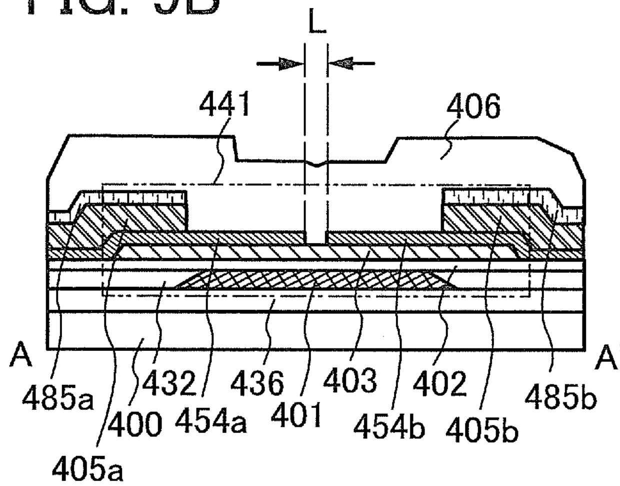



FIG. 9C

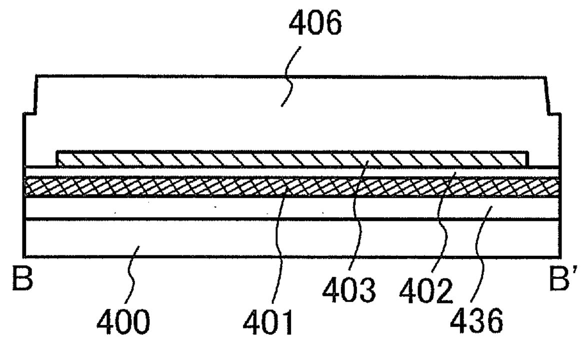


FIG. 10A1

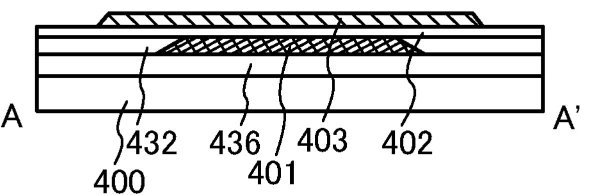



FIG. 10A2

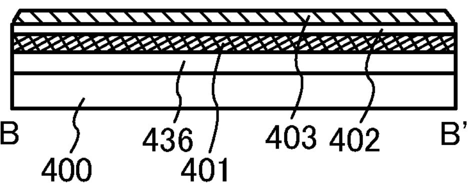



FIG. 10A3

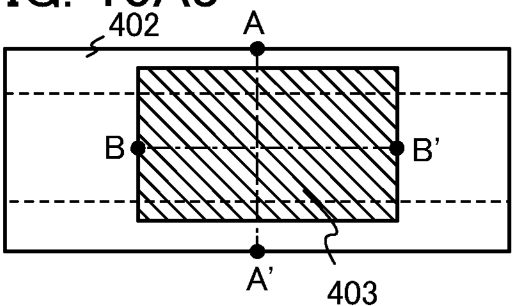



FIG. 10B1

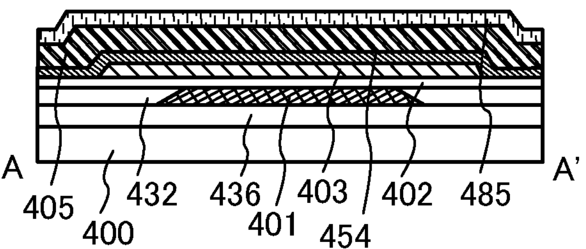



FIG. 10B2

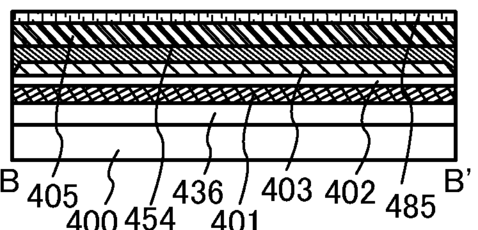



FIG. 10B3

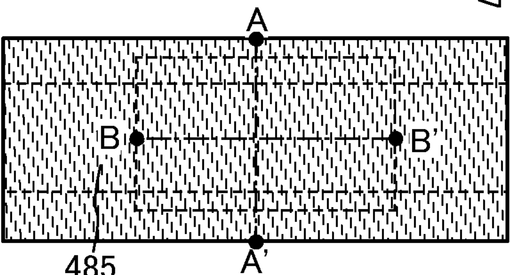



FIG. 10C1

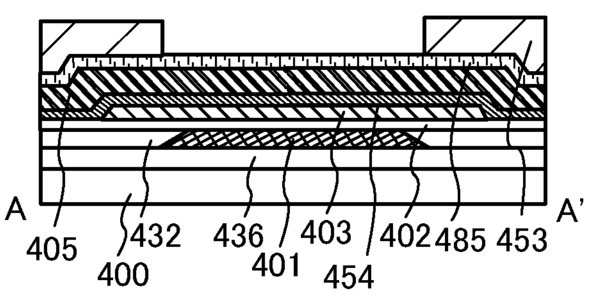



FIG. 10C2

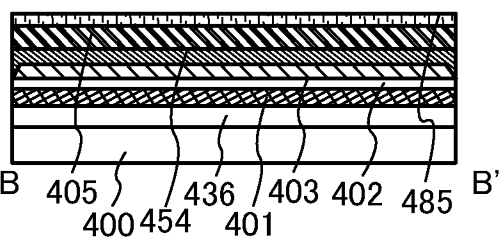



FIG. 10C3

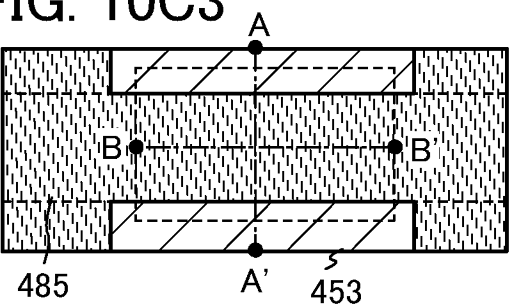


FIG. 11A1

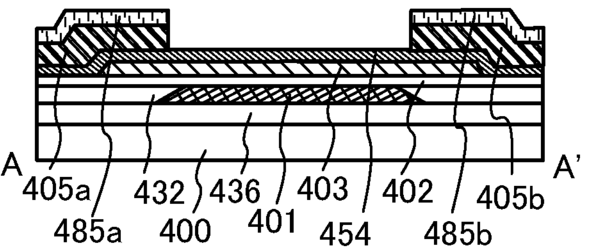



FIG. 11A2

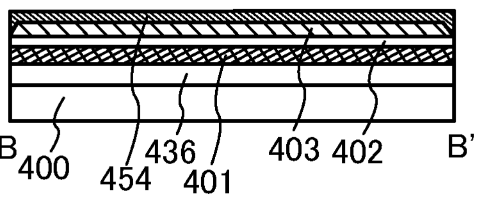



FIG. 11A3

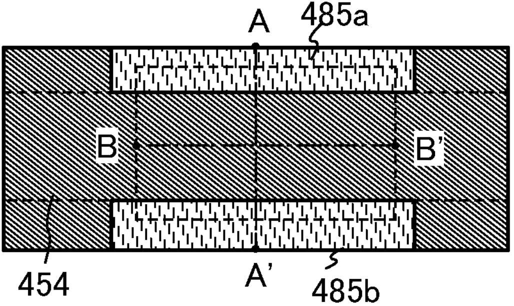



FIG. 11B1

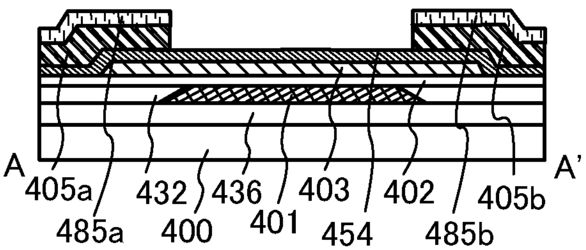



FIG. 11B2

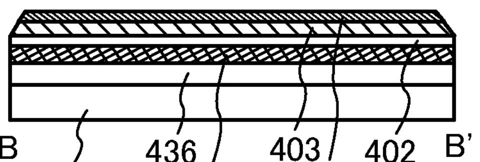



FIG. 11B3

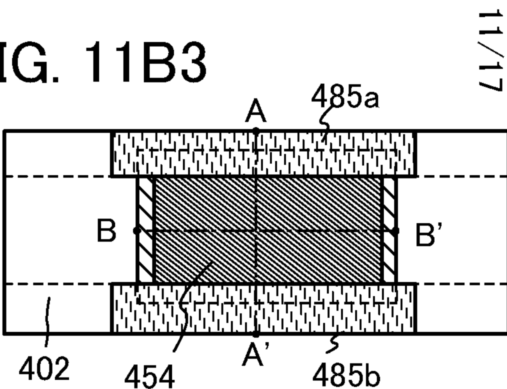



FIG. 11C1

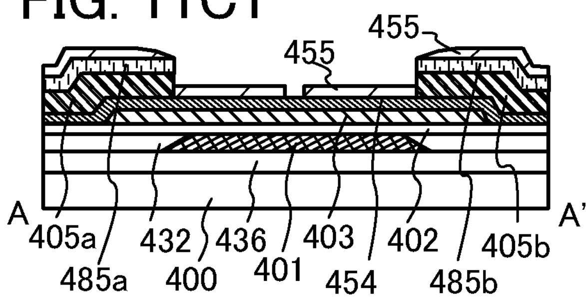



FIG. 11C2

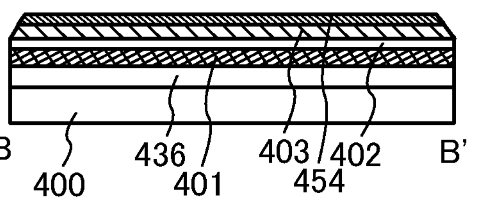



FIG. 11C3

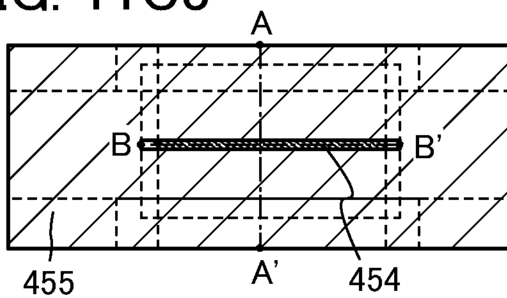


FIG. 12A1

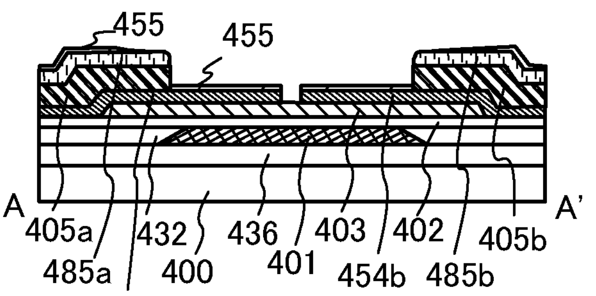



FIG. 12A2

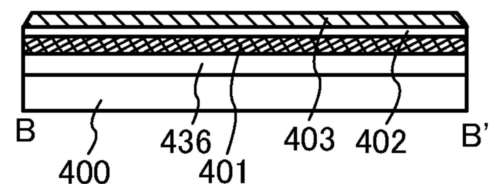



FIG. 12A3

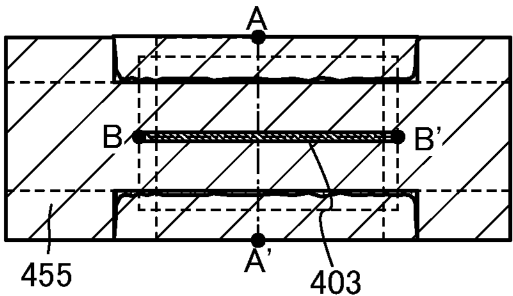



FIG. 12B1

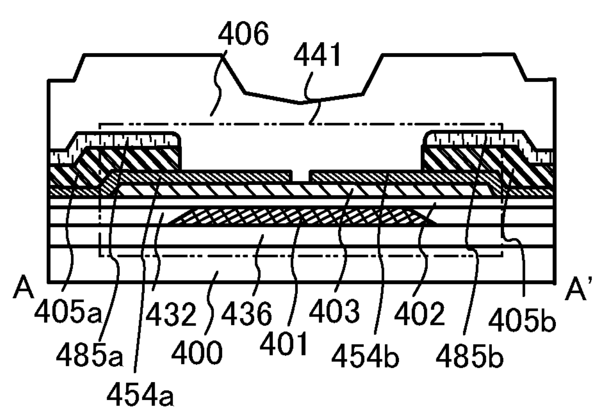



FIG. 12B2

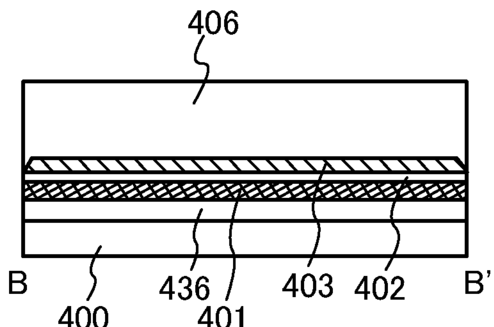



FIG. 12B3

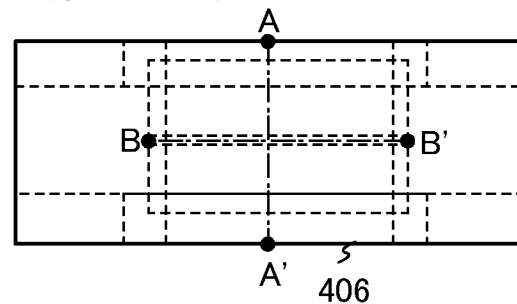


FIG. 13A

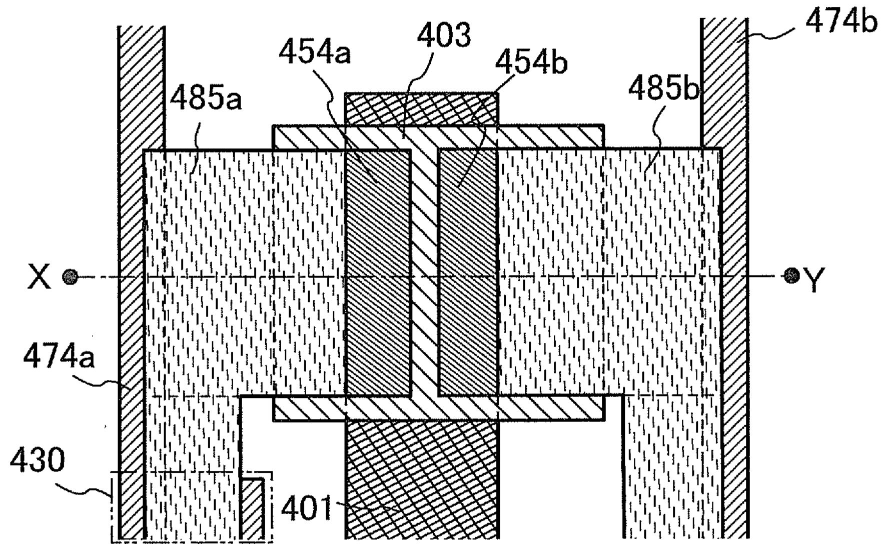



FIG. 13B

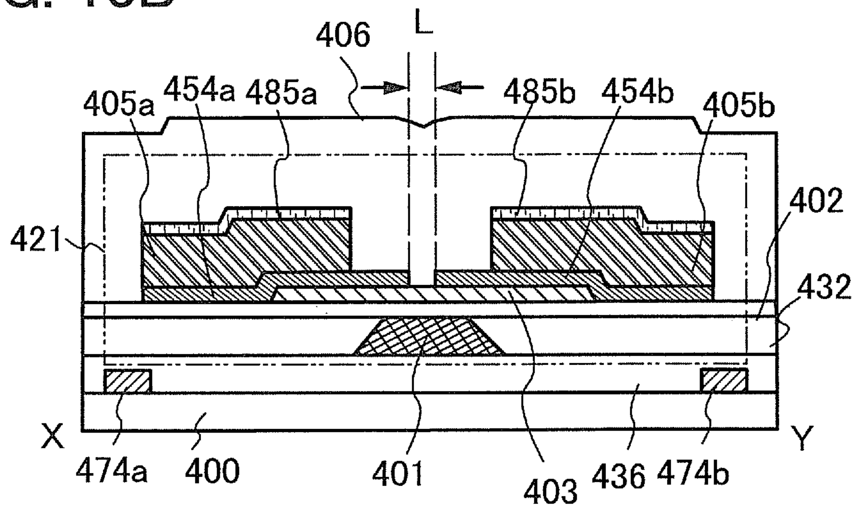


FIG. 14A

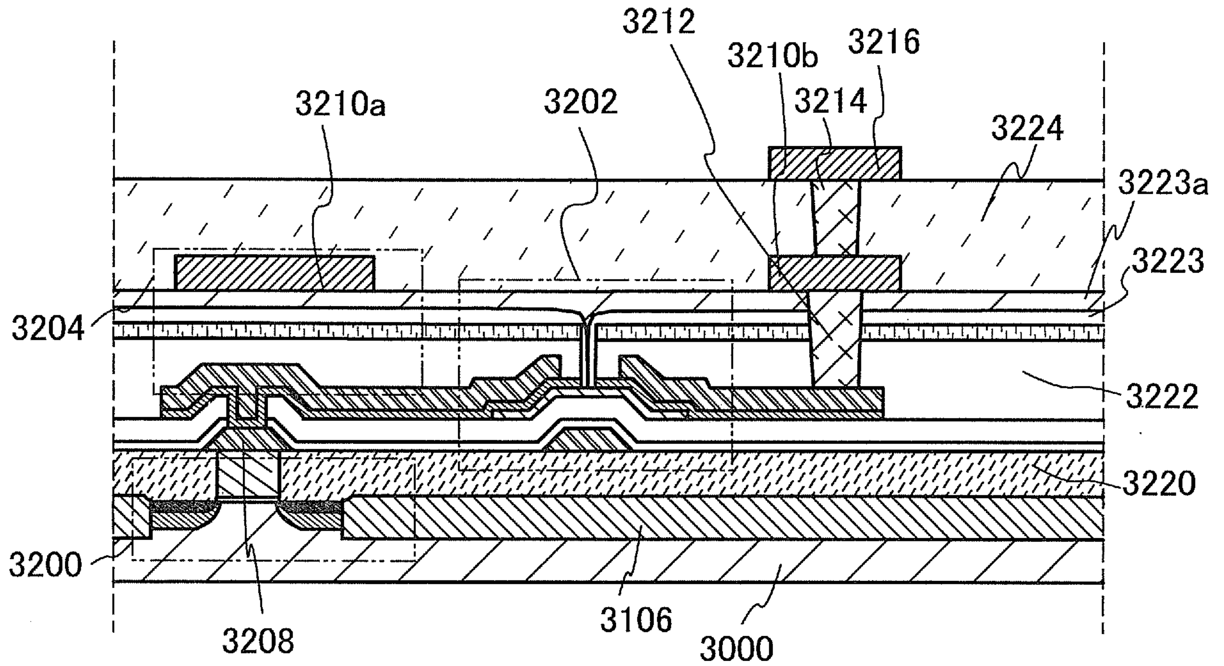



FIG. 14B

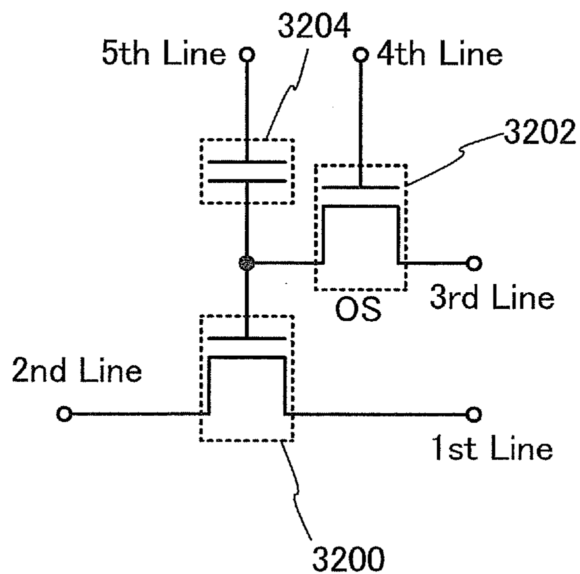


FIG. 15

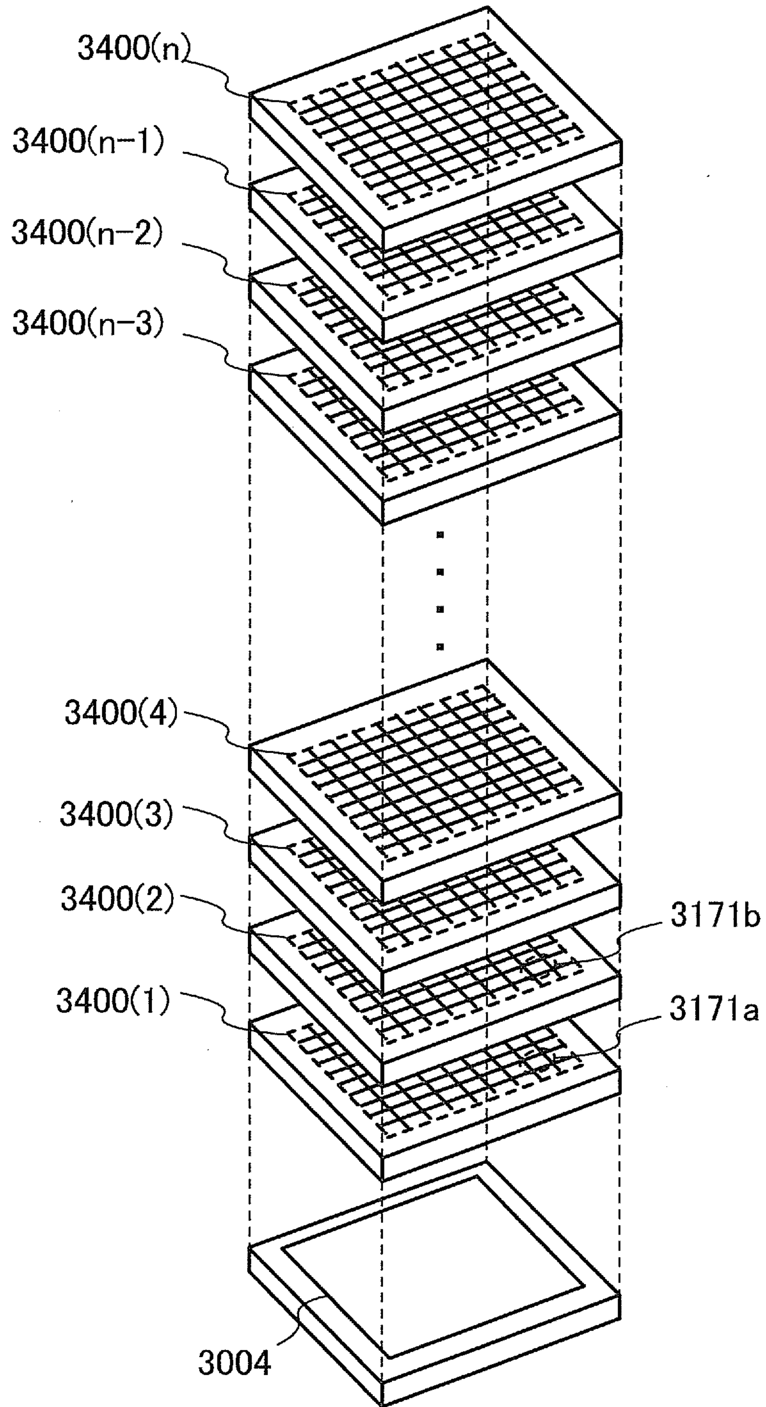


FIG. 16

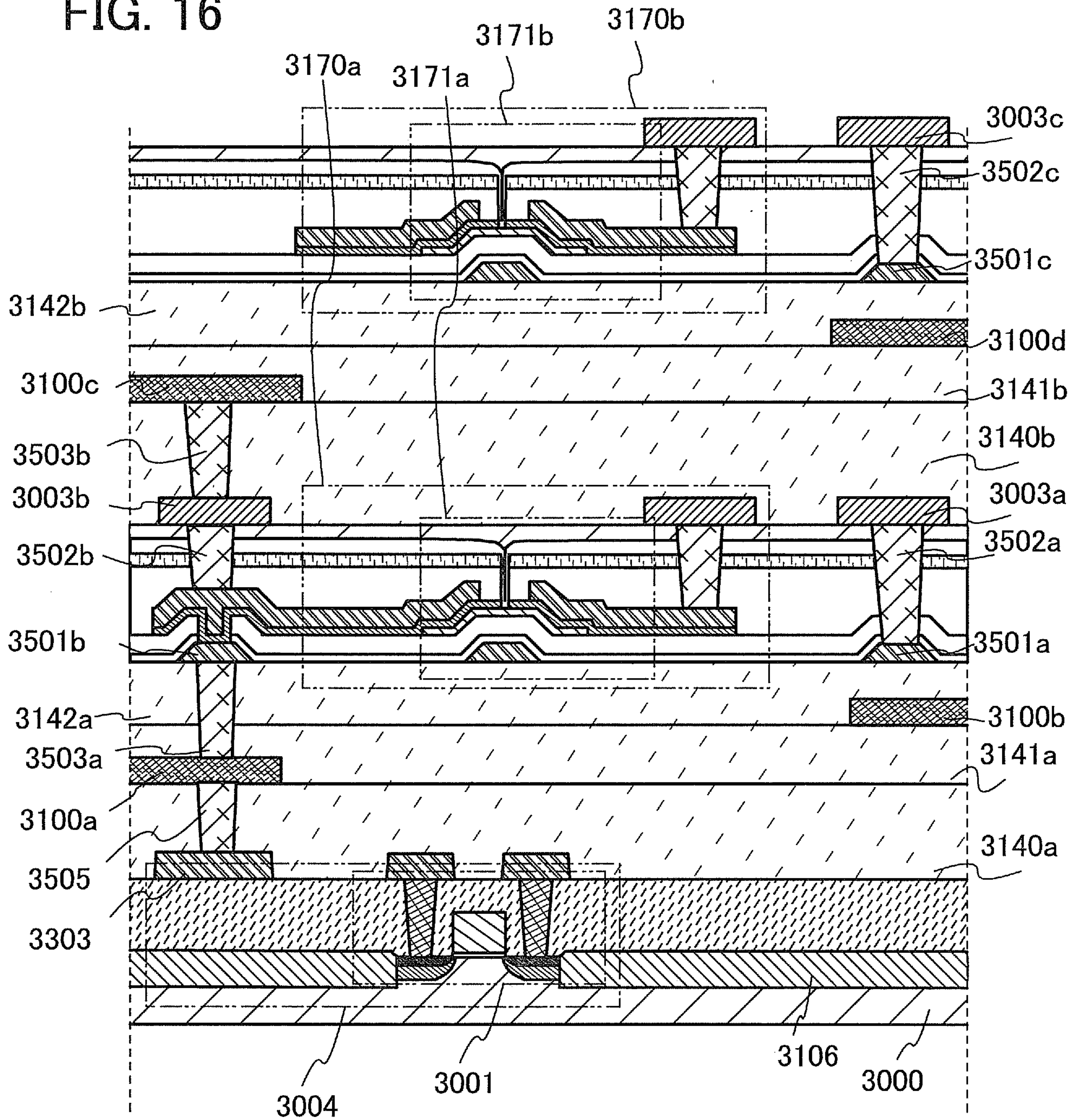


FIG. 17A

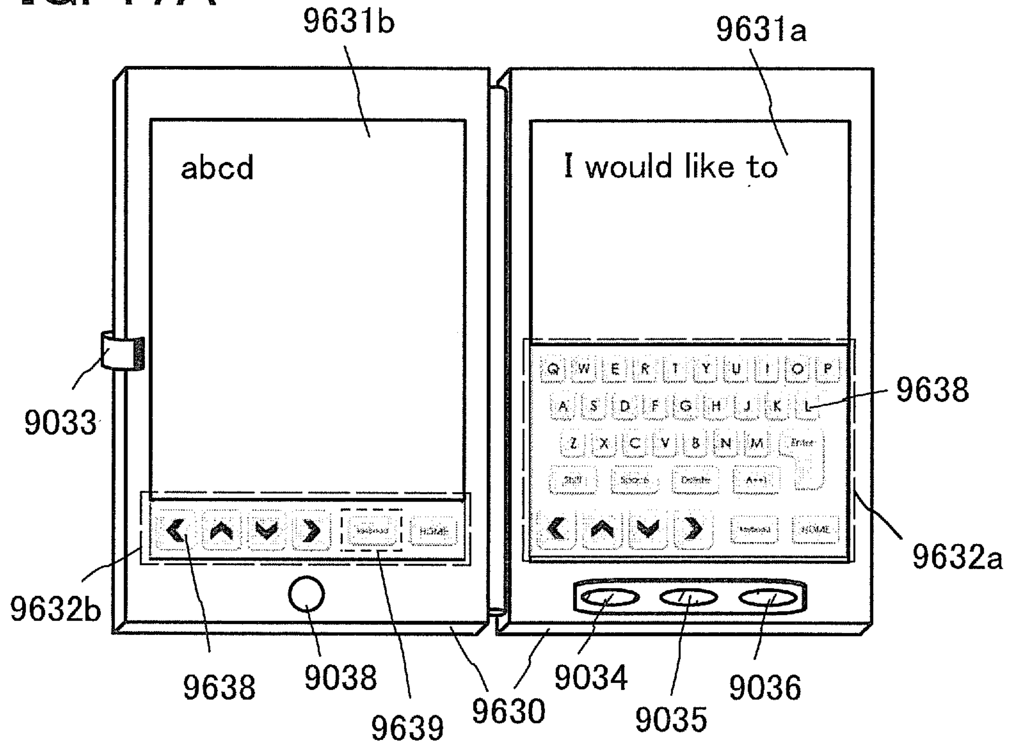



FIG. 17B

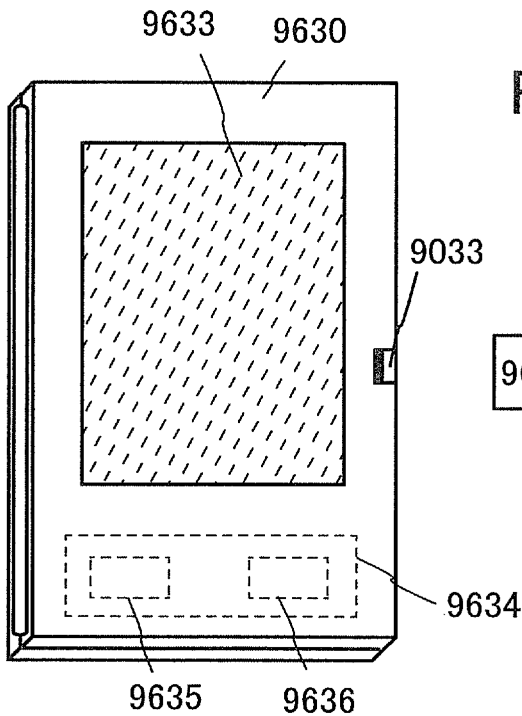
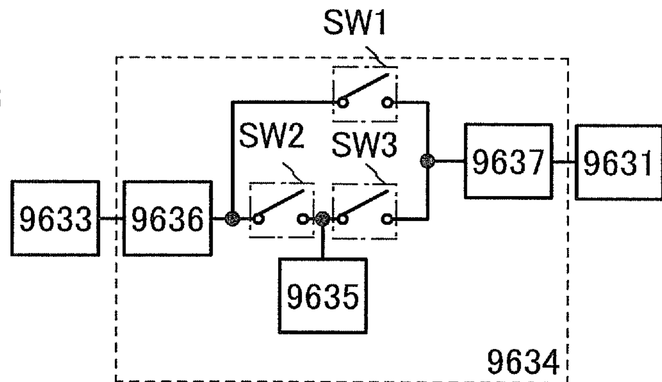



FIG. 17C



# Electronic Patent Application Fee Transmittal

| | |
|---|---|
| **Application Number:** | |
| **Filing Date:** | |
| **Title of Invention:** | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME |
| **First Named Inventor/Applicant Name:** | Shinya Sasagawa |
| **Filer:** | Eric J. Robinson |
| **Attorney Docket Number:** | 0756-10540 |

Filed as Large Entity

## Utility under 35 USC 111(a) Filing Fees

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| Utility application filing | 1011 | 1 | 280 | 280 |
| Utility Search Fee | 1111 | 1 | 600 | 600 |
| Utility Examination Fee | 1311 | 1 | 720 | 720 |
| **Pages:** | | | | |
| **Claims:** | | | | |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Post-Allowance-and-Post-Issuance:** | | | | |
| **Extension-of-Time:** | | | | |
| **Miscellaneous:** | | | | |
| | | **Total in USD ($)** | | **1600** |

# Electronic Acknowledgement Receipt

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| **EFS ID:** | 19645395 |
| **Application Number:** | 14337583 |
| **International Application Number:** | |
| **Confirmation Number:** | 7546 |
| **Title of Invention:** | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME |
| **First Named Inventor/Applicant Name:** | Shinya Sasagawa |
| **Customer Number:** | 31780 |
| **Filer:** | Eric J. Robinson/Sue Ann Carr |
| **Filer Authorized By:** | Eric J. Robinson |
| **Attorney Docket Number:** | 0756-10540 |
| **Receipt Date:** | 22-JUL-2014 |
| **Filing Date:** | |
| **Time Stamp:** | 14:22:23 |
| **Application Type:** | Utility under 35 USC 111(a) |

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| 1 | Transmittal of New Application | TRNA.pdf | 428950<br>82d7381ea1937ab7cda4828b9b94700c255f3e0a | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | Assignee showing of ownership per 37 CFR 3.73. | 373c_STATEMENT.pdf | 554915<br>35a5a51b989afed0d8d8e27d8f8b0bbabbcf728a | no | 3 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 3 | Power of Attorney | POA.pdf | 196576<br>8b312aaacfcf7a2b773739ac30644cd4015b0d89 | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 4 | Application Data Sheet | ADS_22JULY2014.pdf | 1561531<br>4c718f30b2645f180402c82acf3120bcf5bd4841 | no | 7 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 5 | Oath or Declaration filed | DEC.pdf | 1154549<br>03b457b2de383364ea265d8f4e82b875e4548fee | no | 4 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 6 | | SPEC.pdf | 1572059<br>10047e887fc37a2bd76c48c7062bb9fe4f91ff04 | yes | 71 |

**Multipart Description/PDF files in .zip description**

| Document Description | Start | End |
|---|---|---|
| Specification | 1 | 49 |
| Claims | 50 | 53 |
| Abstract | 54 | 54 |
| Drawings-only black and white line drawings | 55 | 71 |

| | | | | | |
|---|---|---|---|---|---|
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 7 | Fee Worksheet (SB06) | fee-info.pdf | 33041<br>158fd41b0e862cfb9fed79bf4d482967aa688171 | no | 2 |
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