Petitioner Bluehouse Global Ltd.

Ex. 1002

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/008,285	07/23/2013	8492840	0756-9138	8496

31780 7590 07/03/2013

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 153 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Shunpei YAMAZAKI, Setagaya, JAPAN;
Hiromichi GODO, Isehara, JAPAN;
Hideomi SUZAWA, Atsugi, JAPAN;
Shinya SASAGAWA, Chigasaki, JAPAN;
Motomu KURATA, Isehara, JAPAN;
Mayumi MIKAMI, Atsugi, JAPAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31780 7590 03/20/2013
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/008,285	01/18/2011	INV001Shunpei YAMAZAKI	0756-9138	8496

TITLE OF INVENTION: SEMICONDUCTOR DEVICE HAVING AN OXIDE SEMICONDUCTOR LAYER

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	06/20/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
RAO, SHRINIVAS H	2814	257-347000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Eric J. Robinson,
Robinson Intellectual
Property Law Office, P.C.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Semiconductor Energy Laboratory Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Atsugi-shi, Kanagawa-ken, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☒ Publication Fee (No small entity discount permitted)

☒ Advance Order - # of Copies 3

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

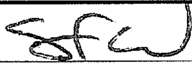
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-2280 (enclose an extra copy of this form).

PTOL-85 (Rev. 02/11)

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature 

Date June 20, 2013

Typed or printed name Sean C. Flood

Registration No. 64,378

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	13008285
Filing Date:	18-Jan-2011
Title of Invention:	SEMICONDUCTOR DEVICE HAVING AN OXIDE SEMICONDUCTOR LAYER
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Filer:	Eric J. Robinson/Doris Vasquez Soriano
Attorney Docket Number:	0756-9138

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Printed Copy of Patent - No Color	8001	3	3	9
		Total in USD ($)		**2089**

Electronic Acknowledgement Receipt	
EFS ID:	16094930
Application Number:	13008285
International Application Number:	
Confirmation Number:	8496
Title of Invention:	SEMICONDUCTOR DEVICE HAVING AN OXIDE SEMICONDUCTOR LAYER
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Doris Vasquez Soriano
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-9138
Receipt Date:	20-JUN-2013
Filing Date:	18-JAN-2011
Time Stamp:	14:54:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$2089
RAM confirmation Number	1246
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	IF.pdf	311853 ae774d317090798e8351ce95214d8998a0fe3235	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	34160 ee49d67357193b3512f68e26fe035793ec5fa04c	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	346013	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

(This IDS was originally submitted on February 14,2012 and resubmitted on April 04,2013.

Please type a plus sign (+) inside this box → [+]

PTO/SB/08A (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2811
Examiner Name	L. A. Gurley
Attorney Docket Number	0756-9138

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2011/0193080		Yamazaki et al.	08/11/2011	
		2011/0210326		Suzawa et al.	09/01/2011	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	/Shrinivas Rao/	Date Considered	05/09/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.R./

Please type a plus sign (+) inside this box → [+]

PTO/SB/08A (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known	
Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2811
Examiner Name	L. A. Gurley
Attorney Docket Number	0756-9138

Sheet 1 of 1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2011/0193080		Yamazaki et al.	08/11/2011	
		2011/0210326		Suzawa et al.	09/01/2011	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt

EFS ID:	15432136
Application Number:	13008285
International Application Number:	
Confirmation Number:	8496
Title of Invention:	SEMICONDUCTOR DEVICE HAVING AN OXIDE SEMICONDUCTOR LAYER
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Jennifer Rosenfeld
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-9138
Receipt Date:	04-APR-2013
Filing Date:	18-JAN-2011
Time Stamp:	13:56:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		RESUBMISSIONOFIDS_04APR2013.pdf	475270 328d50b318e2d55f84d66c8033f99ba97d2a1e57	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	3
	Information Disclosure Statement (IDS) Form (SB08)	4	4

Warnings:

Information:

Total Files Size (in bytes):	475270

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
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Attorney Docket No. 0756-9138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 8496
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2814
Serial No. 13/008,285	)	Examiner: Shrinivas H. Rao
Filed: January 18, 2011	)	
For: SEMICONDUCTOR DEVICE HAVING AN OXIDE SEMICONDUCTOR LAYER	)	

RESUBMISSION OF INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

It has come to Applicant's attention that the Information Disclosure Statement previously filed on February 14, 2012 was only partially considered by the Examiner. Specifically, it is noted that while it appears that the Examiner has considered the references cited therein by placing the electronic signature "/Shrinivas Rao/" in the "Examiner Signature" block and the date "06/12/2012" in the "Date Considered" block, the Examiner has not included the phrase "'ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH' along with the examiner's electronic initials" as required by the alternate electronic signature method set forth in MPEP § 609.05(b).

Further in this regard, it is noted that while a copy of the above-referenced form 1449 can be found in PAIR (Mail Room Date: 02-14-2012; Document Code: IDS; Document Description: Information Disclosure Statement (IDS) Form (SB08)), further to the telephone conversation with Examiner Rao on April, 4, 2013, the Applicant resubmits a copy of form 1449, as requested by the Examiner, which was previously filed with the Office on February 14, 2012, for the Examiner's convenience. The above-referenced Information Disclosure Statement was properly and timely filed on February 14, 2012 and is merely being resubmitted as requested by the Examiner. The Applicant respectfully requests that the Examiner provide a copy of the Form PTO-1449 in conformance with MPEP § 609.05(b) evidencing consideration of the above-referenced Information Disclosure Statement.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

Attorney Docket No. 0756-9138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 8496
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2811
Serial No. 13/008,285	)	Examiner: L. A. Gurley
Filed: January 18, 2011	)	
For: SEMICONDUCTOR DEVICE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

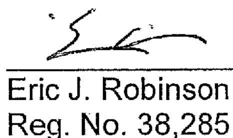
Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

This Information Disclosure Statement is being submitted before the issuance of a first Office Action on the merits, therefore, no fee is required.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

31780 7590 03/20/2013

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3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/20/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/008,285	01/18/2011	INV001Shunpei YAMAZAKI	0756-9138	8496

TITLE OF INVENTION: SEMICONDUCTOR DEVICE HAVING AN OXIDE SEMICONDUCTOR LAYER

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	06/20/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31780 7590 03/20/2013

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/008,285	01/18/2011	INV001Shunpei YAMAZAKI	0756-9138	8496

TITLE OF INVENTION: SEMICONDUCTOR DEVICE HAVING AN OXIDE SEMICONDUCTOR LAYER

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	06/20/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
RAO, SHRINIVAS H	2814	257-347000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
   (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
   1 ______________________
   2 ______________________
   3 ______________________

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies ______________________

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____________ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ____ Date ______________________________________

Typed or printed name ____ Registration No. ______________________________

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/008,285	01/18/2011	INV001Shunpei YAMAZAKI	0756-9138	8496

31780 7590 03/20/2013

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 03/20/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 194 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 194 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	**Application No.** 13/008,285	**Applicant(s)** YAMAZAKI ET AL.	
	Examiner STEVEN RAO	**Art Unit** 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *08/12/2012*.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-23*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a) ☒ All b) ☐ Some* c) ☐ None of the:

   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

Response to Amendment

Applicants' amendment filed on 08/15/2012 has been entered.

Therefore Claims 1-23 as recited in the amendment are currently pending in the Application.

Information Disclosure Statement

No further IDS after the one filed on 06/25/2012 (previously considered) have been filed in the Application.

Allowable Subject Matter

1. Claims 1 to 23 are allowed.

2. The following is an examiner's statement of reasons for allowance:

3. The Applied prior art of record does not describe/suggest the combination of elements suggested in independent claims 1, 7,14 and 22 including the fourth conductive layer in contact with the oxide semiconductor layer and wherein the source /drain electrode region in contact with channel formation region has higher resistance than other regions of the source/drain electrode (cl.22), as Applicants. Initially stated that 2011/0210326 to Suzawa was prior art in their IDS filed on 05/25/2012 (which was considered and mailed to Applicants') and have argued in their response filed on 08/15/2012 that the present Application has an earlier effective filling date and therefore effectively removing Suzawa as an applicable reference.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

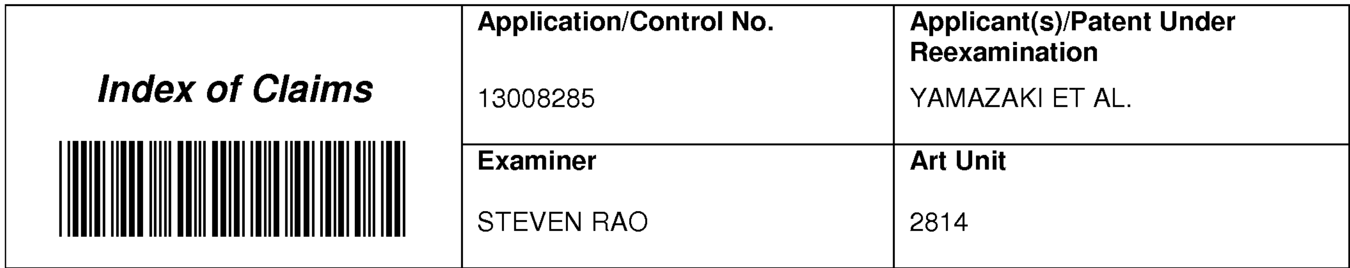
Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN RAO whose telephone number is (571)272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven H Rao/
Examiner, Art Unit 2814

/Howard Weiss/
Primary Examiner, Art Unit 2814



Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13008285	YAMAZAKI ET AL.
	Examiner	Art Unit
	STEVEN RAO	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/13/2012	01/11/2013							
	1	✓								
	2	✓	=							
	3	✓	=							
	4	✓	=							
	5	✓	=							
	6	✓	=							
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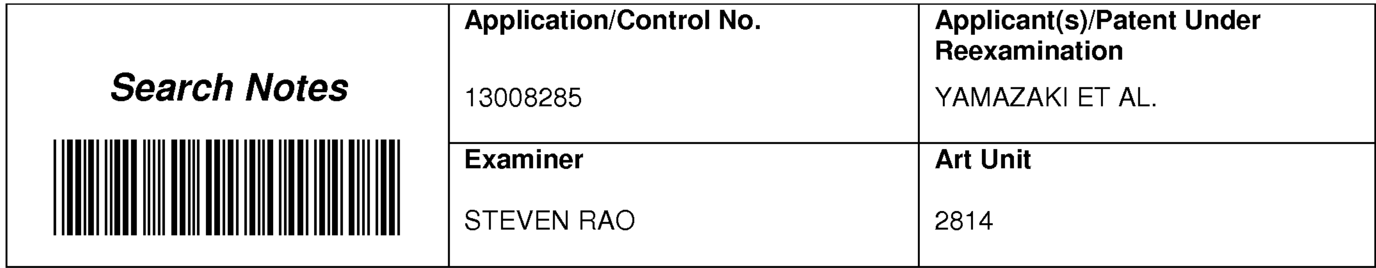

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13008285	YAMAZAKI ET AL.
	Examiner	**Art Unit**
	STEVEN RAO	2814

CPC- SEARCHED

Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner
257	347, E 29.14	03/15/13	SR

SEARCH NOTES

Search Notes	Date	Examiner
East	03/15/2013	SR

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	347, E23.14	03/15/2013	SR

Issue Classification	**Application/Control No.** 13008285	**Applicant(s)/Patent Under Reexamination** YAMAZAKI ET AL.
	Examiner STEVEN RAO	**Art Unit** 2814

CPC				
Symbol			**Type**	**Version**
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CPC Combination Sets						
Symbol			**Type**	**Set**	**Ranking**	**Version**
		/				
		/				

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
257	347

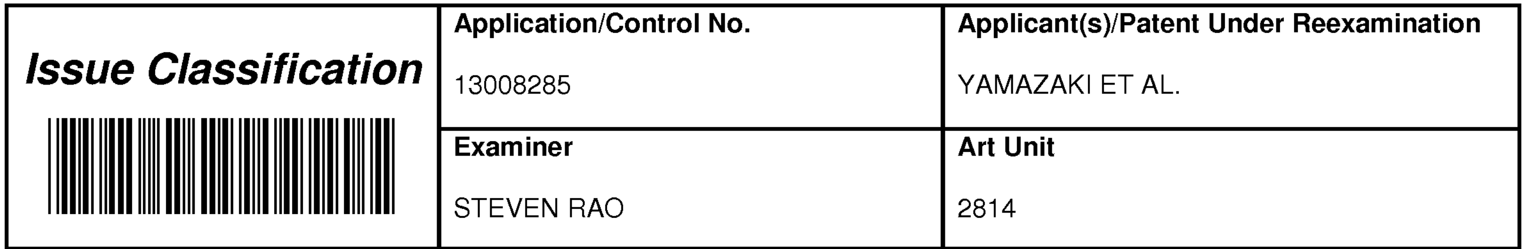
CROSS REFERENCE(S)					
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**				
257	E 29.14				

INTERNATIONAL CLASSIFICATION									
CLAIMED					**NON-CLAIMED**				
H	0	1	L	27 / 12 (2006.01.01)					

/STEVEN RAO/ Examiner.Art Unit 2814 (Assistant Examiner)	031213 (Date)	**Total Claims Allowed:** 23	
/HOWARD WEISS/ Primary Examiner.Art Unit 2814 (Primary Examiner)	03/18/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Issue Classification	Application/Control No. 13008285	Applicant(s)/Patent Under Reexamination YAMAZAKI ET AL.
	Examiner STEVEN RAO	Art Unit 2814

/STEVEN RAO/ Examiner.Art Unit 2814 (Assistant Examiner)	031213 (Date)	Total Claims Allowed: 23	
/HOWARD WEISS/ Primary Examiner.Art Unit 2814 (Primary Examiner)	03/18/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1



Issue Classification	**Application/Control No.** 13008285	**Applicant(s)/Patent Under Reexamination** YAMAZAKI ET AL.
	Examiner STEVEN RAO	**Art Unit** 2814

☒ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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	14														
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	16														

/STEVEN RAO/ Examiner.Art Unit 2814 (Assistant Examiner)	031213 (Date)	**Total Claims Allowed:** 23	
/HOWARD WEISS/ Primary Examiner.Art Unit 2814 (Primary Examiner)	03/18/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

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BIB DATA SHEET

CONFIRMATION NO. 8496

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/008,285	01/18/2011 RULE	257	2814	0756-9138

APPLICANTS

INV001Shunpei YAMAZAKI, Setagaya, JAPAN;
INV002Hiromichi GODO, Isehara, JAPAN;
INV003Hideomi SUZAWA, Atsugi, JAPAN;
INV004Shinya SASAGAWA, Chigasaki, JAPAN;
INV005Motomu KURATA, Isehara, JAPAN;
INV006Mayumi MIKAMI, Atsugi, JAPAN;

** **CONTINUING DATA** *************************

** **FOREIGN APPLICATIONS** *************************
JAPAN 2010-012540 01/22/2010

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** **
01/31/2011

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /STEVEN H RAO/ Examiner's Signature	☑ Met after Allowance /SR/ Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	13	23	4

ADDRESS

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033
UNITED STATES

TITLE

SEMICONDUCTOR DEVICE HAVING AN OXIDE SEMICONDUCTOR LAYER

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1466	No.____________ to charge/credit DEPOSIT ACCOUNT No.____________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other ________________ ☐ Credit

Attorney Docket No. 0756-9138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No.: 8496
Shunpei YAMAZAKI et al.	)	Examiner: Shrinivas H. Rao
Serial No. 13/008,285	)	Group Art Unit: 2814
Filed: January 18, 2011	)	
For: SEMICONDUCTOR DEVICE	)	

AMENDMENT

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action dated June 25, 2012, please consider the following amendments and remarks in connection with the above-identified application.

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.

Amendments to the Specification:

Please replace the title beginning at page 1, line 1, with the following amended title:

SEMICONDUCTOR DEVICE HAVING AN OXIDE SEMICONDUCTOR LAYER

REMARKS

The Official Action mailed June 25, 2012, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on January 18, 2011; February 8, 2011; April 14, 2011; May 31, 2011; February 14, 2012 and May 18, 2012.

Claims 1-23 are pending in the present application, of which claims 1, 7, 14 and 22 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

The Official Action objects to the title as not descriptive and requests a new title that is clearly indicative of the invention to which the claims are directed page 2, Paper No. 20120612). In response, the title has been changed to "SEMICONDUCTOR DEVICE HAVING AN OXIDE SEMICONDUCTOR LAYER," which is consistent with the claims and is believed to be sufficiently descriptive. If the presently amended title is not sufficiently descriptive, the Applicant respectfully requests that the Examiner further clarify why the title is not descriptive or, if possible, suggest a title believed to be sufficiently descriptive. Reconsideration of the objection is requested.

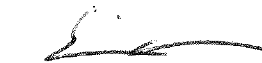
Paragraph 2 of the Official Action rejects claims 1-23 as obvious based on the combination of U.S. Publication No. 2007/0187760 to Furuta and U.S. Publication No. 2011/0210326 to Suzawa. The Applicant respectfully disagrees and traverses the rejection. In this regard, it is noted that Suzawa is not prior art to the present application. Specifically, because Suzawa's filing date of **February 17, 2011**, is **later** than the current application's filing date of **January 18, 2011**, Suzawa does not qualify as prior art under 35 U.S.C. § 102. As such, the Applicant respectfully submits that the Office has failed to provide a proper *prima facie* case for obviousness. Accordingly,

reconsideration and withdrawal of the rejections under 35 U.S.C. § 103 are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive,
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

Electronic Acknowledgement Receipt

EFS ID:	13503501
Application Number:	13008285
International Application Number:	
Confirmation Number:	8496
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Adele Stamper
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-9138
Receipt Date:	15-AUG-2012
Filing Date:	18-JAN-2011
Time Stamp:	15:12:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	AMENDMENT_15AUG2012_07569138.pdf	375152 e5990a42b9675507d4dd32b8adbd74d5fef6f518	no	4

Warnings:

Information:

Total Files Size (in bytes):	375152

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	To be Mailed
13/008,285	01/18/2011	☐

APPLICATION AS FILED – PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
			TOTAL			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT

08/15/2012	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 23	Minus	** 23	= 0	X $ =		OR	X $60=	0
Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $250=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/CHRISTINE MOLLISH/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/008,285	01/18/2011	Shunpei YAMAZAKI	0756-9138	8496

31780 7590 06/25/2012

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
06/25/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/008,285	Applicant(s) YAMAZAKI ET AL.	
	Examiner STEVEN RAO	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-23* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-23* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *18 January 2011* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/18/11 02/08,04/14,05/03,02/14.5/18/12*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgement is made of papers filed claiming priority from Japanese Patent Application No. 2010-012540 filed on January 22, 2010.

Information Disclosure Statement

The IDSs filed on 01/18/2011, 02/08/2011, 04/14/2011, 05/03/2011 and 02/14/2012 and 05/18/2012 has been considered and the initialed PTO1449s made of record.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Furuta (U.S. Patent Publication No. 2007/ 0187760 and suzuwa U.S. Patent Application No. 20110210326 both cited by Applicants; in their IDs)

With respect to claim/s 1,7 Furuta describes Furuta semiconductor device comprising:
an oxide semiconductor layer; (Fig. 9a 110) 5
a source electrode (fig. 9A 102) in contact with the oxide semiconductor layer comprising: (figs. 102 in electrical contact with 110)

a first conductive layer; (fig.9a,110a)and

a second conductive layer; (Fig.9a,103)
a drain electrode (Fig. (a, second 102) in contact with the oxide semiconductor layer (fig, (a, 102 in contact with 110) comprising:

a third conductive layer; (fig. 8C,161) and

Furuta does not specifically mention a fourth conductive layer.

However Suzawa describes in para 130 etc. a fourth wiring line (a fourth conductive layer) to vertically integrate the elements of the transistor and form a miniature transistor that operates at high speed and low power consumption.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Suzawa's fourth conductive layer in Furuta's device, the motivation for the combination is to vertically integrate the elements of the transistor and form a miniature transistor that operates at high speed and low power consumption. (Suzawa para 017).
The remaining limitations of claim/s 1,7 :

a gate electrode overlapping with the oxide semiconductor layer; (Furuta fig. 9a, 106) and a gate insulating layer provided (Furuta 104)between the oxide semiconductor layer and the gate electrode, (fig.9 A)

wherein the second conductive layer extends beyond an end portion of the first conductive layer, (Furuta fig. 9a 119 a extends beyond 103)

wherein the fourth conductive layer extends beyond an end portion of the third conductive layer, (Suzuwa figs,244 extends beyond 242)and

wherein the end portion of the first conductive layer and the end portion of the third conductive layer are opposed to each other. (Furuta fig. 9A) .

second conductive layer has a higher resistance than the first conductive layer, and wherein the fourth conductive layer is over the third conductive layer, and the fourth conductive layer has a higher resistance than the third conductive layer. (Furuta abstract lines 3,5 etc.)

With respect to claim/s, 2,10,18,19 Furuta describes the semiconductor device according to claim 1, wherein the first conductive layer, the second conductive layer, the third conductive layer and the fourth conductive layer each has a tapered shape. (Furua figs. three tapered layers Suzawa figs. four tapered layers)

With respect to claims 3,15 Furuta describes the semiconductor device according to claim 1, further comprising:
a first sidewall insulating layer over the second conductive layer and in contact with the end portion of the first conductive layer; (Suzawa fig.2 E, 254a)
and a second side wall insulating layer over the fourth conductive layer and in contact with the end portion of the third conductive layer. Suzawa fig.4C).

With respect to claims 4,11 Furuta describes the semiconductor device according to claim 1, wherein a material of the second conductive layer and a material of the fourth conductive layer are a nitride of a metal. (Suzawa para 0024)

With respect to claims 5,12,20 Furuta describes the semiconductor device according to claim 1, wherein a thickness of the second conductive layer and a thickness of the fourth conductive layer are from 5 nm to 15 nm. (Furuta para 0024)

With respect to claims 6,13,21 Furuat describes the semiconductor device according to claim 1, further comprising:
a first insulating layer provided between the oxide semiconductor layer and the source electrode; and a second insulating layer provided between the oxide semiconductor layer and the drain electrode, (Furuta figs. 4 between s/d 2 and 3) wherein the source electrode and the drain electrode are in contact with the oxide semiconductor layer at end portions of the source electrode and the drain electrode. (Furuta figs., Suzawa figs.)

With respect to claim 8 Furuta describes the semiconductor device according to claim 7, wherein the first conductive layer and the third conductive layer are in contact with the oxide semiconductor layer. (Furuta figs., Suzawa figs,)

With respect to claims 9. 16 Furuta he semiconductor device according to claim 7, wherein the second conductive layer extends beyond an end portion of the first conductive layer, wherein the fourth conductive layer extends beyond an end portion of the third conductive layer, and wherein the end portion of the first conductive layer and the end portion of the third conductive layer are opposed to each other.

With respect to 14 Furuata describes a semiconductor device comprising:
an oxide semiconductor layer; a source electrode comprising: a first conductive layer; and a second conductive layer in contact with the oxide semiconductor layer; a drain electrode comprising: a third conductive layer; and a fourth conductive layer in contact with the oxide semiconductor layer; a gate electrode overlapping with the oxide semiconductor layer; and a gate insulating layer provided between the oxide semiconductor layer and the
gate electrode, wherein the first conductive layer is over the second conductive layer,

and the second conductive layer has a higher resistance than the first conductive layer, and wherein the third conductive layer is over the fourth conductive layer, and the fourth conductive layer has a higher resistance than the third conductive layer. (rejected for reasons under claims 1,7 above)

With respect to claim 22 Futura describes a semiconductor device comprising:
an oxide semiconductor layer including a channel formation region;
a source electrode including a region in contact with the channel formation region; a drain electrode including a region in contact with the channel formation region; a gate electrode overlapping with the channel formation region; and
a gate insulating layer provided between the oxide semiconductor layer and the gate electrode, wherein the region of the source electrode has a higher resistance than other regions of the source electrode, and wherein the region of the drain electrode has a higher resistance than other regions of the drain electrode. (rejected for reasons under claim 7 etc. above).

With respect to claim 23 Futura describes the semiconductor device according to claim 22, further comprising: a first insulating layer provided between the oxide semiconductor layer and the source electrode; and a second insulating layer provided between the oxide semiconductor layer and the drain electrode, wherein the source electrode and the drain electrode are in contact with the oxide semiconductor layer at end portions of the source electrode and the drain electrode. (rejected for reasons under claims 1,7 14 etc. above).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN RAO whose telephone number is (571)272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven H Rao/
Examiner, Art Unit 2814

/Howard Weiss/
Primary Examiner, Art Unit 2814

Notice of References Cited	Application/Control No. 13/008,285	Applicant(s)/Patent Under Reexamination YAMAZAKI ET AL.	
	Examiner STEVEN RAO	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2007/0187760	08-2007	Furuta et al.	257/347
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/008,285
Filing Date	01/18/2011
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2811
Examiner Name	Unknown
Attorney Docket Number	0756-9138

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		5,744,864		Cillessen et al.	04/28/1998	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

Examiner Signature	/Shrinivas Rao/	Date Considered	06/12/2012

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Sheet 1 of 1

Complete if Known	
Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2811
Examiner Name	L. A. Gurley
Attorney Docket Number	0756-9138

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] *(if known)*	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2011/0193080		Yamazaki et al.	08/11/2011	
		2011/0210326		Suzawa et al.	09/01/2011	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] *(if known)*	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Complete if Known	
Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2811
Examiner Name	Unknown
Attorney Docket Number	0756-9138

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-2007/0108446	05-17-2007	AKIMOTO.K	
		US-2007/0187760	08-16-2007	FURUTA.M et al.	
		US-2009/0186437	07-23-2009	AKIMOTO.K	
		US-2009/0186445	07-23-2009	AKIMOTO.K	
		US-2009/0189156	07-30-2009	AKIMOTO.K	
		US-2009/0189155	07-30-2009	AKIMOTO.K	
		US-2007/0278490	12-06-2007	HIRAO.T et al.	
		US-7576394	08-18-2009	FURUTA.M et al.	
		US-2009/0269881	10-29-2009	FURUTA.M et al.	
		US-2010/0003783	01-07-2010	AKIMOTO.K	
		US-2010/0038639	02-18-2010	AKIMOTO.K	
		US-7598520	10-06-2009	HIRAO.T et al.	
		US-2009/0286351	11-19-2009	HIRAO.T et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] -Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		WO-2007/058329	05-24-2007			Eng.
		WO-2007/089048	08-09-2007			Eng.
		WO-2007/142167	12-13-2007			Eng.

Examiner Signature	/Shrinivas Rao/	Date Considered	06/12/2012

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Substitute for form 1449/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	13/008,285
	Filing Date	January 18, 2011
	First Named Inventor	Shunpei YAMAZAKI et al.
(Use as many sheets as necessary)	Art Unit	2811
	Examiner Name	Unknown
Sheet 2 of 2	Attorney Docket Number	0756-9138

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		INTERNATIONAL SEARCH REPORT (Application No.PCT/JP2010/073886) Dated February 15, 2011.	Eng.
		WRITTEN OPINION (Application No.PCT/JP2010/073886) Dated February 15, 2011.	Eng.

Examiner Signature	/Shrinivas Rao/	Date Considered	06/12/2012

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

Complete if Known	
Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2814
Examiner Name	S. Rao
Attorney Docket Number	0756-9138

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Examiner Initials*	Cite No.[1]	Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

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Sheet	1	of	12

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Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2811
Examiner Name	Unknown
Attorney Docket Number	0756-9138

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Examiner Signature	/Shrinivas Rao/	Date Considered	06/12/2012

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Sheet 2 of 12

Complete if Known	
Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2811
Examiner Name	Unknown
Attorney Docket Number	0756-9138

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		JP-63-210024A	08-31-1988			Full

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	13/008,285
				Filing Date	January 18, 2011
				First Named Inventor	Shunpei YAMAZAKI et al.
				Art Unit	2811
(Use as many sheets as necessary)				Examiner Name	Unknown
Sheet	3	of	12	Attorney Docket Number	0756-9138

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Art Unit	2811
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	13/008,285
				Filing Date	January 18, 2011
				First Named Inventor	Shunpei YAMAZAKI et al.
(Use as many sheets as necessary)				Art Unit	2811
				Examiner Name	Unknown
Sheet	6	of	12	Attorney Docket Number	0756-9138

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		JANOTTI.A et al., "NATIVE POINT DEFECTS IN ZnO,", PHYS. REV. B (PHYSICAL REVIEW. B), October 4, 2007, Vol. 76, No. 16, pp. 165202-1-165202-22.	Eng.
		PARK.J et al., "ELECTRONIC TRANSPORT PROPERTIES OF AMORPHOUS INDIUM-GALLIUM-ZINC OXIDE SEMICONDUCTOR UPON EXPOSURE TO WATER,", APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), 2008, Vol. 92, pp. 072104-1-072104-3.	Eng.
		HSIEH.H et al., "P-29:Modeling of Amorphous Oxide Semiconductor Thin Film Transistors and Subgap Density of States,", SID DIGEST '08 : SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, 2008, Vol. 39, pp. 1277-1280.	Eng.
		JANOTTI.A et al., "Oxygen Vacancies In ZnO,", APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), 2005, Vol. 87, pp. 122102-1-122102-3.	Eng.
		OBA.F et al., "Defect energetics in ZnO: A hybrid Hartree-Fock density functional study,", PHYS. REV. B (PHYSICAL REVIEW. B), 2008, Vol. 77, pp. 245202-1-245202-6.	Eng.
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		HOSONO.H et al., "Working hypothesis to explore novel wide band gap electrically conducting amorphous oxides and examples,", J. NON-CRYST. SOLIDS (JOURNAL OF NON-CRYSTALLINE SOLIDS), 1996, Vol. 198-200, pp. 165-169.	Eng.
		MO.Y et al., "Amorphous Oxide TFT Backplanes for Large Size AMOLED Displays,", IDW '08 : PROCEEDINGS OF THE 6TH INTERNATIONAL DISPLAY WORKSHOPS, December 3, 2008, pp. 581-584.	Eng.
		KIM.S et al., "High-Performance oxide thin film transistors passivated by various gas plasmas,", 214TH ECS MEETING, 2008, No. 2317.	Eng.
		CLARK.S et al., "FIRST PRINCIPLES METHODS USING CASTEP,", Zeitschrift fur Kristallographie, 2005, Vol. 220, pp. 567-570.	Eng.

Examiner Signature	/Shrinivas Rao/	Date Considered	06/12/2012

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	13/008,285
				Filing Date	January 18, 2011
				First Named Inventor	Shunpei YAMAZAKI et al.
(Use as many sheets as necessary)				Art Unit	2811
				Examiner Name	Unknown
Sheet	12	of	12	Attorney Docket Number	0756-9138

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		LANY.S et al., "Dopability, Intrinsic Conductivity, and Nonstoichiometry of Transparent Conducting Oxides,", PHYS. REV. LETT. (PHYSICAL REVIEW LETTERS), January 26, 2007, Vol. 98, pp. 045501-1-045501-4.	Eng.
		PARK.J et al., "Dry etching of ZnO films and plasma-induced damage to optical properties,", J. VAC. SCI. TECHNOL. B (JOURNAL OF VACUUM SCIENCE & TECHNOLOGY B), March 1, 2003, Vol. 21, No. 2, pp. 800-803.	Eng.
		OH.M et al., "IMPROVING THE GATE STABILITY OF ZNO THIN-FILM TRANSISTORS WITH ALUMINUM OXIDE DIELECTRIC LAYERS,", J. ELECTROCHEM. SOC. (JOURNAL OF THE ELECTROCHEMICAL SOCIETY), 2008, Vol. 155, No. 12, pp. H1009-H1014.	Eng.
		UENO.K et al., "FIELD-EFFECT TRANSISTOR ON SrTiO3 WITH SPUTTERED Al2O3 GATE INSULATOR,", APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), September 1, 2003, Vol. 83, No. 9, pp. 1755-1757.	Eng.

Examiner Signature	/Shrinivas Rao/	Date Considered	06/12/2012

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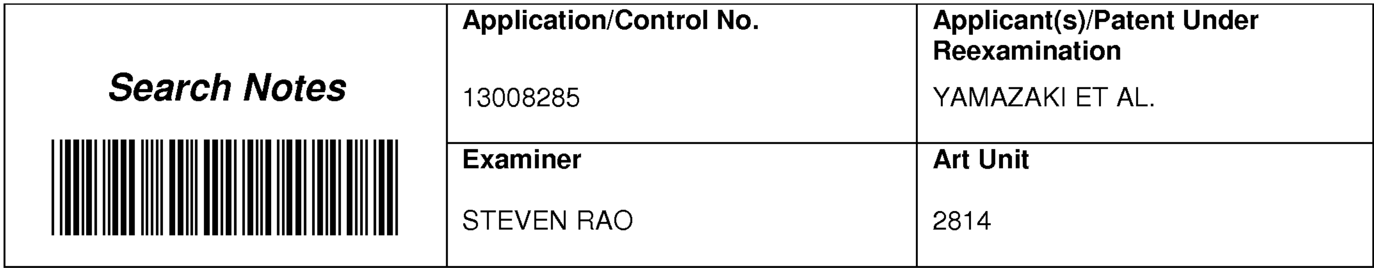


Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13008285	YAMAZAKI ET AL.
	Examiner	**Art Unit**
	STEVEN RAO	2814

SEARCHED

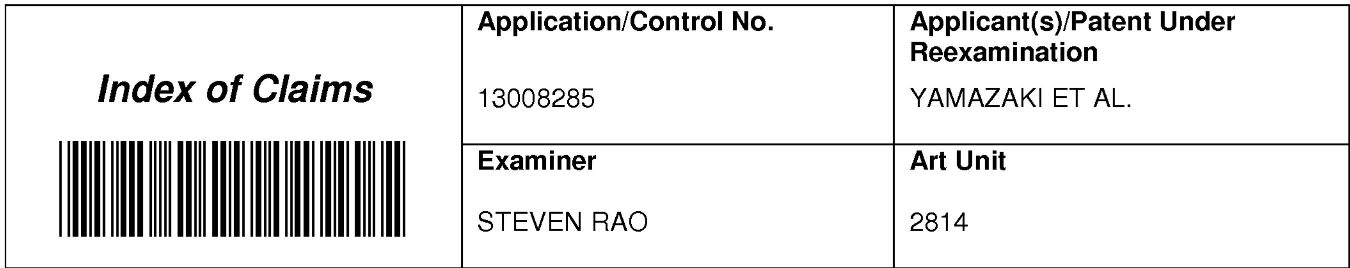
Class	Subclass	Date	Examiner
257	347, E 29.14	06/12/2012	SR

SEARCH NOTES

Search Notes	Date	Examiner
East	06/12/12	SR

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner



Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13008285	YAMAZAKI ET AL.
	Examiner	**Art Unit**
	STEVEN RAO	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

CLAIM		DATE								
Final	Original	06/13/2012								
	1	✓								
	2	✓								
	3	✓								
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	1	of	2

Complete if Known	
Application Number	
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	
Examiner Name	
Attorney Docket Number	0756-9138

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6,727,522		Kawasaki et al.	04/27/2004	
		7,061,014		Hosono et al.	06/13/2006	
		5,648,662		Zhang et al.	07/15/1997	
		2009/0134383		Imahayashi et al.	05/28/2009	
		2008/0048183		Ohsawa et al.	02/28/2008	
		2010/0297809		Imahayashi et al.	11/25/2010	

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		JP	60-198861			10/08/1985		Full
		JP	08-264794			10/11/1996		Full
		JP	11-505377			05/18/1999		Abst.
		JP	2000-150900			05/30/2000		Abst.
		JP	2004-103957			04/02/2004		Abst.

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		Nomura et al., "Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Amorphous Oxide Semiconductors," NATURE, November 25, 2004, Vol. 432, pp. 488-492.	Eng.

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Complete if Known	
Application Number	
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	
Examiner Name	
Attorney Docket Number	0756-9138

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		Prins et al., "A Ferroelectric Transparent Thin-Film Transistor," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), June 17, 1996, Vol. 68, No. 25, pp. 3650-3652.	Eng.
		Nakamura et al., "The Phase Relations In the In_2O_3-Ga_2ZnO_4-ZnO System at 1350°C," JOURNAL OF SOLID STATE CHEMISTRY, August 1, 1991, Vol. 93, No. 2, pp. 298-315.	Eng.
		Kimizuka et al., "Syntheses and Single-Crystal Data of Homologous Compounds, $In_2O_3(ZnO)_m$ (m = 3, 4, and 5), $InGaO_3(ZnO)_3$, and $Ga_2O_3(ZnO)_m$ (m = 7, 8, 9, and 16) in the In_2O_3-$ZnGa_2O_4$-ZnO System," JOURNAL OF SOLID STATE CHEMISTRY, April 1, 1995, Vol. 116, No. 1, pp. 170-178.	Eng.
		Nakamura et al., "Syntheses and crystal structures of new homologous compounds, indium iron zinc oxides ($InFeO_3(ZnO)_m$) (m: natural number) and related compounds," KOTAI BUTSURI (SOLID STATE PHYSICS), 1993, Vol. 28, No. 5, pp. 317-327.	Full
		Nomura et al., "Thin-Film Transistor Fabricated in Single-Crystalline Transparent Oxide Semiconductor," SCIENCE, May 23, 2003, Vol. 300, No. 5623, pp. 1269-1272.	Eng.

Examiner Signature	/Shrinivas Rao/	Date Considered	06/12/2012

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IFW

Docket No.:0756-9138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of	)	
Shunpei YAMAZAKI, et al.	)	
Serial No. 13/008,285	)	Group Art Unit: 2814
Filed: January 18, 2011	)	Examiner: Shrinvas Rao
For: SEMICONDUCTOR DEVICE	)	
	)	

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REQUEST FOR STATUS

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Sir:

To date the undersigned attorney of record has received no action in the above-identified patent application. Please provide the undersigned with a status report of the application in writing.

Respectfully submitted,

[signature]

Eric J. Robinson
Reg. No. 38,285

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Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789
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(use as many sheets as necessary)	**Filing Date**	January 18, 2011
	First Named Inventor	Shunpei YAMAZAKI et al.
	Group Art Unit	2814
	Examiner Name	S. Rao
Sheet 1 of 1	**Attorney Docket Number**	0756-9138

U.S. PATENT DOCUMENTS

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		2003/0146452		Chiang	08/07/2003	

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EFS ID:	12813674
Application Number:	13008285
International Application Number:	
Confirmation Number:	8496
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Doris Vasquez Soriano
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-9138
Receipt Date:	18-MAY-2012
Filing Date:	18-JAN-2011
Time Stamp:	14:55:08
Application Type:	Utility under 35 USC 111(a)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 8496
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2814
Serial No. 13/008,285	)	Examiner: S. Rao
Filed: January 18, 2011	)	
For: SEMICONDUCTOR DEVICE	)	

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Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

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Sheet 1 of 1

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Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2811
Examiner Name	L. A. Gurley
Attorney Docket Number	0756-9138

U.S. PATENT DOCUMENTS

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		2011/0193080		Yamazaki et al.	08/11/2011	
		2011/0210326		Suzawa et al.	09/01/2011	

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EFS ID:	12070735
Application Number:	13008285
International Application Number:	
Confirmation Number:	8496
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Doris Vasquez Soriano
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-9138
Receipt Date:	14-FEB-2012
Filing Date:	18-JAN-2011
Time Stamp:	13:23:52
Application Type:	Utility under 35 USC 111(a)

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Attorney Docket No. 0756-9138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 8496
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2811
Serial No. 13/008,285	)	Examiner: L. A. Gurley
Filed: January 18, 2011	)	
For: SEMICONDUCTOR DEVICE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

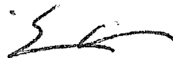
Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

This Information Disclosure Statement is being submitted before the issuance of a first Office Action on the merits, therefore, no fee is required.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

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This is to certify that the annexed is a true copy of the following application as filed with this Office.

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特許庁長官
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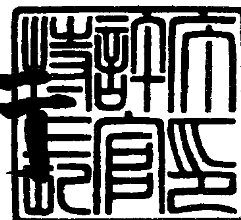

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【あて先】　特許庁長官　細野　哲弘　殿
【発明者】
　【住所又は居所】　神奈川県厚木市長谷３９８番地　株式会社半導体エネルギー研究所内
　【氏名】　山崎　舜平
【発明者】
　【住所又は居所】　神奈川県厚木市長谷３９８番地　株式会社半導体エネルギー研究所内
　【氏名】　郷戸　宏充
【発明者】
　【住所又は居所】　神奈川県厚木市長谷３９８番地　株式会社半導体エネルギー研究所内
　【氏名】　須沢　英臣
【発明者】
　【住所又は居所】　神奈川県厚木市長谷３９８番地　株式会社半導体エネルギー研究所内
　【氏名】　笹川　慎也
【発明者】
　【住所又は居所】　神奈川県厚木市長谷３９８番地　株式会社半導体エネルギー研究所内
　【氏名】　倉田　求
【発明者】
　【住所又は居所】　神奈川県厚木市長谷３９８番地　株式会社半導体エネルギー研究所内
　【氏名】　三上　真弓
【特許出願人】
　【識別番号】　000153878
　【氏名又は名称】　株式会社半導体エネルギー研究所
　【代表者】　山崎　舜平
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　【物件名】　特許請求の範囲　1
　【物件名】　明細書　1
　【物件名】　図面　1
　【物件名】　要約書　1

【書類名】明細書
【発明の名称】半導体装置
【技術分野】
【０００１】
発明の技術分野は、半導体装置に関する。ここで、半導体装置とは、半導体特性を利用することで機能する素子および装置全般を指すものである。
【背景技術】
【０００２】
金属酸化物は多様に存在し、さまざまな用途に用いられている。酸化インジウムはよく知られた材料であり、液晶表示装置などに必要とされる透明電極の材料として用いられている。
【０００３】
金属酸化物の中には半導体特性を示すものがある。半導体特性を示す金属酸化物としては、例えば、酸化タングステン、酸化錫、酸化インジウム、酸化亜鉛などがあり、このような金属酸化物をチャネル形成領域に用いた薄膜トランジスタが既に知られている（例えば、特許文献１乃至特許文献４、非特許文献１等参照）。
【０００４】
ところで、金属酸化物には、一元系酸化物のみでなく多元系酸化物も知られている。例えば、ホモロガス相を有するＩｎＧａＯ$_{3}$（ＺｎＯ）$_{m}$（ｍ：自然数）は、Ｉｎ、ＧａおよびＺｎを有する多元系酸化物半導体として知られている（例えば、非特許文献２乃至非特許文献４等参照）。
【０００５】
そして、上記のようなＩｎ－Ｇａ－Ｚｎ系酸化物で構成される酸化物半導体も、薄膜トランジスタのチャネル形成領域に適用可能であることが確認されている（例えば、特許文献５、非特許文献５および非特許文献６等参照）。
【先行技術文献】
【特許文献】
【０００６】
【特許文献１】特開昭６０－１９８８６１号公報
【特許文献２】特開平８－２６４７９４号公報
【特許文献３】特表平１１－５０５３７７号公報
【特許文献４】特開２０００－１５０９００号公報
【特許文献５】特開２００４－１０３９５７号公報
【非特許文献】
【０００７】
【非特許文献１】Ｍ．　Ｗ．　Ｐｒｉｎｓ，　Ｋ．　Ｏ．　Ｇｒｏｓｓｅ－Ｈｏｌｚ，　Ｇ．　Ｍｕｌｌｅｒ，　Ｊ．　Ｆ．　Ｍ．　Ｃｉｌｌｅｓｓｅｎ，　Ｊ．　Ｂ．　Ｇｉｅｓｂｅｒｓ，　Ｒ．　Ｐ．　Ｗｅｅｎｉｎｇ，　ａｎｄ　Ｒ．　Ｍ．　Ｗｏｌｆ、「Ａ　ｆｅｒｒｏｅｌｅｃｔｒｉｃ　ｔｒａｎｓｐａｒｅｎｔ　ｔｈｉｎ－ｆｉｌｍ　ｔｒａｎｓｉｓｔｏｒ」、Ａｐｐｌ．　Ｐｈｙｓ．　Ｌｅｔｔ．、１７　Ｊｕｎｅ　１９９６、　Ｖｏｌ．６８　ｐ．３６５０－３６５２
【非特許文献２】Ｍ．　Ｎａｋａｍｕｒａ，　Ｎ．　Ｋｉｍｉｚｕｋａ，　ａｎｄ　Ｔ．　Ｍｏｈｒｉ、「Ｔｈｅ　Ｐｈａｓｅ　Ｒｅｌａｔｉｏｎｓ　ｉｎ　ｔｈｅ　Ｉｎ２Ｏ３－Ｇａ２ＺｎＯ４－ＺｎＯ　Ｓｙｓｔｅｍ　ａｔ　１３５０℃」、Ｊ．　Ｓｏｌｉｄ　Ｓｔａｔｅ　Ｃｈｅｍ．、１９９１、Ｖｏｌ．９３，　ｐ．２９８－３１５
【非特許文献３】Ｎ．　Ｋｉｍｉｚｕｋａ，　Ｍ．　Ｉｓｏｂｅ，　ａｎｄ　Ｍ．　Ｎａｋａｍｕｒａ、「Ｓｙｎｔｈｅｓｅｓ　ａｎｄ　Ｓｉｎｇｌｅ－Ｃｒｙｓｔａｌ　Ｄａｔａ　ｏｆ　Ｈｏｍｏｌｏｇｏｕｓ　Ｃｏｍｐｏｕｎｄｓ，　Ｉｎ２Ｏ３（ＺｎＯ）ｍ（ｍ＝３，４，　ａｎｄ　５），　ＩｎＧａＯ３（ＺｎＯ）３，　ａｎｄ

Ｇａ２Ｏ３（ＺｎＯ）ｍ（ｍ＝７，８，９， ａｎｄ １６） ｉｎ ｔｈｅ Ｉｎ２Ｏ３－ＺｎＧａ２Ｏ４－ＺｎＯ Ｓｙｓｔｅｍ」、 Ｊ． Ｓｏｌｉｄ Ｓｔａｔｅ Ｃｈｅｍ．、１９９５、Ｖｏｌ．１１６， ｐ．１７０－１７８
【非特許文献４】中村真佐樹、君塚昇、毛利尚彦、磯部光正、「ホモロガス相、ＩｎＦｅＯ３（ＺｎＯ）ｍ（ｍ：自然数）とその同型化合物の合成および結晶構造」、固体物理、１９９３年、Ｖｏｌ．２８、Ｎｏ．５、ｐ．３１７－３２７
【非特許文献５】Ｋ． Ｎｏｍｕｒａ， Ｈ． Ｏｈｔａ， Ｋ． Ｕｅｄａ， Ｔ． Ｋａｍｉｙａ， Ｍ． Ｈｉｒａｎｏ， ａｎｄ Ｈ． Ｈｏｓｏｎｏ、「Ｔｈｉｎ－ｆｉｌｍ ｔｒａｎｓｉｓｔｏｒ ｆａｂｒｉｃａｔｅｄ ｉｎ ｓｉｎｇｌｅ－ｃｒｙｓｔａｌｌｉｎｅ ｔｒａｎｓｐａｒｅｎｔ ｏｘｉｄｅ ｓｅｍｉｃｏｎｄｕｃｔｏｒ」、ＳＣＩＥＮＣＥ、２００３、Ｖｏｌ．３００、ｐ．１２６９－１２７２
【非特許文献６】Ｋ． Ｎｏｍｕｒａ， Ｈ． Ｏｈｔａ， Ａ． Ｔａｋａｇｉ， Ｔ． Ｋａｍｉｙａ， Ｍ． Ｈｉｒａｎｏ， ａｎｄ Ｈ． Ｈｏｓｏｎｏ、「Ｒｏｏｍ－ｔｅｍｐｅｒａｔｕｒｅ ｆａｂｒｉｃａｔｉｏｎ ｏｆ ｔｒａｎｓｐａｒｅｎｔ ｆｌｅｘｉｂｌｅ ｔｈｉｎ－ｆｉｌｍ ｔｒａｎｓｉｓｔｏｒｓ ｕｓｉｎｇ ａｍｏｒｐｈｏｕｓ ｏｘｉｄｅ ｓｅｍｉｃｏｎｄｕｃｔｏｒｓ」、ＮＡＴＵＲＥ、２００４、Ｖｏｌ．４３２ ｐ．４８８－４９２
【発明の概要】
【発明が解決しようとする課題】
【０００８】
ところで、トランジスタの動作の高速化、トランジスタの低消費電力化、低価格化、などを達成するためには、トランジスタの微細化は必須である。
【０００９】
トランジスタを微細化する場合には、製造工程において発生する不良が大きな問題となる。例えば、ソース電極およびドレイン電極と、チャネル形成領域とは電気的に接続されるが、微細化に伴う被覆性の低下などに起因して、断線や接続不良などが生じうる。
【００１０】
また、トランジスタを微細化する場合には、短チャネル効果の問題も生じる。短チャネル効果とは、トランジスタの微細化（チャネル長（Ｌ）の縮小）に伴って顕在化する電気特性の劣化である。短チャネル効果は、ドレインの電界の効果がソースにまでおよぶことに起因するものである。短チャネル効果の具体例としては、しきい値電圧の低下、Ｓ値の増大、漏れ電流の増大などがある。特に、酸化物半導体を用いたトランジスタは、室温においてシリコンを用いたトランジスタと比較してオフ電流が小さいことが知られており、これは熱励起により生じるキャリアが少ない、つまりキャリア密度が小さいためと考えられる。キャリア密度が小さい材料を用いたトランジスタでは、しきい値電圧の低下などの短チャネル効果が現れやすい傾向にある。
【００１１】
そこで、開示する発明の一態様は、不良を抑制しつつ微細化を達成した半導体装置の提供を目的の一とする。または、良好な特性を維持しつつ微細化を達成した半導体装置の提供を目的の一とする。
【課題を解決するための手段】
【００１２】
開示する発明の一態様は、酸化物半導体層と、酸化物半導体層と接するソース電極及びドレイン電極と、酸化物半導体層と重なるゲート電極と、酸化物半導体層とゲート電極との間に設けられたゲート絶縁層と、を有し、ソース電極またはドレイン電極は、第１の導電層と、第１の導電層の端面よりチャネル長方向に伸長した領域を有する第２の導電層と、を含む半導体装置である。
【００１３】
上記の半導体装置において、第１の導電層および第２の導電層はテーパー形状であるのが

好ましい。
【００１４】
また、上記の半導体装置において、第２の導電層の領域の上にサイドウォール絶縁層を有するのが好ましい。
【００１５】
また、開示する発明の別の一態様は、酸化物半導体層と、酸化物半導体層と接するソース電極及びドレイン電極と、酸化物半導体層と重なるゲート電極と、酸化物半導体層とゲート電極との間に設けられたゲート絶縁層と、を有し、ソース電極及びドレイン電極は、第１の導電層と、第１の導電層よりも高抵抗である第２の導電層と、を含み、第２の導電層において、酸化物半導体層と接する半導体装置である。
【００１６】
また、上記の半導体装置において、第２の導電層は、金属の窒化物であるのが好ましい。
【００１７】
また、上記の半導体装置において、第２の導電層の膜厚は５ｎｍ乃至１５ｎｍであるのが好ましい。
【００１８】
また、開示する発明の別の一態様は、チャネル形成領域を含む酸化物半導体層と、チャネル形成領域と接するソース電極及びドレイン電極と、チャネル形成領域と重なるゲート電極と、酸化物半導体層とゲート電極との間に設けられたゲート絶縁層と、を有し、ソース電極またはドレイン電極において、酸化物半導体層のチャネル形成領域と接する領域は、その他の領域よりも高抵抗である半導体装置である。
【００１９】
また、上記の半導体装置において、ソース電極またはドレイン電極は、その端面において酸化物半導体層と接し、かつ、ソース電極またはドレイン電極と、酸化物半導体層との間に絶縁層を有するのが好ましい。
【００２０】
ここで半導体装置とは、半導体特性を利用することで機能しうる装置全般を指す。例えば、表示装置や記憶装置、集積回路などは半導体装置に含まれうる。
【００２１】
また、本明細書等において「上」や「下」の用語は、構成要素の位置関係が「直上」または「直下」であることを限定するものではない。例えば、「ゲート絶縁層上のゲート電極」の表現であれば、ゲート絶縁層とゲート電極との間に他の構成要素を含むものを除外しない。また、「上」「下」の用語は説明の便宜のために用いる表現に過ぎず、特に言及する場合を除き、その上下を入れ替えたものも含む。
【００２２】
また、本明細書等において「電極」や「配線」の用語は、これらの構成要素を機能的に限定するものではない。例えば、「電極」は「配線」の一部として用いられることがあり、その逆もまた同様である。さらに、「電極」や「配線」の用語は、複数の「電極」や「配線」が一体となって形成されている場合をなどをも含む。
【００２３】
また、「ソース」や「ドレイン」の機能は、異なる極性のトランジスタを採用する場合や、回路動作において電流の方向が変化する場合などには入れ替わることがある。このため、本明細書においては、「ソース」や「ドレイン」の用語は、入れ替えて用いることができるものとする。
【００２４】
また、本明細書等において、「電気的に接続」には、「何らかの電気的作用を有するもの」を介して接続されている場合が含まれる。ここで、「何らかの電気的作用を有するもの」は、接続対象間での電気信号の授受を可能とするものであれば、特に制限を受けない。例えば、「何らかの電気的作用を有するもの」には、電極や配線をはじめ、トランジスタなどのスイッチング素子、抵抗素子、インダクタ、キャパシタ、その他の各種機能を有す

る素子などが含まれる。
【発明の効果】
【００２５】
開示する発明の一態様によって、以下のいずれか、または双方の効果を得ることが可能である。
【００２６】
第一に、ソース電極またはドレイン電極を第１の導電層と第２の導電層の積層構造として、第２の導電層に、第１の導電層の端面よりチャネル長方向に伸長した領域を設けることで、ソース電極またはドレイン電極上に半導体層を形成する際の被覆性が向上する。このため、接続不良などの発生が抑制される。
【００２７】
第二に、ソース電極またはドレイン電極において、チャネル形成領域と接する領域の近傍を高抵抗領域とすることで、ソース電極とドレイン電極の間の電界を緩和することができる。このため、しきい値電圧低下などの短チャネル効果を抑制することができる。
【００２８】
このような効果により、微細化に伴う問題点が解消されることになるため、結果として、トランジスタサイズを十分に小さくすることが可能になる。トランジスタサイズを十分に小さくすることで、半導体装置の占める面積が小さくなり、半導体装置の取り数が増大する。これにより、半導体装置あたりの製造コストは抑制される。また、半導体装置が小型化されるため、同程度の大きさでさらに機能が高められた半導体装置を実現することができる。また、チャネル長の縮小による、動作の高速化、低消費電力化などの効果を得ることもできる。つまり、開示する発明の一態様により酸化物半導体を用いたトランジスタの微細化が達成されることで、これに付随する様々な効果を得ることが可能である。
【００２９】
このように、開示する発明の一態様によって、不良を抑制しつつ、または、良好な特性を維持しつつ、微細化を達成した半導体装置を提供することができる。
【図面の簡単な説明】
【００３０】
【図１】半導体装置の断面図
【図２】半導体装置の作製工程に係る断面図
【図３】半導体装置の作製工程に係る断面図
【図４】半導体装置の断面図
【図５】半導体装置の作製工程に係る断面図
【図６】半導体装置の回路図の例
【図７】半導体装置の回路図の例
【図８】半導体装置の回路図の例
【図９】電子機器の例
【図１０】計算に用いたトランジスタのモデルを示す断面図
【図１１】チャネル長Ｌ（ｎｍ）としきい値電圧のシフト量ΔＶｔｈ（Ｖ）との関係を示す図
【発明を実施するための形態】
【００３１】
本発明の実施の形態の一例について、図面を用いて以下に説明する。但し、本発明は以下の説明に限定されず、本発明の趣旨およびその範囲から逸脱することなくその形態および詳細を様々に変更し得ることは当業者であれば容易に理解される。従って、本発明は以下に示す実施の形態の記載内容に限定して解釈されるものではない。
【００３２】
なお、図面等において示す各構成の、位置、大きさ、範囲などは、理解の簡単のため、実際の位置、大きさ、範囲などを表していない場合がある。このため、開示する発明は、必ずしも、図面等に開示された位置、大きさ、範囲などに限定されない。

【００３３】
なお、本明細書等における「第１」、「第２」、「第３」などの序数は、構成要素の混同を避けるために付すものであり、数的に限定するものではないことを付記する。
【００３４】
（実施の形態１）
本実施の形態では、開示する発明の一態様に係る半導体装置の構成およびその作製工程の例について、図１乃至図３を参照して説明する。
【００３５】
〈半導体装置の構成例〉
図１（Ａ）乃至図１（Ｄ）に、半導体装置の例として、トランジスタの断面構造を示す。図１（Ａ）乃至図１（Ｄ）では、開示する発明の一態様に係るトランジスタとして、トップゲート型のトランジスタを示している。
【００３６】
図１（Ａ）に示すトランジスタ１６０は、基板１００上に、第１の導電層１４２ａ及び第２の導電層１４５ａが順に積層されたソース電極と、第１の導電層１４２ｂ及び第２の導電層１４５ｂが順に積層されたドレイン電極と、ソース電極上に設けられた絶縁層１４３ａと、ドレイン電極上に設けられた絶縁層１４３ｂと、絶縁層１４３ａ及び絶縁層１４３ｂ上に設けられた酸化物半導体層１４４と、酸化物半導体層１４４上に設けられたゲート絶縁層１４６と、ゲート絶縁層１４６上に設けられたゲート電極１４８と、を有している。
【００３７】
図１（Ａ）に示すトランジスタ１６０において、第２の導電層１４５ａは、第１の導電層１４２ａの端面よりチャネル長方向（キャリアの流れる方向）に伸長した領域を有しており、第２の導電層１４５ａと酸化物半導体層１４４の少なくともチャネル形成領域とは接している。また、第２の導電層１４５ｂは、第１の導電層１４２ｂの端面よりチャネル長方向に伸長した領域を有しており、第２の導電層１４５ｂと酸化物半導体層１４４の少なくともチャネル形成領域とは接している。
【００３８】
図１（Ｂ）に示すトランジスタ１７０と、図１（Ａ）に示すトランジスタ１６０との相違の一は、絶縁層１４３ａ、１４３ｂの有無である。図１（Ｂ）に示すトランジスタ１７０は、第２の導電層１４５ａ及び第２の導電層１４５ｂの上面及び端面に接するように、酸化物半導体層１４４が設けられている。
【００３９】
図１（Ｂ）に示すトランジスタ１７０においても、トランジスタ１６０と同様に、第２の導電層１４５ａは、第１の導電層１４２ａの端面よりチャネル長方向に伸長した領域を有しており、第２の導電層１４５ｂは、第１の導電層１４２ｂの端面よりチャネル長方向に伸長した領域を有している。
【００４０】
図１（Ｃ）に示すトランジスタ１８０と、図１（Ａ）に示すトランジスタ１６０との相違の一は、第１の導電層１４２ａ及び第２の導電層１４５ａの積層順、及び第１の導電層１４２ｂ及び第２の導電層１４５ｂの積層順である。図１（Ｃ）に示すトランジスタ１８０は、第２の導電層１４５ａ及び第１の導電層１４２ａが順に積層されたソース電極と、第２の導電層１４５ｂ及び第１の導電層１４２ｂが順に積層されたドレイン電極と、を有している。
【００４１】
また、図１（Ｃ）に示すトランジスタ１８０において、第２の導電層１４５ａは、第１の導電層１４２ａの端面よりチャネル長方向に伸長した領域を有しており、第２の導電層１４５ｂは、第１の導電層１４２ｂの端面よりチャネル長方向に伸長した領域を有している。したがって、絶縁層１４３ａは、第２の導電層１４５ａにおいて第１の導電層１４２ａの端面よりチャネル長方向に伸長した領域と、第１の導電層１４２ａと、に接して設けら

れている。また、絶縁層１４３ｂは、第２の導電層１４５ｂにおいて第１の導電層１４２ｂの端面よりチャネル長方向に伸長した領域と、第１の導電層１４２ｂと、に接して設けられている。

【００４２】
図１（Ｄ）に示すトランジスタ１９０と、図１（Ｃ）に示すトランジスタ１７０との相違の一は、絶縁層１４３ａ、１４３ｂの有無である。図１（Ｄ）に示すトランジスタ１９０では、第１の導電層１４２ａと、第１の導電層１４２ｂと、第２の導電層１４５ａにおいて第１の導電層１４２ａの端面よりチャネル長方向に伸長した領域と、第２の導電層１４５ｂにおいて第１の導電層１４２ｂの端面よりチャネル長方向に伸長した領域と、に接して酸化物半導体層１４４が設けられている。

【００４３】
図１（Ｄ）に示すトランジスタ１９０において、第２の導電層１４５ａは、第１の導電層１４２ａの端面よりチャネル長方向に伸長した領域を有しており、第２の導電層１４５ａと酸化物半導体層１４４の少なくともチャネル形成領域とは接している。また、第２の導電層１４５ｂは、第１の導電層１４２ｂの端面よりチャネル長方向に伸長した領域を有しており、第２の導電層１４５ｂと酸化物半導体層１４４の少なくともチャネル形成領域とは接している。

【００４４】
〈トランジスタの作製工程の例〉
以下、図２及び図３を用いて、図１に示すトランジスタの作製工程の例について説明する。

【００４５】
〈トランジスタ１６０またはトランジスタ１７０の作製工程〉
まず、図２（Ａ）乃至図２（Ｆ）を用いて、図１（Ａ）に示すトランジスタ１６０の作製工程の一例について説明する。なお、図１（Ｂ）に示すトランジスタ１７０は、絶縁層１４３ａ、１４３ｂを有しない以外は、トランジスタ１６０の作製工程を参酌することができるため、詳細な記載を省略する。

【００４６】
絶縁表面を有する基板１００上に第１の導電膜を形成し、該導電膜を選択的にエッチングして、第１の導電層１４２ａ、１４２ｂを形成する（図２（Ａ）参照）。第１の導電膜の膜厚は、例えば、５０ｎｍ乃至５００ｎｍとする。

【００４７】
なお、基板１００に使用することができる基板に大きな制限はないが、少なくとも、後の加熱処理に耐えうる程度の耐熱性を有していることが必要となる。例えば、ガラス基板、セラミック基板、石英基板、サファイア基板など基板を用いることができる。また、絶縁表面を有していれば、シリコンや炭化シリコンなどの単結晶半導体基板、多結晶半導体基板、シリコンゲルマニウムなどの化合物半導体基板、ＳＯＩ基板などを適用することも可能であり、これらの基板上に半導体素子が設けられていてもよい。また、基板１００上に下地膜が設けられていても良い。

【００４８】
第１の導電膜は、スパッタ法をはじめとするＰＶＤ法や、プラズマＣＶＤ法などのＣＶＤ法を用いて形成することができる。また、第１の導電膜の材料としては、アルミニウム、クロム、銅、タンタル、チタン、モリブデン、タングステンからから選ばれた元素やこれらの窒化物、上述した元素を成分とする合金等を用いることができる。マンガン、マグネシウム、ジルコニウム、ベリリウムのいずれか、またはこれらを複数組み合わせた材料を用いてもよい。また、アルミニウムに、チタン、タンタル、タングステン、モリブデン、クロム、ネオジム、スカンジウムから選ばれた元素、またはこれらを複数組み合わせた材料を用いてもよい。

【００４９】
第１の導電膜は、単層構造であっても良いし、２層以上の積層構造としてもよい。例えば

、チタン膜の単層構造、シリコンを含むアルミニウム膜の単層構造、アルミニウム膜上にチタン膜が積層された２層構造、チタン膜とアルミニウム膜とチタン膜とが積層された３層構造などが挙げられる。なお、第１の導電膜を単層構造とする場合には、テーパー形状を有するソース電極またはドレイン電極への加工が容易であるというメリットがある。

【００５０】

また、第１の導電膜は、導電性の金属酸化物を用いて形成しても良い。導電性の金属酸化物としては酸化インジウム（In_2O_3）、酸化スズ（SnO_2）、酸化亜鉛（ＺｎＯ）、酸化インジウム酸化スズ合金（$In_2O_3-SnO_2$、ＩＴＯと略記する場合がある）、酸化インジウム酸化亜鉛合金（In_2O_3-ZnO）、または、これらの金属酸化物材料にシリコン若しくは酸化シリコンを含有させたものを用いることができる。

【００５１】

第１の導電膜のエッチングは、形成される第１の導電層１４２ａ、１４２ｂの端部が、テーパー形状となるように行うことが好ましい。ここで、テーパー角は、例えば、３０°以上６０°以下であることが好ましい。

【００５２】

次に、第１の導電層１４２ａ、１４２ｂ、及び基板１００を覆うように、第２の導電膜１４５を形成する。第２の導電膜１４５の膜厚は、３ｎｍ乃至３０ｎｍ、好ましくは５ｎｍ乃至１５ｎｍとする。

【００５３】

第２の導電膜１４５は、第１の導電膜と同様の材料、同様の成膜方法で形成することができる。つまり、第２の導電膜の材料としては、アルミニウム、クロム、銅、タンタル、チタン、モリブデン、タングステンからから選ばれた元素やこれらの窒化物、上述した元素を成分とする合金等を用いることができる。マンガン、マグネシウム、ジルコニウム、ベリリウムのいずれか、またはこれらを複数組み合わせた材料を用いてもよい。また、アルミニウムに、チタン、タンタル、タングステン、モリブデン、クロム、ネオジム、スカンジウムから選ばれた元素、またはこれらを複数組み合わせた材料を用いてもよい。また、酸化インジウム（In_2O_3）、酸化スズ（SnO_2）、酸化亜鉛（ＺｎＯ）、酸化インジウム酸化スズ合金（$In_2O_3-SnO_2$、ＩＴＯと略記する場合がある）、酸化インジウム酸化亜鉛合金（In_2O_3-ZnO）、または、これらの金属酸化物材料にシリコン若しくは酸化シリコンを含有させた導電性の金属酸化物を用いても良い。

【００５４】

なお、第２の導電膜１４５の材料として、第１の導電層１４２ａ、１４２ｂよりも高抵抗な材料を用いると、作製されるトランジスタ１６０のソース電極及びドレイン電極において、酸化物半導体層のチャネル形成領域と接する領域が、その他の領域よりも高抵抗となるため、ソース電極とドレイン電極の間の電界を緩和して短チャネル効果を抑制することができ、好ましい。第２の導電膜１４５に用いる導電材料としては、例えば、窒化チタン、窒化タングステン、窒化タンタル、または窒化モリブデン等の金属窒化物を好ましく用いることができる。また、第２の導電膜１４５はソース電極またはドレイン電極の一部となり酸化物半導体層と接するから、第２の導電膜１４５には、酸化物半導体層との接触により化学反応しない材料を用いるのが望ましい。上述の金属窒化物は、この点においても好適である。

【００５５】

次いで、第２の導電膜１４５上に、絶縁膜１４３を膜厚５０ｎｍ乃至３００ｎｍ、好ましくは、１００ｎｍ乃至２００ｎｍで形成する（図２（Ａ）参照）。本実施の形態においては、絶縁膜１４３として、酸化シリコン膜を形成するものとする。なお、図１（Ｂ）においてトランジスタ１７０で示したように、絶縁膜１４３は必ずしも形成しなくてもよいが、絶縁膜１４３を設ける場合には、後に形成されるソース電極またはドレイン電極と、酸化物半導体層との接触領域（接触面積など）の制御が容易になる。つまり、ソース電極またはドレイン電極の抵抗の制御が容易になり、短チャネル効果の抑制を効果的に行うことができる。また、絶縁膜１４３を設けることにより、後に形成されるゲート電極と、ソー

ス電極及びドレイン電極と、の間の寄生容量を低減することが可能である。
【００５６】
次いで、絶縁膜１４３上にマスクを形成し、該マスクを用いて絶縁膜１４３をエッチングすることにより、絶縁層１４３ａ、１４３ｂを形成する（図２（Ｂ）参照）。絶縁膜１４３のエッチングには、ウェットエッチングまたはドライエッチングを用いることができ、ウェットエッチングとドライエッチングを組み合わせて用いてもよい。絶縁膜を所望の形状にエッチングできるよう、材料に合わせてエッチング条件（エッチングガスやエッチング液、エッチング時間、温度等）を適宜設定するものとする。ただし、トランジスタのチャネル長（Ｌ）を微細に加工するためには、ドライエッチングを用いるのが好ましい。ドライエッチングに用いるエッチングガスとしては、例えば、フッ化硫黄（SF_6）、フッ化窒素（NF_3）、トリフルオロメタン（CHF_3）などのフッ素を含むガス、又は、四フッ化メタン（CF_4）と水素の混合ガス等を用いることができ、希ガス（ヘリウム（Ｈｅ）、アルゴン（Ａｒ）、キセノン（Ｘｅ））、一酸化炭素、又は二酸化炭素等を添加しても良い。
【００５７】
次いで、絶縁膜１４３のエッチングに用いたマスクを用いて、第２の導電膜１４５をエッチングすることにより、第２の導電層１４５ａ、１４５ｂを形成する（図２（Ｃ）参照）。なお、第２の導電膜１４５をエッチングする前にマスクを除去し、絶縁層１４３ａ及び絶縁層１４３ｂをマスクとして用いて第２の導電膜１４５をエッチングしても良い。また、図１（Ｂ）のトランジスタ１７０で示したように、絶縁層を設けない場合は、第２の導電膜１４５上に直接マスクを形成して第２の導電膜をエッチングすればよい。
【００５８】
第２の導電膜１４５のエッチングには、ウェットエッチングまたはドライエッチングを用いることができ、ウェットエッチングとドライエッチングを組み合わせて用いてもよい。所望の形状にエッチングできるよう、材料に合わせてエッチング条件（エッチングガスやエッチング液、エッチング時間、温度等）を適宜設定するものとする。ただし、トランジスタのチャネル長（Ｌ）を微細に加工するためには、ドライエッチングを用いるのが好ましい。第２の導電膜１４５のエッチングに用いるエッチングガスとしては、例えば、塩素（Cl_2）、三塩化ホウ素（BCl_3）、四塩化ケイ素（$SiCl_4$）、四フッ化メタン（CF_4）フッ化硫黄（SF_6）、フッ化窒素（NF_3）等を用いることができ、これらのうちから複数を選択した混合ガスを用いてもよい。また、希ガス（ヘリウム（Ｈｅ）、アルゴン（Ａｒ））、又は酸素等を添加しても良い。また、第２の導電膜のエッチングは絶縁層１４３のエッチングと同じガスを用いて連続的に行うことも可能である。
【００５９】
このエッチング工程によって、第１の導電層１４２ａ及び第２の導電層１４５ａが積層したソース電極と、第１の導電層１４２ｂ及び第２の導電層１４５ｂが積層したドレイン電極とが形成される。エッチングに用いるマスクを適宜調整することで、第１の導電層１４２ａの端面よりチャネル長方向に伸長した領域を有する第２の導電層１４５ａ、または、第１の導電層１４２ｂの端面よりチャネル長方向に伸長した領域を有する第２の導電層１４５ｂとすることができる。
【００６０】
なお、トランジスタ１６０のチャネル長（Ｌ）は、第２の導電層１４５ａの下端部と第２の導電層１４５ｂの下端部との間隔によって決定される。チャネル長（Ｌ）は、トランジスタ１６０の用途によって異なるが、例えば１０ｎｍ乃至１０００ｎｍ、好ましくは２０ｎｍ乃至４００ｎｍとすることができる。
【００６１】
なお、チャネル長（Ｌ）が２５ｎｍ未満のトランジスタを形成する場合、絶縁膜１４３及び第２の導電膜１４５のエッチングに用いるマスク形成の露光を行う際には、数ｎｍ～数１０ｎｍと波長の短い超紫外線（Ｅｘｔｒｅｍｅ　Ｕｌｔｒａｖｉｏｌｅｔ）を用いるのが望ましい。超紫外線による露光は、解像度が高く焦点深度も大きい。従って、後に形成

されるトランジスタのチャネル長（Ｌ）を、十分に小さくすることも可能であり、回路の動作速度を高めることが可能である。また、微細化によって、半導体装置の消費電力を低減することも可能である。

【００６２】
また、第２の導電層において、第１の導電層の端面よりチャネル長方向に伸長した領域は、後の酸化物半導体層及びゲート絶縁層形成工程において、被覆性を向上させる効果を奏する。第２の導電層１４５ａにおいて、第１の導電層１４２ａの端面よりチャネル長方向に伸長した領域のチャネル長方向の長さ（$Ｌ_{Ｓ}$）と、第２の導電層１４５ｂにおいて、第１の導電層１４２ｂの端面よりチャネル長方向に伸長した領域のチャネル長方向の長さ（$Ｌ_{Ｄ}$）と、は、必ずしも同一ではないが、トランジスタ１６０を同一基板上に複数設ける場合、各トランジスタにおける$Ｌ_{Ｓ}$と$Ｌ_{Ｄ}$との合計の値は略一定となる。

【００６３】
次に、絶縁層１４３ａ、１４３ｂ、及び基板１００上に、酸化物半導体層１４４をスパッタ法によって形成する（図２（Ｄ）参照）。酸化物半導体層１４４の膜厚は、例えば、３ｎｍ乃至３０ｎｍ、好ましくは５ｎｍ乃至１５ｎｍとする。形成された酸化物半導体層１４４は、第２の導電層１４５ａ及び第２の導電層１４５ｂと少なくともチャネル形成領域において接している。

【００６４】
ここで、第２の導電層１４５ａ、１４５ｂが、第１の導電層１４２ａ、１４２ｂの端面よりもチャネル長方向に伸長した領域を有することで、ソース電極及びドレイン電極の端部における段差を緩やかなものとすることができるため、酸化物半導体層１４４の被覆性を向上させ、段切れを防止することが可能である。

【００６５】
なお、作製されるトランジスタ１６０のソース電極またはドレイン電極は、第２の導電層１４５ａ及び第２の導電層１４５ｂの端面においてのみ、酸化物半導体層１４４と接しており、ソース電極またはドレイン電極の上面においても酸化物半導体層と接する場合と比較して、その接触面積を大幅に低減することができる。このように、ソース電極またはドレイン電極と、酸化物半導体層１４４との接触面積を低減することで、接触界面におけるコンタクト抵抗を増大させることができ、ソース電極とドレイン電極の間の電界を緩和することができる。なお、開示する発明の技術思想は、ソース電極またはドレイン電極に高抵抗な領域を形成することにあるので、ソース電極またはドレイン電極は、厳密に第２の導電層１４５ａ及び第２の導電層１４５ｂの端面においてのみ酸化物半導体層１４４と接する必要はない。例えば、第２の導電層１４５ａ及び第２の導電層１４５ｂは、上面の一部において、酸化物半導体層１４４と接していても良い。

【００６６】
酸化物半導体層１４４は、四元系金属酸化物であるＩｎ－Ｓｎ－Ｇａ－Ｚｎ－Ｏ系や、三元系金属酸化物であるＩｎ－Ｇａ－Ｚｎ－Ｏ系、Ｉｎ－Ｓｎ－Ｚｎ－Ｏ系、Ｉｎ－Ａｌ－Ｚｎ－Ｏ系、Ｓｎ－Ｇａ－Ｚｎ－Ｏ系、Ａｌ－Ｇａ－Ｚｎ－Ｏ系、Ｓｎ－Ａｌ－Ｚｎ－Ｏ系や、二元系金属酸化物であるＩｎ－Ｚｎ－Ｏ系、Ｓｎ－Ｚｎ－Ｏ系、Ａｌ－Ｚｎ－Ｏ系、Ｚｎ－Ｍｇ－Ｏ系、Ｓｎ－Ｍｇ－Ｏ系、Ｉｎ－Ｍｇ－Ｏ系や、Ｉｎ－Ｏ系、Ｓｎ－Ｏ系、Ｚｎ－Ｏ系などを用いて形成することができる。

【００６７】
中でも、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系の酸化物半導体材料は、無電界時の抵抗が十分に高くオフ電流を十分に小さくすることが可能であり、また、電界効果移動度も高いため、半導体装置に用いる半導体材料としては好適である。

【００６８】
Ｉｎ－Ｇａ－Ｚｎ－Ｏ系の酸化物半導体材料の代表例としては、$ＩｎＧａＯ_3（ＺｎＯ）_{ｍ}$（ｍ＞０）で表記されるものがある。また、Ｇａに代えてＭを用い、$ＩｎＭＯ_3（ＺｎＯ）_{ｍ}$（ｍ＞０）のように表記される酸化物半導体材料がある。ここで、Ｍは、ガリウム（Ｇａ）、アルミニウム（Ａｌ）、鉄（Ｆｅ）、ニッケル（Ｎｉ）、マンガン（Ｍｎ）、

コバルト（Ｃｏ）などから選ばれた一の金属元素または複数の金属元素を示す。例えば、Ｍとしては、Ｇａ、ＧａおよびＡｌ、ＧａおよびＦｅ、ＧａおよびＮｉ、ＧａおよびＭｎ、ＧａおよびＣｏなどを適用することができる。なお、上述の組成は結晶構造から導き出されるものであり、あくまでも一例に過ぎないことを付記する。

【００６９】

酸化物半導体層１４４をスパッタ法で作製するためのターゲットとしては、Ｉｎ：Ｇａ：Ｚｎ＝１：ｘ：ｙ（ｘは０以上、ｙは０．５以上５以下）の組成式で表されるものを用いるのが好適である。例えば、Ｉｎ：Ｇａ：Ｚｎ＝１：１：１［ａｔｏｍ比］（ｘ＝１、ｙ＝１）、（すなわち、In_2O_3：Ga_2O_3：ＺｎＯ＝１：１：２［ｍｏｌ数比］）の組成比を有する金属酸化物ターゲットなどを用いることができる。また、Ｉｎ：Ｇａ：Ｚｎ＝１：１：０．５［ａｔｏｍ比］（ｘ＝１、ｙ＝０．５）の組成比を有する金属酸化物ターゲットや、Ｉｎ：Ｇａ：Ｚｎ＝１：１：２［ａｔｏｍ比］（ｘ＝１、ｙ＝２）の組成比を有する金属酸化物ターゲットや、Ｉｎ：Ｇａ：Ｚｎ＝１：０：１［ａｔｏｍ比］（ｘ＝０、ｙ＝１）の組成比を有する金属酸化物ターゲットを用いることもできる。

【００７０】

本実施の形態では、非晶質構造の酸化物半導体層１４４を、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系の金属酸化物ターゲットを用いるスパッタ法により形成することとする。

【００７１】

金属酸化物ターゲット中の金属酸化物の相対密度は８０％以上、好ましくは９５％以上、さらに好ましくは９９．９％以上である。相対密度の高い金属酸化物ターゲットを用いることにより、緻密な構造の酸化物半導体層１４４を形成することが可能である。

【００７２】

酸化物半導体層１４４の形成雰囲気は、希ガス（代表的にはアルゴン）雰囲気、酸素雰囲気、または、希ガス（代表的にはアルゴン）と酸素との混合雰囲気とするのが好適である。具体的には、例えば、水素、水、水酸基、水素化物などの不純物が、濃度１ｐｐｍ以下（望ましくは濃度１０ｐｐｂ以下）にまで除去された高純度ガス雰囲気を用いるのが好適である。

【００７３】

酸化物半導体層１４４の形成の際には、例えば、減圧状態に保持された処理室内に被処理物（ここでは、基板１００を含む構造体）を保持し、被処理物の温度が１００℃以上５５０℃未満、好ましくは２００℃以上４００℃以下となるように被処理物を熱する。または、酸化物半導体層１４４の形成の際の被処理物の温度は、室温としてもよい。そして、処理室内の水分を除去しつつ、水素や水などが除去されたスパッタガスを導入し、上記ターゲットを用いて酸化物半導体層１４４を形成する。被処理物を熱しながら酸化物半導体層１４４を形成することにより、酸化物半導体層１４４に含まれる不純物を低減することができる。また、スパッタによる損傷を軽減することができる。処理室内の水分を除去するためには、吸着型の真空ポンプを用いることが好ましい。例えば、クライオポンプ、イオンポンプ、チタンサブリメーションポンプなどを用いることができる。また、ターボポンプにコールドトラップを加えたものを用いてもよい。クライオポンプなどを用いて排気することで、処理室から水素や水などを除去することができるため、酸化物半導体層１４４中の不純物濃度を低減できる。

【００７４】

酸化物半導体層１４４の形成条件としては、例えば、被処理物とターゲットの間との距離が１７０ｍｍ、圧力が０．４Ｐａ、直流（ＤＣ）電力が０．５ｋＷ、雰囲気が酸素（酸素１００％）雰囲気、またはアルゴン（アルゴン１００％）雰囲気、または酸素とアルゴンの混合雰囲気、といった条件を適用することができる。なお、パルス直流（ＤＣ）電源を用いると、ごみ（成膜時に形成される粉状の物質など）を低減でき、膜厚分布も均一となるため好ましい。酸化物半導体層１４４の膜厚は、例えば、３ｎｍ乃至３０ｎｍ、好ましくは５ｎｍ乃至１５ｎｍとする。このような厚さの酸化物半導体層１４４を用いることで、微細化に伴う短チャネル効果を抑制することが可能である。ただし、適用する酸化物半

導体材料や、半導体装置の用途などにより適切な厚さは異なるから、その厚さは、用いる材料や用途などに応じて選択することもできる。
【００７５】
なお、酸化物半導体層１４４をスパッタ法により形成する前には、アルゴンガスを導入してプラズマを発生させる逆スパッタを行い、形成表面（例えば絶縁層１４３ａ、１４３ｂの表面）の付着物を除去するのが好適である。ここで、逆スパッタとは、通常のスパッタにおいては、スパッタターゲットにイオンを衝突させるところを、逆に、処理表面にイオンを衝突させることによってその表面を改質する方法のことをいう。処理表面にイオンを衝突させる方法としては、アルゴン雰囲気下で処理表面側に高周波電圧を印加して、被処理物付近にプラズマを生成する方法などがある。なお、アルゴン雰囲気に代えて窒素、ヘリウム、酸素などによる雰囲気を適用してもよい。
【００７６】
その後、酸化物半導体層１４４に対して、熱処理（第１の熱処理）を行うことが望ましい。この第１の熱処理によって酸化物半導体層１４４中の、過剰な水素（水や水酸基を含む）を除去し、酸化物半導体層の構造を整え、エネルギーギャップ中の欠陥準位を低減することができる。第１の熱処理の温度は、例えば、３００℃以上５５０℃未満、または４００℃以上５００℃以下とする。
【００７７】
熱処理は、例えば、抵抗発熱体などを用いた電気炉に被処理物を導入し、窒素雰囲気下、４５０℃、１時間の条件で行うことができる。この間、酸化物半導体層１４４は大気に触れさせず、水や水素の混入が生じないようにする。
【００７８】
熱処理装置は電気炉に限られず、加熱されたガスなどの媒体からの熱伝導、または熱輻射によって、被処理物を加熱する装置を用いても良い。例えば、ＧＲＴＡ（Ｇａｓ　Ｒａｐｉｄ　Ｔｈｅｒｍａｌ　Ａｎｎｅａｌ）装置、ＬＲＴＡ（Ｌａｍｐ　Ｒａｐｉｄ　Ｔｈｅｒｍａｌ　Ａｎｎｅａｌ）装置等のＲＴＡ（Ｒａｐｉｄ　Ｔｈｅｒｍａｌ　Ａｎｎｅａｌ）装置を用いることができる。ＬＲＴＡ装置は、ハロゲンランプ、メタルハライドランプ、キセノンアークランプ、カーボンアークランプ、高圧ナトリウムランプ、高圧水銀ランプなどのランプから発する光（電磁波）の輻射により、被処理物を加熱する装置である。ＧＲＴＡ装置は、高温のガスを用いて熱処理を行う装置である。ガスとしては、アルゴンなどの希ガス、または窒素のような、熱処理によって被処理物と反応しない不活性気体が用いられる。
【００７９】
例えば、第１の熱処理として、熱せられた不活性ガス雰囲気中に被処理物を投入し、数分間熱した後、当該不活性ガス雰囲気から被処理物を取り出すＧＲＴＡ処理を行ってもよい。ＧＲＴＡ処理を用いると短時間での高温熱処理が可能となる。また、被処理物の耐熱温度を超える温度条件であっても適用が可能となる。なお、処理中に、不活性ガスを、酸素を含むガスに切り替えても良い。酸素を含む雰囲気において第１の熱処理を行うことで、酸素欠損に起因するエネルギーギャップ中の欠陥準位を低減することができるためである。
【００８０】
なお、不活性ガス雰囲気としては、窒素、または希ガス（ヘリウム、ネオン、アルゴン等）を主成分とする雰囲気であって、水、水素などが含まれない雰囲気を適用するのが望ましい。例えば、熱処理装置に導入する窒素や、ヘリウム、ネオン、アルゴン等の希ガスの純度を、６Ｎ（９９．９９９９％）以上、好ましくは７Ｎ（９９．９９９９９％）以上（すなわち、不純物濃度が１ｐｐｍ以下、好ましくは０．１ｐｐｍ以下）とする。
【００８１】
いずれにしても、第１の熱処理によって不純物を低減し、ｉ型（真性半導体）またはｉ型に限りなく近い酸化物半導体層１４４を形成することで、極めて優れた特性のトランジスタを実現することができる。

【００８２】
ところで、上述の熱処理（第１の熱処理）には水素や水などを除去する効果があるから、当該熱処理を、脱水化処理や、脱水素化処理などと呼ぶこともできる。当該脱水化処理や、脱水素化処理は、酸化物半導体層の形成後やゲート絶縁層の形成後、ゲート電極の形成後、などのタイミングにおいて行うことも可能である。また、このような脱水化処理、脱水素化処理は、一回に限らず複数回行っても良い。
【００８３】
次に、酸化物半導体層１４４に接するゲート絶縁層１４６を形成する（図２（Ｅ）参照）。ここで、第２の導電層１４５ａ、１４５ｂが、第１の導電層１４２ａ、１４２ｂの端面よりもチャネル長方向に伸長した領域を有することで、ソース電極及びドレイン電極の端部における段差を緩やかなものとすることができるため、ゲート絶縁層１４６の被覆性を向上させ、段切れを防止することが可能である。
【００８４】
ゲート絶縁層１４６は、ＣＶＤ法やスパッタ法等を用いて形成することができる。また、ゲート絶縁層１４６は、酸化シリコン、窒化シリコン、酸窒化シリコン、酸化アルミニウム、酸化タンタル、酸化ハフニウム、酸化イットリウム、ハフニウムシリケート（ＨｆＳｉｘＯｙ（ｘ＞０、ｙ＞０））、窒素が添加されたハフニウムシリケート（ＨｆＳｉｘＯｙ（ｘ＞０、ｙ＞０））、窒素が添加されたハフニウムアルミネート（ＨｆＡｌｘＯｙ（ｘ＞０、ｙ＞０））、などを含むように形成するのが好適である。ゲート絶縁層１４６は、単層構造としても良いし、積層構造としても良い。また、その厚さは特に限定されないが、半導体装置を微細化する場合には、トランジスタの動作を確保するために薄くするのが望ましい。例えば、酸化シリコンを用いる場合には、１ｎｍ以上１００ｎｍ以下、好ましくは１０ｎｍ以上５０ｎｍ以下とすることができる。
【００８５】
上述のように、ゲート絶縁層を薄くすると、トンネル効果などに起因するゲートリークが問題となる。ゲートリークの問題を解消するには、ゲート絶縁層１４６に、酸化ハフニウム、酸化タンタル、酸化イットリウム、ハフニウムシリケート（ＨｆＳｉｘＯｙ（ｘ＞０、ｙ＞０））、窒素が添加されたハフニウムシリケート（ＨｆＳｉｘＯｙ（ｘ＞０、ｙ＞０））、窒素が添加されたハフニウムアルミネート（ＨｆＡｌｘＯｙ（ｘ＞０、ｙ＞０））、などの高誘電率（ｈｉｇｈ－ｋ）材料を用いると良い。ｈｉｇｈ－ｋ材料をゲート絶縁層１４６に用いることで、電気的特性を確保しつつ、ゲートリークを抑制するために膜厚を大きくすることが可能になる。なお、ｈｉｇｈ－ｋ材料を含む膜と、酸化シリコン、窒化シリコン、酸化窒化シリコン、窒化酸化シリコン、酸化アルミニウムなどのいずれかを含む膜との積層構造としてもよい。
【００８６】
ゲート絶縁層１４６の形成後には、不活性ガス雰囲気下、または酸素雰囲気下で第２の熱処理を行うのが望ましい。熱処理の温度は、２００℃以上４５０℃以下、望ましくは２５０℃以上３５０℃以下である。例えば、窒素雰囲気下で２５０℃、１時間の熱処理を行えばよい。第２の熱処理を行うことによって、トランジスタの電気的特性のばらつきを軽減することができる。また、ゲート絶縁層１４６が酸素を含む場合、酸化物半導体層１４４に酸素を供給し、該酸化物半導体層１４４の酸素欠損を補填して、ｉ型（真性半導体）またはｉ型に限りなく近い酸化物半導体層を形成することもできる。
【００８７】
なお、本実施の形態では、ゲート絶縁層１４６の形成後に第２の熱処理を行っているが、第２の熱処理のタイミングはこれに特に限定されない。例えば、ゲート電極の形成後に第２の熱処理を行っても良い。また、第１の熱処理に続けて第２の熱処理を行っても良いし、第１の熱処理に第２の熱処理を兼ねさせても良いし、第２の熱処理に第１の熱処理を兼ねさせても良い。
【００８８】
上述のように、第１の熱処理と第２の熱処理の少なくとも一方を適用することで、酸化物

半導体層１４４を、その主成分以外の不純物が極力含まれないように高純度化することができる。これにより、酸化物半導体層１４４中の水素濃度を、５×１０^{19}ａｔｏｍｓ／ｃｍ^{3}以下、望ましくは５×１０^{18}ａｔｏｍｓ／ｃｍ^{3}以下、より望ましくは５×１０^{17}ａｔｏｍｓ／ｃｍ^{3}以下とすることができる。また、酸化物半導体層１４４のキャリア密度を、一般的なシリコンウェハにおけるキャリア密度（１×１０^{14}／ｃｍ^{3}程度）と比較して、十分に小さい値（例えば、１×１０^{12}／ｃｍ^{3}未満、より好ましくは、１．４５×１０^{10}／ｃｍ^{3}未満）とすることができる。そして、これにより、オフ電流が十分に小さくなる。例えば、トランジスタ１６０の室温でのオフ電流（ここでは、単位チャネル幅（１μｍ）あたりの値）は、１００ｚＡ／μｍ（１ｚＡ（ゼプトアンペア）は１×１０$^{-21}$Ａ）以下、望ましくは、１０ｚＡ／μｍ以下となる。

【００８９】

次に、ゲート絶縁層１４６上において酸化物半導体層１４４のチャネル形成領域と重畳する領域にゲート電極１４８を形成する（図２（Ｆ）参照）。ゲート電極１４８は、ゲート絶縁層１４６上に導電膜を形成した後に、当該導電膜を選択的にエッチングすることによって形成することができる。ゲート電極１４８となる導電膜は、スパッタ法をはじめとするＰＶＤ法や、プラズマＣＶＤ法などのＣＶＤ法を用いて形成することができる。詳細は、ソース電極またはドレイン電極などの場合と同様であり、これらの記載を参酌できる。ただし、ゲート電極１４８の材料の仕事関数が酸化物半導体層１４４の電子親和力と同程度またはそれより小さいと、トランジスタを微細化した場合に、そのしきい値電圧がマイナスにシフトすることがある。よって、ゲート電極１４８には、酸化物半導体層１４４の電子親和力より大きい仕事関数を有する材料を用いるのが好ましい。このような材料としては、例えば、タングステン、白金、金、ｐ型の導電性を付与したシリコンなどがある。

【００９０】

以上により、酸化物半導体層１４４を用いたトランジスタ１６０が完成する。

【００９１】

〈トランジスタ１８０またはトランジスタ１９０の作製工程〉

次いで、図３（Ａ）乃至（Ｆ）を用いて、図１（Ｃ）に示すトランジスタ１８０の作製工程の一例について説明する。なお、図１（Ｄ）に示すトランジスタ１９０は、絶縁層１４３ａ、１４３ｂを有しない以外は、トランジスタ１８０の作製工程を参酌することができるため、詳細な記載を省略する。

【００９２】

基板１００上に、第２の導電膜１４５を成膜する。第２の導電膜１４５の膜厚は、３ｎｍ乃至３０ｎｍ、好ましくは５ｎｍ乃至１５ｎｍとする。次いで、第２の導電膜１４５上に第１の導電膜を形成し、該第１の導電膜を選択的にエッチングして、第１の導電層１４２ａ、１４２ｂを形成する。その後、第１の導電層１４２ａ、１４２ｂ、及び第２の導電膜１４５上に、絶縁膜１４３を形成する（図３（Ａ）参照）。

【００９３】

なお、第２の導電膜上に第１の導電膜を成膜する場合には、第２の導電膜と第１の導電膜は、エッチングの選択比がとれる材料をそれぞれ選択するものとする。また、第２の導電膜は、第１の導電膜よりも高抵抗な材料を用いることが好ましい。本実施の形態においては、第２の導電膜１４５として窒化チタン膜を形成し、第１の導電膜としてタングステン膜またはモリブデン膜を形成し、四フッ化メタン（CF_4）と塩素（Cl_2）と酸素（O_2）との混合ガス、四フッ化メタン（CF_4）と酸素（O_2）の混合ガス、フッ化硫黄（SF_6）と塩素（Cl_2）と酸素（O_2）との混合ガス、または、フッ化硫黄（SF_6）と酸素（O_2）との混合ガスを用いて第１の導電膜をエッチングすることで、第１の導電層１４２ａ、１４２ｂを形成するものとする。

【００９４】

また、図１（Ｄ）においてトランジスタ１９０で示したように、絶縁膜１４３は必ずしも形成しなくてもよいが、絶縁膜１４３を設けることにより、後に形成されるゲート電極と、ソース電極及びドレイン電極と、の間の寄生容量を低減することが可能である。

【００９５】
次いで、図２（Ｂ）で示した工程と同様に、絶縁膜１４３上にマスクを形成し、該マスクを用いて絶縁膜１４３をエッチングすることにより、絶縁層１４３ａ、１４３ｂを形成する（図３（Ｂ）参照）。
【００９６】
次いで、図２（Ｃ）で示した工程と同様に、絶縁層１４３ａ及び絶縁層１４３ｂのエッチングに用いたマスクを用いて第２の導電膜１４５をエッチングすることにより、第２の導電層１４５ａ、１４５ｂを形成する（図３（Ｃ）参照）。なお、第２の導電膜１４５をエッチングする前にマスクを除去し、絶縁層１４３ａ及び絶縁層１４３ｂをマスクとして用いて第２の導電膜１４５をエッチングしても良い。第２の導電膜１４５のエッチングに用いるエッチングガスとしては、例えば、塩素（Cl_2）、三塩化ホウ素（BCl_3）、四塩化ケイ素（$SiCl_4$）、四フッ化メタン（CF_4）フッ化硫黄（SF_6）、フッ化窒素（NF_3）等を用いることができ、これらのうちから複数を選択した混合ガスを用いてもよい。また、希ガス（ヘリウム（Ｈｅ）、アルゴン（Ａｒ））を添加しても良い。また、図１（Ｄ）のトランジスタ１９０で示したように、絶縁層を設けない場合は、第２の導電膜１４５上に直接マスクを形成して第２の導電膜をエッチングすればよい。
【００９７】
次いで、図２（Ｄ）で示した工程と同様に、絶縁層１４３ａ、１４３ｂ、及び基板１００上に、酸化物半導体層１４４をスパッタ法によって形成する（図３（Ｄ）参照）。形成された酸化物半導体層１４４は、第２の導電層１４５ａ及び第２の導電層１４５ｂと少なくともチャネル形成領域において接している。また、酸化物半導体層１４４に対しては、熱処理（第１の熱処理）を行うことが望ましい。
【００９８】
次いで、図２（Ｅ）で示した工程と同様に、酸化物半導体層１４４に接するゲート絶縁層１４６を形成する（図３（Ｅ）参照）。ゲート絶縁層１４６の形成後には、熱処理（第２の熱処理）を行うのが望ましい。
【００９９】
次いで、図２（Ｆ）で示した工程と同様に、ゲート絶縁層１４６上において酸化物半導体層１４４のチャネル形成領域と重畳する領域にゲート電極１４８を形成する（図３（Ｆ）参照）。
【０１００】
以上により、酸化物半導体層１４４を用いたトランジスタ１８０が完成する。
【０１０１】
本実施の形態において示すトランジスタ１６０、１７０、１８０、１９０では、第１の導電層及び第２の導電層が積層されたソース電極及びドレイン電極を含み、第２の導電層１４５ａ、１４５ｂは、第１の導電層１４２ａ、１４２ｂの端面よりもチャネル長方向に伸長した領域を有する。これによって、ソース電極及びドレイン電極の端部における段差を緩やかなものとすることができるため、酸化物半導体層１４４及びゲート絶縁層１４６の被覆性を向上し、接続不良の発生を抑制することができる。
【０１０２】
また、本実施の形態において示すトランジスタ１６０、１７０、１８０、１９０では、ソース電極またはドレイン電極において、チャネル形成領域と接する領域の近傍を高抵抗領域とすることで、ソース電極とドレイン電極の間の電界を緩和することができ、トランジスタサイズの縮小に伴う短チャネル効果を抑制することができる。
【０１０３】
このように、開示する発明の一態様では、微細化に伴う問題点を解消することができるため、結果として、トランジスタサイズを十分に小さくすることが可能になる。トランジスタサイズを十分に小さくすることで、半導体装置の占める面積が小さくなるため、半導体装置の取り数が増大する。これにより、半導体装置あたりの製造コストは抑制される。また、半導体装置が小型化されるため、同程度の大きさでさらに機能が高められた半導体装

置を実現することができる。また、チャネル長の縮小による、動作の高速化、低消費電力化などの効果を得ることもできる。つまり、開示する発明の一態様により酸化物半導体を用いたトランジスタの微細化が達成されることで、これに付随する様々な効果を得ることが可能である。

【０１０４】

以上、本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。

【０１０５】

（実施の形態２）

本実施の形態では、実施の形態１とは異なる、開示する発明の一態様に係る半導体装置の構成およびその作製工程について、図４乃び図５を参照して説明する。

【０１０６】

<半導体装置の構成例>

図４に示すトランジスタ２８０は、半導体装置の構成の例である。トランジスタ２８０は、図１（Ｃ）に示すトランジスタ１８０に対応しており、第２の導電層２４５ａの第１の導電層２４２ａの端面からチャネル長方向に伸長した領域の上にサイドウォール絶縁層２５２ａが設けられ、第２の導電層２４５ｂの、第１の導電層２４２ｂの端面からチャネル長方向に伸長した領域の上にサイドウォール絶縁層２５２ｂが設けられている点において異なっている。

【０１０７】

図４に示すトランジスタ２８０は、基板２００上に、第２の導電層２４５ａ及び第１の導電層２４２ａが順に積層されたソース電極と、第２の導電層２４５ｂ及び第１の導電層２４２ｂが順に積層されたドレイン電極と、ソース電極上に設けられた絶縁層２４３ａと、ドレイン電極上に設けられた絶縁層２４３ｂと、絶縁層２４３ａ及び絶縁層２４３ｂ上に設けられた酸化物半導体層２４４と、酸化物半導体層２４４上に設けられたゲート絶縁層２４６と、ゲート絶縁層２４６上に設けられたゲート電極２４８と、を有している。

【０１０８】

図４に示すトランジスタ２８０において、第２の導電層２４５ａは、第１の導電層２４２ａの端面からチャネル長方向に伸長した領域を有しており、第２の導電層２４５ａと酸化物半導体層２４４の少なくともチャネル形成領域とは接している。また、第２の導電層２４５ｂは、第１の導電層２４２ｂの端面からチャネル長方向に伸長した領域を有しており、第２の導電層２４５ｂと酸化物半導体層２４４の少なくともチャネル形成領域とは接している。

【０１０９】

さらに、図４に示すトランジスタ２８０は、第２の電極層２４５ａにおいて、第１の導電層２４２ａの端面からチャネル長方向に伸長した領域上に、サイドウォール絶縁層２５２ａを有し、第２の電極層２４５ｂにおいて、第１の導電層２４２ｂの端面からチャネル長方向に伸長した領域の上に、サイドウォール絶縁層２５２ｂを有している。サイドウォール絶縁層２５２ａは、酸化物半導体層２４４の少なくともチャネル形成領域、第２の導電層２４５ａ、第１の導電層２４２ａ、及び絶縁層２４３ａに接して設けられている。また、サイドウォール絶縁層２５２ａにおいて、酸化物半導体層２４４と接する領域の少なくとも一部は湾曲形状を有している。サイドウォール絶縁層２５２ｂは、酸化物半導体層２４４の少なくともチャネル形成領域、第２の導電層２４５ｂ、第１の導電層２４２ｂ、及び絶縁層２４３ｂに接して設けられている。また、サイドウォール絶縁層２５２ｂにおいて、酸化物半導体層２４４と接する領域の少なくとも一部は湾曲形状を有している。

【０１１０】

<トランジスタ２８０の作製工程の例>

次に、上記トランジスタ２８０の作製工程の例について、図５（Ａ）乃至（Ｆ）を参照して説明する。

【０１１１】

まず、基板２００上に第２の導電膜２４５を形成する。次いで、第２の導電膜２４５上に、第１の導電膜２４２を形成し、該第１の導電膜２４２上に絶縁膜２４５を形成する（図５（Ａ）参照）。

【０１１２】

ここで、基板２００は、実施の形態１で示した基板１００と同様の材料を用いることができる。また、第２の導電膜２４５は、実施の形態１で示した第２の導電膜１４５と同様の材料、成膜方法を用いて形成することができる。また、第１の導電膜２４２は、実施の形態１で示した第１の導電膜と同様の材料、成膜方法を用いて形成することができる。以上の詳細については、実施の形態１の記載を参酌することができる。

【０１１３】

ただし、第１の導電膜２４２と、第２の導電膜２４５とは、エッチング選択比が確保される材料を用いる。本実施の形態においては、第２の導電膜２４５として窒化チタン膜を形成し、第１の導電膜２４２としてタングステン膜またはモリブデン膜を形成するものとする。

【０１１４】

次いで、絶縁膜２４３上にマスクを形成し、該マスクを用いて絶縁膜２４３をエッチングすることにより、絶縁層２４３ａ、２４３ｂを形成する。絶縁膜２４３のエッチングには、ウェットエッチングまたはドライエッチングを用いることができ、ウェットエッチングとドライエッチングを組み合わせて用いてもよい。絶縁膜を所望の形状にエッチングできるよう、材料に合わせてエッチング条件（エッチングガスやエッチング液、エッチング時間、温度等）を適宜設定するものとする。ただし、トランジスタのチャネル長（Ｌ）を微細に加工するためには、ドライエッチングを用いるのが好ましい。ドライエッチングに用いるエッチングガスとしては、例えば、フッ化硫黄（SF_6）、フッ化窒素（NF_3）、トリフルオロメタン（CHF_3）などのフッ素を含むガス、又は、四フッ化メタン（CF_4）と水素の混合ガス等を用いることができ、希ガス（ヘリウム（Ｈｅ）、アルゴン（Ａｒ）、キセノン（Ｘｅ））、一酸化炭素、又は二酸化炭素等を添加しても良い。

【０１１５】

次いで、絶縁膜２４３のエッチングに用いたマスクを用いて、第１の導電膜２４２をエッチングすることにより、第１の導電層２４２ａ、２４２ｂを形成する（図５（Ｂ）参照）。なお、第１の導電膜２４２をエッチングする際には、第２の導電膜２４５とのエッチングの選択比が確保されるエッチング材料を用いる。また、第１の導電膜２４２をエッチングする前にマスクを除去し、絶縁層２４３ａ及び絶縁層２４３ｂをマスクとして用いて第１の導電膜２４２をエッチングしても良い。

【０１１６】

本実施の形態においては、第１の導電膜２４２をエッチングするためのエッチングガスとして四フッ化メタン（CF_4）と塩素（Cl_2）と酸素（O_2）との混合ガス、四フッ化メタン（CF_4）と酸素（O_2）の混合ガス、フッ化硫黄（SF_6）と塩素（Cl_2）と酸素（O_2）との混合ガス、または、フッ化硫黄（SF_6）と酸素（O_2）との混合ガスを用いるものとする。

【０１１７】

絶縁層２４３ａ、絶縁層２４３ｂを設けることで、後に形成されるソース電極またはドレイン電極と、酸化物半導体層との接触領域（接触面積など）の制御が容易になる。つまり、ソース電極またはドレイン電極の抵抗の制御が容易になり、短チャネル効果の抑制を効果的に行うことができる。また、絶縁層２４３ａ、絶縁層２４３ｂを設けることにより、後に形成されるゲート電極と、ソース電極及びドレイン電極と、の間の寄生容量を低減することが可能である。

【０１１８】

次に、絶縁層２４３ａ、２４３ｂ、および、露出した第２の導電膜２４５を覆うように絶縁膜２５２を形成する（図５（Ｃ）参照）。絶縁膜２５２は、ＣＶＤ法やスパッタリング法を用いて形成することができる。また、絶縁膜２５２は、酸化シリコン、窒化シリコン

、酸化窒化シリコン、酸化アルミニウムなどを含むように形成するのが好適である。また、絶縁膜２５２は、単層構造としても良いし、積層構造としても良い。
【０１１９】
次に、第２の導電膜２４５の露出した領域（第１の導電層２４２ａと第１の導電層２４２ｂの間の領域）上に、サイドウォール絶縁層２５２ａ、２５２ｂを形成する（図５（Ｄ）参照）。サイドウォール絶縁層２５２ａ、２５２ｂは、絶縁膜２５２に異方性の高いエッチング処理を行うことで、自己整合的に形成することができる。ここで、異方性の高いエッチングとしては、ドライエッチングが好ましく、例えば、エッチングガスとして、トリフルオロメタン（$ＣＨＦ_3$）などのフッ素を含むガスを用いることができ、ヘリウム（Ｈｅ）やアルゴン（Ａｒ）などの希ガスを添加しても良い。さらに、ドライエッチングとして、基板に高周波電圧を印加する、反応性イオンエッチング法（ＲＩＥ法）を用いるのが好ましい。
【０１２０】
次に、サイドウォール絶縁層２５２ａ、２５２ｂをマスクとして第２の導電膜２４５を選択的にエッチングし、第２の導電層２４５ａ、２４５ｂを形成する（図５（Ｅ）参照）。このエッチング工程によって、第２の導電層２４５ａ及び第１の導電層２４２ａが積層したソース電極と、第２の導電層２４５ｂ及び第１の導電層２４２ｂが積層したドレイン電極とが形成される。なお、第２の導電膜２４５のエッチングは、サイドウォール絶縁層２５２ａ、２５２ｂをマスクとして用いること以外は、実施の形態１で図２（Ｃ）を用いて示した方法と同様の方法で行うことができる。
【０１２１】
トランジスタ２８０のチャネル長（Ｌ）は、第２の導電層２４５ａの下端部と第２の導電層２４５ｂの下端部との間隔によって決定される。チャネル長（Ｌ）は、トランジスタ２８０の用途によって異なるが、例えば１０ｎｍ乃至１０００ｎｍ、好ましくは２０ｎｍ乃至４００ｎｍとすることができる。
【０１２２】
なお、本実施の形態で示すトランジスタの作製工程では、サイドウォール絶縁層２５２ａまたは２５２ｂを用いて第２の導電膜２４５をエッチングしているため、第２の導電層２４５ａにおいて、第１の導電層２４２ａの端面からチャネル長方向に伸長した領域のチャネル長方向の長さ（$Ｌ_Ｓ$）と、サイドウォール絶縁層２５２ａの底面におけるチャネル長方向の長さは略一致している。同様に、第２の導電層２４５ｂにおいて、第１の導電層２４２ｂの端面からチャネル長方向に伸長した領域のチャネル長方向の長さ（$Ｌ_Ｄ$）と、サイドウォール絶縁層２５２ｂの底面におけるチャネル長方向の長さは略一致している。サイドウォール絶縁層２５２ａ、２５２ｂは、絶縁膜２５２のエッチング処理によって自己整合的に形成されるため、上記（$Ｌ_Ｓ$）または（$Ｌ_Ｄ$）は、絶縁膜２５２の膜厚によって決定される。つまり、絶縁膜２５２の膜厚を制御することで、トランジスタ２８０のチャネル長（Ｌ）を微細に調整することができる。例えば、トランジスタ２８０のチャネル長（Ｌ）を、マスク形成のための露光装置の最小加工寸法より微細に調整することもできる。このため、トランジスタ２８０の所望のチャネル長（Ｌ）および、第１の導電層２４２ａ、２４２ｂの加工に用いる露光装置の解像度等に応じて、絶縁膜２５２の膜厚を決定すればよい。
【０１２３】
次に、絶縁層２４３ａ、２４３ｂ、サイドウォール絶縁層２５２ａ、２５２ｂを覆い、且つ、第２の導電層２４５ａ及び第２の導電層２４５ｂに接するように酸化物半導体層２４４を形成し、酸化物半導体層２４４上にゲート絶縁層２４６を形成する。その後、ゲート絶縁層２４６上において、トランジスタ２８０のチャネル形成領域となる領域と重畳する領域にゲート電極２４８を形成する（図５（Ｆ）参照）。
【０１２４】
酸化物半導体層２４４は、実施の形態１で示した酸化物半導体層１４４と同様の材料、方法により形成することができる。また、酸化物半導体層２４４に対しては、熱処理（第１

の熱処理）を行うことが望ましい。詳細については、実施の形態１の記載を参酌することができる。

【０１２５】

ゲート絶縁層２４６は、実施の形態１で示したゲート絶縁層１４６と同様の材料、方法により形成することができる。また、ゲート絶縁層２４６の形成後には、不活性ガス雰囲気下、または酸素雰囲気下で熱処理（第２の熱処理）を行うのが望ましい。詳細については、実施の形態１の記載を参酌することができる。

【０１２６】

ゲート電極２４８は、ゲート絶縁層２４６上に導電膜を形成した後に、当該導電膜を選択的にエッチングすることによって形成することができる。ゲート電極２４８は、実施の形態１で示したゲート電極１４８と同様の材料、方法により形成することができる。

【０１２７】

なお、トランジスタ２８０のソース電極は、第２の導電層２４５ａにおいて、第１の導電層２４２ａの端面よりもチャネル長方向に伸長した領域の端面で、酸化物半導体層２４４と接している。また、ドレイン電極は、第２の導電層２４５ｂにおいて、第１の導電層２４２ｂの端面よりもチャネル長方向に伸長した領域の端面で、酸化物半導体層２４４と接している。このように、第１の導電層２４２ａ、２４２ｂよりも膜厚の小さい第２の導電層２４５ａ、２４５ｂの端面において酸化物半導体層２４４と接することで、ソース電極またはドレイン電極と酸化物半導体層２４４との接触面積を低減することができるため、接触界面におけるコンタクト抵抗を増大させることができる。したがって、トランジスタ２８０のチャネル長（Ｌ）を短くしても、ソース電極とドレイン電極の間の電界を緩和して短チャネル効果を抑制することができる。加えて、第２の導電層を第１の導電層よりも高抵抗な材料を用いて作製すると、より効果的にコンタクト抵抗を高めることができるため、好ましい。なお、開示する発明の技術思想は、ソース電極またはドレイン電極に高抵抗な領域を形成することにあるので、ソース電極またはドレイン電極は、厳密に第２の導電層２４５ａ及び第２の導電層２４５ｂの端面においてのみ酸化物半導体層２４４と接する必要はない。

【０１２８】

以上により、酸化物半導体層２４４を用いたトランジスタ２８０を作製することができる。

【０１２９】

本実施の形態に示すトランジスタ２８０のチャネル長（Ｌ）は、サイドウォール絶縁層２５２ａ、２５２ｂを形成するための絶縁層２５２の膜厚によって微細に制御することができる。よって、該絶縁層２５２の膜厚を適宜設定することにより、トランジスタ２８０のチャネル長（Ｌ）を縮小し、容易に半導体装置の微細化を図ることができる。

【０１３０】

本実施の形態に示すトランジスタ２８０は、第２の導電層２４５ａにおいて、第１の導電層２４２ａの端面からチャネル長方向に伸長した領域、及び、第２の導電層２４５ｂにおいて、第１の導電層２４２ｂの端面からチャネル長方向に伸長した領域に、サイドウォール絶縁層２５２ａ及びサイドウォール絶縁層２５２ｂがそれぞれ設けられることにより、酸化物半導体層２４４、ゲート絶縁層２４６の被覆性を向上し、接続不良などの発生を抑制することができる。

【０１３１】

さらに、本実施の形態に示すトランジスタ２８０は、第２の導電層２４５ａに第１の導電層２４２ａの端面からチャネル長方向に伸長した領域を設け、且つ、第２の導電層２４５ｂに第１の導電層２４２ｂの端面からチャネル長方向に伸長した領域を設けて、酸化物半導体層２４４のチャネル形成領域と接する領域の近傍を高抵抗領域とすることで、ソース電極とドレイン電極の間の電界を緩和して、しきい値電圧低下などの短チャネル効果を抑制することができる。

【０１３２】

このように、開示する発明の一態様では、微細化に伴う問題点を解消することができるため、結果として、トランジスタサイズを十分に小さくすることが可能になる。トランジスタサイズを十分に小さくすることで、半導体装置の占める面積が小さくなるため、半導体装置の取り数が増大する。これにより、半導体装置あたりの製造コストは抑制される。また、半導体装置が小型化されるため、同程度の大きさでさらに機能が高められた半導体装置を実現することができる。また、チャネル長の縮小による、動作の高速化、低消費電力化などの効果を得ることもできる。つまり、開示する発明の一態様により酸化物半導体を用いたトランジスタの微細化が達成されることで、これに付随する様々な効果を得ることが可能である。

【０１３３】

以上、本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。

【０１３４】

（実施の形態３）

本実施の形態では、開示する発明の一態様に係る半導体装置の応用例について、図６を参照して説明する。ここでは、記憶装置の一例について説明する。なお、回路図においては、酸化物半導体を用いたトランジスタであることを示すために、ＯＳの符号を併せて付す場合がある。

【０１３５】

図６（Ａ－１）に示す半導体装置において、第１の配線（１ｓｔ　Ｌｉｎｅ）とトランジスタ３００のソース電極とは、電気的に接続され、第２の配線（２ｎｄ　Ｌｉｎｅ）とトランジスタ３００のドレイン電極とは、電気的に接続されている。また、第３の配線（３ｒｄ　Ｌｉｎｅ）とトランジスタ３１０のソース電極またはドレイン電極の他方とは、電気的に接続され、第４の配線（４ｔｈ　Ｌｉｎｅ）と、トランジスタ３１０のゲート電極とは、電気的に接続されている。そして、トランジスタ３００のゲート電極と、トランジスタ３１０のソース電極またはドレイン電極の一方は、容量素子３２０の電極の一方と電気的に接続され、第５の配線（５ｔｈ　Ｌｉｎｅ）と、容量素子３２０の電極の他方は電気的に接続されている。

【０１３６】

ここで、トランジスタ３１０には、上述の酸化物半導体を用いたトランジスタが適用される。酸化物半導体を用いたトランジスタは、オフ電流が極めて小さいという特徴を有している。このため、トランジスタ３１０をオフ状態とすることで、トランジスタ３００のゲート電極の電位を極めて長時間にわたって保持することが可能である。そして、容量素子３２０を有することにより、トランジスタ３００のゲート電極に与えられた電荷の保持が容易になり、また、保持された情報の読み出しが容易になる。

【０１３７】

なお、トランジスタ３００については特に限定されない。情報の読み出し速度を向上させるという観点からは、例えば、単結晶シリコンを用いたトランジスタなど、スイッチング速度の高いトランジスタを適用するのが好適である。

【０１３８】

また、図６（Ｂ）に示すように、容量素子３２０を設けない構成とすることも可能である。

【０１３９】

図６（Ａ－１）に示す半導体装置では、トランジスタ３００のゲート電極の電位が保持可能という特徴を生かすことで、次のように、情報の書き込み、保持、読み出しが可能である。

【０１４０】

はじめに、情報の書き込みおよび保持について説明する。まず、第４の配線の電位を、トランジスタ３１０がオン状態となる電位にして、トランジスタ３１０をオン状態とする。これにより、第３の配線の電位が、トランジスタ３００のゲート電極、および容量素子３

２０に与えられる。すなわち、トランジスタ３００のゲート電極には、所定の電荷が与えられる（書き込み）。ここでは、異なる二つの電位を与える電荷（以下、低電位を与える電荷を電荷Q_L、高電位を与える電荷を電荷Q_Hという）のいずれかが与えられるものとする。なお、異なる三つまたはそれ以上の電位を与える電荷を適用して、記憶容量を向上させても良い。その後、第４の配線の電位を、トランジスタ３１０がオフ状態となる電位にして、トランジスタ３１０をオフ状態とすることにより、トランジスタ３００のゲート電極に与えられた電荷が保持される（保持）。

【０１４１】

トランジスタ３１０のオフ電流は極めて小さいから、トランジスタ３００のゲート電極の電荷は長時間にわたって保持される。

【０１４２】

次に、情報の読み出しについて説明する。第１の配線に所定の電位（定電位）を与えた状態で、第５の配線に適切な電位（読み出し電位）を与えると、トランジスタ３００のゲート電極に保持された電荷量に応じて、第２の配線は異なる電位をとる。一般に、トランジスタ３００をｎチャネル型とすると、トランジスタ３００のゲート電極にQ_Hが与えられている場合の見かけのしきい値V_{th_H}は、トランジスタ３００のゲート電極にQ_Lが与えられている場合の見かけのしきい値V_{th_L}より低くなるためである。ここで、見かけのしきい値電圧とは、トランジスタ３００を「オン状態」とするために必要な第５の配線の電位をいうものとする。したがって、第５の配線の電位をV_{th_H}とV_{th_L}の中間の電位V_0とすることにより、トランジスタ３００のゲート電極に与えられた電荷を判別できる。例えば、書き込みにおいて、Q_Hが与えられていた場合には、第５の配線の電位がV_0（$>V_{th_H}$）となれば、トランジスタ３００は「オン状態」となる。Q_Lが与えられていた場合には、第５の配線の電位がV_0（$<V_{th_L}$）となっても、トランジスタ３００は「オフ状態」のままである。このため、第２の配線の電位を見ることで、保持されている情報を読み出すことができる。

【０１４３】

なお、メモリセルをアレイ状に配置して用いる場合には、所望のメモリセルの情報のみを読み出せることが必要になる。このように、所定のメモリセルの情報を読み出し、それ以外のメモリセルの情報を読み出さない場合には、読み出しの対象ではないメモリセルの第５の配線に対して、ゲート電極の状態にかかわらずトランジスタ３００が「オフ状態」となるような電位、つまり、V_{th_H}より小さい電位を与えればよい。または、ゲート電極の状態にかかわらずトランジスタ３００が「オン状態」となるような電位、つまり、V_{th_L}より大きい電位を第５の配線に与えればよい。

【０１４４】

次に、情報の書き換えについて説明する。情報の書き換えは、上記情報の書き込みおよび保持と同様に行われる。つまり、第４の配線の電位を、トランジスタ３１０がオン状態となる電位にして、トランジスタ３１０をオン状態とする。これにより、第３の配線の電位（新たな情報に係る電位）が、トランジスタ３００のゲート電極および容量素子３２０に与えられる。その後、第４の配線の電位を、トランジスタ３１０がオフ状態となる電位にして、トランジスタ３１０をオフ状態とすることにより、トランジスタ３００のゲート電極は、新たな情報に係る電荷が与えられた状態となる。

【０１４５】

このように、開示する発明に係る半導体装置は、再度の情報の書き込みによって直接的に情報を書き換えることが可能である。このためフラッシュメモリなどにおいて必要とされる高電圧を用いてのフローティングゲートからの電荷の引き抜きが不要であり、消去動作に起因する動作速度の低下を抑制することができる。つまり、半導体装置の高速動作が実現される。

【０１４６】

なお、トランジスタ３１０のソース電極またはドレイン電極は、トランジスタ３００のゲート電極と電気的に接続されることにより、不揮発性メモリ素子として用いられるフロー

ティングゲート型トランジスタのフローティングゲートと同等の作用を奏する。このため、図中、トランジスタ３１０のソース電極またはドレイン電極とトランジスタ３００のゲート電極が電気的に接続される部位をフローティングゲート部ＦＧと呼ぶ場合がある。トランジスタ３１０がオフの場合、当該フローティングゲート部ＦＧは絶縁体中に埋設されたと見ることができ、フローティングゲート部ＦＧには電荷が保持される。酸化物半導体を用いたトランジスタ３１０のオフ電流は、シリコン半導体などで形成されるトランジスタの１０万分の１以下であるため、トランジスタ３１０のリークによる、フローティングゲート部ＦＧに蓄積される電荷の消失を無視することが可能である。つまり、酸化物半導体を用いたトランジスタ３１０により、電力の供給が無くても情報の保持が可能な不揮発性の記憶装置を実現することが可能である。

【０１４７】

例えば、トランジスタ３１０の室温でのオフ電流が１０ｚＡ（１ｚＡ（ゼプトアンペア）は１×１０$^{-21}$Ａ）以下であり、容量素子３２０の容量値が１０ｆＦ程度である場合には、少なくとも１０^{4}秒以上のデータ保持が可能である。なお、当該保持時間が、トランジスタ特性や容量値によって変動することはいうまでもない。

【０１４８】

また、この場合、従来のフローティングゲート型トランジスタにおいて指摘されているゲート絶縁膜（トンネル絶縁膜）の劣化という問題が存在しない。つまり、従来問題とされていた、電子をフローティングゲートに注入する際のゲート絶縁膜の劣化という問題を解消することができる。これは、原理的な書き込み回数の制限が存在しないことを意味するものである。また、従来のフローティングゲート型トランジスタにおいて書き込みや消去の際に必要であった高電圧も不要である。

【０１４９】

図６（Ａ－１）に示す半導体装置は、当該半導体装置を構成するトランジスタなどの要素が抵抗および容量を含むものとして、図６（Ａ－２）のように考えることが可能である。つまり、図６（Ａ－２）では、トランジスタ３００および容量素子３２０が、それぞれ、抵抗および容量を含んで構成されると考えていることになる。Ｒ１およびＣ１は、それぞれ、容量素子３２０の抵抗値および容量値であり、抵抗値Ｒ１は、容量素子３２０を構成する絶縁層による抵抗値に相当する。また、Ｒ２およびＣ２は、それぞれ、トランジスタ３００の抵抗値および容量値であり、抵抗値Ｒ２はトランジスタ３００がオン状態の時のゲート絶縁層による抵抗値に相当し、容量値Ｃ２はいわゆるゲート容量（ゲート電極と、ソース電極またはドレイン電極との間に形成される容量、及び、ゲート電極とチャネル形成領域との間に形成される容量）の容量値に相当する。

【０１５０】

トランジスタ３１０がオフ状態にある場合のソース電極とドレイン電極の間の抵抗値（実効抵抗とも呼ぶ）をＲＯＳとすると、トランジスタ３１０のゲートリークが十分に小さい条件において、Ｒ１およびＲ２が、Ｒ１≧ＲＯＳ、Ｒ２≧ＲＯＳを満たす場合には、電荷の保持期間（情報の保持期間ということもできる）は、主としてトランジスタ３１０のオフ電流によって決定されることになる。

【０１５１】

逆に、当該条件を満たさない場合には、トランジスタ３１０のオフ電流が十分に小さくとも、保持期間を十分に確保することが困難になる。トランジスタ３１０のオフ電流以外のリーク電流（例えば、ソース電極とゲート電極の間において生じるリーク電流等）が大きいためである。このことから、本実施の形態において開示する半導体装置は、上述の関係を満たすものであることが望ましいといえる。

【０１５２】

一方で、Ｃ１とＣ２は、Ｃ１≧Ｃ２の関係を満たすことが望ましい。Ｃ１を大きくすることで、第５の配線によってフローティングゲート部ＦＧの電位を制御する際（例えば、読み出しの際）に、第５の配線の電位の変動を低く抑えることができるためである。

【０１５３】

上述の関係を満たすことで、より好適な半導体装置を実現することが可能である。なお、Ｒ１およびＲ２は、トランジスタ３００のゲート絶縁層や容量素子３２０の絶縁層によって制御される。Ｃ１およびＣ２についても同様である。よって、ゲート絶縁層の材料や厚さなどを適宜設定し、上述の関係を満たすようにすることが望ましい。

【０１５４】

本実施の形態で示す半導体装置においては、フローティングゲート部ＦＧが、フラッシュメモリ等のフローティングゲート型のトランジスタのフローティングゲートと同等の作用をするが、本実施の形態のフローティングゲート部ＦＧは、フラッシュメモリ等のフローティングゲートと本質的に異なる特徴を有する。フラッシュメモリでは、コントロールゲートに印加される電圧が高いため、その電位の影響が、隣接するセルのフローティングゲートにおよぶことを防ぐために、セルとセルとの間隔をある程度保つ必要が生じる。このことは、半導体装置の高集積化を阻害する要因の一つである。そして、当該要因は、高電界をかけてトンネル電流を発生させるというフラッシュメモリの根本的な原理に起因するものである。

【０１５５】

また、フラッシュメモリの上記原理によって、絶縁膜の劣化が進行し、書き換え回数の限界（$１０^{４}$～$１０^{５}$回程度）という別の問題も生じる。

【０１５６】

開示する発明に係る半導体装置は、酸化物半導体を用いたトランジスタのスイッチングによって動作し、上述のようなトンネル電流による電荷注入の原理を用いない。すなわち、フラッシュメモリのような、電荷を注入するための高電界が不要である。これにより、隣接セルに対する、コントロールゲートによる高電界の影響を考慮する必要がないため、高集積化が容易になる。

【０１５７】

また、トンネル電流による電荷の注入を用いないため、メモリセルの劣化の原因が存在しない。つまり、フラッシュメモリと比較して高い耐久性および信頼性を有することになる。

【０１５８】

また、高電界が不要であり、大型の周辺回路（昇圧回路など）が不要である点も、フラッシュメモリに対するアドバンテージである。

【０１５９】

なお、Ｃ１を構成する絶縁層の比誘電率εｒ１と、Ｃ２を構成する絶縁層の比誘電率εｒ２とを異ならせる場合には、Ｃ１の面積Ｓ１と、Ｃ２の面積Ｓ２とが、２・Ｓ２≧Ｓ１（望ましくはＳ２≧Ｓ１）を満たしつつ、Ｃ１≧Ｃ２を実現することが容易である。具体的には、例えば、Ｃ１においては、酸化ハフニウムなどのｈｉｇｈ－ｋ材料でなる膜、または酸化ハフニウムなどのｈｉｇｈ－ｋ材料でなる膜と酸化物半導体でなる膜との積層構造を採用してεｒ１を１０以上、好ましくは１５以上とし、Ｃ２においては、酸化シリコンを採用して、εｒ２＝３～４とすることができる。

【０１６０】

このような構成を併せて用いることで、開示する発明に係る半導体装置の、より一層の高集積化が可能である。

【０１６１】

なお、上記説明は、電子を多数キャリアとするｎ型トランジスタ（ｎチャネル型トランジスタ）を用いる場合についてのものであるが、ｎ型トランジスタに代えて、正孔を多数キャリアとするｐ型トランジスタを用いることができるのはいうまでもない。

【０１６２】

以上示したように、開示する発明の一態様の半導体装置は、オフ状態でのソースとドレイン間のリーク電流（オフ電流）が少ない書き込み用トランジスタ、該書き込み用トランジスタと異なる半導体材料を用いた読み出し用トランジスタ及び容量素子を含む不揮発性のメモリセルを有している。

【０１６３】
書き込み用トランジスタのオフ電流は、使用時の温度（例えば、２５℃）で１００ｚＡ（１×１０$^{-19}$Ａ）以下、好ましくは１０ｚＡ（１×１０$^{-20}$Ａ）以下、さらに好ましくは、１ｚＡ（１×１０$^{-21}$Ａ）以下である。通常のシリコン半導体では、上述のように低いオフ電流を得ることは困難であるが、酸化物半導体を適切な条件で加工して得られたトランジスタにおいては達成しうる。このため、書き込み用トランジスタとして、酸化物半導体を含むトランジスタを用いることが好ましい。

【０１６４】
さらに酸化物半導体を用いたトランジスタはサブスレッショルドスイング値（Ｓ値）が小さいため、比較的移動度が低くてもスイッチング速度を十分大きくすることが可能である。よって、該トランジスタを書き込み用トランジスタとして用いることで、フローティングゲート部ＦＧに与えられる書き込みパルスの立ち上がりを極めて急峻にすることができる。また、オフ電流が小さいため、フローティングゲート部ＦＧに保持させる電荷量を少なくすることが可能である。つまり、酸化物半導体を用いたトランジスタを書き込み用トランジスタとして用いることで、情報の書き換えを高速に行うことができる。

【０１６５】
読み出し用トランジスタとしては、オフ電流についての制限はないが、読み出しの速度を高くするために、高速で動作するトランジスタを用いるのが望ましい。例えば、読み出し用トランジスタとしてスイッチング速度が１ナノ秒以下のトランジスタを用いるのが好ましい。

【０１６６】
メモリセルへの情報の書き込みは、書き込み用トランジスタをオン状態とすることにより、書き込み用トランジスタのソース電極またはドレイン電極の一方と、容量素子の電極の一方と、読み出し用トランジスタのゲート電極とが電気的に接続されたフローティングゲート部ＦＧに電位を供給し、その後、書き込み用トランジスタをオフ状態とすることにより、フローティングゲート部ＦＧに所定量の電荷を保持させることで行う。ここで、書き込み用トランジスタのオフ電流は極めて小さいため、フローティングゲート部ＦＧに供給された電荷は長時間にわたって保持される。オフ電流が例えば実質的に０であれば、従来のＤＲＡＭで必要とされたリフレッシュ動作が不要となるか、または、リフレッシュ動作の頻度を極めて低く（例えば、一ヶ月乃至一年に一度程度）することが可能となり、半導体装置の消費電力を十分に低減することができる。

【０１６７】
また、メモリセルへの再度の情報の書き込みによって直接的に情報を書き換えることが可能である。このためフラッシュメモリなどにおいて必要とされる消去動作が不要であり、消去動作に起因する動作速度の低下を抑制することができる。つまり、半導体装置の高速動作が実現される。また、従来のフローティングゲート型トランジスタで書き込みや消去の際に必要とされた高い電圧を必要としないため、半導体装置の消費電力をさらに低減することができる。本実施の形態に係るメモリセルに印加される電圧（メモリセルの各端子に同時に印加される電位の最大のものと最小のものの差）の最大値は、２段階（１ビット）の情報を書き込む場合、一つのメモリセルにおいて、５Ｖ以下、好ましくは３Ｖ以下である。

【０１６８】
開示する発明に係る半導体装置に配置されるメモリセルは、書き込み用トランジスタと、読み出し用トランジスタと、容量素子とを少なくとも含んでいればよく、また、容量素子の面積は小さくても動作可能である。したがって、メモリセルあたりの面積を、例えば、１メモリセルあたり６つのトランジスタを必要とするＳＲＡＭと比較して、十分に小さくすることが可能であり、半導体装置においてメモリセルを高密度で配置することができる。

【０１６９】
また、従来のフローティングゲート型トランジスタでは、書き込み時にゲート絶縁膜（ト

ンネル絶縁膜）中を電荷が移動するために、該ゲート絶縁膜（トンネル絶縁膜）の劣化が不可避であった。しかしながら、本発明の一態様に係るメモリセルにおいては、書き込み用トランジスタのスイッチング動作により情報の書き込みがなされるため、ゲート絶縁膜の劣化の問題がない。これは、原理的な書き込み回数の制限が存在せず、書き換え耐性が極めて高いことを意味するものである。例えば、本発明の一態様に係るメモリセルは、１×１０^{９}回（１０億回）以上の書き込み後であっても、電流－電圧特性に劣化が見られない。

【０１７０】

さらに、メモリセルの書き込み用トランジスタとして酸化物半導体を用いたトランジスタを用いる場合、酸化物半導体は一般にエネルギーギャップが大きく（例えば、Ｉｎ－Ｇａ－Ｚｎ－Ｏ系の場合３．０～３．５ｅＶ）熱励起キャリアが極めて少ないこともあり、例えば、１５０℃もの高温環境下でもメモリセルの電流－電圧特性に劣化が見られない。

【０１７１】

本発明者らは、鋭意研究の結果、酸化物半導体を用いたトランジスタは、１５０℃の高温下であっても特性の劣化を起こさず、且つオフ電流が１００ｚＡ以下と極めて小さいという優れた特性を有すること見出した。本実施の形態では、このような優れた特性を有するトランジスタをメモリセルの書き込み用トランジスタとして適用し、従来にない特徴を有する半導体装置を提供するものである。

【０１７２】

開示する発明の一態様により、酸化物半導体を用いたトランジスタにおいて、不良を抑制しつつ、または良好な特性を維持しつつ、微細化を達成することができる。そして、このようなトランジスタを用いることにより、上述のような優れた記憶装置を、高度に集積化することができるのである。

【０１７３】

以上、本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。

【０１７４】

（実施の形態４）

本実施の形態では、開示する発明の一態様に係る半導体装置の応用例について、図７および図８を用いて説明する。

【０１７５】

図７（Ａ）および図７（Ｂ）は、図６（Ａ－１）に示す半導体装置（以下、メモリセル４００とも記載する。）を複数用いて形成される半導体装置の回路図である。図７（Ａ）は、メモリセル４００が直列に接続された、いわゆるＮＡＮＤ型の半導体装置の回路図であり、図７（Ｂ）は、メモリセル４００が並列に接続された、いわゆるＮＯＲ型の半導体装置の回路図である。

【０１７６】

図７（Ａ）に示す半導体装置は、ソース線ＳＬ、ビット線ＢＬ、第１信号線Ｓ１、複数本の第２信号線Ｓ２、複数本のワード線ＷＬ、複数のメモリセル４００を有する。図７（Ａ）では、ソース線ＳＬおよびビット線ＢＬを１本ずつ有する構成となっているが、これに限られることなく、ソース線ＳＬおよびビット線ＢＬを複数本有する構成としてもよい。

【０１７７】

各メモリセル４００において、トランジスタ３００のゲート電極と、トランジスタ３１０のソース電極またはドレイン電極の一方と、容量素子３２０の電極の一方とは、電気的に接続されている。また、第１信号線Ｓ１とトランジスタ３１０のソース電極またはドレイン電極の他方とは、電気的に接続され、第２信号線Ｓ２と、トランジスタ３１０のゲート電極とは、電気的に接続されている。そして、ワード線ＷＬと、容量素子３２０の電極の他方は電気的に接続されている。

【０１７８】

また、メモリセル４００が有するトランジスタ３００のソース電極は、隣接するメモリセ

ル４００のトランジスタ３００のドレイン電極と電気的に接続され、メモリセル４００が有するトランジスタ３００のドレイン電極は、隣接するメモリセル４００のトランジスタ３００のソース電極と電気的に接続される。ただし、直列に接続された複数のメモリセルのうち、一方の端に設けられたメモリセル４００が有するトランジスタ３００のドレイン電極は、ビット線と電気的に接続される。また、直列に接続された複数のメモリセルのうち、他方の端に設けられたメモリセル４００が有するトランジスタ３００のソース電極は、ソース線と電気的に接続される。

【０１７９】

図７（Ａ）に示す半導体装置では、行ごとの書き込み動作および読み出し動作を行う。書き込み動作は次のように行われる。書き込みを行う行の第２の信号線Ｓ２にトランジスタ３１０がオン状態となる電位を与え、書き込みを行う行のトランジスタ３１０をオン状態にする。これにより、指定した行のトランジスタ３００のゲート電極に第１の信号線Ｓ１の電位が与えられ、該ゲート電極に所定の電荷が与えられる。このようにして、指定した行のメモリセルにデータを書き込むことができる。

【０１８０】

また、読み出し動作は次のように行われる。まず、読み出しを行う行以外のワード線ＷＬに、トランジスタ３００のゲート電極に与えられた電荷によらず、トランジスタ３００がオン状態となるような電位を与え、読み出しを行う行以外のトランジスタ３００をオン状態とする。それから、読み出しを行う行のワード線ＷＬに、トランジスタ３００のゲート電極が有する電荷によって、トランジスタ３００のオン状態またはオフ状態が選択されるような電位（読み出し電位）を与える。そして、ソース線ＳＬに定電位を与え、ビット線ＢＬに接続されている読み出し回路（図示しない）を動作状態とする。ここで、ソース線ＳＬ－ビット線ＢＬ間の複数のトランジスタ３００は、読み出しを行う行を除いてオン状態となっているため、ソース線ＳＬ－ビット線ＢＬ間のコンダクタンスは、読み出しを行う行のトランジスタ３００の状態（オン状態またはオフ状態）によって決定される。読み出しを行う行のトランジスタ３００のゲート電極が有する電荷によって、トランジスタのコンダクタンスは異なるから、それに応じて、ビット線ＢＬの電位は異なる値をとることになる。ビット線の電位を読み出し回路によって読み出すことで、指定した行のメモリセルから情報を読み出すことができる。

【０１８１】

図７（Ｂ）に示す半導体装置は、ソース線ＳＬ、ビット線ＢＬ、第１信号線Ｓ１、第２信号線Ｓ２、およびワード線ＷＬをそれぞれ複数本有し、複数のメモリセル４００を有する。各トランジスタ３００のゲート電極と、トランジスタ３１０のソース電極またはドレイン電極の一方と、容量素子３２０の電極の一方とは、電気的に接続されている。また、ソース線ＳＬとトランジスタ３００のソース電極とは、電気的に接続され、ビット線ＢＬとトランジスタ３００のドレイン電極とは、電気的に接続されている。また、第１信号線Ｓ１とトランジスタ３１０のソース電極またはドレイン電極の他方とは、電気的に接続され、第２信号線Ｓ２と、トランジスタ３１０のゲート電極とは、電気的に接続されている。そして、ワード線ＷＬと、容量素子３２０の電極の他方は電気的に接続されている。

【０１８２】

図７（Ｂ）に示す半導体装置では、行ごとの書き込み動作および読み出し動作を行う。書き込み動作は、上述の図７（Ａ）に示す半導体装置と同様の方法で行われる。読み出し動作は次のように行われる。まず、読み出しを行う行以外のワード線ＷＬに、トランジスタ３００のゲート電極に与えられた電荷によらず、トランジスタ３００がオフ状態となるような電位を与え、読み出しを行う行以外のトランジスタ３００をオフ状態とする。それから、読み出しを行う行のワード線ＷＬに、トランジスタ３００のゲート電極が有する電荷によって、トランジスタ３００のオン状態またはオフ状態が選択されるような電位（読み出し電位）を与える。そして、ソース線ＳＬに定電位を与え、ビット線ＢＬに接続されている読み出し回路（図示しない）を動作状態とする。ここで、ソース線ＳＬ－ビット線ＢＬ間のコンダクタンスは、読み出しを行う行のトランジスタ３００の状態（オン状態また

はオフ状態）によって決定される。つまり、読み出しを行う行のトランジスタ３００のゲート電極が有する電荷によって、ビット線ＢＬの電位は異なる値をとることになる。ビット線の電位を読み出し回路によって読み出すことで、指定した行のメモリセルから情報を読み出すことができる。

【０１８３】

なお、上記においては、各メモリセル４００に保持させる情報量を１ビットとしたが、本実施の形態に示す記憶装置の構成はこれに限られない。トランジスタ３００のゲート電極に与える電位を３以上用意して、各メモリセル４００が保持する情報量を増加させても良い。例えば、トランジスタ３００のゲート電極にあたえる電位を４種類とする場合には、各メモリセルに２ビットの情報を保持させることができる。

【０１８４】

次に、図７に示す半導体装置などに用いることができる読み出し回路の一例について図８を用いて説明する。

【０１８５】

図８（Ａ）には、読み出し回路の概略を示す。当該読み出し回路は、トランジスタとセンスアンプ回路を有する。

【０１８６】

読み出し時には、端子Ａは読み出しを行うメモリセルが接続されたビット線に接続される。また、トランジスタのゲート電極にはバイアス電位Ｖｂｉａｓが印加され、端子Ａの電位が制御される。

【０１８７】

メモリセル４００は、格納されるデータに応じて、異なる抵抗値を示す。具体的には、選択したメモリセル４００のトランジスタ３００がオン状態の場合には低抵抗状態となり、選択したメモリセル４００のトランジスタ３００がオフ状態の場合には高抵抗状態となる。

【０１８８】

メモリセルが高抵抗状態の場合、端子Ａの電位が参照電位Ｖｒｅｆより高くなり、センスアンプは端子Ａの電位に対応する電位を出力する。一方、メモリセルが低抵抗状態の場合、端子Ａの電位が参照電位Ｖｒｅｆより低くなり、センスアンプ回路は端子Ａの電位に対応する電位を出力する。

【０１８９】

このように、読み出し回路を用いることで、メモリセルからデータを読み出すことができる。なお、本実施の形態の読み出し回路は一例である。他の回路を用いても良い。また、読み出し回路は、プリチャージ回路を有しても良い。参照電位Ｖｒｅｆの代わりに参照用のビット線が接続される構成としても良い。

【０１９０】

図８（Ｂ）に、センスアンプ回路の一例である差動型センスアンプを示す。差動型センスアンプは、入力端子Ｖｉｎ（＋）とＶｉｎ（－）と出力端子Ｖｏｕｔを有し、Ｖｉｎ（＋）とＶｉｎ（－）の差を増幅する。Ｖｉｎ（＋）＞Ｖｉｎ（－）であればＶｏｕｔは、概ねＨｉｇｈ出力、Ｖｉｎ（＋）＜Ｖｉｎ（－）であればＶｏｕｔは、概ねＬｏｗ出力となる。当該差動型センスアンプを読み出し回路に用いる場合、Ｖｉｎ（＋）とＶｉｎ（－）の一方は入力端子Ａと接続し、Ｖｉｎ（＋）とＶｉｎ（－）の他方には参照電位Ｖｒｅｆを与える。

【０１９１】

図８（Ｃ）に、センスアンプ回路の一例であるラッチ型センスアンプを示す。ラッチ型センスアンプは、入出力端子Ｖ１およびＶ２と、制御用信号Ｓｐ、Ｓｎの入力端子を有する。まず、信号ＳｐをＨｉｇｈ、信号ＳｎをＬｏｗとして、電源電位（Ｖｄｄ）を遮断する。そして、比較を行う電位をＶ１とＶ２に与える。その後、信号ＳｐをＬｏｗ、信号ＳｎをＨｉｇｈとして、電源電位（Ｖｄｄ）を供給すると、比較を行う電位Ｖ１ｉｎとＶ２ｉｎがＶ１ｉｎ＞Ｖ２ｉｎの関係にあれば、Ｖ１の出力はＨｉｇｈ、Ｖ２の出力はＬｏｗと

なり、Ｖ１ｉｎ<Ｖ２ｉｎの関係にあれば、Ｖ１の出力はＬｏｗ、Ｖ２の出力はＨｉｇｈとなる。このような関係を利用して、Ｖ１ｉｎとＶ２ｉｎの差を増幅することができる。当該ラッチ型センスアンプを読み出し回路に用いる場合、Ｖ１とＶ２の一方は、スイッチを介して端子Ａおよび出力端子と接続し、Ｖ１とＶ２の他方には参照電位Ｖｒｅｆを与える。

【０１９２】
本実施の形態に示す構成、方法などは、他の実施の形態に示す構成、方法などと適宜組み合わせて用いることができる。

【０１９３】
（実施の形態５）
本実施の形態では、上述の実施の形態で説明した半導体装置を電子機器に適用する場合について、図９を用いて説明する。本実施の形態では、コンピュータ、携帯電話機（携帯電話、携帯電話装置ともいう）、携帯情報端末（携帯型ゲーム機、音響再生装置なども含む）、デジタルカメラ、デジタルビデオカメラ、電子ペーパー、テレビジョン装置（テレビ、またはテレビジョン受信機ともいう）などの電子機器に、上述の半導体装置を適用する場合について説明する。

【０１９４】
図９（Ａ）は、ノート型のパーソナルコンピュータであり、筐体６０１、筐体６０２、表示部６０３、キーボード６０４などによって構成されている。筐体６０１と筐体６０２内には、先の実施の形態に示す微細化された半導体装置が設けられている。そのため、小型、高速動作、低消費電力、といった特徴を備えたノート型のパーソナルコンピュータが実現される。

【０１９５】
図９（Ｂ）は、携帯情報端末（ＰＤＡ）であり、本体６１１には、表示部６１３と、外部インターフェイス６１５と、操作ボタン６１４等が設けられている。また、携帯情報端末を操作するスタイラス６１２などを備えている。本体６１１内には、先の実施の形態に示す微細化された半導体装置が設けられている。そのため、小型、高速動作、低消費電力、といった特徴を備えた携帯情報端末が実現される。

【０１９６】
図９（Ｃ）は、電子ペーパーを実装した電子書籍６２０であり、筐体６２１と筐体６２３の２つの筐体で構成されている。筐体６２１及び筐体６２３には、それぞれ表示部６２５及び表示部６２７が設けられている。筐体６２１と筐体６２３は、軸部６３７により接続されており、該軸部６３７を軸として開閉動作を行うことができる。また、筐体６２１は、電源６３１、操作キー６３３、スピーカー６３５などを備えている。筐体６２１、筐体６２３の少なくとも一には、先の実施の形態に示す微細化された半導体装置が設けられている。そのため、小型、高速動作、低消費電力、といった特徴を備えた電子書籍が実現される。

【０１９７】
図９（Ｄ）は、携帯電話機であり、筐体６４０と筐体６４１の２つの筐体で構成されている。さらに、筐体６４０と筐体６４１は、スライドし、図９（Ｄ）のように展開している状態から重なり合った状態とすることができ、携帯に適した小型化が可能である。また、筐体６４１は、表示パネル６４２、スピーカー６４３、マイクロフォン６４４、ポインティングデバイス６４６、カメラ用レンズ６４７、外部接続端子６４８などを備えている。また、筐体６４０は、携帯電話機の充電を行う太陽電池セル６４９、外部メモリスロット６５０などを備えている。また、アンテナは、筐体６４１に内蔵されている。筐体６４０と筐体６４１の少なくとも一には、先の実施の形態に示す微細化された半導体装置が設けられている。そのため、小型、高速動作、低消費電力、といった特徴を備えた携帯電話機が実現される。

【０１９８】
図９（Ｅ）は、デジタルカメラであり、本体６６１、表示部６６７、接眼部６６３、操作

スイッチ６６４、表示部６６５、バッテリー６６６などによって構成されている。本体６６１内には、先の実施の形態に示す微細化された半導体装置が設けられている。そのため、小型、高速動作、低消費電力、といった特徴を備えたデジタルカメラが実現される。
【０１９９】
図９（Ｆ）は、テレビジョン装置６７０であり、筐体６７１、表示部６７３、スタンド６７５などで構成されている。テレビジョン装置６７０の操作は、筐体６７１が備えるスイッチや、リモコン操作機６８０により行うことができる。筐体６７１及びリモコン操作機６８０には、先の実施の形態に示す微細化された半導体装置が搭載されている。そのため、高速動作、低消費電力、といった特徴を備えたテレビジョン装置が実現される。
【０２００】
以上のように、本実施の形態に示す電子機器には、先の実施の形態に係る半導体装置が搭載されている。このため、小型、高速動作、低消費電力、といった特徴を備えた電子機器が実現される。
【実施例１】
【０２０１】
本実施例では、発明の一態様に係る半導体装置の特性について、計算機を用いて検証した結果について説明する。具体的には、異なるチャネル長Ｌを有するトランジスタの特性について比較した。なお、計算には、デバイスシミュレーションソフトＡｔｌａｓ（Ｓｉｌｖａｃｏ　Ｄａｔａ　Ｓｙｓｔｅｍｓ社製）を用いた。
【０２０２】
計算に用いたトランジスタの構造を、図１０に示す。図１０（Ａ）は本発明の一態様に係る構造（ソース電極またはドレイン電極の一部を伸長させた構造）であり、図１０（Ｂ）は、比較のための構造（ソース電極またはドレイン電極の一部を伸長させていない構造）である。
【０２０３】
計算に用いたトランジスタの詳細について説明する。図１０（Ａ）に示すトランジスタは、第１の導電層７４２ａ（材質：チタン、厚さ：１００ｎｍ）および第２の導電層７４５ａ（材質：窒化チタン、厚さ：任意）が順に積層されたソース電極と、第１の導電層７４２ｂ（材質：チタン、厚さ：１００ｎｍ）および第２の導電層７４５ｂ（材質：窒化チタン、厚さ：任意）が順に積層されたドレイン電極と、ソース電極上に設けられた絶縁層７４３ａ（材質：酸化シリコン、厚さ：１００ｎｍ）と、ドレイン電極上に設けられた絶縁層７４３ｂ（材質：酸化シリコン、厚さ：１００ｎｍ）と、絶縁層７４３ａおよび絶縁層７４３ｂ上に設けられた酸化物半導体層７４４（材質：Ｉｎ－Ｇａ－Ｚｎ－Ｏ系の酸化物半導体、厚さ：１０ｎｍ）と、酸化物半導体層７４４上に設けられたゲート絶縁層７４６（材質：酸化ハフニウム、厚さ：１０ｎｍ）と、ゲート絶縁層７４６上に設けられたゲート電極７４８（材質：タングステン）を有する。
【０２０４】
図１０（Ａ）に示すトランジスタにおいて、第２の導電層７４５ａは、第１の導電層７４２ａの端面よりチャネル長方向に伸長した領域を有しており（つまり、第２の導電層７４５ａの端部は、第１の導電層７４２ａの端部よりチャネル形成領域に近い。）、第２の導電層７４５ａの端部は、酸化物半導体層７４４のチャネル形成領域と接している。同様に、第２の導電層７４５ｂは、第１の導電層７４２ｂの端面よりチャネル長方向に伸長した領域を有しており（つまり、第２の導電層７４５ｂの端部は、第１の導電層７４２ｂの端部よりチャネル形成領域に近い。）、第２の導電層７４５ｂの端部は、酸化物半導体層７４４のチャネル形成領域と接している。
【０２０５】
図１０（Ｂ）に示すトランジスタは、導電層７５２ａでなるソース電極（材質：窒化チタン、厚さ：１００ｎｍ）および導電層７５２ｂでなるドレイン電極（材質：窒化チタン、厚さ：１００ｎｍ）と、ソース電極およびドレイン電極上に設けられた酸化物半導体層７４４（材質：Ｉｎ－Ｇａ－Ｚｎ－Ｏ系の酸化物半導体、厚さ：１０ｎｍ）と、酸化物半導

体層７４４上に設けられたゲート絶縁層７４６（材質：酸化ハフニウム、厚さ：１０ｎｍ）と、ゲート絶縁層７４６上に設けられたゲート電極７４８（材質：タングステン）を有する。

【０２０６】

図１０（Ａ）と図１０（Ｂ）の相違は、上述の第２の導電層７４５ａにおける、第１の導電層７４２ａの端面よりチャネル長方向に伸長した領域、および、第２の導電層７４５ｂにおける、第１の導電層７４２ｂの端面よりチャネル長方向に伸長した領域の有無、ソース電極上の絶縁層およびドレイン電極上の絶縁層の有無である。

【０２０７】

図１０（Ａ）において、第２の導電層７４５ａにおける、第１の導電層７４２ａの端面よりチャネル長方向に伸長した領域（第２の導電層でなる領域）は、他の領域（第１の導電層と第２の導電層の積層でなる領域）と比較して電極の厚さが小さい。つまり、電荷の流れに垂直な断面の面積が小さくなっている。抵抗は断面積に反比例するから、第２の導電層７４５ａにおける、第１の導電層７４２ａの端面よりチャネル長方向に伸長した領域は、他の領域と比較して抵抗が高いということができる。第２の導電層７４５ｂについても同様のことがいえる。以下、本実施例において、第２の導電層７４５ａにおける、第１の導電層７４２ａの端面よりチャネル長方向に伸長した領域、および、第２の導電層７４５ｂにおける、第１の導電層７４２ｂの端面よりチャネル長方向に伸長した領域を高抵抗領域（ＨＲＲ：Ｈｉｇｈ－Ｒｅｓｉｓｔａｎｃｅ　Ｒｅｇｉｏｎ）と記載する。

【０２０８】

また、図１０（Ａ）において、ソース電極の上部は絶縁層７４３ａに覆われており、ドレイン電極の上部は絶縁層７４３ｂに覆われているため、ソース電極やドレイン電極と、酸化物半導体層７４４の接触面積は非常に小さくなっている（ここでは、第２の導電層の端部のみが接する）。つまり、ソース電極やドレイン電極は、チャネル形成領域と接する領域の近傍において、他の領域よりも高抵抗になっていることになる。

【０２０９】

上述の構成（図１０（Ａ）、および図１０（Ｂ））において、チャネル長Ｌを変更して、トランジスタのしきい値電圧Ｖｔｈがどのような挙動を示すかを調査した。チャネル長Ｌとしては、２０ｎｍ、３０ｎｍ、５０ｎｍ、１００ｎｍ、２００ｎｍ、４００ｎｍの６条件を採用した。

【０２１０】

また、第２の導電層の厚さを変更してしきい値電圧Ｖｔｈの挙動を調査した。第２の導電層の厚さとしては、３ｎｍ、１０ｎｍ、５０ｎｍ、１００ｎｍの４条件を採用した。

【０２１１】

ソース電極とドレイン電極の間の電圧Ｖｄｓは、１Ｖとした。また、高抵抗領域のチャネル長方向の長さは０．３μｍとした。

【０２１２】

計算に用いたパラメータは以下の通りである。

１．Ｉｎ－Ｇａ－Ｚｎ－Ｏ系の酸化物半導体（酸化物半導体層の材料）

バンドギャップＥｇ：３．１５ｅＶ、電子親和力χ：４．３ｅＶ、比誘電率：１５、電子移動度：１０cm^2／Ｖｓ、伝導帯の実効状態密度：$5\times10^{18}cm^{-3}$

２．窒化チタン（ソース電極およびドレイン電極の材料）

仕事関数φ_M：３．９ｅＶ、抵抗率ρ：$2.2\times10^{-4}\Omega\cdot cm$

３．酸化ハフニウム（ゲート絶縁層の材料）

比誘電率：１５

４．タングステン（ゲート電極の材料）

仕事関数φ_M：４．９ｅＶ

【０２１３】

計算結果を図１１に示す。図１１において、横軸はチャネル長Ｌ（ｎｍ）を、縦軸はしきい値電圧のシフト量ΔＶｔｈ（Ｖ）を、それぞれ示している。なお、ΔＶｔｈは、チャネ

ル長Ｌ＝４００ｎｍのしきい値電圧を基準に算出したものである。
【０２１４】
図１１（Ａ）乃至図１１（Ｄ）は図１０（Ａ）に示す構造の計算結果であり、図１１（Ａ）は、第２の導電層の厚さが１００ｎｍ、図１１（Ｂ）は、第２の導電層の厚さが５０ｎｍ、図１１（Ｃ）は、第２の導電層の厚さが１０ｎｍ、図１１（Ｄ）は、第２の導電層の厚さが３ｎｍ、の場合をそれぞれ示している。また、図１１（Ｅ）は図１０（Ｂ）に示す構造の計算結果である。
【０２１５】
図１１（Ａ）～図１１（Ｄ）の比較により、第２の導電層が薄くなるほど、しきい値電圧のマイナスシフトが抑制されるのが分かる。また、図１１（Ａ）と図１１（Ｅ）の比較により、ソース電極やドレイン電極を覆う絶縁層を設ける場合には、Ｖｔｈのマイナスシフトが抑制されるのが分かる。これらはいずれも、ソース電極やドレイン電極と酸化物半導体層の接触面積を縮小し、抵抗を増大させることにより、短チャネル効果を抑制できることを示唆するものである。
【０２１６】
さらに上述の結果より、半導体層と接する領域の近傍において、ソース電極やドレイン電極の抵抗が高くなっていれば、短チャネル効果抑制の効果を得ることができるということもできる。
【０２１７】
以上より、ソース電極またはドレイン電極のチャネル形成領域と接する領域近傍を高抵抗にする（具体的には、例えば、ソース電極またはドレイン電極の一部の断面積を小さくする、ソース電極またはドレイン電極の上部を覆う絶縁層を形成して酸化物半導体層との接触面積を小さくする）ことで、しきい値電圧のマイナスシフトが抑制されることが理解される。これは、ソース電極とドレイン電極の間の電界強度が緩和されることに起因するものである。このように、開示する発明の一態様によって、しきい値電圧低下などの短チャネル効果を抑制できることが示された。
【符号の説明】
【０２１８】
１００　基板
１４２ａ　第１の導電層
１４２ｂ　第１の導電層
１４３　絶縁膜
１４３ａ　絶縁層
１４３ｂ　絶縁層
１４４　酸化物半導体層
１４５　導電膜
１４５ａ　第２の導電層
１４５ｂ　第２の導電層
１４６　ゲート絶縁層
１４８　ゲート電極
１６０　トランジスタ
１７０　トランジスタ
１８０　トランジスタ
１９０　トランジスタ
２００　基板
２４２ａ　第１の導電層
２４２ｂ　第１の導電層
２４３　絶縁膜
２４３ａ　絶縁層
２４３ｂ　絶縁層

２４４　　酸化物半導体層
２４５　　導電膜
２４５ａ　　第２の導電層
２４５ｂ　　第２の導電層
２４６　　ゲート絶縁層
２４８　　ゲート電極
２５２　　絶縁膜
２５２ａ　　サイドウォール絶縁層
２５２ｂ　　サイドウォール絶縁層
２８０　　トランジスタ
３００　　トランジスタ
３１０　　トランジスタ
３２０　　容量素子
４００　　メモリセル
６０１　　筐体
６０２　　筐体
６０３　　表示部
６０４　　キーボード
６１１　　本体
６１２　　スタイラス
６１３　　表示部
６１４　　操作ボタン
６１５　　外部インターフェイス
６２０　　電子書籍
６２１　　筐体
６２３　　筐体
６２５　　表示部
６２７　　表示部
６３１　　電源
６３３　　操作キー
６３５　　スピーカー
６３７　　軸部
６４０　　筐体
６４１　　筐体
６４２　　表示パネル
６４３　　スピーカー
６４４　　マイクロフォン
６４６　　ポインティングデバイス
６４７　　カメラ用レンズ
６４８　　外部接続端子
６４９　　太陽電池セル
６５０　　外部メモリスロット
６６１　　本体
６６３　　接眼部
６６４　　操作スイッチ
６６５　　表示部
６６６　　バッテリー
６６７　　表示部
６７０　　テレビジョン装置
６７１　　筐体

６７３　　　表示部
６７５　　　スタンド
６８０　　　リモコン操作機
７４２ａ　　導電層
７４２ｂ　　導電層
７４３ａ　　絶縁層
７４３ｂ　　絶縁層
７４４　　　酸化物半導体層
７４５ａ　　導電層
７４５ｂ　　導電層
７４６　　　ゲート絶縁層
７４８　　　ゲート電極
７５２ａ　　導電層
７５２ｂ　　導電層

【書類名】特許請求の範囲
【請求項１】
　酸化物半導体層と、
　前記酸化物半導体層と接するソース電極及びドレイン電極と、
　前記酸化物半導体層と重なるゲート電極と、
　前記酸化物半導体層と前記ゲート電極との間に設けられたゲート絶縁層と、を有し、
　前記ソース電極または前記ドレイン電極は、第１の導電層と、前記第１の導電層の端面よりチャネル長方向に伸長した領域を有する第２の導電層と、を含む半導体装置。
【請求項２】
前記第１の導電層および前記第２の導電層はテーパー形状である請求項１に記載の半導体装置。
【請求項３】
前記第２の導電層の前記領域の上にサイドウォール絶縁層を有する請求項１または請求項２に記載の半導体装置。
【請求項４】
　酸化物半導体層と、
　前記酸化物半導体層と接するソース電極及びドレイン電極と、
　前記酸化物半導体層と重なるゲート電極と、
　前記酸化物半導体層と前記ゲート電極との間に設けられたゲート絶縁層と、を有し、
　前記ソース電極及び前記ドレイン電極は、第１の導電層と、前記第１の導電層よりも高抵抗である第２の導電層と、を含み、前記第２の導電層において、前記酸化物半導体層と接する半導体装置。
【請求項５】
前記第２の導電層は、金属の窒化物である請求項１乃至請求項４のいずれか一に記載の半導体装置。
【請求項６】
前記第２の導電層の膜厚は５ｎｍ乃至１５ｎｍである請求項１乃至請求項５のいずれか一に記載の半導体装置。
【請求項７】
　チャネル形成領域を含む酸化物半導体層と、
　前記チャネル形成領域と接するソース電極及びドレイン電極と、
　前記チャネル形成領域と重なるゲート電極と、
　前記酸化物半導体層と前記ゲート電極との間に設けられたゲート絶縁層と、を有し、
　前記ソース電極または前記ドレイン電極において、前記酸化物半導体層の前記チャネル形成領域と接する領域は、その他の領域よりも高抵抗である半導体装置。
【請求項８】
前記ソース電極または前記ドレイン電極は、その端面において前記酸化物半導体層と接し、かつ、前記ソース電極または前記ドレイン電極と、前記酸化物半導体層との間に絶縁層を有する請求項１乃至請求項７のいずれか一に記載の半導体装置。

【書類名】要約書
【要約】
【課題】良好な特性を維持しつつ、微細化を達成した、酸化物半導体を用いた半導体装置を提供することを目的の一とする。
【解決手段】酸化物半導体層と、酸化物半導体層と接するソース電極及びドレイン電極と、酸化物半導体層と重なるゲート電極と、酸化物半導体層とゲート電極との間に設けられたゲート絶縁層と、を有し、ソース電極またはドレイン電極は、第１の導電層と、第１の導電層の端面よりチャネル長方向に伸長した領域を有する第２の導電層と、を含む半導体装置である。
【選択図】図１

【書類名】図面
【図１】

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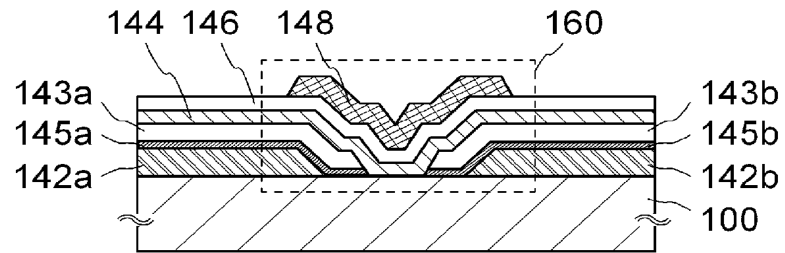

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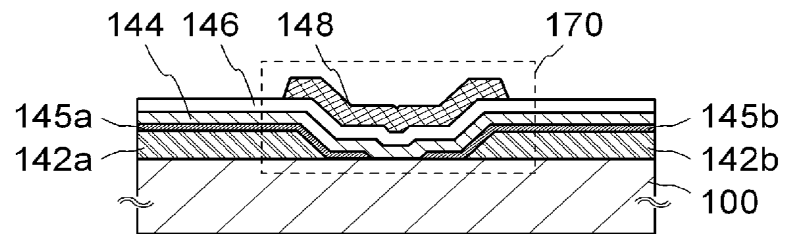

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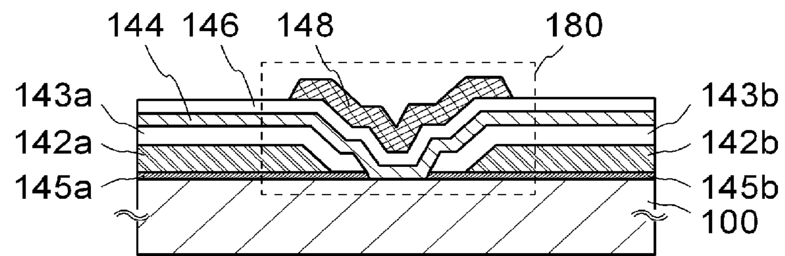

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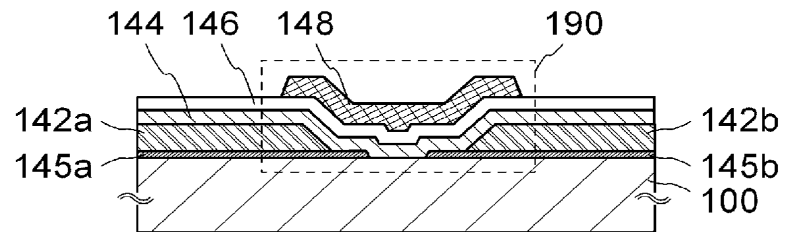

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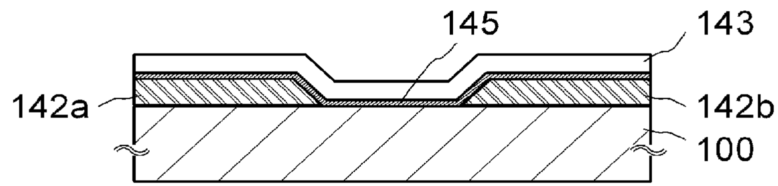

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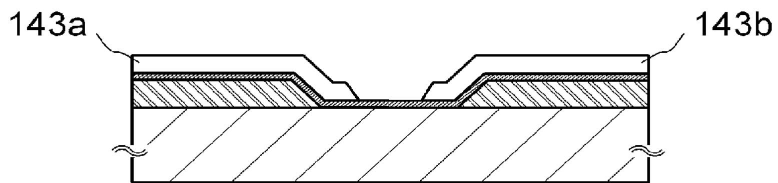

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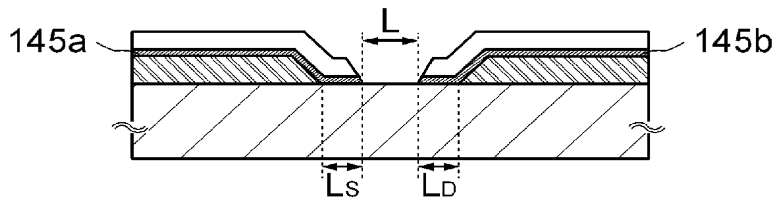

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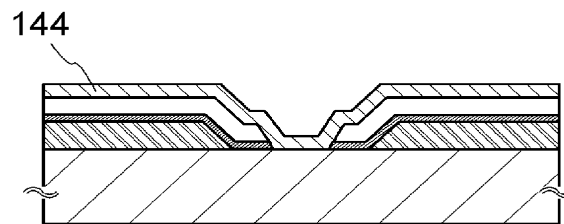

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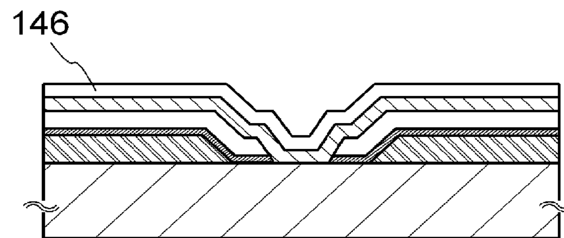

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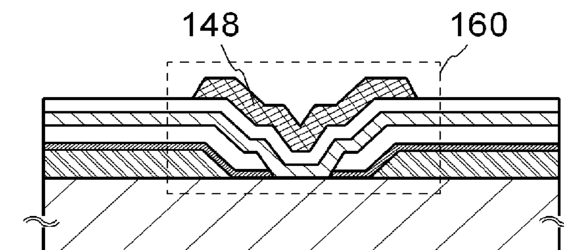

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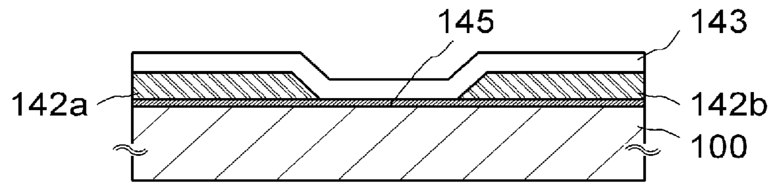

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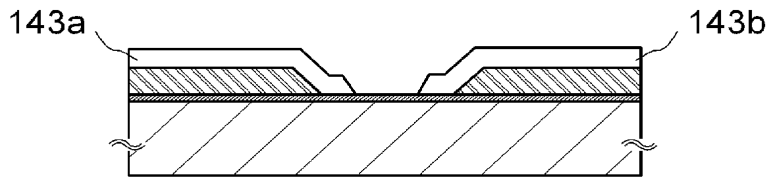

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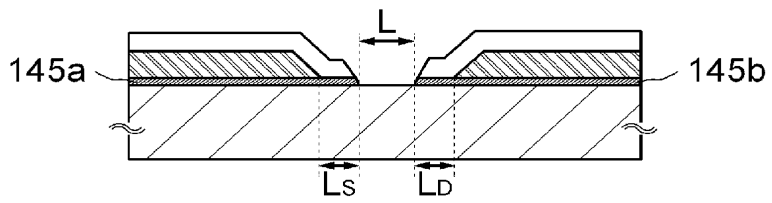

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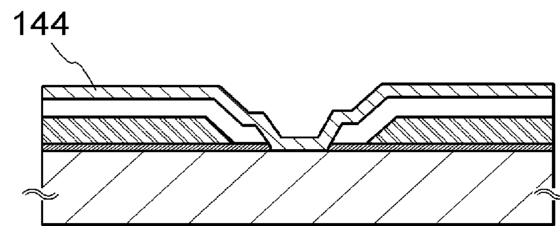

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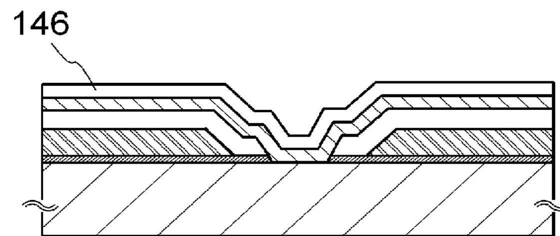

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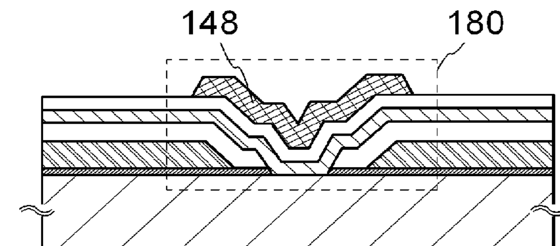

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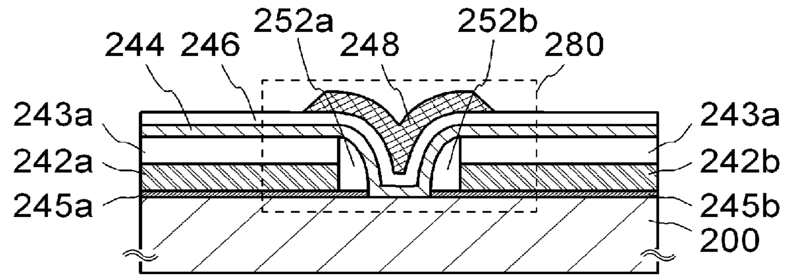

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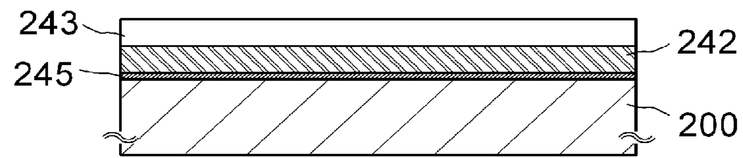

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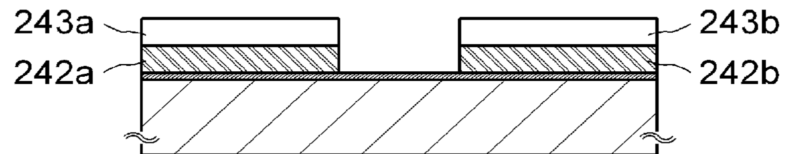

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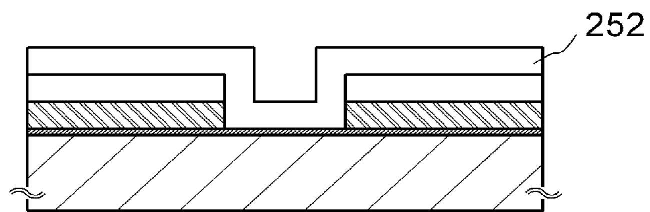

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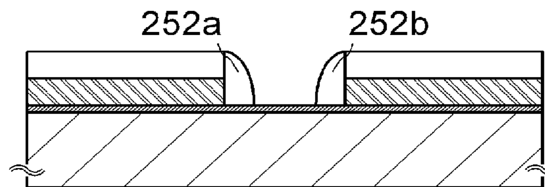

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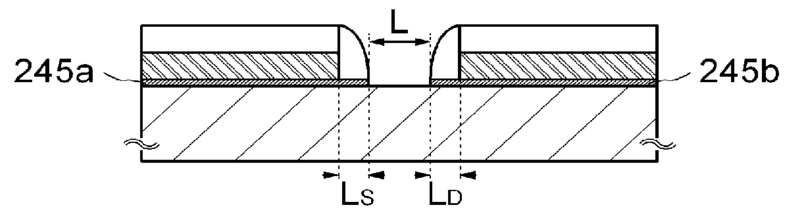

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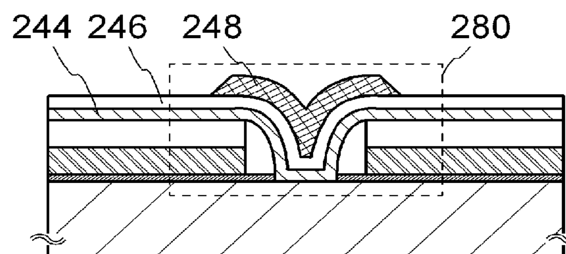

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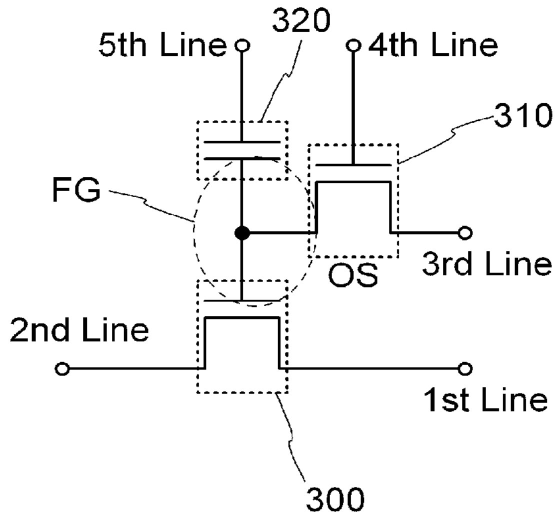

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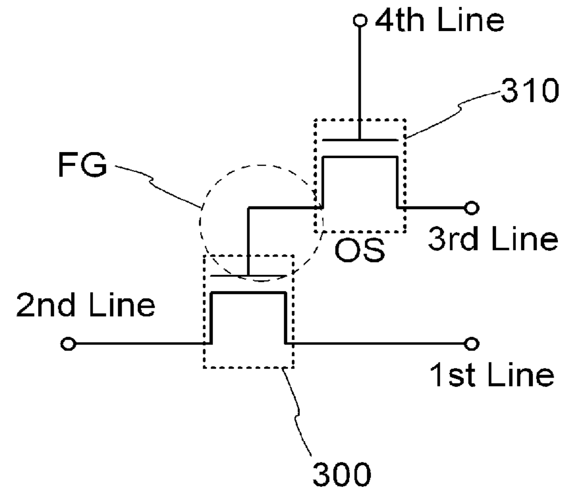

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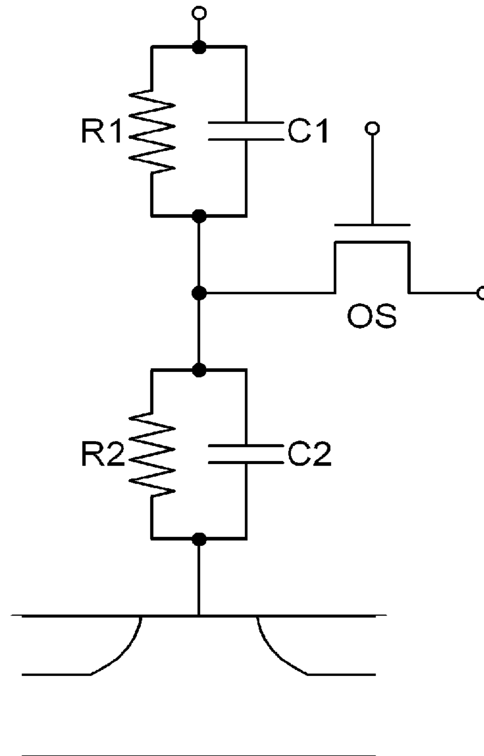

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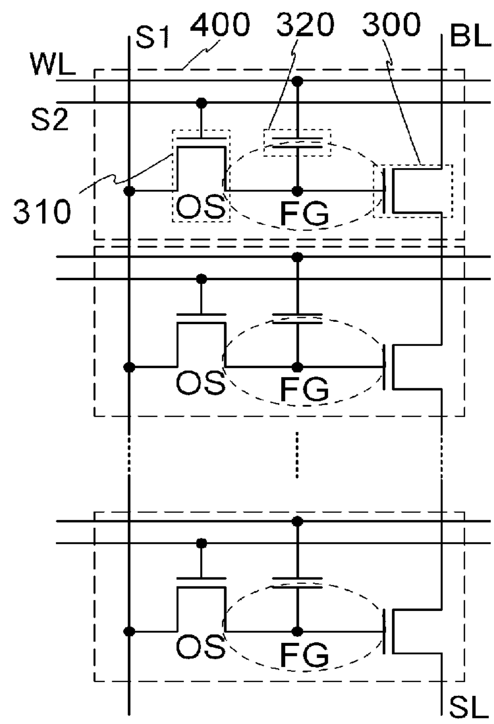

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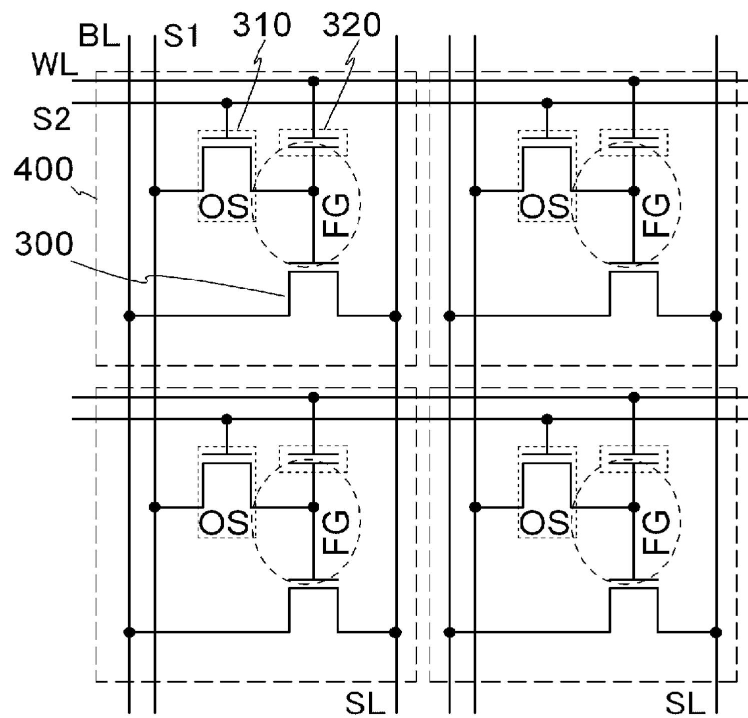

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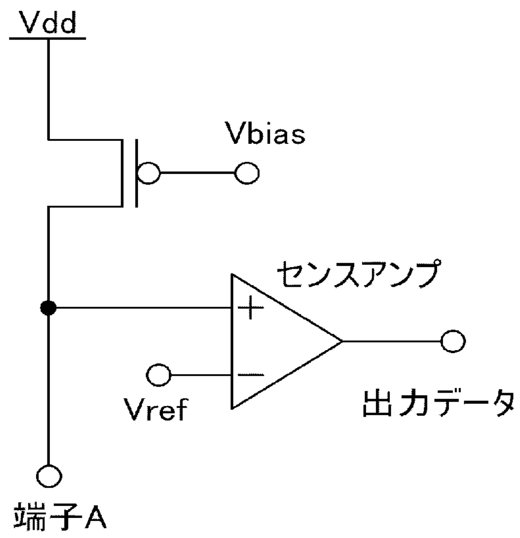

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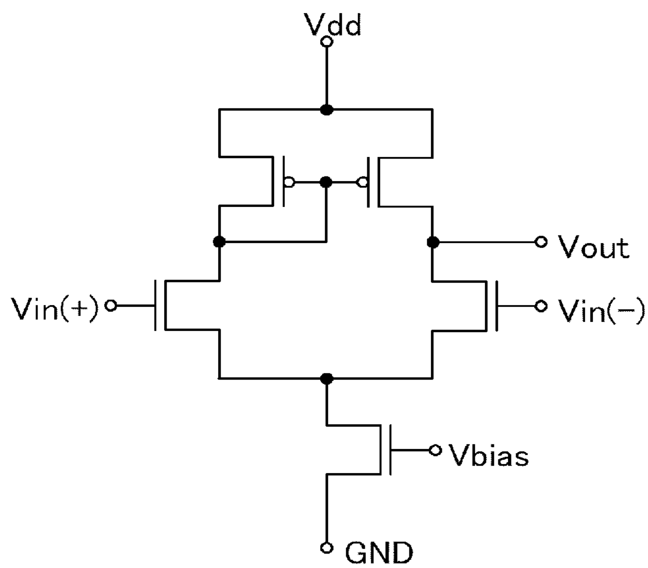

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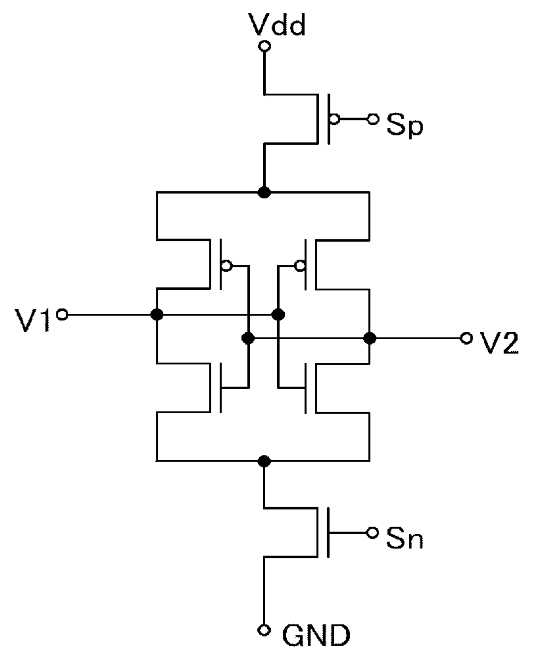

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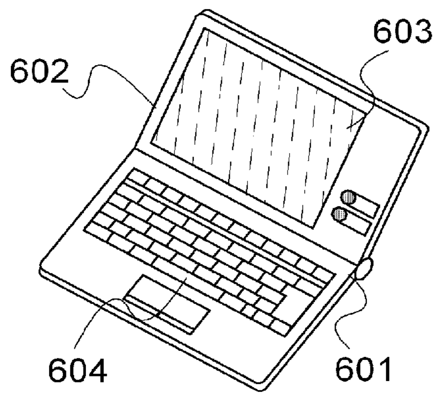

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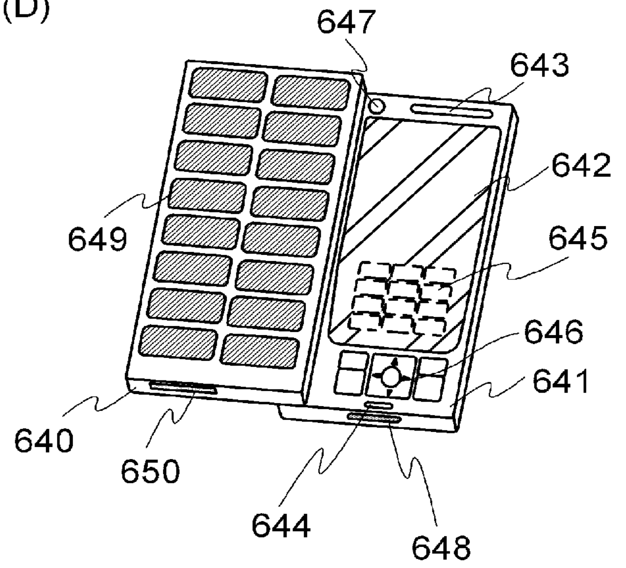

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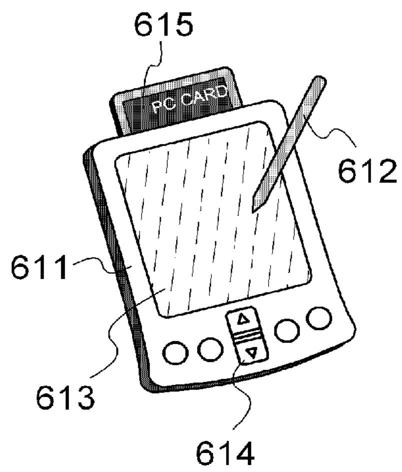

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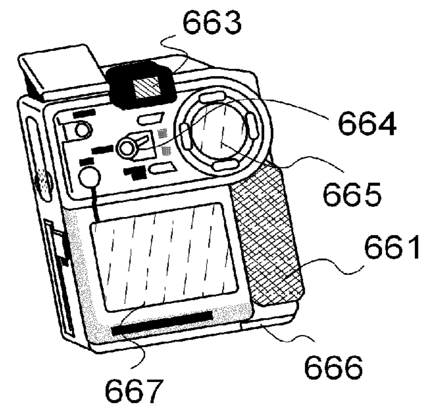

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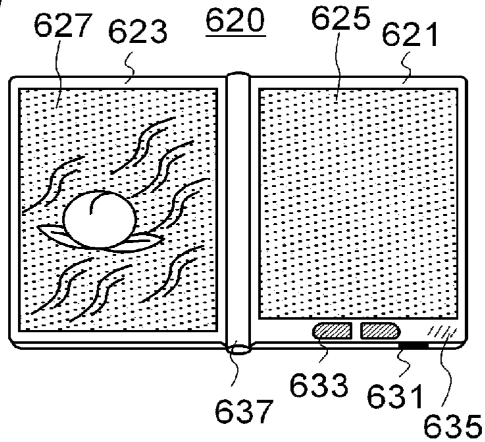

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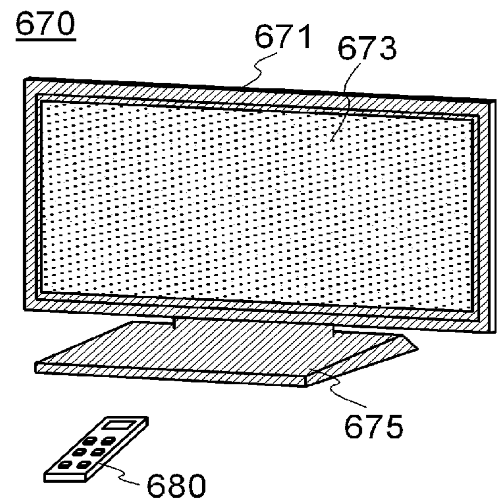

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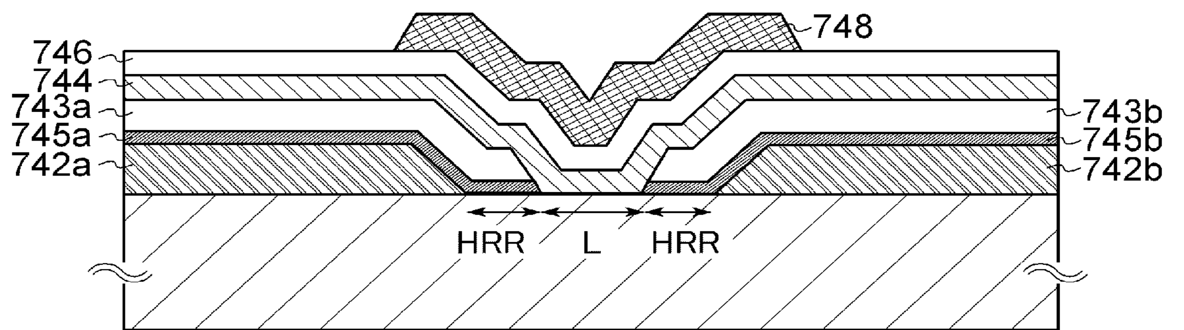

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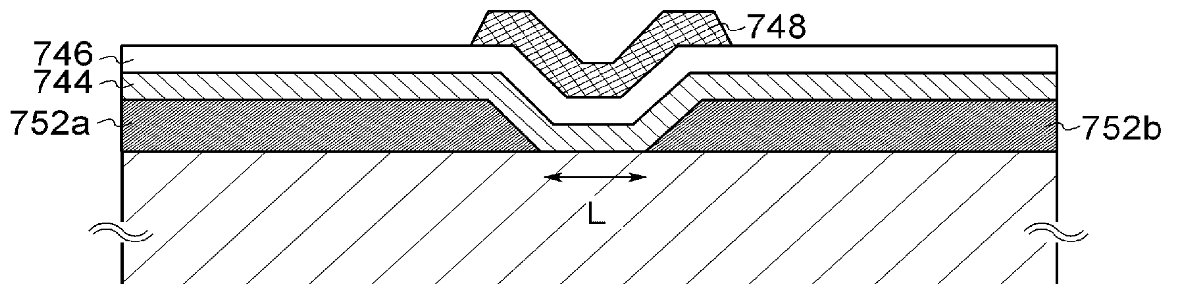

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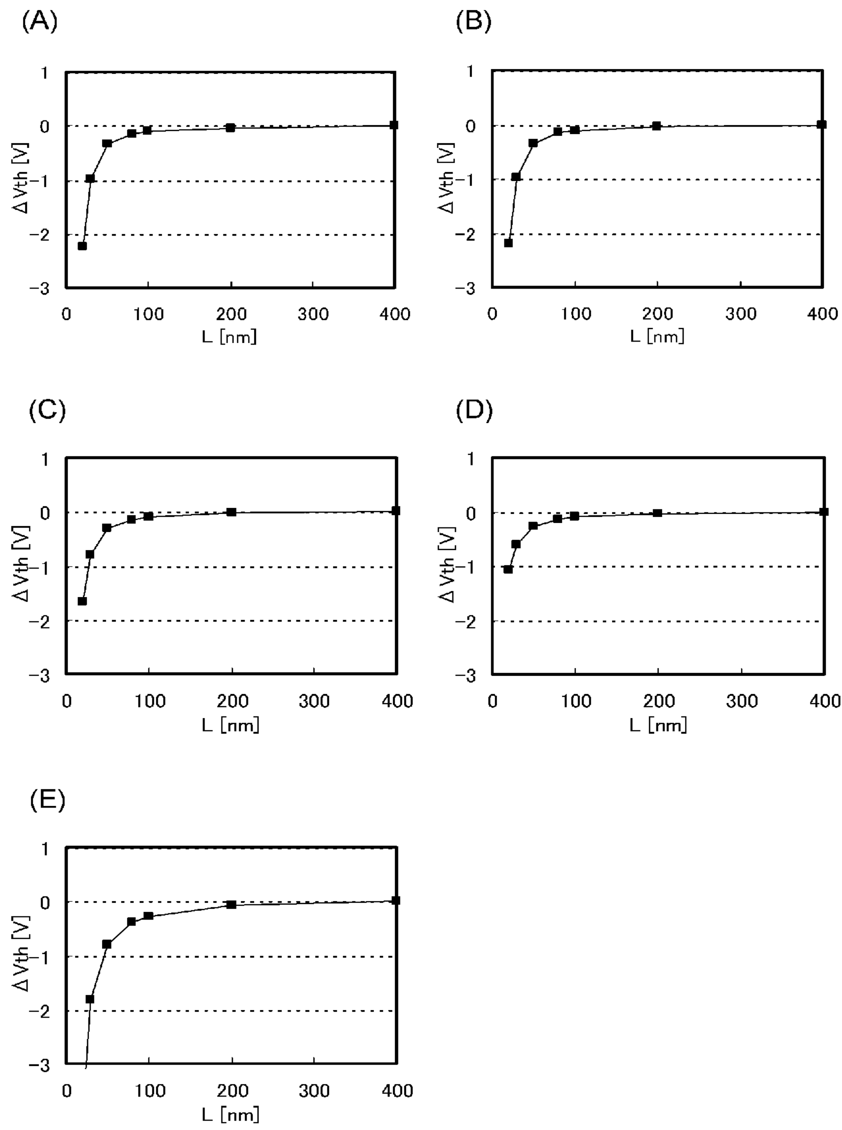

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０００１５３８７８

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
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Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2811
Examiner Name	Unknown
Attorney Docket Number	0756-9138

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Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-2002/0056838	05-16-2002	OGAWA.K	
		US-2003/0189401	10-09-2003	KIDO.J et al.	
		US-2006/0169973	08-03-2006	ISA.T et al.	
		US-2006/0208977	09-21-2006	KIMURA.H	
		US-2006/0238135	10-26-2006	KIMURA.H	
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		US-2006/0170111	08-03-2006	ISA.T et al.	
		US-2007/0054507	03-08-2007	KAJI.N et al.	
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		US-2004/0127038	07-01-2004	CARCIA.P et al.	
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FOREIGN PATENT DOCUMENTS

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		JP-2002-289859A	10-04-2002			Full
		JP-05-251705A	09-28-1993			Full
		JP-2002-076356A	03-15-2002			Full
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Examiner Name	Unknown
Attorney Docket Number	0756-9138

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		US-6294274	09-25-2001	KAWAZOE.H et al.	
		US-2008/0296568	12-04-2008	RYU.M et al.	
		US-7282782	10-16-2007	HOFFMAN.R et al.	
		US-7297977	11-20-2007	HOFFMAN.R et al.	
		US-7462862	12-09-2008	HOFFMAN.R et al.	
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Sheet 3 of 12

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Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2811
Examiner Name	Unknown
Attorney Docket Number	0756-9138

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				Filing Date	January 18, 2011
				First Named Inventor	Shunpei YAMAZAKI et al.
(Use as many sheets as necessary)				Art Unit	2811
				Examiner Name	Unknown
Sheet	4	of	12	Attorney Docket Number	0756-9138

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		KUROKAWA.Y et al., "UHF RFCPUS ON FLEXIBLE AND GLASS SUBSTRATES FOR SECURE RFID SYSTEMS,", JOURNAL OF SOLID-STATE CIRCUITS , 2008, Vol. 43, No. 1, pp. 292-299.	Eng.
		OHARA.H et al., "Amorphous In-Ga-Zn-Oxide TFTs with Suppressed Variation for 4.0 inch QVGA AMOLED Display,", AM-FPD '09 DIGEST OF TECHNICAL PAPERS, July 1, 2009, pp. 227-230, THE JAPAN SOCIETY OF APPLIED PHYSICS.	Eng.
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	13/008,285
				Filing Date	January 18, 2011
				First Named Inventor	Shunpei YAMAZAKI et al.
(Use as many sheets as necessary)				Art Unit	2811
				Examiner Name	Unknown
Sheet	9	of	12	Attorney Docket Number	0756-9138

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		OSADA.T et al., "DEVELOPMENT OF DRIVER-INTEGRATED PANEL USING AMORPHOUS IN-GA-ZN-OXIDE TFT,", AM-FPD '09 DIGEST OF TECHNICAL PAPERS, July 1, 2009, pp. 33-36.	Eng.
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Complete if Known	
Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2811
Examiner Name	Unknown
Attorney Docket Number	0756-9138

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		LANY.S et al., "Dopability, Intrinsic Conductivity, and Nonstoichiometry of Transparent Conducting Oxides,", PHYS. REV. LETT. (PHYSICAL REVIEW LETTERS), January 26, 2007, Vol. 98, pp. 045501-1-045501-4.	Eng.
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Application Number:	13008285
International Application Number:	
Confirmation Number:	8496
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Doris Vasquez Soriano
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36	NPL Documents	NPL_23_FUNG.pdf	475659 3e93a908933ce63c4560e314e1d88dd559e1d319	no	2
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Warnings:					
Information:					
38	NPL Documents	NPL_25_PARK_HIGH.pdf	397716 bc077a90d0c5f093fd79e0e899183139bc8fae60	no	4
Warnings:					
Information:					
		Total Files Size (in bytes):	67611128		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Attorney Docket No. 0756-9138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 8496
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2811
Serial No. 13/008,285	)	
Filed: January 18, 2011	)	
For: SEMICONDUCTOR DEVICE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

U.S. Patent No. 6,563,174 is in the family of JP 2003-086808.

U.S. Publication No. 2006/0244107 is in the family of WO 2004/114391.

This Information Disclosure Statement is being submitted before the issuance of a first Office Action on the merits, therefore, no fee is required.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

Electronic Acknowledgement Receipt

EFS ID:	10193973
Application Number:	13008285
International Application Number:	
Confirmation Number:	8496
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Doris Vasquez Soriano
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-9138
Receipt Date:	31-MAY-2011
Filing Date:	18-JAN-2011
Time Stamp:	14:16:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	NPL Documents	NPL_26_KUROKAWA.pdf	2177235 2967ac1691ad7a3a32132066238c6eef6c654f3b	no	8

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2811
Examiner Name	Unknown
Attorney Docket Number	0756-9138

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-2007/0108446	05-17-2007	AKIMOTO.K	
		US-2007/0187760	08-16-2007	FURUTA.M et al.	
		US-2009/0186437	07-23-2009	AKIMOTO.K	
		US-2009/0186445	07-23-2009	AKIMOTO.K	
		US-2009/0189156	07-30-2009	AKIMOTO.K	
		US-2009/0189155	07-30-2009	AKIMOTO.K	
		US-2007/0278490	12-06-2007	HIRAO.T et al.	
		US-7576394	08-18-2009	FURUTA.M et al.	
		US-2009/0269881	10-29-2009	FURUTA.M et al.	
		US-2010/0003783	01-07-2010	AKIMOTO.K	
		US-2010/0038639	02-18-2010	AKIMOTO.K	
		US-7598520	10-06-2009	HIRAO.T et al.	
		US-2009/0286351	11-19-2009	HIRAO.T et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] -Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		WO-2007/058329	05-24-2007			Eng.
		WO-2007/089048	08-09-2007			Eng.
		WO-2007/142167	12-13-2007			Eng.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known	
Application Number	13/008,285
Filing Date	January 18, 2011
First Named Inventor	Shunpei YAMAZAKI et al.
Art Unit	2811
Examiner Name	Unknown
Attorney Docket Number	0756-9138

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		INTERNATIONAL SEARCH REPORT (Application No.PCT/JP2010/073886) Dated February 15, 2011.	Eng.
		WRITTEN OPINION (Application No.PCT/JP2010/073886) Dated February 15, 2011.	Eng.

Examiner Signature		Date Considered	

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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(10) International Publication Number
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(51) International Patent Classification:
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(71) Applicant *(for all designated States except US)*: SEMICONDUCTOR ENERGY LABORATORY CO., LTD. [JP/JP]; 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: AKIMOTO, Kengo [JP/JP]; c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD., 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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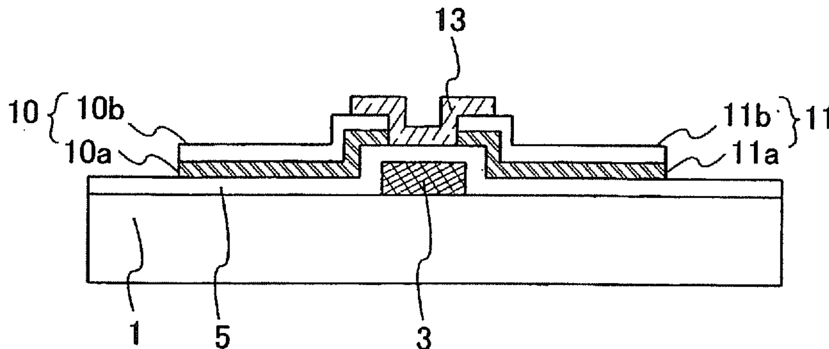
(54) Title: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF



(57) Abstract: To provide a semiconductor device in which a defect or fault is not generated and a manufacturing method thereof even if a ZnO semiconductor film is used and a ZnO film to which an n-type or p-type impurity is added is used for a source electrode and a drain electrode. The semiconductor device includes a gate insulating film formed by using a silicon oxide film or a silicon oxynitride film over a gate electrode, an Al film or an Al alloy film over the gate insulating film, a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film, and a ZnO semiconductor film over the ZnO film to which an n-type or p-type impurity is added and the gate insulating film.

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DESCRIPTION

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

5 TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device using ZnO (Zinc Oxide) and a manufacturing method thereof.

BACKGROUND ART

10 [0002]

A semiconductor device used for a display panel of a liquid crystal display device or an EL (Electroluminescent) display device, for example, a semiconductor portion of a TFT (Thin Film Transistor), is generally formed by using a-Si (amorphous silicon) or poly-Si (polycrystalline silicon).

15 [0003]

Si (silicon) does not have a large band gap (for example, single-crystalline Si is 1.1 eV), and absorbs visible light. By irradiation with the light, electrons and holes (carriers) are formed in Si. If a Si film is used for a channel formation region of a TFT, a carrier is generated in the channel formation region by irradiation with the light even in an OFF state. Then, current 20 flows between a source region and a drain region. The current which flows in an OFF state is called "OFF-leak current". If the current value is high, a display panel does not operate normally. Consequently, a light shielding film is formed so as not to irradiate the Si film with light. However, a process becomes complex when the light shielding film is formed, because a deposition step, a photolithography step, and an etching step are required.

25 [0004]

To solve the problem, an attention is paid to a transparent transistor using zinc oxide (ZnO) which is a semiconductor having a larger band gap of 3.4 eV than that of Si. Concerning such a transparent transistor, the band gap is larger than light energy in a visible light band and the visible light is not absorbed. Consequently, it has an advantage that the OFF-leak current

does not increase if irradiated with light.

[0005]

A semiconductor device using ZnO for the channel formation region is disclosed in Reference 1, for example. The structure of the semiconductor device using ZnO is described referring to FIG. 7A.

[0006]

A semiconductor device in FIG. 7A has a source electrode 1001 and a drain electrode 1002, a ZnO layer 1003 arranged so as to be contacted with the source electrode 1001 and the drain electrode 1002, and a gate insulating layer 1004 stacked over the ZnO layer 1003 and a gate electrode 1005 over an insulating substrate 1000 such as a glass substrate.

[0007]

For the source electrode 1001 and the drain electrode 1002, a conductive ZnO is used. The conductive ZnO is doped with one of the following: B(boron), Al (aluminum), Ga (gallium), In (indium), or Tl (thallium), which are III group elements; F(fluorine), Cl (chlorine), Br (bromine), or I (iodine), which are VII group elements; Li (lithium), Na (sodium), K (potassium), Rb (rubidium), or Cs (caesium), which are I group elements; and N (nitrogen), P (phosphorus), As (arsenic), Sb (antimony), or Bi (bismuth), which are V group elements.

[Reference 1] Japanese Published Patent Application No. 2000-150900

DISCLOSURE OF INVENTION

[0008]

According to the examination by the present inventor, it was revealed that the substrate 1000 is etched in some cases when the source electrode 1001 and the drain electrode 1002 of the top gate semiconductor device shown in FIG. 7A is formed by etching. Even in the case of forming a base film 1006 formed by using a silicon oxide film or a silicon oxynitride film on the substrate 1000, the surface of the substrate 1000 is exposed in some cases when the base film is etched. In addition, in the case of a bottom gate semiconductor device shown in FIG. 7B, it is revealed that a gate insulating film 1004 formed by using a silicon oxide film or a silicon oxynitride film is etched when a source electrode 1001 and a drain electrode 1002 are formed by etching.

[0009]

It the case of the top gate semiconductor device, when the glass substrate 1000 or the base film 1006 formed by using a silicon oxide film or a silicon oxynitride film is etched, an impurity such as sodium is diffused into a semiconductor film 1003 from the substrate 1000, so that characteristics are deteriorated.

5 [0010]

In the case of the bottom gate semiconductor device (FIG. 7B), if the gate insulating film 1004 is etched when the source electrode 1001 and the drain electrode 1002 are formed by etching, the characteristics are not stable and causes a fault.

[0011]

10 In consideration of the above situation, it is an object of the present invention to provide a semiconductor device in which a defect or a fault is not generated and a manufacturing method thereof even if a ZnO semiconductor film is used for the channel formation region, and a ZnO film to which an n-type or p-type impurity is added is used for the source electrode and the drain electrode.

15 [0012]

An aspect of a semiconductor device of this invention has an Al film or an Al alloy film over a silicon oxide film or a silicon oxynitride film, and a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film. "A silicon oxide film", "a silicon oxynitride film", "an Al film", "an Al alloy film" and "a ZnO film" in this specification means a

20 film containing silicon oxide, a film containing silion oxynitride, a film containing Al, a film containing Al alloy, a film containing ZnO, respectively.

[0013]

An aspect of a semiconductor device of this invention has a gate insulating film formed by using a silicon oxide film or a silicon oxynitride film over a gate electrode, an Al film or an Al

25 alloy film over the gate insulating film, a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film, and a ZnO semiconductor film over the ZnO film to which an n-type or p-type impurity is added and the gate insulating film.

[0014]

An aspect of a semiconductor device of this invention has an Al film or an Al alloy film

30 over a silicon oxide film or a silicon oxynitride film, a ZnO film to which an n-type or p-type

impurity is added over the Al film or the Al alloy film, a ZnO semiconductor film over the silicon oxide film or the silicon oxynitride film and the ZnO film to which an n-type or p-type impurity is added, a gate insulating film over the ZnO semiconductor film, and a gate electrode over the gate insulating film.

5 [0015]

An aspect of a manufacturing method of a semiconductor device of this invention has the steps of: forming a silicon oxide film or a silicon oxynitride film; forming an Al film or an Al alloy film over the silicon oxide film or the silicon oxynitride film; forming a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film, wherein the ZnO film 10 to which an n-type or p-type impurity is added is etched to have an island-like shape by a first etching, and the Al film or the Al alloy film is etched to have an island-like shape by a second etching.

[0016]

An aspect of a manufacturing method of a semiconductor device of this invention, 15 wherein a ZnO semiconductor film is formed over the ZnO film to which an n-type or p-type impurity is added, and the silicon oxide film or the silicon oxynitride film after the second etching.

[0017]

In the case of the bottom gate semiconductor device, a gate insulating film formed by 20 using the silicon oxide film or the silicon oxynitride film is formed over the gate electrode after forming a gate electrode.

[0018]

In the case of the top gate semiconductor device, a gate insulating film is formed and a gate electrode is formed after the ZnO semiconductor film is formed.

25 [0019]

A first etching of this invention may be wet etching.

[0020]

A first etching of this invention may be wet etching using buffered fluoric acid.

[0021]

30 A first etching of this invention may be dry etching.

[0022]

A first etching of this invention may be dry etching using CH_4 (methane) gas.

[0023]

A second etching of this invention may be wet etching.

5 [0024]

A second etching of this invention may be wet etching using developing solution for a photoresist.

[0025]

A second etching of this invention may be wet etching using an organic alkaline

10 solution.

[0026]

A second etching of this invention may be wet etching using TMAH (tetramethylammonium hydroxide).

[0027]

15 An aspect of a semiconductor device of this invention has a gate electrode, a gate insulating film over the gate electrode, a first film comprising metal material over the gate insulating film, a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the first film, and a third film comprising the transparent semiconductor material over the second film and the gate insulating film.

20 [0028]

An aspect of a semiconductor device of this invention has an insulating film over a substrate, a first film comprising a metal material over the insulating film, a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the metal film, a third film comprising the transparent semiconductor material over the insulating film and

25 the second film, a gate insulating film over the third film, and a gate electrode over the gate insulating film.

[0029]

An aspect of a manufacturing method of a semiconductor device of this invention has the steps of: forming an insulating film over a substrate, forming a first film comprising a metal

30 material over the insulating film, forming a second film comprising a transparent semiconductor

material and an n-type or p-type impurity over the first film, etching the second film, and etching the first film.

[0030]

An aspect of a manufacturing method of a semiconductor device of this invention has the steps of: forming a gate electrode over a substrate, forming a gate insulating film over the gate electrode, forming a first film comprising a metal material over the gate insulating film, forming a second film comprising a transparent semiconductor material and an n-type or p-type impurity over second film, etching the second film, and etching the first film.

[0031]

In the top gate semiconductor device, a base film formed by using a glass substrate, a silicon oxide film or a silicon oxynitride film is not etched, and an impurity such as sodium is not diffused from a substrate into a semiconductor film so that its characteristics are not deteriorated.

[0032]

In the bottom gate semiconductor device, the gate insulating film is not etched and its characteristics do not become unstable.

[0033]

Since Al is used for a part of the source electrode and drain electrode, low resistance of a wire can be obtained.

BRIEF DESCRIPTION OF DRAWINGS

[0034]

In the accompanying drawings:

FIGS. 1A and 1B show semiconductor devices of this invention;

FIGS. 2A to 2D show manufacturing steps of a semiconductor device of this invention;

FIGS. 3A to 3D show manufacturing steps of a semiconductor device of this invention;

FIGS. 4A and 4B show manufacturing steps of a semiconductor device of this invention;

FIGS. 5A to 5D show manufacturing steps of a semiconductor device of this invention;

FIGS. 6A to 6C show manufacturing steps of a semiconductor device of this invention;

FIGS. 7A and 7B show conventional examples;

FIGS. 8A and 8B show a manufacturing step of a liquid crystal display device;

FIGS. 9A and 9B show manufacturing steps of a liquid crystal display device;

FIGS. 10A and 10B show manufacturing steps of a light-emitting device;

FIGS. 11A and 11B show manufacturing steps of a light-emitting device;

5 FIGS. 12A to 12F each show an equivalent circuit of a light-emitting device;

FIG. 13 shows an equivalent circuit of a light-emitting device;

FIG. 14A illustrates a top front view of a pixel portion and FIG. 14B illustrates an equivalent circuit of a light-emitting device;

FIGS. 15A to 15E each show an example of an electronic apparatus to which this

10 invention is applied; and

FIG. 16 shows an example of electronic apparatuses to which this invention is applied.

[0035]

The embodiments of this invention will be described hereinafter referring to the

15 accompanying drawings. Note that this invention is not limited to the description below, and it is easily understood by those skilled in the art that the embodiments and details herein disclosed can be modified in various ways without departing from the purpose and the scope of the invention. Therefore, this invention should not be interpreted as being limited to the description of the embodiments to be given below.

20

BEST MODE FOR CARRYING OUT THE INVENTION

[0036]

[Embodiment 1]

Here, a bottom gate semiconductor device is described.

25 [0037]

FIG. 1A is a cross-sectional view in which one example of the embodiment of this invention is shown. In FIG. 1A, numeral reference 1 denotes a substrate, 3 denotes a gate electrode, 5 denotes a gate insulating film, 10 denotes a source electrode, 10a denotes a first conductive film, 10b denotes a second conductive film, 11 denotes a drain electrode, 11a denotes

30 a first conductive film, 11b denotes a second conductive film, and 13 denotes a semiconductor

film. An insulating film for passivation or planarization may be formed over the semiconductor film 13.

[0038]

The gate electrode 3 is formed over the substrate 1, the gate insulating film 5 is formed over the gate electrode 3, and the source electrode 10 and the drain electrode 11 are formed over the gate insulating film 5. The source electrode 10 is formed of a layered film having the first conductive film 10a and the second conductive film 10b, and the drain electrode 11 is formed of a layered film having the first conductive film 11a and the second conductive film 11b. A third conductive film may be formed between the first conductive film 10a and the second conductive film 10b, or between the first conductive film 11a and the second conductive film 11b. The source electrode 10 and the drain electrode 11 may be each formed so as to overlap partially with the gate electrode 3 through the gate insulating film 5. The semiconductor film 13 is formed over the source electrode 10 and the drain electrode 11 over the gate insulating film 5.

[0039]

Hereinafter, each structure is described.

(1) substrate

The following can be used for forming a substrate: a substrate formed by using a glass substrate; an insulating material such as alumina; and a plastic substrate which can resist a processing temperature in post-steps; and the like. In the case of using a plastic substrate for the substrate 1, the following can be used: PC (polycarbonate); PES (polyethersulfone); PET (polyethylene terephthalate); PEN (polyethylene naphthalate); or the like. In the case of the plastic substrate, an inorganic layer or an organic layer may be provided as a gas barrier layer over the surface. In the case where a prominence due to dust or the like which is generated on the substrate in the manufacturing process of the plastic substrate, the substrate may be used after polishing it with CMP or the like to make its surface planarized. An insulating film such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y) ($X>Y$), and silicon nitride oxide (SiN_xO_y) ($X>Y$) may be formed over the substrate 1 for preventing an impurity or the like from diffusing from the substrate side.

[0040]

(2) gate electrode

A gate electrode can be formed by using an Al (aluminum) film, a W (tungsten) film, a Mo (molybdenum) film, a Ta (tantalum) film, a Cu (copper) film, a Ti (titanium) film, an alloy material containing the elements as a main component (for example, an Al alloy film, a MoW (molybdenum tungsten) alloy film), or the like. A semiconductor film represented by a polycrystalline silicon film doped with an impurity element such as P (phosphourus) may be used. The gate electrode 3 may be a single layer or a layered film in which two or more layers are stacked.

[0041]

(3) gate insulating film

The gate insulating film 5 is formed by using an insulating film containing silicon as a main component, for example, silicon oxide film, and silicon oxynitride film. In addition, it may be a single layer or a layered film.

[0042]

(4) source electrode and drain electrode

The source electrode 10 is formed with a layered film of the first conductive film 10a and the second conductive film 10b, and the drain electrode 11 is formed with a layered film of the first conductive film 11a and the second conductive film 11b.

[0043]

As the first conductive film, an Al film, an Al alloy film such as an AlNi (aluminum nickel) film, and an AlNd (neodymium aluminum) film can be used. As the second conductive film, ZnO (zinc oxide) to which a p-type or n-type impurity of B (boron), Al (aluminum), Ga (gallium), P (phosphorus), or As (arsenic) is added can be used. A metal film such as a Ti film may be provided as a third conductive film between the first conductive film and the second conductive film.

[0044]

(5) semiconductor film

A ZnO film is used as a semiconductor film. Since the source electrode and the drain electrode contacted with the semiconductor film have the ZnO film to which a p-type or n-type impurity is added, they can be easily connected with the semiconductor film.

[0045]

(6) insulating film

An insulating film such as a passivation film and a planarization film may be formed over the semiconductor film 13, although not shown. Silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy) (x>y), silicon nitride oxide (SiNxOy) (x>y), a SOG
5 (spin-on-glass) film, or an organic resin film of acryl, or a layered film of those can be used.

[0046]

In the bottom gate semiconductor device, a gate insulating film is not etched in manufacturing process, and characteristics do not become unstable. Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

10 [0047]

[Embodiment 2]

Here, a top gate semiconductor device is described.

[0048]

FIG. 1B is a cross-sectional view showing one example of an embodiment of this
15 invention. In FIG. 1B, numeral reference 1 denotes a substrate, 20 denotes an insulating film, 25 denotes a source electrode, 25a denotes a first conductive film, 25b denotes a second conductive film, 26 denotes a drain electrode, 26a denotes a first conductive film, 26b denotes a second conductive film, 27 denotes a semiconductor film, 28 denotes a gate insulating film, and 29 denotes a gate electrode. An insulating film for passivation or planarization may be formed
20 over the gate electrode.

[0049]

The insulating film 20 is formed on the substrate 1, and the source electrode 25 and the drain electrode 26 are formed over the insulating film 20. The source electrode 25 is formed with a layered film of the first conductive film 25a and the second conductive film 25b, and the
25 drain electrode 26 is formed with a layered film of the first conductive film 26a and the second conductive film 26b. A third conductive film may be formed between the first conductive film 25a and the second conductive film 25b, or between the first conductive film 26a and the second conductive film 26b. The semiconductor film 27 is formed over the source electrode 25 and the drain electrode 26 over the insulating film 20, the gate insulating film 28 is formed over the
30 semiconductor film 27, and the gate electrode 29 is formed over the gate insulating film 28.

The gate electrode 29 may be formed so as to partially overlap with the source electrode and the drain electrode with the gate insulating film 28 and the semiconductor film 27 interposed therebetween.

[0050]

5 Here, each structure is described.

[0051]

For the substrate, the source electrode, the drain electrode, the semiconductor film, and the gate electrode, the same ones described in Embodiment 1 can be used.

(1) insulating film over substrate

10 An silicon oxide film or a silicon oxynitride film is formed as the insulating film 20 for preventing an impurity or the like from diffusing from the substrate side over the substrate 1. In addition, it may be a single layer or a layered film.

[0052]

(2) gate insulating film

15 The gate insulating film 28 is formed by using an insulating film containing silicon as a main component, for example, a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, and a silicon nitride film. In addition, it may be a single layer or a layered film.

[0053]

(3) insulating film over gate electrode

20 An interlayer insulating film such as a passivation film and a planarization film may be formed over the gate electrode 29, although not shown. A SiO_x film, a SiNx film, a SiON film, SiNO film, an SOG (spin-on-glass) film, and an organic resin film of acrylic or a layered film of those can be used.

[0054]

25 In the top gate semiconductor device, the substrate or the base film formed by using a silicon oxide film or a silicon oxynitride film is not etched, so that an impurity such as sodium is not diffused into the semiconductor film from the substrate and the characteristics are not deteriorated. Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

30 [0055]

[Embodiment 3]

A manufacturing method of the bottom gate semiconductor device is described, in which a silicon oxide film or a silicon oxynitride film is formed as a gate insulating film over the gate electrode, an Al film or an Al alloy film is formed as a first conductive film, and a ZnO film to which an n-type or p-type impurity is added is formed as a second conductive film, and then, the second conductive film is etched to have an island-like shape by a first etching and the first conductive film is etched to have an island-like shape by a second etching to form source and drain electrodes, and a ZnO semiconductor film is formed.

[0056]

As shown in FIG. 2A, a gate electrode 3 is formed. The thickness of the gate electrode may be 10 to 200 nm over a substrate 1. The substrate 1 may be formed by using the material shown in Embodiment 1. Here, a glass substrate is used.

[0057]

An insulating film 2 containing silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy) (x>y), silicon nitride oxide (SiNxOy) (x>y), or the like may be formed with a thickness of 10 to 200 nm by CVD or sputtering so as to prevent impurity or the like from diffusing from the substrate side (FIG. 2B).

[0058]

The insulating film 2 may be formed by processing the surface of the substrate 1 with high density plasma. For example, the high density plasma can be generated using a microwave of 2.45 GHz, and it is only required that electron density ranges from 1×10^{11} to $1\times10^{13}/cm^3$, and electron temperature is 2 eV or less. Such high density plasma has a low kinetic energy of active species and a film with fewer defects can be formed with less damage caused by plasma compared to a conventional plasma treatment.

[0059]

The surface of the substrate 1 can be nitrided by the high density plasma treatment under a nitriding atmosphere such as an atmosphere containing nitrogen and a noble gas, an atmosphere containing nitrogen, hydrogen and a noble gas, and an atmosphere containing ammonia and a noble gas. In the case where a glass substrate is used as the substrate 1 subjected to a nitriding treatment by the high density plasma, as a nitride film formed over the

surface of the substrate 1, the insulating film 2 containing silicon nitride as a main component can be formed. The insulating film 2 may be formed by using a plurality of layers in which a silicon oxide film or a silicon oxynitride film is formed by plasma CVD over the nitride film.

[0060]

5 In addition, a nitride film can be formed by nitriding over the surface of the insulating film 2 with high density plasma similarly.

[0061]

The nitride film formed by nitriding with high density plasma can suppress diffusion of impurity from the substrate 1.

10 [0062]

The gate electrode 3 can be formed by using materials shown in Embodiment 1. Here, an AlNd (aluminum neodymium) film is formed by sputtering using an AlNd target and processed into an island-like shape. A photolithography method is used for processing the film into an island-like shape, and dry etching or wet etching is used.

15 [0063]

After cleaning the surface of the gate electrode 3 and the surface of the substrate 1 or the insulating film 2, a gate insulating film 5 is formed with a thickness of 10 to 200 nm using a known CVD or sputtering over the gate electrode 3 (FIG. 2A and 2B). The surface cleaning step and the formation step of the gate insulating film 5 may be carried out continuously without

20 being exposed to air. In the case where an Al film is used for the gate electrode 3, when the gate insulating film 5 is formed at a high temperature, a hillock is generated in some cases. Thus, it is preferable to form the film at a low temperature of 500°C or less, preferably 350 °C or less.

[0064]

25 The gate insulating film 5 can be formed by using the material shown in Embodiment 1. Here, a silicon oxide film is formed. Note that the insulating film 2 is omitted in the drawings below.

[0065]

A first conductive film 6 for source and drain electrodes is formed with a thickness of

30 10 to 200 nm on the gate insulating film 5. The first conductive film 6 can be formed by using

the material shown in Embodiment 1. Here, an AlNi (aluminum nickel) film or an AlNd film is used. The first conductive film 6 can be formed by sputtering using an AlNi target or an AlNd target. After forming the gate insulating film 5, the first conductive film 6 may be formed continuously without being exposed to the air.

5 [0066]

A second conductive film 7 is formed with a thickness of 10 to 200 nm on the first conductive film 6 (FIG. 2C). The second conductive film 7 can be formed by using the material shown in Embodiment 1. Here, ZnO (zinc oxide) to which an impurity such as Al or Ga is added is used. Consequently, an ohmic contact can be easily created between the second

10 conductive film 7 and a ZnO film which is formed as a semiconductor layer later. The second conductive film 7 can be formed by sputtering. For example, the following methods can be used for adding Al or Ga: sputtering using a ZnO target to which 1 to 10 weight % of Al or Ga is added; or sputtering in which an Al or Ga chip is mounted on a ZnO target at 200 to 300°C.

[0067]

15 After forming the first conductive film 6, the second conductive film 7 may be formed continuously without being exposed to the air. Therefore, formation from the gate insulating film 5 to the second conductive film 7 may be continuously carried out without being exposed to air.

[0068]

20 A third conductive film 8 may be formed with a thickness of 10 to 200 nm between the first conductive film 6 and the second conductive film 7 (FIG. 2D). A contact resistance is occasionally increased between the first conductive film 6 and the second conductive film 7 depending on a heat treatment temperature in a manufacturing process. However, the contact resistance can be reduced between the first conductive film 6 and the second conductive film 7

25 by forming the third conductive film 8. The third conductive film 8 can be formed by using a metal film such as a Ti film which is formed by sputtering or the like.

[0069]

A resist mask 9 is formed over the second conductive film 7, and the second conductive film 7 is etched (FIGS. 3A and 3B). In the case of using wet etching, buffered fluoric acid (in

30 which HF (hydrofluoric acid) and NH_4F (ammonium fluoride) are mixed), for example, solution

with a ratio of HF:NH_4F (weight ratio)=1: 100 to 1: 10 is used.

[0070]

In the case of using dry etching, anisotropic plasma etching using CH_4 gas can be used.

[0071]

5 Under the second conductive film 7, the first conductive film 6 is formed. Thus, the first conductive film 6 serves as an etching stopper when the second conductive film 7 is etched. Consequently, source and drain electrodes can be formed without damaging the gate insulating film 5 in etching.

[0072]

10 A part of the first conductive film 6 may be etched when the second conductive film 7 is etched. However, attention is required to be paid so as not to totally etch the first conductive film 6 because the gate insulating film is damaged if the first conductive film 6 is totally etched.

[0073]

Next, a source electrode 10 and a drain electrode 11 are formed by etching the first 15 conductive film 6 using the resist mask 9 (FIG. 3C). In this invention, the first conductive film 6 is etched using an organic alkaline solution represented by TMAH (tetramethylammonium hydroxide), which is a developer for a photoresist.

[0074]

In the case of using an AlNi film for the first conductive film 6 and TMAH for etching 20 solution, the etching ratio is approximately 300 nm/min at 30°C. On the other hand, the second conductive film 7 or the gate insulating film 5 to which the above-mentioned material is used is not etched with TMAH. Consequently, the source electrode 10 and the drain electrode 11 can be formed without damaging the gate insulating film 5. Further, the island-like shaped second conductive films 10b and 11b are not reduced in size. In this invention, the first conductive 25 film 6 can be etched using a developer which is used when a resist mask is formed without using a special etching solution. Consequently, cost is reduced and efficiency is increased.

[0075]

The resist mask 9 is removed after forming the source electrode 10 and the drain electrode 11.

30 [0076]

A ZnO film is formed as a semiconductor film 12 with a thickness of 20 to 200 nm by sputtering over the source electrode 10, the drain electrode 11, and the gate insulating film 5 (FIG. 3D). For example, the film can be formed by sputtering using a ZnO target with a flow ratio of oxygen/argon ranging from 30 to 20, at 200 to 300°C.

5 [0077]

The semiconductor film 12 is etched by a photolithography method to form an island-like shaped semiconductor film 13 (FIG. 4A). A wet etching method using a buffered fluoric acid or anisotropic dry etching method using CH_4 gas can be used.

[0078]

10 Zno is commonly used in the semiconductor film 12 and the second conductive films 10b and 11b, and it is difficult to obtain a sufficient etching selectivity. However, since the second conductive film 7 is required to be formed in a portion in contact with the semiconductor film 12, the second conductive film 7 may be etched in a portion out of contact with the semiconductor film 12, for example, a wire portion. In the above-mentioned etching method, 15 the second conductive films 10b and 11b may be etched, but the first conductive films 10a and 11a are not etched. Consequently, the first conductive films 10a and 11a serve as wires, and the electrical connection with the semiconductor device is ensured.

[0079]

An insulating film 14 is formed with a thickness of 50 nm to 1 μm over a semiconductor 20 film 13 by CVD or sputtering (FIG. 4B). An insulating film containing silicon as a main component can be formed as the insulating film 14. An organic resin film or the like may be stacked over the insulating film containing silicon. The insulating film 14 functions as a planarization film or a passivation film. Since Al is included in the source electrode 10 and the drain electrode 11, a hillock is occasionally generated when the insulating film 14 is formed at 25 high temperature. Thus, it is preferably formed at low temperature, 500°C or less, preferably 350°C or less.

[0080]

Contact holes are formed in the insulating film 14, and conductive films in contact with the gate electrode 3, the source electrode 10, and the drain electrode 11 are provided if necessary.

30 [0081]

According to this invention, a semiconductor device can be formed without damaging the gate insulating film. An Al alloy film such as an AlNi film is used as the first conductive film, thereby achieving lower resistance of the wire.

[0082]

5 [Embodiment 4]

Here, a manufacturing method of a top gate semiconductor device is described, in which an Al film or an Al alloy film is formed as a first conductive film on a silicon oxide film or a silicon oxynitride film, and a ZnO film to which an n-type or p-type impurity is added is formed as a second conductive film, and then, the second conductive film is formed to have an

10 island-like shape by a first etching, the first conductive film is formed to have an island-like shape by a second etching to form source and drain electrodes, a ZnO semiconductor film is formed, a gate insulating film is formed, and a gate electrode is formed. Note that it is needless to say that materials and methods for manufacture described in Embodiments 1 to 3 can be applied to those used for the present embodiment.

15 [0083]

As shown in FIG. 5A, a silicon oxide (SiOx) film is formed as an insulating film 20 over a substrate 1 with a thickness of 10 to 200 nm by CVD or sputtering. The insulating film 20 prevents impurity or the like from diffusing from the substrate 1 side.

[0084]

20 A first conductive film 21 for the source and drain electrodes is formed with a thickness of 10 to 200 nm by sputtering or evaporation over the insulating film 20. An Al alloy film such as AlNi (aluminum nickel) film which is shown in Embodiment 1 can be used as the first conductive film 21. After forming the insulating film 20, the first conductive film 21 may be formed continuously without being exposed to the air.

25 [0085]

A second conductive film 22 is formed with a thickness of 10 to 200 nm by sputtering on the first conductive film 21 (FIG. 5A). As the second conductive film 22, ZnO (zinc oxide) to which a p-type or n-type impurity such as B (boron), Al (aluminum), Ga (gallium), P (phosphourus), or As (arsenic) is added can be used. After forming the first conductive film 21,

30 the second conductive film 22 may be formed continuously without being exposed to the air.

Therefore, the steps of forming the insulating film 20 to the second conductive film 22 may be carried out continuously without being exposed to the air.

[0086]

A metal film such as a Ti film may be formed as a third conductive film 23 with a thickness of 10 to 200 nm by sputtering between the first conductive film 21 and the second conductive film 22 in order to reduce the contact resistance between the first conductive film 21 and the second conductive film 22 (FIG. 5B).

[0087]

A resist mask 24 is formed over the second conductive film 22, and the second conductive film 22 is etched (FIG. 5C). Wet etching using buffered fluoric acid or dry etching using CH_4 gas can be used as an etching method.

[0088]

The first conductive film 21 is formed under the second conductive film 22. Therefore, the first conductive film 21 serves as an etching stopper when the second conductive film 22 is etched. Thus, the source and drain electrodes can be formed without exposing the substrate 1 by etching the insulating film 20.

[0089]

When the second conductive film 22 is etched, a part of the first conductive film 21 may be etched. Note that if all of the first conductive film 21 is etched, the insulating film 20 is etched and the substrate 1 is exposed, which would cause diffusion of impurity included in the substrate 1.

[0090]

The first conductive film 21 is etched to form the source electrode 25 and the drain electrode 26 (FIG. 5D). Wet etching using a developer for a photoresist, TMAH is used as an etching method. Thus, the source electrode 25 and the drain electrode 26 can be formed without etching the insulating film 20. Further, the sizes of the island-like shaped second conductive films 25b and 26b are not reduced because the ZnO film is not etched by TMAH. Etching can be performed with a developer which is used in formation of a resist mask without a special etching solution for the first conductive film 21, which leads to cost reduction and improvement in efficiency.

[0091]

After forming the source electrode 25 and the drain electrode 26, the resist mask 24 is removed.

[0092]

5 A ZnO film is formed with a thickness of 20 to 200 nm by sputtering as the semiconductor film 27 over the source electrode 25, the drain electrode 26, and the insulating film 20 (FIG. 6A).

[0093]

The semiconductor film 27 is etched by a photolithography method to make an 10 island-like shaped semiconductor film 27. Wet etching using buffered fluoric acid or dry etching using CH_4 gas can be used as an etching method.

[0094]

ZnO is commonly used for the semiconductor film 27 and the second conductive films 25b and 26b, and it is difficult to obtain a high etching selectivity. However, the second 15 conductive film may be etched in the portion out of contact with the semiconductor film 27, specially the wire portion, because the second conductive film 22 may be formed in the source and drain electrode portions, which is the same as Embodiment 3.

[0095]

A gate insulating film 28 is formed with a thickness of 10 to 200 nm by CVD or 20 sputtering over the semiconductor film 27 (FIG. 6B). The semiconductor film 27 may be subjected to a high density plasma treatment shown in the above-mentioned Embodiment to form a gate insulating film. The surface of the semiconductor film 27 can be nitrided by the high density plasma treatment under a nitriding atmosphere such as an atmosphere containing nitrogen and a noble gas; an atmosphere containing nitrogen, hydrogen, and a noble gas; and an 25 atmosphere containing ammonia and a noble gas.

[0096]

The gate insulating film 28 may be formed by using an insulating film containing silicon as a main component, for example, a silicon oxide film, a silicon oxynitride film, a silicon nitride film, and a silicon nitride oxide film. In addition, it may be a single layer or a layered 30 film.

[0097]

A gate electrode 29 is formed over the gate insulating film 28 (FIG. 6B). The gate electrode 29 can be formed by using the material shown in the above-mentioned embodiment, and may be a single layer or a layered film including two or more layers. A known CVD sputtering, evaporation, or the like can be employed as a method for film formation. Dry etching or wet etching method can be used for processing the gate electrode 29 into an island-like shape with a photolithography method.

[0098]

An insulating film 30 is formed with a thickness of 50 nm to 1 μm by CVD or sputtering over the gate electrode 29 and the gate insulating film 28 (FIG. 6C). The insulating film 30 can be formed by using an insulating film containing silicon. An organic resin film or the like may be stacked over the insulating film containing silicon. The insulating film 30 functions as a planarization film or a passivation film. Since Al is included in the source electrode 25 and the drain electrode 26, a hillock is occasionally generated when the gate insulating film 28, the gate electrode 29, and the insulating film 30 are formed at a high temperature. Thus, they are preferably formed at a low temperature, at 500°C or less, preferably 350°C or less.

[0099]

As described above, this invention can prevent an impurity from diffusing due to an exposure of the substrate 1. An Al alloy film such as an AlNi film is used as the first conductive film, thereby achieving lower resistance of a wire.

[0100]

[Embodiment 5]

Here, a description is made of a method of manufacturing a liquid crystal display device using a bottom gate semiconductor device which is shown in Embodiments 1 and 3 referring to FIGS. 8A and 8B and 9A and 9B. Note that it is needless to say that the top gate semiconductor device which is shown in Embodiments 2 and 4 can be applied. FIGS. 8A and 9A show cross-sectional views taken along line X-Y in FIG. 8B.

[0101]

A gate wire 40 and an auxiliary capacitor wire 41 are formed over a glass substrate or a

plastic substrate 1. An AlNd film is formed by sputtering, and then, formed by known photolithography method and etching.

[0102]

A gate insulating film 42 formed by using a silicon oxide film or a silicon oxynitride film is formed by CVD or sputtering.

[0103]

An AlNi film is formed as a first conductive film by sputtering over the gate insulating film 42. The first conductive film forms a source electrode 45a, a drain electrode 46a and a source wire 47 later.

[0104]

A ZnO (zinc oxide) film to which Al is added is formed as a second conductive film by sputtering over the first conductive film. The second conductive film forms a source electrode 45b, a drain electrode 46b, and a source wire 47 later.

[0105]

A resist mask is formed in a region which is to be a source electrode portion, a drain electrode portion, and a source wire portion, over the second conductive film (not shown in the figure). Then, the second conductive film is etched. Here, etching is performed using buffered fluoric acid and a solution of $HF:NH_4F=1:100$ (weight ratio).

[0106]

Next, the first conductive film is etched using TMAH solution to form the source electrode 45a, the drain electrode 46a, and the source wire 47. After that, the resist mask is removed. Then, the source electrode 45, the drain electrode 46, and the source wire 47 can be formed without damaging the gate insulating film 42. In addition, since the ZnO film is not etched by TMAH, the size of the island-like shaped second conductive film is not reduced. Further, since an AlNi film is used for the first conductive film, the resistance of the source wire can be reduced.

[0107]

Next, a semiconductor film 48 is formed. A ZnO film is formed by sputtering, and then, the semiconductor film 48 is formed from the ZnO film by a photolithography method and etching. Wet etching using buffered fluoric acid is used as etching. The portion of the second

conductive film out of contact with the semiconductor film 48 may be partially removed here, because the first conductive film is formed in a portion to be a wire.

[0108]

An insulating film 49 is formed by CVD, sputtering, coating, or the like over the
5 semiconductor film 48. The insulating film 49 can be formed by using a layered film having an insulating film containing silicon, an organic resin film, or the like. The insulating film 49 may be a film which makes the unevenness of the surface planarized.

[0109]

A contact hole leading to the drain electrode 46 and a contact hole for the auxiliary
10 capacitor are formed in the insulating film 49 using a photolithography method and an etching method.

[0110]

A transparent conductive film is formed by sputtering, and then, a pixel electrode 50 is formed using a photolithography method and etching. For example, ITO (Indium Tin Oxide),
15 ITSO (Indium Tin Oxide containing silicon oxide), or IZO (Indium Zinc Oxide) may be used.

[0111]

In the case of a reflective liquid crystal display device, a light reflective metal material such as Ag (silver), Au (gold), Cu (copper), W (tungsten), or Al (aluminum) is formed instead of a transparent electrode.

20 [0112]

The portion where the pixel electrode 50 and the auxiliary capacitor wire 41 are overlapped forms an auxiliary capacitor 100 which is formed of the pixel electrode 50, the gate insulating film 42, and the auxiliary capacitor wire 41 (FIGS. 8A and 8B).

[0113]

25 A corner of a bent portion or a portion where width changes may be smoothed and rounded in a wire and an electrode. A shape of a chamfered corner can be realized by using a photomask pattern manufactured using a pattern of photomask. This will have advantages described below. When dry etching using plasma is performed, generation of fine particles due to abnormal discharge can be suppressed by chamfering a projecting portion. Even though the
30 fine particles are generated, the fine particles can be prevented from accumulating at the corner

at the time of cleaning, and the fine particles can be washed away by chamfering a concave portion. Thus, a problem of fine particles or dust in the manufacturing process can be solved and the yield can be improved.

[0114]

5 An alignment film 51 is formed so as to cover the pixel electrode 50. The alignment film is formed by a droplet discharge method, printing, or the like. After forming the alignment film, rubbing is conducted.

[0115]

A color filter 55 is formed by using a colored layer and a light-shielding layer (black 10 matrix), and a protective insulating film 54 is formed on an opposing substrate 56. A transparent electrode 57 is formed, and an alignment film 53 is formed on the protective insulating film 54 (FIG. 9A). The alignment film is subjected to a rubbing process.

[0116]

Next, a closed pattern 75 of a sealant is formed by a droplet discharge method (FIG. 9B). 15 A region surrounded by the sealant is filled with liquid crystal composition 52 (FIG. 9A).

[0117]

After dropping the liquid crystal composition 52 in the closed pattern 75, the opposing substrate 56 and a substrate 1 in which a semiconductor device is formed are attached to each other. When the liquid crystal composition 52 is filled, thefollowing alternative may be 20 adopted: a seal pattern having an opening portion is provided on the substrate 1; the opposing substrate 56 and the substrate 1 are attached to each other; then, liquid crystal is injected using capillary action.

[0118]

As an alignment mode of the liquid crystal composition 52, TN mode in which the 25 alignment of liquid crystal molecules is twisted at 90° from the side of light incidence to the side of light emission, FLC mode, IPS mode, or the like can be used. Note that an electrode pattern is different from one shown in FIG. 8B and is a comb-like shape in the case of the IPS mode.

[0119]

Polarizing plates are attached to both of the opposing substrate 56 and the substrate 1 on 30 which the semiconductor device is formed. In addition, an optical film can be attached if

required.

[0120]

The distance between the opposing substrate 56 and the substrate 1 on which the semiconductor device is formed may be kept by dispersing spherical spacers or forming a columnar spacer formed of a resin, or by mixing fillers in the sealant. The aforementioned columnar spacer is formed of an organic resin material containing at least one of acrylic, polyimide, polyimide amide, or epoxy as a main component, or an inorganic material having one of silicon oxide, silicon nitride and silicon oxide containing nitrogen, or a layered film thereof.

[0121]

Then, an FPC (Flexible Printed Circuit) is attached to the the substrate 1 with an anisotropic conductive layer interposed therebetween using a known technique.

[0122]

A peripheral driver circuit may be formed over the substrate. A plane exemplary diagram is shown in FIG. 9B.

[0123]

A gate wire driver circuit 62, a source wire driver circuit 63, and an active matrix portion 64 are formed over a substrate 61 formed of glass or the like. The gate wire driver circuit 62 is constituted from at least a shift register 62a and a buffer 62b. The source wire driver circuit 63 is constituted from at least a shift register 63a, a buffer 63b, and an analog switch 69 which samples video signals transmitted via video lines 68. A plurality of gate wires 72 extended from the gate wire driver circuit 62 is arranged in parallel with each other in the active matrix portion 64. A plurality of source wires 71 extended from the source wire driver circuit 63 is arranged orthogonally to the gate wires 72. In addition, an auxiliary capacitor wire 73 is arranged in parallel with the gate wires 72. In addition, a semiconductor device 65, a liquid crystal portion 66, and an auxiliary capacitor 67 are provided in a region surrounded by the gate wire 72, the source wires 71, and the auxiliary capacitor wire 73.

[0124]

The gate wire driver circuit 62, the source wire driver circuit 63, and the analog switch 69 are provided with a semiconductor device manufactured by the same manufacturing method as the semiconductor device 65 to have a similar structure.

[0125]

In the semiconductor device 65, a gate electrode is connected to the gate wire 72, and the source electrode is connected to the source wire 71. A liquid crystal portion 66 is formed by introducing a liquid crystal to be sealed between a pixel electrode connected to the drain electrode of the semiconductor device 65 and an opposing electrode over the opposing substrate. The auxiliary capacitor wire 73 is connected to an electrode having the same potential as the opposing electrode.

[0126]

In the aforementioned liquid crystal display device, the gate insulating film is not etched and the characteristics do not become unstable, and thus, high reliability is realized. In the case of using a top gate semiconductor device, a glass substrate or a base film formed by using, a silicon oxide film or a silicon oxynitride film is not etched, so that impurity such as sodium is not diffused into a semiconductor film from the substrate and the characteristics are not deteriorated, and thus, high reliability can be realized.

[0127]

Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

[0128]

[Embodiment 6]

Here, a description is made of a method for manufacturing a light-emitting device with using the bottom gate semiconductor device shown in Embodiments 1 and 3 referring to FIGS. 10A and 10B and 11A and 11B. Note that it is needless to say that the semiconductor device of Embodiments 2 and 4 can be applied.

[0129]

The semiconductor device is manufactured based on the description of the aforementioned embodiment, and formation to the stage shown in FIG. 10A is carried out. Note that the same parts as those of the above embodiments are denoted by the same reference numerals.

[0130]

In the EL display device, the pixel electrode 50 functions as an anode or a cathode. As

the material for the pixel electrode 50, the following can be employed: a conductive metal such as aluminum (Al), silver (Ag), gold (Au), platinum (Pt), nickel (Ni), tungsten (W), chromium (Cr), molybdenum (Mo), iron (Fe), cobalt (Co), copper (Cu), palladium (Pd), lithium (Li), caesium (Cs), magnesium (Mg), calcium (Ca), strontium (Sr), or titanium (Ti); an alloy such as
5 aluminum-silicon (Al-Si), aluminum-titanium (Al-Ti), or aluminum-silicon-copper (Al-Si-Cu); nitride of a metal material such as titanium nitride (TiN); a metal compound such as ITO, ITO containing silicon, or IZO.

[0131]

An electrode from which light emitted from an EL layer is extracted is only required to
10 be formed by using a light-transmitting conductive film, and a very thin film of metal such as Al or Ag may be used as well as a metal compound such as ITO, ITO containing silicon, or IZO.

[0132]

When light-emission is extracted from an electrode which is opposed to the pixel electrode 50, a highly reflective material (Al, Ag, or the like) can be used for the pixel electrode
15 50. In this embodiment, ITSO, which means ITO containing silicon, is used as the pixel electrode 50 (FIG. 10A).

[0133]

Next, an insulating film formed by using an organic material or an inorganic material is formed so as to cover the insulating film 49 and the pixel electrode 50. Then, the insulating
20 film is processed to expose the pixel electrode 50 partially, thereby forming partition walls 81. As the material of the partition walls 81, a photosensitive organic material (such as acrylic or polyimide) is preferable. Alternatively, a non-photosensitive organic material or inorganic material may also be used. Further, the partition walls 81 may be used as a black matrix by coloring the partition walls 81 black in such a way that a black pigment or dye such as titanium
25 black or carbon nitride is dispersed into the material of the partition wall 81 with the use of a dispersant. It is desirable that the partitions wall 81 have a tapered shape and those end surfaces 81a toward the pixel electrode have curvatures changing continuously (FIG. 10B).

[0134]

Next, a layer 82 including a light-emitting substance is formed, and an opposing
30 electrode 83 which covers the layer 82 including a light-emitting substance is formed. Then, a

light-emitting element with the layer 82 including a light-emitting substance interposed between the pixel electrode 50 and the opposing electrode 83 can be manufactured, and light-emission can be obtained by applying a voltage between the opposing electrode 83 and the pixel electrode 50.

5 [0135]

As an electrode material used for forming the opposing electrode 83, a material similar to one which can be used for the pixel electrode can be used. In this embodiment, aluminum is used for a second electrode.

[0136]

10 The layer 82 including a light-emitting substance is formed by evaporation, ink-jet, spin coating, dip coating, roll-to-roll method, sputtering, or the like.

[0137]

In the case of an organic electroluminescent display device, the layer 82 including a light-emitting substance may be a layered film of layers having functions of hole transportation, 15 hole injection, electron transportation, electron injection, or light-emission, respectively, or a single layer of a light-emitting layer. As a layer including a light-emitting substance, a single layer or a layered film of an organic compound may be used.

[0138]

A hole injecting layer is provided between an anode and a hole transporting layer. As 20 the hole injecting layer, a mixed layer of an organic compound and a metal oxide can be used. This prevents short circuit between the pixel electrode 50 and the opposing electrode 83 due to unevenness which is formed on the surface of the pixel electrode 50 or a foreign substance which is left on the surface of the electrode. The thickness of the mixed layer is preferably 60 nm or more, more preferably 120 nm or more. Since increase in thickness of a film does not cause 25 increase in driving voltage, the thickness of the film can be selected such that the influence of the unevenness or foreign substance can be covered sufficiently. Thus, a dark spot is not generated, and driving voltage or power consumption is not increased in the light-emitting device manufactured by this invention.

[0139]

30 An oxide or a nitride of transition metal is preferable as a metal oxide, concretely,

zirconium oxide, hafnium oxide, vanadium oxide, niobium oxide, tantalum oxide, chromium oxide, molybdenum oxide, tungsten oxide, titanium oxide, manganese oxide, and rhenium oxide.

[0140]

As an organic compound, the following can be employed: an organic material having an arylamino group such as 4,4′-bis[N-(1-napthyl)-N-phenylamino]biphenyl (NPB); 4,4′-bis[N-(3-methylphenyl]-N-phenylamino]biphenyl (TPD), 4,4′,4″-tris(N,N-diphenylamino)triphenylamine (TDATA), 4,4′,4″-tris[N-(3-methylphenyl)-N-phenylamino]triphenylamine (MTDATA), 4,4′-bis{N-[4-(N,N-di-m-tolylamino)phenyl]-N-phenylamino}biphenyl (DNTPD), 1,3,5-tris[N,N-di(m-tolyl)amino] benzene (m-MTDAB), and 4,4',4"-tris(N-carbazolyl) triphenylamine (TCTA); phthalocyanine (H_2Pc); copper phthalocyanine (CuPc); vanadyl phthalocyanine (VOPc); or the like.

[0141]

The hole transporting layer is provided between the anode and a light-emitting layer, or between the hole injecting layer and the light-emitting layer when the hole injecting layer is provided. The hole transporting layer is formed by using a layer which has an excellent property of transporting a hole, for example, a layer formed by using a compound of aromatic amine (that is, having a benzene ring-nitrogen bond) such as NPB, TPD, TDATA, MTDATA, and BSPB. The substances mentioned here have the hole mobility of 1×10^{-6} to 10 cm^2/Vs mainly. Note that a substance having higher transporting property of holes than electrons may be used as well as the materials. Note that the hole transporting layer may be formed by not only a single layer but also a layered film in which two or more layers formed from the above mentioned substances are stacked.

[0142]

The light-emitting layer is provided between the anode and the cathode, or between the hole transporting layer and the electron transporting layer when the hole transporting layer and the electron transporting layer are provided. There is no particular limitation on the light-emitting layer; however, a layer serving as the light-emitting layer has two modes roughly. One is a host-guest type layer which includes a dispersed light-emitting substance in a layer formed of a material (host material) having a larger energy gap than an energy gap of a

light-emitting substance (dopant material) which becomes a luminescent center, while the other is a layer in which a light-emitting layer is made of a light-emitting substance only. The former is preferable, because concentration quenching hardly occurs. As the light-emitting substance to be a luminescent center, the following can be employed:
5 4-dicyanomethylene-2-methyl-6-(1,1,7,7-tetramethyljulolidyl-9-enyl)-4H-pyran (DCJT); 4-dicyanomethylene-2-t-butyl-6-(1,1,7,7-tetramethyljulolidine-9-enyl)-4H-pyran; periflanthene; 2,5-dicyano-1, 4-bis(10-methoxy-1,1,7,7-tetramethyljulolidine-9-enyl)benzene; N,N′-dimethylquinacridone (DMQd); coumarin 6; coumarin 545T; tris (8-quinolinolato)aluminum (Alq_3); 9,9′-bianthryl; 9,10-diphenylanthracene (DPA);
10 9,10-bis(2-naphthyl)anthracene (DNA); 2,5,8,11-tetra-t-butylperylene (TBP); PtOEP; $Ir(ppy)_3$; $Btp_2Ir(acac)$; FIrpic; or the like. As the base material to be a host material in the case of forming the layer in which the light-emitting substance is diffused, the following can be used: an anthracene derivative such as 9,10-di(2-naphtyl)-2-tert-butylanthracene (t-BuDNA); a carbazole derivative such as 4,4′-bis(N-carbazolyl)biphenyl (CBP); or a metal complex such as
15 tris(8-quinolinolato)aluminum (Alq_3), tris(4-methyl-8-quinolinolato)aluminum ($Almq_3$); bis(10-hydroxybenzo[h]-quinolinato)beryllium ($BeBq_2$); bis(2-methyl-8-quinolinolato)-4-phenylphenolato-aluminum (BAlq); bis[2-(2-hydroxyphenyl)pyridinato]zinc ($Znpp_2$); or bis[2-(2-hydroxyphenyl)benzoxazolate]zinc (ZnBOX). As the material which can constitute the light-emitting layer only with a
20 light-emitting substance, tris(8-quinolinolato)aluminum (Alq_3), 9,10-bis(2-naphtyl)anthracene (DNA), bis(2-methyl-8-quinolinolato)-4-phenylphenolato-aluminum (BAlq), or the like can be used.

[0143]

An electron transporting layer is provided between the light-emitting layer and the
25 cathode, or between the light-emitting layer and an electron injecting layer when the electron injecting layer is provided. The electron transporting layer is a layer having an excellent electron transporting property, and for example, a layer formed using a metal complex having a quinoline skeleton or a benzoquinoline skeleton such as tris(8-quinolinolato)aluminum (Alq_3), tris(5-methyl-8-quinolinolato)aluminum ($Almq_3$), bis(10-hydroxybenzo[h]-quinolinato)beryllium
30 ($BeBq_2$), and bis(2-methyl-8-quinolinolato)-4-phenylphenolato-aluminum (BAlq). In addition,

a metal complex having an oxazole ligand or a thiazole ligand such as bis[2-(2-hydroxyphenyl)-benzoxazolato]zinc ($Zn(BOX)_2$), bis[2-(2-hydroxyphenyl)-benzothiazolato]zinc ($Zn(BTZ)_2$), or the like can be used. In addition to the metal complexes, 2-(4-biphenylyl)-5-(4-tert-butylphenyl)-1,3,4-oxadiazole (PBD);
5 1,3-bis[5-(p-tert-butylphenyl)-1,3,4-oxadiazole-2-yl]benzene (OXD-7); 3-(4-tert-butylphenyl)-4-phenyl-5-(4-biphenylyl)-1,2,4-triazole (TAZ); 3-(4-tert-butylphenyl)-4-(4-ethylphenyl)-5-(4-biphenylyl)-1,2,4-triazole (p-EtTAZ); bathophenanthroline (BPhen); bathocuproine (BCP); or the like can be used. These substances mentioned here mainly have the electron mobility of 1×10^{-6} to 10 cm^2/Vs. Note that other
10 substance may be used for the electron transporting layer so long as it has a higher electron transporting property than a hole transporting property. Further, the electron transporting layer may be formed by not only a single layer but also a layered film in which two or more layers made from the above mentioned substances are stacked.

[0144]

15 The electron injecting layer is provided between the cathode and the electron transporting layer. As the electron injecting layer, a compound of alkali metal or alkaline earth metal such as lithium fluoride (LiF), cesium fluoride (CsF), or calcium fluoride (CaF_2) can be employed. In addition to that, a layer formed by using an electron transporting substance which contains alkali metal or alkaline earth metal, for example, Alq_3 containing magnesium (Mg) or
20 the like can be used.

[0145]

In the case of an inorganic electroluminescent display device, one in which a fluorescent substance particles are diffused in dispersing agent for the layer 82 including a light-emitting substance can be used.

25 [0146]

A fluorescent substance in which a donor impurity such as Cl (chlorine), I (iodine), or Al (aluminum) is added with Cu (copper) in ZnS can be used.

[0147]

As the dispersing agent, the following can be employed: a polymer having a relatively
30 high dielectric constant such as cyanoethyl cellulose based resin, polyethylene based resin,

polypropylene based resin, polystyrene based resin, silicone resin, epoxy resin, vinylidene fluoride resin, or the like. The dielectric constant can be adjusted by mixing the resin and minute particles having high dielectric constant such as $BaTiO_3$ (barium titanate) or $SrTiO_3$ (strontium titanate). As a diffusing means, an ultrasonic diffusing machine or the like can be
5 used.

[0148]

A dielectric layer may be provided between the layer 82 including a light-emitting substance and one of the electrodes. For the dielectric layer, a highly dielectric and insulating material which has a high dielectric breakdown voltage is employed. One is selected from a
10 metal oxide or nitride, for example, TiO_2, $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $KNbO_3$, $PbNbO_3$, Ta_2O_3, $BaTa_2O_6$, $LiTaO_3$, Y_2O_3, Al_2O_3, ZrO_2, AlON, ZnS, or the like. Those may be disposed as a uniform film or a film having a particle structure.

[0149]

In the case of an inorganic electroluminescent display device, a double-insulating
15 structure in which a light-emitting layer is interposed between insulating layers may be employed. The light-emitting layer can be formed by using a II-VI compound such as Mn (manganese) or ZnO (zinc sulfide) containing a rare earth element, and the insulating layer can be formed by using oxide or nitride such as Si_3N_4, SiO_2, Al_2O_3, or TiO_2.

[0150]

20 A silicon oxide film containing nitrogen is formed as a passivation film over the opposing electrode 83 by plasma CVD (not shown). In the case of using a silicon oxide film containing nitrogen, the following can be used: a silicon oxynitride film formed by using SiH_4, N_2O, and NH_3 by plasma CVD; a silicon oxynitride film formed by using SiH_4, and N_2O; or a silicon oxynitride film formed by using a gas in which SiH_4 and N_2O is diluted with Ar.

25 [0151]

A silicon oxide nitride hydride film manufactured from SiH_4, N_2O, and H_2 may be employed as a passivation film. Note that a passivation film is not limited to the aforementioned substance. Another insulating film containing silicon as a main component can be also used. In addition, a layered film structure may be employed as well as a single layer
30 structure. Further, a multilayer film of a carbon nitride film and a silicon nitride film or a

multilayer film of a styrene polymer can be used. A silicon nitride film or a diamond-like carbon film may be formed.

[0152]

Then, a display portion is sealed to protect a light-emitting element from a material such as water which promotes deterioration. In the case of using an opposing substrate for sealing, the opposing substrate is attached by using an insulating sealant so as to expose an external connection portion. A space between the opposing substrate and an element substrate may be filled with an inert gas such as dry nitrogen, or the opposing substrate may be attached by applying a sealant to the pixel portion entirely. It is preferable to use an ultraviolet curing resin or the like as the sealant. A drying agent or particles for keeping the gap between the substrates constant may be mixed in the sealant. Then, the light-emitting device is completed by attaching a flexible wire board to the external connection portion.

[0153]

One example of a structure of the light-emitting device manufactured as described above is shown referring to FIGS. 11A and 11B. Note that portions having the same functions are sometimes denoted by the same reference numerals even though they have different shapes, and the explanations are occasionally omitted.

[0154]

FIG. 11A shows a structure in which the pixel electrode 50 is formed using a light transmitting conductive film, and light generated in the layer 82 including a light-emitting substance is emitted toward a substrate 1. Further, reference numeral 86 denotes an opposing substrate. This opposing substrate is firmly attached to the substrate 1 using a sealant or the like after forming a light emitting element. A space between the opposing substrate 86 and the element is filled with resin 85 having a light-transmitting property or the like to seal the light emitting element. Accordingly, the light emitting element can be prevented from being deteriorated by moisture or the like. Preferably, the resin 85 has a hygroscopic property. More preferably, a drying agent 84 with a high light-transmitting property is dispersed in the resin 85 to prevent the adverse influence of moisture.

[0155]

FIG. 11B shows a structure in which both the pixel electrode 50 and an opposing

substrate 83 are formed by using conductive films having light-transmitting property. Accordingly, light can be emitted toward both the substrate 1 and the opposing substrate 86 as shown by an arrow of dotted lines. In this structure, by providing polarizing plates 88 outside of the substrate 1 and the opposing substrate 86, a screen can be prevented from being
5 transparent, thereby improving visibility. Protection films 87 are preferably provided outside of the polarizing plates 88.

[0156]

The light-emitting device of this invention having a display function may employ either an analog video signal or a digital video signal. If a digital video signal is used, the video
10 signal may use either a voltage or a current.

[0157]

When the light-emitting element emits light, a video signal to be inputted to a pixel may have either a constant voltage or a constant current. When a video signal has a constant voltage, a constant voltage is applied to a light-emitting element or a constant current flows through the
15 light-emitting element.

[0158]

Also, when a video signal has a constant current, a constant voltage is applied to a light-emitting element or a constant current flows through the light-emitting element. A driving method where a constant voltage is applied to a light-emitting element is called a constant
20 voltage drive. Meanwhile, a driving method where a constant current flows through a light-emitting element is called a constant current drive. In the constant current drive, constant current flows regardless of change in resistance of a light emitting element. The light emitting display device according to this invention and the driving method thereof may use any one of the aforementioned methods.

25 [0159]

In the light-emitting device, a gate insulating film is not etched, and the characteristics of the light-emitting element is not unstable so that its reliability is high. In the case of using a top gate semiconductor device, since a glass substrate or a base film formed by using, a silicon oxide film or a silicon oxynitride film is not etched, impurity such as sodium which deteriorates
30 characteristics is not diffused from the substrate into the semiconductor film so that high

reliability is obtained.

[0160]

Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

5 [0161]

A pixel circuit and a protective circuit included in a panel and module, and operation thereof are shown referring to FIGS. 12A to 12F and 13 or the like. FIGS. 10A and 10B and 11A and 11B each show a cross-sectional view of a driving TFT 1403 of the semiconductor device. A switching TFT 1401, a current control TFT 1404, and an eraser TFT 1406 may be manufactured at the same time of the driving TFT 1403, and may have the same structure as the driving TFT 1403.

[0162]

A pixel shown in FIG. 12A includes a signal line 1410 and power source lines 1411 and 1412 arranged in a column direction and a scan line 1414 arranged in a row direction. The pixel further includes a switching TFT 1401, the driving TFT 1403, the current control TFT 1404, an auxiliary capacitor 1402, and a light-emitting element 1405.

[0163]

A pixel shown in FIG. 12C has the same structure as one in FIG. 12A except for that the gate electrode of the driving TFT 1403 is connected to the power source line 1412 provided in the row direction. In other words, the pixels shown in FIGS. 12A and 12C have the same equivalent circuit diagram. However, a power source line formed in the case of arranging the power source line 1412 in the column direction (FIG. 12A) is formed by using a conductive layer in a different layer from a layer in which a power source line is formed by using a conductive layer in the case of arranging the power source line 1412 in the row direction (FIG. 12C). Here, attention is paid to a wire connected to the gate electrode of the driving TFT 1403, and the structure is shown separately in FIGS. 12A and 12C in order to show that these wires are manufactured with different layers.

[0164]

As a feature of the pixels shown in FIGS. 12A and 12C, the driving TFT 1403 and the current control TFT 1404 are connected serially within the pixel, and it is preferable to set the

channel length L (1403) and the channel width W (1403) of the driving TFT 1403, and the channel length L (1404) and the channel width W (1404) of the current control TFT 1404 so as to satisfy L (1403)/W (1403):L (1404)/W (1404)=5 to 6000:1.

[0165]

5 The driving TFT 1403 operates in a saturation region and serves to control the current value of the current flowing into the light-emitting element 1405. The current control TFT 1404 operates in a linear region and serves to control the current supplied to the light-emitting element 1405. Both the TFTs preferably have the same conductivity type in the manufacturing process, and the TFTs are n-channel type TFTs in this embodiment. The driving TFT 1403 may 10 be either an enhancement mode TFT or a depletion mode TFT. Since the current control TFT 1404 operates in the linear region in the light-emitting device having the above structure, slight fluctuation of Vgs of the current control TFT 1404 does not affect the current value of the light-emitting element 1405. That is to say, the current value of the light-emitting element 1405 can be determined by the driving TFT 1403 operating in the saturation region. With the above 15 structure, the variation of the luminance of the light-emitting element due to the variation of the characteristics of the TFT can be remedied, thereby providing a light-emitting device having improved image quality.

[0166]

In each pixel shown in FIGS. 12A to 12D, the switching TFT 1401 is to control the 20 input of the video signal to the pixel, and the video signal is inputted into the pixel when the switching TFT 1401 is turned on. Then, the voltage of the video signal is held in the auxiliary capacitor 1402. Although FIGS. 12A and 12C show the structure in which the auxiliary capacitor 1402 is provided, this invention is not limited thereto. When the gate capacitance and the like can serve as a capacitor holding the video signal, the auxiliary capacitor 1402 is not 25 necessarily provided.

[0167]

A pixel shown in FIG. 12B has the same pixel structure as that in FIG. 12A except for that a TFT 1406 and a scan line 1415 are added. In the same way, a pixel shown in FIG. 12D has the same pixel structure as that in FIG. 12C expect for that the TFT 1406 and the scan line 30 1415 are added.

[0168]

ON and OFF of the TFT 1406 is controlled by the additionally provided scan line 1415. When the TFT 1406 is turned on, the charge held in the auxiliary capacitor 1402 is discharged, thereby turning off the current control TFT 1404. In other words, by the provision of the TFT 1406, a state can be produced compellingly in which the current does not flow into the light-emitting element 1405. For this reason, the TFT 1406 can be referred to as an eraser TFT. Consequently, in the structures shown in FIGS. 12B and 12D, a lighting period can be started at the same time as or just after the start of a writing period before the writing of the signal into all the pixels; therefore the duty ratio can be increased.

[0169]

In a pixel shown in FIG. 12E, the signal line 1410 and the power source line 1411 are arranged in the column direction, and the scan line 1414 is arranged in the row direction. Further, the pixel includes the switching TFT 1401, the driving TFT 1403, the auxiliary capacitor 1402, and the light-emitting element 1405. A pixel shown in FIG. 12F has the same pixel structure as that shown in FIG. 12E except for that the TFT 1406 and the scan line 1415 are added. In the structure shown in FIG. 12F, the duty ratio can also be increased by the provision of the TFT 1406.

[0170]

Such an active matrix light-emitting device can be driven at low voltage when the pixel density increases, because the TFTs are provided in respective pixels. Therefore, it is considered that the active matrix light-emitting device is advantageous.

[0171]

Although this embodiment described the active matrix light-emitting device in which the respective TFTs are provided in respective pixels, a passive matrix light-emitting device can also be formed. Since the TFTs are not provided in respective pixels in the passive matrix light-emitting device, high aperture ratio can be obtained. In the case of a light-emitting device in which light is emitted to both sides of the light emission stack, the transmissivity of the passive matrix light-emitting device is increased.

[0172]

Subsequently, a case will be described in which a diode is provided as a protective

circuit on the scan line and the signal line with the use of an equivalent circuit shown in FIG 12E.

[0173]

In FIG 13, the switching TFT 1401, the driving TFT 1403, the auxiliary capacitor 1402, and the light-emitting element 1405 are provided in a pixel area 1500. Diodes 1561 and 1562 are provided on the signal line 1410. In the similar way to the switching TFT 1401 and the driving TFT 1403, the diodes 1561 and 1562 are manufactured based on the above embodiments, and have a gate electrode, a semiconductor layer, a source electrode, a drain electrode, and the like. The diodes 1561 and 1562 are operated as diodes by connecting the gate electrode with the drain electrode or the source electrode.

[0174]

Common potential lines 1554 and 1555 connecting to the diodes 1561 and 1562 are formed by using the same layer as the gate electrode. Therefore, in order to connect the common potential lines 1554 and 1555 with the source electrode or the drain electrode of the diode, it is necessary to form a contact hole in the gate insulating layer.

[0175]

Diodes 1563 and 1564 provided on the scan line 1414 have a similar structure. Further, common potential lines 1565 and 1566 has the similar structure.

[0176]

In this manner, protection diodes can be simultaneously formed in an input stage according to this invention. Further, the positions of the protection diodes are not limited to this, and they can be provided between a driver circuit and a pixel.

[0177]

A top view of a pixel portion in the case of using an equivalent circuit shown in FIG 12E is described in FIG 14A. In addition, the same equivalent circuit as that in FIG 12E is shown in FIG 14B. Each semiconductor device shown in FIGS. 10A, 10B, 11A, and 11B is corresponds to each driving TFT 1403. FIGS. 10A, 10B, 11A and 11B show cross-sectional views taken along line X-Y in FIG 14A and 14B. The power source line 1411, the signal line 1410, and the source electrode and the drain electrode of the switching TFT 1401 are formed by using the first conductive film, and the source electrode and the drain electrode of the driving

TFT 1403 are formed by using the second conductive film.

[0178]

The switching TFT 1401 is manufactured by the same method as the driving TFT 1403. The drain electrode of the switching TFT 1401 and a gate electrode 40 of the driving TFT 1403 are connected electrically with each other through a contact hole formed in an insulating film in the same layer as the gate insulating film 42.

[0179]

The auxiliary capacitor 1402 is formed by using a portion where the gate electrode of the driving TFT 1403 is extended, the power source line 1411, and an insulating film in the same layer as the gate insulating film 42.

[0180]

A light-emitting region 1420 is formed in an opening portion of a partition wall 81. The partition wall 81 is formed in the vicinity of the light-emitting region 1420, although it is not shown. The corner portion of the light-emitting region 1420 may be rounded. By making the corner portion of the opening portion of the partition wall 81 rounded, the corner portion of the light-emitting region 1420 can be rounded. When dry etching using plasma is performed to process the partition wall 81, generation of fine particles due to abnormal discharge can be suppressed by making the corner portion rounded.

[0181]

This embodiment can be combined with a suitable structure of the above embodiments as appropriate.

[0182]

[Embodiment 7]

As an electronic device having semiconductor devices according to this invention mounted with modules shown as examples in the above embodiments, a camera such as a video camera or a digital camera; a goggle type display (a head mounted display); a navigation system; an audio reproducing device (e.g., a car audio component); a computer; a game machine; a portable information terminal (e.g., a mobile computer, a cellular phone, a portable game machine, an electronic book, or the like); an image reproducing device equipped with a recording medium (specifically, a device which can reproduce the content of a recording medium

such as a digital versatile disc (DVD) and which has a display for displaying an image stored therein); and the like can be given. Specific examples of these electronic appliances are shown in FIGS. 15A to 15E, and FIG. 16.

[0183]

5 FIG. 15A shows a monitor for a television receiver or a personal computer, or the like, including a housing 3001, a display area 3003, speakers 3004, and the like. An active matrix display device is provided in the display area 3003. Each pixel of the display area 3003 includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a television with less characteristic 10 deterioration can be obtained.

[0184]

FIG. 15B shows a cellular phone, including a main body 3101, a housing 3102, a display area 3103, an audio input portion 3104, an audio output portion 3105, operation keys 3106, an antenna 3108, and the like. An active matrix display device is provided in the display area 15 3103. Each pixel of the display area 3103 includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a cellular phone with less characteristic deterioration can be obtained.

[0185]

FIG. 15C shows a computer, including a main body 3201, a housing 3202, a display area 20 3203, a keyboard 3204, an external connection port 3205, a pointing mouse 3206, and the like. An active matrix display device is provided in the display area 3203. Each pixel of the display area 3203 includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a computer with less characteristic deterioration can be obtained.

25 [0186]

FIG. 15D shows a mobile computer, including a main body 3301, a display area 3302, a switch 3303, operation keys 3304, an infrared port 3305, and the like. An active matrix display device is provided in the display area 3302. Each pixel of the display area 3302 includes a semiconductor device manufactured in accordance with this invention. By using the 30 semiconductor device of this invention with this structure, a mobile computer with less

characteristic deterioration can be obtained.

[0187]

FIG. 15E shows a portable game machine, including a housing 3401, a display area 3402, speakers 3403, operation keys 3404, a recording medium insert portion 3405, and the like. An active matrix display device is provided in the display area 3402. Each pixel of the display area 3402 includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a portable game machine with less characteristic deterioration can be obtained.

[0188]

FIG. 16 shows a flexible display, including a main body 3110, a pixel area 3111, a driver IC 3112, a receiving device 3113, a film buttery 3114, and the like. The receiving device can receive a signal from an infrared communication port 3107 of the above described cellular phone. An active matrix display device is provided in the pixel area 3111. Each pixel of the pixel area 3111 includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a flexible display with less characteristic deterioration can be obtained.

[0189]

As set forth above, the application range of this invention is extremely wide, and this invention can be applied to electronic devices in all fields.

[0190]

The present application is based on Japanese Patent Application serial No. 2005-329806 filed on November 15, 2005 in Japanese Patent Office, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

a gate electrode;

5 a gate insulating film over the gate electrode;

a first film comprising metal material over the gate insulating film;

a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the first film; and

a third film comprising the transparent semiconductor material over the second film and 10 the gate insulating film.

2. A semiconductor device according to claim 1, wherein the gate insulating film comprises silicon oxide or silicon oxynitride.

15 3. A semiconductor device according to claim 1, wherein the metal material is aluminum or aluminum alloy.

4. A semiconductor device according to claim 1, wherein the transparent semiconductor material is zinc oxide.

20

5. A semiconductor device comprising:

an insulating film over a substrate;

a first film comprising a metal material over the insulating film;

a second film comprising a transparent semiconductor material and an n-type or p-type 25 impurity over the metal film;

a third film comprising the transparent semiconductor material over the insulating film and the second film;

a gate insulating film over the third film; and

a gate electrode over the gate insulating film.

30

6. A semiconductor device according to claim 5, wherein the insulating film comprises silicon oxide or silicon oxynitride.

7. A semiconductor device according to claim 5, wherein the metal material is aluminum
5 or aluminum alloy.

8. A semiconductor device according to claim 5, wherein the transparent semiconductor material is zinc oxide.

10 9. A manufacturing method of a semiconductor device, comprising:

forming an insulating film over a substrate;

forming a first film comprising a metal material over the insulating film;

forming a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the first film,

15 etching the second film, and

etching the first film.

10. A manufacturing method of a semiconductor device according to Claim 9, further comprising forming a third film comprising the transparent semiconductor material over the
20 second film and the insulating film after the step of etching the first film.

11. A manufacturing method of a semiconductor device according to claim 9, wherein the insulating film comprises silicon oxide or silicon oxynitride.

25 12. A manufacturing method of a semiconductor device according to claim 9, wherein the metal material is aluminum or aluminum alloy.

13. A manufacturing method of a semiconductor device according to claim 9, wherein the transparent semiconductor material is zinc oxide.

30

14. A manufacturing method of the semiconductor device according to claim 9, wherein the substrate is a glass substrate.

15. A manufacturing method of the semiconductor device according to claim 10, wherein the transparent semiconductor material is zinc oxide.

16. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the second film is wet etching.

17. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the second film is wet etching using a buffered fluoric acid.

18. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the second film is performed by dry etching.

19. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the second film is performed by dry etching using CH_4 gas.

20. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the first film is performed by wet etching.

21. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the first film is performed by wet etching using a developer for a photoresist.

22. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the first film is performed by wet etching using an organic alkali solution.

23. A manufacturing method of the semiconductor device according to Claim 9, wherein the etching of the first film is performed by wet etching using TMAH (tetramethylammonium hydroxide).

24. A manufacturing method of a semiconductor device, comprising:

forming a gate electrode over a substrate;

forming a gate insulating film over the gate electrode;

5 forming a first film comprising a metal material over the gate insulating film;

forming a second film comprising a transparent semiconductor material and an n-type or p-type impurity over second film,

etching the second film, and

etching the first film.

10

25. A manufacturing method of the semiconductor device according to Claim 24, further comprising forming a third film comprising the transparent semiconductor material over the second film and the gate insulating film after the step of etching the first film.

15 26. A manufacturing method of the semiconductor device according to claim 24, wherein the gate insulating film comprises silicon oxide or silicon oxynitride.

27. A manufacturing method of the semiconductor device according to claim 24, wherein the metal material is aluminum or aluminum alloy.

20

28. A manufacturing method of the semiconductor device according to claim 24, wherein the transparent semiconductor material is zinc oxide.

29. A manufacturing method of the semiconductor device according to claim 24,

25 wherein the substrate is a glass substrate.

30. A manufacturing method of the semiconductor device according to claim 25, wherein the transparent semiconductor material is zinc oxide.

30 31. A manufacturing method of the semiconductor device according to Claim 25, further

comprising:

forming a gate insulating film over the third film, and

forming a gate electrode over the gate insulating film.

5 32. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the second film is performed by wet etching.

33. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the second film is performed by wet etching using a buffered fluoric acid.

10

34. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the second film is performed by dry etching using CH_4 gas.

35. A manufacturing method of the semiconductor device according to Claim 24,

15 wherein the etching of the first film is performed by wet etching.

36. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the first film is performed by wet etching using a developer for a photoresist.

20

37. A manufacturing method of the semiconductor device according to Claim 24, wherein the etching of the first film is performed by wet etching using an organic alkali solution.

38. A manufacturing method of the semiconductor device according to Claim 24,

25 wherein the etching of the first film is performed by wet etching using TMAH (tetramethylammonium hydroxide).

30

FIG. 1A

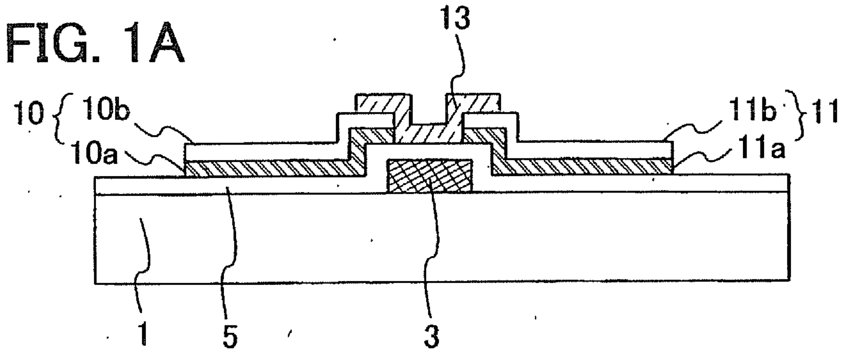


FIG. 1B

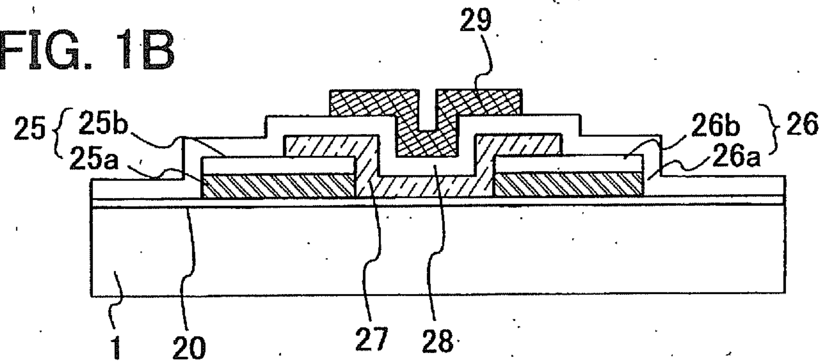


FIG. 2A

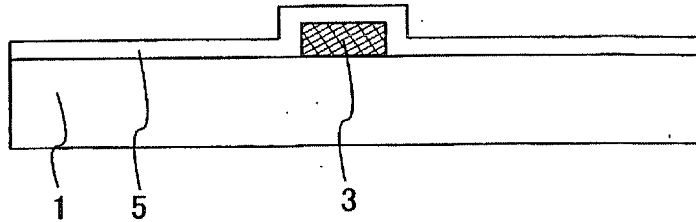


FIG. 2B

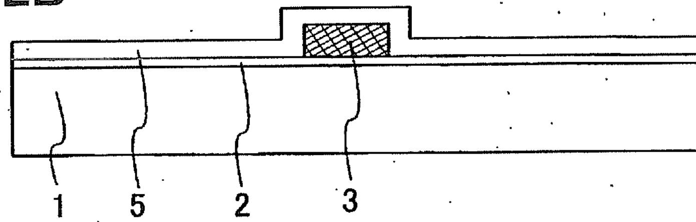


FIG. 2C

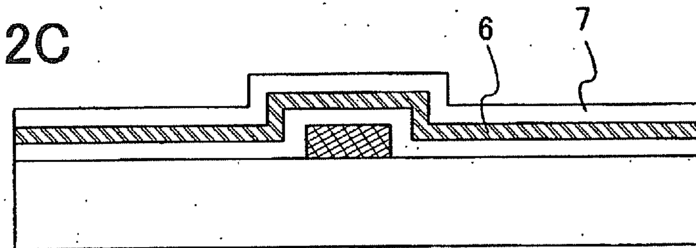


FIG. 2D

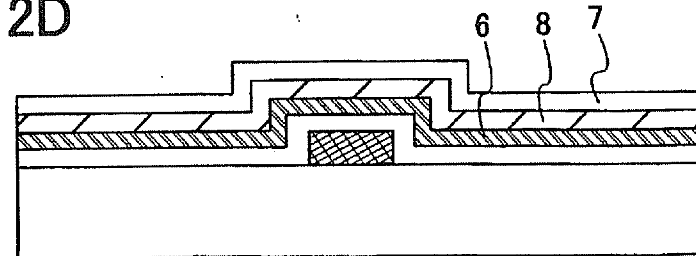


FIG. 3A

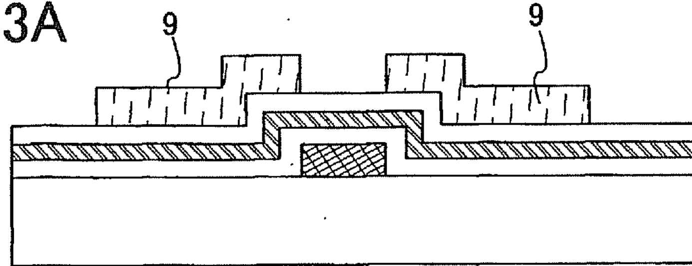


FIG. 3B

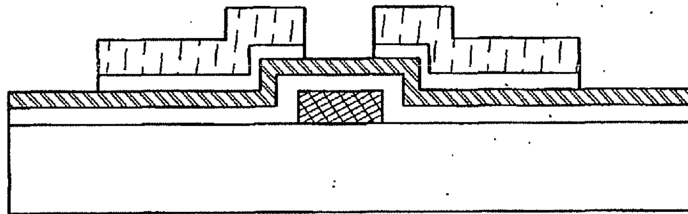


FIG. 3C

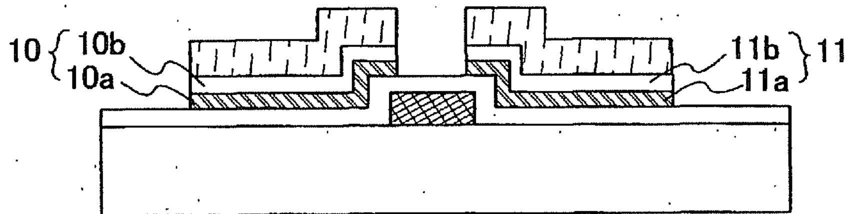


FIG. 3D

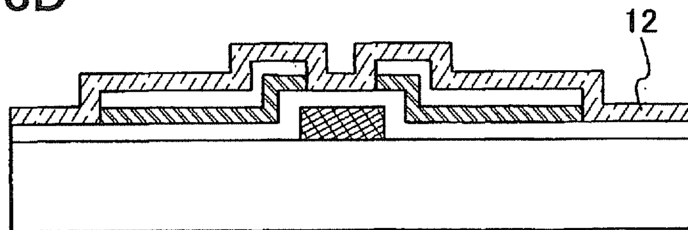


FIG. 4A

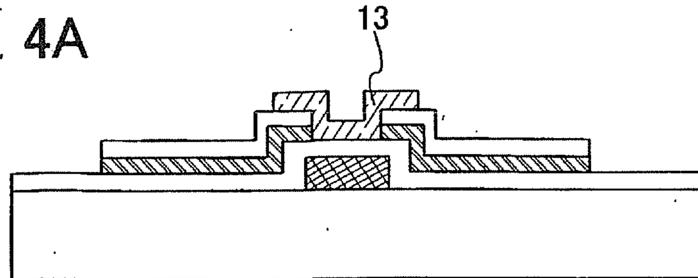


FIG. 4B

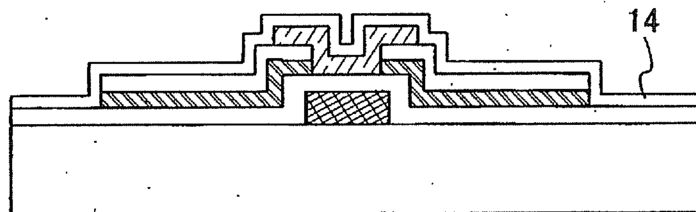


FIG. 5A

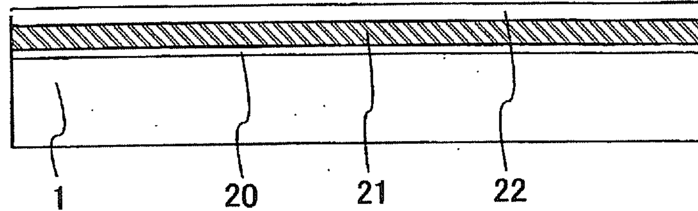


FIG. 5B

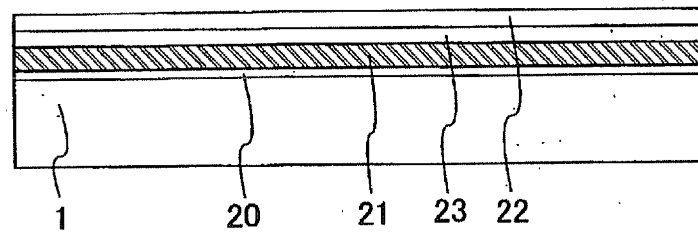


FIG. 5C

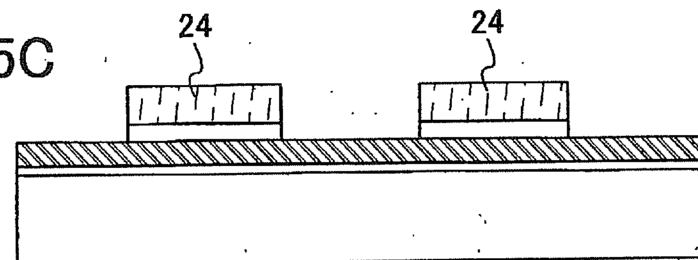


FIG. 5D

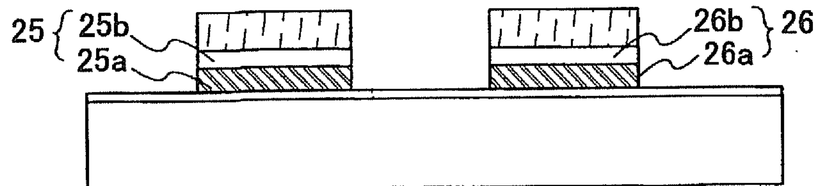


FIG. 6A

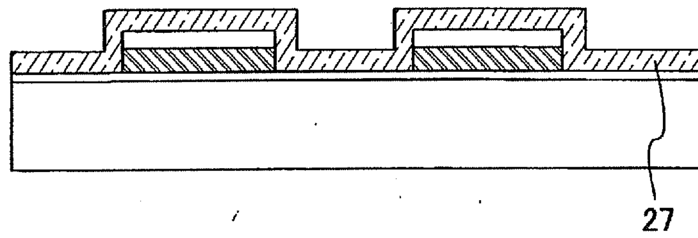


FIG. 6B

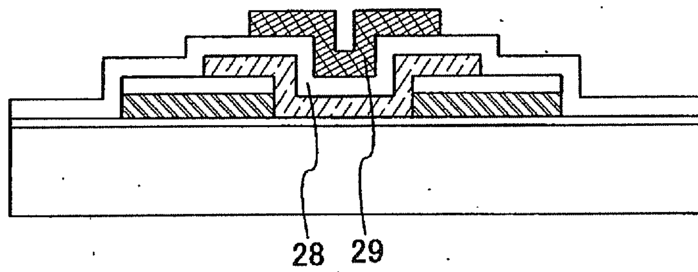


FIG. 6C

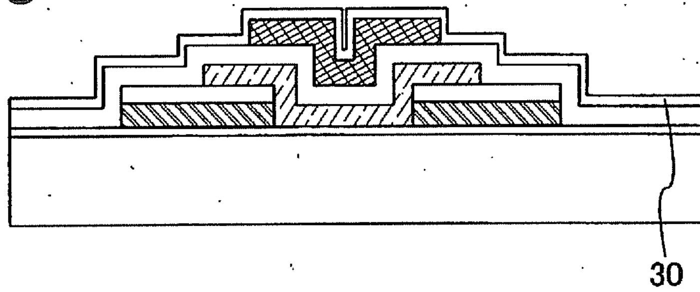


FIG. 7A

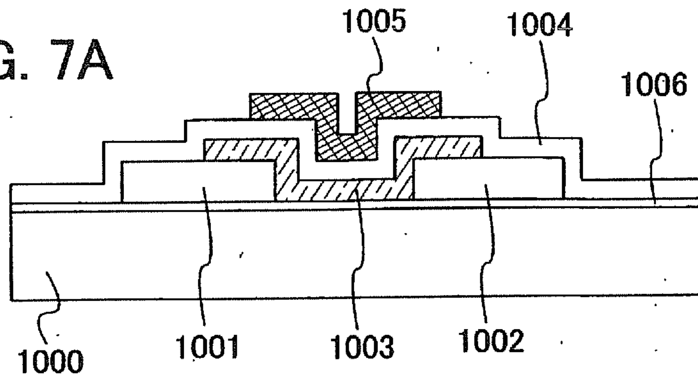
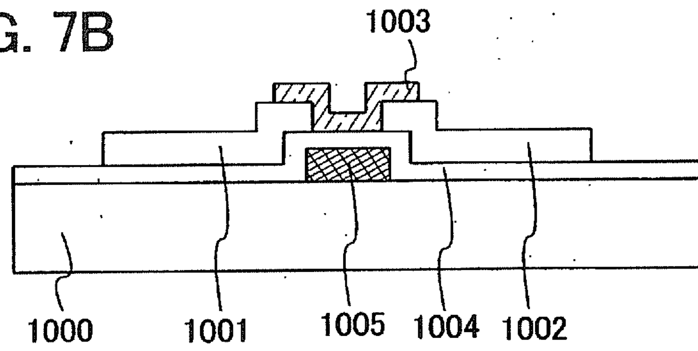


FIG. 7B



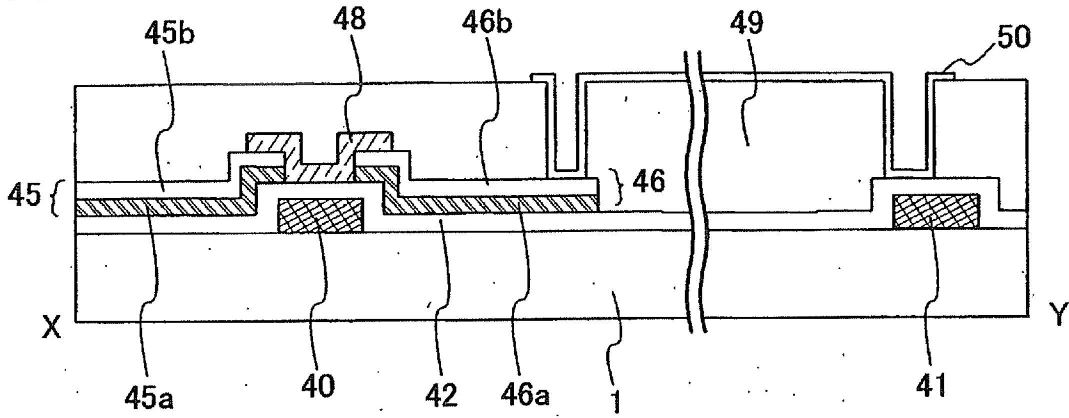


FIG. 8A
45b
48
46b
49
50
45
46
X
Y
45a
40
42
46a
1
41

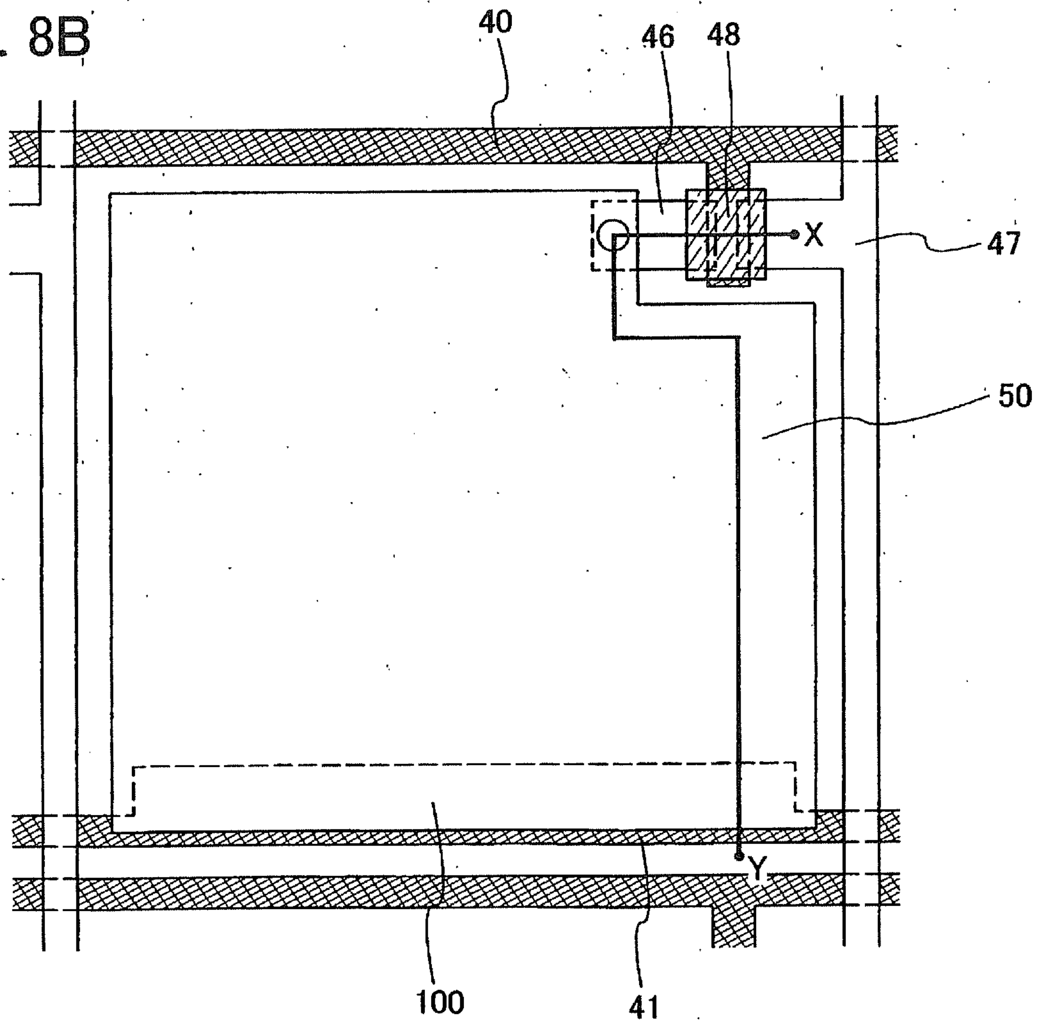


FIG. 8B
40
46
48
X
47
50
Y
100
41

FIG. 9A

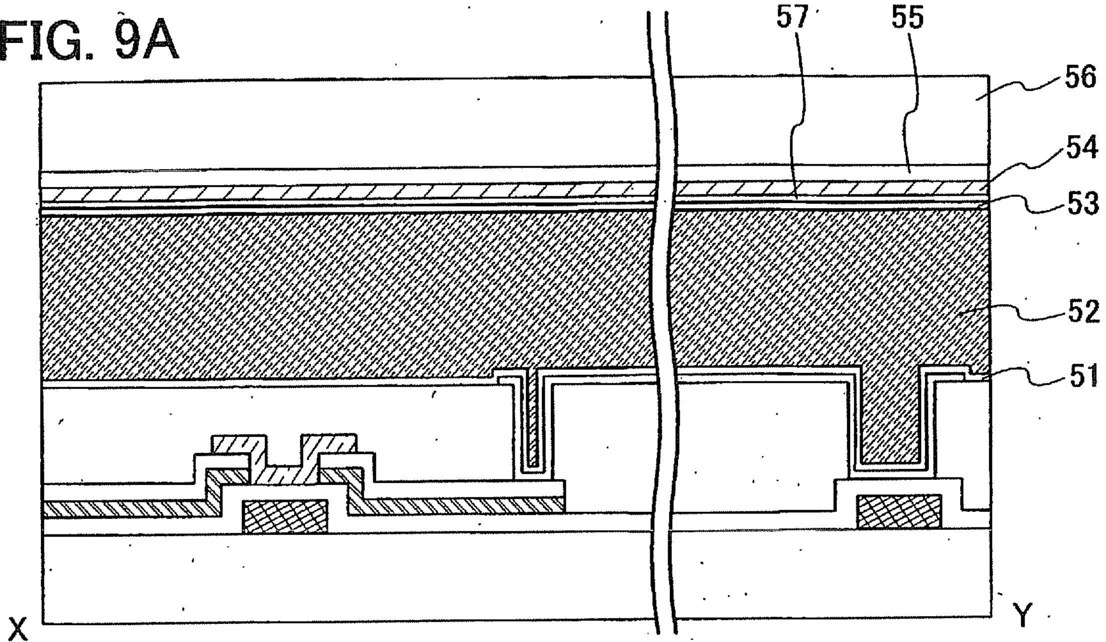


FIG. 9B

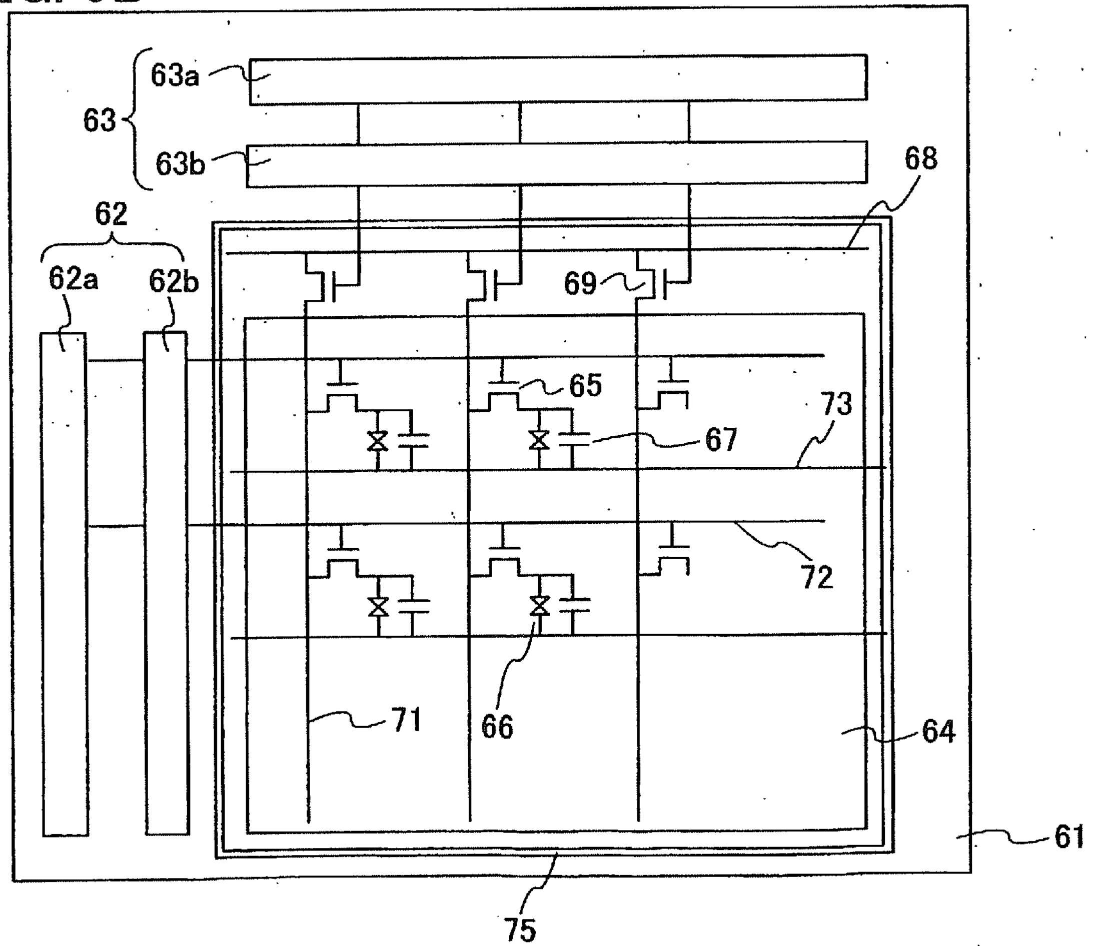


FIG. 10A

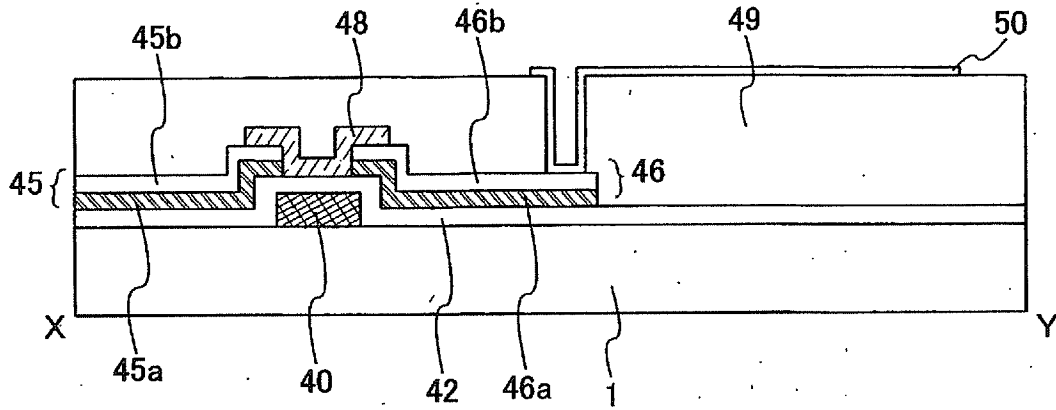


FIG. 10B

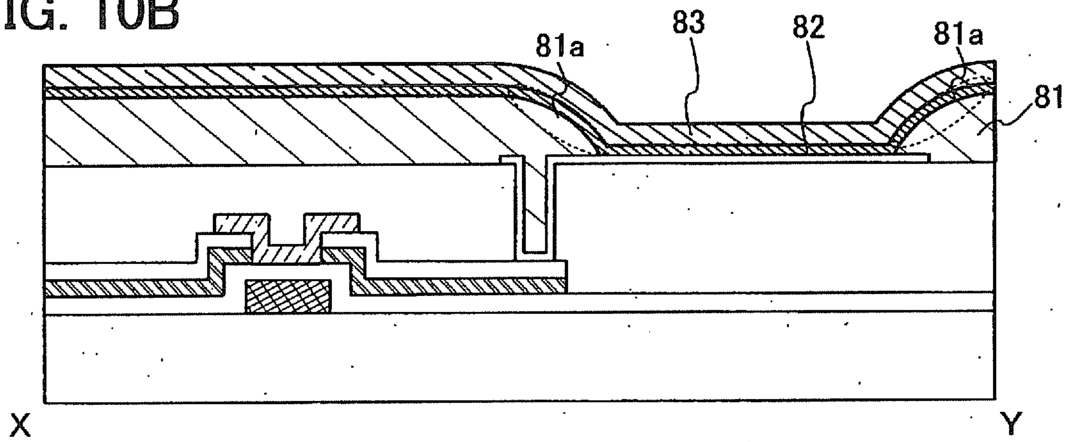


FIG. 11A

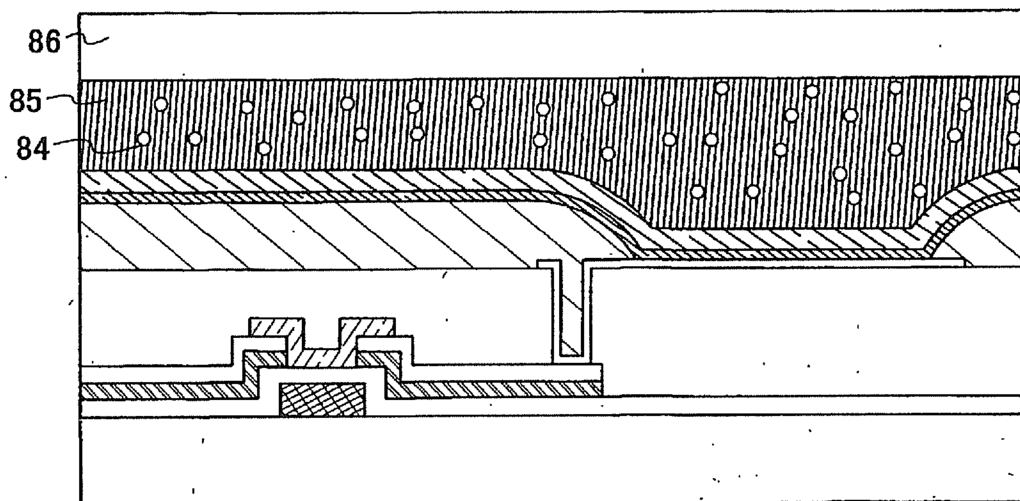


FIG. 11B

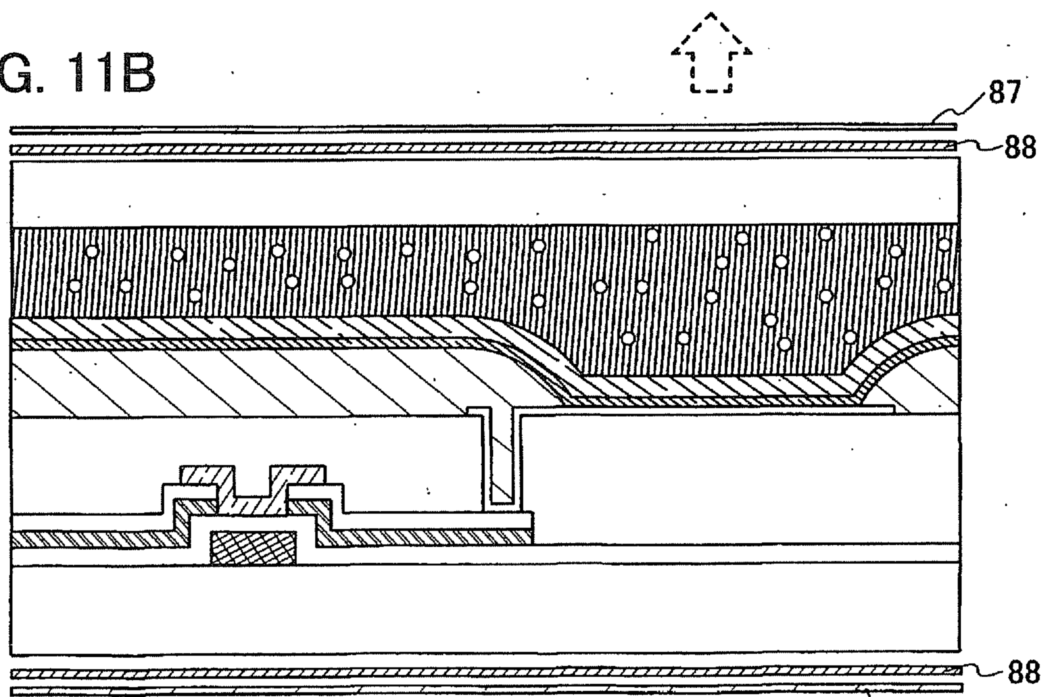


FIG. 12A

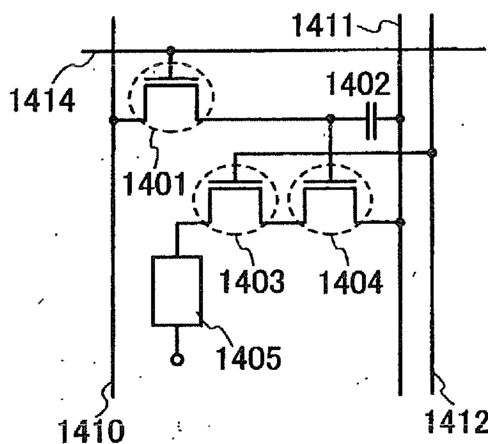


FIG. 12B

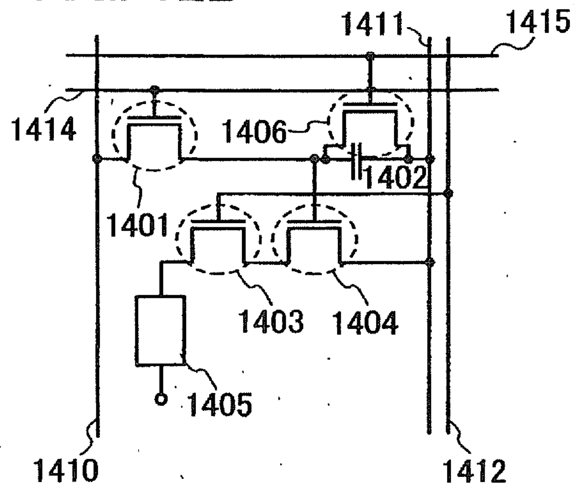


FIG. 12C

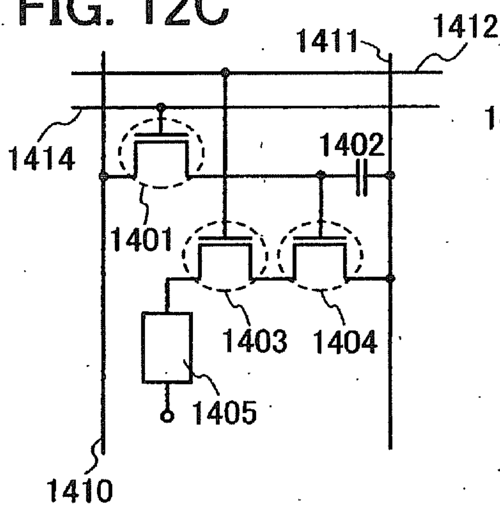


FIG. 12D

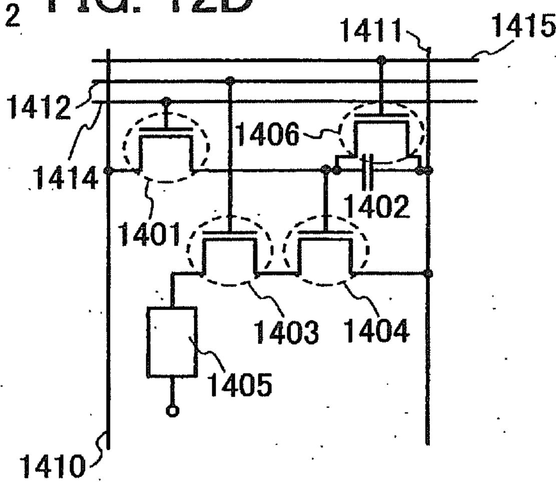


FIG. 12E

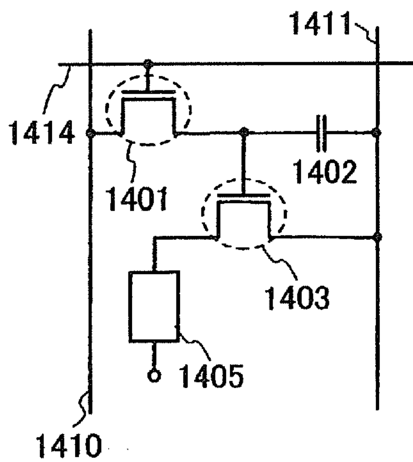


FIG. 12F

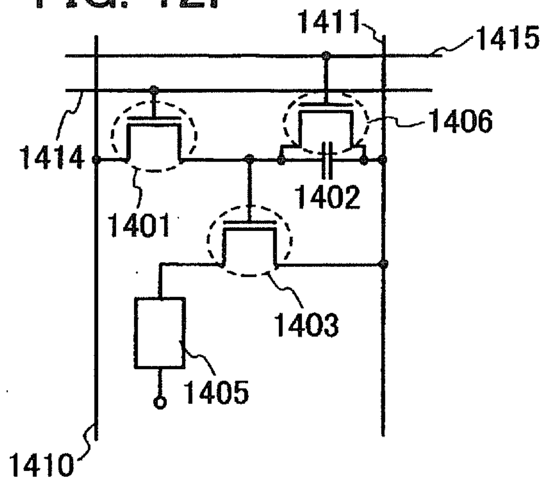


FIG. 13

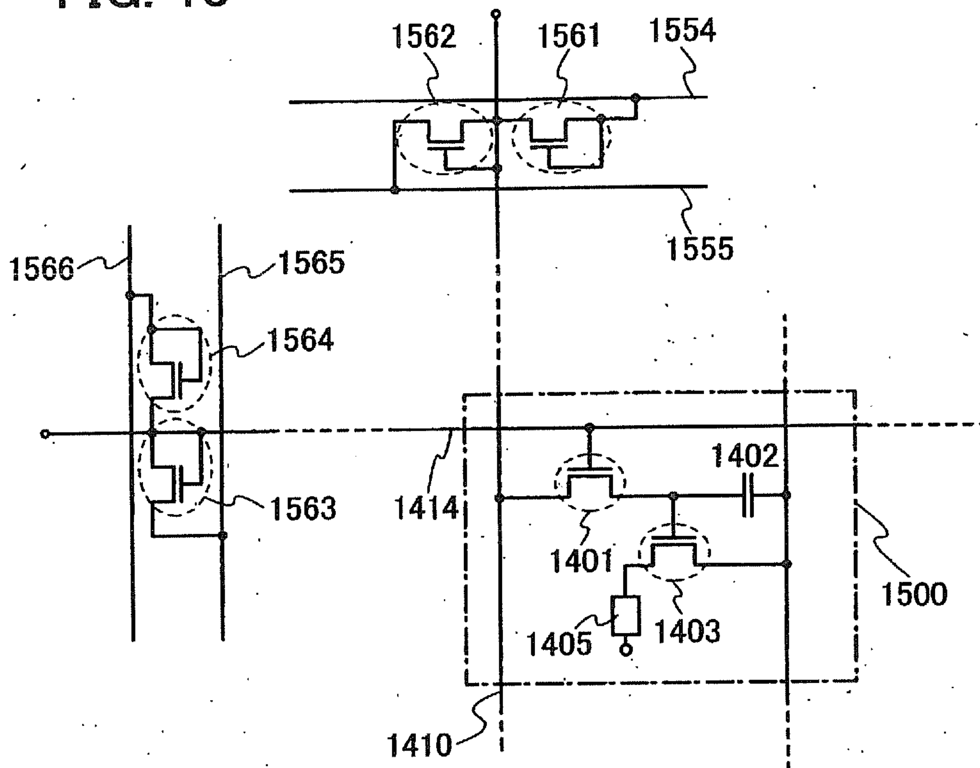


FIG. 14A

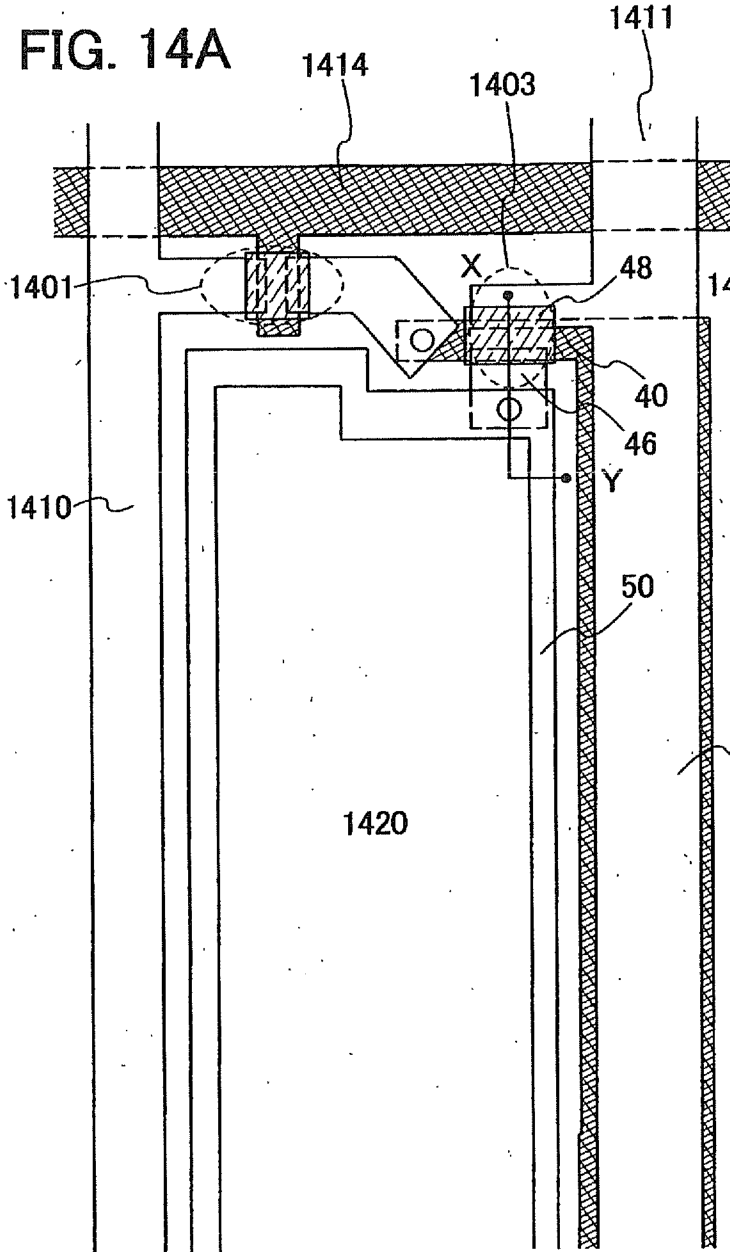


FIG. 14B

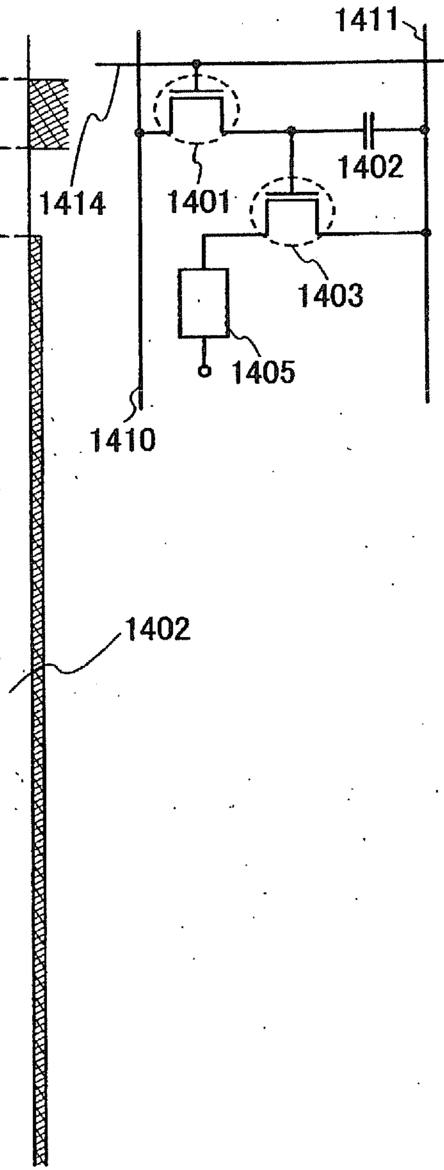


FIG. 15A

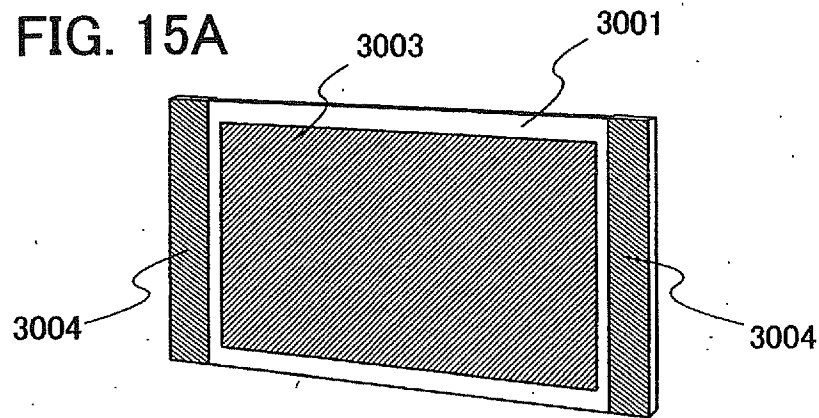


FIG. 15B

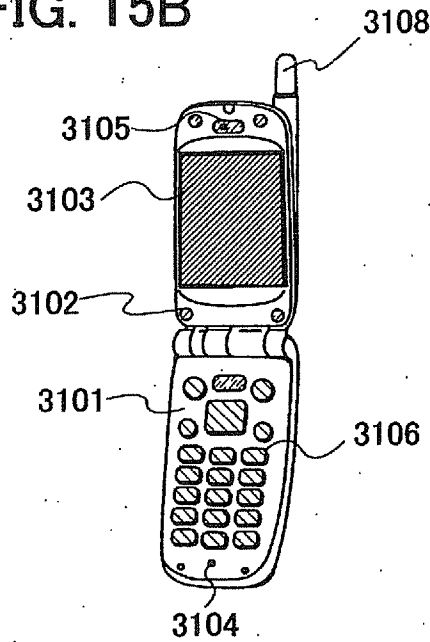


FIG. 15C

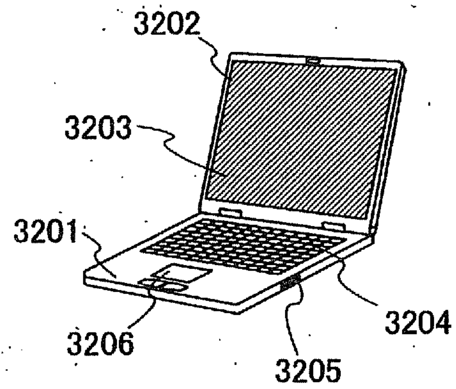


FIG. 15D

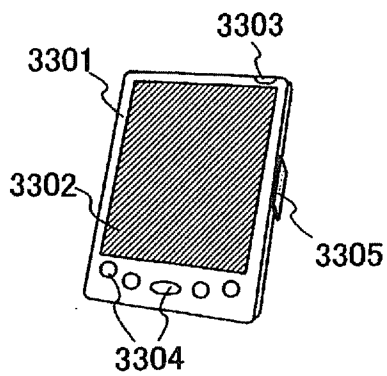


FIG. 15E

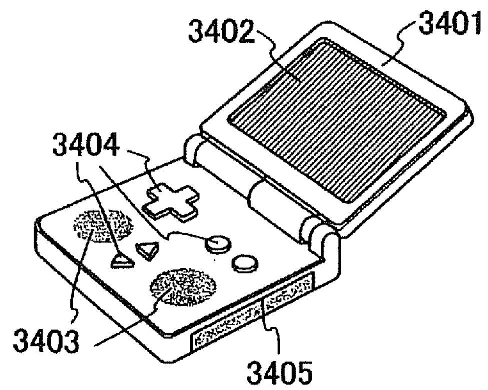
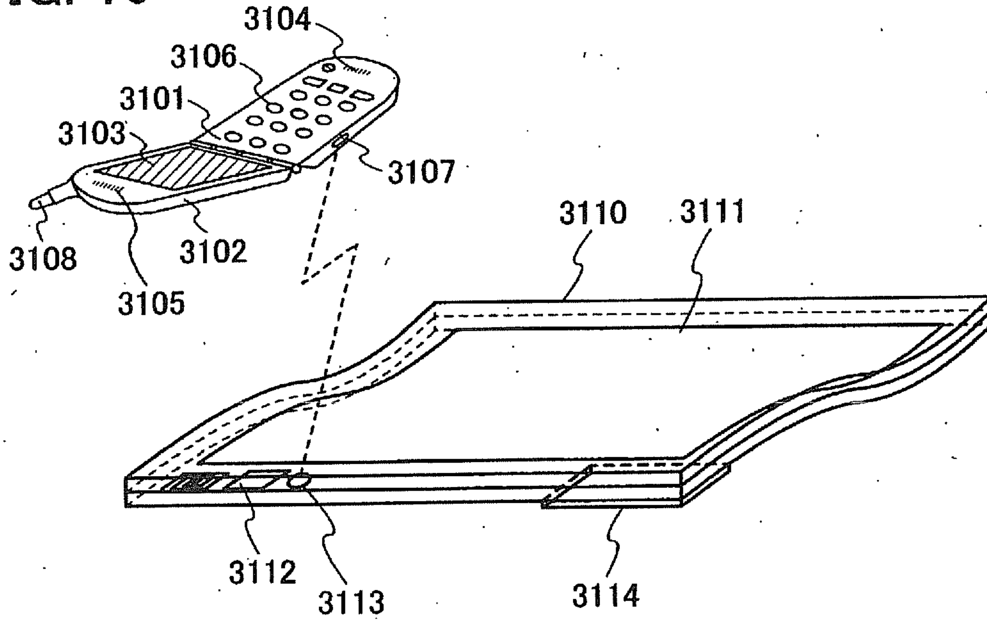


FIG. 16



EXPLANATION OF REFERENCE

1: substrate, 2: insulating film, 3: gate electrode, 5: gate insulating film, 6: first conductive film, 7: second conductive film, 8: third conductive film, 9: resist mask, 10: source electrode, 10a: source electrode, first conductive film, 10b: source electrode, second conductive film, 11: drain electrode, 11a: drain electrode, first conductive film, 11b: drain electrode, second conductive film, 12: semiconductor film, 13: island-like shaped semiconductor film, 14: insulating film, 20: insulating film, 21: first conductive film, 22: second conductive film, 23: third conductive film, 24: resist mask, 25: source electrode, 25a: source electrode, first conductive film, 25b: source electrode, second conductive film, 26: drain electrode, 26a: drain electrode, first conductive film, 26b: drain electrode, second conductive film, 27: semiconductor film, 28: gate insulating film, 29: gate electrode, 30: insulting film, 40: gate electrode, gate wire, 41: auxiliary capacitor wire, 42: gate insulating film, 45: source electrode, 45a: source electrode, 45b: source electrode, 46: drain electrode, 46a: drain electrode, 46b: drain electrode, 47: source wire, 48: semiconductor film, 49: insulating film, 50: pixel electrode, 51: alignment wire, 52: liquid crystal composition, 53: alignment film, 54: protective insulating film, 55: color filter, 56: opposing substrate, 61: substrate, 62: gate wire driver circuit, 62a: shift register, 62b: buffer, 63: source wire driver circuit, 63a: shift register, 63b: buffer, 64: active matrix portion, 65: semiconductor device, 66: liquid crystal portion, 67: auxiliary capacitor, 68: video line, 69: analog switch, 71: source wire, 72: gate wire, 73: auxiliary capacitor wire, 75: sealant, 81: partition wall, 81a: end surface, 82: layer including light-emitting substance, 83: opposing electrode, 84: drying agent, 85: resin, 86: opposing substrate, 87: protective film, 88: polarizing plate, 100: auxiliary capacitor, 1000: substrate, 1001: source electrode, 1002: drain electrode, 1003: semiconductor film, 1004: gate insulating film, 1005: gate electrode, 1006: base film, 1401: switching TFT, 1402: auxiliary capacitor, 1403: driving TFT, 1404: current control TFT, 1405: light-emitting element, 1406: TFT, 1410: signal line, 1411: power source line, 1412: power source line, 1414: scan line, 1415: scan line, 1420: light-emitting region, 1500: pixel portion, 1554: common potential line, 1555: common potential line, 1561: diode, 1562: diode, 1563: diode, 1564: diode, 1565: common potential line, 1566: common potential line, 3001: housing, 3003: display area, 3004: speaker,

3101: main body, 3102: housing, 3102: housing, 3103: display area, 3104: audio input portion, 3105: audio output portion, 3106: operation keys, 3107: infrared communication port, 3108: antenna, 3110: main body, 3111: pixel portion, 3112: driver IC, 3113: receiving device, 3114: film buttery, 3201: main body, 3202: housing, 3203: display area, 3204: keyboard, 3205: external
5 connection port, 3206: pointing mouse, 3301: main body, 3302: display area, 3303: switch, 3304: operation keys, 3305: infrared port, 3401: housing, 3402: display area, 3403: speakers, 3404: operation keys, 3405: recording medium insert portion

10

INTERNATIONALSEARCHREPORT

International application No.
PCT/JP2006/323042

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L21/336(2006.01)i, G02F1/1368(2006.01)i, H01L21/28(2006.01)i, H01L29/786(2006.01)i, H01L51/50(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L21/336, G02F1/1368, H01L21/28, H01L29/786, H01L51/50

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2007
Registered utility model specifications of Japan 1996-2007
Published registered utility model applications of Japan 1994-2007

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 02-226729 A (SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.) 1990.09.10, Fig.4 (Family: none)	1-2

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13.02.2007	27.02.2007

Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office	KAZUNARI TANADA 4L 9361
3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Telephone No. +81-3-3581-1101 Ext. 3498

The "special technical feature" of claims 1-38 relates to "a gate electrode; a gate insulating film over the gate electrode; a first film comprising metal material over the gate insulating film; a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the first film; and a third film comprising the transparent semiconductor material over the second film and the gate insulating film". However, this feature is disclosed in a prior art document JP 02-226729 A(SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.), 1990.09.10., Fig.4. So the feature cannot be a special technical feature. And there exists no special technical feature linking the inventions of claims 1-38 as to form a single general inventive concept among the inventions.

Therefore there is no technical relationship which is considered as "special technical feature"(PCT rule 13.2) among the claims 1-38. So this application contains the following groups of invention which are not so linked as to form a single inventive concept under PCT rule 13.2.

Group 1:Claims 1-2
Group 2:Claim 3
Group 3:Claim 4
Group 4:Claims 5-6
Group 5:Claim 7
Group 6:Claim 8
Group 7:Claims 9-10,15
Group 8:Claim 11
Group 9:Claim 12
Group 10:Claim 13
Group 11:Claim 14
Group 12:Claim 16
Group 13:Claim 17
Group 14:Claim 18
Group 15:Claim 19
Group 16:Claim 20
Group 17:Claim 21
Group 18:Claim 22
Group 19:Claim 23
Group 20:Claims 24-25,30
Group 21:Claim 26
Group 22:Claim 27
Group 23:Claim 28
Group 24:Claim 29
Group 25:Claim 31
Group 26:Claim 32
Group 27:Claim 33
Group 28:Claim 34
Group 29:Claim 35
Group 30:Claim 36
Group 31:Claim 37
Group 32:Claim 38

INTERNATIONALSEARCHREPORT

International application No.
PCT/JP2006/323042

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
Refer to extra sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☑ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-2

Remark on Protest
☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☐ No protest accompanied the payment of additional search fees.

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(25) Filing Language: English

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(30) Priority Data:
2006-26320 2 February 2006 (02.02.2006) JP

(71) Applicants *(for all designated States except US)*: **KOCHI INDUSTRIAL PROMOTION CENTER** [JP/JP]; 3992-2, Nunoshida, Kochi-shi, Kochi 781-5101 (JP). **CASIO COMPUTER CO., LTD.** [JP/JP]; 6-2, Hon-machi 1-chome, Shibuya-ku, Tokyo 151-8543 (JP).

(72) Inventors; and

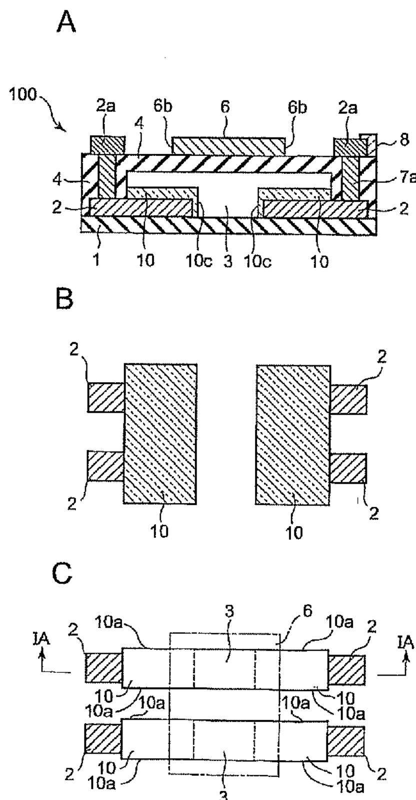
(75) Inventors/Applicants *(for US only)*: **FURUTA, Mamoru** [JP/JP]; c/o Kochi Industrial Promotion Center, 3992-2, Nunoshida, Kochi-shi, Kochi 781-5101 (JP). **HIRAO, Takashi** [JP/JP]; c/o Kochi Industrial Promotion Center 3992-2, Nunoshida, Kochi-shi, Kochi 781-5101 (JP). **FURUTA, Hiroshi** [JP/JP]; c/o Kochi Industrial Promotion Center, 3992-2, Nunoshida, Kochi-shi, Kochi 781-5101 (JP). **MATSUDA, Tokiyoshi** [JP/JP]; c/o Kochi Industrial Promotion Center, 3992-2, Nunoshida, Kochi-shi, Kochi 781-5101 (JP). **HIRAMATSU, Takahiro** [JP/JP]; c/o Kochi Industrial Promotion Center, 3992-2, Nunoshida, Kochi-shi, Kochi 781-5101 (JP). **ISHII, Hiromitsu** [JP/JP]; c/o Casio Computer Co., Ltd., Hamura R & D Center, 2-1, Sakae-cho 3-chome, Hamura-shi, Tokyo 205-8555 (JP). **HOKARI, Hitoshi** [JP/JP]; c/o Casio Computer Co., Ltd., Hamura R & D Center, 2-1, Sakae-cho 3-chome, Hamura-shi, Tokyo 205-8555 (JP). **YOSHIDA, Motohiko** [JP/JP]; c/o Casio Computer Co., Ltd. Hamura R & D Center, 2-1, Sakae-cho 3-chome, Hamura-shi, Tokyo 205-8555 (JP).

(74) Agent: **KIYOHARA, Yoshihiro**; 1-3, Dojimahama 2-chome, Kita-ku, Osaka-shi, Osaka 5300004 (JP).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM,

[Continued on next page]

(54) Title: THIN FILM TRANSISTOR AND MANUFACTURING METHOD THEREOF



(57) Abstract: A thin film transistor includes a substrate (1, 11), and a pair of source/drain electrodes (2, 14) (i.e., a source electrode and a drain electrode) formed on the substrate and defining a gap therebetween. A pair of low resistance conductive thin films (10, 20) are provided such that each coats at least a part of one of the source/drain electrodes. The low resistance conductive thin films define a gap therebetween. An oxide semiconductor thin film layer (3, 15) is continuously formed on upper surfaces of the pair of low resistance conductive thin films and extends along the gap defined between the low resistance conductive thin films so as to function as a channel. Side surfaces of the oxide semiconductor thin film layer and corresponding side surfaces of the low resistance conductive thin films coincide with each other in a channel width direction of the channel.

WO 2007/089048 A2

AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

DESCRIPTION

THIN FILM TRANSISTOR AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS

5 This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2006-26320, filed on February 2, 2006, the entire contents of which are incorporated herein by reference.

10 BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a thin film transistor and the manufacturing method thereof, and particularly to a thin film transistor including an oxide semiconductor thin film layer and a manufacturing 15 method thereof.

Description of the Background Art

It has been known for many years that oxides such as zinc oxide or magnesium zinc oxide have excellent characteristics as a semiconductor (an 20 active layer). In recent years, active research and development of a semiconductor thin film layer using these compounds have been made in order to apply such a semiconductor thin film layer to electronic devices such as a thin film transistor (hereinafter abbreviated as TFT), a light emitting device, and a transparent conductive film.

25 An oxide TFT including a semiconductor thin film layer made of zinc oxide or magnesium zinc oxide has greater electron mobility and better TFT

characteristics than an amorphous silicon TFT including a semiconductor thin film layer of amorphous silicon (a-Si: H), which has been mainly used for liquid crystal displays. Another advantage of the oxide TFTs is that high electron mobility can be expected because a crystalline thin film is formed even at a temperature as low as a room temperature. These advantages have been encouraging the development of the oxide TFTs.

TFTs using an oxide semiconductor thin film layer, such as a bottom gate type TFT (See, for example, Japanese Patent Publication No. 2005-033172 and No. 2004-349583) and a top gate type TFT, have been reported.

The bottom gate type TFTs include, for example, a lamination of a gate electrode disposed over a substrate, a gate insulating film, source/drain electrodes, and an oxide semiconductor thin film layer, which are laminated in this order.

On the other hand, the top gate type TFTs, for example, include a lamination of source/drain electrodes disposed over a substrate, an oxide semiconductor thin film layer, a gate insulating film, and a gate electrode, which are laminated in this order.

In both of the bottom and top gate type TFTs, sufficient contact is required between each of the source/drain electrodes and the oxide semiconductor thin film layer primarily comprising zinc oxide in order to ensure high current drive power.

In a conventional method, a source/drain region having lower resistance than the oxide semiconductor thin film layer is provided to improve the contact property between the source/drain electrodes and the oxide semiconductor thin film layer.

Fig. 9A shows a TFT (500) as one example of the TFTs provided according to the conventional method. The TFT (500) has a pair of low resistance conductive thin films (110) sandwiched between the oxide semiconductor thin film layer (103) and a pair of source/drain electrodes (102) placed on a substrate (101). Since the low resistance conductive thin films (110) have a lower resistance than the oxide semiconductor thin film layer (103), they improve the contact between each of the source/drain electrodes (102) and the oxide semiconductor thin film layer (103). The oxide semiconductor thin film layer (103) is disposed on the low resistance conductive thin films (110) and on an area of the substrate (101) exposed between the pair of the low resistance conductive thin films (110), while the outer periphery (110a) (See Fig. 9B (described below) for a plan view) of the low resistance conductive thin films (110) remains uncovered. All the exposed surfaces of the oxide semiconductor thin film layer (103) are covered with a gate insulating film (104). A gate electrode (106) is disposed over the gate insulating film (104). Fig. 9B is a plan view of an array of the TFTs (500) shown in Fig. 9A. In Fig. 9B, two of the TFTs (500) are aligned in parallel. Fig. 9A is a cross sectional view along line IXA-IXA of Fig. 9B. For clarity, Fig. 9B omits gate insulating film 104 shown in Fig. 9A.

In manufacturing the TFT (500), first a pair of source/drain electrodes (102) is patterned and then the low resistance conductive thin film (110) is formed. The low resistance conductive thin film (110) is separated into a plurality of low resistance conductive thin films (110) that are spaced apart from each other, using a photo-lithography technique. Accordingly, an outer periphery (110a) (cross-hatched in Fig. 9B) of the low resistance conductive thin films (110) protrudes from the outer profile of the

oxide semiconductor thin film layer (103). As shown in Fig. 9B, at least a distance D (distance D = width A + gap B + width A) is needed between the oxide semiconductor thin film layers of the TFTs. Narrower distance D is preferable in order to achieve higher integration of TFTs. The width A is defined by the mask-alignment accuracy of an aligner, in other words, by the alignment accuracy in the photo-lithography of the low resistance conductive thin film (110) and the oxide semiconductor thin film layer (103). The higher the alignment accuracy is, the smaller the width A becomes. On the other hand, the gap B is defined by the minimum resolution during the patterning of the low resistance conductive thin film (110). The higher the minimum resolution is, the smaller the gap B becomes. When a conventional aligner for an LCD is used, the width A determined by the alignment accuracy, is about 1.5 μm, and the gap B determined by the minimum resolution is about 4.0 μm. Therefore in the conventional TFT 500, the distance D between the oxide semiconductor thin film layer 103 is approximately 7.0 μm (1.5 μm + 4.0 μm +1.5 μm) (see Fig. 9B).

On the other hand, in manufacturing a TFT that includes no low resistance conductive thin film, an oxide semiconductor thin film layer is laid over the source/drain electrodes of a plurality of TFTs, and then the oxide semiconductor thin film layer is patterned. Therefore, the width A required in TFT (500) according to the mask-alignment accuracy is not necessary. Thus the width A is eliminated from the distance D so that the distance D includes only the gap B.

As mentioned above, for TFTs including no low resistance conductive thin film, the minimum distance D between the adjacent oxide semiconductor thin film layers is equal to the gap B, whereas, for TFTs (e.g.

TFT (500)) including the low resistance conductive thin film, the minimum distance D between the oxide semiconductor thin film layers is equal to the sum of width A , gap B, and width A (width A + gap B + width A). In other words, in the TFTs (e.g. TFT (500)) including the low resistance conductive
5 thin film for improving the contact properties, the low resistance conductive thin film (110) forces the gap between the oxide semiconductor thin film layers to be wider, which results in difficulty in achieving a high integration of the TFTs.

10 SUMMARY OF THE INVENTION

Considering the above-mentioned problems, one object of the present invention is to decrease the distance D between oxide semiconductor thin film layers by eliminating the width A so as to increase a degree of integration of the thin film transistors.

15 According to one aspect of the presnet invention, a thin film transistor includes a substrate, and a pair of source/drain electrodes (i.e., a source electrode and a drain electrode) formed on the substrate and defining a gap therebetween. A pair of low resistance conductive thin films are provided such that each coats at least a part of one of the source/drain
20 electrodes. The low resistance conductive thin films define a gap therebetween. An oxide semiconductor thin film layer is continuously formed on upper surfaces of the par of low resistance conductive thin films and extends along the gap defined between the low resistnace conductive thin films so as to function as a channel. Side surfaces of the oxide
25 semiconductor thin film layer and corresponding side surfaces of the low resistance conductive thin films coincide with each other in a channel width

direction of the channel.

The manufacturing method of the thin film transistor according to one aspect of the present invention includes forming a pair of source/drain electrodes on a substrate; forming low resistance conductive thin films, which are made of an oxide, on the source/drain electrodes; and forming an oxide semiconductor thin film layer, which functions as a channel, along the gap defined between the low resistance conductive thin films and on the upper surfaces of the low resistance conductive thin films. The low resistance conductive thin films and the oxide semiconductor thin film layer are etched so that side surfaces of the oxide semiconductor thin film layer and corresponding side surfaces of the low resistance conductive thin films coincide with each other in a channel width direction of the channel.

BRIEF DESCRIPTION OF THE DRAWINGS

Further features and advantages of the present invention will become apparent from the following detailed description, taken in combination with the accompanying drawings.

Figs. 1A to 1C show the thin film transistor of the first embodiment of the present invention. Fig. 1A is a cross-sectional view of the thin film transistor of the present invention along line IA-IA in Fig. 1C; Fig. 1B is a plan view of the layout of the thin film transistor according to the first embodiment after forming source/drain electrodes and low resistance conductive thin films; and Fig. 1C is a plan view of the layout of the thin film transistor according to the first embodiment.

Figs. 2A to 2D are cross-sectional views showing steps of the manufacturing method of the thin film transistor according to the first

embodiment of the present invention. Fig. 2A is a cross-sectional view of the thin film transistor according to the first embodiment after forming the source/drain electrodes and the low resistance conductive thin films on the substrate; Fig. 2B is a cross-sectional view of the thin film transistor according to the first embodiment after coating the oxide semiconductor thin film layer; Fig. 2C is a cross-sectional view of the thin film transistor according to the first embodiment after performing etching; Fig. 2D is a cross-sectional view of the thin film transistor according to the first embodiment after laminating the gate insulating film and a gate electrode; and Fig. 2E is a cross-sectional view after laminating contact parts, external source/drain electrodes, and a display electrode.

Fig. 3 is a cross-sectional view of the thin film transistor according to the second embodiment of the present invention.

Figs. 4A to 4D are cross-sectional views showing steps of the manufacturing method of the thin film transistor according to the second embodiment of the present invention. Fig. 4A is a cross-sectional view of the thin film transistor according to the second embodiment after forming the source/drain electrodes, the low resistance conductive thin films and the oxide semiconductor thin film layer on the substrate; Fig. 4B is a cross-sectional view of the thin film transistor according to the second embodiment after forming the first insulating film; Fig. 4C is a cross-sectional view of the thin film transistor according to the second embodiment after performing etching; and Fig. 4D is a cross-sectional view of the thin film transistor according to the second embodiment after laminating the second gate insulating film and the gate electrode. Fig. 5 is a cross-sectional view of the thin film transistor according to the third

embodiment of the present invention.

Figs. 6A to 6D are cross-sectional views showing steps of the manufacturing method of the thin film transistor according to the third embodiment of the present invention. Fig. 6A is a cross-sectional view of the thin film transistor according to the third embodiment after forming the gate electrode and the gate insulating film on the substrate; Fig. 6B is a cross-sectional view of the thin film transistor according to the third embodiment after forming the source/drain electrodes, the low resistance conductive thin films, and the oxide semiconductor thin film layer; Fig. 6C is a cross-sectional view of the thin film transistor according to the third embodiment after performing etching; and Fig. 6D is a cross-sectional view after forming an overcoat insulating film.

Fig. 7 is a cross-sectional view of the thin film transistor according to the fourth embodiment of the present invention.

Figs. 8A to 8D are cross-sectional views showing steps of the manufacturing method of the thin film transistor according to the fourth embodiment of the present invention. Fig. 8A is a cross-sectional view of the thin film transistor according to the fourth embodiment after forming the gate electrode and the gate insulating film on the substrate; Fig. 8B is a cross-sectional view of the thin film transistor according to the fourth embodiment after forming the source/drain electrodes, the low resistance conductive thin films, the oxide semiconductor thin film layer, and the first overcoat insulating film; Fig. 8C is a cross-sectional view of the thin film transistor according to the fourth embodiment after performing etching; and Fig. 8D is a cross-sectional view of the thin film transistor according to the fourth embodiment after forming the second overcoat insulating film.

Fig. 9 shows one example of a conventional thin-film transistor. Fig. A is a cross-sectional viewalong line IXA-IXA in Fig. 9B; and Fig. 9B is a plan view of the layout of the conventional thin film transistor of Fig. 9A.

5

DETAILED DESCRIPTION

Figs. 1A-1C are views of the TFT (100) according to the first embodiment of the present invention. Fig. 1A is a cross-sectional view along line IA-IA of Fig. 1C. Fig. 1B shows the TFTs (100) at a stage of manufacturing after formation of the source/drain electrodes and low
10 resistance conductive thin films and before coating the TFTs (100) with an oxide semiconductor thin film layer. In Fig. 1B a plurality (two in the figure) of the TFTs (100) are aligned in parallel for integration. Fig. 1C is a plan view for describing the subsequent processes. Hereinafter, the first embodiment of the present invention will be described referring mainly to
15 Fig. 1A, as well as Fig. 1B and Fig. 1C.

"Channel length direction" as used herein refers to the direction perpendicular to the channel width. The channel length direction is the right-to-left direction in Fig. 1A. "Channel width direction" as used herein refers to the up-and-down direction in Fig. 1C.

20 A thin film transistor (100) according to the first embodiment of the present invention includes a substrate (1), a pair of source/drain electrodes (2), a pair of low resistance conductive thin films (10), an oxide semiconductor thin film layer (3), a gate insulating film (4), a gate electrode (6), contact parts (7a), a pair of external source/drain electrodes (2a), and a
25 display electrode (8), which are laminated in the order shown in Fig. 1A.

The thin film transistor (100), as shown in Fig. 1A, is formed on a

substrate (1) made of glass (non-alkali glass primarily comprising SiO_2 and Al_2O_3). The material for the substrate (1) is not limited to glass, and other insulating materials, such as plastics covered with an insulator and metal foils covered with an insulator, are applicable to form the substrate 1 according to the present invention.

The pair of the source/drain electrodes (2) is laminated on the upper surface of the substrate (1). The source/drain electrodes (2) include a source electrode and a drain electrode that are spaced apart from each other.

The source/drain electrodes (2) are made of metal. Conductive oxides, such as indium tin oxide (ITO) and n+ZnO, which are generally used as source/drain electrodes, are preferably not used in the source/drain electrode (2) of the present invention because a conductive oxide such as ITO or n+ZnO would be etched when the oxide semiconductor thin film layer and low resistance conductive thin films are etched.

The length in the channel width direction (the up-and-down direction in Fig. 1C) of the source/drain electrodes (2) is preferably equal to or smaller than the length of the oxide semiconductor thin film layer (3) in the channel width direction. If the length of the source/drain electrodes (2) in the channel width direction is larger than the length of the oxide semiconductor thin film layer (3) in the channel width direction, it prevents high integration of the thin film transistors when a plurality of TFTs are integrated as shown in Fig. 1C.

The source/drain electrodes (2) may be formed as a monolayer of Ti, Cr, Ta, Mo, W, Al, Cu, and Ni or as a lamination of two or more of these materials, or as an alloy containing one or more of Ti, Cr, Ta, Mo, W, Al, Cu,

Si and Ni. Specific examples of the alloy include, for example, TiW, TaW, MoW, MoSi, AlCu, AlSi, and NiSi.

The thickness of the source/drain electrodes (2) may be, for example, though not limited to, 30 to 150 nm (in the hight direction of the layer of the source/drain electrodes 2 corresponding to the up-and-down direction of Fig. 1).

The low resistance conductive thin films (10) are formed on the pair of source/drain electrodes (2) in the manner shown in Fig. 1B. The low resistance conductive thin films (10) may be, for example, a thin film primarily comprising indium tin oxide (ITO); or zinc oxide doped with gallium (Ga) or aluminum (Al); or the like. If the oxide semiconductor thin film layer 3 primarily comprises zinc oxide the low resistance conductive thin films 10 may be made of intrinsic zinc oxide (ZnO) with no impurity introduced. When the low resistance conductive thin films 10 are made of intrinsic zinc oxide with no impurities introduced, the zinc oxide in the low resistance conductive thin films (10) must have larger crystal grain size than the zinc oxide in the oxide semiconductor thin film layer (3). The crystal grain size of the zinc oxide may be adjusted by applying high frequency bias during film formation or by changing film forming conditions during the film formation.

The resistance of the low resistance conductive thin films (10) is higher than the resistance of the source/drain electrodes (2) and lower than that of the oxide semiconductor thin film layer (3). Therefore, the contact properties between the source/drain electrodes (2) and the oxide semiconductor thin film layer (3) are improved by using the low resistance conductive thin films (10).

The oxide semiconductor thin film layer (3), which is formed by an oxide semiconductor, is arranged so that a channel is formed on each of the low resistance conductive thin films (10) and between the pair of the source/drain electrodes (2). The oxide semiconductor thin film layer 3 may be an oxide semiconductor primarily comprising zinc oxide. As used herein, an oxide semiconductor primarily comprising zinc oxide includes intrinsic zinc oxide; zinc oxide doped with a p-type dopant such as Li, Na, N, C; zinc oxide doped with an n-type dopant such as B, Al, Ga, In; and zinc oxide doped with Mg, Be. The oxide semiconductor thin film layer 3 may be an amorphous oxide semiconductor, such as an IGZO (In-Ga-Zn-O).

The oxide semiconductor thin film layer (3) covers the entire upper surfaces of each of the low resistance conductive thin films (10). At least side surfaces (10a) (see Fig. 1C) of the low resistance conductive thin films (10), extending in the channel length direction, are positioned coincident with the side surfaces of the oxide semiconductor thin film layer (3).

The thickness of the oxide semiconductor thin film layer (3) may be, for example, though not limited to, about 25 to 200 nm, and preferably about 50 to 100 nm (in the height direction of the layer of the source/drain electrodes 2, corresponding to the up-and-down direction of Fig. 1).

In the present invention, the low resistance conductive thin films (10) and the oxide semiconductor thin film layer (3) are formed in a self-aligning manner in the channel width direction, as shown in Fig. 1C, so that the low resistance conductive thin films (10) below the oxide semiconductor thin film layer (3) are not seen when viewed from above. In other words, the entire upper surfaces of the low resistance conductive thin films (10) are coated with the oxide semiconductor thin film layer (3).

Consequently, the space provided between the adjacent oxide semiconductor thin films (3) according to the accuracy of mask alignment between the low resistance conductive thin films (10) and the oxide semiconductor thin film layer (3) (width A described above with respect to Fig. 9B) is not necessary.
5 Therefore, it is possible to shorten the distance (spacing) between the low resistance conductive thin films (10) to the minimum line width of the aligner (gap B described above with respect to Fig. 9B) and this enables high integration of the thin film transistors (100).

A specific comparison between the conventional TFT (500) (see Fig.
10 9) and the TFT (100) according to the first embodiment of the present invention is set forth below.

As mentioned above, the TFT (500) is fabricated by patterning the low resistance conductive thin films (110) on each TFT and then forming the oxide semiconductor thin film layers (103). Consequently, the distance
15 (spacing) between the oxide semiconductor thin film layers (103) is defined as gap B + 2 × width A (here the gap B is the width of an area determined by the minimum resolution: and the width A is the width of an area determined by the alignment accuracy of the photolithography of the low resistance conductive thin film (110) and the oxide semiconductor thin film layer (103)).
20 As explained above with respect to Fig. 9B, when a conventional aligner for an LCD is used, the width A determined by the alignment accuracy, is about 1.5 μm, and the gap B determined by the minimum resolution is about 4.0 μm. Therefore, in the conventional TFT (500), the distance D between the oxide semiconductor thin film layers (103) is approximately 7.0 μm (1.5 μm
25 + 4.0 μm +1.5 μm) (see Fig. 9B).

On the other hand, in manufacturing the TFT (100) according to the

present invention, the low resistance conductive thin films (10) are formed on multiple pairs of the source/drain electrodes (2) (two pairs in the example shown in Fig. 1B) of the TFTs (100) as shown in Fig. 1B. Then the oxide semiconductor thin film layer (3) is coated on the low resistance conductive thin films (10). The oxide semiconductor thin film layer (3) and the low resistance conductive thin films (10) are subsequently etched together in a self-aligning manner so that the side surfaces (10a) of the low resistance conductive thin films (10) have an identical shape to the side surfaces of the oxide semiconductor thin film layer (3) so that the side surfaces of the low resistance conductive thin films (10) and the oxide semiconductor thin film layer (3) are positioned coincident with each other. Therefore, although the width A, which is determined by the alignment accuracy, is necessary in the conventional TFT (500), the width A is not necessary in the TFT (100) of the present invention. The distance between the adjacent oxide semiconductor thin film layers (3) of the TFT (100) may be reduced to be equal to the gap B (4.0 µm), which is determined by the minimum resolution. Consequently, the TFT (100) according to the present invention enables nearly twice as high integration as the conventional TFT (500).

The gate insulating film (4) is formed so as to cover the upper surface and the side surfaces of the oxide semiconductor thin film layer (3).

The gate insulating film (4) may be a silicon oxide (SiO_x) film, a silicon oxide nitride (SiON) film, a silicon nitride (SiN_x) film, or a silicon nitride (SiN_x) film that is doped with oxygen using oxygen or a compound containing oxygen. Preferably, the gate insulating film (4) is formed by a silicon nitride (SiN_x) film that is doped with oxygen using oxygen or compound (e.g. N_2O) containing oxygen. Such a doped silicon nitride film

has a higher dielectric constant than silicon oxide compound (SiO_x) or silicon oxide nitride (SiON). Therefore, if the TFT (100) has a the gate insulating film (4) made of a SiN_x film doped with oxygen, the gate insulating film has a high dielectric constant and an excellent protecting effect on the oxide semiconductor thin film layer 3.

The gate electrode (6) is formed on the gate insulating film (4). The gate electrode (6) is configured to control electron density in the oxide semiconductor thin film layer (3) according to the gate voltages applied to the thin film transistor. The gate electrode (6) is made of a metal film such as films comprising Cr or Ti.

Along the channel length direction, the outer ends (6b) of the gate electrode (6) are positioned outside the inner ends 10c of the low resistance conductive thin films (10).

Each of the external source/drain electrodes (2a) is connected to the corresponding source/drain electrodes (2) via the contact part (7a).

The display electrode (8) is configured to apply a voltage to a liquid crystal in a liquid crystal display via the thin film transistor. The display electrode (8) is formed by a conductive oxide thin film such as an indium tin oxide (ITO) thin film and the like because it must have high transmittance with respect to visible light.

Referring to Figs. 2A-2E, a manufacturing method of a thin film transistor (TFT) according to the first embodiment of the present invention will be described.

First, as shown in Fig. 2A, the source/drain electrodes (2) are formed on the substrate (1). In the case a plurality of TFTs are arranged in parallel on the substrate (1), the corresponding number of pairs of the

source/drain electrodes (2) are patterned, as shown in Fig. 1B (which shows two pairs of source/drain electrodes 2 corresponding to two TFTs). Next, the low resistance conductive thin film (10) having, for example, a 10 to 100 nm thickness is coated on the source/drain electrodes (2) and the substrate (1) by means of magnetron sputtering. The low resistance conductive thin film (10) is then patterned as shown in Fig. 1B. In the patterning, the low resistance conductive thin film (10) is etched in an area (channel-corresponding area) that corresponds to the gap extending between the source electrodes and the drain electrodes. The resultant low resistance conductive thin film (10) is separated into a first low resistance conductive thin film piece and a second low resistance conductive thin film piece. The first low resistance conductive thin film piece bridges one of the source electrodes and the drain electrodes of the plurality of the TFTs (e.g., the source electrodes), while the second low resistance conductive thin film piece bridges the other of the source electrodes and the drain electrodes of the plurality of the TFTs (e.g., the drain electrodes).

At this stage, the low resistance conductive thin films (10) are shaped to extend longer in the channel length direction than the final shape of the low resistance conductive thin films (10). The outer ends of the low resistance conductive thin films (10) are then etched together with the oxide semiconductor thin film layer (3) that is formed thereon so that the outer ends of the low resistance conductive thin films (10) and the oxide semiconductor thin film layer (3) have an identical shape, as described below.

As shown in Fig. 2B, the oxide semiconductor thin film layer (3) is coated on all the exposed surfaces of the substrate (1), the source/drain

electrodes (2), and the low resistance conductive thin films (10), with a thickness, for example, of about 50 to 100 nm.

After being coated with the oxide semiconductor thin film layer (3), the low resistance conductive thin films (10) are etched together with the
5 oxide semiconductor thin film layer (3).

It is preferable to perform the etching treatment by means of dry etching. Wet etching is also applicable but not preferable because the wet-etched edges form a nonplanar surface, which results in insufficient step coverage of the gate insulating film (4) to be formed on these layers and
10 in increasing leak current.

If the low resistance conductive thin film (10) is made of zinc oxide doped with gallium (Ga) or aluminum (Al); or intrinsic zinc oxide (ZnO) with no impurity introduced, gases such as CH_4, CF_4, CHF_3, Cl_2, or gas containing one of these gases and oxygen may be used in the dry etching.
15 On the other hand, if the low resistance conductive thin film (10) is made of indium tin oxide (ITO), gases such as CH_4 or mixture of CH_4 and oxygen may be used.

For example, conventional reactive ion etching (RIE method) or inductively coupled plasma (ICP) etching may be used in the dry etching
20 process of the present invention. The low resistance conductive thin films (10) and the oxide semiconductor thin film layer (3) are etched together. As a result, the outer ends (10b) of each of the low resistance conductive thin films (10) and the outer ends (3b) of the oxide semiconductor thin film layer (3) are positioned coincident with each other along the channel length
25 direction, as shown in Fig. 2C. Also, the low resistance conductive thin films (10) and the oxide semiconductor thin film layer (3) are formed to have

an identical shape in the channel width direction. The low resistance conductive thin films 10 and the oxide semiconductor thin film layer 3 are slightly longer than the source/drain electrodes 2 along the channel width direction, as shown in Fig. 1C.

5 Fig. 2C is a sectional view illustrating the lamination of the substrate (1), the source/drain electrodes (2), the low resistance conductive thin films (10), and the oxide semiconductor thin film layer (3) after performing dry etching as described above. In the manufacturing stage shown in Fig. 2C, etched surfaces (3b and 10b in Fig. 2C) must be 10 formed outside the respective inner ends (2c) of the source/drain electrodes (2), along the channel length direction. The source/drain electrodes (2) subsequently serve as etching stoppers (since the source/drain electrodes 2 are made of metal, as described above) so that only the low resistance conductive thin films (10) and the oxide semiconductor thin film layers (3) 15 are etched.

Next, a gate insulating film (4) is formed on the oxide semiconductor thin film layer (3) using a technique and under a condition(s) that do not reduce the resistance of the semiconductor thin film layer (3).

The gate insulating film (4) may be a silicon-based-insulating film 20 such as a silicon oxide (SiO_x) film; a silicon oxide nitride (SiON) film; a silicon nitride (SiN_x) film; or a silicon nitride (SiN_x) film doped with oxygen using oxygen or a compound containing oxygen as a constituent element. Among these, a film of SiN_x doped with oxygen using oxygen or a compound (e.g. N_2O) including oxygen or the like is desirable because the constituents 25 of such a film have a high dielectric constant as well as an excellent effect of preventing reduction and removal of oxygen and zinc from the oxide

semiconductor thin film layer (3).

The gate insulating film (4) may be a 100 to 300 nm thick SiN_x film created by means of a plasma-enhanced chemical vapor deposition (PCVD) under a condition, for example, where a substrate temperature is 250 °C and
5 mixed gas containing NH_3 and SiH_4 is used at a flow rate ratio of 4 to 1.

As shown in Fig. 2D, a gate electrode (6) is disposed over the gate insulating film (4) so that both of the outer ends (6b) of the gate electrode (6) are positioned outside the respective inner ends (10c) of the low resistance conductive thin films (10).

10 As shown in Fig. 2E, contact holes are opened in the gate insulating film 4 to expose portions of the source/drain electrodes (2) by means of photolithography. The external source/drain electrodes (2a) are respectively connected to the source/drain electrodes 2 through the contact holes via contact parts (7a), respectively. In the final step to form a TFT
15 array, a display electrode (8) made of indium tin oxide (ITO) and the like is formed.

Fig. 3 is a cross-sectional view showing the structure of the thin film transistor (200) according to the second embodiment of the present invention. The TFT (200) according to the second embodiment has some
20 similar structures to the TFT (100) according to the first embodiment. These structures are denoted by the same reference numerals. However, in place of the gate insulating film (4) of the TFT 100 according to the first embodiment, the TFT (200) according to the second embodiment includes a first gate insulating film and a second gate insulating film, which are
25 denoted as the first gate insulating film (41) and the second gate insulating film (5).

The first gate insulating film (41) is formed to cover only the upper surface of the oxide semiconductor thin film layer (3). The first gate insulating film (41) is provided as a part of the gate insulating film. The first gate insulating film (41) serves as a protective film configured to
5 protect the oxide semiconductor thin film layer (3) from the resist stripper used in the manufacturing process.

The second gate insulating film (5) is laminated to cover the side surfaces of the source/drain electrodes (2) and the oxide semiconductor thin film layer (3) as well as the entire upper surfaces of the first gate insulating
10 film (41). Since the upper surface of the oxide semiconductor thin film layer (3) is covered with the first gate insulating film (41), the coverage on all the exposed surfaces of the oxide semiconductor thin film layer 3 is then completed.

The first gate insulating film (41) and the second gate insulating
15 film (5) may be a silicon oxide (SiO_x) film; a silicon oxide nitride (SiON) film; a silicon nitride (SiN_x) film; or a silicon nitride (SiN_x) film doped with oxygen using oxygen or a compound containing oxygen as a constituent element. Preferably, the first gate insulating film (41) and the second gate insulating film (5) are formed by a SiN_x film doped with oxygen using
20 oxygen or a compound (e.g. N_2O) containing oxygen. Such a doped SiN_x film has a higher dielectric constant than silicon oxide compounds (SiO_x) or silicon oxide nitride (SiON).

The first gate insulating film (41) and the second gate insulating film (5) are formed by means of a plasma-enhanced chemical vapor
25 deposition (PCVD) process. It is desirable to perform the film formation by the plasma-enhanced chemical vapor deposition (PCVD) process at a

substrate temperature of 250 °C or below. In this temperature range, the reduction of the oxide semiconductor thin film layer or removal of oxygen and zinc does not occur.

Hereinafter, a manufacturing method of a thin film transistor (TFT) according to the second embodiment of the present invention will be explained referring to Figs. 4A-4D.

First, as shown in Fig. 4A, source/drain electrodes (2) and low resistance conductive thin films (10) are formed on a substrate (1) and as in the first embodiment of the present invention. The low resistance conductive thin films (10) are formed over the source/drain electrodes (2) of a plurality of TFTs (200). An oxide semiconductor thin film layer (3) is formed on all the exposed surfaces of the substrate (1), the source/drain electrodes (2), and the low resistance conductive thin films (10).

Next, as shown in Fig. 4B, a first gate insulating film (41) is formed on the oxide semiconductor thin film layer (3) with an approach and a condition that do not reduce the resistance of the oxide semiconductor thin film layer (3). Then, a photo-resist is coated on the first gate insulating film (41) and patterned. Using the patterned photo-resist as a mask, the first gate insulating film (41), the low resistance conductive thin film (10), and the oxide semiconductor thin film layer (3) are simultaneously etched. Preferably, dry etching is used in the etching process because the dry-etched edges are positioned coincident with each other. Thus leakage current resulting from insufficient step coverage is suppressed after the first gate insulating film (41) is formed.

As in the first embodiment of the present invention, if the low resistance conductive thin film (20) is made of zinc oxide doped with gallium

(Ga) or aluminum (Al); or intrinsic zinc oxide (ZnO) with no impurity introduced, gases such as CH_4, CF_4, CHF_3, Cl_2, or gas containing one of these and oxigen may be used in the dry etching. On the other hand, if the low resistance conductive thin films (10) are made of indium tin oxide (ITO), 5 gases such as CH_4 or a mixture of CH_4 and oxygen may be used. For example, common reactive ion etching (RIE method) or inductively coupled plasma (ICP) etching may be used in the dry etching process.

Fig. 4C shows a cross-section of a lamination comprising the oxide semiconductor thin film layer (3), the low resistance conductive thin films 10 (10), and the first gate insulating film (41) after etching and removing the photo-resist. Etched surfaces (3b), etched surfaces (10b), and etched surfaces (41b) of the layers are positioned coincident with each other. Consequently, sufficient step coverage is maintained and leakage current is suppressed, after a second gate insulating film (5) is formed.

15 The etched surfaces must be formed outside the respective inner ends (2c) of the source/drain electrodes (2) in the channel length direction. Thus, only the first gate insulating film (41), the low resistance conductive thin films (10) and the oxide semiconductor thin film layer (3) are etched.

The first gate insulating film (41) not only forms an interface with 20 the oxide semiconductor thin film layer (3) but also protects the oxide semiconductor thin film layer (3) while an active region of the TFT is patterned. If the first gate insulating film 41 is not present, while the resist stripper is used to remove photo-resist after the patterning of the active layer, the resist stripper contacts with the surface of the oxide 25 semiconductor thin film layer (3). The resist stripper generally etches and roughens the surface and crystal grain boundary of the oxide semiconductor

thin film layer (3). However, if the first gate insulating film (41) is present on the surface of the oxide semiconductor thin film layer (3), the first gate insulating film (41) functions as a protective film against various kinds of liquid chemicals such as a resist stripper used in a photo-lithography process. The first gate insulating film (41) therefore prevents the surface of the oxide semiconductor thin film layer (3) from roughening. Thus, sufficient interface properties between the oxide semiconductor thin film layer (3) and the gate insulating film are maintained.

Referring to Fig. 4D, after a TFT active layer region is patterned, a second gate insulating film (5) is formed on all the exposed surfaces of substrate (1), the source/drain electrodes (2), the oxide semiconductor thin film layer (3), the low resistance conductive thin films (10), and the first gate insulating film (41). Then contact holes are opened in the gate insulating film 5 to expose portions of the source/drain electrodes (2). In this embodiment, it is desirable to form the second gate insulating film (5) under similar conditions to the first gate insulating film (41).

A gate electrode (6) made of a metal film is formed on the second gate insulating film (5). After that, external source/drain electrodes (2a) are formed with the same material as the gate electrode (6). The external source/drain electrodes are connected to the source/drain electrodes (2) via contact parts (7a). A display electrode (8) is formed in the final step to form a TFT array of the second embodiment of the present invention (see the TFT shown in Fig. 3).

Hereinafter, the thin film transistor according to the third embodiment of the present invention will be described with reference to Fig. 5.

Fig. 5 is a cross-sectional view showing the structure of a thin film transistor (300) according to the third embodiment of the present invention. The thin film transistor (300) includes a substrate (11), a gate electrode (12), a gate insulating film (13), source/drain electrodes (14), low resistance conductive thin films (20), an oxide semiconductor thin film layer (15), an overcoat insulating film (16), external source/drain electrodes (14a), contact parts (18a), and a display electrode (19). The TFT (300) is a bottom gate type TFT in which these layers are laminated in the order shown in Fig. 5.

As shown in Fig. 5, the thin film transistor (300) is formed on the substrate (11). The gate electrode (12) is formed on the substrate (11). In this step, the gate electrode (12) is disposed over the substrate (11) so that the outer ends of the gate electrode (12) will be positioned outside the inner ends of the low resistance conductive thin films (20) (described below), along the channel length direction.

The gate insulating film (13) is laminated on the entire upper surface of the substrate (11) so as to cover the gate electrode (12).

The source/drain electrodes (14) are laminated on the gate insulating film (13). The source/drain electrodes (14) are made of metal. In general, source/drain electrodes are formed with conductive oxides such as indium tin oxide (ITO) and n+ZnO. In the present invention, however, the conductive oxides are not preferable because the source/ drain electrodes made of the conductive oxides are etched when the oxide semiconductor thin film layer and low resistance conductive thin films are etched.

The length in the channel width direction of the source/drain electrodes (14) is preferably equal to or smaller than the length of the oxide semiconductor thin film layer (15) in the channel width direction. If the

length of the source/drain electrodes (14) is larger than the length of the source drain electrodes in the channel width direction, it prevents high integration of the thin film transistors when a plurality of TFTs are integrated.

5 The low resistance conductive thin films (20) are formed on the source/drain electrodes (14). The low resistance conductive thin films (20) may be, for example, a thin film primarily comprising indium tin oxide (ITO); or the zinc oxide doped with gallium (Ga) or aluminum (Al); or the like. If the oxide semiconductor thin film layer 15 primarily comprises zinc
10 oxide, the low resistance conductive thin films 20 may be made of intrinsic zinc oxide (ZnO) with no impurity introduced. When the low resistance conductive thin films 10 are made of intrinsic zinc oxide with no impurities introduced, the zinc oxide in the low resistance conductive thin films (20) must have larger crystal grain size than the zinc oxide in the oxide
15 semiconductor thin film layer (15).

The resistance of the low resistance conductive thin films (20) is higher than the resistance of the source/drain electrodes (14) and lower than the resistance of the oxide semiconductor thin film layer (15). Therefore, the contact properties between each of the source/drain electrodes (14) and
20 the oxide semiconductor thin film layer (15) are improved by using the low resistance conductive thin films (20).

The oxide semiconductor thin film layer (15), is arranged so that a channel is formed on each of the low resistance conductive thin films (20) and between the electrodes of the low resistance conductive thin films (20).
25 The oxide semiconductor thin film layer 15 may be made of, for example, an oxide semiconductor primarily comprising zinc oxide or an IGZO as the

oxide semiconductor thin film layer 3 described above.

The oxide semiconductor thin film layer (15) covers the entire upper surfaces of the low resistance conductive thin films (20). At least side surfaces of the low resistance conductive thin films (20) have an identical shape to the side surfaces of the oxide semiconductor thin film layer (15) so that they form a planar surface.

Consequently, the space provided between the adjacent oxide semiconductor thin films (15) according to the accuracy of mask alignment of the low resistance conductive thin films (20) and the oxide semiconductor thin film layer (15) (i.e., a space corresponding to width A described above with respect to Fig. 9B) is not necessary. Therefore, it is possible to shorten the distance (spacing) between the low resistance conductive thin films (20) to the minimum line width of the aligner (i.e., the gap B described above with respect to Fig. 9B), which enables high integration of the thin film transistors (300).

The overcoat insulating film (16) is formed so as to cover the upper surface and side surfaces of the oxide semiconductor thin film layer (15). The external source/drain electrodes (14a) are formed so as to be connected to the source/drain electrodes (14) via the contact parts (18a) in the contact holes opened in the overcoat insulating film (16).

The display electrode (19) is configured to apply a voltage to a liquid crystal in a liquid crystal display via the thin film transistor. The display electrode (19) is formed by a conductive oxide thin film such as an indium tin oxide (ITO) thin film and the like because it must have high transmittance with respect to visible light.

Referring to Figs. 6A-6D, a manufacturing method of the bottom

gate type TFT according to the third embodiment of the present invention will be described below.

As shown in Fig. 6A, a gate electrode (12) is formed on a substrate (11) made of, for example, glass. Then, a gate insulating film (13) is formed on the entire upper surface of the substrate (11) so as to cover the gate electrode (12). Although the method for forming the gate insulating film (11) is not limited especially, it is preferable to use a plasma-enhanced chemical vapor deposition (PCVD) process that enables film formation on a substrate having a large area.

Referring to Fig. 6B, after the gate insulating film (13) is formed, a metal film is formed on the entire upper surfaces of the gate insulating film (13). The metal film is then subjected to photolithography to form the source/drain electrodes (14). After that, low resistance conductive thin film 20 having a thickness of, for example, about 10 to 100 nm, are formed on the source/drain electrodes (14) by means of a magnetron sputtering process. The low resistance conductive thin film (20) is then patterned to bridge the source/drain electrodes (14) of a plurality of TFTs. More specifically, in the patterning, the low resistance conductive thin film (20) is etched in an area (channel-corresponding area) that corresponds to the gap extending between the source electrodes and the drain electrodes. The resultant low resistance conductive thin films (20) are separated into a first low resistance conductive thin film piece and a second low resistance conductive thin film piece. The first low resistance conductive thin film piece bridges, for example, the source electrodes of the plurality of the TFTs, while the second low resistance conductive thin film piece bridges, for example, the drain electrodes of the plurality of the TFTs. At this stage, the low resistance

conductive thin films (20) are shaped to extend longer in the channel length direction than the final shape of the low resistance conductive thin films (20). The oxide semiconductor thin film layer (15) is then coated on the low resistance conductive thin films (20), as shown in Fig. 6B.

5 A photo-resist is coated on the upper surface of the oxide semiconductor thin film layer (15) and patterned. Using the patterned photo-resist as a mask, the low resistance conductive thin films (20) and the oxide semiconductor thin film layer (15) are simultaneously etched. Preferably, dry etching is used in the etching process because the dry-etched 10 edges form a planer surface. Thus, leakage current resulting from insufficient step coverage is suppressed after an overcoat insulating film (16) is formed.

If the low resistance conductive thin film (20) is made of zinc oxide doped with gallium (Ga) or aluminum (Al); or intrinsic zinc oxide (ZnO) with 15 no impurity introduced, gases such as CH_4, CF_4, CHF_3, Cl_2, or gas containing one of these gases and oxygen may be used in the dry etching. On the other hand, if the low resistance conductive thin film (10) is made of indium tin oxide (ITO), gases such as CH_4 or a mixture of CH_4 and oxygen may be used. For example, common reactive ion etching (RIE method) or 20 inductively coupled plasma (ICP) etching may be used in the dry etching process of the present invention.

Fig. 6C is a cross-sectional view of the TFT (300) after performing dry etching. At this stage, etched surfaces (15b) of the oxide semiconductor thin film layer (15) and etched surfaces (20b) of the low resistance 25 conductive thin films (20) must be located outside respective inner ends (14c) of the source/drain electrodes (14) in the channel length direction.

The source/drain electrodes (14) subsequently serve as etching stoppers so that only the low resistance conductive thin films (20) and the oxide semiconductor thin film layer (15) are etched.

After the patterning of the oxide semiconductor thin film layer (15), the overcoat insulating film (16) is formed to cover all the exposed surfaces of the oxide semiconductor thin film layer (15), as shown in Fig. 6D.

The overcoat insulating film (16) may be a silicon oxide (SiO_x) film; a silicon oxide nitride (SiON) film; a silicon nitride (SiN_x) film; or a silicon nitride (SiN_x) film doped with oxygen using oxygen or a compound containing oxygen as a constituent element. Preferably, the overcoat insulating film (16) is formed with a SiN_x film that is doped with oxygen using oxygen or a compound (e.g. N_2O) containing oxygen. Such a doped SiN_x film has a higher dielectric constant than silicon oxide compounds (SiO_x) or silicon oxide nitride (SiON).

The overcoat insulating film (16) is formed by means of a plasma-enhanced chemical vapor deposition (PCVD) process.

After forming the overcoat insulating film (16), external source/drain electrodes (14a) are formed. The external source/drain electrodes (14a) are connected to the source/drain electrodes (14) via contact parts (18a). A display electrode (19) is formed in the final step to form a TFT array of the third embodiment of the present invention (see the TFT shown in Fig. 5).

Finally, the fourth embodiment of the present invention will be described.

Fig. 7 is a cross-sectional view showing the structure of the thin film transistor 400 according to the fourth embodiment of the present invention.

The TFT (400) according to the fourth embodiment has some similar structures to the TFT (300) according to the third embodiment. These structures are denoted by the same reference numerals. However, in place of the overcoat insulating film (16) of the TFT 300 according to the third embodiment, TFT (400) according to the fourth embodiment includes a first overcoat insulating film and a second overcoat insulating film, which are denoted as the first overcoat insulating film (161) and the second overcoat insulating film (17).

The first overcoat insulating film (161) is formed so as to cover only the upper surface of the oxide semiconductor thin film layer (15). The first overcoat insulating film (161) is provided as a part of the gate insulating film. The first overcoat insulating film (161) serves as a protective film configured to protect the oxide semiconductor thin film layer (15) from resist stripper used in the manufacturing process.

The second overcoat insulating film (17) is provided for protecting the TFT (400). The second overcoat insulating film (17) is laminated to cover all the exposed surfaces of the first overcoat insulating film (161) and side surfaces of the oxide semiconductor thin film layer (15).

The second overcoat insulating film (17) ensures that the entire side surfaces of the oxide semiconductor thin film layer (15) get covered even if some parts of them are not covered with the first overcoat insulating film (161).

The first overcoat insulating film (161) and the second overcoat insulating film (17) may be a silicon oxide (SiO_x) film; a silicon oxide nitride (SiON) film; a silicon nitride (SiN_x) film; or a silicon nitride (SiN_x) film doped with oxygen using oxygen or a compound containing oxygen.

Preferably, the first overcoat insulating film (161) and the second overcoat insulating film (17) are formed with the SiN_x film that is doped with oxygen using oxygen or a compound (e.g. N_2O) containing oxygen. Such a doped SiN_x film has a higher dielectric constant than silicon oxide compounds (SiO_x) or silicon oxide nitride (SiON).

The first overcoat insulating film (161) and the second overcoat insulating film (17) are formed by, for example, a plasma-enhanced chemical vapor deposition (PCVD) process.

Referring to Figs. 8A-8D, a manufacturing method of the thin film transistor (TFT) according to the fourth embodiment of the present invention will be described below.

First, as shown in Fig. 8A, a gate electrode (12) and a gate insulating film (13) are formed on a substrate (11) as in the third embodiment of the present invention.

Next, as shown in Fig. 8B, source/drain electrodes (14), low resistance conductive thin films (20), an oxide semiconductor thin film layer (15), and a first overcoat insulating film (16) are laminated in this order on the gate insulating film (13). Then, the low resistance conductive thin films (20), the oxide semiconductor thin film layer (15) and the first overcoat insulating film (161) are simultaneously etched. Preferably, dry etching is used in the etching process because the dry-etched edges are positioned coincident with each other. Thus leakage current resulting from insufficient step coverage is suppressed, after the first overcoat insulating film (161) is formed.

As in the third embodiment of the present invention, if the low resistance conductive thin film (20) is made of zinc oxide doped with gallium

(Ga) or aluminum (Al); or intrinsic zinc oxide (ZnO) with no impurity introduced, gases such as CH_4, CF_4, CHF_3, Cl_2, or gas containing one of these gases and oxygen may be used in the dry etching. On the other hand, if the low resistance conductive thin film (20) is made of indium tin oxide (ITO), gases such as CH_4 or a mixture of CH_4 and oxygen may be used. In the fourth embodiment of the present invention, for example, common reactive ion etching (RIE method) or inductively coupled plasma (ICP) etching may be used in the dry etching process, as in the first embodiment of the present invention.

Fig. 8C shows a cross-section of a lamination comprising the oxide semiconductor thin film layer (15), the low resistance conductive thin films (20), and the first overcoat insulating film (161) after etching and removing the photo-resist. Etched surfaces (15b), etched surfaces (20b), and etched surfaces (161b) of the above-mentioned layers are positioned coincident with each other. Consequently, sufficient step coverage is maintained after a second overcoat insulating film (17) is formed.

The first overcoat insulating film (161) also protects the oxide semiconductor thin film layer (15) while an active region of the TFT is patterned. If the first overcoat insulating film 161 is not present when the resist stripper is used to remove photo-resist after the patterning of an active layer, the resist stripper contacts with the surface of the oxide semiconductor thin film layer 15. The resist stripper generally etches and roughens the surface and crystal grain boundary of the oxide semiconductor thin film layer 15. However, if the first overcoat insulating film 161 is present on the surface of the oxide semiconductor thin film layer 15, the first overcoat insulating film 161 functions as a protective film against

various kinds of liquid chemicals such as a resist stripper used in a photo-lithography process. The first overcoat insulating film (161) therefore prevents the surface of the oxide semiconductor thin film layer (15) from roughening. Thus, sufficient interface properties between the
5 oxide semiconductor thin film layer (15) and the first overcoat insulating film (161) are maintained.

Referring to Fig. 8D, after the active layer region of the TFT is patterned, a second overcoat insulating film (17) is formed on all the exposed surfaces of the gate insulating film (13), the source/drain electrodes
10 (14), the oxide semiconductor thin film layer (15), the low resistance conductive thin films (20), and the first overcoat insulating film (161).

Then contact holes are opened in the first overcoat layer 17 to expose portions of the source/drain electrodes (14).

External source/drain electrodes (14a), which are connected to the
15 source/ drain electrodes (14) via contact parts (18a), are formed. Then a display electrode (19) is formed in the final step to form a TFT array of the fourth embodiment of the present invention (see the FTF shown in Fig. 7).

As described above, the thin film transistor according to the present invention has excellent performance so that it is preferably used as an
20 active element of a liquid crystal display device and the like.

CLAIMS

1. A thin film transistor comprising:

a substrate (1, 11);

5 a pair of source/drain electrodes (2, 14) formed on the substrate and defining a gap therebetween;

a pair of low resistance conductive thin films (10, 20), each coating at least a part of one of the source/drain electrodes, the low resistance conductive thin films defining a gap therebetween; and

10 an oxide semiconductor thin film layer (3, 15), which is continuously formed on upper surfaces of the pair of low resistance conductive thin films, and which extends along the gap defined between the low resistance conductive thin films so as to function as a channel;

wherein side surfaces of the oxide semiconductor thin film layer and 15 corresponding side surfaces of the low resistance conductive thin films coincide with each other in a channel width direction of the channel.

2. The thin film transistor according to claim 1, wherein a length of the oxide semiconductor thin film layer (3, 15) in a channel width 20 direction of the channel is equal to or larger than a length of the source/drain electrodes (2, 14) in the channel width direction.

3. The thin film transistor according to claim 1, wherein the oxide semiconductor thin film layer primarily comprises zinc oxide.

25

4. The thin film transistor according to claim 1, wherein the

source/drain electrodes (2, 14) are made of metal.

5. The thin film transistor according to claim 1, wherein each of the low resistance conductive thin films (10, 20) primarily comprises any one selected from a group consisting of indium tin oxide (ITO), zinc oxide doped with gallium (Ga), and zinc oxide doped with aluminum (Al).

6. The thin film transistor according to claim 1, wherein the low resistance conductive thin films (10, 20) are made of intrinsic zinc oxide and the zinc oxide forming the low resistance conductive thin films has a crystal grain size that is larger than a crystal grain size of the zinc oxide forming the oxide semiconductor thin film layer (3, 15).

7. The thin film transistor according to claim 1, further comprising:

a gate insulating film disposed over the oxide semiconductor thin film layer (3), the gate insulating film (41, 5) having a dual-layer structure comprising a lamination of a first gate insulating film (41) that covers only an upper surface of the oxide semiconductor thin film layer and a second gate insulating film (5) that covers an upper surface and side surfaces of the first gate insulating film and side surfaces of the oxide semiconductor thin film layer; and

a gate electrode (6) disposed over the gate insulating film.

8. The thin film transistor according to claim 1, further comprising:

a gate electrode (12) disposed below the oxide semiconductor thin film layer (15); and

an overcoat insulating film (161, 17) disposed over the oxide semiconductor thin film layer, the overcoat insulating film having a dual-layer structure comprising a lamination of a first overcoat insulating film (161) that covers only the upper surface of the oxide semiconductor thin film layer and a second overcoat insulating film (17) that covers an upper surface and side surfaces of the first overcoat insulating film and side surfaces of the oxide semiconductor thin film layer.

9. A thin film transistor comprising:

an oxide semiconductor thin film layer (3, 15) having a pair of side surfaces;

a pair of low resistance conductive thin films (10, 20) defining a gap therebetween along an area corresponding to a channel of the thin film transistor, each of the low resistance conductive thin films having a pair of side surfaces, each of the side surfaces being positioned so as to coincide with a corresponding one of the side surfaces of the oxide semiconductor thin film layer; and

a pair of source/drain electrodes (2, 14), each having a pair of side surfaces, each of the side surfaces being one of positioned so as to coincide with and positioned inside of a corresponding one of the side surfaces of the low resistance conductive thin films.

10. A manufacturing method of a thin film transistor comprising:

forming a pair of source/drain electrodes (2) on a substrate (1), such that the source/drain electrodes define a gap therebetween;

forming low resistance conductive thin films (10), which define a gap therebetween, on the source/drain electrodes;

5 forming an oxide semiconductor thin film layer (3) on upper surface of the low resistance conductive thin films and in the gap defined between the low resistance conductive thin films so that the oxide semiconductor thin film layer functions as a channel;

etching the low resistance conductive thin films and the oxide 10 semiconductor thin film layer so that side surfaces of the low resistance conductive thin films and corresponding side surfaces of the oxide semiconductor thin film layer coincide with each other in a channel width direction of the channel; and

mounting a gate electrode (6) over the oxide semiconductor thin film 15 layer.

11. The method according to claim 10, wherein the oxide semiconductor thin film layer primarily comprises zinc oxide.

12. The method according to claim 1, further comprising:

20 forming a first gate insulating film (41) on the oxide semiconductor thin film layer (3);

etching the first gate insulating film together with the low resistance conductive thin films (10), and the oxide semiconductor thin film layer such that the side surfaces of the low resistance conductive thin films, 25 the corresponding side surfaces of the oxide semiconductor thin film, and corresponding side surfaces of the first gate insulating film coincide with

each other at least in the channel width direction, and such that respective outer ends of the low resistance conductive thin films, the oxide semiconductor thin film, and the first gate insulating film, are positioned outside the inner ends of the source/drain electrodes (2) in the channel length direction; and

forming a second gate insulating film (5) on the first gate insulating film (6) and mounting a gate electrode over the second gate insulating film.

13. The method according to claim 10, wherein the etching is dry etching.

14. A manufacturing method of a thin film transistor comprising:

mounting a gate electrode (12) over a substrate (11);

placing a gate insulating film (13) on the gate electrode and forming a pair of source/drain electrodes (14) on the gate insulating film, such that the source/drain electrodes define a gap therebetween;

forming a pair of low resistance conductive thin films (20), which define a gap therebetween, each of the low resistance conductive thin films covering at least a part of the one of source/drain electrodes and having an inner end that is positioned inside outer ends of the gate electrode in the channel length direction of a channel of the thin film transistor;

forming an oxide semiconductor thin film layer (15) on upper surface of the low resistance conductive thin films and in the gap so that the oxide semiconductor thin film layer functions as the channel; and

etching the low resistance conductive thin films and the oxide

semiconductor thin film layer such that side surfaces of the low resistance conductive thin films and corresponding side surfaces of the oxide semiconductor thin film layer coincide with each other in a channel width direction of the channel.

5

15. The method according to claim 14, herein the oxide semiconductor thin film layer primarily comprises zinc oxide.

16. The method according to claim 14, further comprising:

10 forming a first overcoat insulating film (161) on the oxide semiconductor thin film layer (15);

etching the first overcoat insulating film, together with the low resistance conductive thin films (20), and the oxide semiconductor thin film layer, such that the side surfaces of the low resistance conductive thin films,

15 the corresponding side surface of the oxide semiconductor thin fim, and corresponding side surfaces of the first gate insulating film coincide with each other at least in the channel width direction; and

forming a second overcoat insulating film (17) on the first overcoat insulating film.

20

17. The method according to claim 14, wherein the etching is dry etching.

18. A manufacturing method of a thin film transistor

25 comprising:

forming a predetermined number of pairs of source/drain electrodes

(2, 14), each pair comprising a source electrode and a drain electrode defining a gap therebetween along a channel-corresponding area and spaced apart from adjacent pair by a spacing;

forming a pair of low resistance conductive thin films (10, 20)
5 defining a gap therebetween along the channel-corresponding area, one of the low resistance conductive thin films covering the source electrodes and the other of the low resistance conductive thin films covering the drain electrodes;

forming an oxide semiconductor thin film layer (3, 15) on the pair of
10 low resistance conductive thin films, on the channel-corresponding area, and on the spacing; and

etching the oxide semiconductor thin film layer and the low resistance conductive thin films to separate each of them into the predetermined number of oxide semiconductor thin film layer pieces and
15 low resistance conductive thin film pieces along the spacing defined between the pairs of source/drain electrodes so that side surfaces of the respective oxide semiconductor thin film layer pieces are positioned coincident with the side surfaces of the corresponding oxide semiconductor thin film layer pieces.

20

19. The method of according to claim 18, wherein the forming of the pair of low resistance conductive thin films (10, 20) comprises etching a low resistance conductive thin film to form the pair of low resistance conductive thin films to have outer ends that are positioned outside outer
25 ends of a final shape of the low resistance conductive thin films.

FIG. 1A

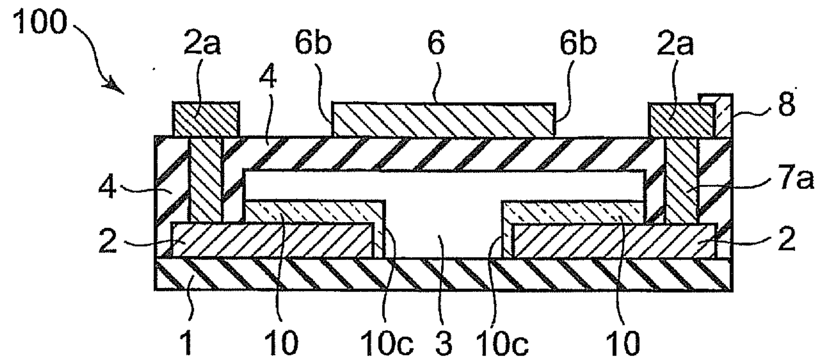


FIG. 1B

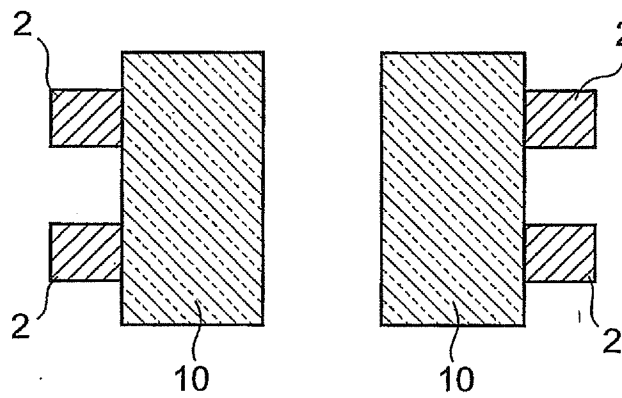


FIG. 1C

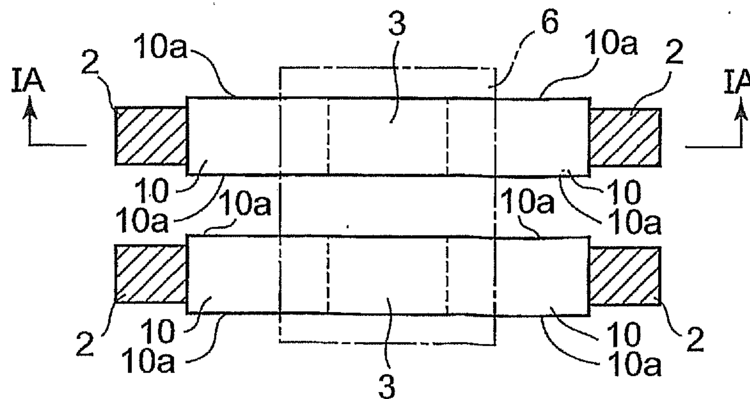


FIG. 2A

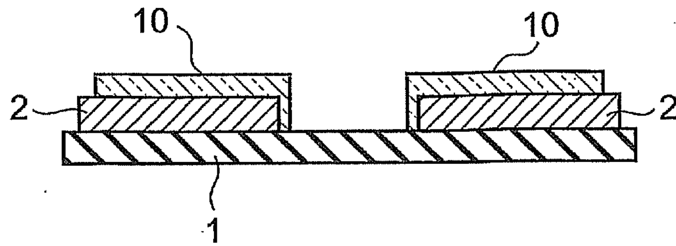


FIG. 2B

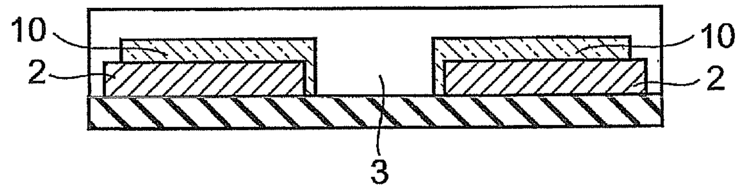


FIG. 2C

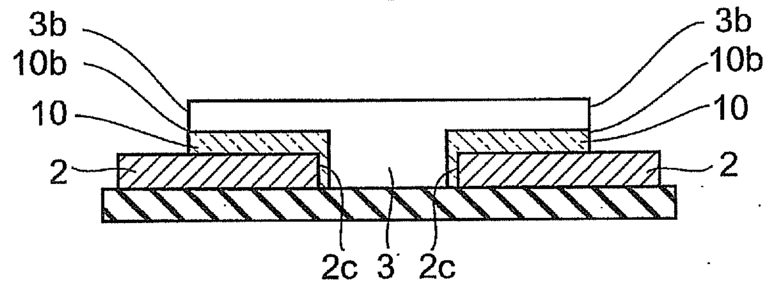


FIG. 2D

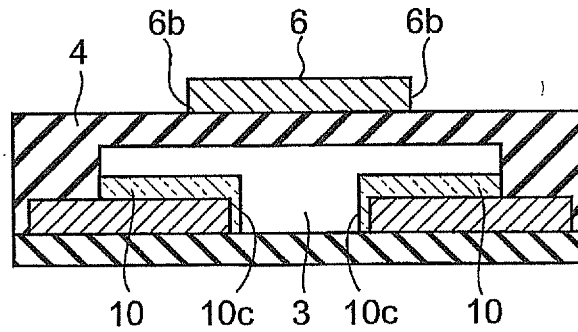


FIG. 2E

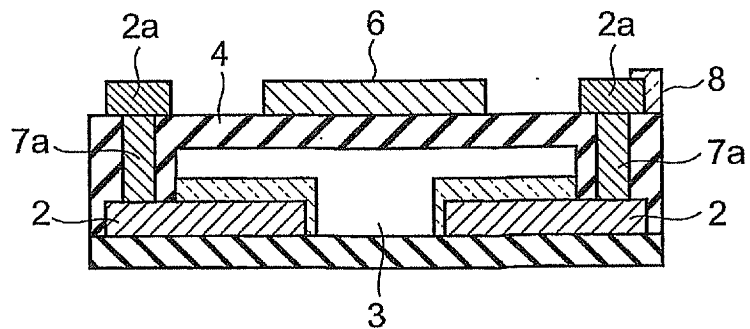


FIG. 3

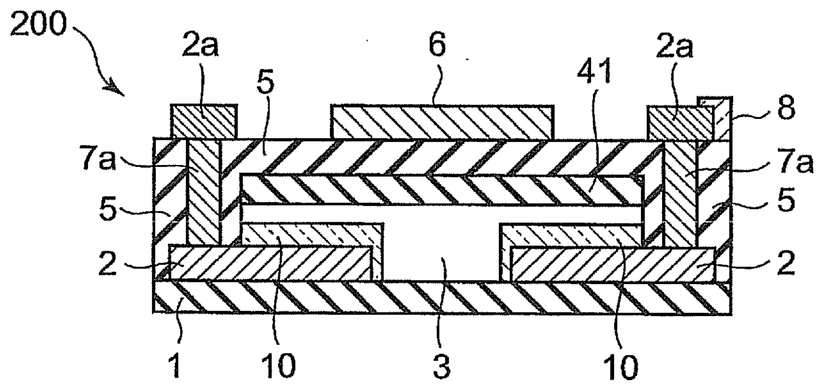


FIG. 4A

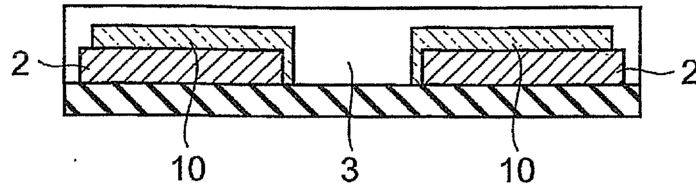


FIG. 4B

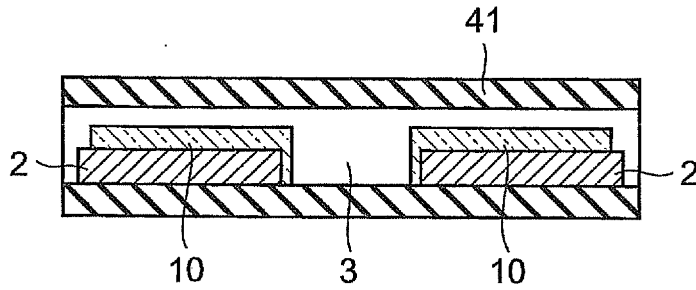


FIG. 4C

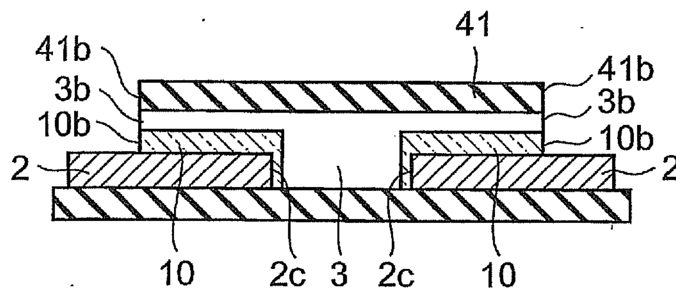


FIG. 4D

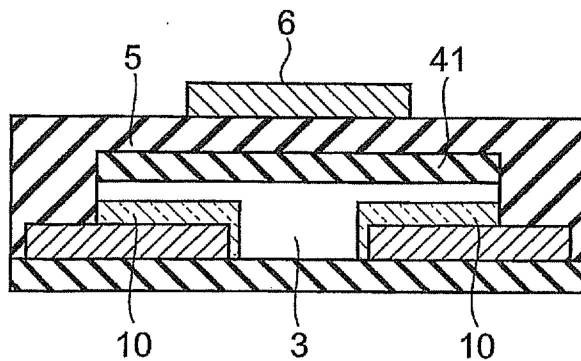


FIG. 5

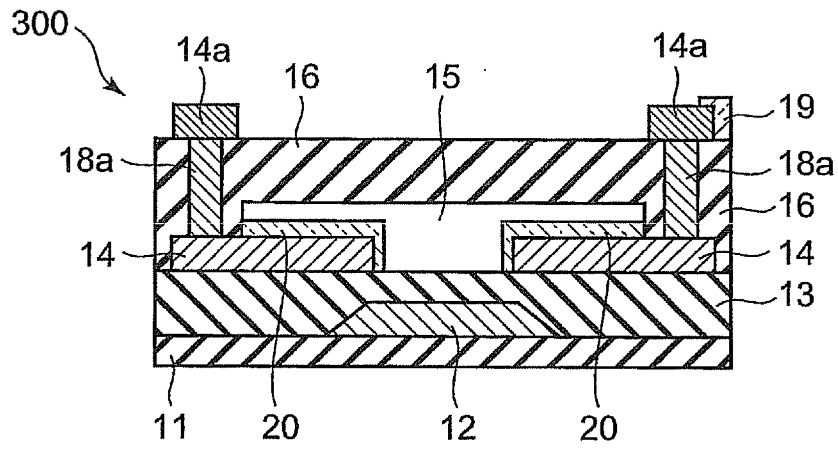


FIG. 6A

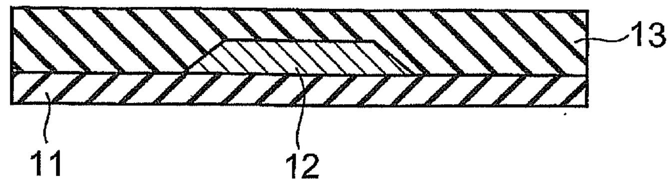


FIG. 6B

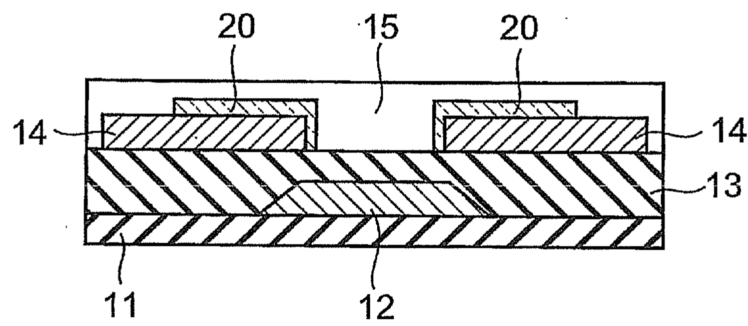


FIG. 6C

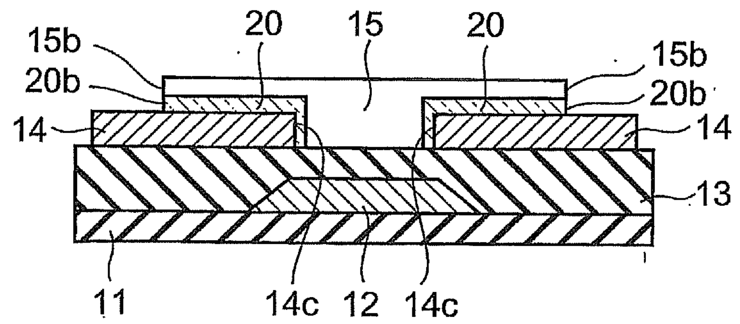


FIG. 6D

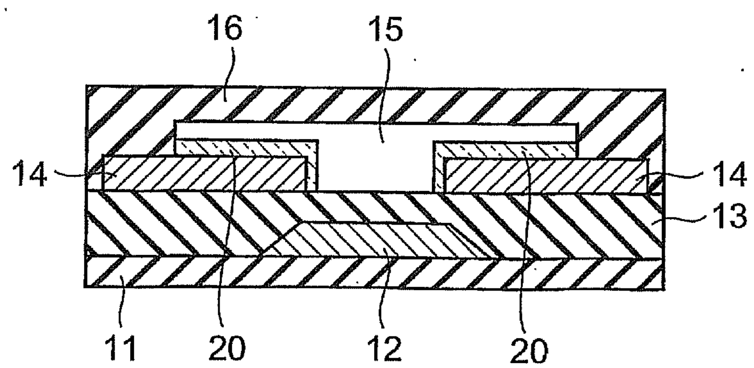


FIG. 7

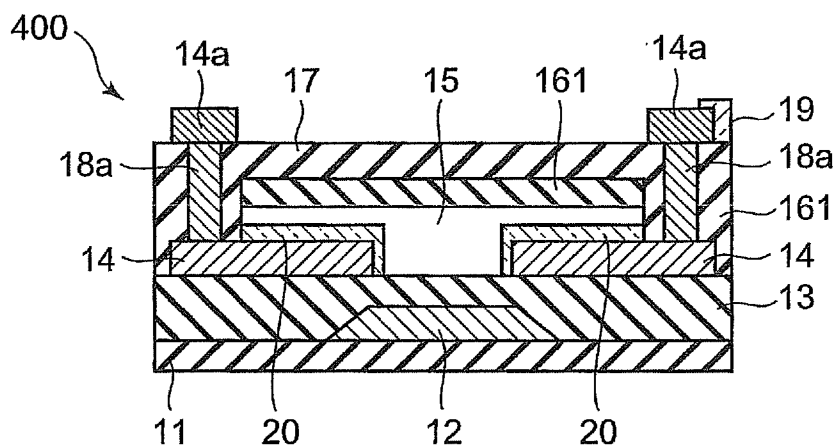


FIG. 8A

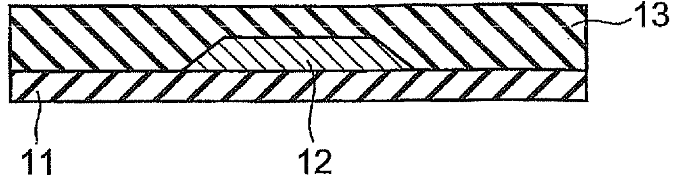


FIG. 8B

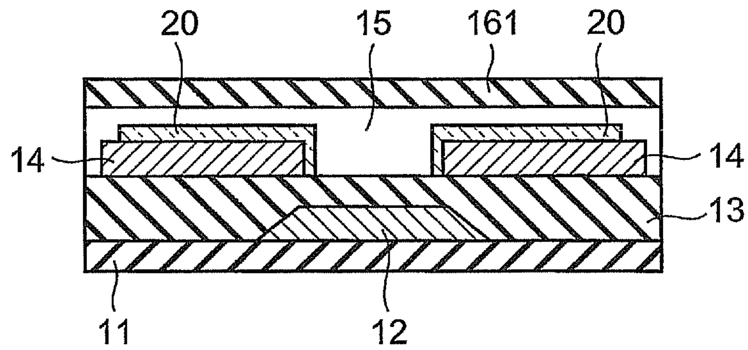


FIG. 8C

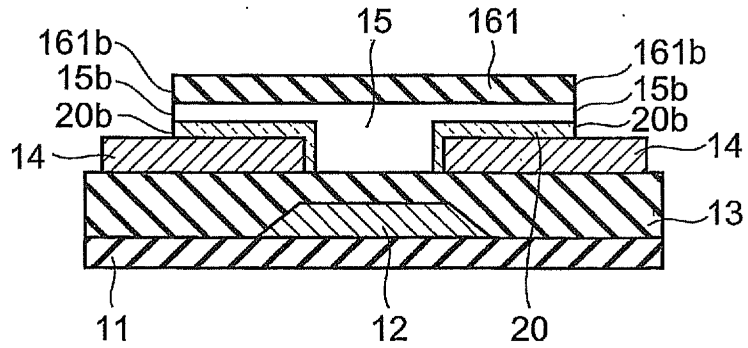


FIG. 8D

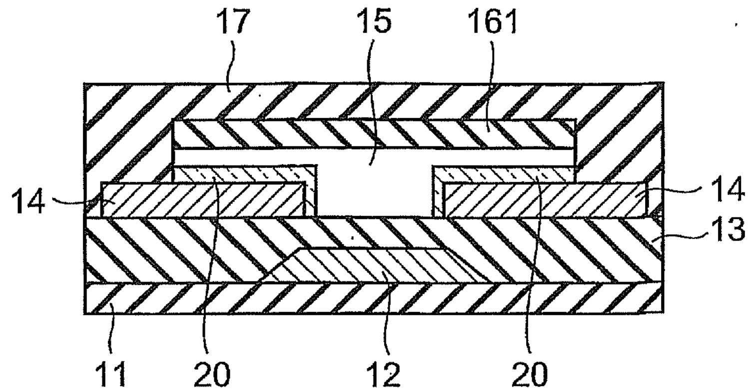


FIG. 9A

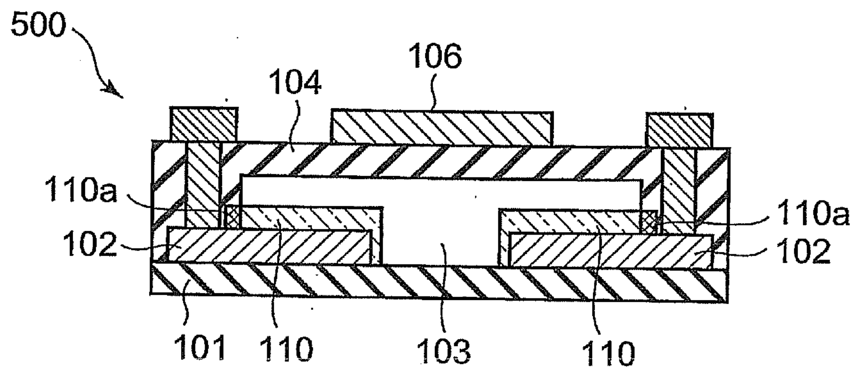
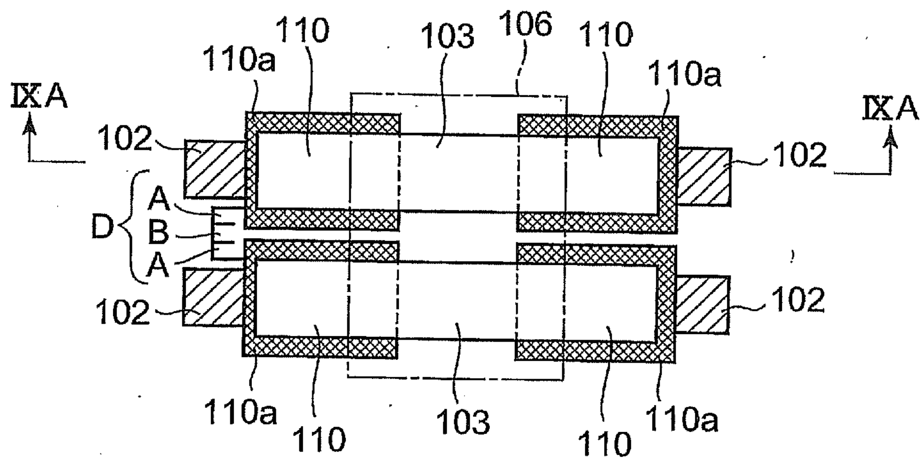


FIG. 9B



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(71) Applicants *(for all designated States except US)*: **KOCHI INDUSTRIAL PROMOTION CENTER** [JP/JP]; 3992-2, Nunoshida, Kochi-shi, Kochi 781-5101 (JP). **CASIO COMPUTER CO., LTD.** [JP/JP]; 6-2, Hon-machi 1-chome, Shibuya-ku, Tokyo 151-8543 (JP).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **HIRAO, Taskashi** [JP/JP]; c/o Kochi Industrial Promotion Center, 3992-2, Nunoshida, kochi-shi, Kochi 781-5101 (JP). **HIRAMATSU, Takahiro** [JP/JP]; c/o Kochi Industrial Promotion Center, 3992-2, Nunoshida, Kochi-shi, Kochi 781-5101 (JP). **FURUTA, Mamoru** [JP/JP]; c/o Kochi Industrial Promotion Center, 3992-2, Nunoshida, Kochi-shi, Kochi 781-5101 (JP). **MATSUDA, Tokiyoshi** [JP/JP]; c/o Kochi Industrial Promotion Center, 3992-2, Nunoshida, Kochi-shi, Kochi 781-5101 (JP).

(74) Agent: **KIYOHARA, Yoshihiro**; 1-3, Dojimahama 2-chome, Kita-ku, Osaka-shi, Osaka 530-0004 (JP).

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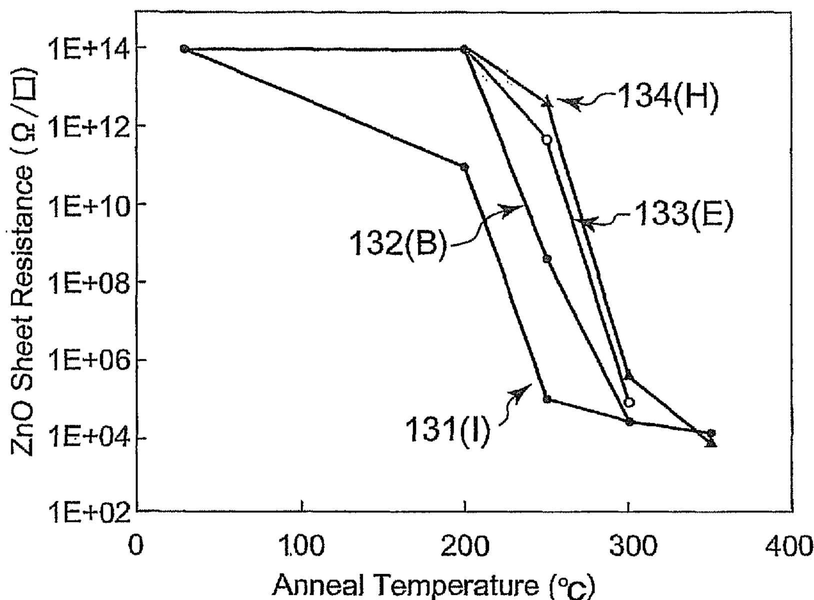

(57) Abstract: A semiconductor device includes an oxide semiconductor thin film layer (3) of zinc oxide. The (002) lattice planes of at least a part of the oxide semiconductor thin film layer have a preferred orientation along a direction perpendicular to a substrate (l) of the semiconductor device and a lattice spacing doo2 of at least 2.619A.

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DESCRIPTION

SEMICONDUCTOR DEVICE INCLUDING AN OXIDE SEMICONDUCTOR THIN FILM LAYER OF ZINC OXIDE AND MANUFACTURING METHOD THEREOF

5

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Applications No. 2006-155188 (filed on June 2, 2006), No. 2006-155189 (filed on June 2, 2006), and No. 2007-37176 (filed
10 on February 16, 2007), the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

15 The present invention relates to a semiconductor device including an active layer of zinc oxide and a manufacturing method thereof.

Description of the Background Art

It has been known for many years that zinc oxide has excellent
20 characteristics as a semiconductor (an active layer). In recent years, active research and development of a semiconductor thin film layer of zinc oxide have been made in order to apply such a semiconductor thin film layer to a semiconductor device which includes a thin film transistor (hereinafter abbreviated as TFT), a light emitting device, a transparent conductive film,
25 or the like.

An oxide TFT including a semiconductor thin film layer of zinc oxide has a greater electron mobility and better TFT performance than an amorphous silicon TFT having a semiconductor thin film layer of amorphous silicon (a-Si: H), which has been mainly used for liquid crystal
5 displays. Another advantage of the oxide TFT is that high electron mobility can be expected because a crystalline thin film is formed even at a temperature as low as a room temperature. These advantages have been encouraging the development of the oxide TFTs.

TFTs using an oxide semiconductor thin film layer, such as a bottom
10 gate TFT and a top gate TFT, have been reported. For example, the bottom gate structure includes, in order: a substrate, a gate electrode, a gate insulator, source/drain electrodes, an oxide semiconductor thin film layer, and a protective insulator. The top gate structure includes, for example, in order: a substrate, a pair of source/drain electrodes, an oxide semiconductor
15 thin film layer, a gate insulator, and a gate electrode.

If an oxide semiconductor thin film layer of zinc oxide is formed on an amorphous material (e.g., glass or plastic as used in a substrate of a display), it is known that physical constants (e.g., orientation and lattice constant) of the zinc oxide vary according to the conditions employed in the
20 film formation. For example, "Microstructural evolution and preferred orientation change of radio-frequency-magnetron sputtered ZnO thin films.", Journal of Vacuum and Science of Technology Part. A Vol. 14, p. 1943 (1996) shows that the orientation and lattice constant of a zinc oxide film vary according to the ratio between argon (Ar) and oxygen (O_2) used as source
25 gases in a sputtering process to form the zinc oxide film. However, this publication does not disclose how the physical properties (e.g., orientation

and lattice constant) of zinc oxide affect the heat resistance of the zinc oxide or the performance of semiconductor devices which include a TFT or the like.

The effect of the orientation and the lattice constant of zinc oxide on the performance of a semiconductor device is described in Japanese Patent Publication No. 2005-150635. Japanese Patent Publication No. 2005-150635 discloses that a thin film transistor exhibits preferable performance when the lattice spacing d_{002} of lattice planes along (002) direction ranges from 2.613Å to 2.618Å. In Japanese Patent Publication No. 2005-150635, TFT performance of a bottom gate TFT was measured. As shown in Fig. 16, the bottom gate TFT includes a substrate 51, a gate electrode 52, a gate insulator 53, oxide semiconductor thin film layer 54 of zinc oxide, and a pair of source/drain electrodes 55. These layers are combined in this order.

Japanese Patent Publication No. 2005-150635 defines a preferable range of lattice spacing d_{002} of oxide semiconductor thin film layer 54 as 2.613Å to 2.618Å based on X-ray diffraction values, which are mean values throughout oxide semiconductor thin film layer 54. Thus, the preferable range 2.613Å to 2.618Å defined by Japanese Patent Publication No. 2005-150635 for the lattice spacing d_{002} is calculated from mean values throughout oxide semiconductor thin film layer 54.

In bottom gate TFTs, a portion of oxide semiconductor thin film layer 54 that forms an interface between gate insulator 53 and oxide semiconductor thin film layer 54, having a thickness of 10 nm or less, functions as a channel region. The channel region has a poorer crystallinity than the other part of oxide semiconductor thin film layer 54

since the channel region is formed at an early stage in formation of oxide semiconductor thin film layer 54.

This means that the channel area formed in oxide semiconductor thin film layer 54 at an early stage of the film formation does not always have a lattice spacing d_{002} that is in the range calculated from the mean value of entire oxide semiconductor thin film layer 54 as disclosed in Japanese Patent Publication No. 2005-150635.

In a practical use of a bottom gate TFT in a liquid crystal display or the like, a protective insulator is formed on the oxide semiconductor thin film layer using a heating process. Since zinc oxide has a poor heat resistance, the heat history during the protective insulator formation results in desorption of zinc or oxygen from the oxide semiconductor thin film layer as well as defects in the oxide semiconductor thin film layer. The defects form a shallow impurity level and reduce the resistance of the oxide semiconductor thin film layer.

In a bottom gate TFT, the defects caused by the formation of the protective insulator form defects in the surface of the oxide semiconductor thin film layer, which is at a back channel side of the bottom gate TFT. As described above, the bottom part of the oxide semiconductor thin film layer functions as a channel in the bottom gate TFT. The defects formed on the back channel side greatly affect the performance of the bottom gate TFT.

In producing the bottom gate TFT disclosed in Japanese Patent Publication No. 2005-150635, only vacuum deposition of source/drain electrodes 55 is performed after oxide semiconductor thin film layer 54 is formed. Thus, oxide semiconductor thin film layer 54 as described in Japanese Patent Publication No. 2005-150635 is not affected by the heat

history caused during the formation of a protective insulator. In other words, the effects of heat on zinc oxide are not taken into account in defining the lattice constant range disclosed in Japanese Patent Publication No. 2005-150635. Therefore, it is not clear whether oxide semiconductor thin film layer 54 has a lattice spacing that is within the above-mentioned range during the actual use of the TFT in a liquid crystal display or the like after a protective insulator is formed in the TFT.

SUMMARY OF INVENTION

One object of the present invention is to provide a semiconductor device that includes an oxide semiconductor thin film layer of zinc oxide and that exhibits excellent performance even after being subjected to a heat treatment process during formation of an insulating film or the like.

According to one aspect of the present invention, a semiconductor device includes an oxide semiconductor thin film layer of zinc oxide. The (002) lattice planes of at least a part of the oxide semiconductor thin film layer have a preferred orientation along a direction perpendicular to a substrate and a lattice spacing d_{002} of at least 2.619Å.

According to one aspect of a manufacturing method of a semiconductor device according to the present invention, a substrate is provided and an oxide semiconductor thin film layer of zinc oxide is deposited on the substrate. In the as-deposited state, the (002) lattice planes of at least a part of the oxide semiconductor thin film layer have a preferred orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å.

BRIEF DESCRIPTION OF THE DRAWINGS

Further features and advantages of the present invention will become apparent from the following detailed description, taken in combination with the accompanying drawings.

Fig. 1 is a cross sectional view of the thin film transistor according to the first embodiment of the present invention;

Figs. 2A to 2F are cross sectional views of the thin film transistor (TFT) sequentially showing a manufacturing method of the thin film transistor of the first embodiment. Fig. 2A is a cross sectional view of the thin film transistor after formation of the pair of source/drain electrodes on the substrate; Fig. 2B is a cross sectional view of the thin film transistor after formation of the oxide semiconductor thin film layer and the first gate insulator; Fig. 2C is a cross sectional view of the thin film transistor after formation of the photoresist; Fig. 2D is a cross sectional view of the thin film transistor after patterning of the oxide semiconductor thin film layer and the first gate insulator; Fig. 2E is a cross sectional view of the thin film transistor after formation of the second gate insulator and the contact holes; and Fig. 2F is a cross sectional view of the thin film transistor after formation of the gate electrode, the contact parts, the external source/drain electrodes, and the display electrode;

Fig. 3 is a cross sectional view of the thin film transistor according to the second embodiment of the present invention;

Figs. 4A to 4E are cross sectional views of the thin film transistor sequentially showing a manufacturing method of the thin film transistor of

the second embodiment. Fig. 4A is a cross sectional view of the thin film transistor after formation of the pair of source/drain electrodes and the contact layers on the substrate; Fig. 4B is a cross sectional view of the thin film transistor after formation of the oxide semiconductor thin film layer; 5 Fig. 4C is a cross sectional view of the thin film transistor after formation of the first gate insulator; Fig. 4D is a cross sectional view of the thin film transistor after patterning of the first gate insulator, the oxide semiconductor thin film layer, and the contact layers; and Fig. 4E is a cross sectional view of the thin film transistor after formation of the second gate 10 insulator and the contact holes;

Fig. 5 is a cross-sectional view of the thin film transistor according to the third embodiment of the present invention;

Figs. 6A to 6F are cross sectional views of the thin film transistor (TFT) sequentially showing a manufacturing method of the thin film 15 transistor of the third embodiment. Fig. 6A is a cross sectional view of the thin film transistor after formation of the pair of source/drain electrodes and the oxide semiconductor thin film layer on the substrate; Fig. 6B is a cross sectional view of the thin film transistor after formation of the first gate insulator; Fig. 6C is a cross sectional view of the thin film transistor after 20 patterning of the oxide semiconductor thin film layer and the gate insulator; Fig. 6D is a cross sectional view of the thin film transistor after formation of the second gate insulator; Fig. 6E is a cross sectional view of the thin film transistor after formation of the gate electrode and patterning of the first gate insulator and the second gate insulator; and Fig. 6F is a cross sectional 25 view of the thin film transistor after formation of the interlayer insulator;

Fig. 7 is a cross-sectional view of the thin film transistor according to the fourth embodiment of the present invention;

Fig. 8 is a cross-sectional view of the thin film transistor according to the fifth embodiment of the present invention;

5 Fig. 9 is a cross-sectional view of the thin film transistor according to the sixth embodiment of the present invention;

Figs. 10A to 10E are cross sectional views of the thin film transistor sequentially showing a manufacturing method of the thin film transistor of the sixth embodiment. Fig. 10A is a cross sectional view of the thin film 10 transistor after formation of the gate electrode and the gate insulator; Fig. 10B is a cross sectional view of the thin film transistor after formation of the oxide semiconductor thin film layer and the first overcoat insulator; Fig. 10C is a cross sectional view of the thin film transistor after patterning of the oxide semiconductor thin film layer and the first overcoat insulator; Fig. 15 10D is a cross sectional view of the thin film transistor after formation of the second overcoat insulator and the contact holes; and Fig. 10E is a cross sectional view of the thin film transistor after formation of the pair of source/drain electrodes;

Fig. 11 is a graph showing (002) diffraction peak locations in zinc 20 oxide thin films formed under different film-formation pressures;

Fig. 12 is a graph showing the dependency of the lattice spacing d_{002}, which is calculated from X-ray diffraction results, on the film-formation pressure under different gas flow rates;

Fig. 13 is a graph showing the dependency of the sheet resistance of 25 zinc oxide thin films on the heat treatment temperatures;

Fig. 14 is a graph showing the drain current versus applied gate voltage;

Fig. 15 is a graph showing the dependency of the sheet resistance of ion-doped zinc oxide thin films on the heating treatment temperature,
5 comparing the zinc oxide thin films of different lattice spacings; and

Fig. 16 is a graph showing the structure of a conventional bottom gate thin film transistor.

DETAILED DESCRIPTION OF THE INVENTION

10 Embodiments of a semiconductor device according to the present invention will be described below using a thin film transistor, which is formed on a substrate, as an example of the semiconductor device. The term "semiconductor device" as used herein refers to a structure including a substrate, and specifically to a device in which at least one semiconductor
15 element (e.g., thin film transistor), which does not include a substrate, is formed on a substrate. It should be understood that the semiconductor device according to the present invention is not limited by the embodiments described below. For example, the semiconductor elements are not limited to thin film transistors but may be other semiconductor elements such as
20 diodes or photoelectric conversion elements. The structure of thin film transistors is not limited by the embodiments shown below.

In the following description, orientations of zinc oxide are represented by the Miller indices, such as (002) preferred orientation. The Miller index (002) corresponds to (0002) preferred orientation represented
25 by an index for the hexagonal crystal system.

The term "intrinsic zinc oxide" as used herein refers to zinc oxide that contains substantially no impurities. The term "dope" as used herein refers to a process of introducing ions and includes an ion-implantation process.

5

First Embodiment

Fig. 1 shows the structure of a thin film transistor 100 according to the first embodiment of the present invention. Thin film transistor 100, which has a top-gate structure, is supported on substrate 1, and includes: a
10 pair of source/drain electrodes 2, an oxide semiconductor thin film layer 3, a first gate insulator 4, contact parts 5a, a pair of external source/drain electrodes 2a, a second gate insulator 6, a gate electrode 7, and a display electrode 8.

The pair of source/drain electrodes 2 are formed on substrate 1.
15 Source/drain electrodes 2 are spaced apart from each other on the upper surface of substrate 1.

Oxide semiconductor thin film layer 3 is formed on substrate 1 and the pair of source/drain electrodes 2. Oxide semiconductor thin film layer 3 is arranged such that a channel is formed between a source electrode and a
20 drain electrode of source/drain electrodes 2. Oxide semiconductor thin film layer 3 is formed by an oxide semiconductor mainly comprising zinc oxide.

In Fig. 1, oxide semiconductor thin film layer 3 is shown as having a thinner portion on the pair of source/drain electrodes 2 and a thicker portion between the pair of source/drain electrodes 2, for convenience of illustration.
25 However, the thinner portion and the thicker portion of oxide semiconductor thin film layer 3 actually have a substantially identical thickness. In other

words, oxide semiconductor thin film layer 3 has a substantially constant thickness on the pair of source/drain electrodes 2 and between the pair of source/drain electrodes 2. This is also true in other drawings described below.

5 The (002) lattice planes of the zinc oxide used in oxide semiconductor thin film layer 3 according to the present invention have a preferred orientation along a direction perpendicular to substrate 1 and a lattice spacing d_{002} of at least 2.619Å. Accordingly, oxide semiconductor thin film layer 3 has a high heat resistance.

10 The (002) lattice planes of single crystal zinc oxide have a lattice spacing d_{002} that is in a range from 2.602Å to 2.604Å. Single crystal zinc oxide therefore exhibits an insufficient heat resistance. If such single crystal zinc oxide having an insufficient heat resistance is used in a top gate thin film transistor having the structure described above, the heat history 15 during formation of gate insulator 4 would cause desorption of zinc and oxygen from the zinc oxide near the surface of oxide semiconductor thin film layer 3 (channel region). The desorption of zinc and oxygen from oxide semiconductor thin film layer 3 causes defects which worsen the film quality of oxide semiconductor thin film layer 3. Such defects form electrically 20 shallow impurity levels and reduce the resistance of oxide semiconductor thin film layer 3. In this situation, thin film transistor 100 operates in a normally-on mode or a depletion mode. Such operation results in increased defect levels, a smaller threshold voltage, and an increased leak current.

The lattice spacing d_{002} of oxide semiconductor thin film layer 3 25 according to the present invention is at least 2.619Å. The oxide semiconductor thin film layer 3 having such a lattice spacing d_{002} exhibits

an excellent heat resistance. In other words, it is possible to suppress desorption of oxygen and zinc and to prevent a decrease in the resistance of oxide semiconductor thin film layer 3. Therefore, leak current in thin film transistor 100 is suppressed.

5 More preferably, the lattice spacing d_{002} of oxide semiconductor thin film layer 3 is at least 2.625Å. Since such oxide semiconductor thin film layer 3 has an improved heat resistance, leak current in thin film transistor 100 is suppressed. The effect of the lattice spacing and the heat resistance on TFT performance will be described in the EXAMPLES section below.

10 First gate insulator 4 is formed to coat only the upper surface of oxide semiconductor thin film layer 3. First gate insulator 4 constitutes a part of a gate insulator. First gate insulator 4 functions not only as a gate insulator but also as a protective film that protects oxide semiconductor thin film layer 3 from etching by a resist stripper that is used to remove a
15 photoresist mask employed in etching oxide semiconductor thin film layer 3.

Second gate insulator 6 is formed to coat the entire exposed surfaces of source/drain electrodes 2, oxide semiconductor thin film layer 3, and first gate insulator 4. By forming such second gate insulator 6, the upper surface of semiconductor thin film layer 3 is thoroughly coated with first
20 gate insulator 4 while the side surfaces of semiconductor thin film layer 3 are thoroughly coated with second gate insulator 6.

First gate insulator 4 and second gate insulator 6 may be a silicon oxide (SiO_x) film, a silicon oxide nitride (SiON) film, a silicon nitride (SiN) film, or a silicon nitride (SiN) film doped with oxygen using oxygen or a
25 compound containing oxygen. Preferably, first gate insulator 4 and second gate insulator 6 are formed by a silicon nitride (SiN) film doped with oxygen

using oxygen or compound (e.g. N_2O) containing oxygen. Such a doped silicon nitride film has a higher dielectric constant than silicon oxide compound (SiOx) or silicon oxide nitride (SiON).

First gate insulator 4 and second gate insulator 6 are formed, for
5 example, by means of plasma-enhanced chemical vapor deposition (PCVD).

External source/drain electrodes 2a are respectively connected to source/drain electrodes 2 through contact holes 5 via contact parts 5a.

Gate electrode 7 is formed on second insulator 6. Gate electrode 7 is configured to control electron density in oxide semiconductor thin film
10 layer 3 according to the gate voltage applied to thin film transistor 100.

Display electrode 8 is configured to apply a voltage to liquid crystal used in a liquid crystal display. Since display electrode 8 is required to have a high transmittance with respect to visible light, display electrode 8 is formed by a conductive oxide thin film containing indium tin oxide (ITO) or
15 the like. It should be understood that the display electrode 8 may be formed by a low resistance zinc oxide thin film of zinc oxide that is doped with dopants such as Al and Ga.

Referring to Figs. 2A to 2G, a manufacturing method of the thin film transistor 100 according to the first embodiment of the present invention
20 will be described below.

Referring to Fig. 2A, a thin metal film is formed on substrate 1, and is then patterned by means of photolithography to form the pair of source/drain electrodes 2.

Referring to Fig. 2B, an intrinsic ZnO semiconductor thin film as
25 oxide semiconductor thin film layer 3 is formed by means of magnetron sputtering on all of the exposed surfaces of substrate 1 and the pair of the

source/drain electrodes 2 to have a thickness of 50 to 100 nm. First gate insulator 4 is formed on oxide semiconductor thin film layer 3 using a technique and condition(s) that do not reduce the resistance of oxide semiconductor thin film layer 3. It is preferable to form first gate insulator 4 at a temperature of 250°C or below.

According to one example of the film formation conditions of semiconductor thin film layer 3 of the present embodiment, semiconductor thin film layer 3 may be formed by way of radio-frequency magnetron sputtering using a mixed gas of argon and oxygen as a source gas.

The film formation conditions of oxide semiconductor thin film layer 3 according to the present invention are controlled such that the (002) lattice planes of oxide semiconductor thin film layer 3, in the as-deposited state, have a lattice spacing d_{002} of at least 2.619Å, while the lattice spacing d_{002} of single crystal zinc oxide is in a range from about 2.602Å to 2.604Å.

Specifically, a lower film-formation pressure results in a larger lattice spacing d_{002}. In addition, if Ar and O_2 are used as source gases in forming a zinc oxide film, a lower Ar/O_2 flow ratio (flow ratio of Ar to O_2) results in a larger lattice spacing d_{002}. Control of the lattice spacing d_{002} will be described in detail in the EXAMPLES section below.

Oxide semiconductor thin film layer 3 experiences a heat history during formation of first gate insulator 4. However, the high heat resistance of oxide semiconductor thin film layer 3 having a lattice spacing of at least 2.619Å according to the present invention suppresses desorption of oxygen and zinc from oxide semiconductor thin film layer 3 during formation of first gate insulator 4, whereby a decrease in the resistance of

oxide semiconductor thin film layer 3 is prevented. Accordingly, leak current in thin film transistor 100 is suppressed.

Referring to Fig. 2C, a photoresist is coated and patterned on first gate insulator 4 so as to form a photoresist 4a. Using photoresist 4a as a mask, first gate insulator 4 is dry-etched. Then oxide semiconductor thin film layer 3 is wet-etched.

Fig. 2D shows a cross section of thin film transistor 100 after removal of photoresist 4a, subsequent to wet-etching of oxide semiconductor thin film layer 3. In thin film transistor 100, a TFT active layer region including first gate insulator 4 is formed in a self-aligning manner with respect to oxide semiconductor thin film layer 3. First gate insulator 4 is configured not only to form an interface with oxide semiconductor thin film layer 3 but also to protect oxide semiconductor thin film layer 3 during patterning of the active region. Specifically, gate insulator 4 protects oxide semiconductor thin film layer 3 from various agents (e.g., resist stripper) used in a photolithography process. Without first gate insulator 4, the resist stripper, which is used for removal of photoresist 4a after the patterning of the active layer, contacts and roughens the surface and the grain boundaries of oxide semiconductor thin film layer 3. The presence of first gate insulator 4 on oxide semiconductor thin film layer 3 prevents roughening of the surface and the grain boundaries of oxide semiconductor thin film layer 3.

First gate insulator 4 and oxide semiconductor thin film layer 3 may be processed using other methods than the above-mentioned methods. For example, both the first gate insulator and the oxide semiconductor thin film layer may be dry-etched or wet-etched.

As shown in FIG. 2E, after patterning of the TFT active region, second gate insulator 6 is formed on the entire exposed surfaces of substrate 1, source/drain electrodes 2, oxide semiconductor thin film layer 3, and first gate insulator 4 such that second gate insulator 6 coats first gate insulator 4 and source/drain electrodes 2. Then contact holes 5 are opened in second gate insulator 6 to expose portions of source/drain electrodes 2. It is preferable to form second gate insulator 6 under the same conditions as those employed in forming first gate insulator 4.

Lastly, referring to Fig. 2F, gate electrode 7 is formed by a metal film on second gate insulator 6. Then external source/drain electrodes 2a are formed by the same material as gate electrode 7. External source/drain electrodes 2a are respectively connected to source/drain electrodes 2 through contact holes 5 via contact parts 5a. Display electrode 8 is formed in the final step to form TFT 100 according to the first embodiment of the present invention.

Although it has been described above that the (002) lattice planes of the entire oxide semiconductor thin film layer 3 have a preferred orientation along a direction perpendicular to substrate 1 and a lattice spacing d_{002} of at least 2.619Å, the orientation and the lattice spacing of zinc oxide vary depending on the material on which the zinc oxide is formed into a film. In thin film transistor 100, a portion of oxide semiconductor thin film layer 3 that is in contact with substrate 1 (a portion that is positioned between the pair of source/drain electrodes 2) may have a different orientation and a different lattice spacing from the other portion of oxide semiconductor thin film layer 3 that is in contact with the pair of source/drain electrodes 2. In this case, at least the portion that is in contact with substrate 1 should have

a lattice spacing d_{002} of at least 2.619Å and maintain a high resistance. Since a channel is formed above the portion that is in contact with substrate 1, the leak current in thin film transistor 100 is suppressed by maintaining the high resistance of the portion that is in contact with substrate 1.

5

Second Embodiment

Next, a thin film transistor 200 according to the second embodiment of the present invention will be described. In the following description, 10 parts that are similar to or the same as parts described above with respect to the thin film transistor 100 of the first embodiment will be identified with the same reference numerals as used above with respect to the thin film transistor 100 according to the first embodiment, and description of these parts will be omitted.

15 Fig. 3 shows a cross section of thin film transistor 200 according to the second embodiment of the present invention. Thin film transistor 200 is formed on a substrate 1, and includes: a pair of source/drain electrodes 2, a pair of contact layers 10, an oxide semiconductor thin film layer 3, a first gate insulator 4, contact parts 5a, a pair of external source/drain electrodes 20 2a, a second gate insulator 6, a gate electrode 7, and a display electrode 8. These layers are combined in this order as shown in Fig. 3. As compared to thin film transistor 100, thin film transistor 200 additionally includes a pair of contact layers 10 between the pair of source/drain electrodes 2 and oxide semiconductor thin film layer 3.

25 The pair of contact layers 10 are mainly formed of zinc oxide and are formed to be in contact with oxide semiconductor thin film layer 3.

Specifically, the pair of contact layers 10 are respectively formed on source/drain electrodes 2. Oxide semiconductor thin film layer 3 is formed on contact layers 10 and between contact layers 10 between source/drain electrodes 2 so as to provide a channel between a source electrode and a
5 drain electrode of source/drain electrodes 2. In this way, contact layers 10 are formed between oxide semiconductor thin film layer 3 and the pair of source/drain electrodes 2 to connect oxide semiconductor thin film layer 3 and the pair of source/drain electrodes 2.

In thin film transistor 200, the (002) lattice planes of the zinc oxide
10 used in oxide semiconductor thin film layer 3 and the pair of contact layers 10 have a preferred orientation along a direction perpendicular to substrate 1. Since both oxide semiconductor thin film layer 3 and the pair of contact layers 10 are zinc oxide having (002) planes with a preferred orientation, it is possible to form these layers using an identical target. Therefore, it is
15 possible to form oxide semiconductor thin film layer 3 and contact layers 10 using an identical apparatus. This eliminates the need to provide another apparatus to form the pair of contact layers 10.

The lattice spacing d_{002} of oxide semiconductor thin film layer 3 is at least 2.619Å. The high heat resistance of oxide semiconductor thin film
20 layer 3 having such a lattice spacing d_{002} reduces effects of the heat treatment during, for example, formation of first gate insulator 4. Therefore it is possible to suppress the occurrence of defects that form shallow impurity levels in oxide semiconductor thin film layer 3 so as to prevent a decrease in the resistance of oxide semiconductor thin film layer 3.
25 Thus, leak current in thin film transistor 200 is suppressed.

The lattice spacing d_{002} of the pair of contact layers 10 is controlled to be smaller than the lattice spacing d_{002} of oxide semiconductor thin film layer 3. Therefore, the heat resistance of the pair of contact layers 10 is lower than the heat resistance of oxide semiconductor thin film layer 3.
5 Accordingly, the heat treatment during, for example, formation of first gate insulator 4 causes more defects in the pair of contact layers 10 than in oxide semiconductor thin film layer 3. The presence of more defects in the pair of contact layers 10 reduces the resistance of the pair of contact layers 10 below the resistance of oxide semiconductor thin film layer 3. This
10 improves the contact between the pair of source/drain electrodes 2 and oxide semiconductor thin film layer 3 as well as the current driving capability of thin film transistor 200.

Specifically, it is preferable that the lattice spacing d_{002} of the pair of contact layers 10 is 2.605Å or below. Contact layers 10 having a lattice
15 spacing d_{002} of 2.605Å or below have a sufficiently lower heat resistance than oxide semiconductor thin film layer 3, which as described above has a lattice spacing d_{002} of at least 2.619Å. Accordingly, after the heat treatment the resistance of the pair of contact layers 10 is lower than the resistance of oxide semiconductor thin film layer 3. This improves the
20 contact between the pair of source/drain electrodes 2 and oxide semiconductor thin film layer 3 as well as the current driving capability of thin film transistor 200.

More preferably, the lattice spacing d_{002} of oxide semiconductor thin film layer 3 is at least 2.625Å. Oxide semiconductor thin film layer 3
25 having a lattice spacing d_{002} of at least 2.625Å has a further improved heat resistance. Therefore, even if oxide semiconductor thin film layer 3 is

subjected to a more intensive heat history, the resistance of oxide semiconductor thin film layer 3 is not significantly reduced (see the more detailed discussion in the EXAMPLES section below). Thus, leak current in thin film transistor 200 is suppressed.

5 If the lattice spacing d_{002} of oxide semiconductor thin film layer 3 is at least 2.625Å, it is preferable that the lattice spacing d_{002} of contact layers 10 is 2.619Å or below. In this case, the heat resistance of contact layers 10 is lower than the heat resistance of oxide semiconductor thin film layer 3. Accordingly, after the heat treatment the resistance of the pair of contact
10 layers 10 is lower than the resistance of oxide semiconductor thin film layer 3. This provides better contact between the pair of source/drain electrodes 2 and oxide semiconductor thin film layer 3. Therefore, thin film transistor 200 has a high current driving capability.

If the lattice spacing d_{002} of oxide semiconductor thin film layer 3 is
15 at least 2.625Å, it is more preferable that the lattice spacing d_{002} of contact layers 10 is 2.605Å or below. In this case, the heat resistance of the pair of contact layers 10 is further reduced, and therefore the resistance of the pair of contact layers 10 having such a lattice spacing is more significantly reduced by a heat treatment. As a result, better contact between the pair
20 of source/drain electrodes 2 and oxide semiconductor thin film layer 3 is provided.

The effect of the lattice spacing d_{002} of zinc oxide used as a main component of the pair of contact layers 10 and oxide semiconductor thin film layer 3 on the resistance of these layers will be described in detail in the
25 EXAMPLES section below.

Next, the manufacturing method of thin film transistor 200 according to the second embodiment of the present invention will be described with reference to Figs. 4A to 4E.

The pair of source/drain electrodes 2 are formed on substrate 1. Then, a contact layer of zinc oxide is formed to have a 10 to 100 nm thickness on all of the exposed surfaces of respective source/drain electrodes 2 and substrate 1. The contact layer of zinc oxide is then patterned so as to form the pair of contact layers 10 on the respective source/drain electrodes 2 with a gap therebetween in the region between the pair of source/drain electrodes 2, as shown in FIG. 4A.

Referring to Fig. 4B, oxide semiconductor thin film layer 3 of zinc oxide is formed on all of the exposed surfaces of substrate 1 and the pair of contact layers 10 to have a thickness of 50 to 100 nm.

The pair of contact layers 10 and the oxide semiconductor thin film layer 3 are formed by means of, for example, magnetron sputtering. The conditions used in these film formations are controlled such that (002) planes of oxide semiconductor thin film layer 3 and the pair of contact layers 10, in the as-deposited state, have a preferred orientation along a direction perpendicular to substrate 1. The film formation conditions are further controlled such that oxide semiconductor thin film layer 3, in the as-deposited state, has a lattice spacing d_{002} of at least 2.619Å and such that the pair of contact layers 10, in the as-deposited state, have a lattice spacing d_{002} that is smaller than the lattice spacing d_{002} of oxide semiconductor thin film layer 3, in the as-deposited state. (See the disclosure of the preferred relationship between the respective lattice spacings d_{002} of the pair of contact layers 10 and the oxide semiconductor thin film layer 3 above.)

The lattice spacing d_{002} may be controlled by varying the film-formation pressure or the gas flow ratio as mentioned above with respect to the first embodiment.

Specifically, a lower film-formation pressure results in a larger lattice spacing d_{002}. Thus, if the oxide semiconductor thin film layer 3 is formed with a film-formation pressure that is lower than the film-formation pressure used when forming the pair of contact layers 10, the oxide semiconductor thin film layer 3 will have a larger lattice spacing d_{002} than the lattice spacing of the pair of contact layers 10. In addition, if Ar and O_2 are used as source gases in forming a zinc oxide film, a lower Ar/O_2 flow ratio (flow ratio of Ar to O_2) results in a larger lattice spacing d_{002}. Control of the lattice spacing d_{002} will be described in detail in the EXAMPLES section below.

The oxide semiconductor thin film layer 3 and the pair of contact layers 10 are both of zinc oxide. The lattice spacing d_{002} of oxide semiconductor thin film layer 3 and contact layers 10 is controlled by modifying film formation conditions. In other words, it is possible to form oxide semiconductor thin film layer 3 and the pair of contact layers 10 by using an identical apparatus under different conditions. Therefore, no additional apparatus is needed to form the pair of contact layers 10 when forming thin film transistor 200 having the pair of contact layers 10.

Referring to Fig. 4C, first gate insulator 4 is formed on oxide semiconductor thin film layer 3. During formation of first gate insulator 4, oxide semiconductor thin film layer 3 and contact layers 10 experience a heat history. As described above, the lattice spacing d_{002} of oxide semiconductor thin film layer 3, in the as-deposited state, is larger than the

lattice spacing d_{002} of contact layers 10, in the as-deposited state. Therefore, oxide semiconductor thin film layer 3 has a higher heat resistance than contact layers 10. Accordingly, the resistance of the pair of contact layers 10 is reduced by the heat history during the formation of first gate insulator 4, while oxide semiconductor thin film layer 3 maintains a high resistance.

Contact layers 10 have a lower resistance than oxide semiconductor thin film layer 3. Providing contact layers 10 having the lower resistance helps to provide better contact between the pair of source/drain electrodes 2 and oxide semiconductor thin film layer 3.

Further, oxide semiconductor thin film layer 3 maintains a high resistance through the heat history to suppress the leak current in thin film transistor 200.

After formation of first gate insulator 4, a photoresist is formed on first gate insulator 4. Using the photoresist as a mask, first gate insulator 4, oxide semiconductor thin film layer 3, and the pair of contact layers 10 are etched.

Fig. 4D shows a cross section of thin film transistor 200 after removal of the photoresist subsequent to the etching. Thin film transistor 200 as shown in Fig. 4D has a TFT active layer region that includes first gate insulator 4 formed in a self-aligning manner with respect to semiconductor thin film layer 3. First gate insulator 4 is configured not only to form an interface with oxide semiconductor thin film layer 3 but also to protect oxide semiconductor thin film layer 3 during patterning of the active region. Specifically, gate insulator 4 protects oxide semiconductor thin film layer 3 from various agents (e.g., resist stripper) used in a

photolithography process. Without first gate insulator 4, the resist stripper, which is used for removal of photoresist 4a after the patterning of the active layer, contacts and roughens the surface and the grain boundaries of oxide semiconductor thin film layer 3. The presence of first gate
5 insulator 4 on oxide semiconductor thin film layer 3 prevents the surface and the grain boundaries of oxide semiconductor thin film layer 3 from roughening.

Referring to Fig. 4E, second gate insulator 6 is then formed on all of the exposed surfaces of substrate 1, the pair of source/drain electrodes 2, the
10 pair of contact layers 10, oxide semiconductor thin film layer 3, and first gate insulator 4, such that second gate insulator 6 coats first gate insulator 4 and source/drain electrodes 2. Then contact holes 5 are opened in second gate insulator 6 to expose portions of source/drain electrodes 2. It is preferable to form second gate insulator 6 under the same conditions used to
15 form first gate insulator 4.

Lastly, gate electrode 7 is formed by a metal film on second gate insulator 6. Then external source/drain electrodes 2a are formed by the same material as gate electrode 7. External source/drain electrodes 2a are respectively connected to source/drain electrodes 2 through contact holes 5
20 via contact parts 5a. Display electrode 8 is formed (see Fig. 3) in the final step to form a TFT 200 according to second embodiment of the present invention.

In a similar manner to the first embodiment described above, the orientation and the lattice spacing of the oxide semiconductor thin film
25 layer 3 and contact layers 10 of TFT 200 vary depending on the underlying layer. The (002) planes of at least a portion of oxide semiconductor thin

film layer 3 that is in contact with substrate 1 (a portion that is positioned between the pair of source/drain electrodes 2) and at least a portion of contact layers 10 that is in contact with substrate 1 (a portion that is positioned between the pair of source/drain electrodes 2) should have a
5 preferred orientation along a direction perpendicular to substrate 1 and a lattice spacing d_{002} of at least 2.619Å in order to maintain a high resistance in an area in which a channel is formed. This further provides better contact between the pair of source/drain electrodes 2 and oxide semiconductor thin film layer 3.

10 Although the thin film transistor 200 of the second embodiment has been described as being a top gate thin film transistor, the thin film transistor 200 having contact layers 10 according to the second embodiment of the present invention may be a top gate thin film transistor of a different structure or a bottom gate thin film transistor.

15

Third to Sixth Embodiments

Next, thin film transistors according to the third to sixth embodiments of the present invention will be described.

Oxide semiconductor thin film layer 3 of the thin film transistors
20 according to the third to sixth embodiments includes a first region of intrinsic zinc oxide and second regions doped with donor ions. The first region is a channel region of the oxide semiconductor thin film layer 3 and the second regions are included in a pair of source/drain regions that define the channel region therebetween. The term "intrinsic zinc oxide" as used
25 herein refers to zinc oxide that contains substantially no impurities. The

term "dope" as used herein refers to a process of introducing ions and includes an ion-implantation process.

Third Embodiment

5 Fig.5 shows thin film transistor 300 according to the third embodiment of the present invention. Thin film transistor 300 is a so-called staggered thin film transistor, which is supported on a substrate 1, and includes: a pair of source/drain electrodes 2 formed on substrate 1 and spaced apart from each other, oxide semiconductor thin film layer 3, a first 10 gate insulator 4, a second gate insulator 6, a gate electrode 7, an interlayer insulator 9, contact parts 5a, a pair of external source/drain electrodes 2a, and a display electrode 8. First gate insulator 4 and second gate insulator 6 are indicated by different numerals because they are formed by separate steps in a manufacturing process of thin film transistor 300.

15 Oxide semiconductor thin film layer 3 of zinc oxide is arranged to form a channel between a source electrode and a drain electrode of the pair of source/drain electrodes 2.

The (002) planes of the zinc oxide used in oxide semiconductor thin film layer 3 have a preferred orientation and a lattice spacing d_{002} of at least 20 2.619Å. Accordingly, oxide semiconductor thin film layer 3 has a high heat resistance.

The high heat resistance of oxide semiconductor thin film layer 3 suppresses desorption of oxygen and zinc and also prevents a decrease in the resistance of oxide semiconductor thin film layer 3. Therefore, leak 25 current in thin film transistor 300 is suppressed.

More preferably, the lattice spacing d_{002} of oxide semiconductor thin film layer 3 is at least 2.625Å. Since semiconductor thin film layer 3 having such a lattice spacing d_{002} has a further improved heat resistance, leak current in thin film transistor 300 is further suppressed.

5 Oxide semiconductor thin film layer 3 has a channel region 31 (the first region) and a pair of source/drain regions 32 (regions including the second regions). Channel region 31 is located directly below gate electrode 7 (as shown in Fig. 5) and functions as a channel.

The pair of source/drain regions 32 are the regions of oxide

10 semiconductor thin film layer 3 other than channel region 31. Source/drain regions 32 include the second regions, which are doped with donor ions and exhibit a low resistance. In the thin film transistor 300 according to the third embodiment, the entire areas of source/drain regions 32 are the second regions having a decreased resistance.

15 By providing source/drain regions 32, it is possible to suppress a parasitic resistance from the pair of source/drain electrodes 2 to the channel as well as current rate degradation. After being ion-doped, the pair of source/drain regions 32 are subjected to an activation treatment in order to reduce the resistance of the pair of source/drain regions 32. The method of

20 reducing the resistance of the pair of source/drain regions 32 will be described in detail later.

First gate insulator 4 is formed to coat only the upper surface of channel region 31 of oxide semiconductor thin film layer 3 whereas second gate insulator 6 is formed to coat only the upper surface of first gate

25 insulator 4. First gate insulator 4 and second gate insulator 6 may be a silicon oxide (SiOx) film, a silicon oxide nitride (SiON) film, a silicon nitride

(SiN_x) film, or a silicon nitride (SiN_x) film doped with oxygen using oxygen or a compound containing oxygen. Also, first gate insulator 4 and second gate insulator 6 may be an aluminum oxide (AlO_x) film.

Gate electrode 7 is formed on second gate insulator 6. Preferably, 5 each end of gate electrode 7 is coincident with one of the inner ends of the pair of source/drain regions 32 along the film thickness direction. This reduces a parasitic capacitance between source/drain regions 32 and gate electrode 7 so as to improve the circuit speed of thin film transistor 300. Preferably, gate electrode 7 is narrower than the spacing between the inner 10 ends of the pair of source/drain electrodes 2. This reduces a parasitic capacitance between source/drain regions 32 and gate electrode 7 so as to suppress a decrease in the circuit speed of thin film transistor 300.

Interlayer insulator 9 is formed to coat all of the exposed surfaces of the pair of source/drain electrodes 2, the pair of source/drain regions 32, and 15 gate electrode 7. Interlayer insulator 9 is configured not only to protect thin film transistor 300 but also to heat the pair of source/drain regions 32. This reduces the resistance of the pair of source/drain regions 32.

External source/drain electrodes 2a are respectively connected to source/drain electrodes 2 through contact holes 5 via contact parts 5a.

20 Display electrode 8 is configured to apply a voltage to liquid crystal used in a liquid crystal display.

Referring to Fig. 6, a manufacturing method of thin film transistor 300 according to the third embodiment will be described.

As shown in Fig. 6A, a semiconductor thin film of zinc oxide is 25 formed on all of the exposed surfaces of substrate 1 and the pair of source/drain electrodes 2 to have a thickness of, for example, 50 to 100 nm.

According to one example of the film formation conditions of semiconductor thin film layer 3 of the third embodiment, semiconductor thin film layer 3 may be formed by way of radio-frequency magnetron sputtering using a mixed gas of argon and oxygen as a source gas.

5 The film formation conditions of oxide semiconductor thin film layer 3 according to the present invention are controlled such that the lattice spacing d_{002} of oxide semiconductor thin film layer 3, in the as-deposited state, is at least 2.619Å. Specifically, the lattice spacing d_{002} may be increased by reducing a film-formation pressure or Ar/O_2 flow ratio.

10 Next, as shown in Fig. 6B, first gate insulator 4 is formed on oxide semiconductor thin film layer 3. During formation of first gate insulator 4, oxide semiconductor thin film layer 3 experiences a heat history. Oxide semiconductor thin film layer 3 according to this embodiment has a lattice spacing d_{002} of at least 2.619Å and exhibits a high heat resistance. The 15 high heat resistance of oxide semiconductor thin film layer 3 prevents the heat history during the formation of first gate insulator 4 from causing desorption of oxygen and zinc from oxide semiconductor thin film layer 3, so as to suppress leak current in thin film transistor 300. Specifically, the high heat resistance of oxide semiconductor thin film layer 3 reduces 20 limitations on the temperature and the time for treating first gate insulator 4. For example, even if thin film transistor 300 is formed at a comparatively high temperature, thin film transistor 300 becomes excellent in suppression of leak current.

Preferably, the film formation temperature of first gate insulator 25 film 4 is 250°C or below. The film formation temperature may be determined according to the lattice spacing d_{002} and other conditions of

oxide semiconductor thin film layer 3 as well as the desired TFT properties in order to prevent a decrease in the resistance of oxide semiconductor thin film layer 3.

Oxide semiconductor thin film layer 3 and first gate insulator 4 are
5 patterned collectively. The collective patterning of oxide semiconductor thin film layer 3 and first gate insulator 4 makes it possible to protect the surface of oxide semiconductor thin film 3 from a resist stripper or the like. The resist stripper is used in, for example, removing a resist for patterning. Fig. 6C shows thin film transistor 300 after the patterning of oxide
10 semiconductor thin film layer 3 and first gate insulator 4.

As shown in Fig. 6D, after the patterning of oxide semiconductor thin film layer 3 and first gate insulator 4, second gate insulator 6 is formed.

Gate electrode 7 is then formed on second gate insulator 6. Using gate-electrode 7 as a mask, first gate insulator 4 and second gate insulator 6
15 are dry-etched using gas such as SF_6.

Fig. 6E shows a cross section of thin film transistor 300 after dry-etching of first gate insulator 4 and second gate insulator 6. As shown in Fig. 6E, first gate insulator 4, second gate insulator 6, and gate electrode 7 are formed in a self-aligning manner. Since oxide semiconductor thin
20 film layer 3 is not etched in the dry-etching, each end of oxide semiconductor thin film layer 3 is not coated by first gate insulator 4, such that the ends of the oxide semiconductor thin film layer 3 are in an uncovered state.

After the patterning of first gate insulator 4 and second gate insulator 6, source/drain regions 32 are doped with ions that function as
25 donors for zinc oxide through the full thickness of semiconductor thin film

layer 3. Source/drain regions 32 are unmasked regions that are adjacent to the channel region 31 masked with gate electrode 7.

The donor ions include, for example, ions obtained by ionizing group III elements. The group III elements may be at least one of indium, gallium, aluminum, and the like.

Preferably, the ion-implantation technique is used in the doping. In the ion-implantation technique, accelerated ions with energies of several keV to several MeV are irradiated and doped to a target object. Using the ion-implantation technique, it is possible to dope source/drain regions 32 with the ions after oxide semiconductor thin film layer 3 is formed. In addition, the ion-doping results in interfaces between the doped region and the undoped region being coincident with the edges of first gate insulator 4, respectively as shown in Fig. 6F.

The donor ions may be, for example, ions obtained by ionizing at least one of hydrogen (H), helium (He), neon (Ne), argon (Ar), krypton (Kr), fluorine (F), xenon (Xe), and oxygen (O). Since it is easy to obtain these ions by way of plasma decomposition or the like, mass segregation is not required to dope the ions to a large area.

The pair of source/drain regions 32 according to this embodiment are in an uncovered state. The ions are doped directly to the pair of source/drain regions 32 and not through first gate insulator 4 or second gate insulator 6. This reduces an acceleration voltage used in the doping so as to reduce damages caused by the ion-doping to other regions than the pair of source/drain regions 32.

Now the mechanism of the decrease in resistance of the pair of source/drain regions 32 will be explained.

The decrease in the resistance of the pair of source/drain electrodes 32 is caused by replacing oxygen and zinc (i.e., components of zinc oxide) with the doped ions, which are caused to enter lattice locations of zinc oxide. The entry of the doped ions to lattice locations of zinc oxide is referred to as 5 activation of ions, and is caused by an activation treatment. If oxide semiconductor thin film layer 3 has a lattice spacing d_{002} of 2.602Å to 2.604Å, which is similar to the lattice spacing of so-called single crystal zinc oxide, the activation of the ions doped in oxide semiconductor thin film layer 3 is easily caused by an activation treatment such as a heat treatment at a 10 relatively low temperature. However, in zinc oxide with a larger lattice spacing d_{002} (as in the structure of the present invention), the doped ions are less likely to enter lattice locations of the zinc oxide. In other words, ion activation is less likely to occur. In this case, the pair of source/drain regions 32 of oxide semiconductor thin film layer 3 are subjected to a heat 15 treatment (activation treatment) at a higher temperature to cause the activation of the ions doped in these regions. In other words, a heat treatment at a higher temperature allows the doped ions occupying interstitial sites to enter lattice sites to be electrically activated. Therefore, it is possible to selectively reduce the resistance of the pair of source/drain 20 regions 32 so as to suppress a parasitic resistance from the pair of source/drain electrodes 2 to the channel as well as current rate degradation.

The required temperature in the heat treatment applied to the pair of source/drain regions 32 to activate the ions depends on the lattice spacing d_{002} of oxide semiconductor thin film layer 3 (the lattice spacing d_{002} of the 25 pair of source/drain regions 32) and the doping amount of the ions. If the lattice spacing d_{002} of oxide semiconductor thin film layer 3 is at least

2.625Å, the temperature of the heat treatment is preferably at least 250°C, and more preferably, at least 300°C. A heat treatment at such temperatures securely reduces the resistance of source/drain regions 32. The heat treatment as an activation treatment of the pair of source/drain
5 regions 32 adds a heat history also to channel region 31. However, channel region 31 has a lattice spacing d_{002} of at least 2.619Å (in this example, at least 2.625Å) and exhibits a high heat resistance. Therefore, channel region 31 maintains a high resistance through the heat history.

Although the activation treatment has been explained using heat
10 treatment as an example, the activation treatment may be laser irradiation or the like. If a laser irradiation is performed as the activation treatment, only the pair of source/drain regions 32 are irradiated with a laser beam and the pair of source/drain regions 32 are thus selectively activated. The laser used in the laser irradiation may be, for example, ultraviolet, infrared,
15 visible light, and the like. Particularly, ultraviolet light with at least 3.3eV energy is effectively used because it exhibits a high absorption rate to zinc oxide. Since the pair of source/drain regions 32 are in an uncovered state, it is possible for a laser to directly irradiate the pair of source/drain regions 32. Thus it is easy to activate the pair of source/drain regions 32.

20 In thin film transistor 300 according to the third embodiment of the present invention, first gate insulator 4 and second gate insulator 6 are temporarily formed on the pair of source/drain regions 32 before the ion-doping to the pair of source/drain regions 32 (see Figs. 6B to 6D). The resistance of the pair of source/drain regions 32 that have experienced such
25 processes is easily reduced by the ion-doping. This is because the heat history during the formation of first gate insulator 4 and second gate

insulator 6 makes the pair of source/drain regions 32 more likely to be activated.

An insulator may be formed on the pair of source/drain regions 32, which are in an uncovered state according to the third embodiment. In
5 this case, the heat history during the formation of the insulator activates the pair of source/drain regions 32 and reduces their resistance.

Specifically, as shown in Fig. 6F, formation of interlayer insulator 9 adds a heat history to the pair of source/drain regions 32. If the resistance of the pair of source/drain regions 32 is sufficiently reduced in the formation
10 of interlayer insulator 9, the above-described activation treatment may not be required, so as to simplify the manufacturing process.

A reduction process may be performed as the activation treatment of the pair of source/drain regions 32. Specifically, interlayer insulator 9 is formed by means of plasma CVD to subject the pair of source/drain regions
15 32 to a reduction atmosphere of hydrogen or the like. In this treatment, only the pair of source/drain regions 32 are subjected to the reduction atmosphere without subjecting channel region 31 to the reduction atmosphere. This is possible because first gate insulator 4, second gate insulator 6, and gate electrode 7 overlie channel region 31. Therefore, it is
20 possible to selectively reduce the resistance of only the pair of source/drain regions 32.

Then contact holes are opened by means of photolithography in interlayer insulator 9 to expose portions of the pair of the source/drain electrodes 2. External source/drain electrodes 2a are respectively
25 connected to source/drain electrodes 2 through contact holes 5 via contact

parts 5a. In the final step to form the TFT 300, display electrode 8 is formed using, for example, indium tin oxide (ITO).

Although thin film transistor 300 as described above includes first gate insulator 4 and second gate insulator 6, thin film transistor 300 may have a single-layered gate insulator to protect the surface of oxide semiconductor thin film layer 3 from etching. In this case, oxide semiconductor thin film layer 3 is patterned before formation of the gate insulator. Then gate electrode 7 is placed on the gate insulator to use the gate electrode 7 as a mask in etching the gate insulator.

Similarly to thin film transistors 100 and 200, it is required in thin film transistor 300 that (002) planes of at least a portion of oxide semiconductor thin film layer 3 that is in contact with substrate 1 (a portion that is positioned between the pair of source/drain electrodes 2) have a preferred orientation along a direction perpendicular to substrate 1 and a lattice spacing d_{002} of at least 2.619Å. However, it is not necessary for entire oxide semiconductor thin film layer 3 to have these properties. Although thin film transistor 300 as described above is a top gate thin film transistor where gate electrode 7 is positioned above oxide semiconductor thin film layer 3, it may be a bottom gate thin film transistors where gate electrode 7 is positioned below oxide semiconductor thin film layer 3.

Fourth embodiment

Fig. 7 shows thin film transistor 400 according to the fourth embodiment. According to the fourth embodiment, thin film transistor 400 has gate insulators 4 and 6 which are configured to coat the entire upper surface of oxide semiconductor thin film layer 3. Thus, in contrast to the

structure of the third embodiment, in thin film transistor 400 according to the fourth embodiment, etching surfaces E defining all of the ends of gate insulators 4 and 6 are not coincident with the ends of gate electrode 7 along a film thickness direction.

5 If etching surfaces E defining every end of gate insulator 4 and 6 are coincident with corresponding ends of gate electrode 7, as in thin film transistor 300 according to the third embodiment, an electric current flows near rough surfaces E, resulting from the etching. This causes a problem of an increased leak current. With the structure of thin film transistor 400

10 according to the fourth embodiment, by contrast, etching surfaces E of gate insulator 4 and 6 are not coincident with the ends of gate electrode 7 along the film thickness direction such that no electric current flows through etching surfaces E. Therefore it is possible to prevent an increase in leak current due to the roughness of etching surfaces E.

15 The pair of source/drain regions 32 of thin film transistor 400 are not in an uncovered state during ion-doping of the pair of source/drain regions 32. In addition, surfaces of the pair of source/drain regions 32 are protected by first gate insulator 4 and second gate insulator 6 during formation of interlayer insulator 9. Although etching surfaces E of first

20 and second gate insulator 4 and 6 are formed in a self-aligning manner in the present embodiment with respect to the etching surfaces E of source/drain regions 32, the etching surfaces E may have a different shape. For example, etching surfaces E of gate insulator 6 and gate electrode 7 and etching surfaces of gate insulator 4 and source/drain regions 32 may be

25 formed in a self-aligning manner to obtain a similar effect as well as to reduce acceleration voltage during ion implantation.

Similarly to thin film transistors 100, 200 and 300, it is required in thin film transistor 400 that (002) planes of at least a portion of oxide semiconductor thin film layer 3 that is in contact with substrate 1 (a portion that is positioned between the pair of source/drain electrodes 2) have a preferred orientation along a direction perpendicular to substrate 1 and a lattice spacing d_{002} of at least 2.619Å. However, it is not necessary for entire oxide semiconductor thin film layer 3 to have these properties.

Although thin film transistor 400 as described above is a top gate thin film transistor where gate electrode 7 is positioned above oxide semiconductor thin film layer 3, it may be a bottom gate thin film transistors where gate electrode 7 is positioned below oxide semiconductor thin film layer 3.

Fifth Embodiment

In the staggered TFTs according to the above-described third and fourth embodiments, the full thickness of the pair of source/drain regions 32 must be doped with ions. However, sometimes it is impossible to dope the full thickness of the source/drain regions 32. For example, it is impossible to dope ions through the full thickness of a film using hydrogen (H), helium (He), neon (Ne), argon (Ar), krypton (Kr), fluorine (F), xenon (Xe), oxygen (O), or the like, even if the ion implantation technique is applied, although the ion implantation technique generally dopes ions to a deeper area of the film than other techniques. In addition, if the film has an excessive thickness, it is impossible to dope ions through the full thickness of a film.

In this case, a coplanar thin film transistor 500 as shown in Fig. 8 is used. The characteristic configurations of the staggered thin film

transistors may be applied to coplanar thin film transistor 500. In coplanar thin film transistor 500 according to the fifth embodiment of the present invention, a pair of source/drain electrodes 2 are formed respectively on a pair of source/drain regions 32. With this structure, even
5 a low resistance of only an upper surface of the pair of source/drain regions 32 helps to suppress current rate degradation between the pair of source/drain electrodes 2 and a channel region 31.

In a coplanar thin film transistor, the doping of hydrogen (H), helium (He), neon (Ne), argon (Ar), krypton (Kr), fluorine (F), xenon (Xe),
10 oxygen (O), or the like may be performed by ionizing these ions using plasma decomposition and then subjecting the pair of source/drain regions 32 to the plasma.

Although thin film transistor 500 as described above is a top gate thin film transistor where gate electrode 7 is positioned above oxide
15 semiconductor thin film layer 3, it may be a bottom gate thin film transistor where gate electrode 7 is positioned below oxide semiconductor thin film layer 3.

Sixth Embodiment

20 Fig. 9 shows bottom gate thin film transistor 600 according to the sixth embodiment of the present invention.

Thin film transistor 600 includes a gate electrode 7 formed on a substrate 1, a gate insulator 4 formed after the gate electrode 7 to coat gate electrode 7, an oxide semiconductor thin film layer 3 formed on gate
25 insulator 4, a first overcoat insulator 11 formed to coat an upper surface of oxide semiconductor thin film layer 3, a second overcoat insulator 12 formed

to coat side surfaces of oxide semiconductor thin film layer 3 (as well as first overcoat insulator 11), and a pair of source/drain electrodes 2. Gate insulator 4 of thin film transistor 600 has a single-layered structure. Similarly to thin film transistors 100 to 500, it is required in thin film transistor 600 that (002) planes of the zinc oxide used in oxide semiconductor thin film layer 3 have a preferred orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å.

In thin film transistor 600, oxide semiconductor thin film layer 3 is configured to have a connection area connected with the pair of source/drain electrodes 2. A portion of oxide semiconductor thin film layer 3 positioned inside the connection area functions as channel region 31. Outside portions of oxide semiconductor thin film layer 3 function as the pair of source/drain regions 32, which include an area having a lower resistance than channel region 31. More specifically, each of the pair of source/drain regions 32 has a connection area (an area connected with one of the source/drain electrodes 2) that has a resistance that is lower than the resistance of the other areas of the pair of source/drain regions 32. This suppresses a parasitic resistance from the pair of source/drain electrodes 2 to a channel as well as current rate degradation.

Next, a manufacturing method of thin film transistor 600 will be described with reference to Figs. 10A to 10E.

As shown in Fig. 10A, gate electrode 7 and gate insulator 4 are formed on substrate 1. As shown in Fig. 10B, oxide semiconductor thin film layer 3 and first overcoat insulator 11 are then sequentially formed on gate insulator 4.

After formation of first overcoat insulator 11, oxide semiconductor thin film layer 3 and first overcoat insulator 11 are etched. Fig. 10C shows a cross section of thin film transistor 600 after the etching. Oxide semiconductor thin film layer 3 and first overcoat insulator 11, as shown in Fig. 10C, are formed in a self-aligning manner. First overcoat insulator 11 is configured to protect oxide semiconductor thin film layer 3 during the etching. Specifically, first overcoat insulator 11 functions as a protective film that protects oxide semiconductor thin film layer 3 from various agents such as a resist stripper used in the etching of oxide semiconductor thin film layer 3. This avoids the surface roughening of semiconductor thin film layer 3.

As seen in Fig. 10D, after formation of first overcoat insulator 11, second overcoat insulator 12 is formed. Then contact holes 5 are opened through first and second overcoat insulators 11 and 12 to oxide semiconductor thin film layer 3 by way of photolithography.

Oxide semiconductor thin film layer 3 is subjected to an activation treatment by ion-doping through contact holes 5 (see Fig. 10D) to reduce the resistance of portions of oxide semiconductor thin film layer 3 under contact holes 5.

Since the portions of oxide semiconductor thin film layer 3 under contact holes 5 are in an uncovered state, it is easy to subject these portions to an ion-doping and an activation treatment.

In the final step to form thin film transistor 600, contact holes 5 are filled with metallic materials or the like (see Fig. 10E). The metallic materials in contact holes 5 form the pair of source/drain electrodes 2. As described above, the portion of oxide semiconductor thin film layer 3

positioned inside the connection area (area connected with the pair of source/drain electrodes) functions as channel region 31, while the outside portions of oxide semiconductor thin film layer 3 function as the pair of source/drain regions 32. Since the exposed portions with the reduced
5 resistance are located in the pair of source/drain regions 32 as the second regions, a parasitic resistance between the pair of source/drain electrodes 2 and the channel is suppressed.

It has been described that a treatment for reducing the resistance of oxide semiconductor thin film layer 3 of thin film transistor 600 is
10 performed through contact holes 5, which are formed in second overcoat insulator 12 by means of photolithography (see Fig. 10D). To use such a treatment, at least a part of contact holes 5 and gate electrode 7 should overlap each other in an overlap area. If such an overlap area is not formed, an offset structure, in which an area of a high resistance is formed
15 between the channel and source/drain regions 32, of the thin film transistor 600 results. This may increase parasitic capacitance of thin film transistor 600 and cause current rate degradation.

If the thin film transistor 600 has this structure in which the overlap area of the contact holes 5 with the gate electrode 7 is not present, one
20 solution to prevent the high resistance area between the channel and source/drain regions 32 and to reduce the parasitic capacitance of thin film transistor 600 is patterning a resist on first overcoat insulator 11 without using a photomask to reduce the resistance of oxide semiconductor thin film layer 3. Specifically, after the patterning of first overcoat insulator 11 and
25 oxide semiconductor thin film layer 3 (see Fig. 10C), a resist is formed on first overcoat insulator 11. The resist is exposed to light from a substrate

side and patterned. The resist is used as a mask in the ion-doping and activation treatment performed subsequently to reduce the resistance of the pair of source/drain regions 32, which are located outside the area that overlies gate electrode 7.

5 In this case, gate electrode 7 should be shorter in a channel length direction and longer in a channel width direction than oxide semiconductor thin film layer 3. A portion of semiconductor thin film layer 3 directly above gate electrode 7 functions as channel region 31 whereas the other portions of oxide semiconductor thin film layer 3 defining the channel region
10 31 therebetween function as the pair of source/drain regions 32.

This method enables the resistance of the entire area of the pair of source/drain regions 32, which are defined as regions in oxide semiconductor thin film layer 3 other than channel region 31, to be reduced.

15 EXAMPLES

Hereinafter, the effect of the film formation conditions of a zinc oxide thin film on the preferred orientation and the lattice spacing of the zinc oxide film will be explained.

A zinc oxide thin film was formed on a glass substrate by means of
20 radio-frequency magnetron sputtering, using nine film formation conditions resulting from combinations between three film-formation pressures and three Ar/O_2 gas flow ratios in a mixed gas of argon and oxygen as a source gas. The three film-formation pressures were 7Pa, 1Pa, and 0.5Pa. The three Ar/O_2 gas flow ratios were 10/5, 10/15, and 10/30ccm (cc/min).

25 The following conditions are used in this example. Sintered and pressed zinc oxide having a purity of 99.999% was used as a target. The

substrate temperature was kept at 150°C. The distance between the substrate and the target was fixed at 88mm. The diameter of the zinc oxide target was 4 inches φ. The applied electric power was 180W, i.e., the radio-frequency power density was $2.2W/cm^2$.

5 X-ray diffraction was used to estimate the preferred orientation and the lattice spacing of the zinc oxide films prepared under the above-mentioned nine film formation conditions. $CuK\alpha 1$ (wave length: 1.54056Å) was used in the X-ray diffraction measurement.

It was confirmed that all of the zinc oxide thin films had an X-ray

10 diffraction peak only in (002) direction. It was also confirmed that the (002) planes of all the zinc oxide thin films had a preferred orientation.

The X-ray enters samples and produces diffraction peaks in an angle that meets the following Bragg's condition,

$$2 \times d \times \sin\theta = n \times \lambda,$$

15 where d is a lattice spacing along the film thickness direction; λ is a wave length of the X-ray used in the measurement; n is a diffraction order; and θ is a diffraction angle (rad) of the X-ray.

For thin films in which (002) planes have a preferred orientation, d corresponds to lattice spacing d_{002} of (002) lattice planes. For $CuK\alpha 1$ ray

20 used in this measurement, λ=1.54056Å. In this example, n=1.

Therefore, this example meets the following equation.

$$d = (1 \times 1.54056)/(2 \times \sin\theta).$$

This means that lattice spacing d depends on the diffraction angle θ at which the X-ray produces diffraction peaks. The increase in lattice

25 spacing d results in a smaller diffraction angle θ.

Since all of the zinc oxide thin films formed under the nine film formation conditions have a preferred c-axis orientation, d obtained for the zinc oxide thin films of this example is lattice spacing d_{002}. Lattice spacing d_{002} is calculated from X-ray diffraction peak locations.

5 It has been reported that the lattice spacing constant $2d_{002}$ of single-crystal zinc oxide along (002) direction ranges from 5.204Å to 5.208Å. Considering that there are two of Zn planes or O planes in a unit lattice, the (002) lattice planes have a lattice spacing d_{002} of single-crystal zinc oxide that is in the range from 2.602Å to 2.604Å.

10 Fig. 11 shows a change in (002) diffraction peak locations of the zinc oxide thin films with respect to different film-formation pressures. Ar/O_2 flow ratio is fixed to 10/15ccm.

In Fig. 11, curves 111, 112, and 113 respectively indicate results when the film-formation pressure is 7Pa, 1Pa, and 0.5Pa. The vertical

15 scale plots X-ray diffraction intensity (arb. unit) whereas the horizontal scale plots diffraction peak location 2θ.

As shown in Fig. 11, the decrease in film-formation pressure from 7Pa to 0.5Pa results in a decreasing shift of X-ray peak location, which indicates increase in lattice spacing d_{002} of (002) lattice planes.

20 Fig. 12 shows the dependency of lattice spacing d_{002} on film-formation pressures according to the X-ray diffraction results obtained for different gas flow ratios.

In Fig. 12, curves 121, 122, and 123 respectively indicate the results when the gas flow ratio Ar/O_2 is 10/5, 10/15, and 10/30ccm. The vertical

25 scale plots lattice spacing d_{002} whereas the horizontal scale plots film-formation pressure during formation of the zinc oxide films.

The lattice spacing of single crystal zinc oxide is distributed within range A shown in Fig. 12.

As shown in Fig. 12, the lower the film-formation pressure is or the Ar/O_2 flow ratio is, the larger the lattice spacing d_{002} becomes.

5 It is noted that it is possible to control the lattice spacing (i.e., lattice constant) of the zinc oxide by changing film formation conditions.

The nine kinds of data plotted in Fig. 11 and Fig. 12 are shown in Table 1 below. The characters A-I respectively indicate the nine zinc oxide thin films.

Table 1

	Ar/O_2	Pressure	2θ	d_{002}
A	10/5	0.5	34.02	2.63280
B	10/5	1	34.20	2.61964
C	10/5	7	34.45	2.60138
D	10/15	0.5	33.93	2.63955
E	10/15	1	34.12	2.62583
F	10/15	7	34.42	2.60327
G	10/30	0.5	34.06	2.63009
H	10/30	1	33.97	2.63685
I	10/30	7	34.39	2.60560

10 Next, the relation between the heat resistance and the lattice spacing of zinc oxide thin films will be described.

Fig. 13 shows the dependency of the sheet resistance of zinc oxide thin films on heat-treatment temperature.

In Fig. 13, curves 131, 132, 133, and 134 respectively indicate the 15 sheet resistivity of zinc oxide thin films in which the (002) lattice planes have a lattice spacing d_{002} of 2.605Å (thin film I), 2.619Å (thin film B), 2.625Å (thin film E), and 2.636Å (thin film H). The sheet resistivity was measured after a heat treatment for 2 hours in a vacuum. The vertical scale plots sheet resistivity whereas the horizontal scale plots anneal

temperature. Since the sheet resistivity of the zinc oxide films exhibits an identical behavior below 200°C, curves 132, 133, and 134 overlap each other in this range.

For a zinc oxide thin film in which the (002) lattice planes have a lattice spacing d_{002} of 2.605Å (thin film I, curve 131 in Fig. 13), which is similar to the lattice spacing d_{002} of single crystal zinc oxide, a heat treatment at200°C results in a reduction in resistivity by at least 3 orders of magnitude from the high resistance ($10^{14}\Omega/\square$ sheet resistance) of the zinc oxide thin film, in the as-deposited state (immediately after the film formation). A heat treatment at 250°C applied to the zinc oxide thin film having a lattice spacing d_{002} of 2.605Å results in a reduction in resistivity by approximately 10 orders of magnitude from the high resistance ($10^{14}\Omega/\square$ sheet resistance) of the zinc oxide thin film in the as-deposited state.

For the zinc oxide thin film in which the (002) lattice planes have a lattice spacing d_{002} of 2.619Å (thin film B, curve 132 in Fig. 13), a heat treatment at 200°C does not significantly reduce the resistvity of the zinc oxide thin film from the resistance of the oxide semiconductor thin film in the as-deposited state. A heat treatment at 250°C applied to the same zinc oxide thin film results in a reduction in the resistivity by approximately 5 orders of magnitude, which is smaller than the reduction by approximately 9 orders of magnitude found when the heat treatment at 250°C is applied to the zinc oxide thin film having a lattice spacing d_{002} of 2.605Å.

For the zinc oxide thin film in which (002) lattice planes have a lattice spacing d_{002} of 2.625Å (thin film E, curve 133 in Fig. 13), a heat treatment at 250°C results in a reduction in resistivity by approximately 2 orders of magnitude. For the zinc oxide thin film having a lattice spacing

d_{002} of 2.636Å (thin film H, curve 134 in Fig. 13), the same heat treatment results in a still smaller reduction in the resistivity by approximately 1 order of magnitude. (As described above the sheet resistivity of the zinc oxide films E and H exhibits a behavior identical to the behavior of the sheet
5 resistivity of the zinc oxide film B below 200°C.)

Thus, an increase in the lattice spacing d_{002} reduces the temperature at which the decrease in resistivity starts and thereby improves heat resistance.

Considering the above results, an oxide semiconductor thin film
10 layer having a lattice spacing d_{002} of at least 2.619Å that exhibits a high heat resistance is preferably used as an oxide semiconductor thin film layer having a high heat resistance, in the present invention. More preferably, an oxide semiconductor thin film layer having a lattice spacing d_{002} of at least 2.625Å is used.

15 It is found from the above results that the thin film transistor 200 according to the second embodiment of the present invention exhibits an excellent TFT performance. For example, if a zinc oxide thin film having a lattice spacing d_{002} of 2.625Å is used as oxide semiconductor thin film layer 3 and if a heat treatment at 250°C is used in formation of first gate
20 insulator 4, a zinc oxide thin film having a lattice spacing d_{002} of 2.619Å or below is preferably used as contact layers 10 so as to control the resistance of the pair of contact layers 10 to be smaller than the resistance of oxide semiconductor thin film layer 3 by at least 2 orders of magnitude. This difference between the resistance of contact layers 10 and the resistance of
25 oxide semiconductor thin film layer 3 is sufficient to provide a better contact between the pair of source/drain electrodes 2 and oxide semiconductor thin

film layer 3. More preferably, a zinc oxide thin film having a lattice spacing d_{002} of 2.605Å or below is used as contact layers 10 so as to control the resistance of the pair of contact layers 10 to be smaller than the resistance of oxide semiconductor thin film layer 3 by at least 6 orders of magnitude.

Alternatively, if a zinc oxide thin film having a lattice spacing d_{002} of 2.619Å is used as oxide semiconductor thin film layer 3 and if a heat treatment at 250°C is used in formation of first gate insulator 4, a zinc oxide thin film having a lattice spacing d_{002} of 2.605Å or below is preferably used as the pair of contact layers 10 so as to control the resistance of the pair of contact layers 10 to be smaller, by at least 2 orders of magnitude, than the resistance of the oxide semiconductor thin film layer 3.

Next, the TFT performance of a thin film transistor is tested to clarify the effects of the present invention.

Thin film transistor 100 (see Fig. 1) is prepared according to the following method (see Fig. 2).

A substrate 1 of no alkali glass mainly comprising SiO_2 and Al_2O_3 is provided. A pair of source/drain electrodes 2 of indium tin oxide are formed on the substrate 1 to be 40nm in thickness.

A zinc oxide thin film is deposited by radio-frequency magnetron sputtering on all of the exposed surfaces of substrate 1 and the pair of source/drain electrodes 2 to form an oxide semiconductor thin film layer 3 of 60nm thickness.

After formation of oxide semiconductor thin film layer 3, first gate insulator 4 of SiN having a 50nm thickness is formed on the entire upper surface of oxide semiconductor thin film layer 3. Formation of first gate

insulator 4 is performed at 250°C by means of plasma enhanced chemical vapor deposition (PCVD) using $SiH_4+NH_3+N_2$ gas.

Then a photoresist is coated and patterned on first gate insulator 4. Using the patterned photoresist as a mask, first gate insulator 4 is
5 dry-etched using CF_4+O_2 gas.

After the etching of first gate insulator 4, oxide semiconductor thin film layer 3 is wet-etched using 0.2% HNO_3 solution to remove the photoresist. Then second gate insulator 6 of SiN_x having a 300nm thickness is formed on all of the exposed surfaces of substrate 1,
10 source/drain electrodes 2, oxide semiconductor thin film layer 3, and first gate insulator 4.

Formation of second gate insulator 6 is performed at 250°C by means of plasma enhanced chemical vapor deposition (PCVD) using $SiH_4+NH_3+N_2$ gas.

15 After formation of second gate insulator 6, contact holes are opened in an upper part of the pair of source/drain electrodes 2.

Lastly, gate electrode 7 of Cr having a 100nm thickness is formed on second gate insulator 6, and then external source/drain electrodes 2a are formed, using the same material. The external source/drain electrodes 2a
20 are respectively connected to source/drain electrodes 2 through contact holes 5 via contact parts 5a in the final step of forming thin film transistor 100 used in the TFT performance test.

Three sample thin film transistors were prepared by the manufacturing process described above using respective zinc oxide thin
25 films having different lattice spacings. A control thin film transistor, referred to below as thin film transistor 101, was formed using a zinc oxide

thin film (thin film I) having a lattice spacing d_{002} of 2.605Å as oxide semiconductor thin film layer 3. A thin film transistor referred to below as thin film transistor 102 was formed using a zinc oxide thin film (thin film E) having a lattice spacing d_{002} of 2.625Å as oxide semiconductor thin film
5 layer 3. And a thin film transistor referred to below as thin film transistor 103 was formed using a zinc oxide thin film (thin film G) having a lattice spacing d_{002} of 2.630Å as oxide semiconductor thin film layer 3.

Thin film transistor 100 and the control thin film transistor have a top gate structure. In the top gate structure, an upper part of oxide
10 semiconductor thin film layer 3 is used as a channel region. The oxide semiconductor thin film layer 3 in a top gate thin film transistor is more directly affected by the heat produced in forming the gate insulator on the oxide semiconductor thin film layer 3 than the oxide semiconductor thin film layer 3 in a bottom gate thin film transistor. Use of the top gate thin
15 film transistor enables results to be obtained that more precisely reflect the effects of the heat applied to the oxide semiconductor thin film layer.

The TFT performance of each of the thin film transistors 101, 102, and 103 formed by the above-described process were tested as described below. Fig. 14 shows a change in the drain current of thin film transistor
20 101, 102, and 103 according to various gate voltages applied to thin film transistor 101, 102, and 103. In Fig. 14, the vertical scale plots the magnitude of drain current Id whereas the horizontal scale plots the magnitude of the applied gate voltage Vg. A constant drain voltage Vd is used in this test.

25 As shown in Fig. 14, thin film transistor 101 including an oxide semiconductor thin film layer having a lattice spacing d_{002} of 2.605Å allows

a constant drain current to remain unaffected by the change in the gate voltage. This means that thin film transistor 101 operates in a so-called normally-on mode or a depletion mode. In other words, thin film transistor 101 does not function as a thin film transistor.

5 The oxide semiconductor thin film layer of thin film transistor 101 has a similar lattice spacing d_{002} to the lattice spacing d_{002} of single crystal zinc oxide and exhibits an insufficient heat resistance, as shown by curve 131 in Fig. 13. The heat history during formation of gate insulator 4 causes desorption of zinc and oxygen from the channel region located
10 around the surface of oxide semiconductor thin film layer 3. The desorption forms defects in the oxide semiconductor thin film layer, which reduces the resistance of the oxide semiconductor thin film layer. Thus thin film transistor 101 loses its functions as a TFT.

The drain current of TFT 103 having a lattice spacing d_{002} of 2.630Å
15 rises at a gate voltage of 2V. This means that TFT 103 has sufficient functions as a TFT.

The drain current of TFT 102 having a lattice spacing d_{002} of 2.625Å exhibits a higher rise characteristic than TFT 103. In addition, the drain current value of TFT 102 at a gate voltage 10V is improved by at least 1
20 order of magnitude, as compared to TFT 103.

As described above, an increase in the lattice spacing d_{002} results in an increase in the heat resistance. The increased heat resistance suppresses defects in the oxide semiconductor thin film layer to improve the TFT performance. The better TFT performance of TFT 102 than the TFT
25 performance of TFT 103 of a greater lattice spacing d_{002} could be due to the more advanced crystallization in thin film E (lattice spacing d_{002}=2.625Å) of

TFT 102 than the crystallization in thin film G (lattice spacing d_{002}=2.630Å) of TFT 103, referring to the comparison between the X-ray diffraction intensities of the curve 113 (thin film D: d_{002}=2.639Å) and the curve 112 (thin film E: d_{002}=2.625Å). Though not shown in the drawings, a test comparing the X-ray diffraction intensities of thin film E and thin film G was carried out and the test revealed a more advanced crystallization in thin film G.

In this example, the TFT performance of top gate thin film transistors has been tested. This is because the top gate thin film transistors are more sensitive to the heat history than bottom gate thin film transistors. However, the heat history during formation of a protective insulator on the oxide semiconductor thin film layer also causes defects in a bottom gate thin film transistor so as to particularly affect the back channel. The effects on the back channel change the TFT performance. Therefore, the high resistance oxide semiconductor thin film layer according to the present invention may also be useful in bottom gate thin film transistors.

The semiconductor element included in the present invention is not limited to a thin film transistor but may be other kinds of semiconductor element. The present invention may be useful not only in a thin film transistor but also in other semiconductor devices. The present invention is particularly useful in a structure where an oxide semiconductor thin film layer is affected by the heat history during formation of an insulator on the oxide semiconductor thin film layer.

Lastly, thin film transistors including an ion-doped oxide semiconductor thin film layer as described in the third to sixth

embodiments were tested. Fig. 15 is a graph showing the heat resistance of ion-doped zinc oxide thin films.

In Fig. 15, curves 151 and 152 respectively indicate the heat resistance of a zinc oxide thin film (thin film I) having a lattice spacing d_{002} of 2.605Å and of a zinc oxide thin film (thin film H) having a lattice spacing d_{002} of 2.636Å, both of which were doped with gallium (Ga) ions. The thin films were heat-treated for 2 hours in a vacuum. After the sample temperature fell below 200°C, the thin films were subjected to the atmosphere. Fig. 15 shows the sheet resistivity of the thin films measured after the subjection to the atmosphere. The vertical scale plots sheet resistivity whereas the horizontal scale plots anneal temperature.

In the doping of gallium, $1\times10^{15}/cm^2$ accelerated gallium ions with 80 keV energy were doped without heating.

The resistance of the zinc oxide thin film having a lattice spacing d_{002} of 2.605Å, which is similar to the lattice spacing d_{002} of zinc oxide single crystal, decreases right after the ion doping (see curve 151 in Fig. 15).

The resistance of the zinc oxide thin film having a lattice spacing d_{002} of 2.636Å does not significantly decrease after the ion-doping.

However, a heat treatment after the ion-doping reduces the resistance of the zinc oxide thin film having a lattice spacing d_{002} of 2.636Å (see curve 152 in Fig. 15). As described by curve 134 in Fig. 13, the non ion-doped zinc oxide thin film maintains a high resistance until around 250°C. The heat treatment causes a difference between the resistance of the ion-doped zinc oxide thin film and the resistance of the non ion-doped zinc oxide thin film. Specifically, a heat treatment at around 200 to 250°C allows the resistance of the ion-doped zinc oxide to be maintained at a high

level (as indicated by curve 134 in Fig. 13) while reducing the resistance of the non ion-doped zinc oxide to a sufficiently lower level than the resistance of the ion-doped zinc oxide (as indicated by curve 152 in Fig. 15).

If a thin film transistor is formed to include an oxide semiconductor thin film layer having a large lattice spacing d_{002}, it is not sufficient to dope ions in order to reduce the resistance of the oxide semiconductor thin film layer such that a pair of source/drain regions are appropriately formed. An activation treatment (e.g., heat treatement) is further used to reduce the resistance of only the ion-doped area such that a pair of source/drain regions are appropriately formed. In addition, the non ion-doped area (i.e., channel area) maintains a high resistance through the activation treatment such that a thin film transistor with a high current driving capability is provided.

At a lattice spacing d_{002} of 2.605Å, a heat treatment at 200°C or above results in a decrease in the resistance of both the ion-doped zinc oxide (see curve 151 in Fig. 15) and the non ion-doped zinc oxide (see curve 131 in Fig. 13). As a result, it is not possible to maintain a high resistance of the channel region so as to form a thin film transistor with a high current driving capability at a lattice spacing d_{002} of 2.605Å.

The rate of decrease in the resistance caused by the heat treatment after the ion-doping depends on the amount of doped ions, the type of doped ions, or the heat treatment.

As described above, the semiconductor device including a semiconductor thin film layer of zinc oxide according to the present invention exhibits an excellent performance and is suitably used as a driving element in, for example, a liquid crystal display device and the like.

CLAIMS

1. A semiconductor device comprising:

a substrate (1); and

a semiconductor element including an oxide semiconductor thin film layer (3) of zinc oxide, which is formed on the substrate, and at least a portion of which includes (002) lattice planes having a preferred orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å.

2. The semiconductor device according to claim 1, wherein the entire oxide semiconductor thin film layer (3) includes (002) lattice planes having a preferred orientation along a direction perpendicular to the substrate (1) and a lattice spacing d_{002} of at least 2.619Å.

3. The semiconductor device according to claim 1, wherein a portion of the oxide semiconductor thin film layer (3) which is in contact with the substrate (1) includes (002) lattice planes having a preferred orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å.

4. The semiconductor device according to claim 1, wherein the lattice spacing d_{002} of the (002) lattice planes of the oxide semiconductor thin film layer (3) is at least 2.625Å.

5. The semiconductor device according to claim 1, further comprising an insulating film (4, 6, 9, 11, 12) formed on the oxide semiconductor thin film layer (3).

5 6. The semiconductor device according to claim 1, wherein the semiconductor element comprises a thin film transistor.

7. A semiconductor device comprising:

a substrate (1);

10 an oxide semiconductor thin film layer (3) of zinc oxide, which is formed on the substrate, and at least a portion of which includes (002) lattice planes having a preferred orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å; and

contact layers (10) of zinc oxide, which are formed in contact with 15 the oxide semiconductor thin film layer, and at least a portion of each of which includes (002) lattice planes having a preferred orientation along the direction perpendicular to the substrate and a lattice spacing d_{002} that is smaller than the lattice spacing d_{002} of the (002) lattice planes of the oxide semiconductor thin film layer.

20

8. The semiconductor device according to claim 7, wherein the entire oxide semiconductor thin film layer (3) and the entire contact layers (10) include (002) lattice planes having a preferred orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 25 2.619Å.

9. The semiconductor device according to claim 7, wherein a portion of the oxide semiconductor thin film layer (3) which is in contact with the substrate (1) and a portion of the contact layers (10) which is in contact with the substrate include (002) lattice planes having a preferred
5 orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å.

10. The semiconductor device according to claim 7, wherein the lattice spacing d_{002} of the (002) lattice planes of the contact layers (10) is not
10 more than 2.605Å.

11. The semiconductor device according to claim 7, wherein the lattice spacing d_{002} of the (002) lattice planes of the oxide semiconductor thin film layer (3) is at least 2.625Å, and the lattice spacing d_{002} of the (002)
15 lattice planes of the contact layers (10) is not more than 2.619Å.

12. The semiconductor device according to claim 11, wherein the lattice spacing d_{002} of the (002) lattice planes of the contact layers (10) is not more than 2.605Å.

20

13. The semiconductor device according to claim 7, further comprising:

a pair of source/drain electrodes (2) electrically coupled to the oxide semiconductor thin film layer (3) via the contact layers (10);

25 a gate insulator (4, 6); and

a gate electrode (7) formed on the gate insulator;

wherein the oxide semiconductor thin film layer, the contact layers, the pair of the source/drain electrodes, the gate insulator, and the gate electrode constitute a thin film transistor.

5 14. A semiconductor device comprising:

a substrate (1); and

an oxide semiconductor thin film layer (3) of zinc oxide which is formed on the substrate, and at least a portion of which includes (002) lattice planes having a preferred orientation along a direction perpendicular
10 to the substrate and a lattice spacing d_{002} of at least 2.619Å;

wherein the oxide semiconductor thin film layer includes a first region (31) of intrinsic zinc oxide and second regions (32) of zinc oxide doped with ions acting as donors to zinc oxide, and

wherein the second regions have a lower resistance than a
15 resistance of the first regions.

15. The semiconductor device according to claim 14, wherein the entire oxide semiconductor thin film layer (3) includes (002) lattice planes having a preferred orientation along a direction perpendicular to the
20 substrate (1) and a lattice spacing d_{002} of at least 2.619Å.

16. The semiconductor device according to claim 14, wherein a portion of the oxide semiconductor thin film layer (3) which is in contact with the substrate (1) includes (002) lattice planes having a preferred
25 orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å.

17. The semiconductor device according to claim 14, wherein the lattice spacing d_{002} of the (002) lattice planes of the oxide semiconductor thin film layer (3) is at least 2.625Å.

5

18. The semiconductor device according to claim 14, further comprising:

a pair of source/drain electrodes (2) electrically coupled to the second regions (32) of the oxide semiconductor thin film layer (3) ;

10 a gate insulator (4, 6); and

a gate electrode (7) formed on the gate insulator to lie over the first region (31) of the oxide semiconductor thin film layer via the gate insulator;

wherein the oxide semiconductor thin film layer, the pair of the source/drain electrodes, the gate insulator and the gate electrode constitute

15 a thin film transistor.

19. The semiconductor device according to claim 14, wherein the ions acting as donors to zinc oxide are obtained by ionizing at least one group III element.

20

20. A manufacturing method of a semiconductor device comprising:

providing a substrate (1); and

depositing an oxide semiconductor thin film layer (3) of zinc oxide on

25 the substrate, such that at least a portion of the oxide semiconductor thin film layer in an as-deposited state includes (002) lattice planes having a

preferred orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å.

21. The manufacturing method of a semiconductor device according to claim 20, wherein the entire oxide semiconductor thin film layer (3) in the as-deposited state includes (002) lattice planes having a preferred orientation along a direction perpendicular to the substrate (1) and a lattice spacing d_{002} of at least 2.619Å.

22. The manufacturing method of a semiconductor device according to claim 20, wherein a portion of the oxide semiconductor thin film layer (3) in the as-deposited state which is in contact with the substrate (1) includes (002) lattice planes having a preferred orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å.

23. The manufacturing method of a semiconductor device according to claim 20, wherein the lattice spacing d_{002} of the (002) lattice planes of the oxide semiconductor thin film layer (3) in the as-deposited state is at least 2.625Å.

24. A manufacturing method of a semiconductor device comprising:

providing a substrate (1);

depositing an oxide semiconductor thin film layer (3) of zinc oxide, such that at least a portion of the oxide semiconductor thin film layer in an

as-deposited state includes (002) lattice planes having a preferred orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å; and

depositing contact layers (10) to be in contact with the oxide
5 semiconductor thin film layer, such that at least a portion of each of the contact layers in an as-deposited state includes (002) lattice planes having a preferred orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} that is smaller than the lattice spacing d_{002} of the (002) planes of the oxide semiconductor thin film layer.

10

25. The manufacturing method of a semiconductor device according to claim 24, wherein the entire oxide semiconductor thin film layer (3) and the entire contact layers (10), which are both in the as-deposited state, include (002) lattice planes having a preferred
15 orientation along a direction perpendicular to the substrate (1) and a lattice spacing d_{002} of at least 2.619Å.

26. The manufacturing method of a semiconductor device according to claim 24, wherein a portion of the oxide semiconductor thin
20 film layer (3) in the as-deposited state which is in contact with the substrate (1) and a portion of the contact layers (10) in the as-deposited state which is in contact with the substrate include (002) lattice planes having a preferred orientation along a direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å.

25

27. The manufacturing method of a semiconductor device according to claim 24, wherein the lattice spacing d_{002} of the (002) lattice planes of the contact layers (10) in the as-deposited state is not more than 2.605Å.

5

28. The manufacturing method of a semiconductor device according to claim 24, wherein the lattice spacing d_{002} of the (002) lattice planes of the oxide semiconductor thin film layer (3) in the as-deposited state is at least 2.625Å, and the lattice spacing d_{002} of the (002) lattice

10 planes of the contact layers (10) in the as-deposited state is not more than 2.619Å.

29. The manufacturing method of a semiconductor device according to claim 28, wherein the lattice spacing d_{002} of the (002) lattice

15 planes of the contact layers (10) in the as-deposited state is not more than 2.605Å.

30. A manufacturing method of a semiconductor device comprising:

20 providing a substrate (1);

depositing, on the substrate, an oxide semiconductor thin film layer (3) of zinc oxide, such that at least a portion of the oxide semiconductor thin film layer in an as-deposited state includes (002) lattice planes having a preferred orientation along a direction perpendicular to the substrate and a

25 lattice spacing of at least 2.619Å;

doping a plurality of regions of the oxide semiconductor thin film layer with ions that act as donors to zinc oxide to form second regions which are doped with the ions, such that a first region (31) of the oxide semiconductor thin film layer is defined as a region other than the second
5 regions (32); and

subjecting the second regions to an activation treatment.

31. The manufacturing method of a semiconductor device according to claim 30, wherein the entire oxide semiconductor thin film
10 layer (3) in the as-deposited state includes (002) lattice planes having a preferred orientation along the direction perpendicular to the substrate (1) and a lattice spacing d_{002} of at least 2.619Å.

32. The manufacturing method of a semiconductor device
15 according to claim 30, wherein a portion of the oxide semiconductor thin film layer (3) in the as-deposited state which is in contact with the substrate (1) includes (002) lattice planes having a preferred orientation along the direction perpendicular to the substrate and a lattice spacing d_{002} of at least 2.619Å.

20

33. The manufacturing method of a semiconductor device according to claim 30, wherein the activation treatment includes a heat treatment.

25 34. The manufacturing method of a semiconductor device according to claim 30, wherein the lattice spacing d_{002} of the (002) lattice

planes of the oxide semiconductor thin film layer (3) in the as-deposited state is at least 2.625Å.

35. The manufacturing method of a semiconductor device according to claim 30, further comprising:

forming source/drain electrodes (2) coupled to the oxide semiconductor thin film layer (3);

forming a gate insulator (4, 6); and

forming a gate electrode on the gate insulator (7);

wherein the oxide semiconductor thin film layer, the source/drain electrodes, the gate insulator and the gate electrode function as a thin film transistor in which the first region (31) of the oxide semiconductor thin film layer functions as a channel.

36. The manufacturing method of a semiconductor device according to claim 35, further comprising uncovering the second regions of the oxide semiconductor thin film layer by removing the gate insulator (4, 6) from the second regions (32) of the oxide semiconductor thin film layer (3) using the gate electrode (7) as a mask.

37. The manufacturing method of a semiconductor device according to claim 36, wherein the doping of the oxide semiconductor thin film layer (3) with the ions that act as donors to zinc oxide to form the second regions (32) is performed after the uncovering of the second regions of the oxide semiconductor thin film layer.

38. The manufacturing method of a semiconductor device according to claim 36, wherein the activation treatment is performed by forming an insulating film (4, 9, 11) on the uncovered second regions (32).

5 39. The manufacturing method of a semiconductor device according to claim 30, wherein the doping of at least a part of the second regions (32) of the oxide semiconductor thin film layer (3) is performed using ions obtained by ionizing at least one group III element.

FIG. 1

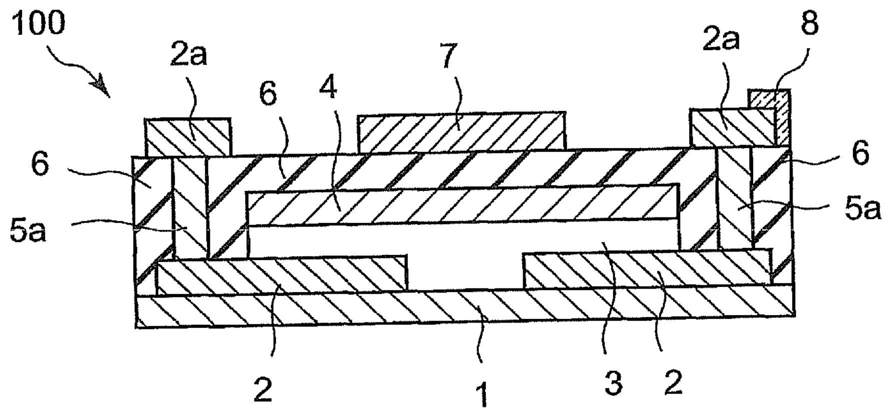


FIG. 2A

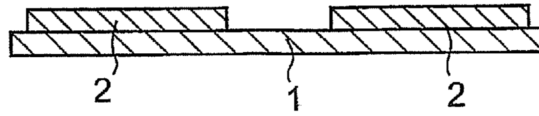


FIG. 2B

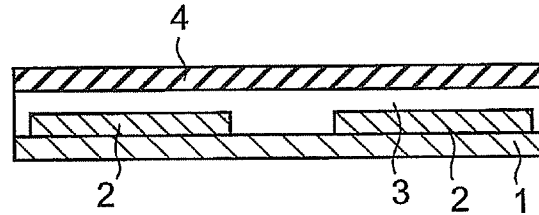


FIG. 2C

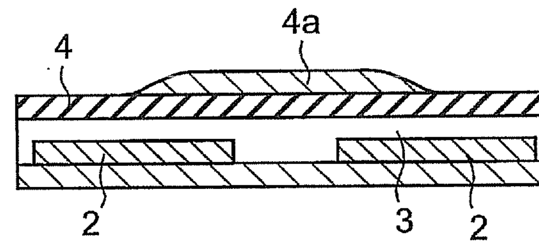


FIG. 2D

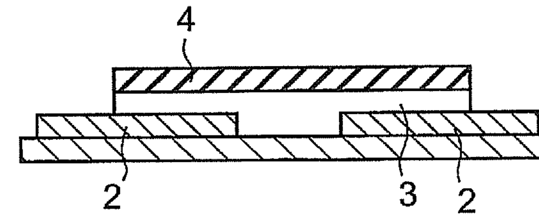


FIG. 2E

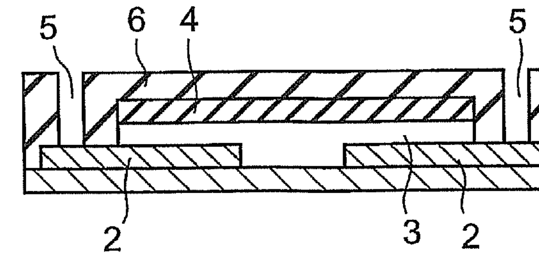


FIG. 2F

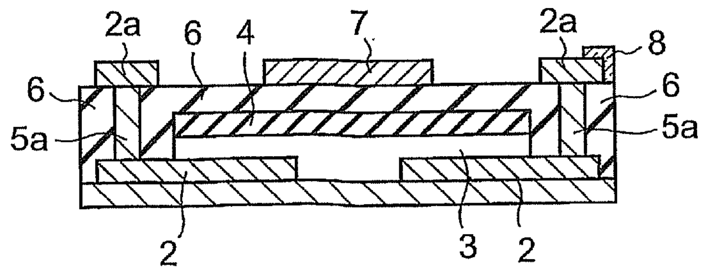


FIG. 3

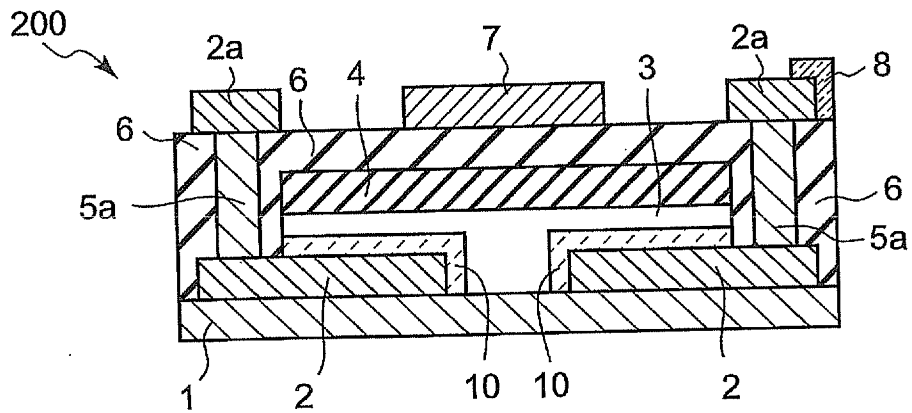


FIG. 4A

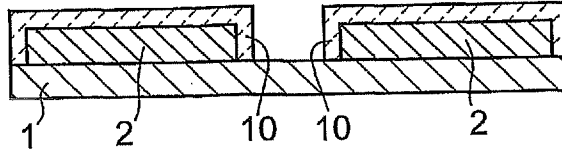


FIG. 4B

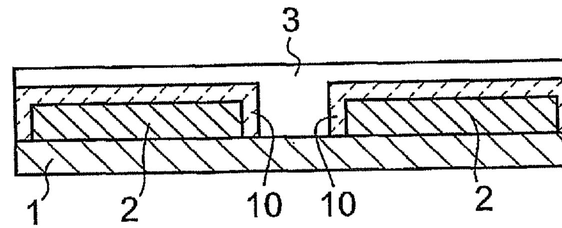


FIG. 4C

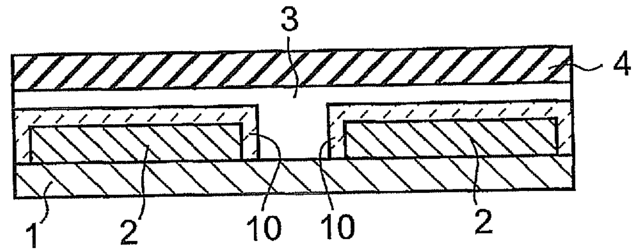


FIG. 4D

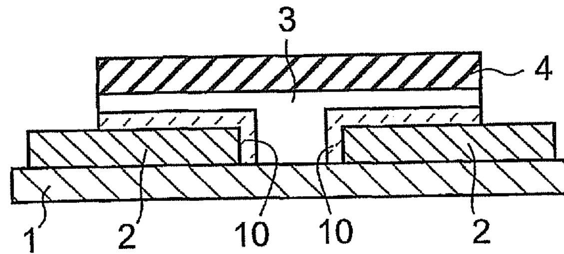


FIG. 4E

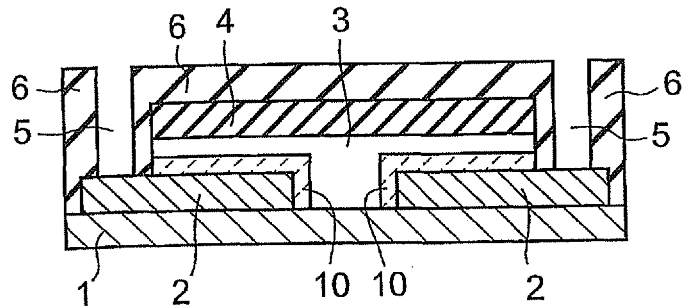


FIG. 5

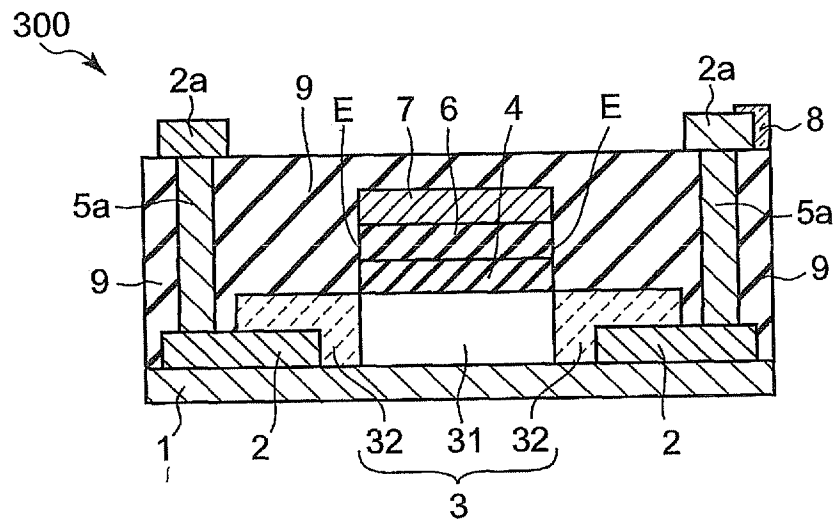


FIG. 6A

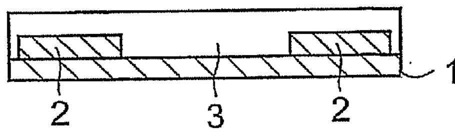


FIG. 6D

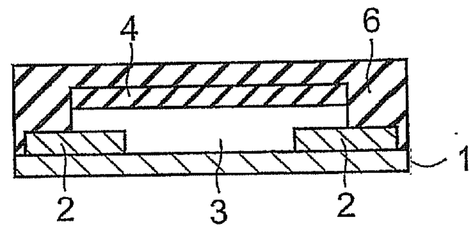


FIG. 6B

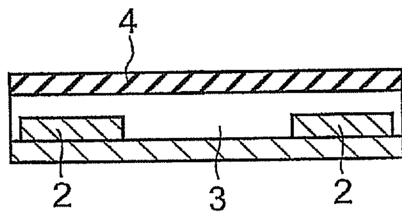


FIG. 6E

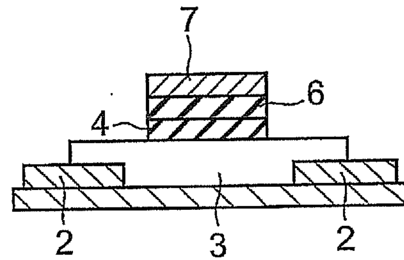


FIG. 6C

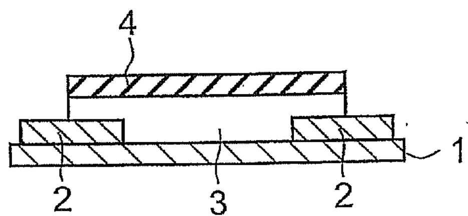


FIG. 6F

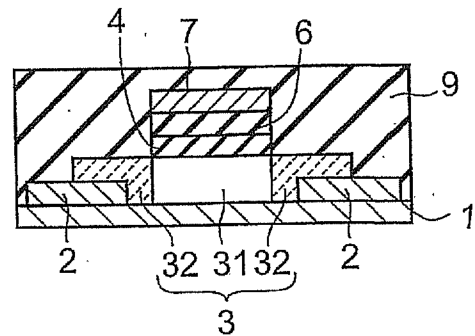


FIG. 7

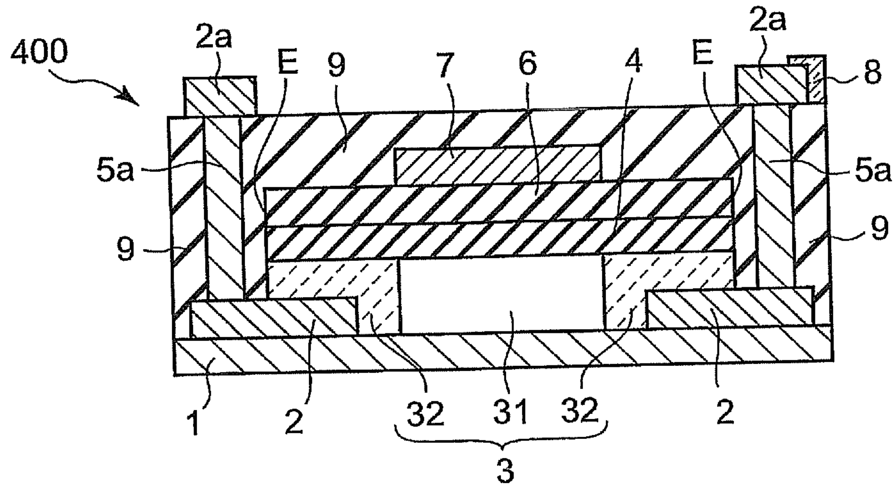


FIG. 8

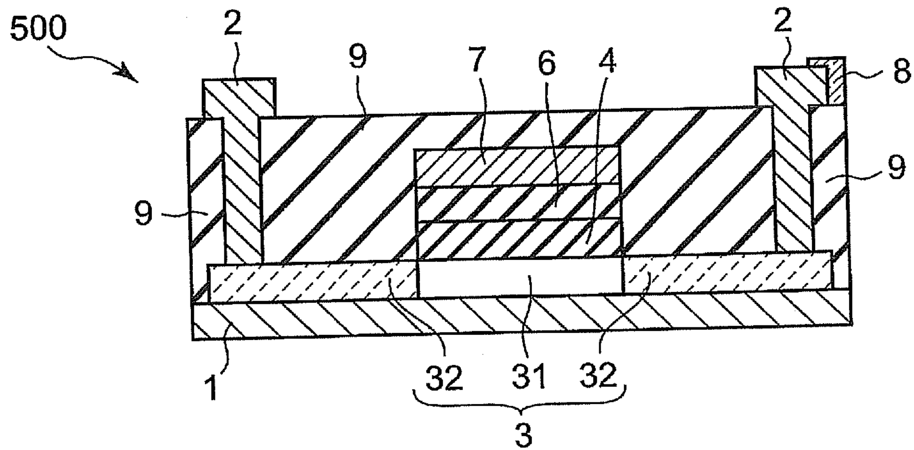


FIG. 9

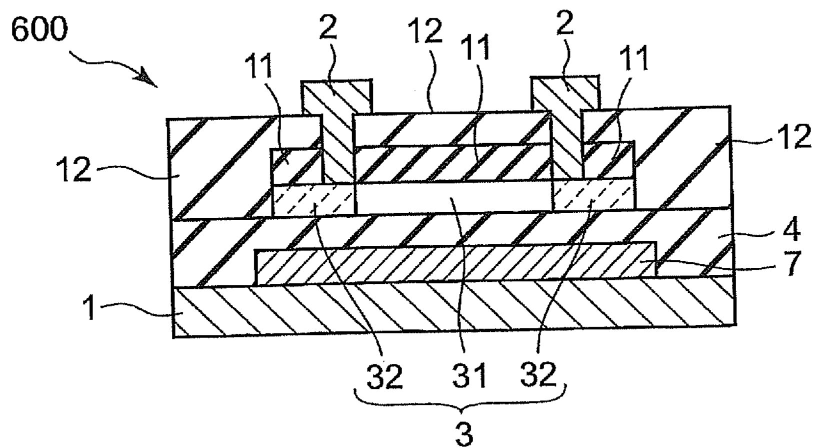


FIG. 10A

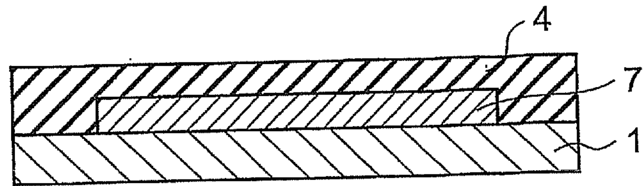


FIG. 10B

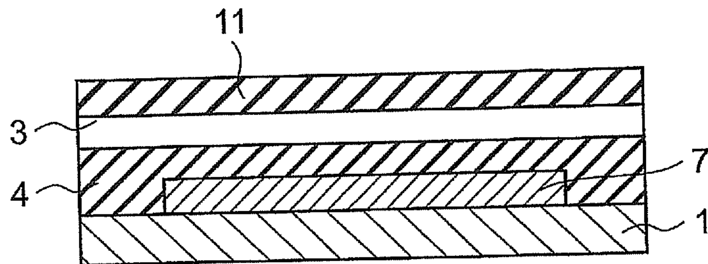


FIG. 10C

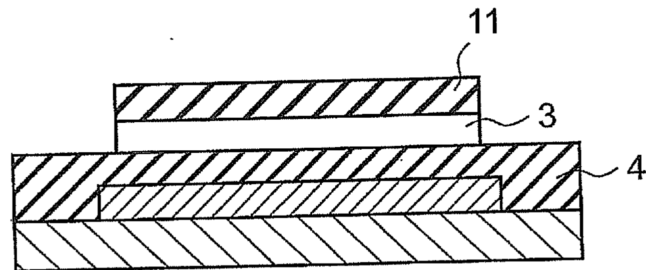


FIG. 10D

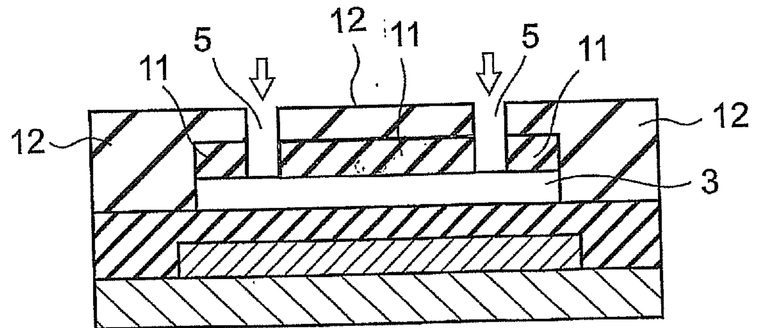


FIG. 10E

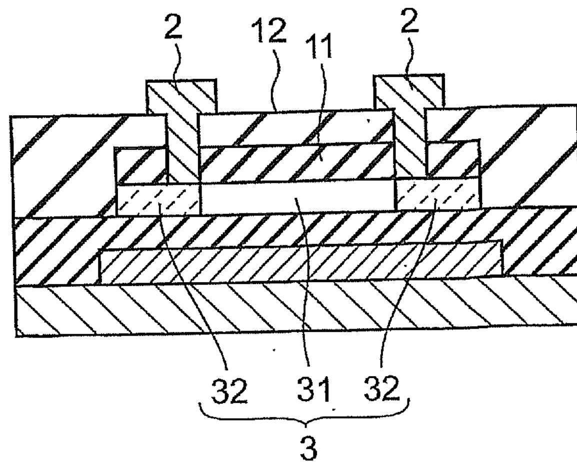


FIG. 11

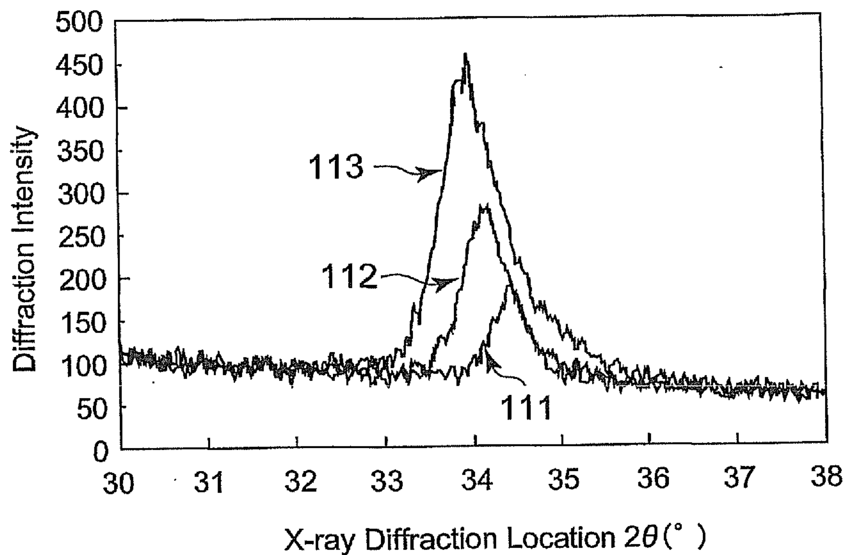


FIG. 12

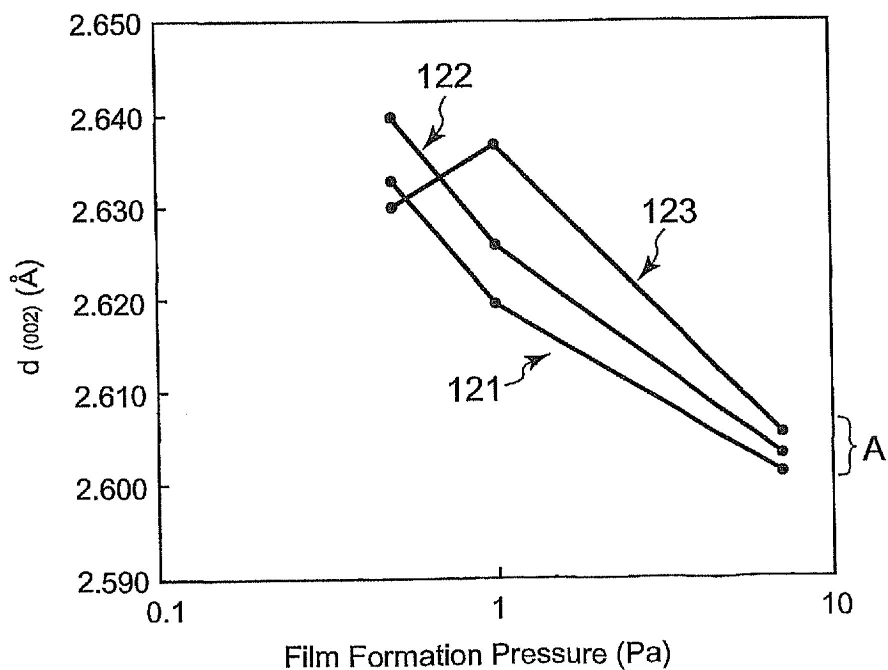


FIG. 13

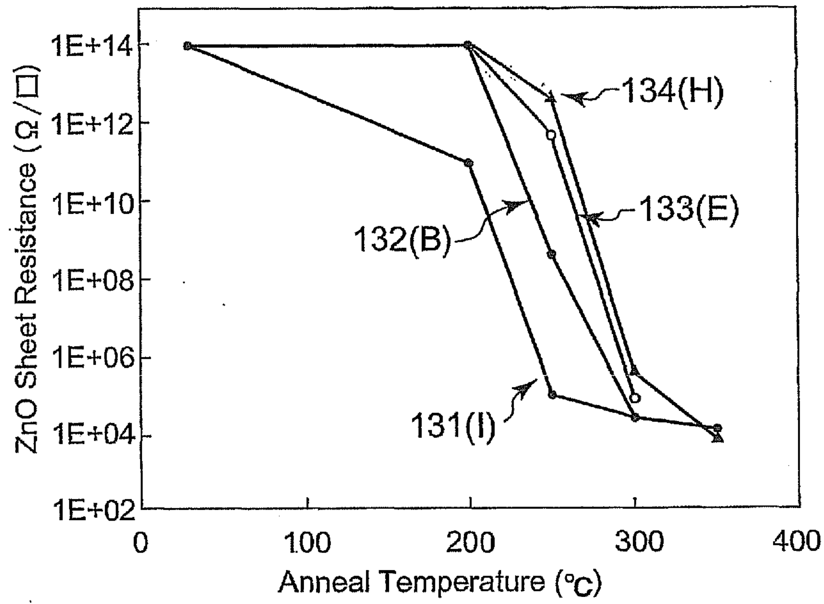


FIG. 14

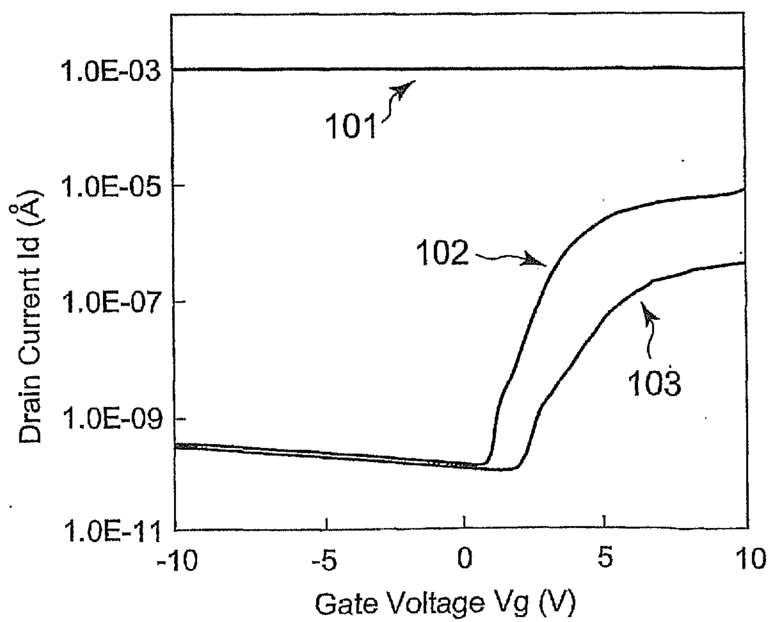


FIG. 15

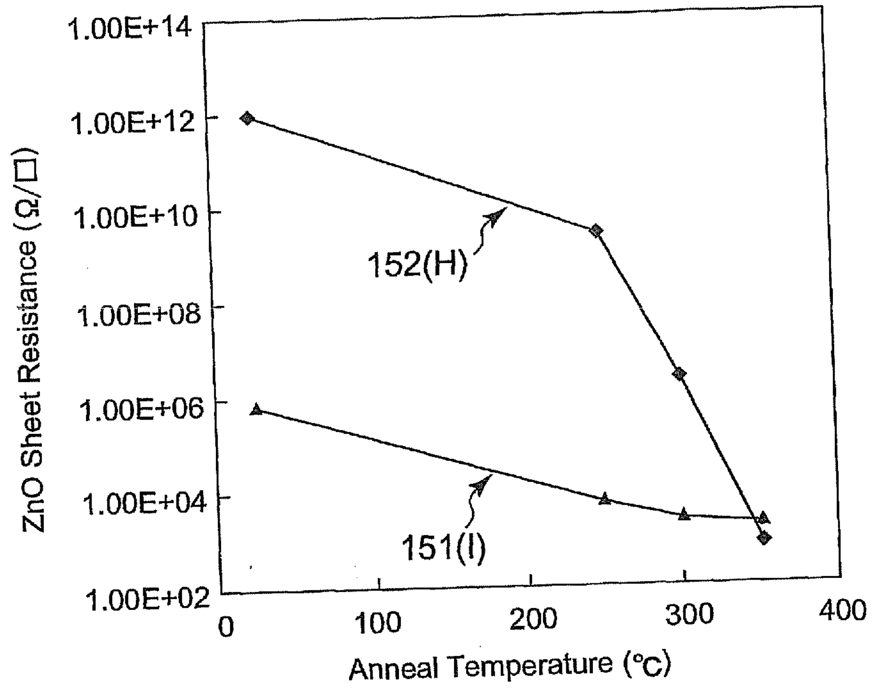
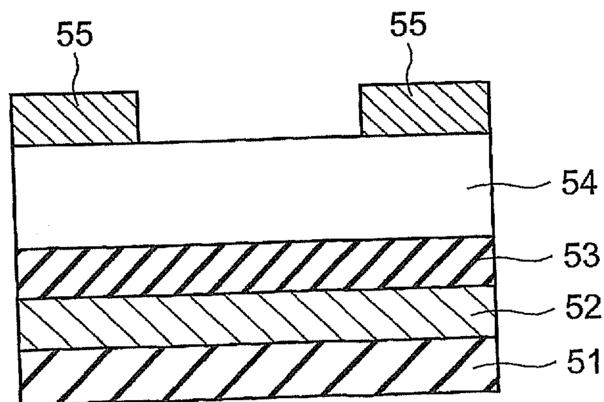


FIG. 16



INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2007/061242

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/786

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	SUN ET AL: "Changes of structure and optical energy gap induced by oxygen pressure during the deposition of ZnO films" PHYSICA B. CONDENSED MATTER, AMSTERDAM, NL, vol. 381, no. 1-2, 31 May 2006 (2006-05-31), pages 109-112, XP005428873 ISSN: 0921-4526 the whole document	1-6, 20-23

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 August 2007	29/08/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Hoffmann, Niels

INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2007/061242

Category*	C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT — Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	HUR TAE-BONG ET AL: "Strain effects in ZnO thin films and nanoparticles" JOURNAL OF APPLIED PHYSICS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 99, no. 6, 27 March 2006 (2006-03-27), pages 64308-64308, XP012084016 ISSN: 0021-8979 the whole document	1-3,5,6, 20-22
X	MAHALINGAM T ET AL: "Growth and characterization of electrosynthesised zinc oxide thin films" MATERIALS RESEARCH BULLETIN, ELSEVIER, KIDLINGTON, GB, vol. 38, no. 2, 25 January 2003 (2003-01-25), pages 269-277, XP004405329 ISSN: 0025-5408	1-5, 20-23
Y	the whole document	6-19, 24-39
Y	EP 1 209 748 A (MATSUSHITA ELECTRIC IND CO LTD [JP]) 29 May 2002 (2002-05-29) paragraph [0099] - paragraph [0130]	6-19, 24-39
A	JP 2005 150635 A (SANYO ELECTRIC CO) 9 June 2005 (2005-06-09) cited in the application abstract	1-39
A	JP 2006 005116 A (CASIO COMPUTER CO LTD; KOCHI PREFECTURE SANGYO SHINKO) 5 January 2006 (2006-01-05) abstract	7-19, 24-39
A	US 2004/127038 A1 (CARCIA PETER FRANCIS [US] ET AL) 1 July 2004 (2004-07-01) paragraph [0046]	7-21, 24-39

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/JP2007/061242

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
EP 1209748	A	29-05-2002	CN	1353329 A	12-06-2002
			KR	20020038482 A	23-05-2002
			SG	102643 A1	26-03-2004
			TW	588209 B	21-05-2004
			US	2002056838 A1	16-05-2002
JP 2005150635	A	09-06-2005	NONE		
JP 2006005116	A	05-01-2006	NONE		
US 2004127038	A1	01-07-2004	US	2006183274 A1	17-08-2006

PATENT COOPERATION TREATY
PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference PCT000013132 W17362	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/JP2010/073886	International filing date *(day/month/year)* 24.12.2010	(Earliest) Priority Date *(day/month/year)* 22.01.2010
Applicant SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☑ the international application in the language in which it was filed.
      ☐ a translation of the international application into ______ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (see Box No. II).
3. ☑ **Unity of invention is lacking** (see Box No. III).
4. With regard to the **title**,
   ☑ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   ☑ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 1
      ☐ as suggested by the applicant.
      ☑ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/073886

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
   because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
   because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Claim 1 lacks novelty over D1, and involves no special technical features. Thus, as for the international application, the unity of invention is lacking.

D1: WO 2007/089048 A2 (KOCHI INDUSTORIAL PROMOTION CENTER) 2007.08.09, page 9 line 6 - page 12 line 19, page 15 line 21 - page 19 line 9, Fig.1, Fig.2 & JP 2008-535205 A & US 2007/0187760 A1 & KR 10-2007-0122517 A & CN 101326644 A

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☑ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/073886

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L29/786(2006.01)i, H01L21/28(2006.01)i, H01L29/417(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, H01L21/28, H01L29/417

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	WO 2007/089048 A2 (KOCHI INDUSTORIAL PROMOTION CENTER) 2007.08.09, page 9 line 6 - page 12 line 19, page 15 line 21 - page 19 line 9, Fig.1, Fig.2 & JP 2008-535205 A & US 2007/0187760 A1 & KR 10-2007-0122517 A & CN 101326644 A	1,2,5,7,9,10,12,22 3,4,6,8,11,13-21,23
X A	WO 2007/058329 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2007.05.24, [0047]-[0054], [0082]-[0099], FIG.1B, FIG.5, FIG.6 & JP 2007-165861 A & US 2007/0108446 A1 & KR 10-2008-0070811 A & CN 101283444 A	7,8,10,12,22 1-6,9,11,13-21,23

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02.02.2011	15.02.2011

Name and mailing address of the ISA/JP
Japan Patent Office
3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

Authorized officer
MITSUO KAWAMOTO 4M 9056
Telephone No. +81-3-3581-1101 Ext. 3462

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/073886

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2007/142167 A1 (KOCHI INDUSTORIAL PROMOTION CENTER) 2007.12.13, page 17 line 7 - page 24 line 22, FIG.3, FIG.4 & JP 2009-528670 A & US 2007/0278490 A1 & EP 2025004 A1 & KR 10-2008-0066678 A & CN 101356652 A	1-23

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.

398,Hase,Atsugi-shi,Kanagawa
2430036 Japan

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY
(PCT Rule 43*bis*.1)

Date of mailing (*day/month/year*)	15.02.2011
Applicant's or agent's file reference PCT000013132	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date (*day/month/year*)	Priority date (*day/month/year*)
PCT/JP2010/073886	24.12.2010	22.01.2010

International Patent Classification (IPC) or both national classification and IPC
Int.Cl. H01L29/786(2006.01)i, H01L21/28(2006.01)i, H01L29/417(2006.01)i

Applicant
SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [x] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Date of completion of this opinion	02.02.2011
Name and mailing address of the ISA/JP **Japan Patent Office** 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Authorized officer 4M 9056 MITSUO KAWAMOTO Telephone No. +81-3-3581-1101 Ext. 3462

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2010/073886

Box No. I **Basis of this opinion**

1. With regard to the **language**, this opinion has been established on the basis of:
   - [x] the international application in the language in which it was filed.
   - [ ] a translation of the international application into ______________ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. [ ] This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(b)).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)
   - [ ] on paper
   - [ ] in electronic form

   b. (time)
   - [ ] in the international application as filed
   - [ ] together with the international application in electronic form
   - [ ] subsequently to this Authority for the purposes of search

4. [ ] In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY	International application No. PCT/JP2010/073886

Box No. IV Lack of unity of invention

1. ☐ In response to the invitation (Form PCT/ISA/206) to pay additional fees the applicant has, within the applicable time limit:
   - ☐ paid additional fees.
   - ☐ paid additional fees under protest and, where applicable, the protest fee.
   - ☐ paid additional fees under protest but the applicable protest fee was not paid.
   - ☐ not paid additional fees.

2. ☑ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is
   - ☐ complied with.
   - ☑ not complied with for the following reasons:

Claim 1 lacks novelty over D1, and involves no special technical features.
Thus, as for the international application, the unity of invention is lacking.

D1:WO 2007/089048 A2 (KOCHI INDUSTORIAL PROMOTION CENTER) 2007.08.09, page 9 line 6 - page 12 line 19, page 15 line 21 - page 19 line 9, Fig.1, Fig.2 & JP 2008-535205 A & US 2007/0187760 A1 & KR 10-2007-0122517 A & CN 101326644 A

4. Consequently, this opinion has been established in respect of the following parts of the international application:
   - ☑ all parts.
   - ☐ the parts relating to claims Nos. ______

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No. PCT/JP2010/073886

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	2-4,6,10,11,13-21,23	YES
	Claims	1,5,7-9,12,22	NO
Inventive step (IS)	Claims	3,4,6,11,13-21,23	YES
	Claims	1,2,5,7-10,12,22	NO
Industrial applicability (IA)	Claims	1-23	YES
	Claims		NO

2. Citations and explanations:

D1: WO 2007/089048 A2 (KOCHI INDUSTORIAL PROMOTION CENTER) 2007.08.09, page 9 line 6 - page 12 line 19, page 15 line 21 - page 19 line 9, Fig.1, Fig.2 & JP 2008-535205 A & US 2007/0187760 A1 & KR 10-2007-0122517 A & CN 101326644 A
D2:WO 2007/058329 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2007.05.24, [0047]-[0054], [0082]-[0099], FIG.1B, FIG.5, FIG.6 & JP 2007-165861 A & US 2007/0108446 A1 & KR 10-2008-0070811 A & CN 101283444 A
D3: WO 2007/142167 A1 (KOCHI INDUSTORIAL PROMOTION CENTER) 2007.12.13, page 17 line 7 - page 24 line 22, FIG.3, FIG.4 & JP 2009-528670 A & US 2007/0278490 A1 & EP 2025004 A1 & KR 10-2008-0066678 A & CN 101356652 A

Claims 1,5,7,9,12,22
The subject matter of claims 1,5,7,9,12,22 does not meet the requirement of novelty and does not appear to involve an inventive step in view of the D1 cited in the ISR.

Claims 7,8,12,22
The subject matter of claims 7,8,12,22 does not meet the requirement of novelty and does not appear to involve an inventive step in view of the D2 cited in the ISR.

Claims 2,10
The subject matter of claim 2,10 does not appear to involve an inventive step in view of the D1,D2 cited in the ISR.
The technical feature [The conductive layer has a tapered shape] is widely known among the skilled person in the art.

Claims 3,4,6,11,13-21,23
The subject matter of claims 3,4,6,11,13-21,23 is novel and is considered to involve an inventive step, since it is not disclosed in any of the prior art documents cited in the international search report.

Electronic Acknowledgement Receipt

EFS ID:	9879938
Application Number:	13008285
International Application Number:	
Confirmation Number:	8496
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Doris Vasquez Soriano
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-9138
Receipt Date:	14-APR-2011
Filing Date:	18-JAN-2011
Time Stamp:	14:13:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_04_14_2011.pdf	669267 93c3d9e5caaeb3a5ca5025982a8cc188f867f141	yes	4

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	2	
	Information Disclosure Statement (IDS) Filed (SB/08)		3	4	
Warnings:					
Information:					
2	Foreign Reference	WO2007058329.pdf	9130477 cc17573bf3eb345e5b7263b6425a458ec57699da	no	67
Warnings:					
Information:					
3	Foreign Reference	WO2007089048.pdf	6976642 4e46feec41d787afb7bfd2ed1f3c6418f1a7a486	no	51
Warnings:					
Information:					
4	Foreign Reference	WO2007142167.pdf	10701990 77238b1eae6ff864656e958841937d1a32ac6476	no	81
Warnings:					
Information:					
5	NPL Documents	INTERNATIONALSEARCHREPORT.pdf	587620 6f057db37b0772958d3035f05367e607ef910e88	no	4
Warnings:					
Information:					
6	NPL Documents	WRITTENOPINION.pdf	561322 4d32740461cdf4fb09f731b7a047c2912051045e	no	4
Warnings:					
Information:					
		Total Files Size (in bytes):	28627318		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Attorney Docket No. 0756-9138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 8496
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2811
Serial No. 13/008,285	)	
Filed: January 18, 2011	)	
For: SEMICONDUCTOR DEVICE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

Unless otherwise noted, the references submitted were cited in PCT Application No. PCT/JP2010/073886 in an International Search Report mailed February 15, 2011.

U.S. Patent No. 7,576,394 and U.S. Publication Nos. 2009/0269881 and 2007/0187760 are in the family of WO2007/089048. U.S. Patent No. 7,576,394 and U.S. Publication No. 2009/0269881 were not directly cited by the foreign patent office, but are submitted herewith for consideration by the Examiner.

U.S. Publication Nos. 2009/0186437; 2009/0186445; 2009/0189155; 2009/0189156; 2010/0003783; 2010/0038639 and 2007/0108446 are in the family of WO2007/058329. U.S. Publication Nos. 2009/0186437; 2009/0186445; 2009/0189155; 2009/0189156; 2010/0003783; 2010/0038639 were not directly cited by the foreign patent office, but are submitted herewith for consideration by the Examiner.

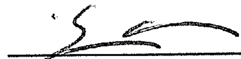
U.S. Patent No. 7,598,520 and U.S. Publication Nos. 2009/0286351 and 2007/0278490 are in the family of WO2007/142167. U.S. Patent No. 7,598,520 and

U.S. Publication No. 2009/0286351 were not directly cited by the foreign patent office, but are submitted herewith for consideration by the Examiner.

This Information Disclosure Statement is being submitted before the issuance of a first Office Action on the merits, therefore, no fee is required.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/008,285

APPLICATION AS FILED - PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	23 minus 20 =	* 3			OR	x 52 =	156
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	* 1				x 220 =	220
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
			TOTAL			TOTAL	1466

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

AMENDMENT A

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/008,285	01/18/2011	2811	1466	0756-9138	23	4

CONFIRMATION NO. 8496

FILING RECEIPT

OC000000045767672

31780
Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, VA 22033

Date Mailed: 02/09/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Shunpei YAMAZAKI, Setagaya, JAPAN;
Hiromichi GODO, Isehara, JAPAN;
Hideomi SUZAWA, Atsugi, JAPAN;
Shinya SASAGAWA, Chigasaki, JAPAN;
Motomu KURATA, Isehara, JAPAN;
Mayumi MIKAMI, Atsugi, JAPAN;

Assignment For Published Patent Application

SEMICONDUCTOR ENERGY LABORATORY CO., LTD., Kanagawa-ken, JAPAN

Power of Attorney:
Eric Robinson--38285

Domestic Priority data as claimed by applicant

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
JAPAN 2010-012540 01/22/2010

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 01/31/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/008,285**

Projected Publication Date: 07/28/2011

Non-Publication Request: No

Early Publication Request: No
Title

SEMICONDUCTOR DEVICE

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Please type a plus sign (+) inside this box → [+]

PTO/SB/08A (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	13/008,285
				Filing Date	01/18/2011
				First Named Inventor	Shunpei YAMAZAKI et al.
				Group Art Unit	2811
				Examiner Name	Unknown
Sheet	1	of	1	Attorney Docket Number	0756-9138

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] *(if known)*	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		5,744,864		Cillessen et al.	04/28/1998	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] *(if known)*	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.)., date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt

EFS ID:	9396804
Application Number:	13008285
International Application Number:	
Confirmation Number:	8496
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Shunpei YAMAZAKI
Customer Number:	31780
Filer:	Eric J. Robinson/Doris Vasquez Soriano
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-9138
Receipt Date:	08-FEB-2011
Filing Date:	18-JAN-2011
Time Stamp:	14:13:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS_02_08_2011.pdf	257227 8ea6ef760829692573bd2f6a6b96ffbeed60f50c	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Information Disclosure Statement (IDS) Filed (SB/08)	2	2
Warnings:			
Information:			
	Total Files Size (in bytes):	257227	

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Attorney Docket No. 0756-9138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No. 8496
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2811
Serial No. 13/008,285	)	
Filed: January 18, 2011	)	
For: SEMICONDUCTOR DEVICE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

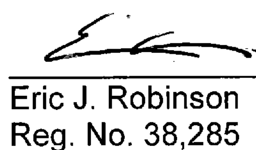
In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

U.S. Patent No. 5,744,864 is in the family of JP 11-505377. JP 11-505377 was previously cited in an Information Disclosure Statement filed January 18, 2011.

This Information Disclosure Statement is being submitted before the issuance of a first Office Action on the merits, therefore, no fee is required.

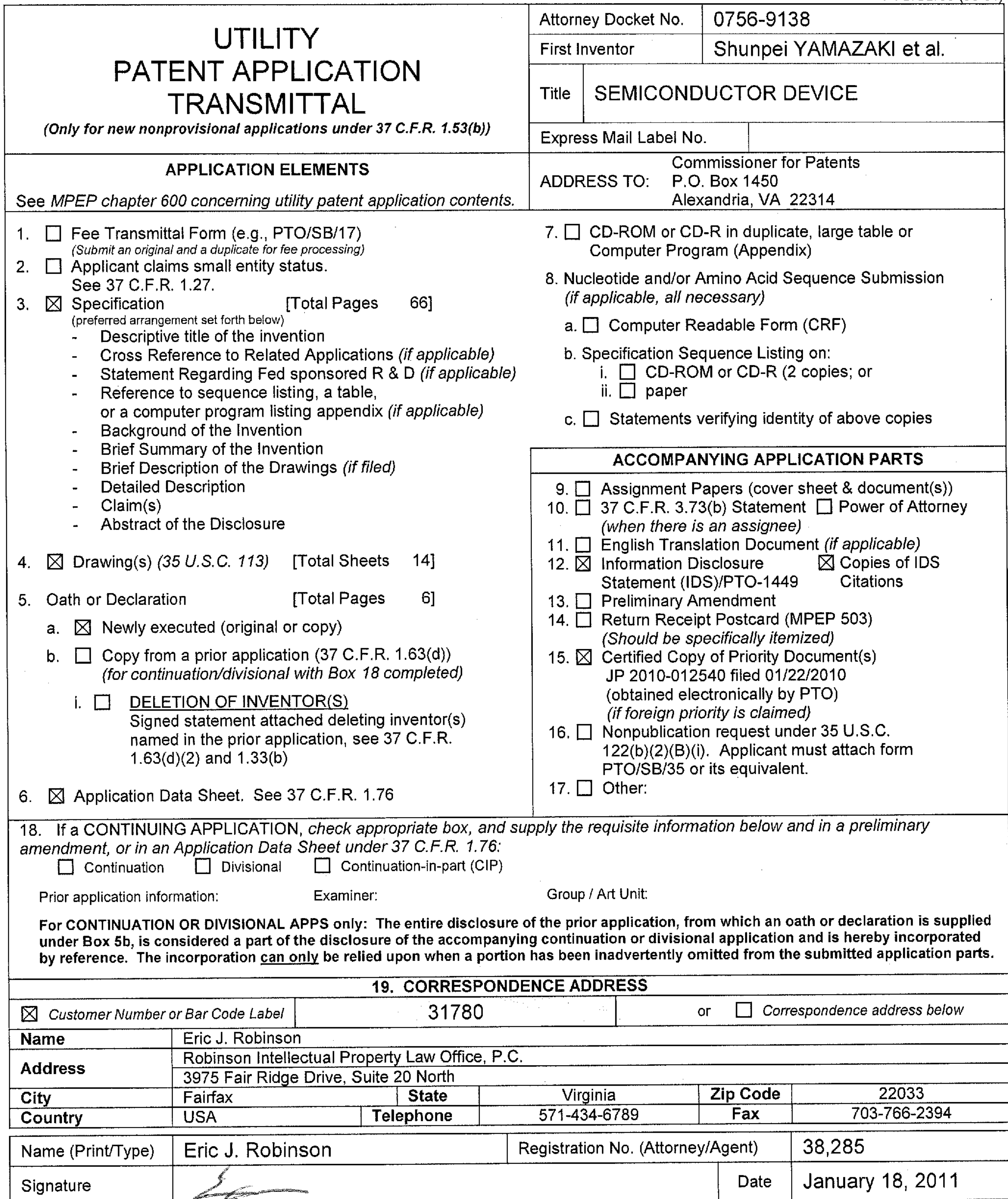
The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789



PTO/SB/05 (03-01)

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Attorney Docket No.	0756-9138
First Inventor	Shunpei YAMAZAKI et al.
Title	SEMICONDUCTOR DEVICE
Express Mail Label No.	

APPLICATION ELEMENTS

See *MPEP chapter 600 concerning utility patent application contents.*

ADDRESS TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22314

1. ☐ Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status.
   See 37 C.F.R. 1.27.
3. ☒ Specification [Total Pages 66]
   (preferred arrangement set forth below)
   - Descriptive title of the invention
   - Cross Reference to Related Applications *(if applicable)*
   - Statement Regarding Fed sponsored R & D *(if applicable)*
   - Reference to sequence listing, a table, or a computer program listing appendix *(if applicable)*
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) *(35 U.S.C. 113)* [Total Sheets 14]
5. Oath or Declaration [Total Pages 6]
   a. ☒ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 C.F.R. 1.63(d))
   (for continuation/divisional with Box 18 completed)
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b)
6. ☒ Application Data Sheet. See 37 C.F.R. 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
   i. ☐ CD-ROM or CD-R (2 copies; or
   ii. ☐ paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 C.F.R. 3.73(b) Statement ☐ Power of Attorney
    (when there is an assignee)
11. ☐ English Translation Document *(if applicable)*
12. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☐ Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
15. ☒ Certified Copy of Priority Document(s)
    JP 2010-012540 filed 01/22/2010
    (obtained electronically by PTO)
    (if foreign priority is claimed)
16. ☐ Nonpublication request under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. ☐ Other:

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 C.F.R. 1.76:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP)

Prior application information: Examiner: Group / Art Unit:

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

☒ *Customer Number or Bar Code Label* 31780 or ☐ *Correspondence address below*

Name	Eric J. Robinson				
Address	Robinson Intellectual Property Law Office, P.C. 3975 Fair Ridge Drive, Suite 20 North				
City	Fairfax	**State**	Virginia	**Zip Code**	22033
Country	USA	**Telephone**	571-434-6789	**Fax**	703-766-2394

Name (Print/Type)	Eric J. Robinson	Registration No. (Attorney/Agent)	38,285
Signature	[signature]	Date	January 18, 2011

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-9138
	Application Number	

Title of Invention	SEMICONDUCTOR DEVICE

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉Inventor ○Legal Representative under 35 U.S.C. 117 ○Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shunpei		YAMAZAKI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Setagaya	Country Of Residence i	JP
Citizenship under 37 CFR 1.41(b) i	JP		

Mailing Address of Applicant:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	State/Province	
Postal Code	243-0036	Country i	JP

Applicant 2 Remove

Applicant Authority ◉Inventor ○Legal Representative under 35 U.S.C. 117 ○Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hiromichi		GODO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Isehara	Country Of Residence i	JP
Citizenship under 37 CFR 1.41(b) i	JP		

Mailing Address of Applicant:

Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	State/Province	
Postal Code	243-0036	Country i	JP

Applicant 3 Remove

Applicant Authority ◉Inventor ○Legal Representative under 35 U.S.C. 117 ○Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hideomi		SUZAWA	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Atsugi	Country Of Residence i	JP

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-9138
	Application Number	

Title of Invention	SEMICONDUCTOR DEVICE

Citizenship under 37 CFR 1.41(b) i	JP		
Mailing Address of Applicant:			
Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country** i	JP

Applicant 4 [Remove]

Applicant Authority ◉Inventor ○Legal Representative under 35 U.S.C. 117 ○Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shinya		SASAGAWA	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Chigasaki	**Country Of Residence** i	JP
Citizenship under 37 CFR 1.41(b) i	JP		
Mailing Address of Applicant:			
Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country** i	JP

Applicant 5 [Remove]

Applicant Authority ◉Inventor ○Legal Representative under 35 U.S.C. 117 ○Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Motomu		KURATA	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Isehara	**Country Of Residence** i	JP
Citizenship under 37 CFR 1.41(b) i	JP		
Mailing Address of Applicant:			
Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country** i	JP

Applicant 6 [Remove]

Applicant Authority ◉Inventor ○Legal Representative under 35 U.S.C. 117 ○Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Mayumi		MIKAMI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Atsugi	**Country Of Residence** i	JP
Citizenship under 37 CFR 1.41(b) i	JP		

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-9138
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE	

Mailing Address of Applicant:			
Address 1	c/o Semiconductor Energy Laboratory Co., Ltd.		
Address 2	398, Hase		
City	Atsugi-shi, Kanagawa-ken	**State/Province**	
Postal Code	243-0036	**Country**i	JP
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.		Add	

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).		
☐ **An Address is being provided for the correspondence Information of this application.**		
Customer Number	31780	
Email Address	erobinson@riplo.com	Add Email / Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE		
Attorney Docket Number	0756-9138	**Small Entity Status Claimed** ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	14	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	31780		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-9138
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country i	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
2010-012540	JP	2010-01-22	◉ Yes ○ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☒

Organization Name	Semiconductor Energy Laboratory Co., Ltd.		
Mailing Address Information:			
Address 1	398, Hase		
Address 2			
City	Atsugi, Kanagawa-ken	**State/Province**	
Country i	JP	Postal Code	243-0036
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the **Add** button. Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Eric J. Robinson/	Date (YYYY-MM-DD)	2011-01-18

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0756-9138
	Application Number	

Title of Invention	SEMICONDUCTOR DEVICE

First Name	Eric J.	Last Name	Robinson	Registration Number	38285

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Attorney Docket No. 0756-9138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	
Shunpei YAMAZAKI et al.	)	New Application
Based on JP 2010-012540	)	
Filed: January 22, 2010	)	
For: SEMICONDUCTOR DEVICE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56 and 37 C.F.R. §§ 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. § 1.98(a).

U.S. Patent Nos. 6,727,522 is in the family of JP 2000-150900.

U.S. Patent No. 7,061,014 is in the family of JP 2004-103957.

Although no fee is due for this Information Disclosure Statement, the Commissioner is hereby authorized to charge fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033
(571) 434-6789

Please type a plus sign (+) inside this box → [+]

PTO/SB/08A (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449A/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				**Application Number**	
				Filing Date	January 18, 2011
				First Named Inventor	Shunpei YAMAZAKI et al.
				Group Art Unit	
				Examiner Name	
Sheet	1	of	2	**Attorney Docket Number**	0756-9138

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] *(if known)*	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6,727,522		Kawasaki et al.	04/27/2004	
		7,061,014		Hosono et al.	06/13/2006	
		5,648,662		Zhang et al.	07/15/1997	
		2009/0134383		Imahayashi et al.	05/28/2009	
		2008/0048183		Ohsawa et al.	02/28/2008	
		2010/0297809		Imahayashi et al.	11/25/2010	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Office[3]	Number[4]	Kind Code[5] *(if known)*	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP	60-198861			10/08/1985		Full
		JP	08-264794			10/11/1996		Full
		JP	11-505377			05/18/1999		Abst.
		JP	2000-150900			05/30/2000		Abst.
		JP	2004-103957			04/02/2004		Abst.

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Nomura et al., "Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Amorphous Oxide Semiconductors," NATURE, November 25, 2004, Vol. 432, pp. 488-492.	Eng.

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] See attached Kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

[1] Unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Please type a plus sign (+) inside this box → [+]

PTO/SB/08A (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	
(use as many sheets as necessary)				**Filing Date**	January 18, 2011
				First Named Inventor	Shunpei YAMAZAKI et al.
				Group Art Unit	
				Examiner Name	
Sheet	2	of	2	**Attorney Docket Number**	0756-9138

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] *(if known)*	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] *(if known)*	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.)., date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Prins et al., "A Ferroelectric Transparent Thin-Film Transistor," APPL. PHYS. LETT. (APPLIED PHYSICS LETTERS), June 17, 1996, Vol. 68, No. 25, pp. 3650-3652.	Eng.
		Nakamura et al., "The Phase Relations In the In_2O_3-Ga_2ZnO_4-ZnO System at 1350°C," JOURNAL OF SOLID STATE CHEMISTRY, August 1, 1991, Vol. 93, No. 2, pp. 298-315.	Eng.
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		Nomura et al., "Thin-Film Transistor Fabricated in Single-Crystalline Transparent Oxide Semiconductor," SCIENCE, May 23, 2003, Vol. 300, No. 5623, pp. 1269-1272.	Eng.

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

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I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

____

____

SEMICONDUCTOR DEVICE

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

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Prior Foreign Application(s)
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Priority Not Claimed
優先権主張なし

2010-012540	Japan	January 22, 2010	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	

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(Application No.) (出願番号)	(Filling Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況:特許許可済、継続中、放棄済)
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(Application No.) (出願番号)	(Filling Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況:特許許可済、継続中、放棄済)
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(Application No.) (出願番号)	(Filling Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況:特許許可済、継続中、放棄済)
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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number).

Eric J. Robinson Reg. No. 38,285

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書類送付先

Send Correspondence to:

Eric J. Robinson.
Robinson Intellectual Property Law Office
3975 Fair Ridge Drive
Suite 20 North
Fairfax, Virginia 22033

直接電話連絡先：（名前及び電話番号）

Direct Telephone Calls to: (name and telephone number)

Eric J. Robinson
(571) 434-6789

唯一または第一発明者名		Full name of sole or first inventor Shunpei YAMAZAKI	
発明者の署名	日付	Inventor's signature	Date
		Shunpei Yamazaki	12/27/2010
住所		Residence Setagaya, Tokyo, Japan	
国籍		Citizenship Japanese	
私書箱		Post Office Address c/o Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036 Japan	

第二共同発明者名		Full name of second joint inventor, if any Hiromichi GODO	
第二共同発明者の署名	日付	Second inventor's signature	Date
		Hiromichi Godo	01/10/2011
住所		Residence Isehara, Kanagawa, Japan	
国籍		Citizenship Japanese	
私書箱		Post Office Address c/o Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036 Japan	

第三共同発明者名		Full name of third joint inventor, if any Hideomi SUZAWA	
第三共同発明者の署名	日付	Third inventor's signature	Date
		Hideomi Suzawa	01/06/2011
住所		Residence Atsugi, Kanagawa, Japan	
国籍		Citizenship Japanese	
私書箱		Post Office Address c/o Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036 Japan	

第四共同発明者名	Full name of fourth joint inventor, if any Shinya SASAGAWA
第四共同発明者の署名　　日付	Fourth inventor's signature　　Date Shinya SASAGAWA　01/06/2011
住所	Residence Chigasaki, Kanagawa, Japan
国籍	Citizenship Japanese
私書箱	Post Office Address c/o Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036 Japan

第五共同発明者名	Full name of fifth joint inventor, if any Motomu KURATA
第五共同発明者の署名　　日付	Fifth inventor's signature　　Date Motomu KURATA　01/06/2011
住所	Residence Isehara, Kanagawa, Japan
国籍	Citizenship Japanese
私書箱	Post Office Address c/o Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036 Japan

第六共同発明者名	Full name of sixth joint inventor, if any Mayumi MIKAMI
第六共同発明者の署名　　日付	Sixth inventor's signature　　Date Mayumi Mikami　01/06/2011
住所	Residence Atsugi, Kanagawa, Japan
国籍	Citizenship Japanese
私書箱	Post Office Address c/o Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036 Japan

DESCRIPTION

SEMICONDUCTOR DEVICE

5 TECHNICAL FIELD

[0001]

A technical field of the present invention relates to a semiconductor device. Note that semiconductor devices herein refer to general elements and devices which function by utilizing semiconductor characteristics.

10

BACKGROUND ART

[0002]

There are a wide variety of metal oxides and such metal oxides are used for various applications. Indium oxide is a well-known material and has been used for 15 transparent electrodes required in liquid crystal display devices or the like.

[0003]

Some metal oxides have semiconductor characteristics. The examples of such metal oxides having semiconductor characteristics are, for example, tungsten oxide, tin oxide, indium oxide, zinc oxide, and the like. A thin film transistor in which a channel 20 formation region is formed using such metal oxides is already known (for example, see Patent Documents 1 to 4, Non-Patent Document 1, and the like).

[0004]

As metal oxides, not only single-component oxides but also multi-component oxides are known. For example, $InGaO_3(ZnO)_m$ (m: natural number) having a 25 homologous phase is known as a multi-component oxide semiconductor including In, Ga, and Zn (for example, see Non-Patent Documents 2 to 4 and the like).

[0005]

Furthermore, it is confirmed that an oxide semiconductor including such an In-Ga-Zn-based oxide is applicable to a channel formation region of a thin film 30 transistor (for example, see Patent Document 5, Non-Patent Documents 5 and 6, and the like).

[References]

[Patent Documents]

[0006]

[Patent Document 1] Japanese Published Patent Application No. S60-198861

[Patent Document 2] Japanese Published Patent Application No. H8-264794

5 [Patent Document 3] Japanese Translation of PCT International Application No. H11-505377

[Patent Document 4] Japanese Published Patent Application No. 2000-150900

[Patent Document 5] Japanese Published Patent Application No. 2004-103957

10 [Non-Patent Document]

[0007]

[Non-Patent Document 1] M. W. Prins, K. O. Grosse-Holz, G. Muller, J. F. M. Cillessen, J. B. Giesbers, R. P. Weening, and R. M. Wolf, "A ferroelectric transparent thin-film transistor", *Appl. Phys. Lett.*, 17 June 1996, Vol.68 pp.3650-3652

15 [Non-Patent Document 2] M. Nakamura, N. Kimizuka, and T. Mohri, "The Phase Relations in the In_2O_3-Ga_2ZnO_4-ZnO System at 1350 °C", *J. Solid State Chem.*, 1991, Vol.93, pp.298-315

[Non-Patent Document 3] N. Kimizuka, M. Isobe, and M. Nakamura, "Syntheses and Single-Crystal Data of Homologous Compounds, $In_2O_3(ZnO)_m$ (m = 3, 4, and 5),

20 $InGaO_3(ZnO)_3$, and $Ga_2O_3(ZnO)_m$ (m = 7, 8, 9, and 16) in the In_2O_3-$ZnGa_2O_4$-ZnO System", *J. Solid State Chem.*, 1995, Vol.116, pp.170-178

[Non-Patent Document 4] M. Nakamura, N. Kimizuka, T. Mohri, and M. Isobe, "Syntheses and crystal structures of new homologous compounds, indium iron zinc oxides ($InFeO_3(ZnO)_m$) (m:natural number) and related compounds", *KOTAI BUTSURI*

25 *(SOLID STATE PHYSICS)*, 1993, Vol. 28, No. 5, pp. 317–327

[Non-Patent Document 5] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor", *SCIENCE*, 2003, Vol. 300, pp. 1269-1272

[Non-Patent Document 6] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H.

30 Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors", *NATURE*, 2004, Vol.432 pp.488-492

DISCLOSURE OF INVENTION

[0008]

In order to achieve high-speed operation, low power consumption, cost reduction, or the like of a transistor, it is necessary to miniaturize a transistor.

[0009]

In the case where a transistor is miniaturized, defects generated in a manufacturing process become a major problem. For example, each of a source electrode and a drain electrode and a channel formation region are electrically connected; however, disconnections, poor connections, and the like may occur due to a decrease in coverage by the miniaturization.

[0010]

In addition, in the case where a transistor is miniaturized, a problem of a short-channel effect is also caused. The short-channel effect refers to degradation of electrical characteristics which becomes obvious with miniaturization of a transistor (a reduction in channel length (L)). The short-channel effect results from the effect of an electric field of a drain electrode on a source electrode. Specific examples of the short-channel effect are a decrease in threshold voltage, an increase in subthreshold swing (S value), an increase in leakage current, and the like. In particular, it is known that a transistor including an oxide semiconductor has smaller off current at a room temperature as compared to a transistor including silicon. This is attributed to the fact that carriers generated by thermal excitation are small, that is, carrier density is small. In the transistor in which a material whose carrier density is small is used as described above, a short-channel effect such as a decrease in a threshold voltage tends to be caused easily.

[0011]

Thus, according to an embodiment of the disclosed invention, it is an object of the present invention to provide a semiconductor device which achieves miniaturization while the defects are suppressed. Further, it is another object of the present invention to provide a semiconductor device which achieves miniaturization while favorable characteristics are maintained.

[0012]

One embodiment of the disclosed invention is a semiconductor device which includes an oxide semiconductor layer, a source electrode and a drain electrode in contact with the oxide semiconductor layer, a gate electrode overlapping with the oxide semiconductor layer, and a gate insulating layer provided between the oxide semiconductor layer and the gate electrode, in which the source electrode and the drain electrode each include a first conductive layer, and a second conductive layer having a region which extends in a channel length direction from an end portion of the first conductive layer.

[0013]

In the above semiconductor device, each of the first conductive layer and the second conductive layer preferably has a tapered shape.

[0014]

In the above semiconductor device, sidewall insulating layers are preferably provided over the regions of each of the second conductive layer.

[0015]

Another embodiment of the disclosed invention is a semiconductor device which includes an oxide semiconductor layer, a source electrode and a drain electrode in contact with the oxide semiconductor layer, a gate electrode overlapping with the oxide semiconductor layer, and a gate insulating layer provided between the oxide semiconductor layer and the gate electrode, in which the source electrode and the drain electrode each include a first conductive layer and a second conductive layer having a higher resistance than the first conductive layer, where the second conductive layer is in contact with the oxide semiconductor layer.

[0016]

Another embodiment of the disclosed invention is a semiconductor device which includes an oxide semiconductor layer, a source electrode and a drain electrode in contact with the oxide semiconductor layer, a gate electrode overlapping with the oxide semiconductor layer, and a gate insulating layer provided between the oxide semiconductor layer and the gate electrode, in which the source electrode and the drain electrode each include a first conductive layer and a second conductive layer having a higher resistance than the first conductive layer, where the second conductive layer and the first conductive layer are in contact with the oxide semiconductor layer.

[0017]

In the above semiconductor device, the second conductive layer is preferably a nitride of a metal.

[0018]

5 In the above semiconductor device, the thickness of the second conductive layer is preferably from 5 nm to 15 nm.

[0019]

Another embodiment of the disclosed invention is a semiconductor device which includes an oxide semiconductor layer including a channel formation region, a 10 source electrode and a drain electrode in contact with the channel formation region, a gate electrode overlapping with the channel formation region, and a gate insulating layer provided between the oxide semiconductor layer and the gate electrode, in which a region in each of the source electrode and the drain electrode in contact with the channel formation region of the oxide semiconductor layer has a higher resistance than other 15 regions.

[0020]

In the above semiconductor device, each of the source electrode and the drain electrode is in contact with the oxide semiconductor layer at an end portion thereof, and an insulating layer is provided between the source electrode and the oxide 20 semiconductor layer or between the drain electrode and the oxide semiconductor layer.

[0021]

Note that semiconductor devices herein refer to general devices which function by utilizing semiconductor characteristics. For example, a display device, a memory device, an integrated circuit, and the like are included in the category of the 25 semiconductor device.

[0022]

In this specification and the like, the terms "over" and "below" do not necessarily mean "directly on" and "directly below", respectively, in the description of a physical relationship between components. For example, the expression "a gate 30 electrode over a gate insulating layer" can mean the case where there is an additional component between the gate insulating layer and the gate electrode. Moreover, the

terms such as "over" and "below" are only used for convenience of description and can include the case where the relation of components is reversed, unless otherwise specified.

[0023]

5 In addition, in this specification and the like, the term such as "electrode" or "wiring" does not limit a function of a component. For example, an "electrode" is sometimes used as part of a "wiring", and vice versa. Furthermore, the term "electrode" or "wiring" can include the case where a plurality of "electrodes" or "wirings" are formed in an integrated manner.

10 [0024]

Functions of a "source electrode" and a "drain electrode" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flowing is changed in circuit operation, for example. Therefore, the terms "source electrode" and "drain electrode" can be replaced with each other in

15 this specification.

[0025]

Note that in this specification and the like, the term "electrically connected" includes the case where components are connected through an object having any electric function. There is no particular limitation on an object having any electric function as

20 long as electric signals can be transmitted and received between components that are connected through the object. Examples of an "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions as well as an electrode and a wiring.

[0026]

25 According to one embodiment of the disclosed invention, either of the following effects or both of the effects can be obtained.

[0027]

First, each of the source electrode and the drain electrode is formed to have a stacked structure including the first conductive layer and the second conductive layer, a

30 region which extends in the channel length direction from an end portion of the first conductive layer is provided; thus, coverage in forming a semiconductor layer over the source electrode and the drain electrode is improved. Therefore, occurrence of poor

connections or the like can be prevented.

[0028]

Second, in the source electrode or the drain electrode, a vicinity of the region in contact with the channel formation region can be high-resistance region, whereby an electric field between the source electrode and the drain electrode can be relieved. Thus, the short-channel effect such as a decrease in a threshold voltage can be suppressed.

[0029]

With such an effect, a problem accompanied with miniaturization can be resolved. As a result, the size of a transistor can be sufficiently reduced. By sufficiently reducing the size of the transistor, an area of a semiconductor device including the transistor is decreased, and the number of semiconductor devices obtained from one substrate is increased. Accordingly, manufacturing costs of the semiconductor device can be reduced. Further, since the semiconductor device is downsized, the semiconductor device which is substantially the same in size with further increased function can be realized. Furthermore, effects of high-speed operation, low power consumption, and the like of a transistor can be obtained in accordance with a reduction in channel length. Thus, miniaturization of a transistor including an oxide semiconductor can be achieved according to an embodiment of the disclosed invention, and various effects accompanied with the miniaturization can be obtained.

[0030]

As described above, according to an embodiment of the disclosed invention, a semiconductor device which achieves miniaturization can be provided while the defects are suppressed and favorable characteristics are maintained.

BRIEF DESCRIPTION OF DRAWINGS

[0031]

In the accompanying drawings:

FIGS. 1A to 1D are cross-sectional views of semiconductor devices;

FIGS. 2A to 2F are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 3A to 3F are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIG. 4 is a cross-sectional view of a semiconductor device;

FIGS. 5A to 5F are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 6A1, 6A2, and 6B illustrate examples of a circuit diagram of a semiconductor device;

FIGS. 7A and 7B illustrate examples of a circuit diagram of a semiconductor device;

FIGS. 8A to 8C illustrate examples of a circuit diagram of a semiconductor device;

FIGS. 9A to 9F illustrate examples of an electronic device;

FIGS. 10A and 10B are cross-sectional views each illustrating a model of a transistor used for the simulation;

FIGS. 11A and 11B are graphs each showing a relationship between a channel length L (nm) and the amount of shift in threshold voltage ΔVth (V);

FIGS. 12A and 12B are graphs each showing a relationship between a channel length L (nm) and the amount of shift in threshold voltage ΔVth (V); and

FIG. 13 is a graph showing a relationship between a channel length L (nm) and the amount of shift in threshold voltage ΔVth (V).

BEST MODE FOR CARRYING OUT THE INVENTION

[0032]

Hereinafter, embodiments of the present invention will be described with reference to the drawings. Note that the present invention is not limited to the following description and it will be readily appreciated by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the invention should not be construed as being limited to the description in the following embodiments.

[0033]

Note that the position, the size, the range, or the like of each structure

illustrated in drawings and the like is not accurately represented in some cases for easy understanding. Therefore, the disclosed invention is not necessarily limited to the position, size, range, or the like as disclosed in the drawings and the like.

[0034]

5 In this specification and the like, ordinal numbers such as "first", "second", and "third" are used in order to avoid confusion among components, and the terms do not mean limitation of the number of components.

[0035]

(Embodiment 1)

10 In this embodiment, an example of a structure and a manufacturing process of a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIGS. 1A to 1D, FIGS. 2A to 2F, and FIGS. 3A to 3F.

[0036]

<Example of Structure of Semiconductor Device>

15 In FIGS. 1A to 1D, as examples of semiconductor devices, cross-sectional structures of transistors are illustrated. In FIGS. 1A to 1D, top-gate transistors are illustrated as transistors according to one embodiment of the disclosed invention.

[0037]

A transistor 160 illustrated in FIG. 1A includes, over a substrate 100, a source 20 electrode in which a first conductive layer 142a and a second conductive layer 145a are stacked in this order; a drain electrode in which a first conductive layer 142b and a second conductive layer 145b are stacked in this order; an insulating layer 143a provided over the source electrode; an insulating layer 143b provided over the drain electrode; an oxide semiconductor layer 144 provided over the insulating layers 143a 25 and 143b; a gate insulating layer 146 provided over the oxide semiconductor layer 144; and a gate electrode 148 provided over the gate insulating layer 146.

[0038]

In the transistor 160 illustrated in FIG. 1A, the second conductive layer 145a has a region which extends in the channel length direction (a flowing direction of 30 carriers) from an end portion of the first conductive layer 142a, and the second conductive layer 145a and at least a channel formation region of the oxide semiconductor layer 144 are in contact with each other. Further, the second conductive

layer 145b has a region which extends in the channel length direction from an end portion of the first conductive layer 142b, and the second conductive layer 145b and at least the channel formation region of the oxide semiconductor layer 144 are in contact with each other.

5 [0039]

More specifically, the second conductive layer 145a has the region which extends in the channel length direction (the flowing direction of carriers) from the end portion of the first conductive layer 142a toward the drain electrode. Further, the second conductive layer 145b has the region which extends in the channel length

10 direction from the end portion of the first conductive layer 142b toward the source electrode.

[0040]

One different point of the transistor 170 illustrated in FIG. 1B from the transistor 160 illustrated in FIG. 1A is the existence of the insulating layers 143a and

15 143b. In the transistor 170 illustrated in FIG. 1B, the oxide semiconductor layer 144 is provided so as to be in contact with top surfaces and end portions of the second conductive layers 145a and 145b.

[0041]

Also in the transistor 170 illustrated in FIG. 1B, as in the transistor 160, the

20 second conductive layer 145a has a region which extends in the channel length direction from the end portion of the first conductive layer 142a, and the second conductive layer 145b has a region which extends in the channel length direction from the end portion of the first conductive layer 142b.

[0042]

25 One different point of the transistor 180 illustrated in FIG. 1C from the transistor 160 illustrated in FIG. 1A is the stacking order of the first conductive layer 142a and the second conductive layer 145a and the stacking order of the first conductive layer 142b and the second conductive layer 145b. The transistor 180 illustrated in FIG. 1C has a source electrode in which the second conductive layer 145a and the first

30 conductive layer 142a are stacked in this order and a drain electrode in which the second conductive layer 145b and the first conductive layer 142b are stacked in this order.

[0043]

Further, in the transistor 180 illustrated in FIG. 1C, the second conductive layer 145a has a region which extends in the channel length direction from the end portion of the first conductive layer 142a, and the second conductive layer 145b has a region which extends in the channel length direction from the end portion of the first conductive layer 142b. Thus, the insulating layer 143a is provided so as to be in contact with the first conductive layer 142a and the region in the second conductive layer 145a, which extends in the channel length direction from the end portion of the first conductive layer 142a. Furthermore, the insulating layer 143b is provided so as to be in contact with the first conductive layer 142b and the region in the second conductive layer 145b, which extends in the channel length direction from the end portion of the first conductive layer 142b.

[0044]

One different point of the transistor 190 illustrated in FIG. 1D from the transistor 180 illustrated in FIG. 1C is the existence of the insulating layers 143a and 143b. In the transistor 190 illustrated in FIG. 1D, the oxide semiconductor layer 144 is provided so as to be in contact with the first conductive layers 142a and 142b, the region in the second conductive layer 145a, which extends in the channel length direction from the end portion of the first conductive layer 142a, and the region in the second conductive layer 145b, which extends in the channel length direction from the end portion of the first conductive layer 142b.

[0045]

In the transistor 190 illustrated in FIG. 1D, the second conductive layer 145a has the region which extends in the channel length direction from the end portion of the first conductive layer 142a, and the second conductive layer 145a and at least the channel formation region of the oxide semiconductor layer 144 are in contact with each other. Furthermore the second conductive layer 145b has the region which extends in the channel length direction from the end portion of the first conductive layer 142b, and the second conductive layer 145b and at least the channel formation region of the oxide semiconductor layer 144 are in contact with each other.

[0046]

<Example of Manufacturing Process of Transistor>

An example of a manufacturing process of a transistor illustrated in FIGS. 1A to 1D will be described below with reference to FIGS. 2A to 2F and FIGS. 3A to 3F.

[0047]

<Manufacturing Process of Transistor 160 and Transistor 170>

First, with reference to FIGS. 2A to 2F, an example of a manufacturing process of the transistor 160 illustrated in FIG. 1A will be described. Note that the manufacturing process of the transistor 160 can be referred to for the transistor 170 illustrated in FIG. 1B except that the insulating layers 143a and 143b are not provided; thus detailed description is omitted.

[0048]

First, a first conductive film is formed over the substrate 100 having an insulating surface, and then etching is selectively performed on the first conductive film, so that the first conductive layers 142a and 142b are formed (see FIG. 2A). The first conductive film has a thickness of, for example, 50 nm to 500 nm.

[0049]

Note that there is no particular limitation on a substrate that can be used as the substrate 100 as long as it has at least heat resistance to withstand later heat treatment. For example, a substrate such as a glass substrate, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like can be used. As long as the substrate 100 has an insulating surface, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon, carbon silicon, or the like; a compound semiconductor substrate of silicon germanium or the like; an SOI substrate; or the like can be used as the substrate 100, and a semiconductor element can be provided over the substrate. In addition, a base film may be provided over the substrate 100.

[0050]

The first conductive film can be formed by a PVD method such as a sputtering method or a CVD method such as a plasma CVD method. As a material of the first conductive layer, an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten, a nitride thereof, an alloy containing any of the above elements as its component, or the like can be used. Any of manganese, magnesium, zirconium, and beryllium, or a material including any of these in combination may be used. Further, aluminum combined with an element selected

from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium, or a material including any of these in combination may be used

[0051]

The first conductive layer may have either a single-layer structure or a staked structure of two or more layers. For example, the first conductive film may have a single-layer structure of a titanium layer, a single-layer structure of an aluminum film including silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, or a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order. Note that in the case where the first conductive layer has a single-layer structure, there is an advantage that the first conductive layer can be easily processed into the source and drain electrode each having a tapered shape.

[0052]

The first conductive film may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an indium oxide-tin oxide alloy (In_2O_3-SnO_2, which is abbreviated to ITO in some cases), an indium oxide-zinc oxide alloy (In_2O_3-ZnO), or any of these metal oxide materials in which silicon or silicon oxide is included can be used.

[0053]

The first conductive film is preferably etched so that end portions of the first conductive layers 142a and 142b are tapered. Here, a taper angle $\alpha 1$ is an angle of a side surface of an end portion of the first conductive layer 142a with respect to a substrate surface, and a taper angle $\beta 1$ is an angle of a side surface of an end portion of the first conductive layer 142b with respect to the substrate surface. For example, each of the taper angle $\alpha 1$ and the taper angle $\beta 1$ is preferably greater than or equal to 30° and less than or equal to 60° (see FIG. 2A).

[0054]

Next, the second conductive film 145 is formed so as to cover the first conductive layers 142a and 142b and the substrate 100. The film thickness of the second conductive film 145 is from 3 nm to 30 nm, preferably, 5 nm to 15 nm.

[0055]

The second conductive film 145 can be formed using a material and a method similar to those of the first conductive film. As a material of the second conductive film, an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten, a nitride thereof, an alloy containing any of the above
5 elements as its component, or the like can be used. Any of manganese, magnesium, zirconium, and beryllium, or a material including any of these in combination may be used. Alternatively, aluminum combined with an element selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium, or a material including any of these in combination may be used. Further alternatively, a conductive
10 metal oxide such as indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an indium oxide-tin oxide alloy (In_2O_3-SnO_2, which is abbreviated to ITO in some cases), an indium oxide-zinc oxide alloy (In_2O_3-ZnO), or any of these metal oxide materials containing silicon or silicon oxide may be used.

[0056]

15 As the material for the second conductive film 145, a material having higher resistance than the first conductive layers 142a and 142b is preferably used. This is because in the source electrode and the drain electrode of the transistor 160 to be manufactured, regions in contact with the channel formation region of the oxide semiconductor layer become higher resistance than other regions, whereby an electric
20 field between the source electrode and the drain electrode can be relieved, and a short-channel effect can be controlled. As a conductive material used for the second conductive film 145, for example, a metal nitride such as titanium nitride, tungsten nitride, tantalum nitride, or molybdenum nitride can be preferably used. The second conductive film 145 serves one part of the source electrode or the drain electrode and is
25 in contact with the oxide semiconductor layer; thus, a material which does not cause a chemical reaction by contact with the oxide semiconductor layer is preferably used. The above mentioned metal nitride is preferable in this regard.

[0057]

Then, the insulating film 143 is formed with a thickness of 50 nm to 300 nm,
30 preferably 100 nm to 200 nm over the second conductive film 145 (see FIG. 2A). In this embodiment, as the insulating film 143, a silicon oxide film is formed. As illustrated in the transistor 170 of FIG. 1B, the insulating film 143 is not necessarily

formed. However, in the case where the insulating film 143 is provided, contact regions (contact areas and the like) between each of the source electrode and the drain electrode to be formed later and the oxide semiconductor layer can be controlled easily. That is, the resistance of the source electrode or the drain electrode can be easily controlled, and the short-channel effect can be effectively controlled. Furthermore, by providing the insulating film 143, parasitic capacitance between the gate electrode to be formed later and each of the source electrode and the drain electrode can be reduced.

[0058]

Next, a mask is formed over the insulating film 143, and the insulating film 143 is etched using the mask, whereby the insulating layers 143a and 143b are formed (see FIG. 2B). For the etching of the insulating film 143, either wet etching or dry etching can be used. Alternatively, wet etching and dry etching may be used in combination. The etching conditions (e.g., an etching gas or an etchant, etching time, and temperature) are set as appropriate depending on the material so that the insulating film can be etched into a desired shape. However, it is preferable to use dry etching for microfabrication of a channel length (L) of the transistor. As an etching gas used for dry etching, for example, a gas containing fluorine, such as sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3), or trifluoromethane (CHF_3), a mixed gas of carbon tetrafluoride (CF_4) and hydrogen, or the like can be used. A rare gas (heliun (He), argon (Ar), or xenon (Xe)), carbon monoxide, carbon dioxide, or the like may be added to the etching gas for dry etching.

[0059]

Then, by using the mask used for etching of the insulating film 143, the second conductive film 145 is etched, whereby the second conductive layers 145a and 145b are formed (see FIG. 2C). The mask is removed before the second conductive film 145 is etched, and the second conductive film 145 may be etched using the insulating layers 143a and 143b as masks. Further, as illustrated in the transistor 170 of FIG. 1B, in the case where the insulating layer is not provided, a mask may be directly formed on the second conductive film 145 and the second conductive film 145 may be etched. The second conductive film 145 is preferably etched so that end portions of the second conductive layers 145a and 145b are tapered. In the case where the insulating layer 143 is provided, etching is preferably performed so that end portions of the insulating

layers 143a and 143b are also tapered. Here, a taper angle α2 is an angle of a side surface of an end portion of the second conductive layer 145a and the insulating film 143a with respect to the substrate surface, and a taper angle β2 is an angle of a side surface of an end portion of the second conductive layer 145b and the insulating layer 143b with respect to the substrate surface. For example, each of the taper angle α2 and the taper angle β2 is preferably greater than or equal to 30° and less than or equal to 60°.

[0060]

For the etching of the second conductive film 145, either wet etching or dry etching can be used. Alternatively, wet etching and dry etching may be used in combination. The etching conditions (e.g., an etching gas or an etchant, etching time, and temperature) are set as appropriate depending on the material so that the second conductive film 145 can be etched into a desired shape. However, it is preferable to use dry etching for microfabrication of a channel length (L) of the transistor. As an etching gas used for etching the second conductive film 145, for example, chlorine (Cl_2), boron trichloride (BCl_3), silicon tetrachloride ($SiCl_4$), carbon tetrafluoride (CF_4), sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3), or the like, or a mixed gas selected from two or more of the above-mentioned gases may be used. Further, a rare gas (heliun (He), or Argon (Ar)), oxygen, or the like may be added to the etching gas for dry etching. Furthermore, the second conductive film 145 can be etched successively using the same gas used for etching of the insulating film 143.

[0061]

With this etching process, the source electrode in which the first conductive layer 142a and the second conductive layer 145a are stacked and the drain electrode in which the first conductive layer 142b and the second conductive layer 145b are stacked are formed. The mask used for the etching is adjusted as appropriate, whereby the second conductive layer 145a having the region which extends in the channel length direction from the end portion of the first conductive layer 142a and the second conductive layer 145b having the region which extends in the channel length direction from the end portion of the first conductive layer 142b can be formed.

[0062]

Note that the channel length (L) of the transistor 160 is determined by the distance between the lower end portion of the second conductive layer 145a and the lower end portion of the second conductive layer 145b. The channel length (L) differs depending on the application of the transistor 160; which can be, for example, 10 nm to 5 1000 nm, preferably, 20 nm to 400 nm.

[0063]

Note that in the case where a transistor with a channel length (L) of less than 25 nm is formed, for light exposure for forming a mask used for etching the insulating film 143 and the second conductive film 145, it is preferable to use extreme ultraviolet 10 whose wavelength is as short as several nanometers to several tens of nanometers. In the light exposure by extreme ultraviolet light, the resolution is high and the focus depth is large. For these reasons, the channel length (L) of the transistor formed later can be sufficiently reduced, and the circuit can operate at higher speed. Moreover, power consumption of the semiconductor device can be reduced by miniaturization.

15 [0064]

In the second conductive layer, the region which extends in the channel length direction from the end portion of the first conductive layer has an effect of improving coverage in the later step of forming the oxide semiconductor layer and the gate insulating layer. In the second conductive layer 145a, the length (L_S) in the channel 20 length direction in the region which extends in the channel length direction from the end portion of the first conductive layer 142a and the length (L_D) in the channel length direction in the region which extends in the channel length direction from the end portion of the first conductive layer 142b are not always the same. However, in the case where a plurality of transistors 160 is provided over one substrate, the total length 25 of L_S and L_D is almost constant.

[0065]

Next, the oxide semiconductor layer 144 is formed over the insulating layers 143a and 143b and the substrate 100 with a sputtering method (see FIG. 2D). The oxide semiconductor layer 144 has a thickness of, for example, 3 nm to 30 nm, 30 preferably, 5 nm to 15 nm. The formed oxide semiconductor layer 144 is in contact with the second conductive layers 145a and 145b at least in its channel formation region.

[0066]

Here, the second conductive layers 145a and 145b have regions which extend in the channel length direction from end portions of the first conductive layers 142a and 142b, respectively; therefore, steps on the end portions of the source electrode and the drain electrode can be made gradual. Thus, it is possible to improve the coverage of the oxide semiconductor layer 144 and to prevent breaking of the film.

[0067]

Note that the source electrode and the drain electrode of the transistor 160 to be manufactured is in contact with the oxide semiconductor layer 144 only at end portions of the second conductive layers 145a and 145b, respectively. Accordingly, the contact area can be drastically reduced compared to the case where the top surface of the source electrode and the drain electrode of the transistor 160 is also in contact with the oxide semiconductor layer 144. By reducing the contact area of the source electrode and the drain electrode and the oxide semiconductor layer 144 in such a manner, contact resistance at a contact interface can be increased and an electric field between the source electrode and the drain electrode can be relieved. Note that a technical idea of the disclosed invention is to form a high-resistance region in the source electrode and the drain electrode. Thus, it is not necessary that the source electrode and the drain electrode be exactly in contact with the oxide semiconductor layer 144 only at end portions of the second conductive layers 145a and 145b. For example, part of the top surfaces of the second conductive layers 145a and 145b may be in contact with the oxide semiconductor layer 144.

[0068]

As the oxide semiconductor layer 144, any of the following oxide semiconductors can be used: an In-Sn-Ga-Zn-O-based oxide semiconductor which is a four-component metal oxide; an In-Ga-Zn-O-based oxide semiconductor, an In-Sn-Zn-O-based oxide semiconductor, an In-Al-Zn-O-based oxide semiconductor, a Sn-Ga-Zn-O-based oxide semiconductor, an Al-Ga-Zn-O-based oxide semiconductor, or a Sn-Al-Zn-O-based oxide semiconductor which are three-component metal oxides; an In-Zn-O-based oxide semiconductor, a Sn-Zn-O-based oxide semiconductor, an Al-Zn-O-based oxide semiconductor, a Zn-Mg-O-based oxide semiconductor, a Sn-Mg-O-based oxide semiconductor, or an In-Mg-O-based oxide semiconductor which

are two-component metal oxides; or an In-O-based oxide semiconductor, a Sn-O-based oxide semiconductor, or a Zn-O-based oxide semiconductor which are single-component metal oxides.

[0069]

5 In particular, an In-Ga-Zn-O-based oxide semiconductor material has sufficiently high resistance when there is no electric field and thus off current can be sufficiently reduced. In addition, having a high field-effect mobility, the In-Ga-Zn-O-based oxide semiconductor material is preferable as a semiconductor material.

10 [0070]

As a typical example of the In-Ga-Zn-O-based oxide semiconductor material, one represented by $InGaO_3(ZnO)_m$ ($m > 0$ and m is not a natural number) is given. Using M instead of Ga, there is an oxide semiconductor material expressed by $InMO_3(ZnO)_m$ ($m > 0$ and m is not a natural number). Here, M denotes one or more of 15 metal elements selected from gallium (Ga), aluminum (Al), iron (Fe), nickel (Ni), manganese (Mn), cobalt (Co), and the like. For example, M may be Ga, Ga and Al, Ga and Fe, Ga and Ni, Ga and Mn, Ga and Co, or the like. Note that the above-described compositions are derived from the crystal structures of the oxide semiconductor material and are only examples.

20 [0071]

As a target for forming the oxide semiconductor layer 144 with a sputtering method, a target having a composition ratio of In:Ga:Zn = 1:x:y (x is 0 or more and y is more than or equal to 0.5 and less than or equal to 5) is preferably used. For example, a metal oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:2 [molar 25 ratio], or the like can be used. Alternatively, a metal oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:1 [molar ratio], a metal oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:4 [molar ratio], or a metal oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:0:2 [molar ratio] can be used.

[0072]

30 In this embodiment, the oxide semiconductor layer 144 having an amorphous structure is formed by a sputtering method using an In-Ga-Zn-O-based metal oxide

target.

[0073]

The relative density of the metal oxide in the metal oxide target is greater than or equal to 80 %, preferably greater than or equal to 95 %, and more preferably greater than or equal to 99.9 %. With the use of the metal oxide target with high relative density, the oxide semiconductor layer 144 having a dense structure can be formed.

[0074]

The atmosphere in which the oxide semiconductor layer 144 is formed is preferably a rare gas (typically argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas (typically argon) and oxygen. Specifically, it is preferable to use a high-purity gas atmosphere, for example, from which an impurity such as hydrogen, water, a hydroxyl group, or a hydride is removed so that the concentration is 1 ppm or lower (preferably 10 ppb or lower).

[0075]

In forming the oxide semiconductor layer 144, for example, an object (here, a structure including the substrate 100) is held in a treatment chamber kept under reduced pressure and the object is heated to a temperature higher than or equal to 100 °C and lower than 550 °C, preferably higher than or equal to 200 °C and lower than or equal to 400 °C. Alternatively, the temperature of the object in forming the oxide semiconductor layer 144 may be room temperature. While moisture remaining in the treatment chamber is removed, a sputtering gas from which hydrogen, moisture and the like are removed is introduced, and the oxide semiconductor layer144 is formed with the use of the target. The oxide semiconductor layer 144 is formed while the object is heated, so that impurities contained in the oxide semiconductor layer 144 can be reduced. Moreover, damage due to sputtering can be reduced. In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, a titanium sublimation pump, or the like can be used. A turbo pump provided with a cold trap may be used. By evacuation with the cryopump or the like, hydrogen, water, and the like can be removed from the treatment chamber, whereby the impurity concentration of the oxide semiconductor layer 144 can be reduced.

[0076]

The oxide semiconductor layer 144 can be formed under the following conditions, for example: the distance between the object and the target is 170 mm, the pressure is 0.4 Pa, the direct current (DC) power is 0.5 kW, and the atmosphere is an oxygen (100 % oxygen) atmosphere, an argon (100 % argon) atmosphere, or a mixed atmosphere of oxygen and argon. A pulse direct current (DC) power supply is preferable because powder substances (also referred to as particles or dust) generated in the film formation can be reduced and the film thickness can be made uniform. The thickness of the oxide semiconductor layer 144 is 3 nm to 30 nm, preferably, 5 nm to 15 nm. Using the oxide semiconductor layer 144 with such a thickness can suppress the short-channel effect due to miniaturization. Note that an appropriate thickness differs depending on an oxide semiconductor material used, the usage of a semiconductor device, or the like; therefore, it is also possible to set the thickness as appropriate depending on the material to be used, the usage, or the like.

[0077]

Note that before the oxide semiconductor layer 144 is formed by a sputtering method, a material attached to a surface on which the oxide semiconductor layer 144 is formed (e.g., a surface of the insulating layers 143a and 143b) is preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. Here, the reverse sputtering is a method by which ions collide with a surface to be processed so that the surface is modified, in contrast to normal sputtering by which ions collide with a sputtering target. An example of a method for making ions collide with a surface to be processed is a method in which high-frequency voltage is applied to the surface to be processed in an argon atmosphere so that plasma is generated near the object. Note that a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used instead of an argon atmosphere.

[0078]

After that, heat treatment (first heat treatment) is preferably performed on the oxide semiconductor layer 144. Excess hydrogen (including water and a hydroxyl group) contained in the oxide semiconductor layer 144 can be removed by the first heat treatment; thus, the structure of the oxide semiconductor layer can be improved and a defect level in an energy gap can be reduced. The temperature of the first heat

treatment is, for example, higher than or equal to 300 °C and lower than 550 °C, or higher than or equal to 400 °C and lower than or equal to 500 °C.

[0079]

The heat treatment can be performed in such a way that, for example, an object is introduced into an electric furnace in which a resistance heating element or the like is used, and heated in a nitrogen atmosphere at 450 °C for an hour. The oxide semiconductor layer 144 is not exposed to the air during the heat treatment so that entry of water and hydrogen can be prevented.

[0080]

The heat treatment apparatus is not limited to the electric furnace and may be an apparatus for heating an object by thermal radiation or thermal conduction from a medium such as a heated gas. For example, a rapid thermal annealing (RTA) apparatus such as a lamp rapid thermal annealing (LRTA) apparatus or a gas rapid thermal annealing (GRTA) apparatus can be used. An LRTA apparatus is an apparatus for heating an object by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for performing heat treatment using a high-temperature gas. As the gas, an inert gas that does not react with an object by heat treatment, for example, nitrogen or a rare gas such as argon is used.

[0081]

For example, as the first heat treatment, a GRTA process may be performed as follows. An object is put in an inert gas atmosphere that has been heated, heated for several minutes, and taken out from the inert gas atmosphere. The GRTA process enables high-temperature heat treatment for a short time. Moreover, the GRTA process can be employed even when the temperature exceeds the upper temperature limit of the object. Note that the inert gas may be changed to a gas containing oxygen during the process. This is because a defect level in an energy gap caused by oxygen deficiency can be reduced by performing the first heat treatment in the atmosphere containing oxygen.

[0082]

Note that as the inert gas atmosphere, an atmosphere that contains nitrogen or a rare gas (e.g., helium, neon, or argon) as its main component and does not contain water, hydrogen, or the like is preferably used. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is greater than or equal to 6 N (99.9999 %), preferably greater than or equal to 7 N (99.99999 %) (that is, the concentration of the impurities is less than or equal to 1 ppm, preferably less than or equal to 0.1 ppm).

[0083]

In any case, the i-type (intrinsic) or substantially i-type oxide semiconductor layer 144 in which impurities are reduced by the first heat treatment is formed, which enables a transistor having extremely excellent characteristics to be realized.

[0084]

The above heat treatment (first heat treatment) can be referred to as dehydration treatment, dehydrogenation treatment, or the like because of its effect of removing hydrogen, water, and the like. The dehydration treatment or dehydrogenation treatment can be performed, for example, after the oxide semiconductor layer is formed, after the gate insulating layer is formed, or after the gate electrode is formed. Such dehydration treatment or dehydrogenation treatment may be performed once or plural times.

[0085]

Next, the gate insulating layer 146 which is in contact with the oxide semiconductor layer 144 is formed (see FIG. 2E). Here, the second conductive layers 145a and 145b have regions which extend in the channel length direction from end portions of the first conductive layers 142a and 142b, respectively; therefore, steps on the end portions of the source electrode and the drain electrode can be made gradual. Thus, it is possible to improve the coverage of the gate insulating layer 146 and to prevent breaking of the film.

[0086]

The gate insulating layer 146 can be formed by a CVD method, a sputtering method, or the like. The gate insulating layer 146 is preferably formed so as to contain silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide, tantalum oxide, hafnium oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate

to which nitrogen is added ($HfSi_xO_yN_z$ ($x > 0$, $y > 0$, $z > 0$)), hafnium aluminate to which nitrogen is added ($HfAl_xO_yN_z$ ($x > 0$, $y > 0$, $z > 0$)), or the like. The gate insulating layer 146 may have a single-layer structure or a stacked structure. There is no particular limitation on the thickness; however, in the case where the semiconductor
5 device is miniaturized, the thickness is preferably small for ensuring operation of the transistor. For example, in the case where silicon oxide is used, the thickness can be set to greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 10 nm and less than or equal to 50 nm.

[0087]

10 As described above, when the gate insulating layer 146 is made thin, there is a problem of gate leakage due to a tunneling effect or the like. In order to solve the problem of gate leakage, a high dielectric constant (high-k) material such as hafnium oxide, tantalum oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate to which nitrogen is added ($HfSi_xO_yN_z$ ($x > 0$, $y > 0$, $z > 0$)), or hafnium
15 aluminate to which nitrogen is added ($HfAl_xO_yN_z$ ($x > 0$, $y > 0$, $z > 0$)) is preferably used for the gate insulating layer 146. By using the high-k material for the gate insulating layer 146, electrical characteristics can be ensured and the thickness can be increased to prevent gate leakage. Note that a stacked structure of a film containing the high-k material and a film containing any one of silicon oxide, silicon nitride, silicon
20 oxynitride, silicon nitride oxide, aluminum oxide, and the like may be employed.

[0088]

After the gate insulating layer 146 is formed, second heat treatment is desirably performed in an inert gas atmosphere or an oxygen atmosphere. The temperature of the heat treatment is set to higher than or equal to 200 °C and lower than or equal to 450
25 °C, preferably higher than or equal to 250 °C and lower than or equal to 350 °C. For example, the heat treatment may be performed at 250 °C for 1 hour in a nitrogen atmosphere. The second heat treatment can reduce variation in electrical characteristics of transistors. Further, in the case where the gate insulating layer 146 contains oxygen, oxygen is supplied to the oxide semiconductor layer 144 to cover
30 oxygen deficiency in the oxide semiconductor layer 144, so that an i-type (intrinsic semiconductor) or substantially i-type oxide semiconductor layer can be formed.

[0089]

Note that although the second heat treatment is performed in this embodiment after the gate insulating layer 146 is formed, the timing of the second heat treatment is not limited thereto. For example, the second heat treatment may be performed after the gate electrode is formed. Alternatively, the second heat treatment may be performed following the first heat treatment, the first heat treatment may serve also as the second heat treatment, or the second heat treatment may serve also as the first heat treatment.

[0090]

As described above, at least one of the first heat treatment and the second heat treatment is applied, whereby the oxide semiconductor layer 144 can be highly purified as to minimize the amount of impurities that are not main components of the oxide semiconductor. The concentration of hydrogen in the oxide semiconductor layer 144 can be 5×10^{19} atoms/cm^3 or less, preferably 5×10^{18} atoms/cm^3 or less, more preferably 5×10^{17} atoms/cm^3 or less. Accordingly, the off-state current is sufficiently small. For example, the off current (per unit channel width (1 μm), here) of the transistor 160 at room temperature is 100 zA/μm (1 zA (zeptoampere) is 1×10^{-21} A) or less, preferably 10 zA/μm or less.

[0091]

Next, the gate electrode 148 is formed over the gate insulating layer 146 in a region overlapping with the channel formation region of the oxide semiconductor layer 144 (see FIG. 2F). The gate electrode 148 can be formed in such a manner that a conductive film is formed over the gate insulating layer 146 and then etched selectively. The conductive film to be the gate electrode 148 can be formed by a PVD method typified by a sputtering method or a CVD method such as a plasma CVD method. The details are similar to those of the source electrode, the drain electrode or the like; thus, the description thereof can be referred to. However, if the work function of the material of the gate electrode 148 is approximately the same as or smaller than the electron affinity of the oxide semiconductor layer 144, the threshold voltage sometimes shifts in the negative direction when a transistor is miniaturized. Thus, a material having a larger work function than the electron affinity of the oxide semiconductor layer

144 is preferably used. As such a material, for example, tungsten, platinum, gold, silicon which imparts p-type conductivity, or the like can be given.

[0092]

Through the above steps, the transistor 160 including the oxide semiconductor
5 layer 144 is completed.

[0093]

<Manufacturing Process of Transistor 180 or Transistor 190>

Next, an example of a manufacturing process of the transistor 180 illustrated in FIG. 1C will be described with reference to FIGS. 3A to 3F. Note that the
10 manufacturing process of the transistor 180 can be referred to for the transistor 190 illustrated in FIG. 1D except that the insulating layers 143a and 143b are not provided; thus detailed description is omitted.

[0094]

The second conductive film 145 is formed over the substrate 100. The second
15 conductive film 145 has a thickness of, for example, 3 nm to 30 nm, preferably, 5 nm to 15 nm. Then, the first conductive film is formed over the second conductive film 145 and then etched selectively, whereby the first conductive layers 142a and 142b are formed. After that, the insulating film 143 is formed over the first conductive layers 142a and 142b and the second conductive film 145 (see FIG. 3A).
20 [0095]

Note that in the case where the first conductive film is formed over the second conductive film, materials which can obtain etching selectivity is selected for the first conductive film and the second conductive film. Further, a material having higher resistance than the first conductive film is preferably used for the second conductive
25 film. In this embodiment, a titanium nitride film is formed as the second conductive film 145; a tungsten film or a molybdenum film is formed as the first conductive film; and the first conductive film is etched using a mixed gas of carbon tetrafluoride (CF_4), chlorine (Cl_2), and oxygen (O_2), a mixed gas of carbon tetrafluoride (CF_4), and oxygen (O_2), a mixed gas of sulfur hexafluoride (SF_6), chlorine (Cl_2), and oxygen (O_2), or a
30 mixed gas of sulfur hexafluoride (SF_6) and oxygen (O_2), whereby the first conductive layers 142a and 142b are formed.

[0096]

As illustrated in the transistor 190 of FIG. 1D, the insulating film 143 is not necessarily formed. However, by providing the insulating film 143, parasitic capacitance between the gate electrode to be formed later and each of the source electrode and the drain electrode can be reduced.

5 [0097]

Next, in a manner similar to the step shown in FIG. 2B, a mask is formed over the insulating film 143, and the insulating film 143 is etched using the mask, whereby the insulating layers 143a and 143b are formed (see FIG. 3B).

[0098]

10 Next, in a manner similar to the step shown in FIG. 2C, the second conductive film 145 is etched using the mask used for etching of the insulating layers 143a and 143b, whereby the second conductive layers 145a and 145b are formed (see FIG. 3C). Note that the mask may be removed before the second conductive film 145 is etched, and then the second conductive film 145 may be etched using the insulating layers 143a

15 and 143b as masks. As an etching gas used for etching the second conductive film 145, for example, chlorine (Cl_2), boron trichloride (BCl_3), silicon tetrachloride ($SiCl_4$), carbon tetrafluoride (CF_4), sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3), or the like, or a mixed gas selected from two or more of the above-mentioned gases can be used. Further, a rare gas (heliun (He), or Argon (Ar)) may be added to the etching gas.

20 Furthermore, as illustrated in the transistor 190 of FIG. 1D, in the case where an insulating layer is not provided, a mask is directly formed on the second conductive film 145, and the second conductive film is etched.

[0099]

Next, in a manner similar to the step illustrated in FIG. 2D, the oxide

25 semiconductor layer 144 is formed over the insulating layers 143a and 143b and the substrate 100 (see FIG. 3D). The formed oxide semiconductor layer 144 is in contact with the second conductive layers 145a and 145b in its channel formation region. Further, the oxide semiconductor layer 144 is desirably subjected to heat treatment (first heat treatment).

30 [0100]

Then, in a manner similar to the step illustrated in FIG. 2E, the gate insulating layer 146 is formed (see FIG. 3E). After forming the gate insulating layer 146, heat

treatment (second heat treatment) is desirably performed.

[0101]

Then, in a manner similar to the step illustrated in FIG. 2F, the gate electrode 148 is formed over the gate insulating layer 146 in a region overlapping with the channel formation region of the oxide semiconductor layer 144 (see FIG. 3F).

[0102]

Through the above steps, the transistor 180 including the oxide semiconductor layer 144 is completed.

[0103]

The transistors 160, 170, 180, and 190 illustrated in this embodiment each include the source electrode and the drain electrode in which the first electrode and the second electrode are stacked. In each of the transistors, the second conductive layers 145a and 145b have regions which extend in the channel length direction from the end portions of the first conductive layers 142a and 142b. Accordingly, steps on end portions of the source electrode and the drain electrode can be made gradual. Thus, it is possible to improve the coverage of the oxide semiconductor layer 144 and the gate insulating layer 146 and to prevent occurrence of poor connections.

[0104]

In each of the transistors 160, 170, 180, and 190 illustrated in this embodiment, in the source electrode or the drain electrode, the vicinity of the region in contact with the channel formation region can be a high-resistance region, whereby an electric field between the source electrode and the drain electrode can be relieved. Thus, a short-channel effect in accordance with a reduction in a transistor size can be controlled.

[0105]

As described above, according to an embodiment of the disclosed invention, a problem due to miniaturization can be resolved. As a result, the size of the transistor can be sufficiently reduced. By sufficiently reducing the size of the transistor, an area of a semiconductor device including the transistor is decreased, and the number of semiconductor devices obtained from one substrate is increased. Accordingly, manufacturing costs of the semiconductor device can be reduced. Further, since the semiconductor device is downsized, the semiconductor device which is substantially the same in size with increased function can be realized. Furthermore, effects of

high-speed operation, low power consumption, and the like of a transistor can be obtained in accordance with a reduction in channel length. Thus, miniaturization of a transistor including an oxide semiconductor can be achieved according to an embodiment of the disclosed invention, and various effects accompanied with the miniaturization can be obtained.

[0106]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0107]

(Embodiment 2)

In this embodiment, a structure and a manufacturing process of a semiconductor device according to one embodiment of the disclosed invention, which are different from those of Embodiment 1, will be described with reference to FIG. 4 and FIGS. 5A to 5F.

[0108]

<Example of Structure of Semiconductor Device>

A transistor 280 illustrated in FIG. 4 is an example of a structure of a semiconductor device. The order of stacking of the transistor 280 corresponds to that of the transistor 180 illustrated in FIG. 1C. The difference between the transistor 280 and the transistor 180 is that a sidewall insulating layer 252a is provided over the second conductive layer 245a in a region which extends in a channel length direction from an end portion of the first conductive layer 242a and a sidewall insulating layer 252b is provided over the second conductive layer 245b in a region which extends in a channel length direction from an end portion of the first conductive layer 242b.

[0109]

The transistor 280 illustrated in FIG. 4 includes, over a substrate 200, a source electrode in which the second conductive layer 245a and the first conductive layer 242a are stacked in this order; a drain electrode in which the second conductive layer 245b and the first conductive layer 242b are stacked in this order; an insulating layer 243a provided over the source electrode; an insulating layer 243b provided over the drain electrode; an oxide semiconductor layer 244 provided over the insulating layers 243a

and 243b; a gate insulating layer 246 provided over the oxide semiconductor layer 244; and a gate electrode 248 provided over the gate insulating layer 246.

[0110]

In the transistor 280 illustrated in FIG. 4, the second conductive layer 245a has the region which extends in the channel length direction from the end portion of the first conductive layer 242a, and the second conductive layer 245a and at least a channel formation region of the oxide semiconductor layer 244 are in contact with each other. Further, the second conductive layer 245b has the region which extends in the channel length direction from the end portion of the first conductive layer 242b, and the second conductive layer 245b and at least the channel formation region of the oxide semiconductor layer 244 are in contact with each other.

[0111]

More specifically, the second conductive layer 245a has the region which extends in the channel length direction (the flowing direction of carriers) from the end portion of the first conductive layer 242a toward the drain electrode. Further, the second conductive layer 245b has the region which extends in the channel length direction from the end portion of the first conductive layer 242b toward the source electrode.

[0112]

Further, the transistor 280 illustrated in FIG. 4 has the sidewall insulating layer 252a over the second conductive layer 245a in the region which extends in the channel length direction from the end portion of the first conductive layer 242a and the sidewall insulating layer 252b over the second conductive layer 245b in the region which extends in the channel length direction from the end portion of the first conductive layer 242b. The sidewall insulating layer 252a is provided so as to be in contact with the oxide semiconductor layer 244 (at least the channel formation region thereof), the second conductive layer 245a, the first conductive layer 242a, and the insulating layer 243a. Further, in the sidewall insulating layer 252a, part of a region in contact with the oxide semiconductor layer 244 has a curved shape. The sidewall insulating layer 252b is provided so as to be in contact with the oxide semiconductor layer 244 (at least the channel formation region thereof), the second conductive layer 245b, the first conductive layer 242b, and the insulating layer 243b. Further, in the sidewall

insulating layer 252b, part of a region in contact with the oxide semiconductor layer 244 has a curved shape.

[0113]

<Example of Manufacturing Process of Transistor 280>

5 Next, an example of a manufacturing process of the transistor 280 will be described with reference to FIG. 5A to 5F.

[0114]

First, the second conductive film 245 is formed over the substrate 200. Next, the first conductive film 242 is formed over the second conductive film 245, and the 10 insulating film 243 is formed over the first conductive film 242 (see FIG. 5A).

[0115]

Here, a material similar to that of the substrate 100 described in Embodiment 1 can be used for the substrate 200. Further, the second conductive film 245 can be formed using a material and a method similar to those of the second conductive film 15 145 described in Embodiment 1. Furthermore, the first conductive film 242 can be formed using a material and a method similar to those of the first conductive film described in Embodiment 1. Embodiment 1 can be referred to for the details.

[0116]

However, materials which can obtain etching selectivity are used for the first 20 conductive film 242 and the second conductive film 245. In this embodiment, a titanium nitride film is formed as the second conductive film 245 and a tungsten film or a molybdenum film is formed as the first conductive film 242.

[0117]

Next, a mask is formed over the insulating film 243, and the insulating film 25 243 is etched using the mask, whereby the insulating layers 243a and 243b are formed. For the etching of the insulating film 243, either wet etching or dry etching can be used. Alternatively, wet etching and dry etching may be used in combination. The etching conditions (e.g., an etching gas or an etchant, etching time, and temperature) are set as appropriate depending on the material so that the insulating film can be etched into a 30 desired shape. However, it is preferable to use dry etching for microfabrication of a channel length (L) of the transistor. As an etching gas used for dry etching, for example, a gas containing fluorine such as, sulfur hexafluoride (SF_6), nitrogen

trifluoride (NF_3), or trifluoromethane (CHF_3)); or a mixed gas of carbon tetrafluoride (CF_4) and hydrogen can be used. A rare gas (heliun (He), Argon (Ar), or xenon (Xe)), carbon monoxide, carbon dioxide, or the like may be added to the etching gas for dry etching.

5 [0118]

Next, the first conductive film 242 is etched using the mask used for etching of the insulating film 243, whereby the first conductive layers 242a and 242b are formed (see FIG. 5B). Note that when the first conductive film 242 is etched, a material which can obtain etching selectivity with respect to the second conductive film 245 is used.
10 Note that the mask may be removed before etching the first conductive film 242, and the first conductive film 242 may be etched using the insulating layers 243a and 243b as masks.

[0119]

In this embodiment, as an etching gas for etching the first conductive film 242,
15 a mixed gas of carbon tetrafluoride (CF_4), chlorine (Cl_2), and oxygen (O_2), a mixed gas of carbon tetrafluoride (CF_4) and oxygen (O_2), a mixed gas of sulfur hexafluoride (SF_6) chlorine (Cl_2), and oxygen (O_2), or a mixed gas of sulfur hexafluoride (SF_6) and oxygen (O_2), is used.

[0120]

20 By providing the insulating layers 243a and 243b, contact regions (contact areas and the like) between each of the source electrode and the drain electrode to be formed later and the oxide semiconductor layer can be controlled easily. That is, the resistance of the source electrode and the drain electrode can be easily controlled, and the short-channel effect can be effectively controlled. Furthermore, by providing the
25 insulating layers 243a and 243b, parasitic capacitance between the gate electrode to be formed later and each of the source electrode and the drain electrode can be reduced.

[0121]

Then, an insulating film 252 is formed so as to cover the insulating layers 243a, 243b, and the exposed second conductive film 245 (see FIG. 5C). The insulating film
30 252 can be formed by a CVD method, or a sputtering method. The insulating film 252 preferably contains silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide, or the like. The insulating film 252 may have a single-layer structure or a stacked

structure.

[0122]

Then, the sidewall insulating layers 252a and 252b are formed over the region where the second conductive film 245 is exposed (a region between the first conductive
5 layer 242a and the first conductive layer 242b) (see FIG. 5D). The insulating film 252 is subjected to highly anisotropic etching treatment, whereby the sidewall insulating layers 252a and 252b can be formed in a self-aligned manner. Here, as a highly anisotropic etching process, dry etching is preferable. As an example of the etching gas, a gas containing fluorine such as, trifluoromethane (CHF_3) can be used, or a rare
10 gas such as heliun (He) or Argon (Ar) may be added. In addition, as the dry etching, a reactive ion etching (RIE) method in which high-frequency voltage is applied to a substrate, is preferably used.

[0123]

Next, the second conductive film 245 is selectively etched using the sidewall
15 insulating layers 252a and 252b as masks (see FIG. 5E). Through this etching process, the source electrode in which the second conductive layer 245a and the first conductive layer 242a are stacked and the drain electrode in which the second conductive layer 245b and the first conductive layer 242b are stacked are formed. The etching of the second conductive film 245 can be performed in a manner similar to that described in
20 Embodiment 1 with reference to FIG. 2C except that the sidewall insulating layers 252a and 252b are used as masks.

[0124]

Note that the channel length (L) of the transistor 280 is determined by the distance between the lower end portion of the second conductive layer 245a and the
25 lower end portion of the second conductive layer 245b. The channel length (L) depends on the application of the transistor 280; which can be, for example, 10 nm to 1000 nm, preferably, 20 nm to 400 nm.

[0125]

Note that in the manufacturing process of the transistor described in this
30 embodiment, the second conductive film 245 is etched using the sidewall insulating layer 252a or the sidewall insulating layer 252b. Therefore, in the second conductive layer 245a, the length (L_S) in a channel length direction in the region which extends in

the channel length direction from the end portion of the first conductive layer 242a and the length in a channel length direction in the bottom face of the sidewall insulating layer 252a are almost the same. At the same time, in the second conductive layer 245b, the length (L_D) in a channel length direction in the region which extends in the channel
5 length direction from the end portion of the first conductive layer 242b and the length in the channel length direction in the bottom face of the sidewall insulating layer 252b are almost the same. Since the sidewall insulating layers 252a and 252b are formed in a self-aligned manner by etching treatment on the insulating film 252, the (L_S) or (L_D) is determined in accordance with the film thickness of the insulating film 252. Thus, by
10 controlling the thickness of the insulating film 252, the channel length (L) of the transistor 280 can be adjusted finely. For example, the channel length (L) of the transistor 280 can be adjusted more minutely than the minimum processing dimension of a light-exposure apparatus for forming a mask. Thus, the thickness of the insulating film 252 is determined in accordance with the desired channel length (L) of the
15 transistor 280, resolution of the light-exposure apparatus used for processing of the first conductive layers 242a and 242b, and the like.

[0126]

Next, the oxide semiconductor layer 244 is formed to cover the insulating layers 243a and 243b and the sidewall insulating layers 252a and 252b and to be in
20 contact with the second conductive layers 245a and 245b, and the gate insulating layer 246 is formed over the oxide semiconductor layer 244. Then, the gate electrode 248 is formed over the gate insulating layer 246 in a region overlapping with the channel formation region of the transistor 280 (see FIG. 5F).

[0127]

25 The oxide semiconductor layer 244 can be formed using a material and a method similar to those of the oxide semiconductor layer 144 illustrated in Embodiment 1. Further, the oxide semiconductor layer 244 is desirably subjected to heat treatment (first heat treatment). Embodiment 1 can be referred to for the details.

[0128]

30 The gate insulating layer 246 can be formed using a material and a method similar to those of the gate insulating layer 146 illustrated in Embodiment 1. Further, the formed gate insulating layer 246 is desirably subjected to heat treatment (second

heat treatment) in an inert gas atmosphere or an oxygen atmosphere. Embodiment 1 can be referred to for the details.

[0129]

The gate electrode 248 can be formed in such a manner that a conductive film is formed over the gate insulating layer 246 and then etched selectively. The gate electrode 248 can be formed using a material and a method similar to those of the gate electrode 148 illustrated in Embodiment 1.

[0130]

Note that the source electrode of the transistor 280 is in contact with the oxide semiconductor layer 244 at an end portion of the region which extends in the channel length direction from an end portion of the first conductive layer 242a in the second conductive layer 245a. On the other hand, the drain electrode of the transistor 280 is in contact with the oxide semiconductor layer 244 at an end portion of the region which extends in the channel length direction from an end portion of the first conductive layer 242b in the second conductive layer 245b. As described, the source electrode and the drain electrode of the transistor 280 is in contact with the oxide semiconductor layer 244 at the end portions of the second conductive layers 245a and 245b which have smaller film thickness than the first conductive layers 242a and 242b, whereby the contact area thereof can be reduced, and contact resistance at an contact interface can be increased. Accordingly, even if the channel length (L) of the transistor 280 is shortened, electric field between the source electrode and the drain electrode can be relieved, and a short-channel effect can be controlled. In addition, when the second conductive layer is formed using a higher resistance material than the first conductive layer, contact resistance can be increased effectively, which is preferable. Note that a technical idea of the disclosed invention is to form a high-resistance region in the source electrode and the drain electrode; thus, the source electrode and the drain electrode does not need to be exactly in contact with the oxide semiconductor layer only at the end portions of the second conductive layers 245a and 245b.

[0131]

Accordingly, the transistor 280 including the oxide semiconductor layer 244 can be manufactured.

[0132]

The channel length (*L*) of the transistor 280 described in this embodiment can be adjusted finely by the film thickness of the insulating film 252 for forming the sidewall insulating layers 252a and 252b. Therefore, the film thickness of the insulating film 252 is set as appropriate, the channel length (*L*) of the transistor 280 is
5 shortened, and thus a semiconductor device can be easily miniaturized.

[0133]

In the transistor 280 described in this embodiment, the sidewall insulating layer 252a is provided over the region which extends in the channel length direction from the end portion of the first conductive layer 242a in the second conductive layer 245a, and
10 the sidewall insulating layer 252b is provided over the region which extends in the channel length direction from the end portion of the first conductive layer 242b in the second conductive layer 245b. Accordingly, coverage of the oxide semiconductor layer 244 and the gate insulating layer 246 are improved, and occurrence of poor connections can be prevented.

15 [0134]

Further, the transistor 280 described in this embodiment includes the region which extends in the channel length direction from the end portion of the first conductive layer 242a in the second conductive layer 245a, and the region which extends in the channel length direction from the end portion of the first conductive layer
20 242b in the second conductive layer 245b, and the vicinity of the regions in contact with the channel formation region of the oxide semiconductor layer 244 is made to be high-resistance region. Therefore, an electric field between the source electrode and the drain electrode can be relieved, and a short-channel effect such as a decrease in a threshold voltage can be controlled.

25 [0135]

As described above, according to an embodiment of the disclosed invention, a problem due to miniaturization can be resolved. As a result, the size of the transistor can be sufficiently reduced. By sufficiently reducing the size of the transistor, an area of a semiconductor device including the transistor is decreased, and the number of
30 semiconductor devices obtained from one substrate is increased. Accordingly, manufacturing costs of the semiconductor device can be reduced. Further, since the semiconductor device is downsized, the semiconductor device which is substantially the

same in size with increased function can be realized. Furthermore, effects of high-speed operation, low power consumption, and the like of a transistor can be obtained in accordance with a reduction in channel length. Thus, miniaturization of a transistor including an oxide semiconductor can be achieved according to one
5 embodiment of the disclosed invention, and various effects accompanied with the miniaturization can be obtained.

[0136]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in
10 the other embodiments.

[0137]

(Embodiment 3)

In this embodiment, application examples of a semiconductor device according to one embodiment of the disclosed invention will be described with reference to FIGS.
15 6A-1, 6A-2, and 6B. Here, an example of a memory device will be described. Note that in a circuit diagram, "OS" is written in order to indicate that a transistor includes an oxide semiconductor.

[0138]

In the semiconductor device illustrated in FIG. 6A-1, a first wiring (a 1st line)
20 is electrically connected to a source electrode of a transistor 300. A second wiring (a 2nd line) is electrically connected to a drain electrode of the transistor 300. Further, a third wiring (a 3rd line) is electrically connected to one of a source electrode and a drain electrode of a transistor 310, and a fourth wiring (4th Line) is electrically connected to a gate electrode of the transistor 310. A gate electrode of the transistor 300 and the other
25 of the source electrode and the drain electrode of the transistor 310 are electrically connected to one of electrodes of a capacitor 320. A fifth wiring (a 5th line) is electrically connected to the other of the electrodes of the capacitor 320.

[0139]

Here, a transistor including an oxide semiconductor described in Embodiments
30 1 and 2 are used for the transistor 310. A transistor including an oxide semiconductor has a characteristic of a significantly small off current. For that reason, a potential of the gate electrode of the transistor 300 can be held for an extremely long time by turning

off the transistor 310. Provision of the capacitor 320 facilitates holding of charge given to the gate electrode of the transistor 300 and reading of stored data.

[0140]

Note that there is no particular limitation on the transistor 300. In terms of
5 increasing the speed of reading data, it is preferable to use, for example, a transistor with high switching rate such as a transistor formed using single crystal silicon.

[0141]

Further, as illustrated in FIG. 6B, a structure in which the capacitor 320 is not provided may also be employed.

10 [0142]

The semiconductor device in FIG. 6A-1 utilizes the advantage that the potential of the gate electrode of the transistor 300 can be held, whereby writing, holding, and reading of data can be performed as described below.

[0143]

15 Firstly, writing and holding of data will be described. First, the potential of the fourth wiring is set to a potential at which the transistor 310 is turned on, so that the transistor 310 is turned on. Accordingly, the potential of the third wiring is supplied to the gate electrode of the transistor 300 and the capacitor 320. That is, predetermined charge is given to the gate electrode of the transistor 300 (writing). Here, one of
20 charges for supply of two different potentials (hereinafter, a charge for supply of a low potential is referred to as a charge Q_L and a charge for supply of a high potential is referred to as a charge Q_H) is given to the gate electrode of the transistor 300. Note that charges giving three or more different potentials may be applied to improve a storage capacitor. After that, the potential of the fourth wiring is set to a potential at
25 which the transistor 310 is turned off, so that the transistor 310 is turned off. Thus, the charge given to the gate electrode of the transistor 300 is held (storing).

[0144]

Since the off current of the transistor 310 is significantly small, the charge of the gate electrode of the transistor 300 is retained for a long time.

30 [0145]

Secondly, reading of data will be described. By supplying an appropriate potential (read-out potential) to the fifth wiring while a predetermined potential

(constant potential) is supplied to the first wiring, the potential of the second wiring varies depending on the amount of charge held in the gate electrode of the transistor 300. This is because in general, when the transistor 300 is an n-channel transistor, an apparent threshold voltage V_{th_H} in the case where Q_H is given to the gate electrode of the transistor 300 is lower than an apparent threshold voltage V_{th_L} in the case where Q_L is given to the gate electrode of the transistor 300. Here, an apparent threshold voltage refers to the potential of the fifth wiring, which is needed to turn on the transistor 300. Thus, the potential of the fifth wiring is set to a potential V_0 intermediate between V_{th_H} and V_{th_L}, whereby charge given to the gate electrode of the transistor 300 can be determined. For example, in the case where Q_H is given in writing, when the potential of the fifth wiring is set to V_0 ($> V_{th_H}$), the transistor 300 is turned on. In the case where Q_L is given in writing, even when the potential of the fifth wiring is set to V_0 ($< V_{th_L}$), the transistor 300 remains in an off state. Therefore, the stored data can be read by the potential of the second wiring.

[0146]

Note that in the case where memory cells are arrayed to be used, only data of desired memory cells is needed to be read. Thus, in order that data of predetermined memory cells is read and data of the other memory cells is not read, in the case where the transistors 300 are connected in parallel between the memory cells, a potential which allows the transistor 300 to be turned off regardless of a state of the gate electrode, that is, a potential lower than V_{th_H} may be applied to the fifth wiring of the memory cells whose data is not to be read. Further, in the case where transistors 300 are connected in series between the memory cells, a potential which allows the transistor 300 to be turned on regardless of a state of the gate electrode, that is, a potential higher than V_{th_L} may be applied to the fifth wiring of the memory cells whose data is not to be read.

[0147]

Then, rewriting of data will be described. Rewriting of data is performed in a manner similar to that of the writing and holding of data. That is, the potential of the fourth wiring is set to a potential at which the transistor 310 is turned on, so that the transistor 310 is turned on. Accordingly, the potential of the third wiring (potential

related to new data) is supplied to the gate electrode of the transistor 300 and the capacitor 320. After that, the potential of the fourth wiring is set to a potential which allows the transistor 310 to be turned off, whereby the transistor 310 is turned off. Accordingly, charge related to new data is given to the gate electrode of the transistor 5 300.

[0148]

In the semiconductor device according to the invention disclosed herein, data can be directly rewritten by another writing of data as described above. Therefore, extracting of charge from a floating gate with the use of a high voltage needed in a flash 10 memory or the like is not necessary and thus, reduction in operation speed, which is attributed to erasing operation, can be suppressed. In other words, high-speed operation of the semiconductor device can be realized.

[0149]

The source electrode or the drain electrode of the transistor 310 is electrically 15 connected to the gate electrode of the transistor 300, thereby having an effect similar to that of a floating gate of a floating gate transistor used for a nonvolatile memory element. Therefore, a portion in the drawing where the source electrode or the drain electrode of the transistor 310 is electrically connected to the gate electrode of the transistor 300 is called a floating gate portion FG in some cases. When the transistor 20 310 is off, the floating gate portion FG can be regarded as being embedded in an insulator and thus charge is held in the floating gate portion FG. The amount of off current of the transistor 310 including an oxide semiconductor is smaller than or equal to one hundred thousandth of the amount of off current of a transistor including a silicon semiconductor; thus, lost of the charge accumulated in the floating gate portion FG due 25 to a leakage current of the transistor 310 is negligible. That is, with the transistor 310 including an oxide semiconductor, a nonvolatile memory device which can store data without being supplied with power can be realized.

[0150]

For example, when the off current of the transistor 310 is 10 zA (1 zA 30 (zeptoampere) is 1×10^{-21} A) or less at room temperature and the capacitance value of the capacitor 320 is approximately 10 fF, data can be stored for 10^4 seconds or longer. It is needless to say that the storage time depends on transistor characteristics and the

capacitance value.

[0151]

Further, in that case, the problem of deterioration of a gate insulating film (tunnel insulating film), which is pointed out in a conventional floating gate transistor, does not exist. That is to say, the problem of deterioration of a gate insulating film when an electron is injected into a floating gate, which has been traditionally regarded as a problem, can be neglected. This means that there is no limit on the number of times of writing in principle. Furthermore, a high voltage needed for writing or erasing in a conventional floating gate transistor is not necessary.

[0152]

The components such as transistors in the semiconductor device in FIG. 6A-1 can be regarded as including a resistor and a capacitor as shown in FIG. 6A-2. That is, in FIG. 6A-2, the transistor 300 and the capacitor 320 are each regarded as including a resistor and a capacitor. R1 and C1 denote the resistance value and the capacitance value of the capacitor 320, respectively. The resistance value R1 corresponds to the resistance value which depends on an insulating layer included in the capacitor 320. R2 and C2 denote the resistance value and the capacitance value of the transistor 300, respectively. The resistance value R2 corresponds to the resistance value which depends on a gate insulating layer at the time when the transistor 300 is on. The capacitance value C2 corresponds to the capacitance value of so-called gate capacitance (capacitance formed between the gate electrode and each of the source electrode and the drain electrode and capacitance formed between the gate electrode and the channel formation region).

[0153]

A charge holding period (also referred to as a data holding period) is determined mainly by off current of the transistor 310 under the conditions that gate leakage of the transistor 310 is sufficiently small and that $R1 \geq ROS$ (R1 is ROS or more) and $R2 \geq ROS$ (R2 is ROS or more) are satisfied, where the resistance value (also referred to as effective resistance) between the source electrode and the drain electrode in the case where the transistor 310 is off is ROS.

[0154]

On the other hand, when the conditions are not met, it is difficult to sufficiently secure the holding period even if the off current of the transistor 310 is small enough. This is because a leakage current other than the off current of the transistor 310 (e.g., a leakage current generated between the source electrode and the gate electrode) is large. Thus, it can be said that the semiconductor device disclosed in this embodiment desirably satisfies the above relation.

[0155]

It is desirable that C1 and C2 satisfy $C1 \geq C2$ (C1 is C2 or more). If C1 is large, variation in potential of the fifth wiring can be suppressed when the potential of the floating gate portion FG is controlled by the fifth wiring (e.g., at the time of reading).

[0156]

When the above relation is satisfied, a more preferable semiconductor device can be realized. Note that R1 and R2 are controlled by the gate insulating layer of the transistor 300 and the insulating layer of the capacitor 320. The same relation is applied to C1 and C2. Therefore, the material, the thickness, and the like of the gate insulating layer are desirably set as appropriate to satisfy the above relation.

[0157]

In the semiconductor device described in this embodiment, the floating gate portion FG has an effect similar to a floating gate of a floating gate transistor of a flash memory or the like, but the floating gate portion FG of this embodiment has a feature which is essentially different from that of the floating gate of the flash memory or the like. In the case of a flash memory, since a voltage applied to a control gate is high, it is necessary to keep a proper distance between cells in order to prevent the potential from affecting a floating gate of the adjacent cell. This is one of inhibiting factors for high integration of the semiconductor device. The factor is attributed to a basic principle of a flash memory, in which a tunneling current flows in applying a high electric field.

[0158]

Further, because of the above principle of a flash memory, deterioration of an insulating film proceeds and thus another problem of the limit on the number of times of rewriting (approximately 10^4 to 10^5 times) occurs.

[0159]

The semiconductor device according to the disclosed invention is operated by switching of a transistor including an oxide semiconductor and does not use the above-described principle of charge injection by a tunneling current. That is, a high
5 electrical field for charge injection is not necessary unlike a flash memory. Accordingly, it is not necessary to consider an influence of a high electric field from a control gate on an adjacent cell, which facilitates high integration.

[0160]

Further, charge injection by a tunneling current is not utilized, which means
10 that there is no causes for deterioration of a memory cell. In other words, the semiconductor device according to the disclosed invention has higher durability and reliability than a flash memory.

[0161]

In addition, it is also advantageous that a high electric field is unnecessary and
15 a large peripheral circuit (such as a booster circuit) is unnecessary as compared to a flash memory.

[0162]

In the case where the dielectric constant $\varepsilon r1$ of the insulating layer included in the capacitor 320 is different from the dielectric constant $\varepsilon r2$ of the insulating layer
20 included in a gate capacitor of the transistor 300, it is easy to satisfy $C1 \geq C2$ (C1 is C2 or greater) while $2 \cdot S2 \geq S1$ ($2 \cdot S2$ is S1 or more) (desirably, $S2 \geq S1$ (S is S1 or more)) is satisfied where S1 is the area of the insulating layer included in the capacitor 320 and S2 is the area of the insulating layer included in a gate capacitor of the transistor 300. That is, it is easy to satisfy that C1 is C2 or greater while reducing S1. Specifically, for
25 example, a film formed of a high-k material such as hafnium oxide or a stack of a film formed of a high-k material such as hafnium oxide and a film formed of an oxide semiconductor is used for the insulating layer included in the capacitor 320 so that $\varepsilon r1$ can be set to 10 or more, preferably 15 or more, and silicon oxide is used for the insulating layer included in a gate capacitor of the transistor 300 so that $\varepsilon r2$ can be set to
30 3 to 4.

[0163]

Combination of such structures enables higher integration of the semiconductor device according to the disclosed invention.

[0164]

Note that an n-channel transistor in which electrons are majority carriers is used in the above description; it is needless to say that a p-channel transistor in which holes are majority carriers can be used instead of the n-channel transistor.

[0165]

As described above, a semiconductor device according to an embodiment of the disclosed invention has a nonvolatile memory cell including a writing transistor where a leakage current (off current) between a source electrode and a drain electrode is small in an off state, a reading transistor formed of a semiconductor material different from that of the writing transistor, and a capacitor.

[0166]

The off current of the writing transistor is preferably 100 zA (1×10^{-19} A) or less, more preferably 10 zA (1×10^{-20} A) or less, still more preferably 1 zA (1×10^{-21} A) or less at a temperature at which the memory cell is used (e.g., 25 °C). Such small off-state current is difficult to obtain with a general silicon semiconductor, but can be achieved by a transistor which is obtained by processing an oxide semiconductor under an appropriate condition. Therefore, a transistor including an oxide semiconductor is preferably used as the writing transistor.

[0167]

In addition, a transistor including an oxide semiconductor has a small subthreshold swing (S value), so that the switching rate can be sufficiently high even if mobility is comparatively low. Therefore, by using the transistor as the writing transistor, rising of a writing pulse given to the floating gate portion FG can be very sharp. Further, an off current is small and thus, the amount of charge held in the floating gate portion FG can be reduced. That is, by using a transistor including an oxide semiconductor, rewriting of data can be performed at high speed.

[0168]

Although there is no limitation on the off-state current of the reading transistor, a transistor that operates at high speed is preferably used as the reading transistor in

order to increase the readout speed. For example, a transistor with a switching rate of 1 nano second or lower is preferably used as the reading transistor.

[0169]

Data is written to the memory cell by turning on the writing transistor so that a potential is supplied to the floating gate portion FG where one of a source electrode and a drain electrode of the writing transistor, one of electrodes of the capacitor, and a gate electrode of the reading transistor are electrically connected, and then turning off the writing transistor so that the predetermined amount of charge is held in the floating gate portion FG. Here, the off current of the writing transistor is very small; thus, the charge supplied to the floating gate portion FG is held for a long time. When an off current is, for example, substantially 0, refresh operation needed for a conventional DRAM can be unnecessary or the frequency of refresh operation can be significantly low (for example, about once a month or a year). Accordingly, power consumption of a semiconductor device can be reduced sufficiently.

[0170]

Further, data can be rewritten directly by overwriting of new data to the memory cell. For that reason, erasing operation which is necessary for a flash memory or the like is not needed, so that a reduction in operation speed because of erasing operation can be prevented. In other words, high-speed operation of the semiconductor device can be realized. Moreover, a high voltage necessary for a conventional floating gate transistor to write and erase data is unnecessary; thus, power consumption of the semiconductor device can be further reduced. The highest voltage applied to the memory cell according to this embodiment (the difference between the highest potential and the lowest potential applied to respective terminals of the memory cell at the same time) can be 5 V or lower or 3 V or lower, preferably, 3V or lower in each memory cell in the case where data of two stages (one bit) is written.

[0171]

The memory cell provided in the semiconductor device according to the disclosed invention may include at least the writing transistor, the reading transistor, and the capacitor. Further, the memory cell can operate even when the area of the capacitor is small. Accordingly, the area of each memory cell can be sufficiently small as compared to an SRAM which requires six transistors in each memory cell, for

example; thus, the memory cells can be arranged in a semiconductor device at high density.

[0172]

In a conventional floating gate transistor, charge travels in a gate insulating
5 film (tunnel insulating film) during writing operation, so that deterioration of the gate insulating film (tunnel insulating film) cannot be avoided. In contrast, in the memory cell according to an embodiment of the present invention, data is written by switching operation of a writing transistor; therefore, there is no deterioration of a gate insulating film. This means that there is no limit on the number of times of writing in principle
10 and writing durability is very high. For example, in the memory cell according to one embodiment of the present invention, the current-voltage characteristic is not degraded even after data is written 1×10^9 or more times (one billion or more times).

[0173]

Further, in the case of using a transistor including an oxide semiconductor as
15 the writing transistor of the memory cell, the current-voltage characteristic of the memory cell is not degraded even at, for example, a high temperature of 150 °C because an oxide semiconductor generally has a wide energy gap (e.g., 3.0 to 3.5 eV in the case of an In-Ga-Zn-O-based oxide semiconductor) and extremely few thermally excited carriers.

20 [0174]

As a result of intensive research, the present inventors have succeeded in finding for the first time that a transistor including an oxide semiconductor has excellent characteristics in that the characteristics do not deteriorate even at a high temperature of 150 °C and off current is less than or equal to 100 zA, which is extremely small.
25 According to this embodiment, a semiconductor device having a novel feature by using a transistor having such excellent characteristics as the writing transistor of the memory cell is provided.

[0175]

According to an embodiment of the disclosed invention, a transistor including
30 an oxide semiconductor can achieves miniaturization while defects are suppressed and favorable characteristics are maintained. By using such a transistor, an excellent

memory device as described above can be highly-integrated.

[0176]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in
5 the other embodiments.

[0177]

(Embodiment 4)

In this embodiment, application examples of a semiconductor device according to one embodiment of the disclosed invention will be described with reference to FIGS.
10 7A and 7B, and FIGS. 8A to 8C.

[0178]

FIGS. 7A and 7B are circuit diagrams of semiconductor devices each including a plurality of semiconductor devices (hereinafter also referred to as memory cells 400) illustrated in FIG. 6A-1. FIG. 7A is a circuit diagram of a so-called NAND
15 semiconductor device in which the memory cells 400 are connected in series, and FIG. 7B is a circuit diagram of a so-called NOR semiconductor device in which the memory cells 400 are connected in parallel.

[0179]

The semiconductor device in FIG. 7A includes a source line SL, a bit line BL, a
20 first signal line S1, m second signal lines S2, m word lines WL, and a plurality of memory cells 400 (1, 1) to 400 (m, 1) which is arranged in m (rows) (in a vertical direction) × 1 (a column) (in a horizontal direction). Note that in FIG. 7A, one source line SL and one bit line BL are provided in the semiconductor device; however, one embodiment of the disclosed invention is not limited to this. n source lines SL and n
25 bit lines BL may be provided so that a memory cell array where the memory cells are arranged in a matrix of m (rows) (in a vertical direction) × n (columns) (in a horizontal direction) is formed.

[0180]

In each of the memory cells 400, the gate electrode of the transistor 300, the
30 one of the source electrode and the drain electrode of the transistor 310, and the one of the electrodes of the capacitor 320 are electrically connected to one another. In

addition, the first signal line S1 and the other of the source electrode and the drain electrode of the transistor 310 are electrically connected to each other, and the second signal line S2 and the gate electrode of the transistor 310 are electrically connected to each other. The word line WL and the other of the electrodes of the capacitor 320 are
5 electrically connected to each other.

[0181]

Further, the source electrode of the transistor 300 in the memory cell 400 is electrically connected to the drain electrode of the transistor 300 in one adjacent memory cell 400. The drain electrode of the transistor 300 included in the memory
10 cell 400 is electrically connected to the source electrode of the transistor 300 in another adjacent memory cell 400. Note that the drain electrode of the transistor 300 included in the memory cell 400 of the plurality of memory cells connected in series, which is provided at one of ends, is electrically connected to the bit line. The source electrode of the transistor 300 included in the memory cell 400 of the plurality of memory cells
15 connected in series, which is provided at the other end, is electrically connected to the source line.

[0182]

In the semiconductor device in FIG. 7A, writing operation and reading operation are performed for each row. The writing operation is performed as follows.
20 A potential at which the transistor 310 is turned on is applied to the second signal line S2 of a row where writing is to be performed, whereby the transistor 310 of the row where writing is to be performed is turned on. Accordingly, a potential of the first signal line S1 is applied to the gate electrode of the transistor 300 of the specified row, whereby predetermined charge is given to the gate electrode of the transistor 300.
25 Thus, data can be written to the memory cell of the specified row.

[0183]

The reading operation is performed as follows. First, a potential at which the transistor 300 is turned on regardless of the charge in the gate electrode of the transistor 300 is applied to the word lines WL of rows other than a row where reading is to be
30 performed, whereby the transistors 300 of the rows other than the row where reading is to be performed are turned on. Then, a potential (a read-out potential) at which an on state or an off state of the transistor 300 is determined depending on the charge in the

gate electrode of the transistor 300 is applied to the word line WL of the row where reading is performed. After that, a constant potential is applied to the source line SL and a read-out circuit (not illustrated) connected to the bit line BL is operated. Here, since the plurality of transistors 300 between the source line SL and the bit line BL are
5 in an on state except the transistors 300 of the row where reading is performed, conductance between the source line SL and the bit line BL is determined by the state of the transistor 300 (on state or off state) of the row where reading is performed. Since the conductance of the transistors varies depending on the charge in the gate electrode of the transistor 300, a potential of the bit line BL varies accordingly. By reading the
10 potential of the bit line BL with the read-out circuit, data can be read out from the memory cells of the specified row.

[0184]

The semiconductor device illustrated in FIG. 7B includes n source lines SL, n bit lines BL, n first signal lines S1, m second signal lines S2, m word lines WL, and a
15 memory cell array 410 including the plurality of memory cells 400 (1, 1) to 400 (m, n) which are arranged in a matrix of m (rows) (in a vertical direction) × n (columns) (in a horizontal direction). The gate electrode of the transistor 300, the one of the source electrode and drain electrode of the transistor 310, and the one electrode of the capacitor 320 are electrically connected to one another. In addition, the source line SL and the
20 source electrode of the transistor 300 are electrically connected to each other, and the bit line BL and the drain electrode of the transistor 300 are electrically connected to each other. In addition, the first signal line S1 and the other of the source electrode and drain electrode of the transistor 310 are electrically connected to each other, and the second signal line S2 and the gate electrode of the transistor 310 are electrically
25 connected to each other. The word line WL and the other electrode of the capacitor 320 are electrically connected.

[0185]

In the semiconductor device in FIG. 7B, writing operation and reading operation are performed in each row. The writing operation is performed in a manner
30 similar to that of the semiconductor device in FIG. 7A. The reading operation is performed as follows. First, a potential at which the transistor 300 is turned off regardless of charge given to the gate electrode thereof is supplied to the word lines WL

of the rows other than the row where reading is to be performed, whereby the transistors 300 of the rows other than the row where reading is to be performed are turned off. Then, a potential (a read-out potential) at which an on state or an off state of the transistor 300 is determined depending on charge in the gate electrode of the transistor 300 is supplied to the word line WL of the row where reading is to be performed. After that, a constant potential is supplied to the source line SL so that a read-out circuit (not illustrated) connected to the bit line BL is operated. Here, conductance between the source line SL and the bit line BL is determined by the state of the transistor 300 of the row where reading is performed. That is, a potential of the bit line BL which is read out by the read-out circuit changes depending on the charge in the gate electrode of the transistor 300 of the row where reading is performed. Thus, data can be read out from to the memory cell of the specified row.

[0186]

Although the amount of data which can be stored in each of the memory cells 400 is one bit in the above description, the structure of the memory device of this embodiment is not limited to this. The amount of data which is stored in each of the memory cells 400 may be increased by preparing three or more potentials to be supplied to the gate electrode of the transistor 300. For example, in the case where the number of potentials to be supplied to the gate electrode of the transistor 300 is four, data of two bits can be stored in each of the memory cells.

[0187]

Next, examples of read-out circuit which can be used for the semiconductor devices in FIGS. 7A and 7B, or the like will be described with reference to FIGS. 8A to 8C.

[0188]

FIG. 8A illustrates a schematic view of the read-out circuit. The read-out circuit includes a transistor and a sense amplifier circuit.

[0189]

At the time of reading data, a terminal A is connected to a bit line to which a memory cell from which data is to be read is connected. Further, a bias potential Vbias is applied to a gate electrode of the transistor to control a potential of the terminal A.

[0190]

The resistance of the memory cell 400 changes depending on stored data. Specifically, when the transistor 300 in the selected memory cell 400 is on, the memory cell 400 has a low resistance, whereas when the transistor 300 in the selected memory cell 400 is off, the memory cell 400 has a high resistance.

5 [0191]

When the memory cell has a high resistance, a potential of the terminal A is higher than a reference potential Vref and the sense amplifier circuit outputs a potential corresponding to the potential of the terminal A. On the other hand, when the memory cell has a low resistance, the potential of the terminal A is lower than the reference
10 potential Vref and the sense amplifier circuit outputs a potential corresponding to the potential of the terminal A.

[0192]

Thus, by using the read-out circuit, data can be read out from the memory cell. Note that the read-out circuit of this embodiment is one of examples. Another circuit
15 may be used. The reading circuit may further include a precharge circuit. Instead of the reference potential Vref, a reference bit line may be connected to the sense amplifier circuit.

[0193]

FIG. 8B illustrates a differential sense amplifier which is an example of sense
20 amplifier circuits. The differential sense amplifier has an input terminal Vin(+) and an input terminal Vin(−), and an output terminal Vout, and amplifies the difference between Vin(+) and Vin(−). When Vin(+) > Vin(−), output of the Vout is substantially High, whereas when Vin(+) < Vin(−), the output of the Vout is substantially Low. In the case where the differential sense amplifier is used for the read-out circuit, one of Vin(+) and
25 Vin(−) is connected to the terminal A, and the reference potential Vref is applied to the other of Vin(+) and Vin(−).

[0194]

FIG. 8C illustrates a latch sense amplifier which is an example of a sense amplifier circuit. The latch sense amplifier includes input/output terminals V1, and V2,
30 an input terminal of a control signal Sp, and an input terminal of a control signal Sn. First, the control signals Sp and Sn are set to High and Low, respectively, and a power

supply potential (Vdd) is cut off. Then, potentials to be compared are applied to V1 and V2. After that, the signals Sp and Sn are set to Low and High, respectively, and a power supply potential (Vdd) is applied. If the potentials V1in and V2in to be compared satisfy V1in > V2in, output of the V1 is High and output of the V2 is Low, whereas if the potentials satisfy V1in < V2in, the output of V1 is Low and the output of V2 is High. By utilizing such a relation, the difference between V1in and V2in can be amplified. When the latch sense amplifier is used for the read-out circuit, one of V1 and V2 is connected to the terminal A and the output terminal through a switch, and the reference potential Vref is applied to the other of V1 and V2.

[0195]

The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[0196]

(Embodiment 5)

In this embodiment, the case where the semiconductor device described in any of embodiments 1 to 4 is applied to an electronic device will be described with reference to FIGS. 9A to 9F. In this embodiment, the case where the semiconductor device described in any of embodiments 1 to 4 is applied to an electronic device such as a computer, a mobile phone (also referred to as a mobile telephone or a mobile telephone device), a portable information terminal (including a portable game console, an audio player, and the like), a digital camera, a digital video camera, an electronic paper, or a television device (also referred to as a television or a television receiver) will be described.

[0197]

FIG. 9A is a notebook personal computer including a housing 601, a housing 602, a display portion 603, a keyboard 604, and the like. The semiconductor device described in any of the above embodiments is provided in the housing 601 and the housing 602. Therefore, the notebook personal computer which is downsized, with high speed operation and lower power consumption is realized.

[0198]

FIG. 9B is a portable information terminal (personal digital assistance (PDA)).

A main body 611 is provided with a display portion 613, an external interface 615, operation buttons 614, and the like. Further, a stylus 612 for operating the portable information terminal or the like is also provided. The miniaturized semiconductor device described in any of the above embodiments is provided in the main body 611.
5 Therefore, the portable information terminal which is downsized, with high speed operation and lower power consumption is realized.

[0199]

FIG. 9C is an e-book reader 620 mounting an electronic paper. The e-book reader has two housings, a housing 621 and a housing 623. The housing 621 and the
10 housing 623 are provided with a display portion 625 and a display portion 627, respectively. The housing 621 and the housing 623 are connected by a hinge 637 and can be opened and closed along the hinge 637. Further, the housing 621 is provided with a power switch 631, operation keys 633, a speaker 635, and the like. At least one of the housing 621 and the housing 623 is provided with the miniaturized
15 semiconductor device described in any of the above embodiments. Therefore, the e-book reader which is downsized, with high speed operation and lower power consumption is realized.

[0200]

FIG. 9 D is a mobile phone including two housings, a housing 640 and a
20 housing 641. Further, the housing 640 and the housing 641 in a state where they are developed as illustrated in FIG. 9D can shift by sliding so that one is lapped over the other; therefore, the size of the mobile phone can be reduced, which makes the mobile phone suitable for being carried. The housing 641 is provided with a display panel 642, a speaker 643, a microphone 644, a pointing device 646, a camera lens 647, an
25 external connection terminal 648, and the like. The housing 640 is provided with a solar cell 649 that charges the mobile phone, an external memory slot 650, and the like. In addition, an antenna is incorporated in the housing 641. At least one of the housing 640 and the housing 641 is provided with the miniaturized semiconductor device described in any of the above embodiments. Therefore, the mobile phone which is
30 downsized, with high speed operation and lower power consumption is realized.

[0201]

FIG. 9E is a digital camera including a main body 661, a display portion 667,

an eyepiece 663, an operation switch 664, a display portion 665, a battery 666, and the like. The miniaturized semiconductor device described in any of the above embodiments is provided in the main body 661. Therefore, the digital camera which is downsized, with high speed operation and lower power consumption is realized.

5 [0202]

FIG. 9F is a television device 670 including a housing 671, a display portion 673, a stand 675, and the like. The television device 670 can be operated by an operation switch of the housing 671 or a separate remote control 680. The miniaturized semiconductor device described in any of the above embodiments is

10 mounted in the housing 671 and the remote control 680. Therefore, the television device which is downsized, with high speed operation and lower power consumption is realized.

[0203]

Thus, the semiconductor device according to any of the above embodiments is

15 mounted on the electronic devices described in this embodiment. Accordingly, electronic devices which are down sized, with high speed operation and lower power consumption are realized.

[Example 1]

[0204]

20 In this example, the results of computational verification of characteristics of the semiconductor device according to an embodiment of the present invention will be described with reference to FIGS. 10A and 10B, FIGS. 11A and 11B, FIG. 12A and 12B, and FIG. 13. Specifically, characteristics of transistors each having a different channel length L were compared. Note that a device simulation software “Atlas” manufactured

25 by Silvaco Inc. was used for the calculation.

[0205]

FIGS. 10A and 10B illustrate structures of transistors which were used for the calculation. FIG. 10A illustrates a structure according to one embodiment of the present invention (a structure in which part of a source electrode or a drain electrode is

30 extended), and FIG. 10B illustrates a structure for comparison (a structure in which part of a source electrode or a drain electrode is not extended).

[0206]

The detail of the transistors used for the calculation is described. The transistor illustrated in FIG. 10A includes a source electrode in which a first conductive layer 742a (material: titanium, thickness: 100 nm) and a second conductive layer 745a (material: titanium nitride, thickness: arbitrary set) are stacked in this order; a drain
5 electrode in which a first conductive layer 742b (material: titanium, thickness: 100 nm) and a second conductive layer 745b (material: titanium nitride, thickness: arbitrary set) are stacked in this order; an insulating layer 743a (material: silicon oxide, thickness: 100 nm) provided over the source electrode; an insulating layer 743b (material: silicon oxide, thickness: 100 nm) provided over the drain electrode; an oxide semiconductor
10 layer 744 (material: In-Ga-Zn-O-based oxide semiconductor, thickness: 10 nm) provided over the insulating layers 743a and 743b; a gate insulating layer 746 (material: hafnium oxide, thickness: 10 nm) provided over the oxide semiconductor layer 744; and a gate electrode 748 (material: tungsten) provided over the gate insulating layer 746.

[0207]

15 In the transistor illustrated in FIG. 10A, the second conductive layer 745a has a region which extends in the channel length direction from an end portion of the first conductive layer 742a (that is, an end portion of the second conductive layer 745a is closer to a channel formation region than an end portion of the first conductive layer 742a), and the end portion of the second conductive layer 745a is in contact with the
20 channel formation region of the oxide semiconductor layer 744. Similarly, the second conductive layer 745b has a region which extends in the channel length direction from an end portion of the first conductive layer 742b (that is, an end portion of the second conductive layer 745b is closer to the channel formation region than an end portion of the first conductive layer 742b), and the end portion of the second conductive layer
25 745b is in contact with the channel formation region of the oxide semiconductor layer 744.

[0208]

The transistor illustrated in FIG. 10B includes a source electrode (material: titanium nitride, thickness: 100 nm) and a drain electrode (material: titanium nitride,
30 thickness: 100 nm) including a conductive layer 752a and a conductive layer 752b, respectively; the oxide semiconductor layer 744 (material: In-Ga-Zn-O-based oxide semiconductor, thickness: 10 nm) over the source electrode and the drain electrode; the

gate insulating layer 746 (material: hafnium oxide, thickness: 10 nm) provided over the oxide semiconductor layer 744; and the gate electrode 748 (material: tungsten) provided over the gate insulating layer 746.

[0209]

5 The difference between FIGS. 10A and 10B is the existences of the region which extends in a channel length direction from the end portion of the first conductive layer 742a in the second conductive layer 745a, the region which extends in a channel length direction from the end portion of the first conductive layer 742b in the second conductive layer 745b, and the insulating layer over the source electrode and the 10 insulating layer over the drain electrode.

[0210]

In FIG. 10A, the region (the region formed of the second conductive layer) which extends in the channel length direction from the end portion of the first conductive layer 742a in the second conductive layer 745a has smaller thickness of the 15 electrode than the other region (the region formed of a stacked-layer of the first conductive layer and the second conductive layer). That is, the area of the cross section perpendicular to the flow of the charge becomes small. The resistance is inversely proportional to the area of the cross section; therefore, the region which extends in the channel length direction from the end portion of the first conductive layer 20 742a in the second conductive layer 745a has higher resistance than other regions. The same can be said for the second conductive layer 745b. Hereinafter, in this example, the region which extends in the channel length direction from the end portion of the first conductive layer 742a in the second conductive layer 745a, and the region which extends in the channel length direction from the end portion of the first conductive layer 25 742b in the second conductive layer 745b are referred to as high-resistance regions (HRR).

[0211]

In FIG. 10A, un upper portion of the source electrode is covered with the insulating layer 743a and un upper portion of the drain electrode is covered with the 30 insulating layer 743b; thus, the contact area between each of the source electrode and drain electrode and the oxide semiconductor layer 744 is extremely small (here, only the end portions of the second conductive layers are in contact with the oxide

semiconductor layer 744). That is, it can be said that the source electrode and drain electrode has higher resistance regions than other regions in the vicinity of the regions in contact with the channel formation region.

[0212]

5 In the above structure (FIGS. 10A and 10B), by changing the channel length (L), how the threshold voltage (V_{th}) of the transistor moves was examined. As the channel length (L), the six conditions of 20 nm, 30 nm, 50 nm, 100 nm, 200 nm, and 400 nm were adopted.

[0213]

10 Further, by changing the thickness of the second conductive layer, how the threshold voltage (V_{th}) of the transistor moves was examined. As the thickness of the second conductive layer (L), the following four conditions were adopted, 3 nm, 10 nm, 50 nm, and 100 nm.

[0214]

15 The voltage (Vds) between the source electrode and the drain electrode was set to 1V. In addition, the length in the channel length direction of the high-resistance regions was set to 0.3 μm.

[0215]

Parameters used for the calculation are given below.

20 1. an In-Ga-Zn-O-based oxide semiconductor (a material for the oxide semiconductor layer), a band gap Eg: 3.15 eV, an electron affinity χ: 4.3 eV, a relative dielectric constant: 15, an electron mobility: 10 cm^2/Vs, and effective density of states in the conduction band: 5×10^{18} cm^{-3}.

2. titanium nitride (a material for the source electrode and drain electrode), a

25 work function ϕ_M: 3.9 eV, and resistivity ρ: 2.2×10^{-4} Ω·cm.

3. hafnium oxide (a material for the gate insulating layer), and a relative dielectric constant: 15.

4. tungsten (a material for the gate electrode), and a work function ϕ_M: 4.9 eV.

[0216]

30 The calculation results are shown in FIGS. 11A and 11B, FIGS. 12A and 12B, and FIG. 13. In FIGS. 11A and 11B, FIGS. 12A and 12B, and FIG. 13, the horizontal axis represents the channel length L (nm), and the vertical axis represents the amount of

shift in the threshold voltage (ΔV_{th}). Note that ΔV_{th} is calculated on the basis of the threshold voltage when the channel length L is 400 nm.

[0217]

FIGS. 11A and 11B, and FIGS. 12A and 12B show calculation results of the structure illustrated in FIG. 10A. FIG. 11A shows a calculation result when the thickness of the second conductive layer is 100 nm, FIG. 11B shows a calculation result when the thickness of the second conductive layer is 50 nm, FIG. 12A shows a calculation result when the thickness of the second conductive layer is 10 nm, and FIG. 12B shows a calculation result when the thickness of the second conductive layer is 3 nm. FIG. 13 shows a calculation result of the structure illustrated in FIG. 10B.

[0218]

By comparison of FIGS. 11A and 11B, and FIGS. 12A and 12B, it is found that, as the second conductive film is thinner, minus shift of the threshold voltage can be suppressed. Further, by comparison of FIG. 11A and FIG. 13, it is found that the minus shift of V_{th} is suppressed when the insulating layer which covers the source electrode and drain electrode is provided. The above suggests that the short-channel effect can be controlled by reducing the contact area between each of the source electrode and drain electrode and the oxide semiconductor layer and increasing contact resistance at a contact interface.

[0219]

Further, from the above results, in the vicinity of the region in contact with the semiconductor layer, when the resistance of the source electrode and drain electrode is increased, an effect of controlling the short-channel effect can be obtained.

[0220]

Accordingly, it can be understood that the minus shift of the threshold voltage can be suppressed by making the vicinity of the region where each of the source electrode and drain electrode is in contact with the channel formation region have high resistance (specifically, for example, by making a small cross-sectional area of part of each of the source electrode and drain electrode, and forming the insulating layer which covers the upper portion of each of the source electrode and drain electrode so that the contact area of the source electrode or drain electrode and the oxide semiconductor layer 144 is reduced). This is because the electric field intensity between the source

electrode and drain electrode is relieved. As described above, it is suggested that the short-channel effect such as a decrease in a threshold voltage can be suppressed according to an embodiment of the present invention.

5

This application is based on Japanese Patent Application serial no. 2010-012540 filed with Japan Patent Office on January 22, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

an oxide semiconductor layer;

5 a source electrode in contact with the oxide semiconductor layer comprising:

a first conductive layer; and

a second conductive layer;

a drain electrode in contact with the oxide semiconductor layer comprising:

a third conductive layer; and

10 a fourth conductive layer;

a gate electrode overlapping with the oxide semiconductor layer; and

a gate insulating layer provided between the oxide semiconductor layer and the gate electrode,

wherein the second conductive layer extends beyond an end portion of the first

15 conductive layer,

wherein the fourth conductive layer extends beyond an end portion of the third conductive layer, and

wherein the end portion of the first conductive layer and the end portion of the third conductive layer are opposed to each other.

20

2. The semiconductor device according to claim 1, wherein the first conductive layer, the second conductive layer, the third conductive layer and the fourth conductive layer each has a tapered shape.

25 3. The semiconductor device according to claim 1, further comprising:

a first sidewall insulating layer over the second conductive layer and in contact with the end portion of the first conductive layer; and

a second side wall insulating layer over the fourth conductive layer and in contact with the end portion of the third conductive layer.

30

4. The semiconductor device according to claim 1, wherein a material of the second conductive layer and a material of the fourth conductive layer are a nitride of a

metal.

5. The semiconductor device according to claim 1, wherein a thickness of the second conductive layer and a thickness of the fourth conductive layer are from 5 nm to
5 15 nm.

6. The semiconductor device according to claim 1, further comprising:

a first insulating layer provided between the oxide semiconductor layer and the source electrode; and

10 a second insulating layer provided between the oxide semiconductor layer and the drain electrode,

wherein the source electrode and the drain electrode are in contact with the oxide semiconductor layer at end portions of the source electrode and the drain electrode .

15

7. A semiconductor device comprising:

an oxide semiconductor layer;

a source electrode comprising:

a first conductive layer; and

20 a second conductive layer in contact with the oxide semiconductor layer;

a drain electrode comprising:

a third conductive layer; and

a fourth conductive layer in contact with the oxide semiconductor
25 layer;

a gate electrode overlapping with the oxide semiconductor layer; and

a gate insulating layer provided between the oxide semiconductor layer and the gate electrode,

wherein the second conductive layer is over the first conductive layer, and the
30 second conductive layer has a higher resistance than the first conductive layer, and

wherein the fourth conductive layer is over the third conductive layer, and the fourth conductive layer has a higher resistance than the third conductive layer.

8. The semiconductor device according to claim 7, wherein the first conductive layer and the third conductive layer are in contact with the oxide semiconductor layer.

5 9. The semiconductor device according to claim 7,

wherein the second conductive layer extends beyond an end portion of the first conductive layer,

wherein the fourth conductive layer extends beyond an end portion of the third conductive layer, and

10 wherein the end portion of the first conductive layer and the end portion of the third conductive layer are opposed to each other.

10. The semiconductor device according to claim 7, wherein the first conductive layer, the second conductive layer, the third conductive layer and the fourth 15 conductive layer each has a tapered shape.

11. The semiconductor device according to claim 7, wherein a material of the second conductive layer and a material of the fourth conductive layer are a nitride of a metal.

20

12. The semiconductor device according to claim 7, wherein a thickness of the second conductive layer and a thickness of the fourth conductive layer are from 5 nm to 15 nm.

25 13. The semiconductor device according to claim 7, further comprising:

a first insulating layer provided between the oxide semiconductor layer and the source electrode; and

a second insulating layer provided between the oxide semiconductor layer and the drain electrode,

30 wherein the source electrode and the drain electrode are in contact with the oxide semiconductor layer at end portions of the source electrode and the drain electrode .

14. A semiconductor device comprising:

an oxide semiconductor layer;

a source electrode comprising:

5 a first conductive layer; and

a second conductive layer in contact with the oxide semiconductor layer;

a drain electrode comprising:

a third conductive layer; and

10 a fourth conductive layer in contact with the oxide semiconductor layer;

a gate electrode overlapping with the oxide semiconductor layer; and

a gate insulating layer provided between the oxide semiconductor layer and the gate electrode,

15 wherein the first conductive layer is over the second conductive layer, and the second conductive layer has a higher resistance than the first conductive layer, and

wherein the third conductive layer is over the fourth conductive layer, and the fourth conductive layer has a higher resistance than the third conductive layer.

20 15. The semiconductor device according to claim 14, wherein the first conductive layer and the third conductive layer are in contact with the oxide semiconductor layer.

16. The semiconductor device according to claim 14,

25 wherein the second conductive layer extends beyond an end portion of the first conductive layer,

wherein the fourth conductive layer extends beyond an end portion of the third conductive layer, and

wherein the end portion of the first conductive layer and the end portion of the third conductive layer are opposed to each other. 30

17. The semiconductor device according to claim 14, wherein the first

conductive layer, the second conductive layer, the third conductive layer and the fourth conductive layer each has a tapered shape.

18. The semiconductor device according to claim 16, further comprising:

5 a first sidewall insulating layer over the second conductive layer and in contact with the end portion of the first conductive layer; and

a second side wall insulating layer over the fourth conductive layer and in contact with the end portion of the third conductive layer.

10 19. The semiconductor device according to claim 14, wherein a material of the second conductive layer and a material of the fourth conductive layer are a nitride of a metal.

20. The semiconductor device according to claim 14, wherein a thickness of the

15 second conductive layer and a thickness of the fourth conductive layer are from 5 nm to 15 nm.

21. The semiconductor device according to claim 14, further comprising:

a first insulating layer provided between the oxide semiconductor layer and the

20 source electrode; and

a second insulating layer provided between the oxide semiconductor layer and the drain electrode,

wherein the source electrode and the drain electrode are in contact with the oxide semiconductor layer at end portions of the source electrode and the drain

25 electrode .

22. A semiconductor device comprising:

an oxide semiconductor layer including a channel formation region;

a source electrode including a region in contact with the channel formation

30 region;

a drain electrode including a region in contact with the channel formation region;

a gate electrode overlapping with the channel formation region; and

a gate insulating layer provided between the oxide semiconductor layer and the gate electrode,

wherein the region of the source electrode has a higher resistance than other regions of the source electrode, and

wherein the region of the drain electrode has a higher resistance than other regions of the drain electrode.

23. The semiconductor device according to claim 22, further comprising:

a first insulating layer provided between the oxide semiconductor layer and the source electrode; and

a second insulating layer provided between the oxide semiconductor layer and the drain electrode,

wherein the source electrode and the drain electrode are in contact with the oxide semiconductor layer at end portions of the source electrode and the drain electrode.

ABSTRACT

An object is to provide a semiconductor device including an oxide semiconductor, which maintains favorable characteristics and achieves miniaturization. The semiconductor device includes an oxide semiconductor layer, a source electrode 5 and a drain electrode in contact with the oxide semiconductor layer, a gate electrode overlapping with the oxide semiconductor layer, and a gate insulating layer provided between the oxide semiconductor layer and the gate electrode, in which the source electrode and the drain electrode each include a first conductive layer, and a second conductive layer having a region which extends in a channel length direction from an 10 end portion of the first conductive layer.

FIG. 1A

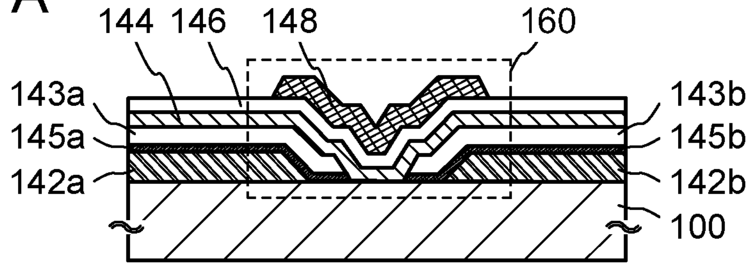


FIG. 1B

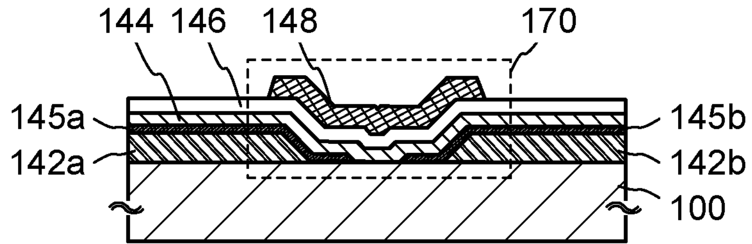


FIG. 1C

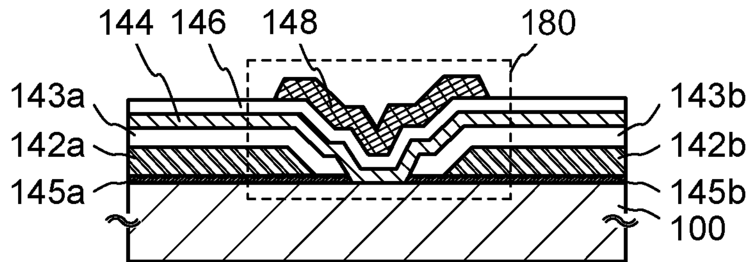


FIG. 1D

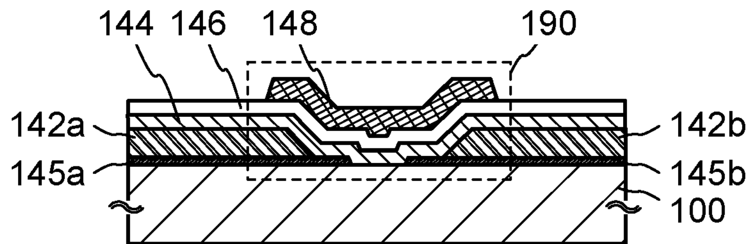


FIG. 2A

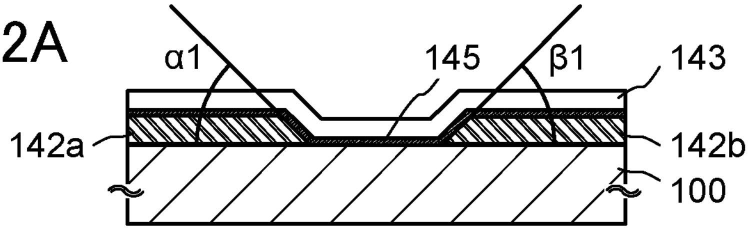


FIG. 2B

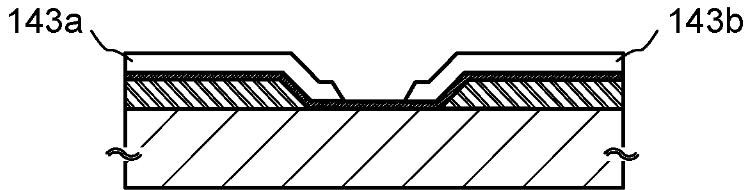


FIG. 2C

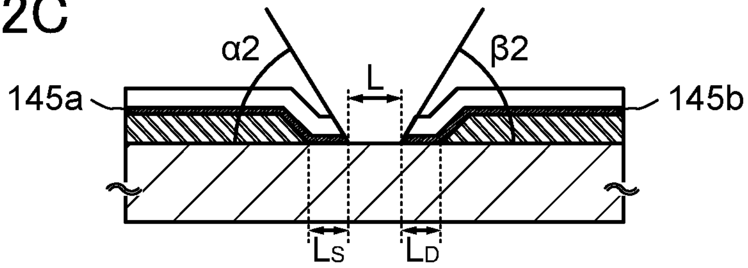


FIG. 2D

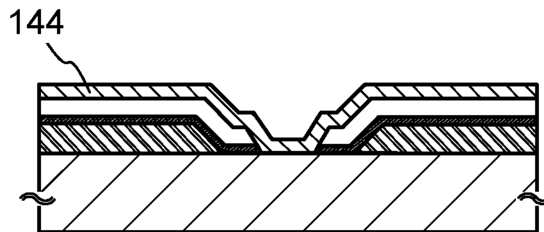


FIG. 2E

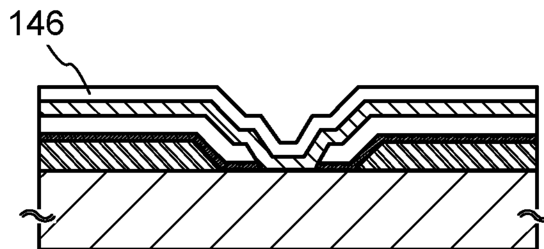


FIG. 2F

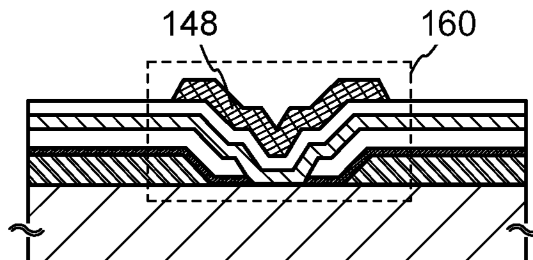


FIG. 3A

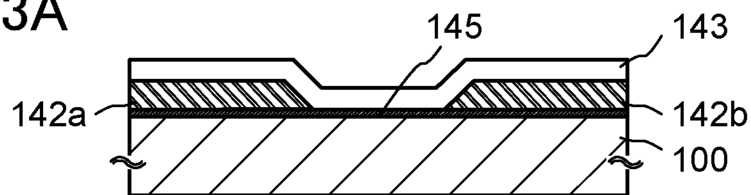


FIG. 3B

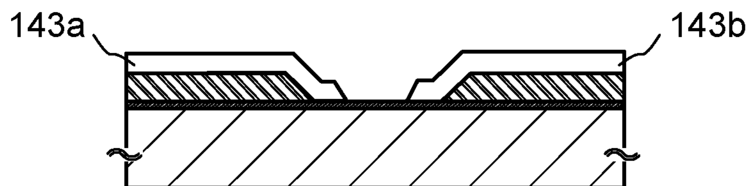


FIG. 3C

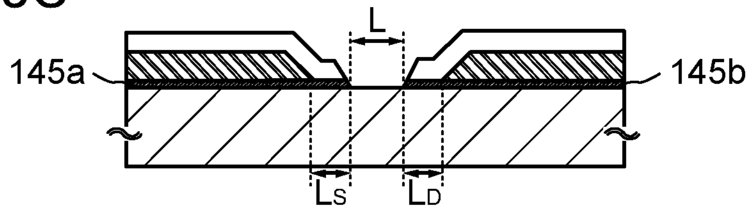


FIG. 3D

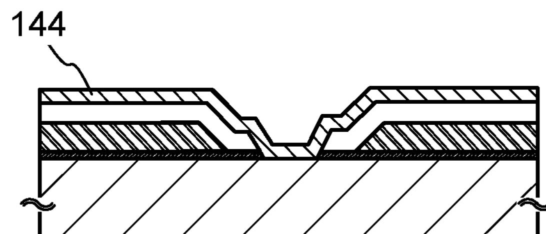


FIG. 3E

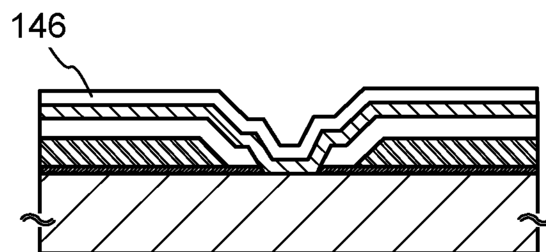


FIG. 3F

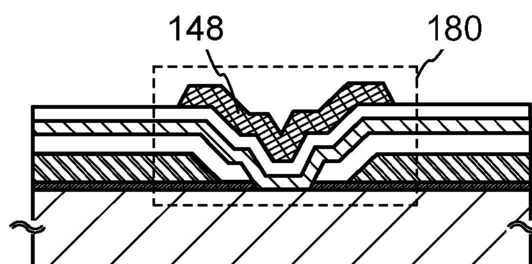


FIG. 4

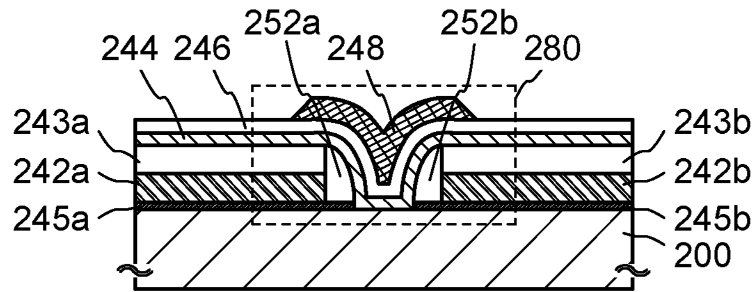


FIG. 5A

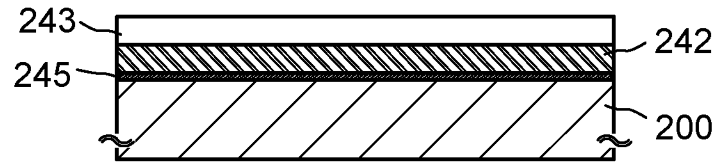


FIG. 5B

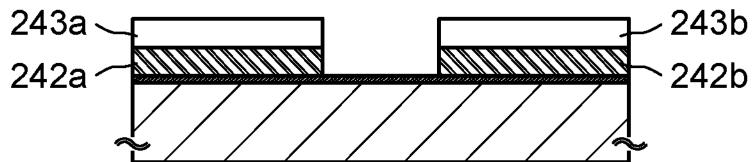


FIG. 5C

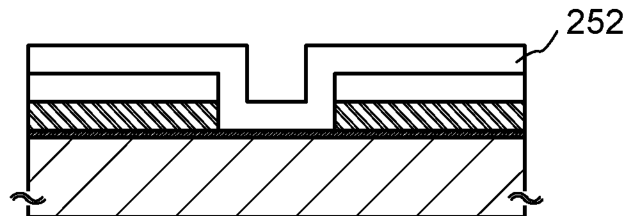


FIG. 5D

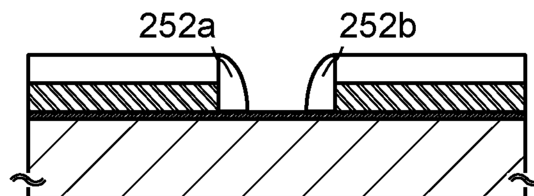


FIG. 5E

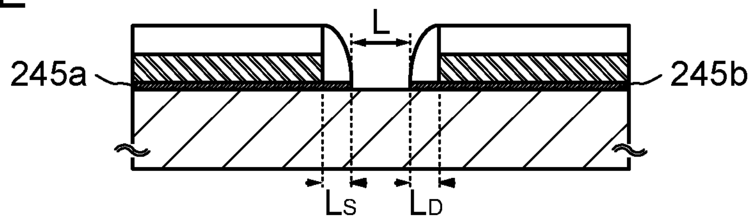


FIG. 5F

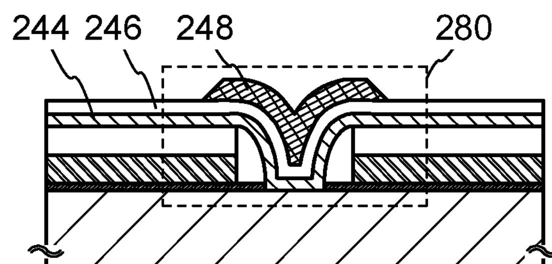


FIG. 6A1

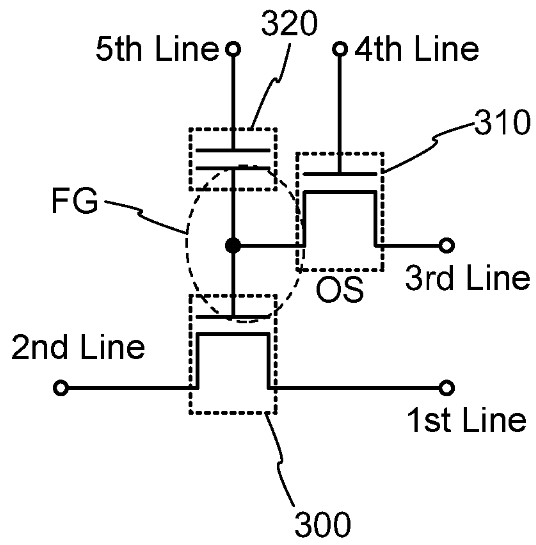


FIG. 6B

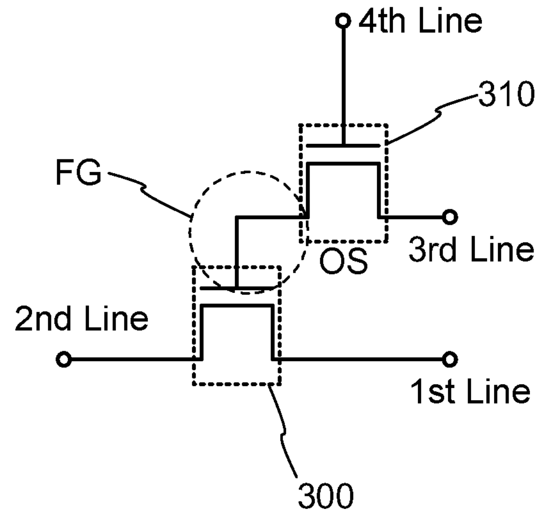


FIG. 6A2

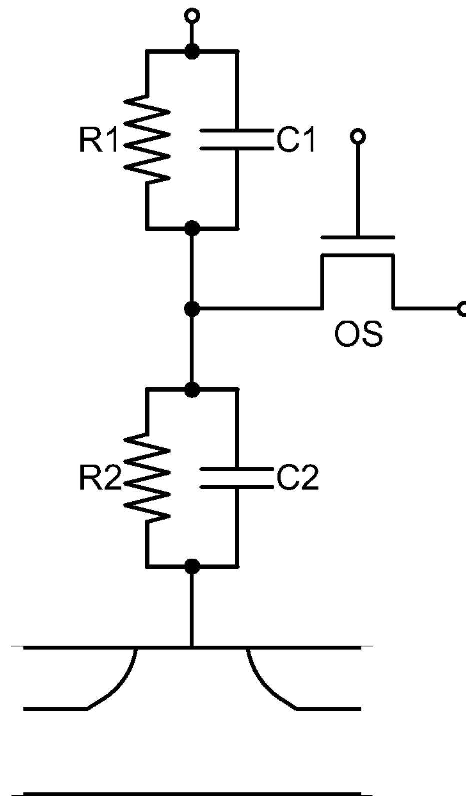


FIG. 7A

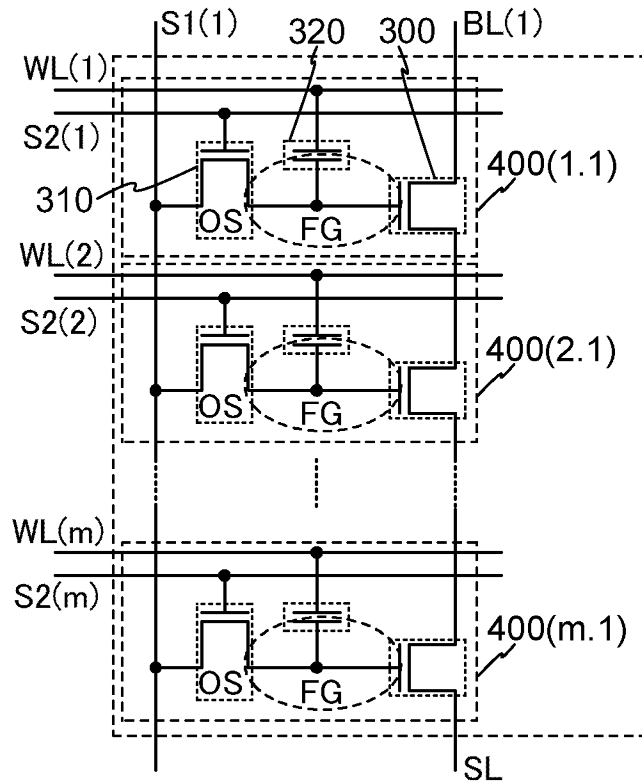


FIG. 7B

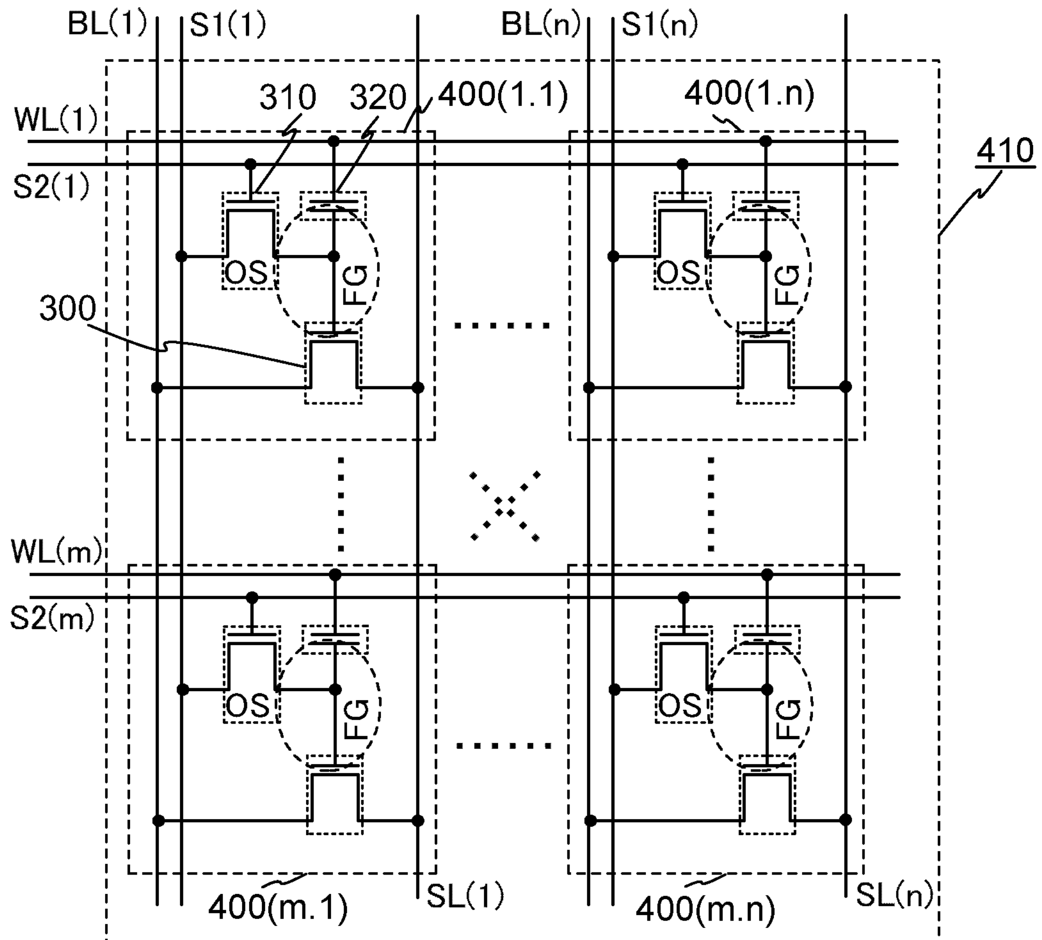


FIG. 8A

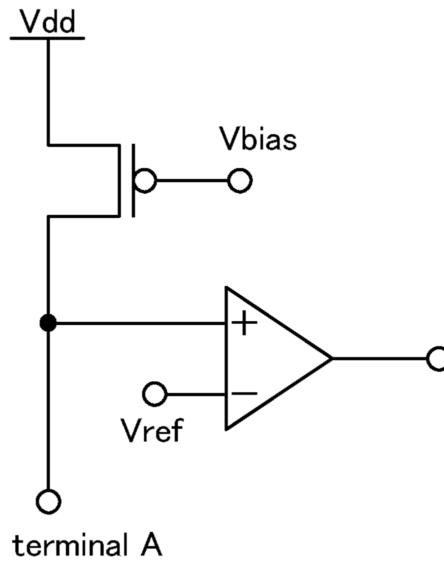


FIG. 8B

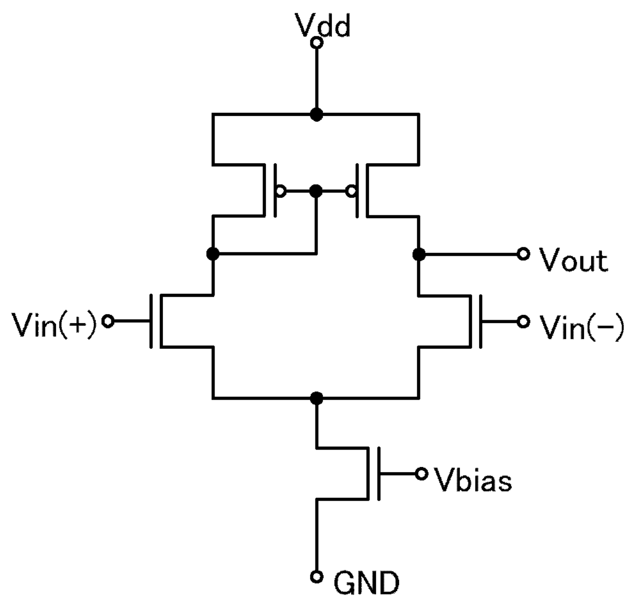


FIG. 8C

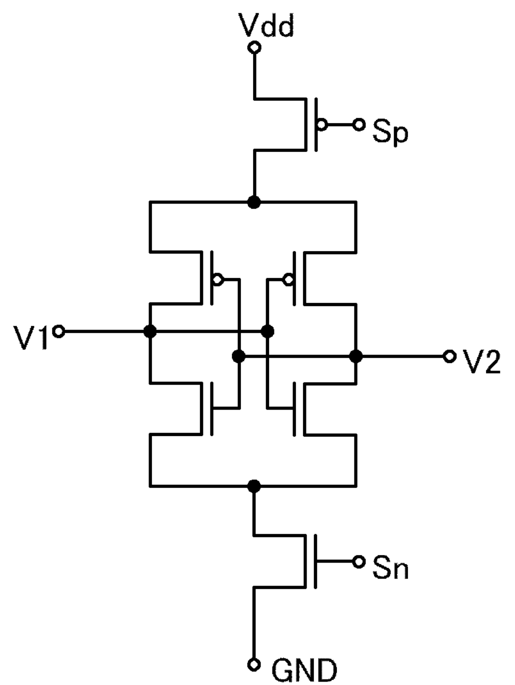


FIG. 9A

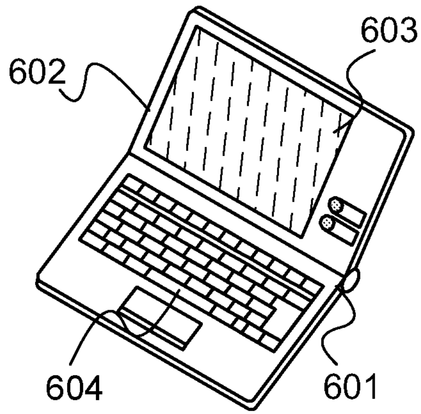


FIG. 9D

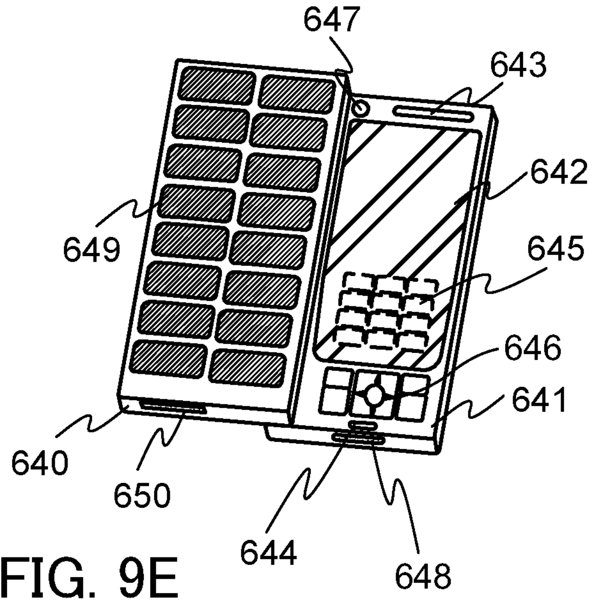


FIG. 9B

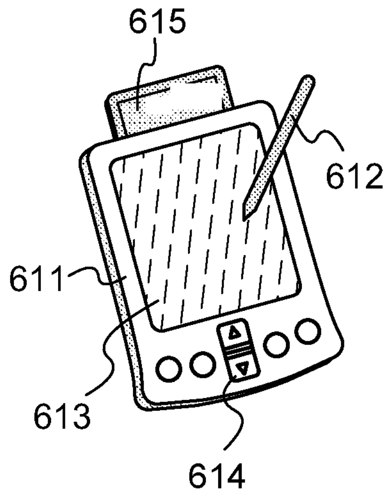


FIG. 9E

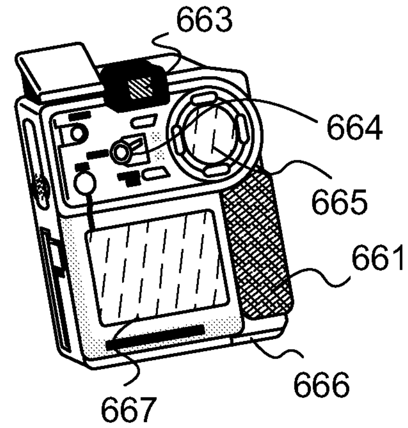


FIG. 9C

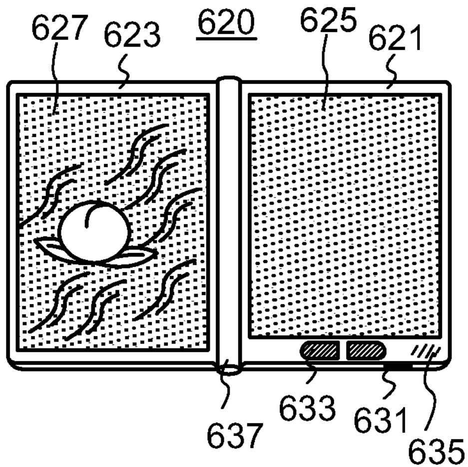


FIG. 9F

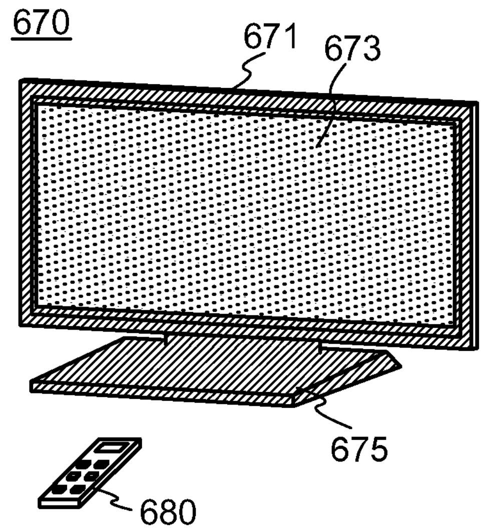


FIG. 10A

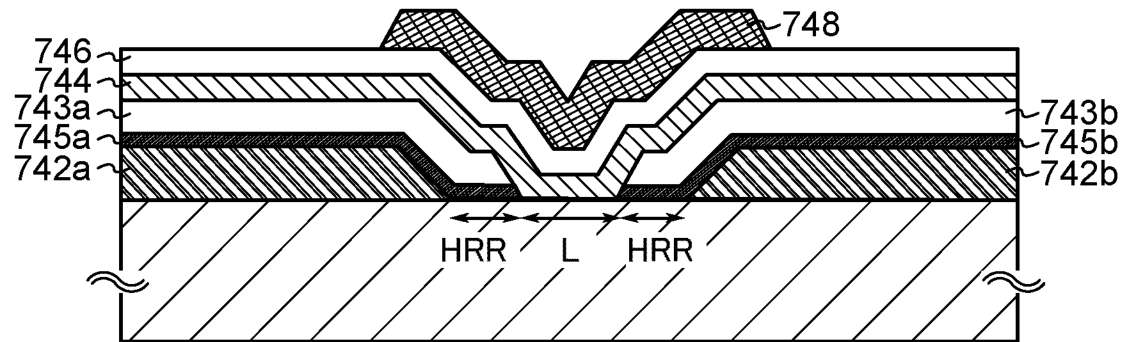


FIG. 10B

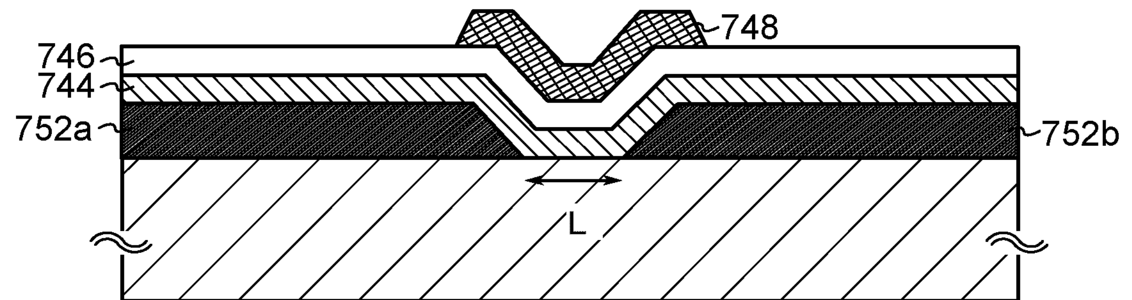


FIG. 11A

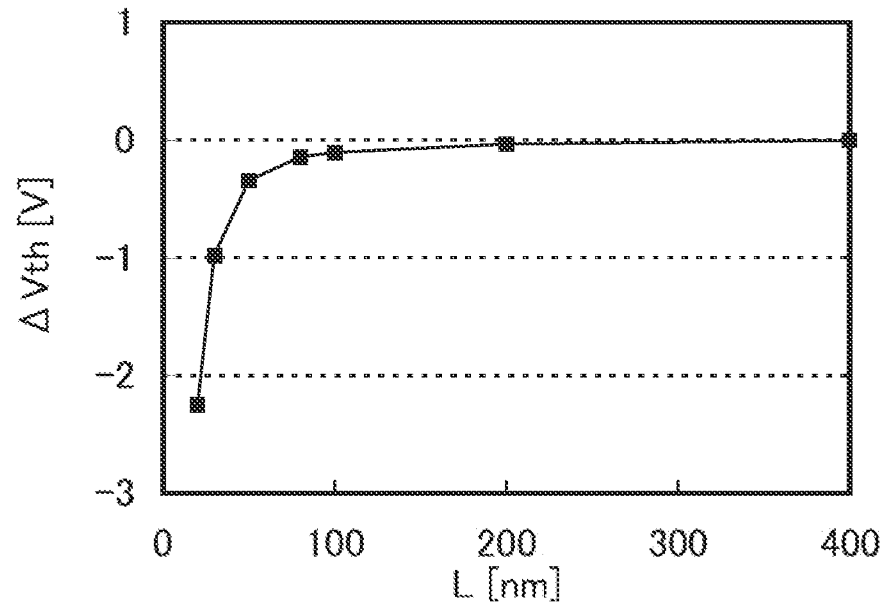


FIG. 11B

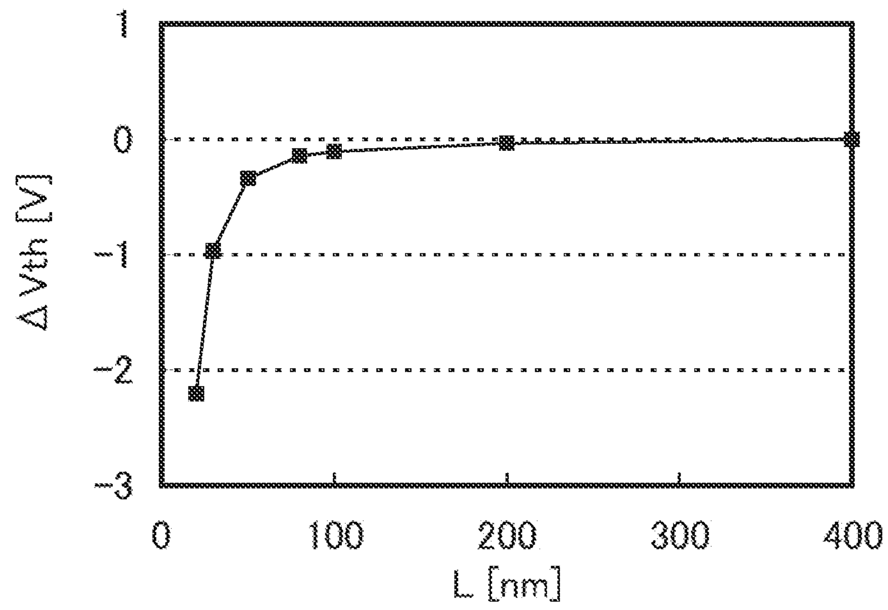


FIG. 12A

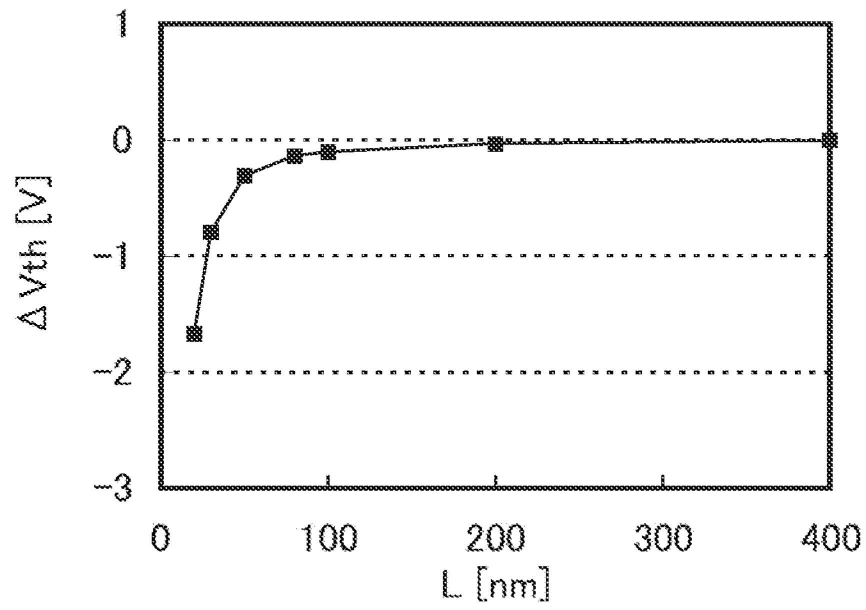


FIG. 12B

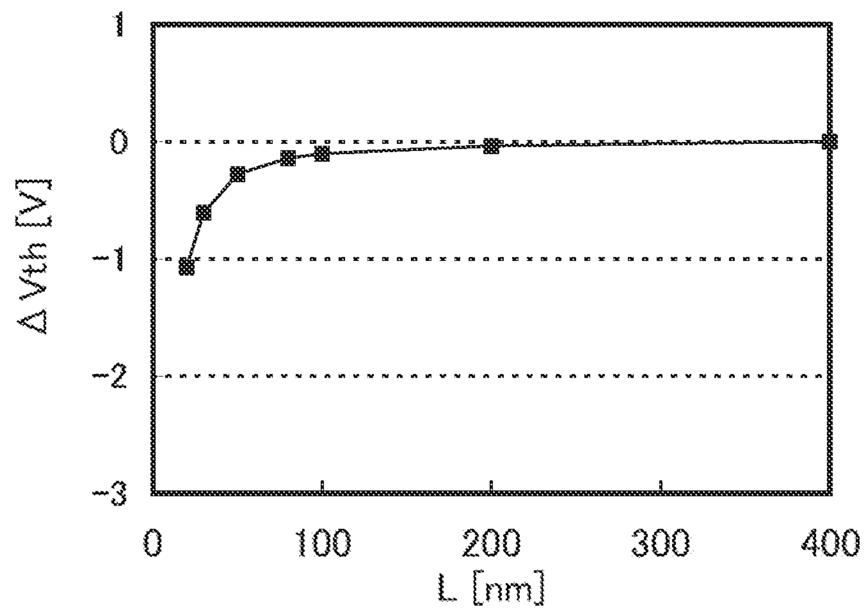
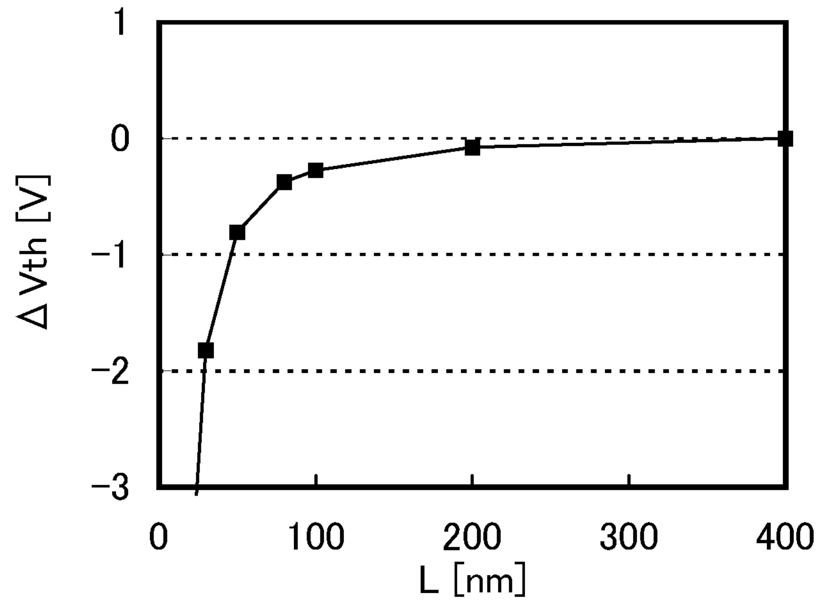


FIG. 13



EXPLANATION OF REFERENCE

100: substrate, 142a: first conductive layer, 142b: first conductive layer, 143: insulating film; 143a: insulating layer, 143b: insulating layer, 144: oxide semiconductor layer, 145: conductive film, 145a: second conductive layer, 145b: second conductive layer, 146: gate insulating layer, 148: gate electrode, 160: transistor, 170: transistor, 180: transistor, 190: transistor, 200: substrate, 242: conductive film, 242a: first conductive layer, 242b: first conductive layer, 243: insulating film, 243a: insulating layer, 243b: insulating layer, 244: oxide semiconductor layer, 245: conductive film, 245a: second conductive layer, 245b: second conductive layer, 246 gate insulating layer, 248: gate electrode, 252: insulating film, 252a: sidewall insulating layer, 252b: sidewall insulating layer, 280: transistor, 300: transistor, 310: transistor, 320: capacitor, 400: memory cell, 410: memory cell array, 601: housing, 602: housing, 603: display portion, 604: keyboard, 611: main body, 612: stylus, 613: display portion, 614: operation button, 615: external interface, 620: e-book reader, 621: housing , 623: housing, 625: display portion, 627: display portion, 631: power switch, 633: operation key, 635: speaker, 637: hinge, 640: housing, 641: housing, 642: display panel, 643: speaker, 644: a microphone, 645: operation key, 646: pointing device, 647: camera lens, 648: an external connection terminal, 649: solar cell, 650: external memory slot, 661: main body, 663: eyepiece, 664: operation switch, 665: display portion, 666: battery, 667: display portion, 670: television device, 671: housing, 673: display portion, 675: stand, 680: remote control, 742a: first conductive layer, 742b: first conductive layer, 743a: insulating layer, 743b: insulating layer, 744: oxide semiconductor layer, 745a: second conductive layer, 745b: second conductive layer, 746: gate insulating layer, 748: gate electrode, 752a: conductive layer.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Shunpei Yamazaki
Filer:	Eric J. Robinson/Sue Ann Carr
Attorney Docket Number:	0756-9138

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	3	52	156
Independent claims in excess of 3	1201	1	220	220
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1466**

Electronic Acknowledgement Receipt

EFS ID:	9246253
Application Number:	13008285
International Application Number:	
Confirmation Number:	8496
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Shunpei Yamazaki
Customer Number:	31780
Filer:	Eric J. Robinson/Sue Ann Carr
Filer Authorized By:	Eric J. Robinson
Attorney Docket Number:	0756-9138
Receipt Date:	18-JAN-2011
Filing Date:	
Time Stamp:	14:38:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$1466
RAM confirmation Number	1020
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Fee Worksheet (PTO-875)	FEEWORKSHEET.pdf	261182 92a414b6401ef5d80911027d55dc7b0bd13536c7	no	2
Warnings:					
Information:					
2	Transmittal of New Application	TRNA.pdf	209230 2e81f954a4b52269854e5911143a186e81286889	no	1
Warnings:					
Information:					
3	Application Data Sheet	ADS.pdf	1354018 01962f0b8d2b96197740e9f70f39752ec0d4a5ca	no	6
Warnings:					
Information:					
4		IDS.pdf	530023 72c95e1eead07ee237e31061daf10c1d47642af1	yes	3

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal Letter	1	1
Information Disclosure Statement (IDS) Filed (SB/08)	2	3

Warnings:					
Information:					
5	Foreign Reference	JP60198861_FULL.pdf	228044 0acc954afc3aa6d54c23c316f70a32f5fff479c7	no	9
Warnings:					
Information:					
6	Foreign Reference	JP08264794_FULL.pdf	1094129 3e924116863efdb8a874c05862f0e691006c8cca	no	30
Warnings:					
Information:					
7	Foreign Reference	JP11505377.pdf	2934355 efd3379c07f11ab4d625b4772ce165eb655587a6	no	28
Warnings:					
Information:					
8	Foreign Reference	JP2000150900.pdf	1959657 f675f6cd41feb6411ede8f150dbf0a3b17d5e3c1	no	10

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	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	59
	Claims	60	65
	Abstract	66	66
	Drawings-only black and white line drawings	67	80

Warnings:

Information:

18	Fee Worksheet (PTO-875)	fee-info.pdf	38020 36ff50bbc68dd4280adc306dc9c63dfe23524c0a	no	2

Warnings:

Information:

Total Files Size (in bytes):	20008595

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (10-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 0756-9138

APPLICATION AS FILED – PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	23 minus 20 =	* 3	x =	0	OR	x 52 =	156
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	* 1	x =	0		x 220 =	220
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			N/A			N/A	
			TOTAL	0		TOTAL	1466

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT A

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE ($)	SMALL ENTITY ADDI-TIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDI-TIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	= 0	x =	0	OR	x =	0
Independent (37 CFR 1.16(h))	*	Minus	***	= 0	x =	0	OR	x =	0
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	0

AMENDMENT B

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE ($)	SMALL ENTITY ADDI-TIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDI-TIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	= 0	x =	0	OR	x =	0
Independent (37 CFR 1.16(h))	*	Minus	***	= 0	x =	0	OR	x =	0
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	0

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.