UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Intel Incorporated
Petitioner

v.

Qualcomm Incorporated
Patent Owner

Case IPR2018-01336
Patent 8,838,949

PRELIMINARY PATENT OWNER RESPONSE TO PETITION FOR INTER PARTES REVIEW PURSUANT TO 37 C.F.R. § 42.107

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I. INTRODUCTION

Intel Incorporated ("Intel" or "Petitioner") seeks review of claims 18-21 of U.S. Patent No. 8,838,949 (the "'949 Patent") based on obviousness grounds.[1] Institution should be denied.

The claims of the '949 Patent relate to a novel way to transfer an executable software image from memory of a first processor into memory of a second processor without requiring an intermediate buffering step. None of the references relied on by the Petitioner address this problem. It is therefore not surprising that Petitioner's proposed combination fails to disclose many claim limitations, forcing Petitioner to repeatedly rely on speculation and lawyer argument about what might have been obvious to the person of ordinary skill in the art (POSA). This type of "hand-waving" obviousness analysis is insufficient under *KSR Int'l Co. v. Teleflex Inc.,* 550 U.S. 398 (2007), and thus fails to establish a reasonable likelihood that at least one of the claims challenged in the petition is unpatentable.

Further, the Declaration of Dr. Bill Lin (Ex. 1202), filed by Petitioner does not remedy the deficiencies of the Petition. In fact, the Declaration provides little to no independent evidence or factual support and largely parrots the arguments made in the Petition. The Board has recognized that declarations that merely "expertize"

[1] Petitioner seeks review of claims 1-9, 22 and 23 of the '949 Patent in IPR2018-01334, and seeks review of claims 10-17 in IPR2018-01335.

lawyer argument without providing independent expert analysis are entitled to little or no evidentiary weight. *See, e.g.*, *Initiative for Medicines, Access, & Knowledge, Inc. v. Gilead Pharmasset LLC*, IPR2018-00120, Paper 7 at 21 (PTAB May 4, 2018) (declaration merely "parrots the Petition … and, therefore, does not remedy the various deficiencies in Petitioner's ground of unpatentability") (citing *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 294 (Fed. Cir. 1985)). Because the Declaration of Dr. Lin adds nothing to the allegations set forth in the Petition, the Declaration should be given little or no evidentiary weight.

Intel's petition fails to establish a reasonable likelihood of prevailing on any claim, and therefore the Board should decline to institute trial on the '949 Patent.

II. THE '949 PATENT AND ITS PROSECUTION HISTORY

A. Overview of the '949 Patent

U.S. Patent No. 8,838,949 ("the '949 Patent"), titled "Direct Scatter Loading of Executable Software Image From a Primary Processor to One or More Secondary Processor in a Multi-Processor System," generally relates to multi-processor systems in which a primary processor is coupled to a non-volatile memory storing executable software image(s) of one or more secondary processors that are each coupled to a dedicated volatile memory, where the executable software images are efficiently communicated from the primary processor to the secondary processor(s) in a segmented format (*e.g.*, using a direct scatter load process). *See* Ex. 1201 ('949

Patent) at 1:25-33. The '949 Patent issued on September 16, 2014 from an application filed on March 21, 2011. The '949 Patent claims priority to three provisional applications, the earliest of which was filed on April 14, 2010.

"In a multi-processor system, each processor may require respective boot code for booting up. As an example, in a smartphone device that includes an application processor and a modem processor, each of the processors may have respective boot code for booting up." *Id.* at 1:39-43. The '949 Patent explains that in some multi-processor systems, one of the processors is responsible for storing the boot code for one or more other processors in the system and loading the respective boot code to the other processor(s) at power-up. "In this type of system, the software (e.g., boot image) is downloaded from the first processor to the other processor(s) (e.g., to volatile memory of the other processor(s)), and thereafter the receiving processor(s) boots with the downloaded image." *Id.* at 2:1-14.

The Background section of the '949 Patent describes systems in which the boot image is loaded onto a target "secondary" processor from a first "primary" processor using "an intermediate step where the binary multi-segmented image is transferred into the system memory and then later transferred into target locations by the boot loader." *See id.* at 2:17-22. "One way of performing such loading is to allocate a temporary buffer into which each packet is received." *Id.* at 2:25-26. "The temporary buffer would be some place in system memory, such as in internal

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