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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,516	03/21/2011	Nitin Gupta	101459	6620

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QUALCOMM INCORPORATED
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EXAMINER	
ELAMIN, ABDELMONIEM I	
ART UNIT	**PAPER NUMBER**
2116	

NOTIFICATION DATE	DELIVERY MODE
07/19/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 13/052,516	Applicant(s) GUPTA ET AL.	
	Examiner ABDELMONIEM ELAMIN	Art Unit 2116	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2011*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-24* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-24* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08)

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-24 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Svensson, International Publication No. WO 2006/077068 A2 (cited by Applicant).

3. Claims 1, 3, 7-8, 19, 21, Svensson teaches a secondary processor [*client processor 104*] comprising system memory [*DSPXRAM 110*] and a hardware buffer [*An intermediate storage area is defined within the memory 108*] for receiving at a least a portion of an executable software

image [*this reserved block of memory is used for intermediate storage of information (code and/or data) to be transferred to the slave- private memory, see page 7, lines 5-8. On receipt of the slave's information, the second stage of the host boot loader fills the intermediate storage area with information (code and/or data) to be loaded into the slave's invisible memory (Step 216) page7, lines25-27*], the secondary processor comprising a scatter loader controller for loading the executable software image directly from the hardware buffer to the system memory [*The slave copies the contents of the intermediate storage area to appropriate locations in its slave-private memory (Step 220), thereby implementing its actual loading, see page 7, last line - page 8, line 2*];

a primary processor [*host processor102*] coupled with a memory [*non-volatile memory 106*], the memory storing the executable software image for the secondary processor [*This*

can be inferred from The first stage resets and holds the slave 104 in the reset state (Step 202) and pushes information (program instructions and/or data) (Step 204) in the usual way from the non-volatile memory 106 into the commonly visible memories 108, see page 5, lines 23-26]; and

an interface communicatively coupling the primary processor and the secondary processor via which the executable software image is received by the secondary processor [*The arrows in FIG. 1 indicate access paths, e.g., busses and DMA paths, between the CPUs and the memories. The ARM host CPU 102 can access the non-volatile memory 106 and the SARAM and DARAM 108 of the DSP, but not the DSP's XRAM 110, and the DSP slave CPU 104 can access all of the RAMs 108, 110, see page 5, lines 8-12*].

4. Claim 2, Svensson teaches the scatter loader controller is configured to load the executable software image directly from the hardware buffer to the system memory of the secondary processor without copying data between system memory locations on the secondary processor [*there is no indication that data is copied between system memory locations on the secondary processor when loading the executable software image from the hardware buffer to the system memory of the secondary processor*].

5. Claims 4-6, Svensson teaches the executable software image comprises an image header and at least one data segment [*Fig. 3, it is clear that the executable software image comprises an image header and at least one segment*].

6. Claim 9, Svensson teaches the portion of the executable software image is loaded into the system memory of the secondm$_5$, processor without an entire executable software image being stored in the hardware buffer [*This also means that a block should be split if it is larger than the*

remaining part of the intermediate storage area, and one part transferred to the intermediate storage area with the remaining part transferred in the next block. Moreover, if a block is several times larger than the intermediate storage area, it may have to be split more than once, see page 8, line 27]

7. Claims 10, 20, 22, Svensson teaches the multi-processor system is integrated into a computer [*This invention relates to initialization of electronic systems having multiple programmable processors, see page 1, line 4*].

8. Claims 11, 14-15, 17, 23, Svensson teaches receiving at a secondary processor [*client processor 104*], from a primary processor [*host processor 102*] via an inter- chip communication bus [*The arrows in FIG. 1 indicate access paths, e.g., busses and DMA paths, between the CPUs and the memories. The ARM host CPU 102 can access the non-volatile memory 106 and the SARAM and DARAM 108 of the DSP, but not the DSP's XRAM 110, and the DSP slave CPU 104 can access all of the RAMs 108, 110, see page 5, lines 8-12*], an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor, the executable software image comprising the image header and at least one data segment [*A block of code and/or data to be transferred into the intermediate storage area includes a header*];

processing, by the secondary processor, the image header to determine at least one location within system memory to which the secondary processor is coupled to store the at least one data segment [*that indicates the length of the block and where it is to be loaded in the slave memory, i.e., the destination address, see page 8, lines 15-18*];

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