

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTEL CORPORATION,  
Petitioner,

v.

QUALCOMM INCORPORATED,  
Patent Owner.

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IPR2018-01334<sup>1</sup>  
Patent 8,838,949 B2

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Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and  
AARON W. MOORE, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

JUDGMENT  
Final Written Decision  
Determining Some Challenged Claims Unpatentable  
*35 U.S.C. § 318(a)*

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<sup>1</sup> IPR2018-01335 and IPR2018-01336 have been consolidated with the instant proceeding.

## I. INTRODUCTION

In this *inter partes* review, Intel Corporation (“Petitioner”) challenges the patentability of all claims (1–23) of U.S. Patent No. 8,838,949 B2 (“the ’949 patent,” Ex. 1001), which is assigned to Qualcomm Incorporated (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 10, 11, 13–15, and 18–23 are unpatentable but that Petitioner has not proven by a preponderance of the evidence that claims 1–9, 12, 16, and 17 are unpatentable. *See* 35 U.S.C. § 316(e) (“In an *inter partes* review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.”).

### A. Procedural History

On July 3, 2018, Petitioner filed three petitions challenging claims of the ’949 patent as follows: IPR2018-01334 (claims 1–9, 22, and 23), IPR2018-01335 (claims 10–17), and IPR2018-01336 (claims 18–21). In each proceeding, Patent Owner filed a Preliminary Response. Paper 7 (in each proceeding). We instituted review in each case on all grounds presented, which are as follows:

Claims Challenged	35 U.S.C. § <sup>2</sup>	References
1–15, 22, 23	103(a)	Bauer, <sup>3</sup> Svensson, <sup>4</sup> Kim <sup>5</sup>
16, 17	103(a)	Bauer, Svensson, Kim, Zhao <sup>6</sup>
18–21	103(a)	Bauer, Svensson, Kim, Lim <sup>7</sup>

IPR2018-01334, Paper 10 (“Dec. on Inst.”), 29; IPR2018-01335, Paper 10 (“1335 Dec. on Inst.”),<sup>8</sup> 38; IPR2018-01336, Paper 10 (“1336 Dec. on Inst.”), 32.

After institution, we consolidated IPR2018-01335 and IPR2018-01336 with IPR2018-01334 and terminated IPR2018-01335 and IPR2018-01336. Paper 12.

During the trial, Patent Owner filed a Response (Paper 16, “PO Resp.”), Petitioner filed a Reply (Paper 21, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 25, “PO Sur-reply”).

An oral hearing was held on December 12, 2019, a transcript of which appears in the record. Paper 29 (“Tr.”).

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<sup>2</sup> The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. §§ 103 and 112 that became effective after the filing of the application for the ’949 patent. Therefore, we apply the pre-AIA versions of these sections.

<sup>3</sup> US 2006/0288019, published Dec. 21, 2006 (Ex. 1009).

<sup>4</sup> US 7,356,680 B2, issued Apr. 8, 2008 (Ex. 1010).

<sup>5</sup> Korean Patent Application Publication No. 10-2002-0036354, published May 16, 2002 (Ex. 1011). References to Kim in this Decision are to the English translation provided by Petitioner as Exhibit 1012.

<sup>6</sup> US 2007/0140199 A1, published June 21, 2007 (Ex. 1013).

<sup>7</sup> US 7,203,829 B2, published Apr. 10, 2007 (Ex. 1014).

<sup>8</sup> We use prefixes “1335” and “1336” to denote papers from IPR2018-01335 and IPR2018-01336, respectively. We do not use a prefix for papers from IPR2018-01334.

*B. Real Parties in Interest*

Petitioner identifies itself and Apple Inc. as real parties in interest.  
Pet. 2. Patent Owner identifies itself as the real party in interest. Paper 4, 2.

*C. The '949 Patent and Illustrative Claim*

The '949 patent generally relates to loading software from one processor to another in a multi-processor system. Ex. 1001, code (57). One example disclosed in the '949 patent involves loading modem image executable data by first retrieving and processing an image header, which “includes information used to identify where the modem image executable data is to be eventually placed into the system memory of the secondary processor.” Ex. 1001, 8:9–21. Figure 3 of the '949 patent is reproduced below.

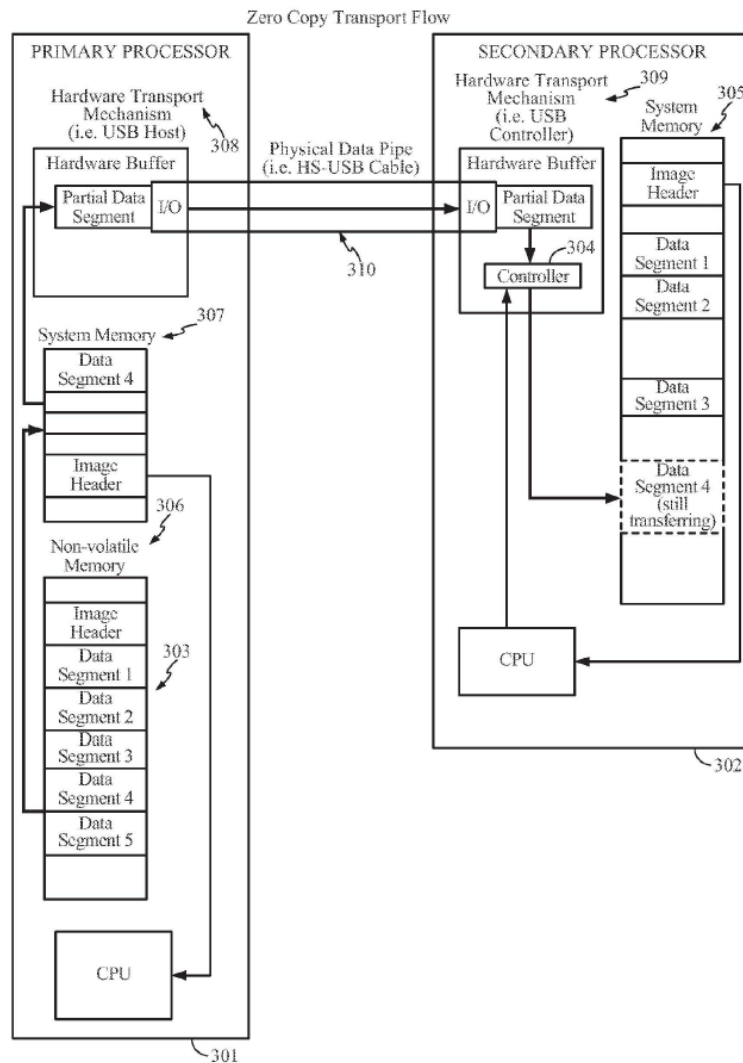


FIG. 3

Figure 3 shows “operational flow for an exemplary loading process for loading an executable image from a primary processor to a secondary processor according to one aspect of the present disclosure.” Ex. 1001, 4:10–13. Referring to various components depicted in Figure 3, the '949 patent discloses the following:

The header information is used by the secondary processor 302 to program the scatter loader/direct memory access controller 304 receive address when receiving the actual executable data. Data segments are then sent from system memory 307 to the primary hardware transport mechanism 308. The segments are

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