

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Nitin GUPTA	Customer No.: 23696
Application No.: 13/052,516	Art Unit: 2116
Filed: March 21, 2011	Conf. No.: 6620
For: DIRECT SCATTER LOADING OF EXECUTABLE SOFTWARE IMAGE FROM A PRIMARY PROCESSOR TO ONE OR MORE SECONDARY PROCESSOR IN A MULTI-PROCESSOR SYSTEM	Examiner: Abdelmoniem I. ELAMIN

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY UNDER 37 C.F.R. 1.111

Dear Sir:

In response to the Office Action dated July 19, 2013, reconsideration and further examination of the above-identified application are respectfully requested based on the following:

Amendments to the Claims are reflected in the listing of claims, which begin on page 2 of this paper.

Remarks begin on page 8 of this paper.

INTEL 1005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A multi-processor system comprising:
a secondary processor comprising:
system memory and a hardware buffer for receiving an image header and at least one data segment at a least a portion of an executable software image, the image header and each data segment being received separately, and
~~the secondary processor comprising a scatter loader controller for loading~~
configured:
to load the image header; and
to scatter load each received data segment executable software image,
based at least in part on the loaded image header, directly from the hardware buffer to the system memory;
a primary processor coupled with a memory, the memory storing the executable software image for the secondary processor; and
an interface communicatively coupling the primary processor and the secondary processor via which the executable software image is received by the secondary processor.

2. (Original) The multi-processor system of claim 1 in which the scatter loader controller is configured to load the executable software image directly from the hardware buffer to the system memory of the secondary processor without copying data between system memory locations on the secondary processor.

3. (Original) The multi-processor system of claim 1 in which raw image data of the executable software image is received by the secondary processor via the interface.

4. (Cancelled)

5. (Currently Amended) The multi-processor system of claim [[4]] 1 in which the secondary processor is configured to ~~receive the image header and~~ process the image header to determine at least one location within the system memory to store the at least one data segment.

6. (Original) The multi-processor system of claim 5 in which the secondary processor is configured to determine, based on the received image header, the at least one location within the system memory to store the at least one data segment before receiving the at least one data segment.

7. (Original) The multi-processor system of claim 1, in which the secondary processor further comprises a non-volatile memory storing a boot loader that initiates transfer of the executable software image for the secondary processor.

8. (Original) The multi-processor system of claim 1 in which the primary and secondary processors are located on different chips.

9. (Original) The multi-processor system of claim 1 in which the portion of the executable software image is loaded into the system memory of the secondary processor without an entire executable software image being stored in the hardware buffer.

10. (Original) The multi-processor system of claim 1 integrated into at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

11. (Currently Amended) A method comprising:
receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor, the executable software image comprising the image header and at least one data segment, the image header and each data segment being received separately;
processing, by the secondary processor, the image header to determine at least one location within system memory to which the secondary processor is coupled to store ~~the at least one~~ each data segment;
receiving at the secondary processor, from the primary processor via the inter-chip communication bus, ~~the at least one~~ each data segment; and
scatter loading, by the secondary processor, the at least one each data segment directly to the determined at least one location within the system memory, and each data segment being scatter loaded based at least in part on the processed image header.
12. (Original) The method of claim 11 further comprising booting the secondary processor using the executable software image.
13. (Original) The method of claim 11 further comprising loading the executable software image directly from a hardware buffer to the system memory of the secondary processor without copying data between system memory locations.
14. (Original) The method of claim 11 in which the processing occurs prior to the loading.
15. (Original) The method of claim 11 in which the primary and secondary processors are located on different chips.

16. (Original) The method of claim 11 further comprising performing the receiving, processing, and loading, in at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

17. (Currently Amended) An apparatus comprising:

means for receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor, the executable software image comprising the image header and at least one data segment, the image header and each data segment being received separately;

means for processing, by the secondary processor, the image header to determine at least one location within system memory to which the secondary processor is coupled to store ~~the at least one~~ each data segment;

means for receiving at the secondary processor, from the primary processor via the inter-chip communication bus, ~~the at least one~~ each data segment; and

means for scatter loading, by the secondary processor, ~~the at least one~~ each data segment directly to the determined at least one location within the system memory, and each data segment being scatter loaded based at least in part on the processed image header.

18. (Original) The apparatus of claim 17 integrated into at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

19. (Currently Amended) A multi-processor system comprising:

a primary processor coupled with a first non-volatile memory, the first non-volatile memory coupled to the primary processor and storing a file system for the primary processor and executable images for the primary processor and secondary processor;

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