UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.

Before the Honorable Thomas B. Pender
Administrative Law Judge

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In the Matter of

CERTAIN MOBILE ELECTRONIC DEVICES AND RADIO FREQUENCY AND PROCESSING COMPONENTS THEREOF

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Investigation No. 337-TA-1065

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JOINT CLAIM CONSTRUCTION CHART

Pursuant to Ground Rule 8.3 and the Procedural Schedule governing this Investigation (Order No. 7), Complainant Qualcomm Incorporated ("Qualcomm"), Respondent Apple Inc. ("Apple"), and the Commission Investigative Staff ("Staff") provide the following Joint Claim Construction Chart. The parties identify the following ten claim terms as most significant to the resolution of the case:

1. "based on" ('558 patent)

2. "current sense amplifier" ('558 patent)

3. "envelope signal" ('558 patent)

4. "plurality of carrier aggregated transmit signals being sent simultaneously" ('675 patent)

5. "power tracker" ('675 patent)

6. "single power tracking signal" ('675 patent)

7. "means for receiving at a secondary processor, from a primary processor via an interchip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor" ('949 patent)

8. "means for receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment" ('949 patent)

9. "programmable streaming processor" ('936 patent)

10. "(conversion / executable) instruction(s) [to]… convert[] graphics data … [from a] (first / second / different) data precision [to a] … (second / first / indicated) data precision" ('936 patent)

'949 Patent

Claim Term	Complainant's Construction	Apple's Construction	Staff's Construction
"scatter load[ing] . . . each [received] data segment directly to . . . system memory" (claims 10-14, 16, 20, 22)	"transfer[ring] each [received] data segment to separate location(s) within system memory without first storing a copy of the entire image in an intermediate storage area" (**same as Staff's construction**)	Indefinite	"transfer[ring] each [received] data segment to separate location(s) within system memory without first storing a copy of the entire image in an intermediate storage area" (**same as Qualcomm's construction**)
"image header" (claims 1, 4, 5, 10, 16, 20, 22) (**AGREED**)	"a header associated with the entire image that specifies where the data segments are to be placed in the system memory"		

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Claim Term	Complainant's Construction	Apple's Construction	Staff's Construction
"means for receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor" (claim 16) (35 U.S.C. § 112 ¶ 6)	**Function:** receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor **Structure:** a modem processor, or a controller in the modem processor, and equivalents thereof (*see* '949 patent at 4:58-5:43, 5:59-6:39, 7:60-10:44, 11:1-10, and Figs. 1-3)	**Function:** receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor **Structure:** a secondary processor connected to a primary processor via an interface for a USB-based High Speed Inter-Chip (HSIC) bus, a MIPI High Speed Synchronous Interface (HSI) bus, a Secure Digital I/O Interface (SDIO) bus, a Universal Asynchronous Receiver/Transmitter (UART) bus, a Serial Peripheral Interface (SPI) bus, or an Inter-Integrated Circuit (I2C) bus, and equivalents thereof, as described at column 5, lines 35-43, and shown in Figure 3	
"means for processing, by the secondary processor,	**Function**: processing, by the secondary processor, the image header to determine at least one	**Function**: processing, by the secondary processor, the image header to determine at least one	**Function**: processing, by the secondary processor, the image header to determine at least one

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Claim Term	Complainant's Construction	Apple's Construction	Staff's Construction
the image header to determine at least one location within system memory to which the secondary processor is coupled to store each data segment" (claim 16) (35 U.S.C. § 112 ¶ 6)	location within system memory to which the secondary processor is coupled to store each data segment **Structure**: a modem processor coupled to system memory, and equivalents thereof, as described in the '949 patent at 3:9-12, 4:58-5:43 & Fig. 1, 5:59-6:39 & Fig. 2, 7:60-10:44 & Fig. 3, 8:50-56, and 9:27-41 **(same as Staff's construction)**	location within system memory to which the secondary processor is coupled to store each data segment **Structure**: indefinite	location within system memory to which the secondary processor is coupled to store each data segment **Structure**: a modem processor coupled to system memory, and equivalents thereof, as described in the '949 patent at 3:9-12, 4:58-5:43 & Fig. 1, 5:59-6:39 & Fig. 2, 7:60-10:44 & Fig. 3, 8:50-56, and 9:27-41 **(same as Qualcomm's construction)**
"means for receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment" (claim 16)	**Function:** receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment **Structure:** a modem processor, or a controller in the modem processor, and equivalents thereof	**Function**: receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment **Structure**: a secondary processor connected to a primary processor via an interface for a USB-based High Speed Inter-Chip (HSIC) bus, a MIPI High Speed Synchronous Interface (HSI) bus, a Secure Digital I/O Interface (SDIO) bus, a Universal Asynchronous Receiver/Transmitter (UART) bus, a Serial Peripheral Interface (SPI) bus, or an Inter-Integrated Circuit (I2C) bus, and equivalents thereof, as described at	

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