UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Intel Corporation,
Petitioner,

v.

Qualcomm Incorporated,
Patent Owner

Case IPR2018-01334[1]
U.S. Patent No. 8,838,949

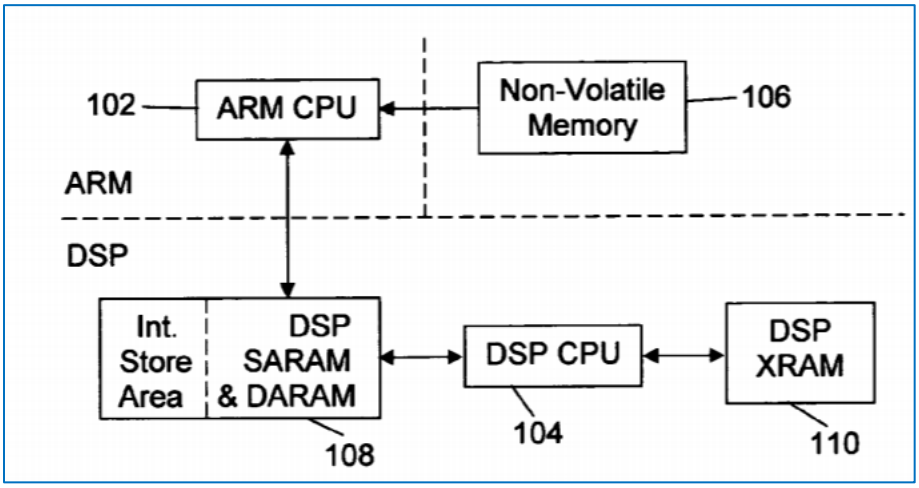
PATENT OWNER SUR-REPLY

[1] IPR2018-01335 and IPR2018-01336 have been consolidated with the instant proceeding.

Table of Contents

I. Introduction

Petitioner's reply introduces unpersuasive arguments that cannot salvage the petitions. The thrust of Petitioner's unpatentability argument is that the intermediate storage area of Bauer/Svensson is not "system memory," and therefore data is loaded "directly" to the DSP XRAM (*i.e.*, the alleged "system memory") despite the data being temporarily buffered in the intermediate storage area. *See*, *e.g.*, Paper 21 at 34-35.



Ex. 1010 (Svensson) at Fig. 1.

But this is erroneous because the intermediate storage area of Bauer/Svensson is indistinguishable from the temporary buffer in system memory that is described in the Background section of the '949 patent. Ex. 1001 at 2:14-41. Both are temporary buffers that are *allocated at run time* and used to hold data that is subsequently transferred to a final destination in system memory:

> ***Ex. 1001 ('949 Background) at 2:23-34***: "[O]ne way of performing such loading is to *allocate a temporary buffer* …. From the temporary buffer, … the payload would get copied over to the final destination [in system memory]. The *temporary buffer would be some place in system memory*."
>
> ***Ex. 1010 (Svensson) at 5:21-28:*** "The idle *process reserves a block of memory in the slave's heap of memory* … [in] 'internal' memory 108 (Step 212). … [T]his reserved block of memory is used for intermediate storage of information (code and/or data) to be transferred to the … 'external' XRAM 110."

See Section III.C below. The combination of Bauer and Svensson thus describes the prior-art temporary buffering operation that the invention of the '949 patent seeks to avoid, and therefore *does not* disclose loading data segments directly to system memory, as required by all of the challenged claims.

The Board should confirm the patentability of claims 1-23 for this reason and those explained below.

II. Claim Construction

A. "System Memory"

Qualcomm showed in its response that the claim term "system memory" should be interpreted to mean "memory that is addressable by the secondary processor." Paper 16 at 9-12. On reply, Petitioner disagrees and argues that the term should be construed as "memory where an executable software image can be loaded and executed." Paper 21 at 6. The Board should reject Petitioner's construction and adopt Qualcomm's for the reasons explained below. But even if the Board were to

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